Radiation Tolerant Multicell Battery Monitor

FEATURES

- **15kRad (SI) Total Ionizing Dose (TID) per MIL-STD-883 TM1019 Condition A**
- **Single Event Effect (LET) Threshold Linear Energy Transfer (LET) ≥ 21.17MeV-cm^2/mg**
- **Processed Using MIL-PRF-38535 Class N and PEM-INST-001 as a Guideline**
- **TID and SEE Reports Available**
- **Measures Up to 12 Battery Cells in Series**
- **Stackable Architecture Supports 100s of Cells**
- **Built-In isoSPI™ Interface:**
  - **1Mbps Isolated Serial Communications**
  - **Uses a Single Twisted Pair, Up to 100 Meters**
  - **Low EMI Susceptibility and Emissions**
- **1.2mV Maximum Total Measurement Error**
- **290µs to Measure All Cells in a System**
- Synchronized Voltage and Current Measurement
- 16-Bit Delta-Sigma ADC with Frequency Programmable 3rd Order Noise Filter
- Engineered for ISO26262 Compliant Systems
- Passive Cell Balancing with Programmable Timer

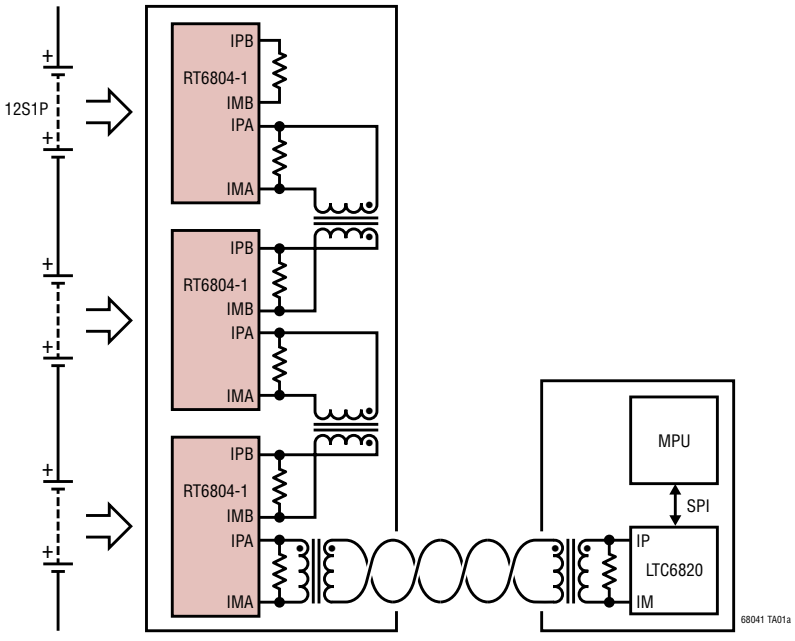
DESCRIPTION

The RT®6804 is a 3rd generation multicell battery stack monitor that measures up to 12 series connected battery cells with a total measurement error of less than 1.2mV. The cell measurement range of 0V to 5V makes the RT6804 suitable for most battery chemistries. All 12 cell voltages can be captured in 290µs, and lower data acquisition rates can be selected for high noise reduction.

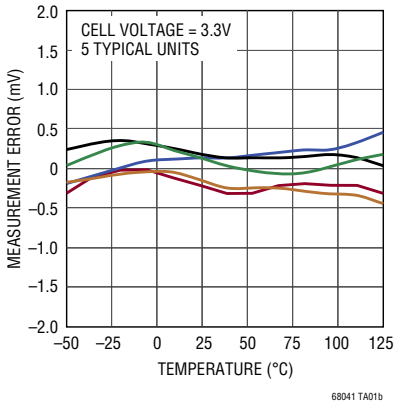
Multiple RT6804 devices can be connected in series, permitting simultaneous cell monitoring of long, high voltage battery strings. The RT6804 has an isoSPI interface for high speed, RF-immune, local area communications. Using the RT6804-1, multiple devices are connected in a daisy-chain with one host processor connection for all devices.

Additional features include passive balancing for each cell, an on-board 5V regulator, and 5 general purpose I/O lines. In sleep mode, current consumption is reduced to 4µA. The RT6804 can be powered directly from the battery, or from an isolated supply.

TYPICAL APPLICATION



Total Measurement Error vs Temperature of 5 Typical Units



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage V^+ to V^- 75V
Input Voltage (Relative to V^-)
- C0 ..... –0.3V to 0.3V
- C12 ..... –0.3V to 75V
- C(n) ..... –0.3V to MIN (8 • n, 75V)
- S(n) ..... –0.3V to MIN (8 • n, 75V)
- IPA, IMA, IPB, IMB ..... –0.3V to V_{REG} + 0.3V
- DRIVE Pin ..... –0.3V to 7V
- All Other Pins ..... –0.3V to 6V

Voltage Between Inputs
- V^+ to C12 ..... –5.5V
- C(n) to C(n – 1) ..... –0.3V to 8V
- S(n) to C(n – 1) ..... –0.3V to 8V
- C12 to C8 ..... –0.3V to 25V
- C8 to C4 ..... –0.3V to 25V
- C4 to C0 ..... –0.3V to 25V

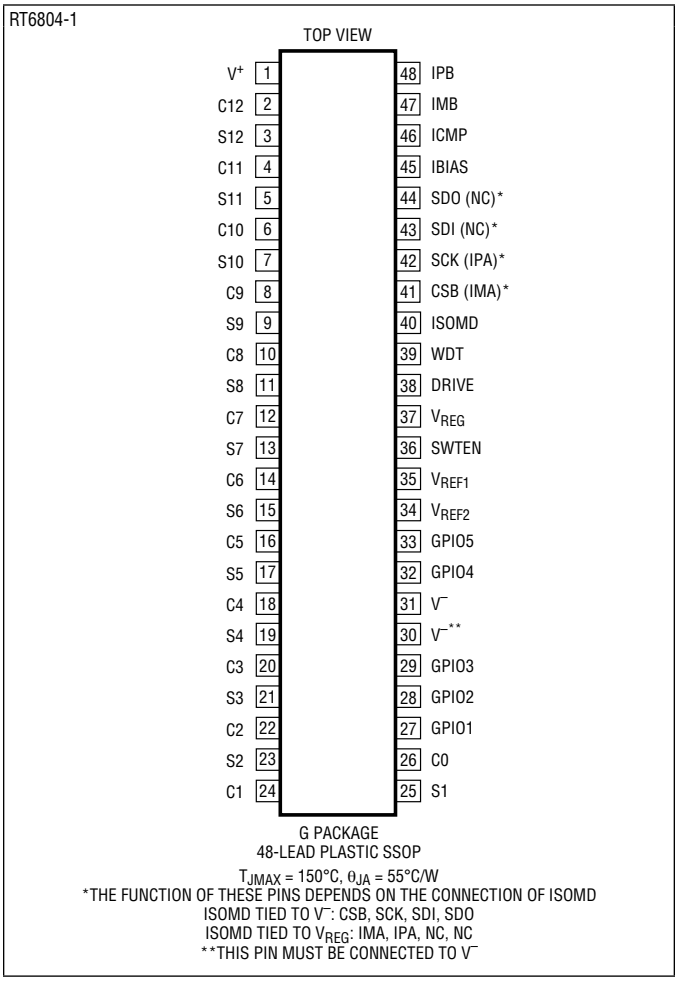
Current In/Out of Pins
- All Pins Except V_{REG}, IPA, IMA, IPB, IMB, S(n) .. 10mA
- IPA, IMA, IPB, IMB 30mA

Operating Temperature Range
- RT6804H ..... –40°C to 125°C

Specified Temperature Range
- RT6804H ..... –40°C to 125°C

Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

PIN CONFIGURATION



G PACKAGE
48-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 55°C/W

*THE FUNCTION OF THESE PINS DEPENDS ON THE CONNECTION OF ISOMD
ISOMD TIED TO V^-: CSB, SCK, SDI, SDO
ISOMD TIED TO V_{REG}: IMA, IPA, NC, NC
**THIS PIN MUST BE CONNECTED TO V^-

ORDER INFORMATION

LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
RT6804HG-1	RT6804HG-1#TR	RT6804G-1	48-Lead Plastic SSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS (Pre-Irradiation)

Specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		T_A = 25°C MIN	TYP	MAX	SUB-GROUP	−40°C ≤ T_A ≤ 125°C MIN	TYP	MAX	SUB-GROUP	UNITS
ADC DC Specifications												
	Total Measurement Error (TME) in Normal Mode	C(n) to C(n-1) = 2.0		−0.8	±0.1	0.8	1	−1.4		1.4	2, 3	mV
		GPIO(n) to V^- = 2.0		−1.4		1.4	1	−1.4		1.4	2, 3	mV
		C(n) to C(n-1) = 3.3		−1.2	±0.2	1.2	1	−2.2		2.2	2, 3	mV
		GPIO(n) to V^- = 3.3		−2.2		2.2	1	−2.2		2.2	2, 3	mV
		C(n) to C(n-1) = 4.2		−1.6	±0.3	1.6	1	−2.8		2.8	2, 3	mV
		GPIO(n) to V^- = 4.2		−2.8		2.8	1	−2.8		2.8	2, 3	mV
		VREG Pin		−0.25	±0.1	0.25	1	−0.25	±0.1	0.25	2, 3	%
	Total Measurement Error (TME) in Filtered Mode	VREG Pin		−0.25	±0.1	0.25	1	−0.25	±0.1	0.25	2, 3	%
I_L	Input Leakage Current When Inputs Are Not Being Measured	C(n), n = 0 to 12		−250	10	250	1	−250	10	250	2, 3	nA
		GPIO(n), n = 1 to 5		−250	10	250	1	−250	10	250	2, 3	nA
Voltage Reference Specifications												
V_{REF1}	1st Reference Voltage	VREF1 Pin, No Load		3.1	3.2	3.3	1	3.1	3.2	3.3	2, 3	V
V_{REF2}	2nd Reference Voltage	VREF2 Pin, No Load		2.99		3.01	1	2.99		3.01	2	V
General DC Specifications												
I_{VP}	V+ Supply Current	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 0V		3.8	6	1		3.8	10	2	µA
			V_{REG} = 5V		1.6	3	1		1.6	5	2	µA
		State: Core = STANDBY		18	32	50	1	10	32	60	2, 3	µA
		State: Core = REFUP or MEASURE		0.4	0.55	0.7	1	0.375	0.55	0.725	2, 3	mA
$I_{REG(CORE)}$	V_{REG} Supply Current	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 5V		2.2	4	1		2.2	6	2	µA
		State: Core = STANDBY		10	35	60	1	6	35	65	2, 3	µA
		State: Core = REFUP		0.2	0.45	0.7	1	0.15	0.45	0.7	2, 3	mA
		State: Core = MEASURE		10.8	11.5	12.2	1	10.7	11.5	12.2	2, 3	mA
	DRIVE output Voltage	Sourcing 1µA		5.4	5.6	5.8	1	5.2	5.6	6.1	2, 3	V
	Discharge Switch ON Resistance	V_{CELL} = 3.6V			10	25	1		10	25	2	Ω
SPI Interface DC Specifications												
$I_{LEAK(DIG)}$	Digital Input Current	Pins CSB, SCK, SDI,ISOMD, SWTEN, A0 to A3		−1		1	1	−1		1	2, 3	µA
isoSPI DC Specifications												
V_{BIAS}	Voltage on IBIAS Pin	READY/ACTIVE State		1.9	2	2.1	1	1.9	2	2.1	2, 3	V
A_{IB}	Isolated Interface Current Gain	V_A ≤ 1.6V	I_B = 1mA	18	20	22	1	18	20	22	2, 3	mA/mA
isoSPI Pulse Timing Specifications												
$t_{1/2PW(D)}$	Data Half-Pulse Width			40	50	60	4	40	50	60	5, 6	ns

ELECTRICAL CHARACTERISTICS (Post-Irradiation)

Specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		10kRad (SI) MIN	10kRad (SI) MAX	15kRad (SI) MIN	15kRad (SI) MAX	UNITS
ADC DC Specifications								
	Total Measurement Error (TME) in Normal Mode	C(n) to C(n-1) = 2.0		–1.8	1.8	–2.6	2.6	mV
		GPIO(n) to V^- = 2.0		–2.4	2.4	–3.2	3.2	mV
		C(n) to C(n-1) = 3.3		–2.6	2.6	–4.0	4.0	mV
		GPIO(n) to V^- = 3.3		–3.6	3.6	–5.0	5.0	mV
		C(n) to C(n-1) = 4.2		–3.4	3.4	–5.3	5.3	mV
		GPIO(n) to V^- = 4.2		–4.6	4.6	–6.5	6.5	mV
		VREG Pin		–17.5	17.5	–31.5	31.5	mV
	Total Measurement Error (TME) in Filtered Mode	VREG Pin		–16.5	16.5	–32.5	32.5	mV
I_L	Input Leakage Current When Inputs Are Not Being Measured	C(n), n = 0 to 12		–360	360	–360	360	nA
		GPIO(n), n = 1 to 5		–360	360	–360	360	nA
Voltage Reference Specifications								
V_{REF1}	1st Reference Voltage	VREF1 Pin, No Load		3.10	3.30	3.10	3.30	V
V_{REF2}	2nd Reference Voltage	VREF2 Pin, No Load		2.98	3.01	2.98	3.01	V
General DC Specifications								
I_{VP}	V^+ Supply Current	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 0V		15		325	µA
			V_{REG} = 5V		3.6		100	µA
		State: Core = STANDBY			140		180	µA
		State: Core = REFUP or MEASURE		0.3	0.8	0.3	0.8	mA
$I_{REG(CORE)}$	V_{REG} Supply Current	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 5V		425		2800	µA
		State: Core = STANDBY			475		3000	µA
		State: Core = REFUP		0.1	1.2	0.1	3.3	mA
		State: Core = MEASURE		10.4	12.6	8.6	14.4	mA
	DRIVE Output Voltage	Sourcing 1µA		5.3	5.9	5.3	5.9	V
	Discharge Switch ON Resistance	V_{CELL} = 3.6V			27		27	Ω
SPI Interface DC Specifications								
$I_{LEAK(DIG)}$	Digital Input Current	Pins CSB, SCK, SDI,ISOMD, SWTEN, A0 to A3		–1.15	1.15	–1.25	1.25	µA
isoSPI DC Specifications								
V_{BIAS}	Voltage on IBIAS Pin	READY/ACTIVE State		1.8	2.2	1.8	2.2	V
A_{IB}	Isolated Interface Current Gain	$V_A \le 1.6V$	I_B = 1mA	17	23	17	23	mA/mA
isoSPI Pulse Timing Specifications								
$t_{1/2PW(D)}$	Data Half-Pulse Width			39	61	38	62	ns

ELECTRICAL CHARACTERISTICS: BURN-IN DELTA PARAMETERS

Specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS	DELTA LIMITS MIN	DELTA LIMITS MAX	UNITS
V_{REF1}	1st Reference Voltage	VREF1 Pin, No Load	–5	5	mV
V_{REF2}	2nd Reference Voltage	VREF2 Pin, No Load	–5	5	mV
I_{VP}	V^+ Supply Current	State: Core = STANDBY	–0.5	0.5	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error specification.

Note 3: V^+ needs to be greater than or equal to the highest C(n) voltage for accurate measurements.

ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6
Group A Test Requirements (Method 5005)	1,2,3,4,5,6
Group B and D for Class S, and End Point Electrical Parameters (Method 5005)	1,2,3

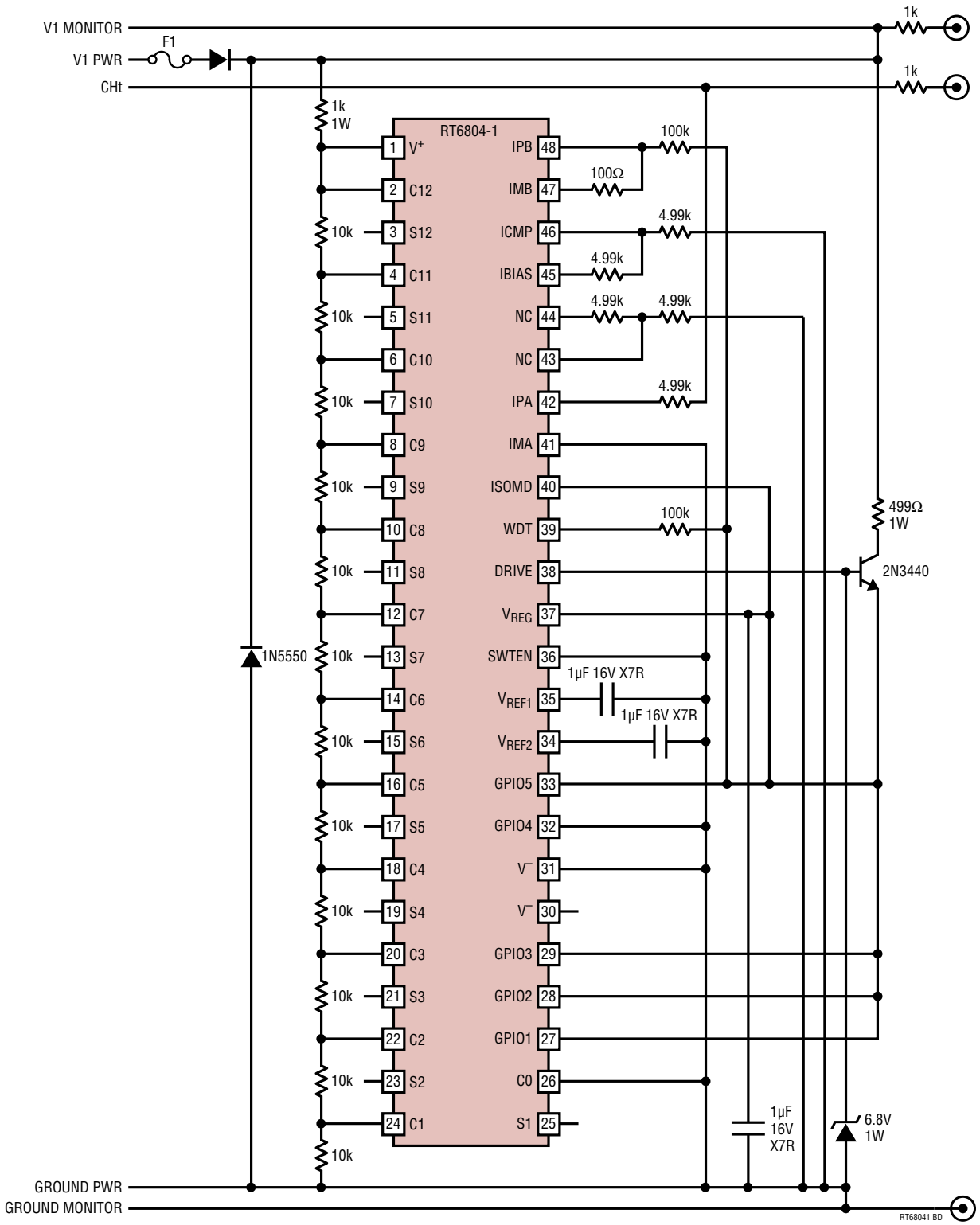
*PDA applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

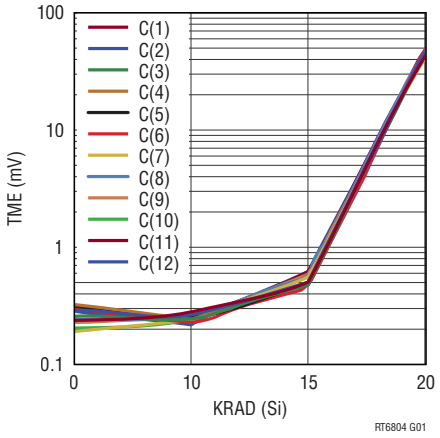
Analog Devices reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT/BURN-IN CIRCUIT

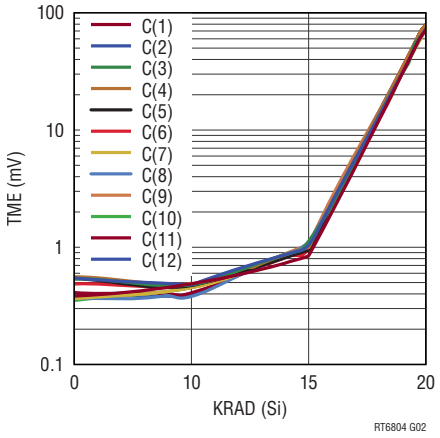


TYPICAL PERFORMANCE CHARACTERISTICS

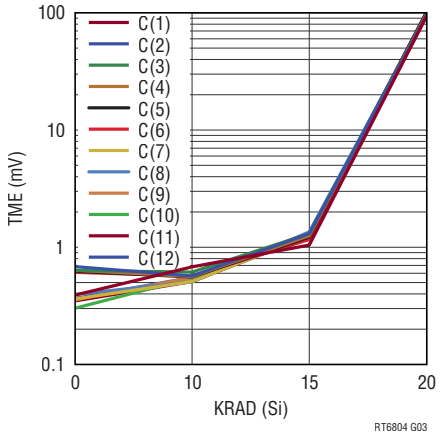
TME in Normal Mode
C(n) to C(n-1) =2V



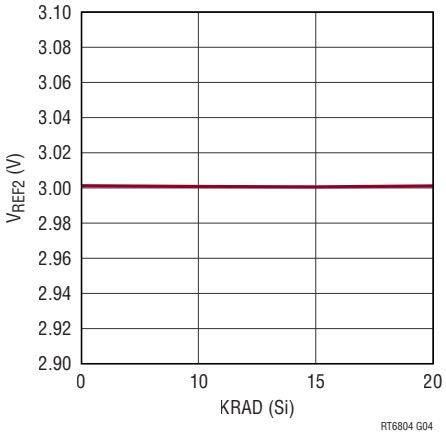
TME in Normal Mode
C(n) to C(n-1) = 3.3V



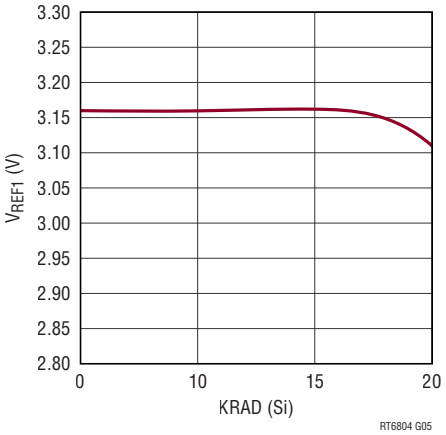
TME in Normal Mode
C(n) to C(n-1) = 4.2V



Reference Voltage 2, V_{REF2},
V_{REG} = 5V

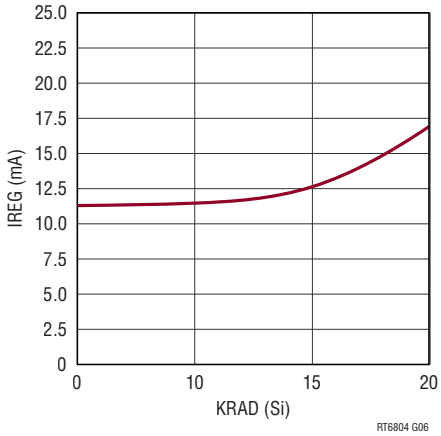


Reference Voltage 1, V_{REF1},
V_{REG} = 5V

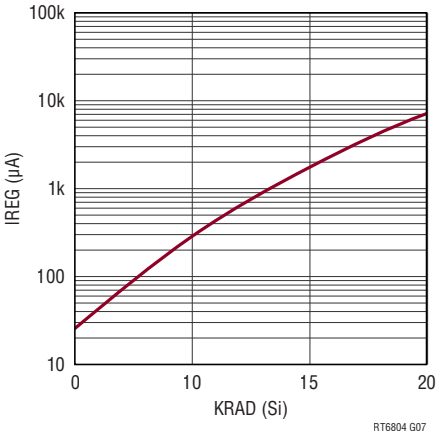


TYPICAL PERFORMANCE CHARACTERISTICS

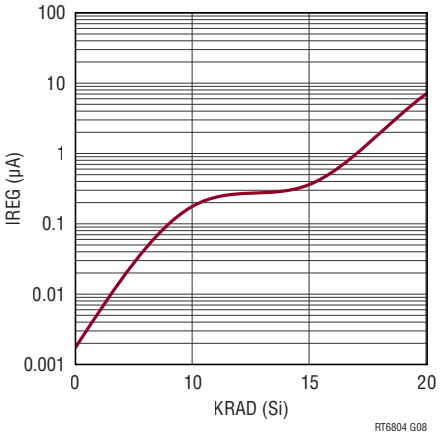
IREG, Core = MEASURE



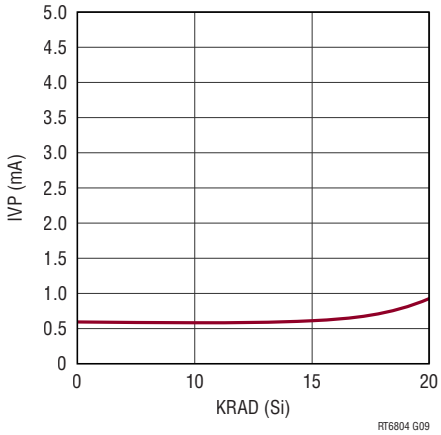
IREG, Core = STANDBY



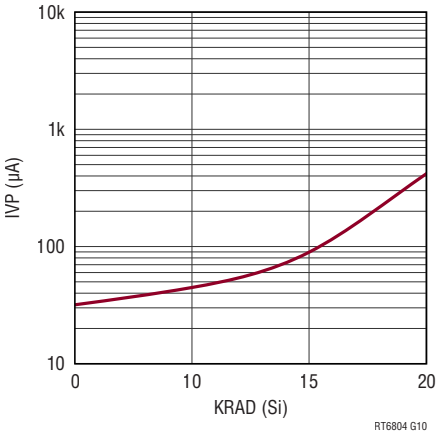
IREG Core = SLEEP, V_{REG} = 5V



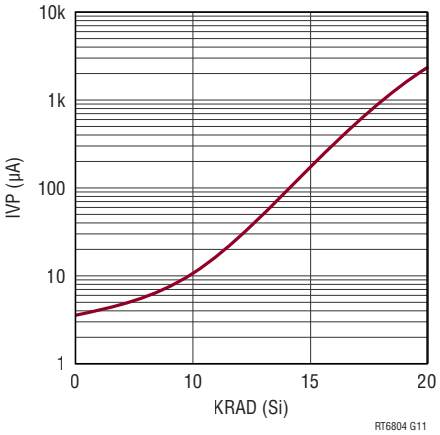
IVP, Core = MEASURE



IVP, Core = STANDBY



IVP, Core = SLEEP, V_{REG} = 0V

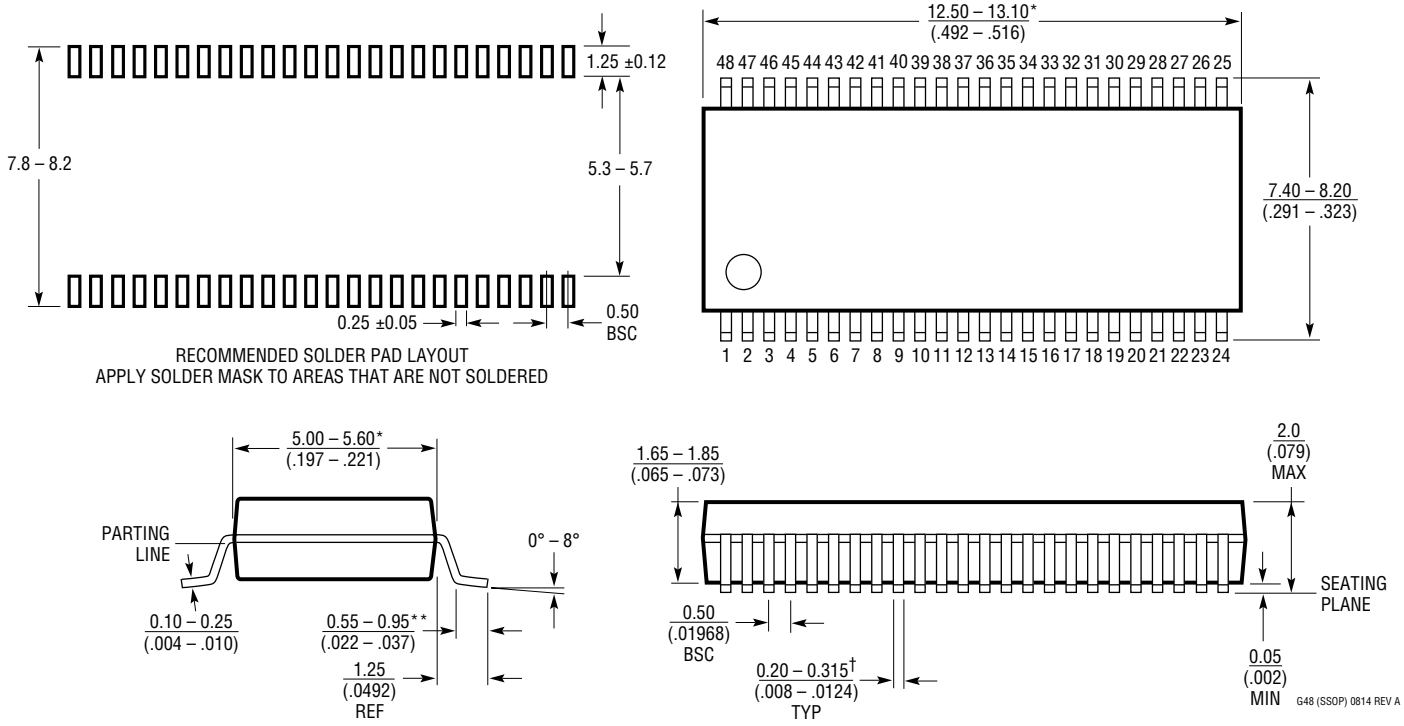


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/20	Increased Post 15kRad (Si) V^+ Supply Current State: Core = SLEEP, isoSPI = IDLE V_{REG} = 5V to 100 µA	4

PACKAGE DESCRIPTION

G Package
48-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1887 Rev A)



NOTE:
1.DRAWING IS NOT A JEDEC OUTLINE
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
4. DRAWING NOT TO SCALE
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH SHALL NOT EXCEED .15mm PER SIDE

**LENGTH OF LEAD FOR SOLDERRING TO A SUBSTRATE

†THE MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS DO NOT EXCEED 0.13mm PER SIDE