

BCD Output Synchro-to-Digital Converters

SBCD1752/1753/1756/1757

FEATURES

BCD (Binary Coded Decimal) Output Representing 0 to 359.9° or 0 to ±179.9°

-15V Power Supply Requirement Optional

High Tracking Rate (75 revs/sec)

Internal Microtransformers for 60Hz, 400Hz and 2.6kHz Options

Voltage Scaling with External Resistors (Unique Feature)
Transformer Isolated Outputs

Low Cost

MIL Spec/Hi Rel Options Available

APPLICATIONS

Visual Display of Angular Information

Valve Position Indication
Antenna Monitoring

Industrial Controls

GENERAL DESCRIPTION

The SBCD1752, SBCD1753, SBCD1736 and the SBCD1757 are modular, continuous tracking Synchro/Resolver-to-Digital converters which employ a type 2 servo loop.

They are intended for use in both Industrial and Military applications either for displaying angular data directly, or for inputting BCD information directly into a data processing system.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in parallel Binary Coded Decimal (BCD).

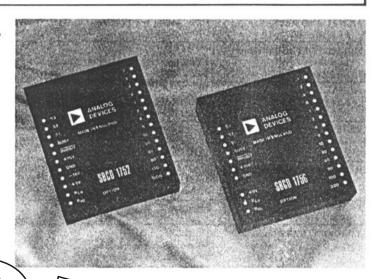
Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

One of the outstanding features of these converters is the use made of precision Scott T and reference microtransformers. This has made it possible to include the transformers within the module, even for the 60Hz version as well as providing facilities for external voltage scaling.

MODELS AVAILABLE

The four Synchro-to-Digital converters described in this data sheet, differ primarily in the areas of output format and power supply requirements.

Model <u>SBCD1752XYZ</u> is a 13-bit plus sign, BCD output converter, giving -180.0° to -0.1° and +0.0 to $+179.9^{\circ}$ requiring $\pm 15V$ and +5V power supplies, and having an overall accuracy of ± 0.2 Degrees.



Model \$BQD1753XYZ is a 14-bit, BCD output converter, giving 0 to 359.9°, requiring ±15V and +5V power supplies, and having an overall acqueacy of 70.2 Degrees.

Model SBCD1756X/Z s. 2 13-bit plus sign, BCD putput converter, giving -180.0° to -0.1° and +0.0 to +179.9° requiring +15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

Model <u>SBCD1757XYZ</u> is a 14-bit, BCD output converter, giving 0 to 359.9°, requiring +15V and 45V power supplies, and having an overall accuracy of ±0.2 Degrees.

The XYZ code defines the option thus:

X signifies the operating temperature range.

Y signifies the reference frequency.

Z signifies the input voltage and range and whether it will accept Synchro or Resolver information.

More information about the option code is given under the heading "Ordering Information".

DATA TRANSFER (ALL MODELS)

The readiness of the converters for data transfer is indicated by the state of the BUSY pin. The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the option (see Specifications table). The converter is busy when the BUSY pin is at TTL "High" level. The pulses occur for increasing and decreasing counts.

The most suitable time for transferring data is 400ns after the tra:ling edge of the BUSY pulse, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.

(typical at 25°C unless otherwise stated)

MODELS	SBCD1752	SBCD1753	SBCD1756	SBCD1757	
ACCURACY ¹ (max Error) All Frequency Options	±0.2 Degrees				
OUTPUT	Parallel BCD, 8TTL Loads	•	•	•	
RESOLUTION	13-Bit + Sign Representing -180.0° to -0.1° and +0.0° to +179.9°	14 Bit Representing 0 to 359.9°	•	••	
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz and 2.6kHz	•	•	•	
SIGNAL VOLTAGE (Line to Lin	ne)			· · · · · · · · · · · · · · · · · · ·	
Low Level High Level	11.8V rms 90.0V rms	:	:	:	
SIGNAL IMPEDANCES		100			
Low Level High Level	26k Ω (Resistive) 200k Ω (Resistive)	:	:	:	
REFERENCE VOLTAGE					
Low Level High Level	26V (11.8V Signal) 115V (90V Signal)	:	:		
REFERENCE IMPEDANCE	1134 (204 Signal)				-
Low Level	56kΩ (Resistive)				
High Level	270kΩ (Resistive)		•	•	
TRANSFORMER ISOLATION	500V dc		*:	*	
TRACKING RATE (min)	N 600000 3890 28 11 30 1891 20	999			
60Hz 400Hz 2.8kHz	5 Revolutions Per Second 6 Revolutions Per Second 75 Revolutions Per Second	:	:		-
Accel. Constant Ka	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\				
400Hz 2.6kHz	2000/sec ² 120,000/sec ² 600,000/sec ²		: ~	:	
400Hz 2.6kHz	120,000/sec ²				
2.6kHz 2.6kHz STEP RESPONSE (179° Step) (For 0.1° Error) 60Hz 400Hz 2.6kHz	120,0007 sc ² 640,000/sec 1.5sec 125ms		+15V@8/mA		
2.6kHz 2.6kHz STEP RESPONSE (179° Step) (For 0.1° Error) 60Hz 400Hz 2.6kHz	1.5sec 125ms 50ms		+ 5V @ 80mA +5V @ 500mA		
2.6kHz 2.6kHz STEP RESPONSE (179° Step) (For 0.1° Error) 60Hz 400Hz 2.6kHz	1.5sec 125ms 50ms +15V @ 25mA				
STEP RESPONSE (179° Step) (For 0.1° Error) 60Hz 400Hz 2.6kHz	1.5sec 125ms 50ms +15V @ 25mA				
STEP RESPONSE (179° Step) (For 0.1° Error) 60Hz 400Hz	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA +5V @ 500mA 3.25 Watts		+5V @ 500mA	7	
2.6kHz 2.6kHz 2.6kHz STEP RESPONSE (179° Step) (For 0.1° Error) 60Hz 400Hz 2.6kHz POWER LINES POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA +5V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5µs		+5V @ 500mA	7	
2.6kHz 2.6kHz STEP RESPONSE (179° Step) (For 0.1° Error) 60Hz 400Hz 2.6kHz POWER LINES POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 400Hz	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA +5V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5µs 0.5 to 1.25µs		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA +5V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5µs		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA +5V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5µs 0.5 to 1.25µs		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity) 60Hz	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA +5V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5µs 0.5 to 1.25µs 0.5 to 1.25µs		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity) 60Hz 400Hz	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA -15V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5µs 0.5 to 1.25µs 0.5 to 1.25µs 0.5 to 1.25µs		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity) 60Hz 400Hz 2.6kHz	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA -15V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5μs 0.5 to 1.25μs 0.5 to 1.25μs 0.5 to 1.25μs		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity) 60Hz 400Hz 2.6kHz INHIBIT INPUT (To Inhibit)	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA -15V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5µs 0.5 to 1.25µs 0.5 to 1.25µs 0.5 to 1.25µs 1.5µs		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity) 60Hz 400Hz 2.6kHz INHIBIT INPUT (To Inhibit)	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA -15V ® 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5μs 0.5 to 1.25μs 0.5 to 1.25μs 0.5 to 1.25μs 0.5 to 1.25μs		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity) 60Hz 400Hz 2.6kHz INHIBIT INPUT (To Inhibit) TEMPERATURE RANGE Operating	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA -15V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5μs 0.5 to 1.25μs 0.5 to 1.25μs 0.5 to 1.25μs 40μs 5.0μs 1.8μs Logic "0" 1TTL Load 0 to +70°C Standard -55°C to +105°C Extended		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity) 60Hz 400Hz 2.6kHz INHIBIT INPUT (To Inhibit) TEMPERATURE RANGE Operating Storage	1.5sec 1.5sec 1.25ms 50ms +15V @ 25mA -15V @ 25mA -15V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5μs 0.5 to 1.25μs 0.5 to 1.25μs 0.5 to 1.25μs 1.8μs Logic "0" 1TTL Load 0 to +70°C Standard -55°C to +105°C Extended -55°C to +125°C		+5V @ 500mA	7	
POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz POWER DISSIPATION BUSY LOGIC OUTPUT, POSITI 60Hz 400Hz 2.6kHz MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity) 60Hz 400Hz 2.6kHz INHIBIT INPUT (To Inhibit) TEMPERATURE RANGE Operating	1.5sec 1.5sec 125ms 50ms +15V @ 25mA -15V @ 25mA -15V @ 500mA 3.25 Watts IVE PULSE (1 TTL Load) 3.5 to 4.5μs 0.5 to 1.25μs 0.5 to 1.25μs 0.5 to 1.25μs 40μs 5.0μs 1.8μs Logic "0" 1TTL Load 0 to +70°C Standard -55°C to +105°C Extended		+5V @ 500mA 3.7 Watts		

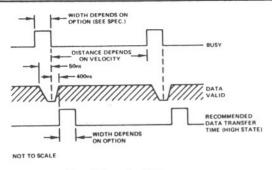
Specifications subject to change without notice.

NOTES

1 Specified over the appropriate operating temperature range and for
(a) ±10% signal and reference amplitude variation
(b) 10% signal and reference harmonic distortion
(c) ±5% power supply variation
(d) ±10% variation in reference frequency.

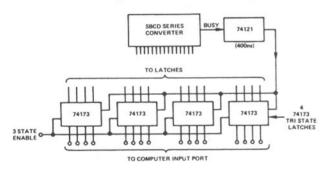
^{*}Specifications same as SBCD1752
**Specifications same as SBCD1753
***Specifications same as SBCD1756

Applying the SBCD1752/1753/1756/1757



Data Transfer Diagram

The function of the INHIBIT pin is to enable the user to inhibit the update of the converter's output counter. This is achieved by taking the INHIBIT pin to a TTL Logic zero. If used, the INHIBIT should be applied 400ns after the trailing edge of the BUSY pulse. This will ensure that the data on the output pins is valid. The data should then be transferred and the INHIBIT released before the next BUSY pulse occurs. The worst case times allowable for data transfer in this case are shown in the Specifications under the heading of "MAX DATA TRANSFER TIME (from 400rs After Trailing Edge of BUSY at Max Velocity)". It should be noted that the application of the INHIBIT will not prevent to ie BUSY pulses appear ing on the BUSY pin, and thus if the INHIBIT is not release by the time that the next BUSY pulse occurs, the BUSY pulse will still appear, although the internal converter loop will have been opened. Under this condition, a worst case recovery time, equivalent to that of a step of 179 degrees may be encountered (see Spec.). To avoid this and to ensure valid data transfer, the system shown in the diagram is recommended.



Suggested External Interface Circuitry

In cases where the converter is connected to a data bus or used as a peripheral, the method outlined in the above diagram is recommended. The INHIBIT is not necessary in this case, and the external "Enable" has control of the converter output.

The AC1755 mounting card described later in this data sheet contains the external components shown in the diagram.

CONNECTING THE CONVERTER

The power lines, which should not be reversed, should be connected to "+15V", "-15V" and "+5V" in the case of the SBCD1752 and SBCD1753, and to "+15V" and "+5V" in the case of the SBCD1756 and SBCD1757, with the common connection to "GND" in all cases.

It is suggested that $0.1\mu F$ and $6.8\mu F$ capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

The digital output connections in the case of the SBCD1753 and SBCD1757 should be taken from the pins marked "0.1" through to "200"; these values being represented in degrees.

In the case of the SBCD1752 and SBCD1756, the data should be taken from the pins marked "0.1" through to "100", these values also being represented in degrees. In the case of these latter units the "SIGN" pin will indicate the polarity of the output, Logic "0" representing positive angles and Logic "1" representing negative angles.

In the case of a synchro, the signals are connected to S_1 , S_2 and S_3 according to the following convention:

Synchro connection

 $E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$

 $E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^{\circ})$

 $E_{S2} - S1 = E_{RLO} - RHI Sin \omega t Sin (\theta + 240°)$

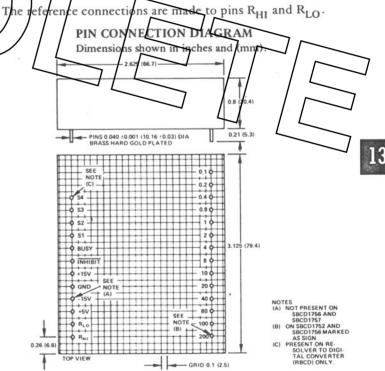
For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

Resolver Connection

 $E_{S1 - S3} = E_{RLO - RHI} \sin \omega t \sin \theta$

 $E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$

The BUSY and INHIBIT pin (if used), should be connected as described under the heading "DATA TRANSFER".



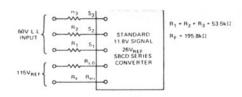
MATING SOCKET: CAMBION 450-3388-01-03

RESISTIVE SCALING OF INPUTS

A unique feature of the SBCD1752/1753/1756/1757 converters is that the inputs can be resistively scaled to accommodate any value of input signal and reference voltage.

In order to calculate the values of the external scaling resistors necessary, add $1.11k\Omega$ in series with the input per extra volt in the case of the signal, and $2.2k\Omega$ per extra volt in the case of the reference.

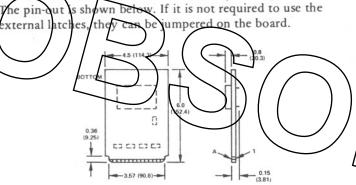
For example, assume that it is required to use a standard 11.8V line to line signal, 26V reference converter with 60V line to line signal and a 115V reference. The resistors should be arranged as in the diagram.



Note: In the case of R_1 , R_2 , and R_3 , the ratio error between the resistances is more critical than the absolute value. In general a 1% ratio error will give rise to an extra inaccuracy of 0.28 Degrees, while a ratio accuracy of 0.1% will give rise to an extra inaccuracy of 0.028 Degrees. The absolute value of R_F is not critical.

CARD MOUNTING

All the converters can be mounted on an AC1755 mounting card. This card contains the latches and monostable, described under the "DATA TRANSFER" heading, which are necessary to transfer the data on to a computer bus system, as well as sockets for the converter. The latches have a tri-state output to facilitate ease of use. The AC1755 also contains facilities for the inclusion of input signal scaling and reference resistors as described under the heading "RESISTIVE SCALING OF INPUTS". The card uses a 22/22 0.156" pitch edge connector.



AC1755 Mounting Card (First Angle Projection). Dimensions Shown in Inches and (mm).

Edge Pin Number	Function	Edge-Pin Letter	Function
1	R (Lo)	A	Tri-State Enable
2	R (Hi)	F	+15 Volts
3	S ₃	Н	+15 Volts
4	S ₂	J	-15 Volts (3)
5	S ₁	K	-15 Volts (3)
6	S ₄	L	GND
		M	GND
13	BUSY	N	+5 Volts
15	INHIBIT	P	+5 Volts
16	0.1	Τ.	8
17	0.2	U	10
18	0.4	V	20
19	0.8	W	40
20	1	X	80
21	2	Y	100
22	4	Z	200 (1) SIGN (2)

NOTES

- (1) SBCD1753 and SBCD1757 only
- (2) SBCD1752 and SBCD1756 only
- (3) SBCD1752 and SBCD1753 only

AC1755 Mounting Card Edge Connections

UNDERHING HATURMATION

Converters should be ordered by the appropriate part number (i.e., SBCD1752, SBCD1753, SBCD1756 or SBCD1757) followed by the appropriate option code.

If the unit is to be a Resolver-to-Digital converter, the SBCD should be replaced by RBCD in the part number.

The XYZ options are as follows:

X signifies the operating temperature range thus;

X = 5 0 to $+70^{\circ}$ C (Commercial Temp.)

X = 6 -55° C to $+105^{\circ}$ C (Extended Temp.)

Y signifies the reference frequency thus;

Y = 1 signifies 400Hz

Y = 2 signifies 60Hz*

Y = 4 signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is a Synchro-to-Digital or a Resolver-to-Digital converter. The options for Z are:

Z = 1 signifies Synchro,

signal 11.8 Volts reference 26 Volts

Z = 2 signifies Synchro,

signal 90 Volts

reference 115 Volts

Z = 8 signifies Resolver,

signal 11.8 Volts reference 26 Volts

Thus an SBCD1753 with a commercial (0 to +70°C) operating range, using a 400Hz, 26 volt reference with an 11.8 volt signal would be ordered as an SBCD1753511.

For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.

In addition a 400Hz unit will work with a 2.6kHz reference and a 60Hz unit will work with a 400Hz reference, however they will have the velocity and acceleration characteristics of the lower frequency rated unit.

OTHER PRODUCTS

The SBCD series of Synchro-to Digital converters are just a few of the modules and instruments concerned with Synchro conversion manufactured by us. Some of our other products are listed below and technical data is available. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

SYNCHRO-TO-DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4") converter with a 12-bit natural binary output. Its overall accuracy is ±8.5 arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz. The SDC1702 is similar to the SDC1700 but has a 10-bit natural binary output and an overall accuracy of ±22 arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14-bit natural binary output and an overall accuracy of ± 2.0 arc-minutes ± 1 LSB.

TWO SPEED PROCESSORS

The TSL1612 and the TSL1729 both produce one digital output word up to 20 bits in length from the outputs of 2 Synchroto-Digital converters in a coarse/fine system. The TSL1612 is used for ratios of 9:1, 18:1 and 36:1, while the TSL1729 is programmable for all ratios from 1:1 to 63:1.