ANALOG DEVICES

AN-204
APPLICATION NOTE

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Applications of the SMP-04 and the SMP-08/SMP-18, Quad and Octal Sample-and-Hold Amplifiers

By Adolfo A. Garcia

The SMP-04 and the SMP-08 are monolithic quad and octal sample-and-hold amplifiers that greatly reduce the complexity and the cost of discrete approaches (op amps, capacitors, switches, and multiplexers). Built on an advanced analog CMOS process, the SMP-04 and SMP-08 exhibit very low droop rates of 2 mV/s and fast acquisition times of 7 μs. The SMP-18, a faster version of the SMP-08 (2.5 μs acquisition time) with similar specifications, is also available. The on-chip MOS capacitors save space and reduce cost by eliminating external, expensive low leakage capacitors. As a result, layout guard-ringing and details for board cleanliness are no longer necessary to maintain specified performance.

Architecturally, the SMP-04 contains four independent sample-and-hold amplifiers; whereas the SMP-08 and the SMP-18 contain eight sample-and-hold amplifiers multiplexing one common input to eight independent outputs. The SMP-04 will be used throughout this application note to describe all devices, unless otherwise noted. Simplified block diagrams of the SMP-04 and the SMP-08/SMP-18 are shown in Figure 1a and Figure 1b.

The versatility of these amplifiers opens up many useful applications which will be described below. This application note will point out special issues and techniques to derive the maximum performance from these devices.

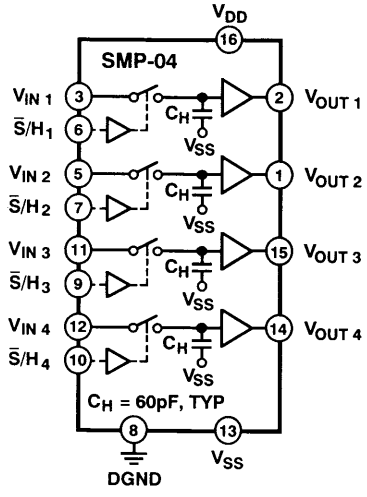


Figure 1a. Block Diagram of the SMP-04

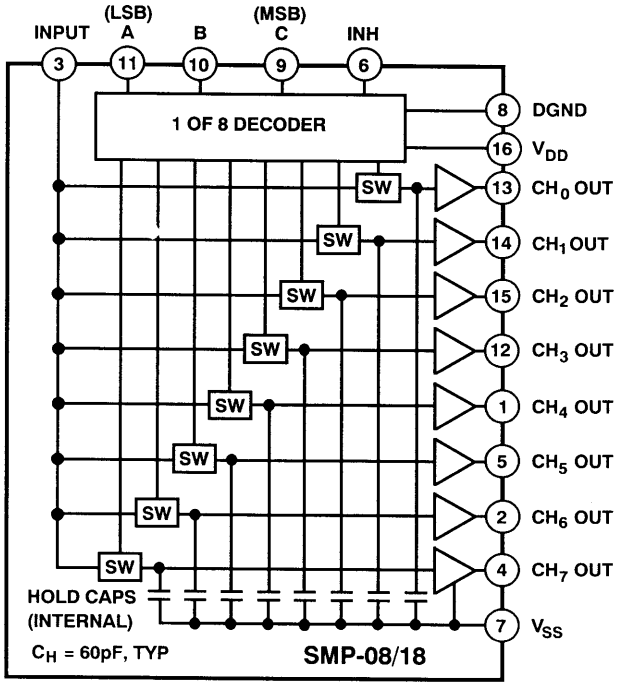
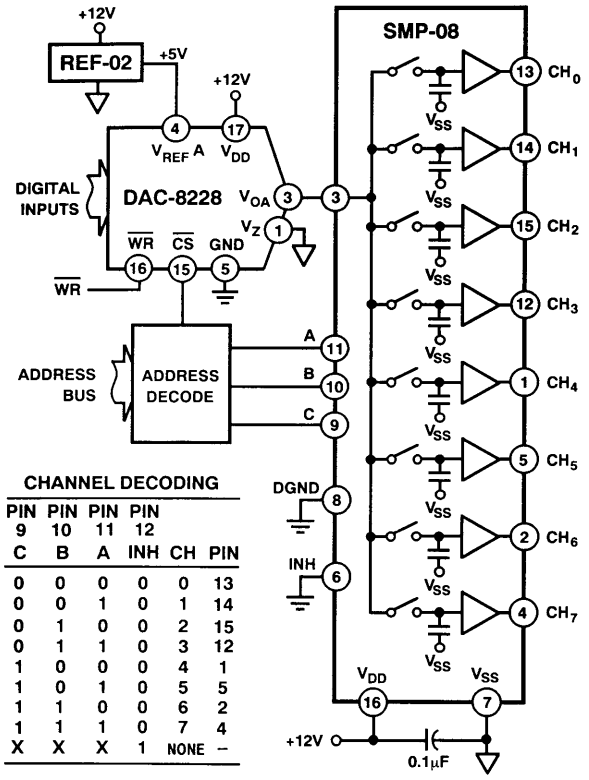


Figure 1b. Block Diagram of the SMP-08/SMP-18

APPLICATION CIRCUITS

An Eight-Channel Setpoint Controller

Figure 2 illustrates a low cost analog setpoint controller circuit by demultiplexing a single DAC output to eight independent channels using the SMP-08. With a maximum droop rate of 20 mV/s, the SMP-08 can maintain 8-bit accuracy (1/2 LSB at 5 V full scale) by refreshing



CHANNEL DECODING

PIN 9 C	PIN 10 B	PIN 11 A	PIN 12 INH	CH	PIN
0	0	0	0	0	13
0	0	1	0	1	14
0	1	0	0	2	15
0	1	1	0	3	12
1	0	0	0	4	1
1	0	1	0	5	5
1	1	0	0	6	2
1	1	1	0	7	4
X	X	X	1	NONE	–

Figure 2. An 8-Channel Setpoint Controller

once every 500 ms. For a 10-bit DAC, the refresh rate must be less than 122 ms and, for a 12-bit system, 31 ms. This implementation is very cost effective when compared to using multiple DACs as the number of output channels increases. Typical operation of the setpoint controller is shown in Figure 3a. With the DAC

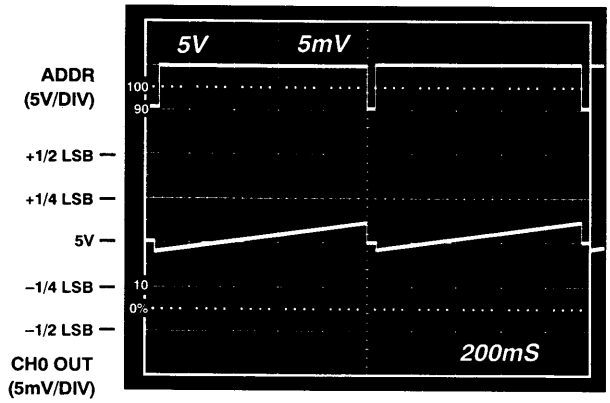


Figure 3a. Illustrates the Operation of the Setpoint Controller. The top trace is the address decoder selecting CH0 (LOW) or CH7 (HIGH). The bottom trace is CH0's output illustrating the SMP-08's typical droop and hold step.

output at 5 V, the address decoder drives all address lines concurrently, selecting either Channel 0 or Channel 7. As the photo shows, the SMP-08 maintains less than 1/4 LSB error (for 8-bit accuracy) for 1 second. An expanded view of the droop, the reset to 5 V, and a hold step of 1 mV is shown in Figure 3b.

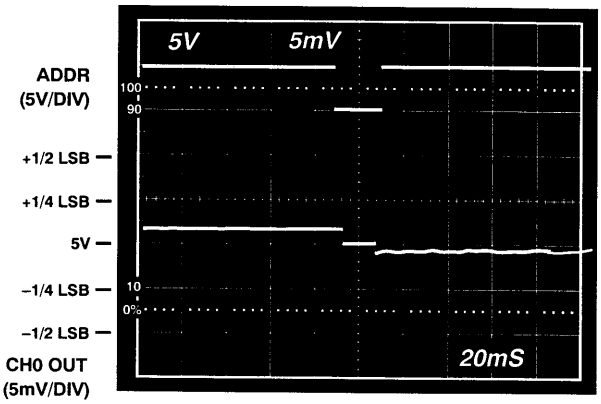


Figure 3b. Illustrates the Expanded View of the Setpoint Controller's Operation

A Single Event Sampler

The circuit in Figure 4 takes 16 equally timed consecutive samples to capture a single event on the input signal. Once captured, the sampled signals can be sequentially reconstructed repetitively on an oscilloscope, either at the original sampling clock rate or a slower clock rate.

By selecting the position of switch SW1, sampling can begin by triggering on the input's signal level, or on an external trigger (negative going) pulse that is no more than one clock period long. In the case where a 1 MHz clock is used, the pulse width must be 1 μs or less. Either signal resets the 74LS161 counter asynchronously. The sequential sampling begins at the rising edge of the second clock period. The reset pulse also clears both J-K flip-flops, removing the inhibit to the SMP-08s. The synchronous counter outputs ensure equal sampling periods to each sample-and-hold amplifier. The J-K flip-flops toggle and subsequently inhibit the SMP-08s from further sampling.

To reconstruct the sampled analog signal, the 16 sampled signals are sequentially addressed by the MUX-16, a 16-channel analog multiplexer. The 74LS163 binary counter cycles the multiplexer which generates a repetitive waveform as shown in Figure 5. The waveform will keep its shape for as long as ten seconds, but beyond that the SMP-08's 20 mV/s maximum droop rate causes it begin to lose its shape gradually.

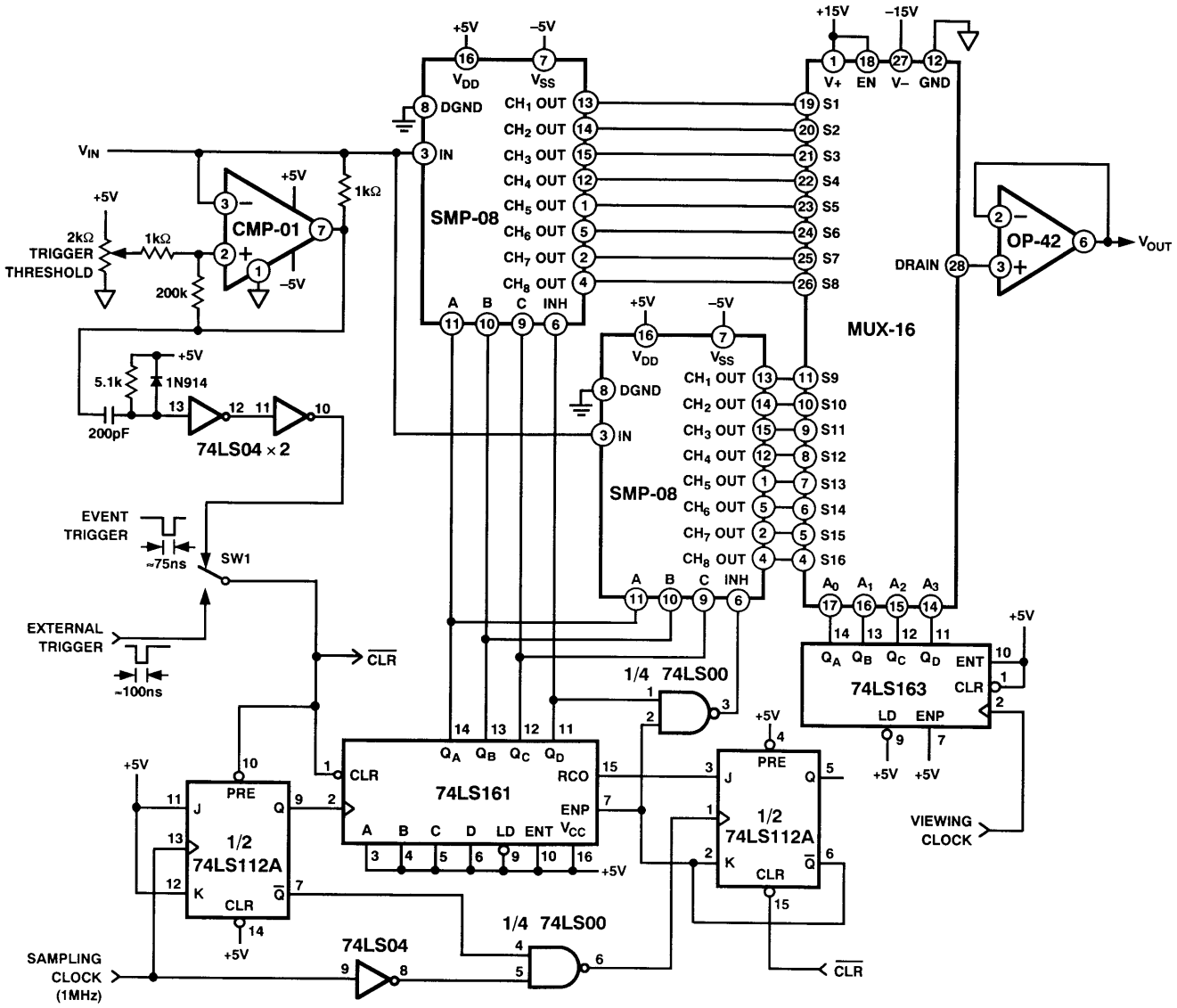


Figure 4. A 16-Channel Single Event Sampler

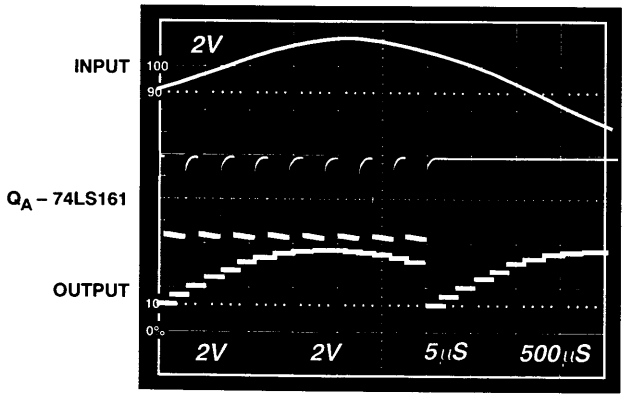


Figure 5. Illustrates the Operation of the 16-Channel Single Event Sampler

A variation of this concept has been demonstrated in other publications. One such design is described in Application Note AN-289 published by National Semiconductor Corp. That approach used eight separate sample-and-hold amplifiers plus eight capacitors. This design, however, illustrates how a considerably smaller circuit using less components, and therefore lower costs, can be realized using a single-chip octal sample-and-hold amplifier like the SMP-08. In fact, the beauty of this configuration is that the number of sample-and-hold channels can be easily expanded to increase the sampling resolution without a heavy penalty in increased circuitry and component costs.

DAC Deglitcher

Most DACs output an appreciable amount of "glitch" energy during a transition from one code to another. The glitch amplitude can range from several millivolts to hundreds of millivolts. This may be unacceptable in many applications. By selectively delaying the DAC's output transition, the SMP-04 can be used to smooth the output waveform. Figure 6 shows the schematic diagram of a quad DAC deglitcher circuit using only a write strobe command ($\overline{WR}$) generated by a microprocessor.

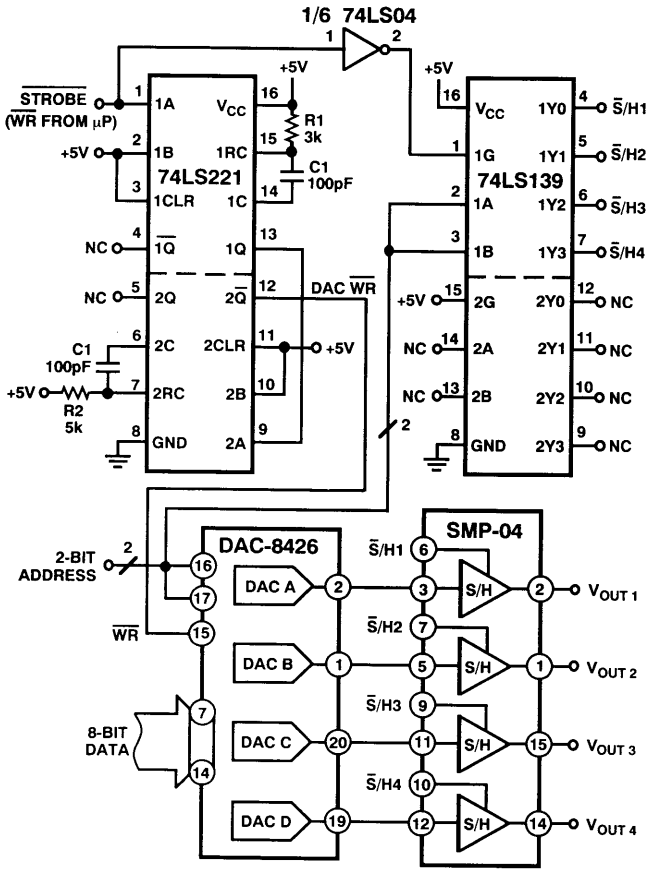


Figure 6. A Quad DAC Deglitcher

Dual one-shots (a 74LS221) and an inverter provide the proper delay timing for the DAC $\overline{WR}$ strobe and the $\overline{S}$/H control signal to the SMP-04. The 74LS139 demultiplexer is used to steer the $\overline{S}$/H control signal to the appropriate SMP-04 channel. Therefore, only one timing circuit is used to deglitch a quad DAC. In this example, a linear ramp signal is generated by the microprocessor whose $\overline{WR}$ strobe is 800 ns in duration. In Figure 7a, new data to

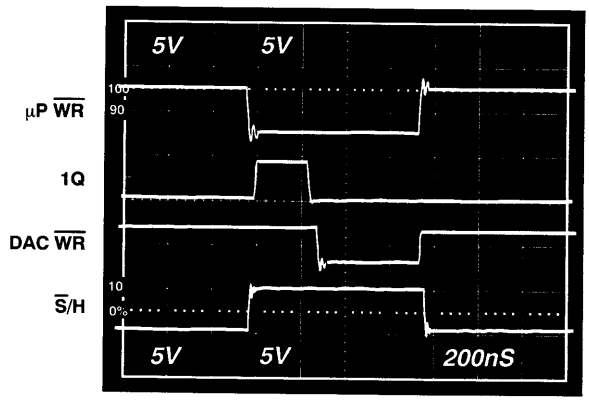


Figure 7a. Shows the Logic Timing of the Deglitcher. The top trace is the $\overline{WR}$ from the microprocessor. The second trace is used to strobe the second one-shot that generates the DAC's $\overline{WR}$ strobe. The bottom trace is the S/H control signal.

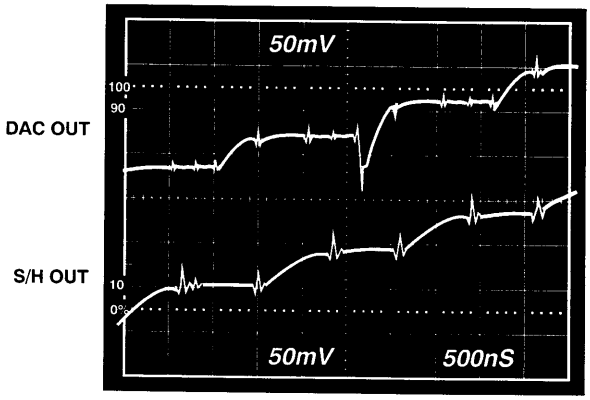


Figure 7b. Shows a Typical DAC Glitch Amplitude (Top Trace) and the Deglitched Output of the SMP-04 (Bottom Trace)

the DAC A input is set up at the S/H1's falling edge, but the DAC A output does not change until its $\overline{WR}$ strobe goes active. When that occurs, the S/H1 begins sampling and tracks DAC A's output. When the $\overline{S}$/H signal goes HIGH, DAC A's output voltage is held by S/H1. After a 300 ns settling, DAC A's $\overline{WR}$ strobe goes LOW to allow the DAC output to change. Any glitch that occurs at the DAC output is blocked by the SMP-04. As soon as the $\overline{WR}$ strobe goes HIGH, the digital data is latched; at the same time, the $\overline{S}$/H goes LOW, and the SMP-04 is allowed to track the new DAC output voltage. Figure 7b shows the deglitching operation. The top trace shows the DAC A's output during transition while the bottom trace shows the deglitched output of the SMP-04.

A Pipelined Data Acquisition System

If a sample-and-hold is used in the front of a successive approximation register (SAR) type ADC, the system throughput can be increased by adding a second sample-and-hold operating in a "ping-pong" fashion as shown in Figure 8. While the first channel is holding the input signal for the A/D conversion, the second sample-and-hold is acquiring another channel through the multiplexer. By the time the A/D conversion is complete on the first sample-and-hold's signal, the second sample-and-hold will have acquired its data and will be ready for the next conversion. This pipeline technique eliminates the acquisition time of the sample-and-hold in the signal path.

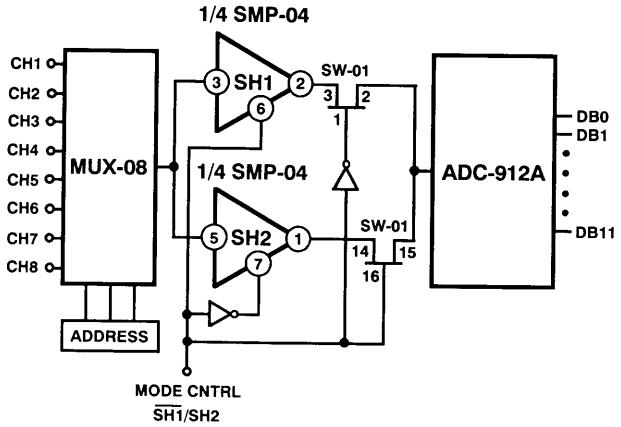


Figure 8. A Pipelined Data Acquisition System

A Low Cost Battery Tester

The condition of a new or old battery can be tested very quickly under a load with the circuit in Figure 9. When the momentary switch is pressed, the no-load battery voltage is sampled by the first sample-and-hold. R3 and R4 are chosen so that, according to the battery manufacturer's end-of-life specifications, the threshold of the PM-139 comparator is set to 87.5% of the no-load battery voltage. Since this is a very low frequency application, approximately 16 mV of hysteresis about the threshold voltage, set by R5 and R6, was chosen to prevent the comparator from oscillating. The gate of the power NMOS transistor is controlled by a differentiator whose time constant is set at 470 μs. When the power FET turns on, it forces a 500 mA load current from the battery. At the same time, the second differentiator controls the second sample-and-hold. Thus, the battery's voltage under load is sampled and applied to the inverting terminal of the comparator. If the battery's voltage is at or above the threshold, then the comparator's output goes low and triggers the GREEN LED through the D flip-flop, indicating a PASS condition; otherwise, the RED LED turns on. To clear the D flip-flop during the power-on sequence, a 100 ms R10-C3 combination was connected to the D flip-flop's RESET pin through an inverter.

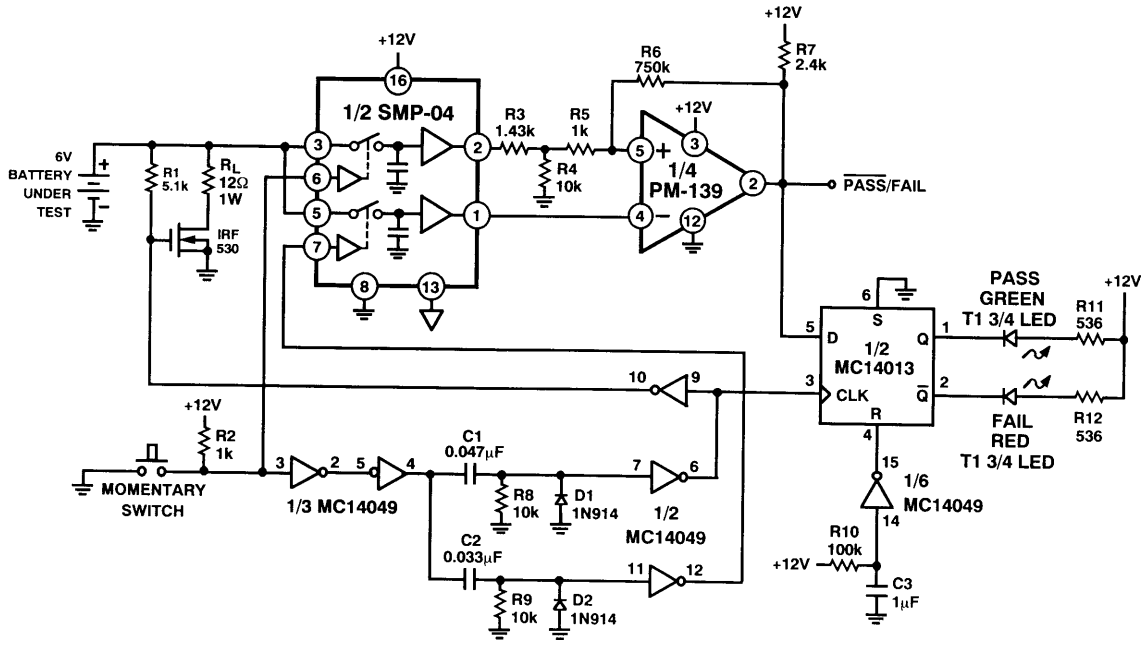


Figure 9. Low Cost Battery Tester

APPLICATIONS HINTS

Input Drive Considerations

For each channel of the SMP-04, the input looks directly into a CMOS transmission gate and an internal, low leakage MOS capacitor, as shown in Figure 10. The ON resistance of the transmission gate and the internal hold capacitor, which is typically 60 pF, largely determine the acquisition time of the SMP-04. Any drive circuit having a finite output resistance will increase the RC charge time and degrade the acquisition time. Consequently, good acquisition time can be preserved by driving the input of the SMP-04 from low output resistance sources.

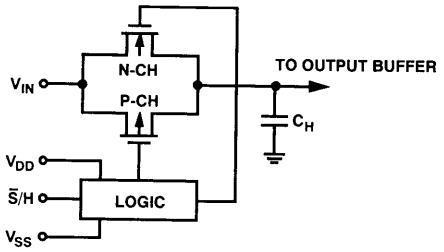


Figure 10. Input Circuit of the SMP-04 and the SMP-08/SMP-18

Since the transmission gate is constructed of enhancement-mode MOSFETs, its ON resistance is a function of both the supply voltages and the applied input signal. Figure 11a shows the transmission gate's ON resistance of the SMP-04 for a single +12 V supply as a function of the applied analog input voltage. Similarly, Figure 11b show the switch resistance for ±5 V supplies as a function of the applied analog input voltage.

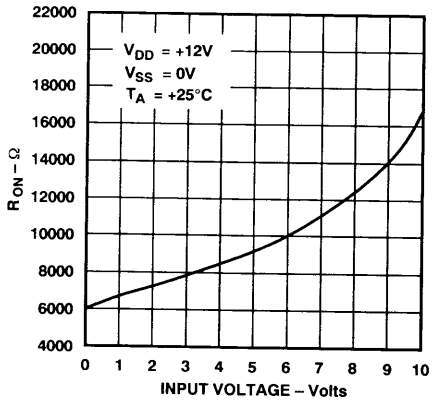


Figure 11a. SMP-04/SMP-08 Switch ON Resistance vs. Input Voltage

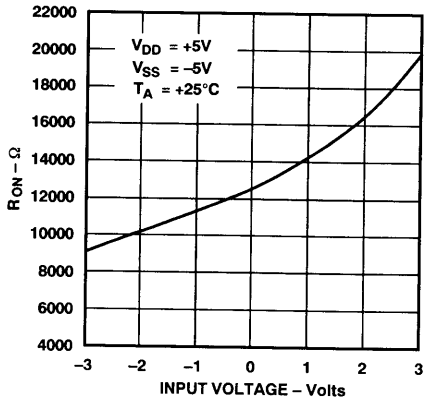


Figure 11b. SMP-04/SMP-08 Switch ON Resistance vs. Input Voltage

Figures 12a, 12b, and 12c illustrate how the SMP-04's acquisition time is affected by different supply voltages and applied input signals. Note that for positive-slewing signals the SMP-04 acquires the signal more slowly than for negative-slewing signals. This is due to the nonsymmetrical slew characteristics of the output buffer. For single supply +15 V or +12 V applications, the analog input should be in the range of 100 mV $\leq V_{IN} \leq V_{DD}-2$ V to avoid significant degradation of the sampled signal.

The input capacitance is a combination of the internal hold capacitor, the transmission gate's parasitic input capacitance, the output buffer's parasitic input capacitance, and the parasitic package pin capacitance. In the sample mode, the SMP-04's typical input capacitance is approximately 60 pF. In the hold mode, the input capacitance drops to under 10 pF. In the case of the SMP-08, the external input capacitance in the sample *or* hold modes is typically 80 pF, and typically 30 pF in the INHIBIT mode. Depending on the amplifier used, ringing and overshoot can occur when driving this input capacitance. Op amps, such as the OP-42 and the AD847, which have low output resistances and excellent capacitive load drive capability, are ideal for driving the SMP-04 and the SMP-08.

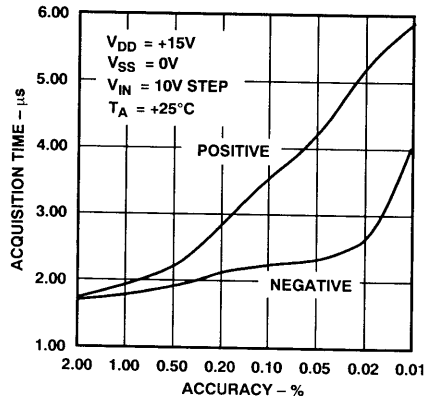


Figure 12a. SMP-04/SMP-08 Acquisition Time vs. Percent Accuracy

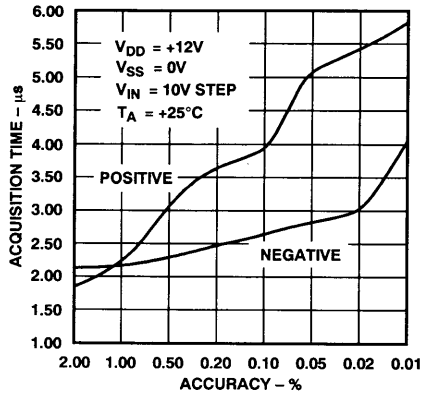


Figure 12b. SMP-04/SMP-08 Acquisition Time vs. Percent Accuracy

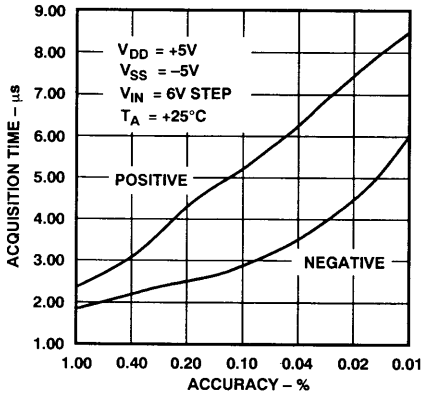


Figure 12c. SMP-04/SMP-08 Acquisition Time vs. Percent Accuracy

Using The SMP-04 As A Buffer

It is sometimes advantageous to use one or more sections of the SMP-04 as a buffer. This is done by setting the SMP-04 in a continuous SAMPLE mode by connecting the $\overline{S}$/H control pin to logic LOW. The SMP-04 has good distortion characteristics over the audio frequency range. For a single 12 V supply, Figure 13a illustrates the track-mode distortion characteristics of the SMP-04. Note that the SMP-04 maintains less than 0.04% total harmonic distortion over the entire audio frequency

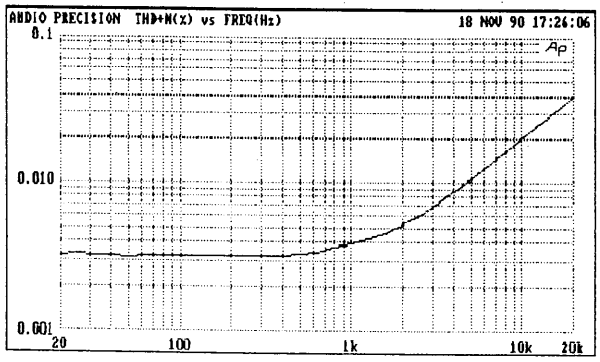


Figure 13a. SMP-04 Track Mode THD+N vs. Frequency. V_S = +12 V/GND, V_{OFFSET} = +6 V, R_L = 10 kΩ, and V_{IN} = 1 V p–p

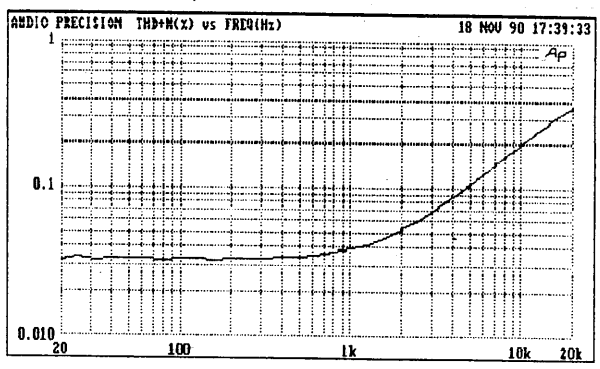


Figure 13b. SMP-04 Track Mode THD+N vs. Frequency. V_S = ±5 V, V_{OFFSET} = +0 V, R_L = 10 kΩ, and V_{IN} = 1 V p–p

band. For a ±5 V supply operation, the SMP-04 exhibits less than 0.4% total harmonic distortion over the same frequency band, as shown in Figure 13b. For audio distribution applications, one might consider using the SMP-08. Figure 14a illustrates its track-mode distortion characteristics for a single 12 V supply. The SMP-08 maintains less than 0.6% total harmonic distortion over the entire audio frequency band. Figure 14b illustrates the SMP-08's distortion characteristics for ±5 V supply operation. Distortion performance is only slightly worse (0.7%) than the single supply case over the entire audio frequency band. In all measurements, a standard 80 kHz

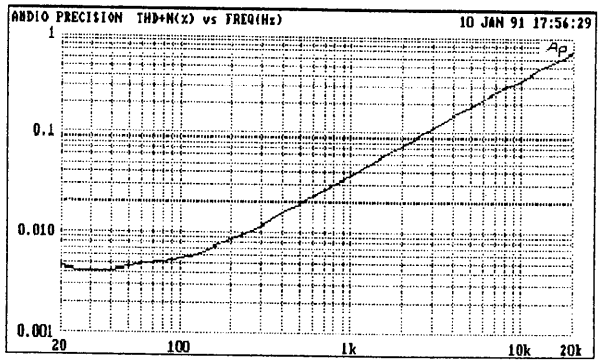


Figure 14a. SMP-08 Track Mode THD+N vs. Frequency. V_S = +12 V/GND, V_{OFFSET} = +6 V, R_L = 10 kΩ, and V_{IN} = 1 V p–p

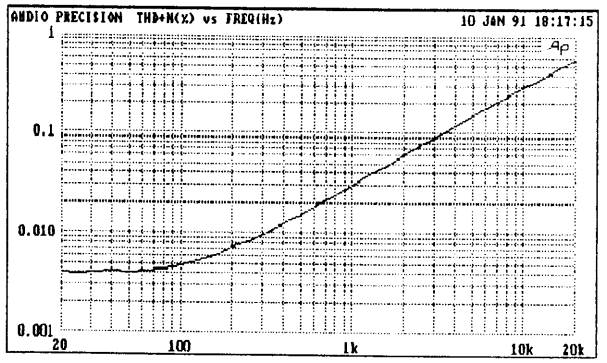


Figure 14b. SMP-08 Track Mode THD+N vs. Frequency. V_S = ±5 V, V_{OFFSET} = +0 V, R_L = 10 kΩ, and V_{IN} = 1 V p–p

filter and an R_L = 10 kΩ were used. If track-mode distortion performance is important, use a large supply voltage range (V_{DD}–V_{SS}) to yield lower distortion products. Be sure to remain well within the absolute maximum supply voltage ratings, that is, V_{DD}–V_{SS} less than 17 V, maximum.

Transient Load Response

When an amplifier is used to drive the input of a SAR ADC, the ADC generates abrupt current changes at the analog input. For accurate conversions, the drive amplifier must be capable of holding a constant output voltage under dynamically changing load conditions. Therefore, it is important to know how quickly the amplifier's output settles under these conditions. Amplifiers with low closed-loop output impedances recover from output load current changes quickly without long settling tails.

The SMP-04's low closed-loop output impedance (1 ohm, typical) allows the output to settle quickly during a SAR ADC's conversion cycle. Figure 15a illustrates a typical transient load response (to 12-bit accuracy) of the SMP-04 with a 1 mA transient load current. This load current is a worst case condition for driving a SAR ADC with a 2 mA reference current. Figure 15b illustrates the

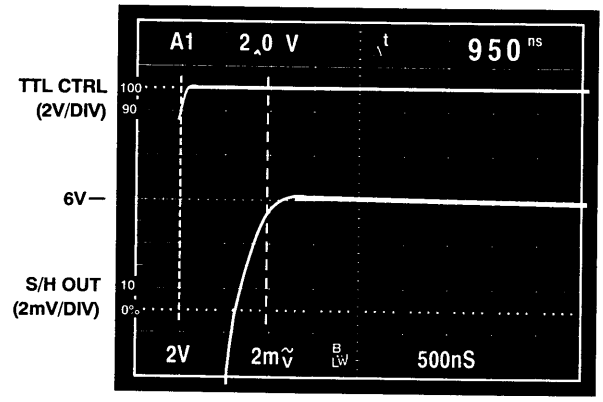


Figure 15a. SMP-04/SMP-08 Output Buffer Response to a 1 mA Load Current Transient. V_{DD} = +12 V, V_{SS} = GND

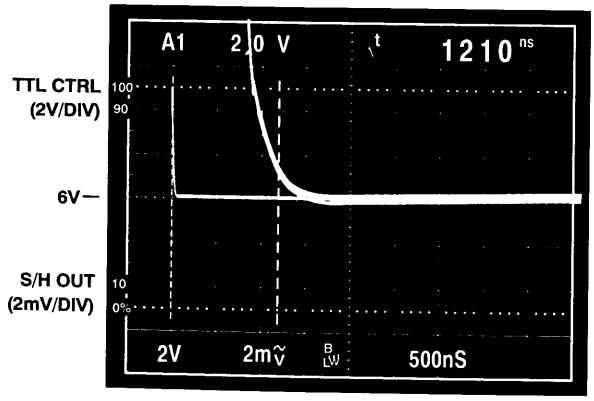


Figure 15b. SMP-04/SMP-08 Output Buffer Recovery from a 1 mA Load Current Transient. V_{DD} = +12 V, V_{SS} = GND

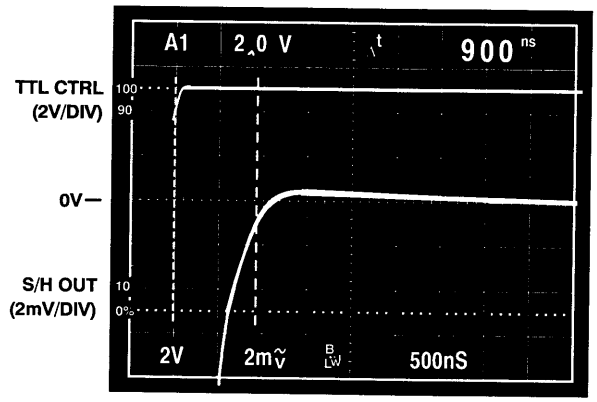


Figure 15c. SMP-04/SMP-08 Output Buffer Response to a 1 mA Load Current Transient. V_{DD} = +5 V, V_{SS} = −5 V

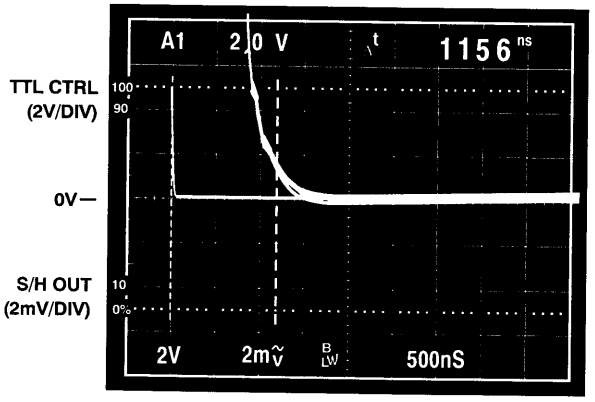


Figure 15d. SMP-04/SMP-08 Output Buffer Recovery from a 1 mA Load Current Transient. V_{DD} = +5 V, V_{SS} = −5 V

SMP-04's typical transient load response when the load current is turned off. The slower transient load recovery is due to asymmetric slew characteristics of the SMP-04's output buffer. For ±5 V supply applications, slightly faster response times to 12-bit accuracy are shown in Figures 15c and 15d. These results suggest that the minimum clock period for a 12-bit SAR ADC should be 1.3 μs.

Aperture Delay Time and Jitter

Two additional dynamic parameters that affect accuracy and total acquisition time are aperture delay time and jitter. Aperture delay is the time required by the internal switches to disconnect the hold capacitor from the input. Aperture jitter is the uncertainty in aperture delay caused by internal noise and variation of switching thresholds with the input signal. Typically, the SMP-04 and the SMP-08 exhibit an aperture delay time of 20 ns and an aperture jitter of 800 ps.

Interchannel Crosstalk and Hold-Mode Feedthrough

The four independent channels of the SMP-04 typically exhibit 100 dB of crosstalk rejection from dc to 100 kHz regardless of supply voltages used. In the hold-mode, its feedthrough measures −85 dB over the same frequency range.

SMP-08/SMP-18 Channel Decode Timing

For applications that require sequencing the SMP-08's (or the SMP-18's) output channels, Figure 16a illustrates the break-before-make timing relationships between the address lines and the analog input. When an address change occurs, the previously selected channel turns off in 45 ns. The next selected channel turns on in 90 ns. Therefore, to avoid potential crosstalk problems, the analog input must not change for 45 ns after an address change.

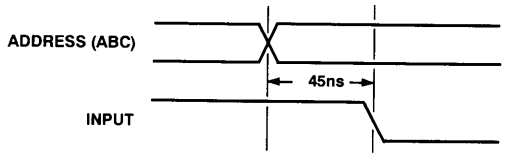


Figure 16a. SMP-08/SMP-18 Decode Timing Option 1

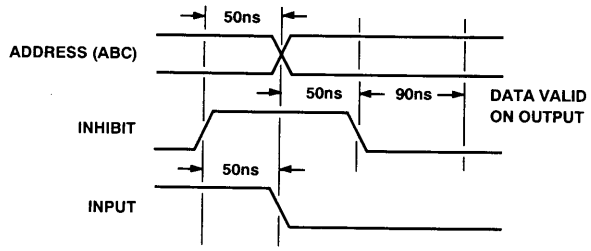


Figure 16b. SMP-08/SMP-18 Decode Timing Option 2

Another option is to use the INHIBIT function to disable all channels during address and analog input changes. The timing diagram in Figure 16b illustrates the relationships between the INHIBIT, the address lines, and the analog input. Once the INHIBIT goes LOW, the next selected channel's analog output is valid in 90 ns. It is therefore, recommended that the minimum INHIBIT pulse width be 100 ns to minimize feedthrough and glitching to the analog outputs. A simplified logic diagram of the 1:8 decoder is shown in Figure 17.

Single +5 V Operation

The SMP-04 and the SMP-08 can operate on a single +5 V supply but with reduced performance. Table I summarizes the performance characteristics of the SMP-04 and the SMP-08 with this supply voltage. For sampling applications, it is recommended that the analog input be in the range of 100 mV $\leq V_{IN} \leq$ 2.5 V to avoid degradation of the sampled signal. To maximize output voltage swing under this limited supply constraint, loads greater than 10 kΩ should be used.

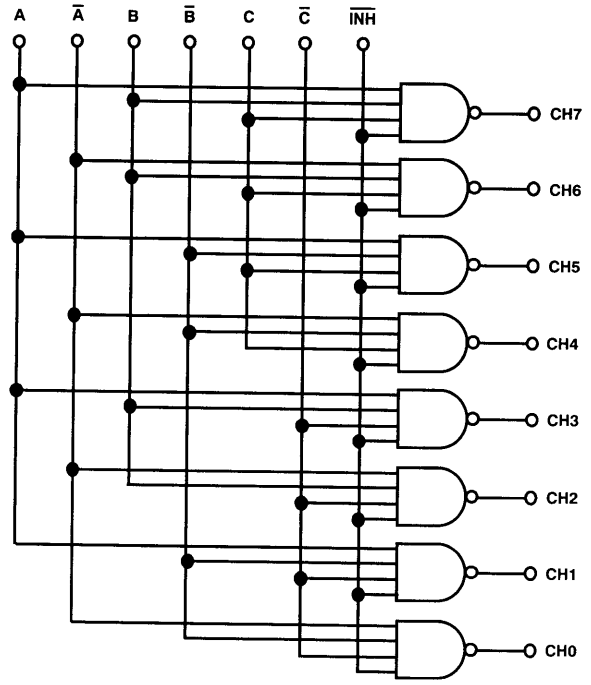


Figure 17. SMP-08/SMP-18 Decode Logic Diagram

Table I. Summary of SMP-04 and SMP-08 Single +5 V Characteristics

Buffer Offset Voltage V_{IN} = 2.5 V	3 mV
Input Voltage Range $R_L = \infty$	0.16 V to 4.1 V
Output Voltage Range $R_L = \infty$ R_L = 1 kΩ	0.15 V to 3.5 V 0.14 V to 1 V
Buffer Small-Signal Bandwidth	200 kHz
Buffer Phase Shift	53°
Acquisition Time 100 mV $\leq V_{IN} \leq$ 2.5 V SMP-04 1% SMP-04 0.1% SMP-08 1% SMP-08 0.1%	 2.3 µs 8.3 µs 3.5 µs 14 µs
Total Harmonic Distortion 20 Hz–20 kHz, R_L = 10 kΩ, V_{IN} = 1 V p–p, Filter = 80 kHz LP SMP-04 SMP-08	 <0.3% <4%
Signal-to-Noise Ratio f_{SAMPLE} = 86 kHz, f_{IN} = 10 kHz f_{SAMPLE} = 14.4 kHz, f_{IN} = 1.8 kHz, t_{pw} = 10 µs	 18 dB 24 dB
SMP-04 Hold-Mode Feedthrough DC to 100 kHz	85 dB
Supply Current SMP-04 SMP-08	 1.5 mA 3 mA

Use of IC sockets

Since the hold capacitors of the SMP-04 are internal and connected to V_{SS}, the SMP-04 and SMP-08/SMP-18 have no external capacitor connections that are exposed to leakage paths which degrade sample-and-hold performance. Therefore, unlike the LM398 that requires expensive, low leakage capacitors and special attention to leakage paths, the SMP-04 and the SMP-08/SMP-18 are tolerant of IC sockets. Wire-wrap sockets, however, are not recommended because of their susceptibility to noise pickup and larger parasitic capacitance compared to solder tail sockets.

ESD Protection

The SMP-04 and the SMP-08/SMP-18 have been designed to withstand over 900 volts of ESD on all pins. However, standard ESD prevention techniques should still be used to minimize potentially excessive high ESD voltages.

The SMP-04 and the SMP-08/SMP-18 are highly resistant to latchup. However, parasitic SCR action can still occur only if a current exceeding 200 mA is forced into the device's analog and digital inputs. This condition is not likely to ever occur because: (1) most amplifiers driving the analog inputs have built-in output short-circuit current limiting; and (2) ICs driving the digital inputs would be destroyed long before the 200 mA limit is reached.

Dual-to-Single Supply Interface

When the SMP-04, connected to a single supply, is driven by an amplifier operating from a dual supply, the circuit in Figure 18 should be used. The circuit configuration is a DAC current-to-voltage converter. The diode is used to clamp the SMP-04's input from negative voltages in the event that the amplifier's output goes to its negative output voltage limit during power on/off situations.

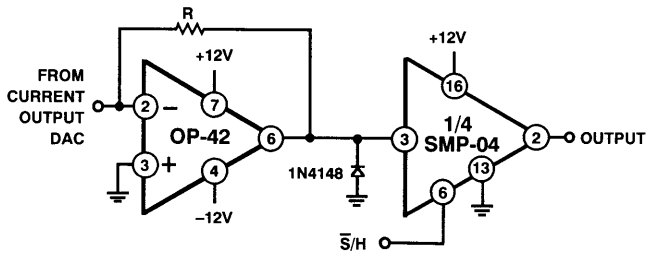


Figure 18. Dual-to-Single Supply Interface Circuit