ANALOG DEVICES

Low Noise Microphone Preamplifier

SSM-2015

FEATURES

- Ultra Low Voltage Noise .... 1.3nV/√Hz
- Wide Bandwidth .... 700kHz @ G = 100
- High Slew Rate 8V/μs
- Very Low Harmonic Distortion .... 0.007% @ G = 100
- Excellent CMR 100dB
- True Differential "Instrumentation" Type Inputs
- Programmable Input Stage Optimizes e_n vs R_{IN}
- Low Cost

ORDERING INFORMATION

	OPERATING TEMPERATURE RANGE
SSM-2015P	−10°C to +55°C
Storage Temperature	−55°C to +125°C

GENERAL DESCRIPTION

The SSM-2015 is an ultra-low noise audio preamplifier particularly suited to microphone preamplification. Gains from 10 to over 2000 can be selected with wide bandwidth and low distortion over the full gain range.

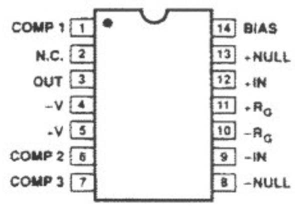
The very low voltage noise performance (1.3nV/√Hz) of the SSM-2015 is enhanced by a programmable input stage which allows overall noise to be optimized for source impedances of up to 4kΩ.

The SSM-2015's true differential inputs with high common-mode rejection provide easy interfacing to flotation transducers such as balanced microphone outputs, as well as single ended devices.

The SSM-2015 also offers high slew rate of about 8V/μs and full DC coupling without any crossover distortion.

This device is packaged in a 14-pin epoxy DIP and is guaranteed over the operating temperature range of −10°C to +55°C.

PIN CONNECTION



14-PIN EPOXY DIP
(P-Suffix)

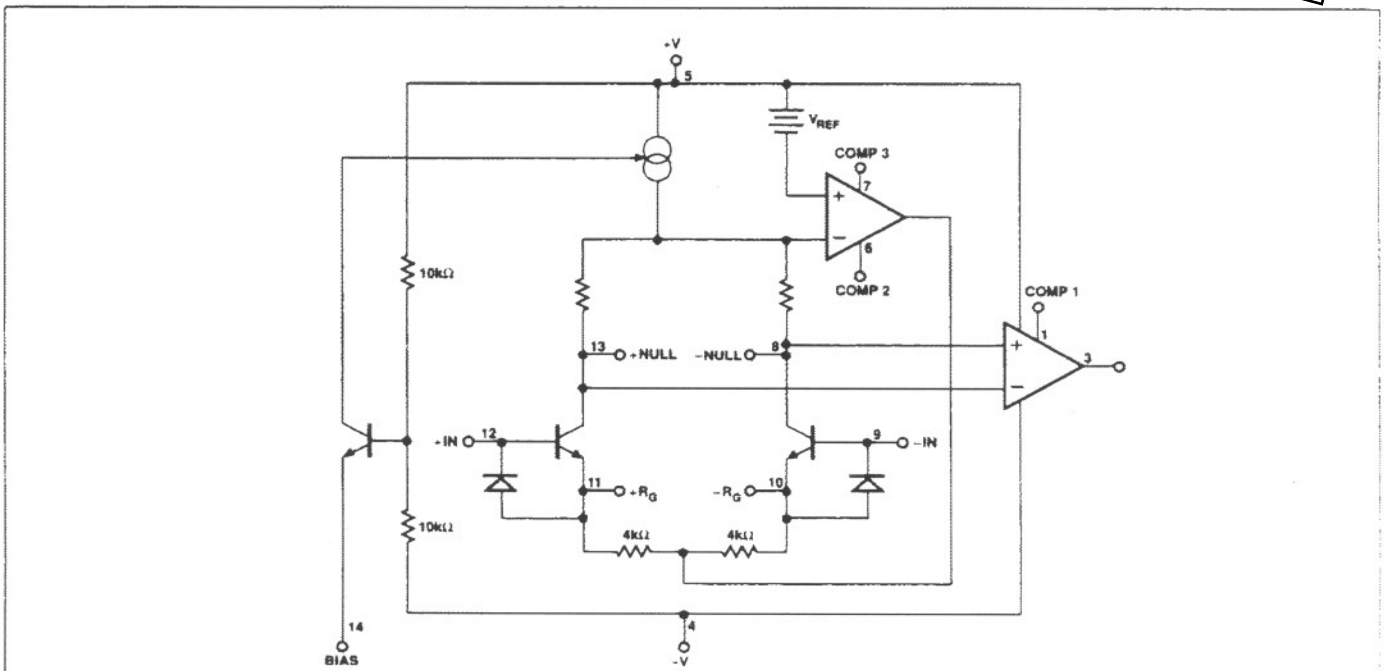
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±18V
Operating Temperature Range .... −10°C to +55°C
Junction Temperature .... +150C
Storage Temperature .... −55°C to +125°C
Lead Temperature Range (Soldering, 60 sec) .... +300°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
14-Pin Plastic DIP (P)	76	33	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for P-DIP package.

BLOCK DIAGRAM



SSM-2015

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, $R_{BIAS} = 33k\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2015 MIN	TYP	MAX	UNITS
Total Harmonic Distortion (Note 1)	THD	V_{OUT} = 7V RMS, R_L = 10kΩ G = 1000 f = 1kHz f = 10kΩ G = 100 f = = 1kHz f = 10kHz G = 10 f = 1kHz f = 10kHz	 – – – – – –	 0.007 0.015 0.007 0.007 0.01 0.01	 0.01 0.02 0.01 0.01 0.015 0.015	%
Input Referred Voltage Noise (Note 1)	E_n	Inputs Shorted to GND 20kHz Bandwidth R_{BIAS} = 33KΩ G = 1000 G = 100 G = 10 R_{BIAS} = 150kΩ G = 1000 G = 100 G = 10	 – – – – – –	 0.2 0.3 1.1 0.28 0.41 1.1	 0.3 0.5 1.7 0.45 0.65 1.7	μV RMS
Input Current Noise (Note 1)	I_n	20kHz Bandwidth R_{BIAS} = 33kΩ R_{BIAS} = 68kΩ R_{BIAS} = 150kΩ	 – – –	 250 200 130	 380 300 200	pA RMS
Error From Gain Equation	ΔG	$R_1 = R_2$ = 10kΩ G = 1000 G = 100 G = 10	 – – –	 0.1 0.1 0.2	 0.3 0.3 0.8	dB
Input Offset Voltage	V_{OS}	$R_1 = R_2$ = 10kΩ G = 1000 G = 100 G = 10	 – – –	 0.25 0.3 3	 2 7 70	mV
Input Bias Current	I_B	V_{CM} = 0V R_{BIAS} = 33kΩ R_{BIAS} = 150kΩ	 – –	 4.5 1	 15 4	μA
Input Offset Current	I_{OS}	V_{CM} = 0V R_{BIAS} = 33kΩ R_{BIAS} = 150kΩ	 – –	 0.5 0.15	 2.5 0.7	μA
Common-Mode Rejection Ratio	CMRR	$R_1 = R_2$ = 10kΩ G = 1000 G = 100 G = 10	 90 70 60	 100 95 75	 – – –	dB
Power Supply Rejection Ratio	PSRR	V_S = ±12 to ±17V	–	100	–	dB
Common-Mode Voltage Range	CMVR		±4	±5.5	–	V
Common-Mode Input Impedance	R_{INCM}		–	50	–	MΩ
Differential-Mode Input Impedance	R_{IN}	G = 1000 G = 100 G = 10	– – –	0.5 5 20	– – –	MΩ
Output Voltage Swing	V_O	R_L = 2kΩ	±10.5	±12.5	–	V
Output Current (Note 2)	I_{OUT}	Source Sink	15 8	25 14	– –	mA
–3dB Bandwidth	GBW	G = 1000 G = 100 G = 10	– – –	150 700 1000	– – –	kHz
Slew Rate	SR		–	8	–	V/μs
Supply Current	I_{SY}		8	12	16	mA

NOTES:
1. Parameter is sample tested to maximum limits.
2. Output is protected from short circuits to ground or either supply.

Specifications subject to change; consult latest data sheet.

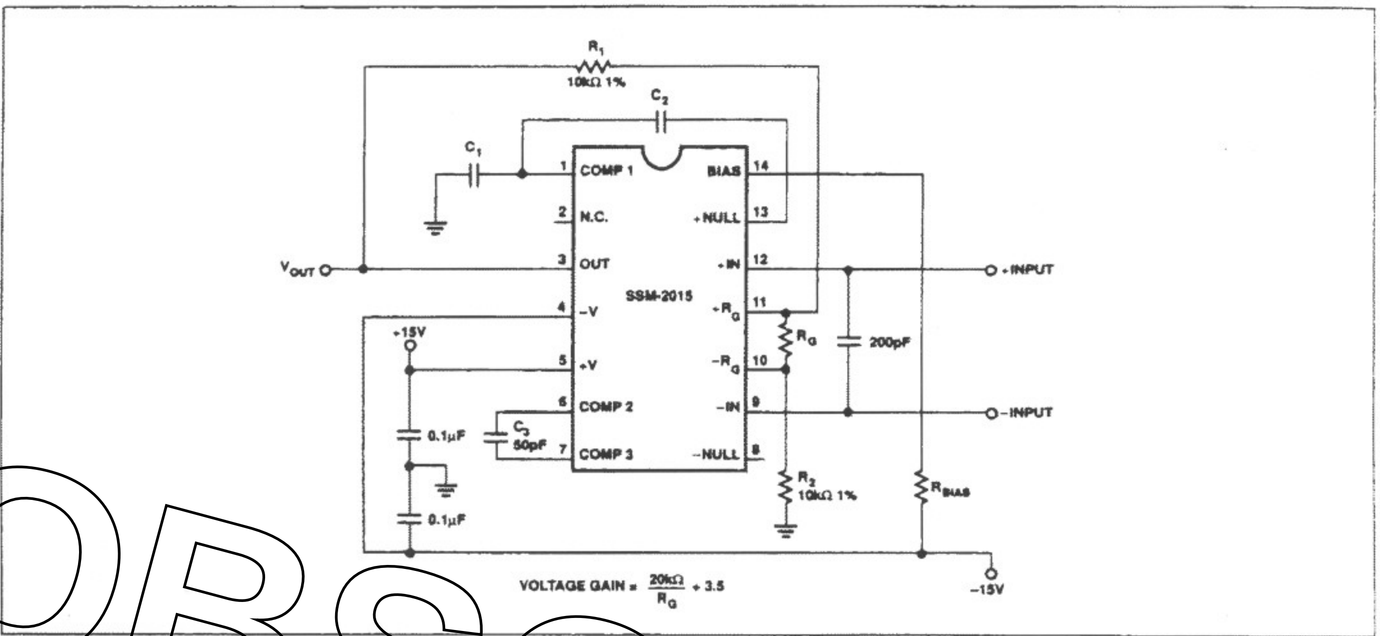


FIGURE 1: *Typical Application*

APPLICATIONS INFORMATION

PRINCIPLE OF OPERATION

Figure 1 shows a typical application for the SSM-2015. This device operates as a true differential amplifier with feedback returned directly to the emitters of the input stage transistors by R_1. This system produces both optimum noise and common-mode rejection while retaining a very high input impedance at both input terminals. An internal feedback loop maintains the input stage current at a value controlled by an external resistor (R_{BIAS}) from pin 14 to V–. This provides a programmability function which allows noise to be optimized for source impedances of up to 4kΩ.

GAIN SETTING

The nominal gain of the SSM-2015 is given by:

$$G \cong \frac{R_1 + R_2}{R_G} + \frac{R_1 + R_2}{8k\Omega} + 1$$

or

$$G = \frac{20k\Omega}{R_G} + 3.5 \quad \text{For } R_1,\ R_2 = 10k\Omega$$

R_1 and R_2 should be equal to 10kΩ for best results (see Figure 1). It is vital that good quality resistors be used in the gain setting network, since low quality types (notably carbon composition) can generate significant amounts of distortion and, under some conditions, low frequency noise. The SSM-2015 will function at gains down to 3.5, but the best performance is obtained at gains above 10. Table 1 gives R_G values for most commonly used gains.

TABLE 1: R_G Values for Commonly Used Gains

$$R_G = \frac{R_1 + R_2}{G - 3.5}$$

GAIN	R_G	ERROR
10	3kΩ	+0.14dB
50	430Ω	+0.002dB
100	200Ω	+0.3dB
500	39Ω	+0.28dB
1000	20Ω	+0.03dB

FREQUENCY COMPENSATION

Referring to Figure 1, C_3 (50pF) provides compensation for the input stage current regulator, while C_1 and C_2 compensate the overall amplifier. The latter two depend on the value of R_{BIAS} chosen. Table 2 shows the recommended values for C_1 and C_2 at various R_{BIAS} levels. These values are valid for all gain settings.

TABLE 2: Recommended Compensation Values

R_{BIAS}	C_1	C_2
27kΩ - 47kΩ	15pF	15pF
47kΩ - 68kΩ	15pF	10pF
68kΩ - 150kΩ	30pF	5pF

SSM-2015

The SSM-2015 has a bandwidth of at least 70kHz under worst case conditions (G = 1000, R_{BIAS} = 150kΩ) and considerably greater at higher set currents and lower gains. This excellent performance is supplemented by a highly symmetric slew rate for optimum large signal audio performance. The SSM-2015 provides stable operation with load capacitances of up to 150pF; larger capacitances should be decoupled with a 100Ω resistor in series with the output (R_1 in Figure 1 should remain connected to pin 3).

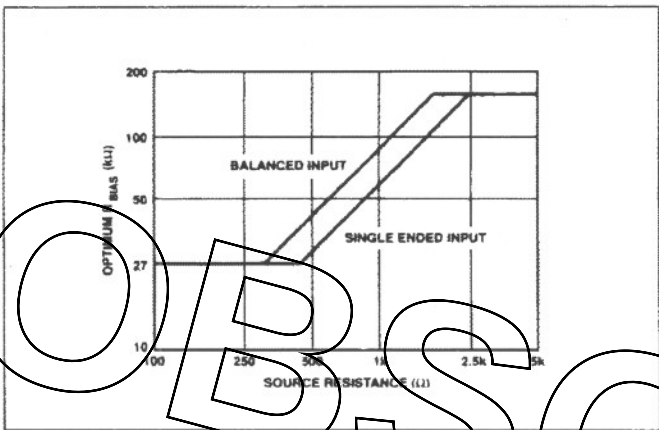


FIGURE 2: *Optimum R_{BIAS} vs. Source Resistance*

NOISE

The programmability of the SSM-2015 provides close to optimum performance for source impedances of up to 4kΩ, and is within 1dB of the theoretical minimum value between 500Ω and 2.5kΩ.

Figure 2 shows the recommended bias resistor (R_{BIAS}) versus source impedance, for balanced or single-ended inputs.

INPUTS

Although the SSM-2015 inputs are fully floating, care must be exercised to ensure that both inputs have a DC bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 3(a), but an alternative way is to float the transducer and use two resistors to set the bias point as in Figure 3(b). The value of these resistors can be up to 10kΩ, but they should be kept as small as possible to limit common-mode noise. Noise generated in the resistors themselves is negligible since it is attenuated by the transducer impedance. Balanced transducers give the best noise immunity, and interface directly as in Figure 3(c).

TRIMMING

The gain of the SSM-2015 can be easily trimmed by adjustment of R_G. However, two further trims may be desirable: Offset Voltage and Common-mode Rejection, although the SSM-2015 provides excellent untrimmed performance in both respects.

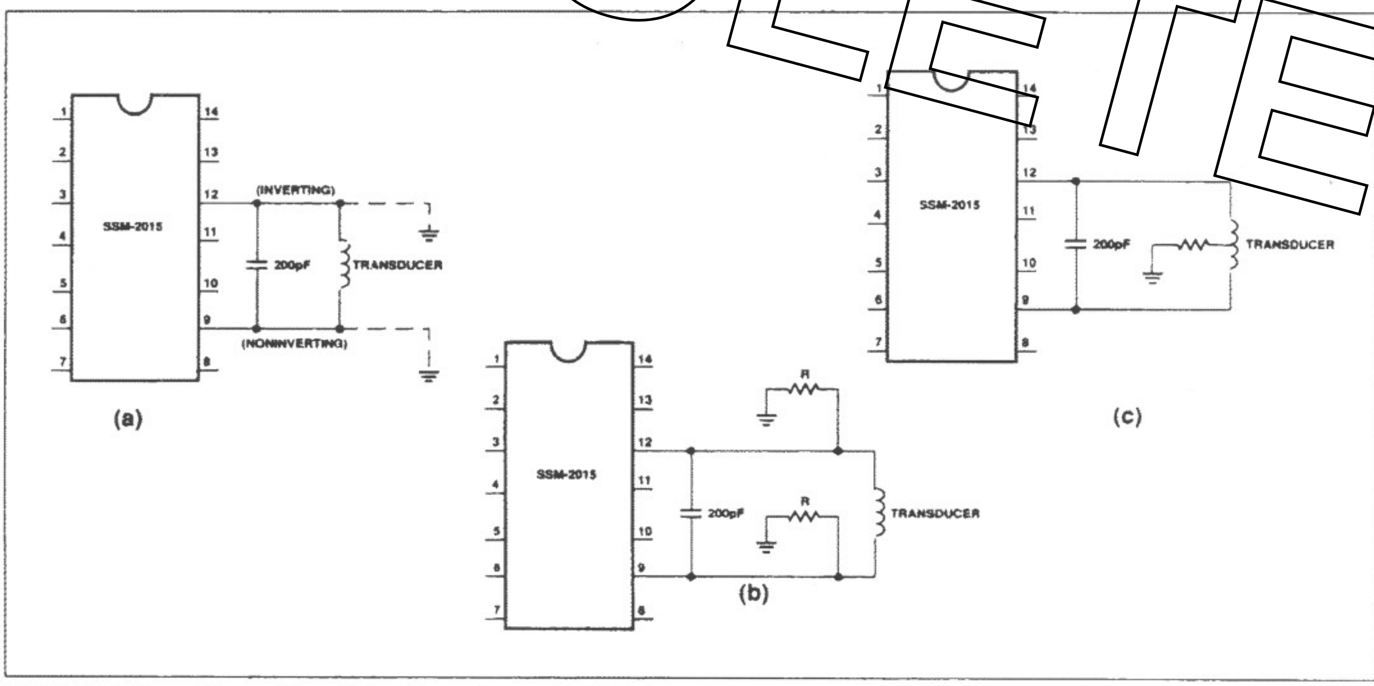


FIGURE 3: *Three Ways of Interfacing Transducers for High Noise Immunity*
(a) Single Ended (b) Pseudo Differential (c) True Differential

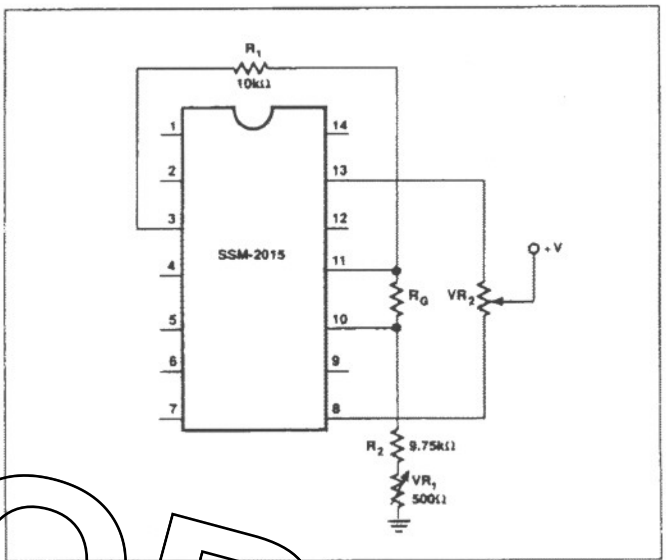


FIGURE 4: *Trimming the SSM-2015*

Figure 4 shows the trimming method for both parameters.

V_{R1} is the CMR trim and should be adjusted for minimum output with an 8Vp-p amplitude 60Hz Sine Wave common to both inputs.

V_{R2} is the offset voltage trim, and should be selected from Table 3. The offset trim should follow the CMR trim, since there is a small (non-reciprocal) interaction.

The offset trim can also be used to null out the gain control

The offset trim can also be used to null out the gain control feedthrough. The output offset at low gains is determined by matching of the feedback resistors while at high gains it is determined by the matching of the input resistors. If the gain setting is changed rapidly, the output shift can cause an (audible) click or thump. To reduce or eliminate this, the offset at high gains is adjusted to be equal to the offset at low gains.

TABLE 3: Recommended Values for the Offset Voltage Trim

	R_{BIAS}		
	27kΩ - 47kΩ	**47kΩ - 68kΩ**	**68kΩ - 150kΩ**
V_{R2}, G = 10	500kΩ	250kΩ	250kΩ
V_{R2}, G = 100	500kΩ	100kΩ	100kΩ
V_{R2}, G = 1000	250kΩ	100kΩ	50kΩ

PHANTOM POWER

A recommended circuit for phantom microphone powering is shown in Figure 5. Z_1 through Z_4 provide transient overvoltage protection for the SSM-2015 whenever microphones are plugged in and out.

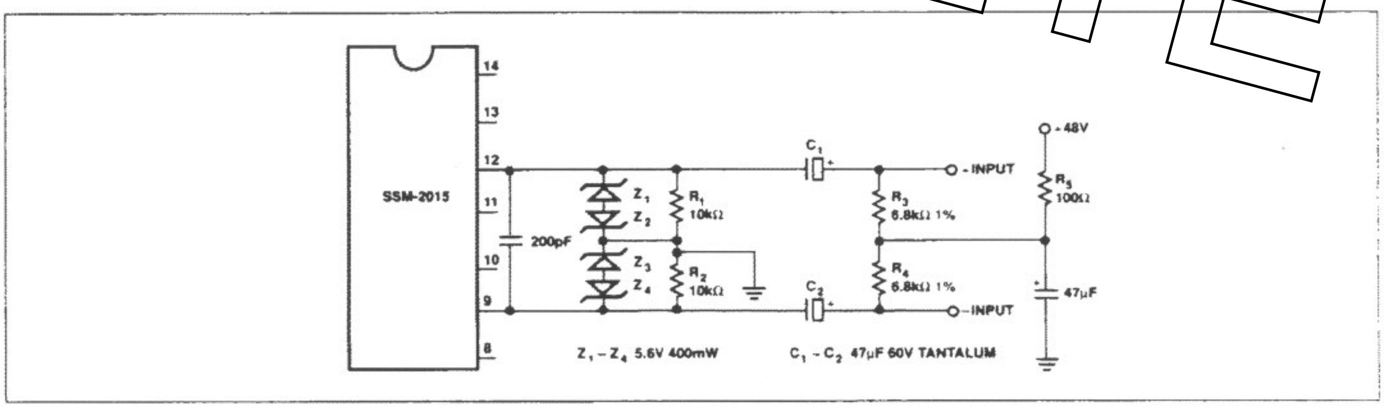


FIGURE 5: *SSM-2015 with Phantom Power*