SSM-2300

8-CHANNEL MULTIPLEXED SAMPLE-AND-HOLD

FEATURES

- On-Chip 1:8 Demultiplexer, 8 Sample-and-Hold Capacitors and 8 Output Buffers
- Saves Space, Reduces System Cost
- Output Buffers Stable for $C_L \leq 500pF$
- Output Swing Includes Negative Supply
- TTL and CMOS Compatible Logic Inputs
- 5 to 18 Volts Total Supply Operation
- Low Cost

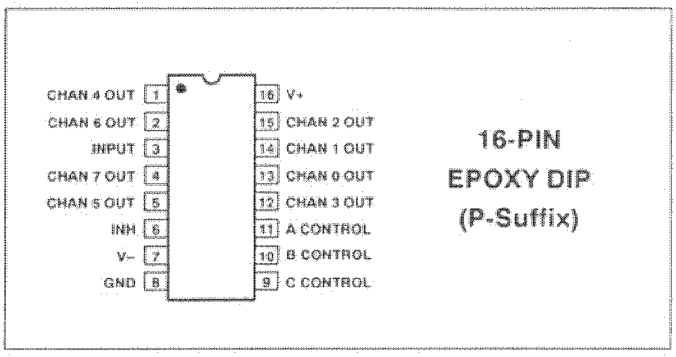
APPLICATIONS

- Automatic Test Equipment
- Process Control and Monitoring Systems
- Audio and Video Systems

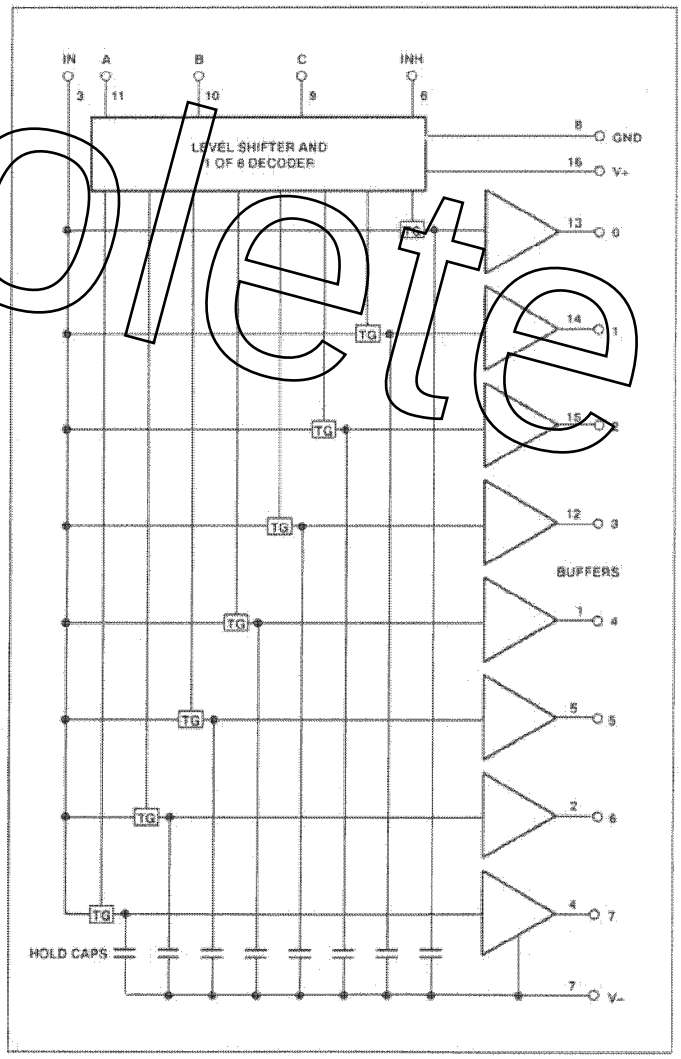
ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2300P	−25°C to +75°C

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The SSM-2300 is an eight-channel CMOS multiplexed sample-and-hold device designed for voltage level distribution in µP controlled systems. On-chip functions include an 8-channel demultiplexer, 8 sample-and-hold capacitors and 8 output buffers. This function saves valuable board space and reduces system cost where multiple voltage levels are required.

The SSM-2300 can operate from single or dual supplies with both TTL and CMOS logic compatibility. Useful for adjusting amplifier offsets or VCA gains, one or more SSM-2300s can be used with a single DAC to provide multiple set points within a system. Applications are in ATE, audio and video, process control and monitoring systems.

For improved performance and system upgrade, request the PMI SMP-08 data sheet.

ABSOLUTE MAXIMUM RATINGS

Total Supply Range 18V
Positive Supply ($V+ - V_{GND}$) 18V
Negative Supply ($V- - V_{GND}$) ..... –10V
Storage Temperature Range
P Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... 150°C
Operating Temperature Range ..... –25°C to +75°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
16-Pin Plastic DIP (P)	82	39	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for P-DIP.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V– = GND, T_A = +25°C, unless otherwise noted.

			SSM-2300			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_S		2	4	8	mA
Positive Supply Voltage	V+	$(V+ - V_{GND})$	5	–	18	V
Negative Supply Voltage	V–	$(V- - V_{GND})$	–10	–	0	V
Logic High (A, B, C, INH)	V_{INH}	See Table 1	6	–	–	V
Logic Low (A, B, C, INH)	V_{INL}	See Table 1	–	–	0.8	V
Channel Select Time	t_{ON}		–	300	–	ns
Channel Deselect Time	t_{OFF}		–	300	–	ns
Inhibit Recovery Time	t_{INH}		–	150	–	ns
Buffer Offset	V_{OS}	$0 < V_{IN} < +13V$	–	8	50	mV
Hold Step	V_{HS}	$0 < V_{IN} < +13V$	–	4	8	mV
Acquisition Time	t_A	$0 < V_{IN} < +13V$	–	1	–	µs
Settling Time	t_S	$0 < V_{IN} < +13V$	–	2	–	µs
Droop Rate	dV_{CH}/dt	$0 < V_{IN} < +13V$	–	500	1500	mV/s
Output Source Current	I_{SOURCE}	$0 < V_{IN} < +13V$	1.2	–	–	mA
Output Sink Current	I_{SINK}	V_{OUT} = V– = GND	0.5	–	–	mA
Input/Output Voltage Range	V_{IN}	R_L = 10kΩ to GND	0	–	11	V
Maximum Output Capacitive Load	$C_{L\ MAX}$		–	500	–	pF

Specifications subject to change; consult latest data sheet.

SIGNAL INPUT (PIN 3)

The signal input should be driven by a low impedance voltage source such as the output of an operational amplifier. The op amp should have a high slew rate and fast settling time if the SSM-2300's fast acquisition time characteristics are desired. As with all CMOS devices, all input voltages should be kept within range of the supply rails (i.e., V– ≤ inputs ≤ V+) to avoid latch-up.

If single supply operation is desired, an op amp such as the OP-21, OP-80, or OP-90 with input and output voltage compliance including GND, can be used to drive pin 3. Split supplies, such as ±7.5V, can be used for the SSM-2300 and the above mentioned op amps.

If the op amp driving pin 3 is powered by dual supplies, the circuit shown in Figure 1 should be used to avoid latch-up due to negative transients during power-up. The addition of a small capacitor as shown may be useful in preventing a large false hold step.

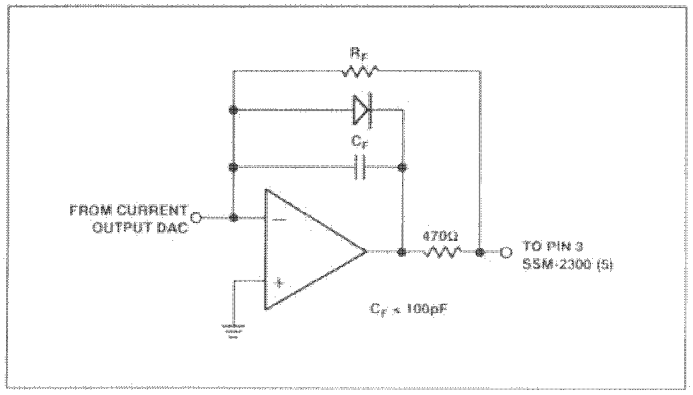


FIGURE 1: *DAC Interface Circuit (SSM-2300 Single Supply, Op Amp Driver Split Supply)*

LOGIC INPUTS (PINS 6, 9, 10 AND 11)

For V+ supplies up to +7.5 V, logic inputs can be driven by TTL or CMOS. For V+ (of the SSM-2300) from +7.5V to +12V, TTL outputs should add pull-up resistors to the +5V logic supply. For V+ of +12V or greater, CMOS logic should be used (see Table 1).

TABLE 1: Control Input Switch Points (Volts)

V+	GND	V–	V_{IH}	V_{IL}
5	0	–5	2.4	0.8
5	0	–10	2.4	0.8
3	0	–12	2	0.8
7.5	0	–7.5	3	0.8
15	0	0	6	0.8
12	0	0	5	0.8

If TTL is used to drive the logic inputs, the V+ supply should be designed to come up before the logic supply, or, current limiting (< 10mA) resistors should be connected in series with the inputs to avoid a potential latch-up condition. Open collector or 74C series logic avoid this problem because of their limited current sourcing capability.

TABLE 2: Channel Decoding

Pin 9 C	Pin 10 B	Pin 11 A	Pin 6 INH	CH	Pin
0	0	0	0	0	13
0	0	1	0	1	14
0	1	0	0	2	15
0	1	1	0	3	12
1	0	0	0	4	1
1	0	1	0	5	5
1	1	0	0	6	2
1	1	1	0	7	4
X	X	X	1	NONE	–

Table 2 shows the channel decoding for the SSM-2300 which is identical to that of 4051 type devices. When there is an address change, it is possible for two or more channels to momentarily be connected to the input at the same time. In order to avoid potential crosstalk problems, either the input signal should be kept at its previous level for 500ns after the address change (Figure 2a) or preferably INH (pin 6) should be exercised as in Figure 2b.

SUPPLIES (PINS 7, 8, AND 16)

The supply voltages V+ and V– establish the input and output voltage range which is :

V– ≤ inputs, outputs ≤ V+ – 2V

V+ and GND determine the control input logic levels and switch points (see Table 1).

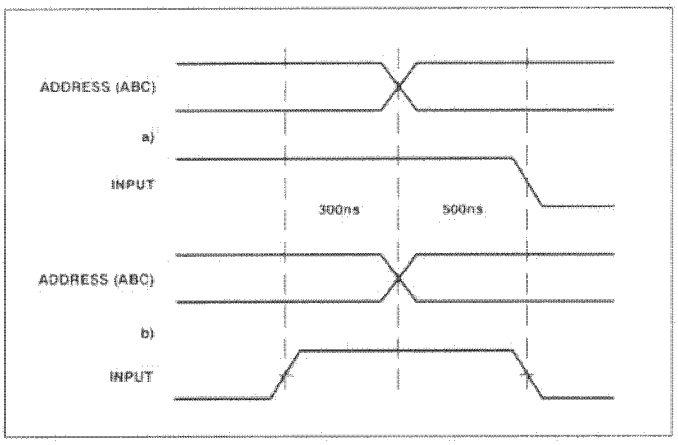


FIGURE 2: *Decode Timing*

The total supply range is 7 to 15V nominal and 5 to 18V absolute maximum, however, several specifications including acquisition time, offset, and output voltage compliance will degrade for a total supply less than 7V. The positive supply current is typically 4mA with the outputs unloaded. If split supplies are used, the negative supply should be bypassed (i.e., parallel 0.1µF and 10µF capacitors to GND). The hold capacitors are connected to this supply pin and any noise on it will feed through to the outputs.

SUPPLY SEQUENCING

If TTL logic is used, the SSM-2300 V+ supply should be designed to come up before the logic supply, otherwise current limiting resistors should be connected in series with the logic inputs to prevent latch-up. Resistors should be chosen to limit current below 10mA.

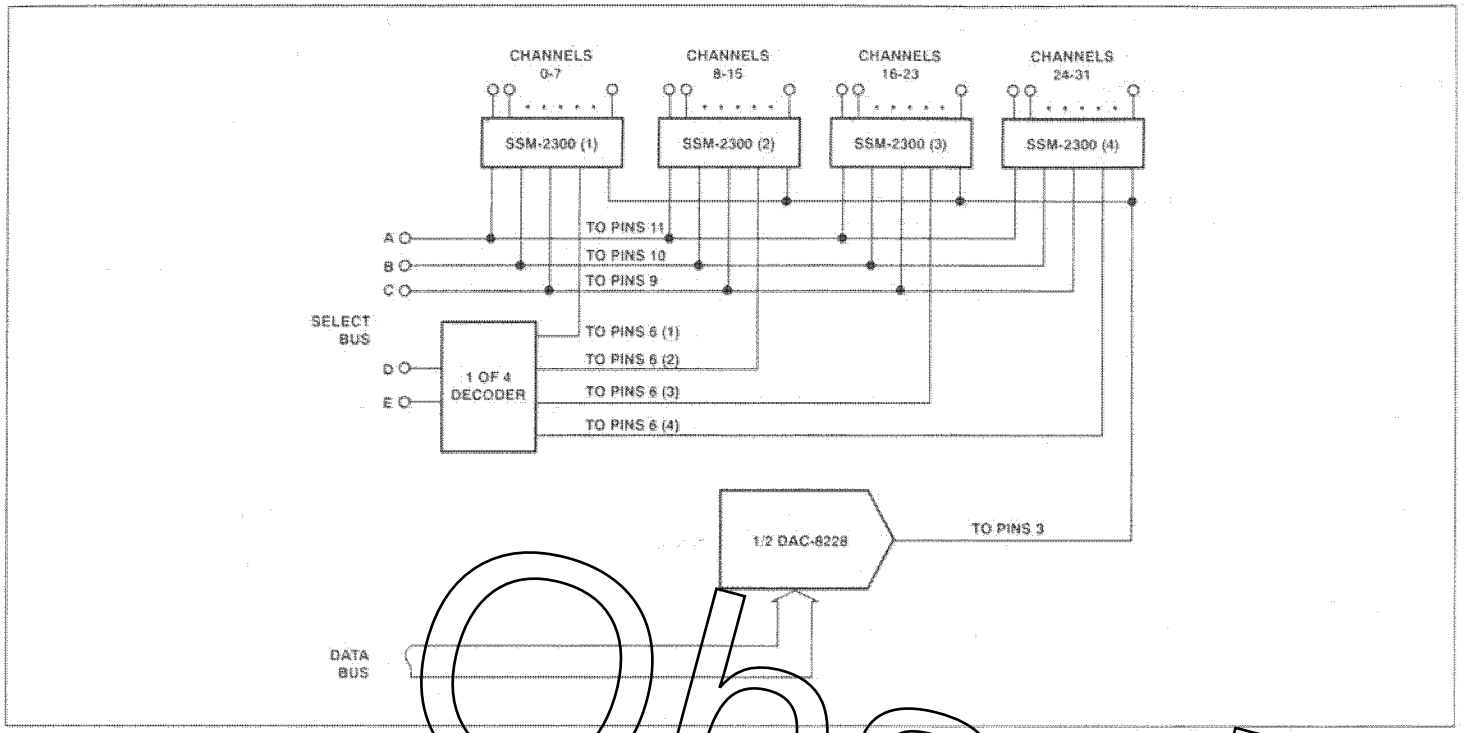
OUTPUT BUFFERS (PINS 1, 2, 3, 4, 5, 12, 13, 14, AND 15)

The buffer offset specification is ±50mV. This is approximately 1 LSB of an 8-bit DAC with a 10V full scale. The change in offset over the output range is typically 3mV. The hold step (the voltage shift when a channel is deselected) is about 4mV with little variation. The droop rate of a held channel is ±500mV/second typical and ±1500mV/second maximum (input and output(s) at opposite extremes of the voltage compliance range).

The buffers were designed primarily to drive loads connected to ground. The outputs can source more than 1.2mA each over the full voltage output range, but have limited current sinking capability near V–. In split supply operation, symmetrical output swing can be obtained by restricting the output range to 2V from either supply. The output impedance with the output sourcing current is approximately 0.1Ω. With the output sinking current, the impedance is approximately 1Ω.

The SSM-2300 buffers eliminate potential stability problems associated with external buffers as the outputs are stable with capacitive loads up to 500pF. However, the SSM-2300 buffer outputs are not short-circuit protected. Care should be taken to avoid shorting any of the outputs to the supplies or ground.

TYPICAL APPLICATION



GENERAL INFORMATION

HANDLING

By design consideration, the SSM-2300 gate inputs have a resistor/ diode protection network. Inherent P-N junction diodes provide diode protection for all gate inputs and outputs. At the input and output interfaces, the diode networks of the SSM-2300 are protected from gate-oxide failure (70 - 100 volt limit) for static discharge or signal voltages up to 1,000 to 2,000 volts under most transient or low current conditions.

OPERATING

All unused inputs should be connected to either V+ or V– depending on the appropriate logic circuit. For connector-driven inputs which may temporarily become unterminated, a pull-up resistor to V+ or V– should be used with a value ranging from 0.2 to 1MΩ.

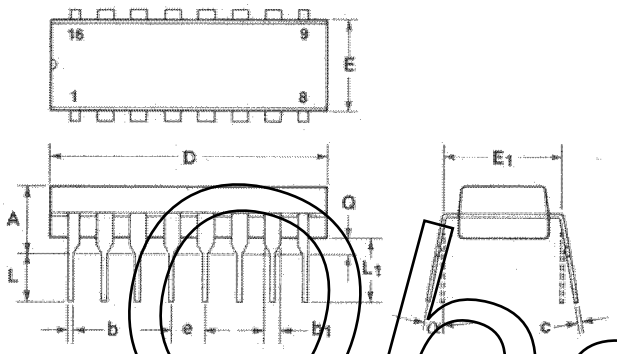
NOTE: Do not apply signals to the SSM-2300 with power off unless the input current's value is limited to less than 10mA.

APPLICATIONS

For signal frequencies near DC, almost any number of SSM-2300s can be connected in parallel; for example, in process control applications this allows a single DAC to service many control channels simultaneously (see Typical Application schematic). The 1μs acquisition time, the number of channels, and the address timing determines the maximum update rate. Sixteen channels of full band audio can be demultiplexed with a single DAC and two SSM-2300s.

PACKAGE DIMENSIONS — EPOXY DIPS

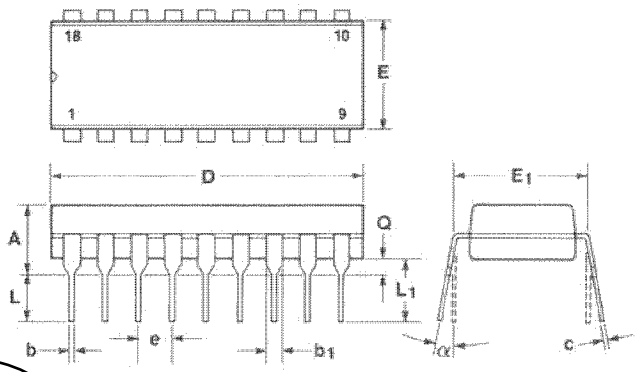
16-Lead Epoxy Dip (P-Suffix)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.210	—	5.33	
b	0.014	0.022	0.356	0.558	—
b_1	0.045	0.070	1.15	1.77	—
c	0.008	0.015	0.20	0.38	—
D	0.745	0.840	18.92	21.33	3
E	0.240	0.280	6.10	7.11	3
E_1	0.300	0.325	7.62	8.25	2
e	0.100 BSC		2.54 BSC		—
L	0.115	0.160	2.92	4.06	—
L_1	0.130	—	3.30	—	—
Q	0.015	—	0.38	—	—
α	0°	15°	0°	15°	—

NOTES:
1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E_1" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusion.

18-Lead Epoxy Dip (P-Suffix)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.210	—	5.33	—
b	0.014	0.022	0.356	0.558	—
b_1	0.045	0.070	1.15	1.77	—
c	0.008	0.015	0.20	0.38	—
D	0.845	0.925	21.46	23.49	3
E	0.240	0.280	6.10	7.11	3
E_1	0.300	0.325	7.62	8.25	2
e	0.100 BSC		2.54 BSC		—
L	0.115	0.160	2.92	4.06	—
L_1	0.130	—	3.30	—	—
Q	0.015	—	0.38	—	—
α	0°	15°	0°	15°	—

NOTES:
1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E_1" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusion.