Arria II GX FPGA Development Board
Overview

Introduction

Signal Integrity Analysis

The ArriaII GX development kit board has several high speed interfaces. Each of these interfaces has its own set of signal integrity challenges

1. The PCI Express X8 edge connector, data speeds up to 2.5G
2. The HSMC port HSMA, data speeds up to 6.375G baud
3. DDR2 SODIMM running with a 333MHz clock
4. DDR3 devices on board running with a 400 MHZ clock

Post Layout Analysis

Below you will find documentation for each interface on the Arria II GX FPGA Development Board.

Table of Contents

Stackup and Material

Part #: A2GX_PCI_14 LYR #3	Rev	Finished Thickness: 0.0620 +/- 0.0060	Finished Over: All
		Lam Thickness: 0.0580 +/- 0.0040	Material Type: Isola 370HR

Impedance Requirements: L#	Impedance Type	Orig Line	Fin. Line	Ref Pln	2nd Ref Pln	Targeted Desired Impedance	Impedance Tolerance	Actual Calculated Impedance	Diff Line Centers	Diff Line Space	Original Coplanar Spacing	Finished Coplanar Spacing
1	DIF-Coated Microstrip Edg Cpld	.00400	.00425	2		100.00 Ω	+/- 10%	99.55 Ω	.01000	.00575		
1	DIF-Coated Microstrip Edg Cpld	.00500	.00500	2		100.00 Ω	+/- 10%	98.86 Ω	.01300	.00800		
1	SE-Coated Microstrip	.00600	.00600	2		50.00 Ω	+/- 10%	50.65 Ω				
1	DIF-Coated Microstrip Edg Cpld	.00625	.00600	2		85.00 Ω	+/- 10%	85.05 Ω	.01125	.00525		
4	DIF-Dual Stripline Edg Cpld	.00400	.00400	3	6	100.00 Ω	+/- 10%	99.39 Ω	.01000	.00600		
4	SE-Dual Stripline	.00500	.00475	3	6	50.00 Ω	+/- 10%	49.03 Ω				
5	DIF-Dual Stripline Edg Cpld	.00400	.00400	6	3	100.00 Ω	+/- 10%	99.39 Ω	.01000	.00600		
5	SE-Dual Stripline	.00500	.00475	6	3	50.00 Ω	+/- 10%	49.03 Ω				
10	DIF-Dual Stripline Edg Cpld	.00400	.00400	9	12	100.00 Ω	+/- 10%	99.39 Ω	.01000	.00600		
10	SE-Dual Stripline	.00500	.00475	9	12	50.00 Ω	+/- 10%	49.03 Ω				
11	DIF-Dual Stripline Edg Cpld	.00400	.00400	12	9	100.00 Ω	+/- 10%	99.39 Ω	.01000	.00600		
11	SE-Dual Stripline	.00500	.00475	12	9	50.00 Ω	+/- 10%	49.03 Ω				
14	DIF-Coated Microstrip Edg Cpld	.00400	.00425	13		100.00 Ω	+/- 10%	99.55 Ω	.01000	.00575		
14	SE-Coated Microstrip	.00600	.00600	13		50.00 Ω	+/- 10%	50.65 Ω				
14	DIF-Coated Microstrip Edg Cpld	.00600	.00600	13		100.00 Ω	+/- 10%	98.86 Ω	.01300	.00700		
14	DIF-Coated Microstrip Edg Cpld	.00625	.00600	13		85.00 Ω	+/- 10%	85.05 Ω	.01125	.00525		

Controlled Impedance Notes:

Lamination Stackup: L#/Type	Description:	Thickness and Tolerances: Cu+:	Laminate/PrePreg:		Base Material Rqmts: Type:	Description:
1 Sig	Foil (H oz)	.00060				
	Pre-Preg (1 x 2113)		.0039	+/- 0.0004		Isola 370HR
2 Pln	Core 0.0020 1/1	.00120	.0020			Isola 370HR
3 Pln		.00120				
	Pre-Preg (1 x 2113)		.0035	+/- 0.0004		Isola 370HR
4 Sig	Core 0.0060 H/H	.00060	.0060			Isola 370HR
5 Sig		.00060				
	Pre-Preg (1 x 2113)		.0035	+/- 0.0004		Isola 370HR
6 Pln	Core 0.0020 1/1	.00120	.0020			Isola 370HR
7 Pln		.00120				
	Pre-Preg (1 x 1080)		.0028	+/- 0.0003		Isola 370HR
8 Pln	Core 0.0020 1/1	.00120	.0020			Isola 370HR
9 Pln		.00120				
	Pre-Preg (1 x 2113)		.0035	+/- 0.0004		Isola 370HR
10 Sig	Core 0.0060 H/H	.00060	.0060			Isola 370HR
11 Sig		.00060				
	Pre-Preg (1 x 2113)		.0035	+/- 0.0004		Isola 370HR
12 Pln	Core 0.0020 1/1	.00120	.0020			Isola 370HR
13 Pln		.00120				
	Pre-Preg (1 x 2113)		.0039	+/- 0.0004		Isola 370HR
14 Sig	Foil (H oz)	.00060				

Target Post-Lam Thickness: 0.0580 +/- 0.0040

Copper Oz Legend: H=1/2oz T=3/8oz Q=1/4oz E=1/8oz S=1/16oz

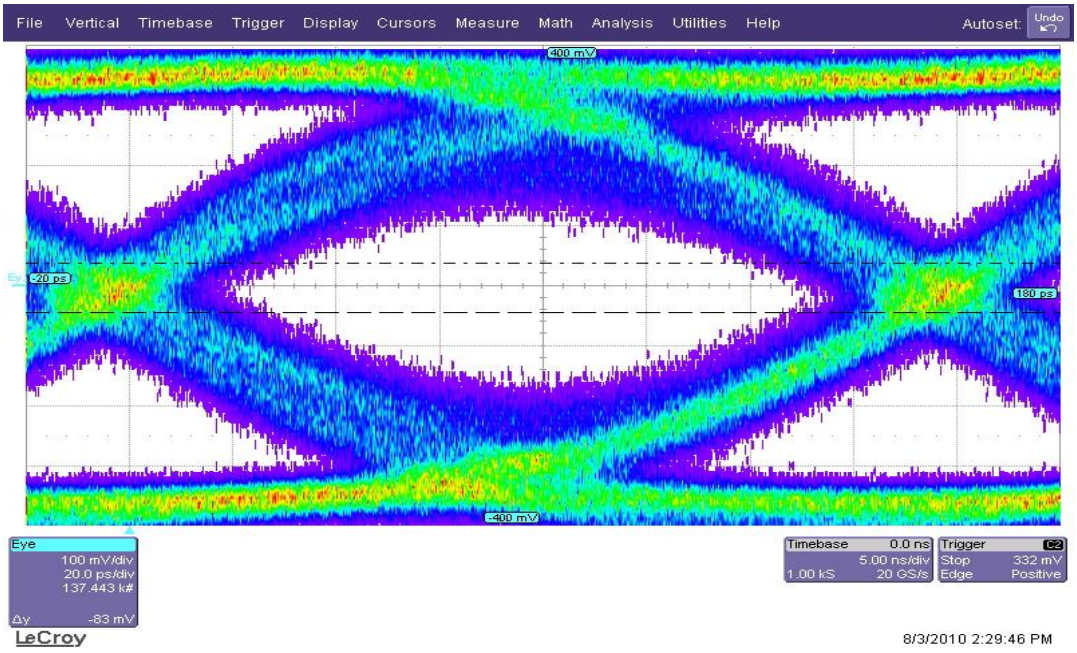
Stackup Notes:

PCI Express X8 edge connector

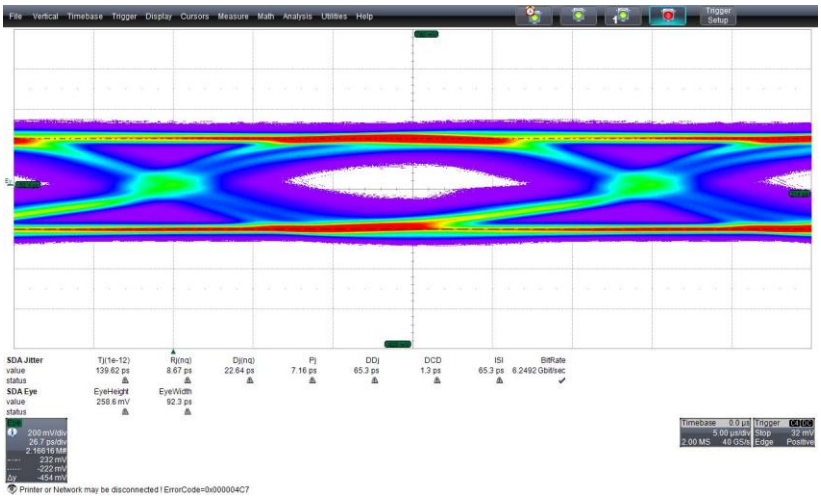
HSMC port HSMA

Transmit Eye, Channel 0

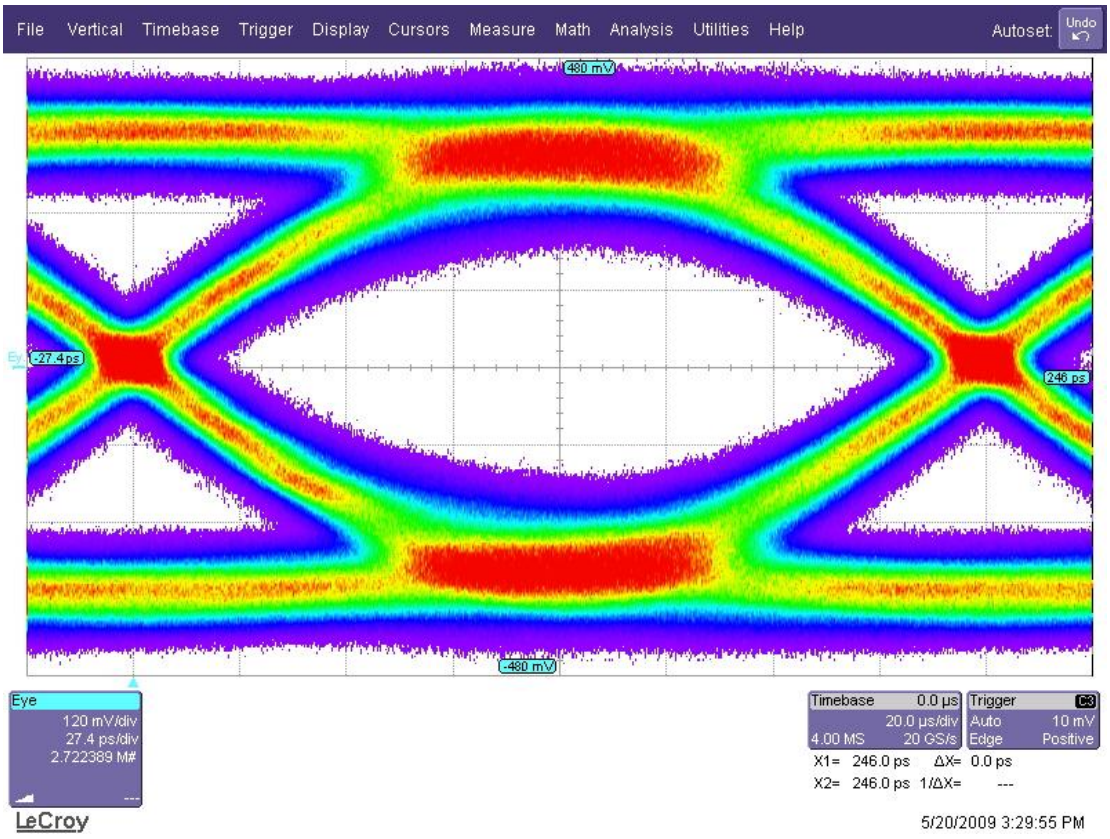
Measured Eye 1, 1 minute



PRBS15



Receive Eye


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
Autoset:
Undo
480 mV
-27.4 ps
246 ps
-480 mV
Eye
120 mV/div
27.4 ps/div
2.722389 M#
Timebase 0.0 ps
20.0 µs/div
4.00 MS 20 GS/s
Trigger C3
Auto 10 mV
Edge Positive
X1= 246.0 ps ΔX= 0.0 ps
X2= 246.0 ps 1/ΔX= ---
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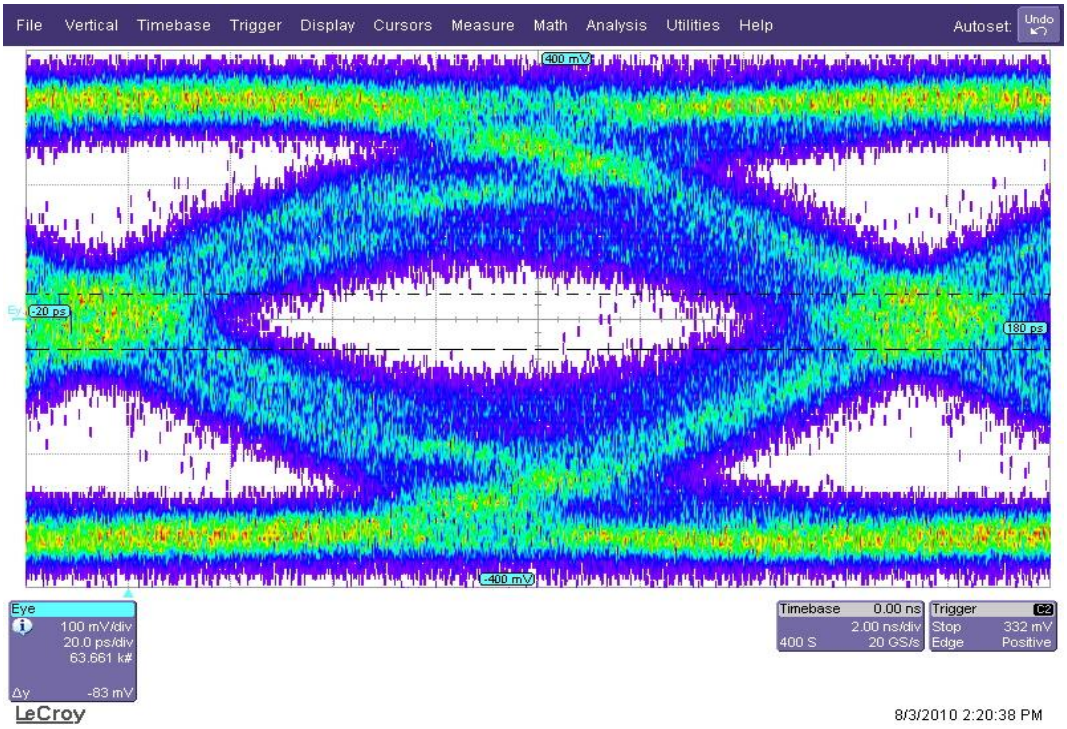
5/20/2009 3:29:55 PM

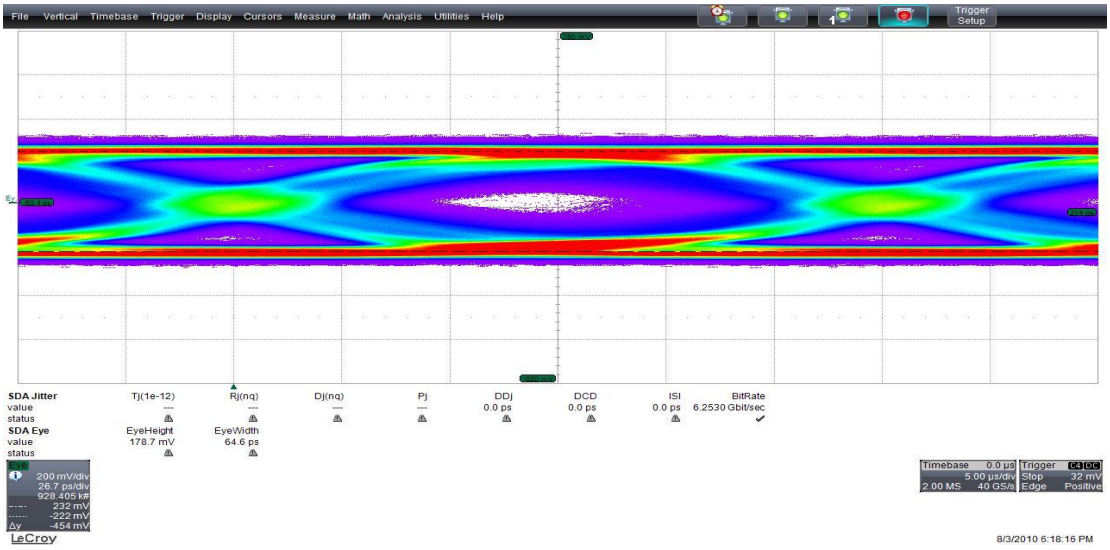
HSMC port HSMB

Transmit Eye, Channel 0

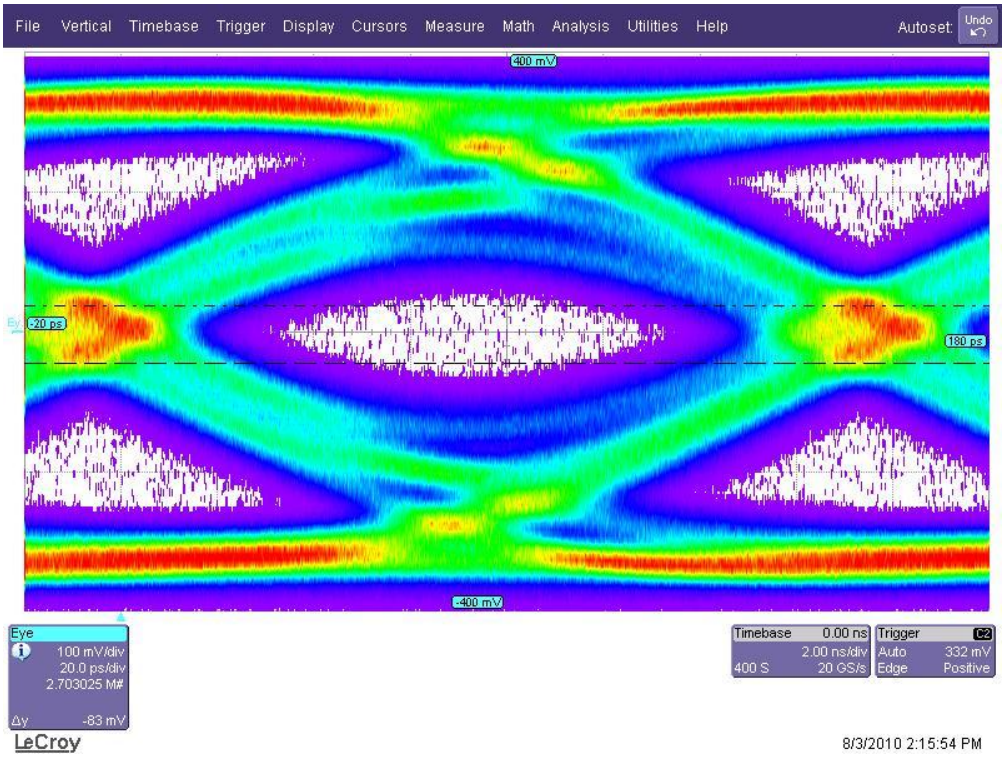
1 Minute



PRBS15



1 Hour


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
Autoset: Undo
400 mV
-20 ps
180 ps
-400 mV
Eye
100 mV/div
20.0 ps/div
2.703025 M#
Δy -83 mV
Timebase 0.00 ns
2.00 ns/div
400 S 20 GS/s
Trigger C2
Auto 332 mV
Edge Positive
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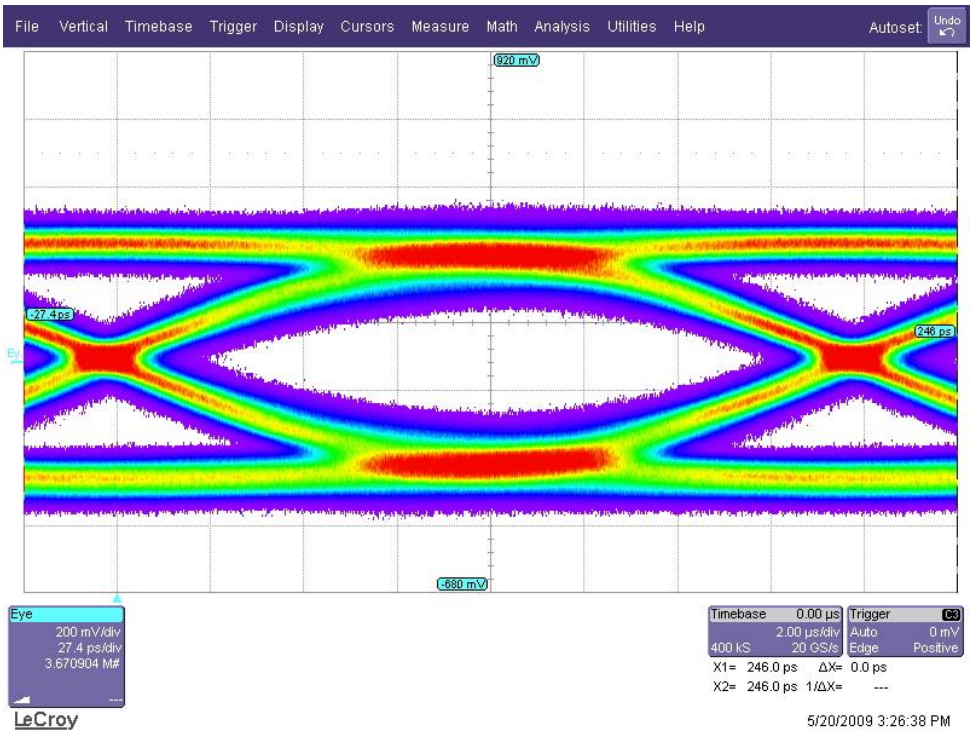
8/3/2010 2:15:54 PM

Receive Eye


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
Autoset: Undo
920 mV
-27.4 ps
246 ps
-680 mV
Eye
200 mV/div
27.4 ps/div
3.670904 M#
Timebase 0.00 µs
2.00 µs/div
400 kS 20 GS/s
Trigger C3
Auto 0 mV
Edge Positive
X1= 246.0 ps ΔX= 0.0 ps
X2= 246.0 ps 1/ΔX= ---
LeCroy
5/20/2009 3:26:38 PM

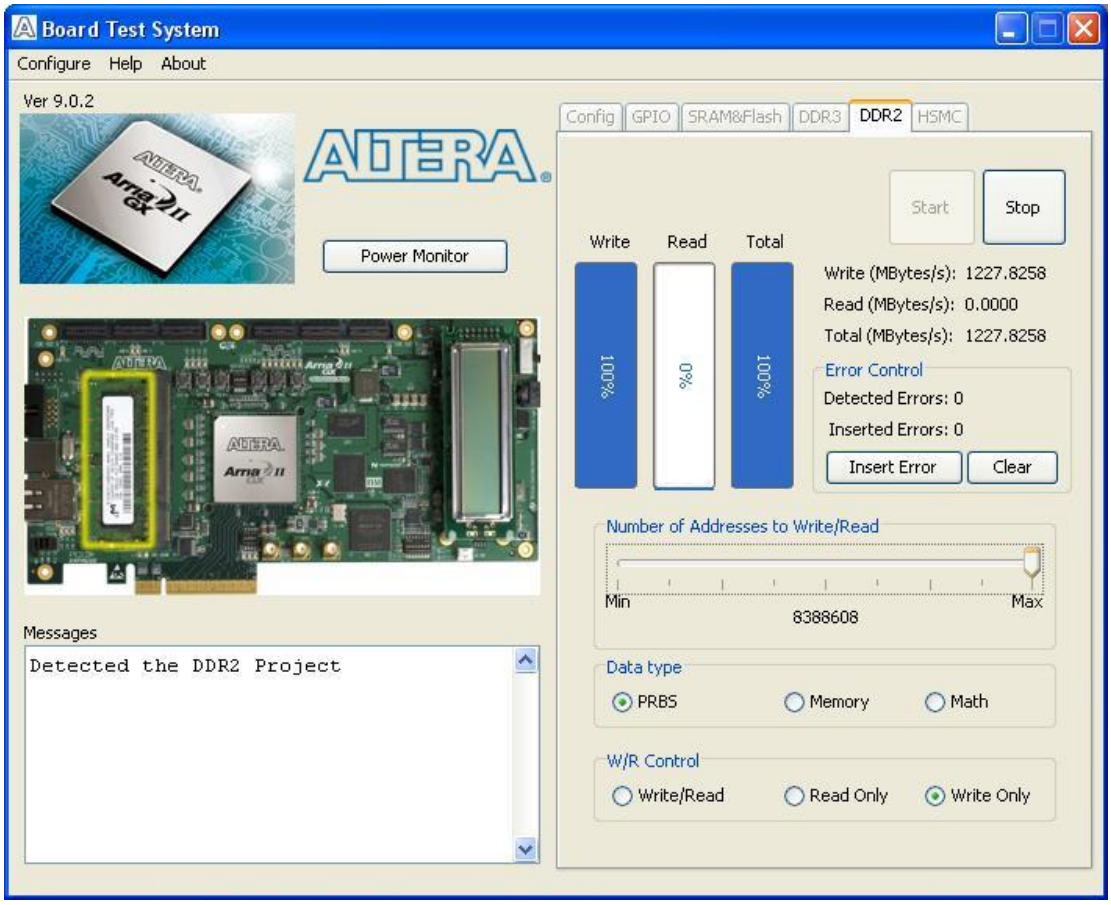
DDR2 SODIMM Interface

Measurements were made on the DDR2 SODIMM interface using the Board Test System user interface.

The Address, Control and Data Out measurements were made by setting the slider labeled “Number of Addresses to Read / Write” to the maximum. Data for the Clock, Control and Data out are made selecting the “Write Only” radio button and “Start”.

Data in to the FPGA is gathered using the “Read Only” button.

☞ Be sure that the dip switches are set up as indicated in the user guide and Reference manual.



Simulations were done in HyperLynx on the finished artwork using IBIS models for the ArriaII GX. These models are available on the Altera web site or generated from QuartusII after the design is finished.

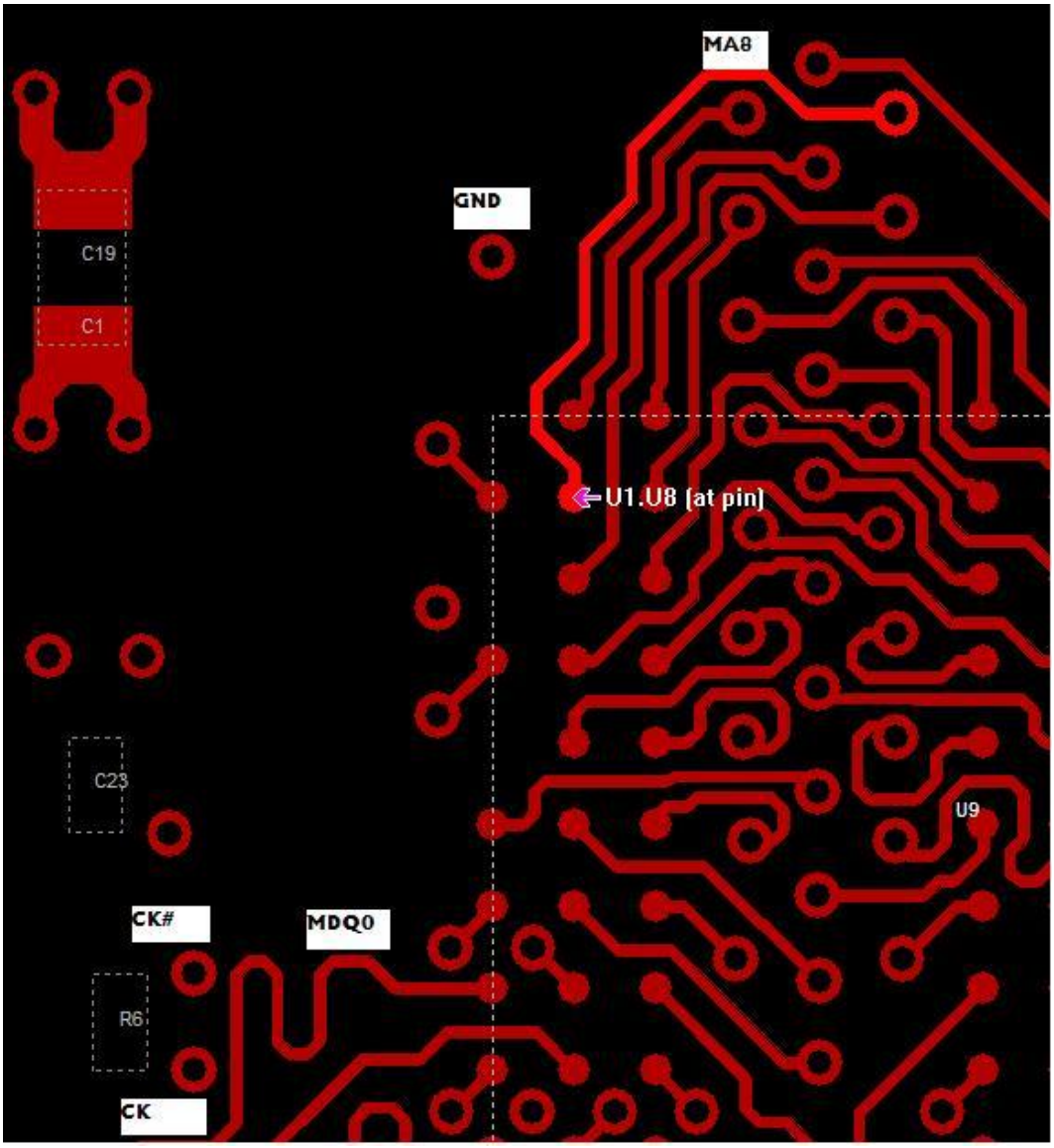
The drive strengths listed for the interface match the IBIS model naming convention. These are easily translated into settings in the design pin planner window.

Oscilloscope shots were done on finished board.

Many of the differential signals were also analyzed single ended for the benefit of users who do not have access to a differential probe.

Probe Points for SODIMM board

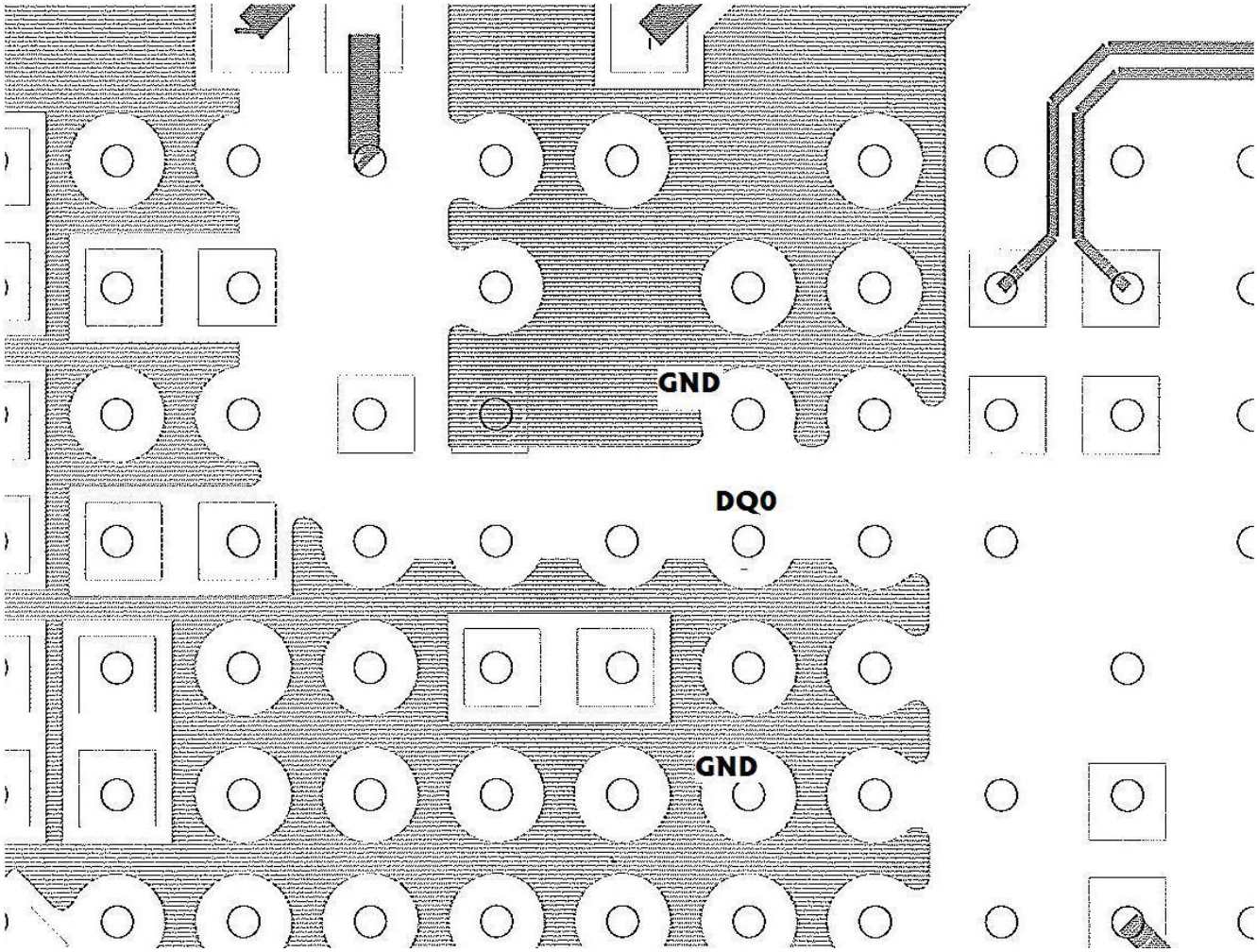
The SODIMM was probed at the points indicated below. The technique for creating this kind of map are explained at the end of this document



☞ The signals we will examine are A8, DQ0 (during write) and CK0. The points of measurement were chosen to be convenient to probe. The signal will look different on the chip. It would be nice to probe the actual device but that is not possible. Probing correctly will require scraping some soldermask off of the MDQ0 trace. Also scraping some soldermask off of the ground plane near the places you want to probe may be needed to keep the ground connection as short as possible for signal integrity.

Probe points at the FPGA

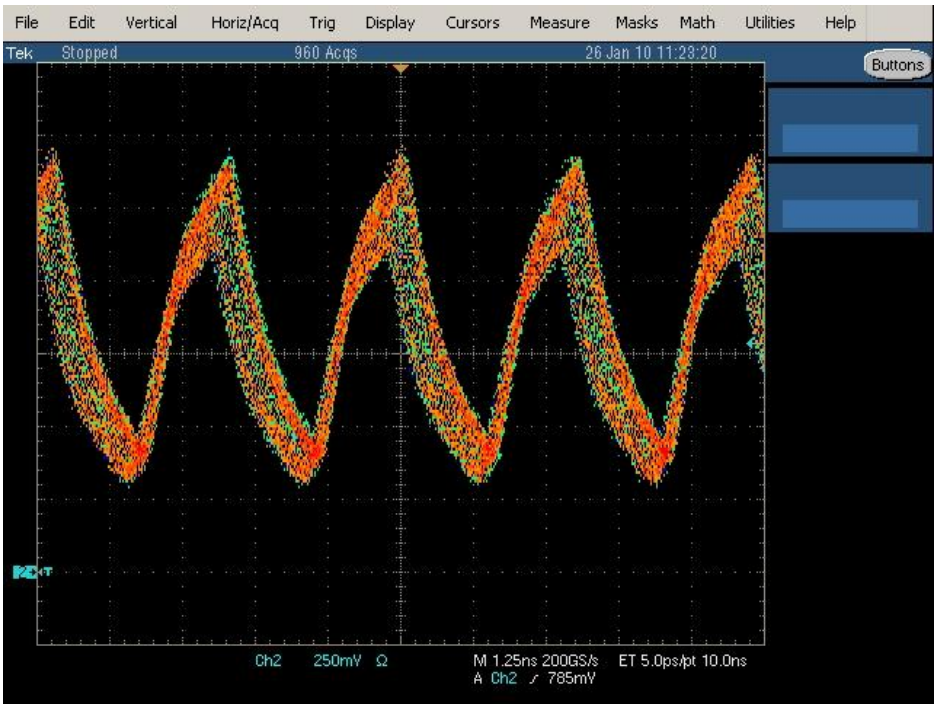
Viewing the bottom of the board



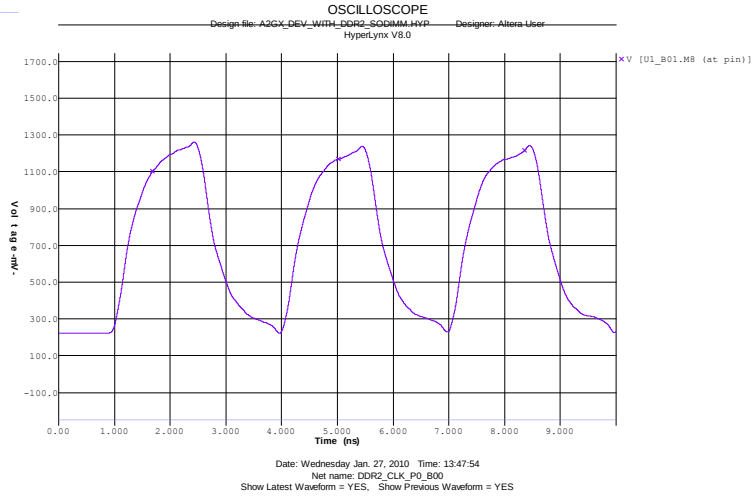
☞ On this map we show where we probed signal DQ0 on the FPGA during read operation. This on the far side via. The signal will look different on the chip.

DDR2_CLK

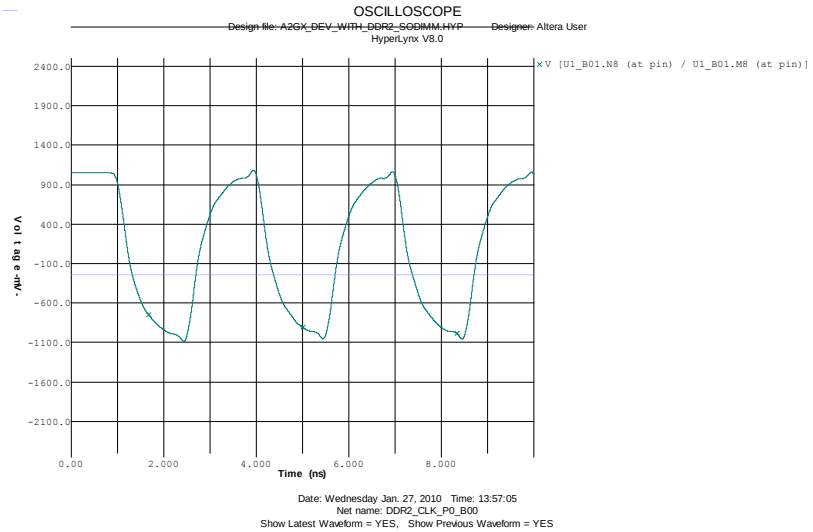
The DDR SODIMM system is clocked at 333MHz.



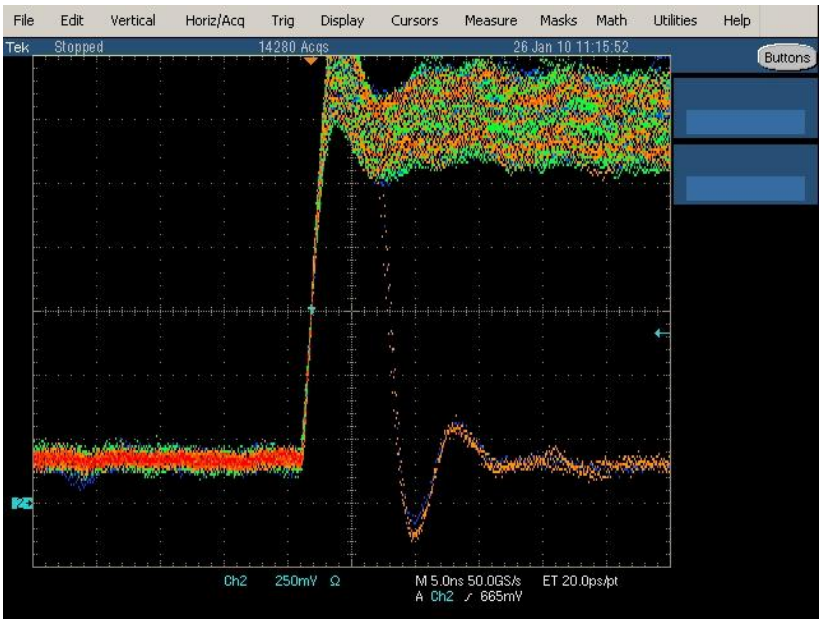
Compare to trace in Simulation for single ended measurement



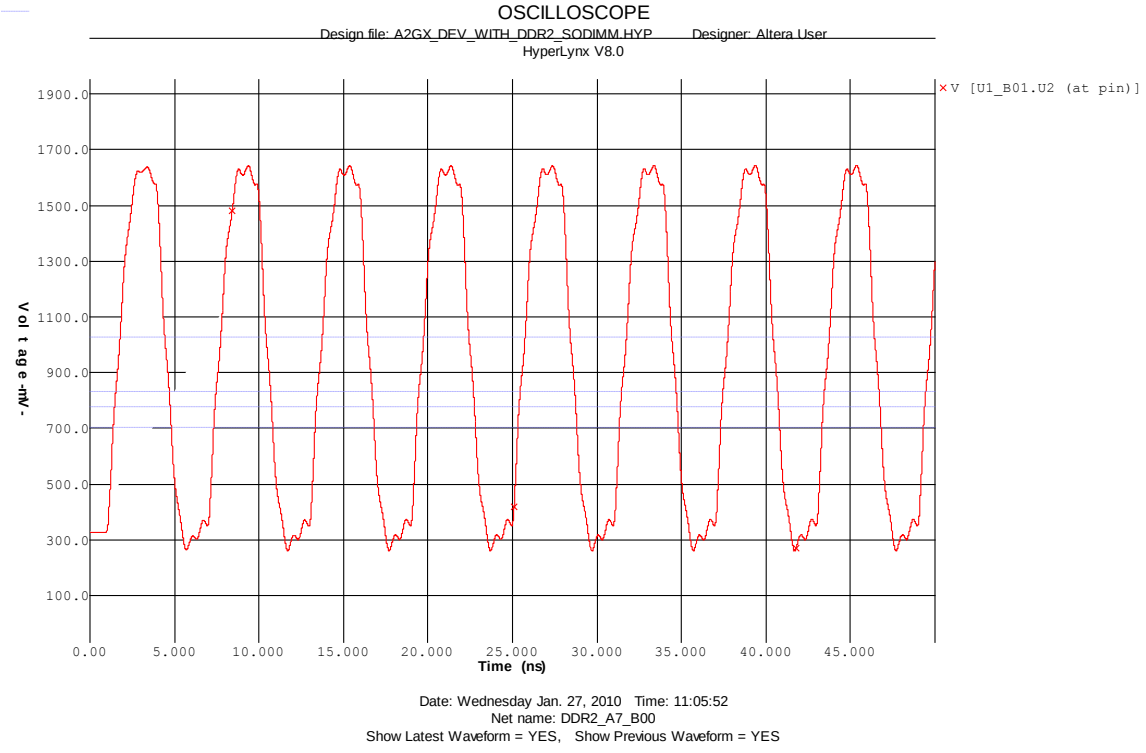
Differential Simulation



DDR2_A7 at via on SODIMM

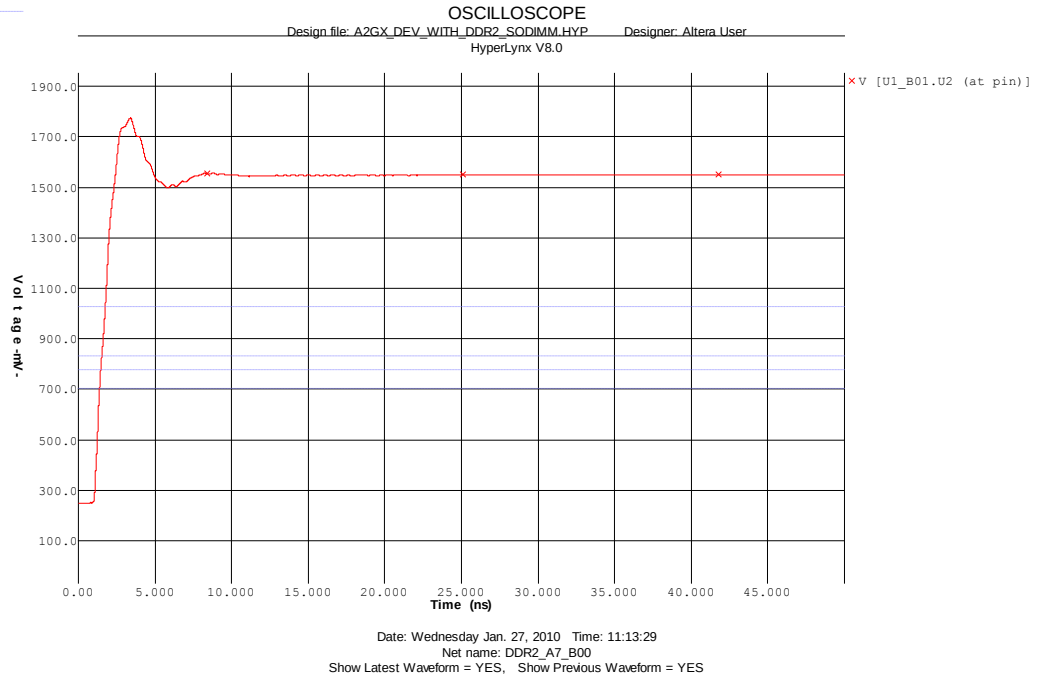


167MHz sstl18c1_cio_d8s3

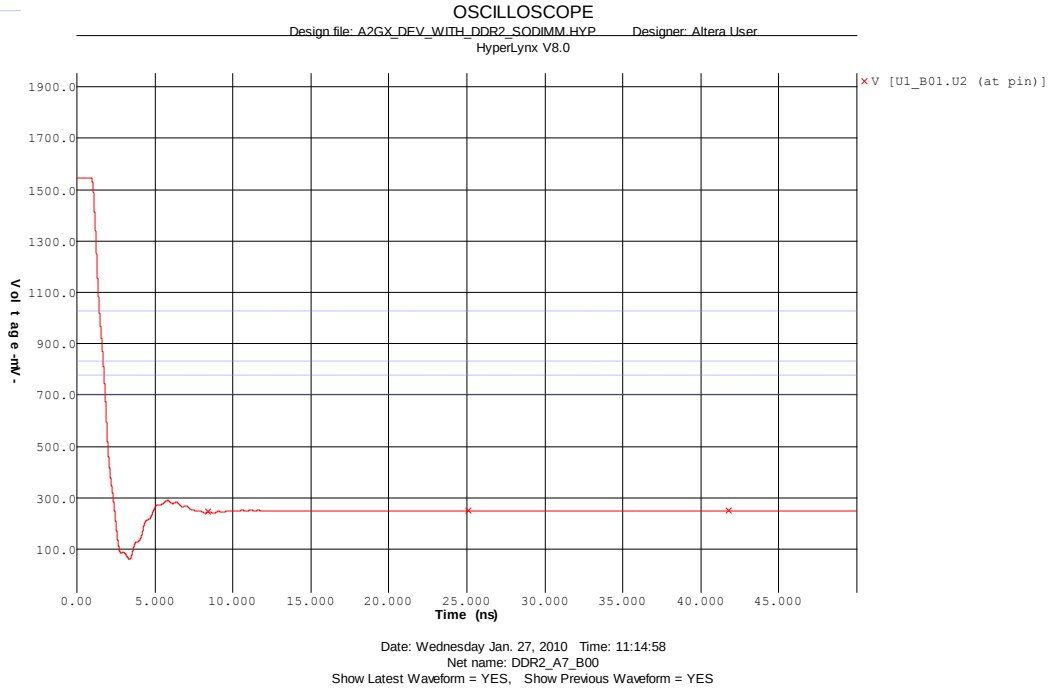


Here we are providing transient waveforms to show how the overshoot looks.

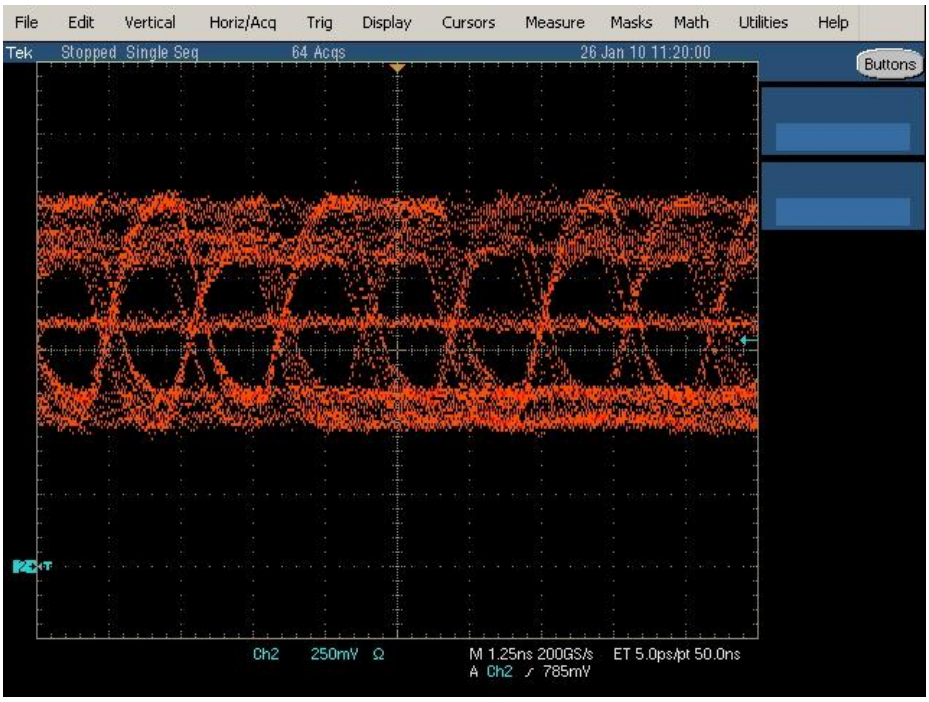
DDR2 A7 167MHz sstl18c1_cio_d10s3 Rising



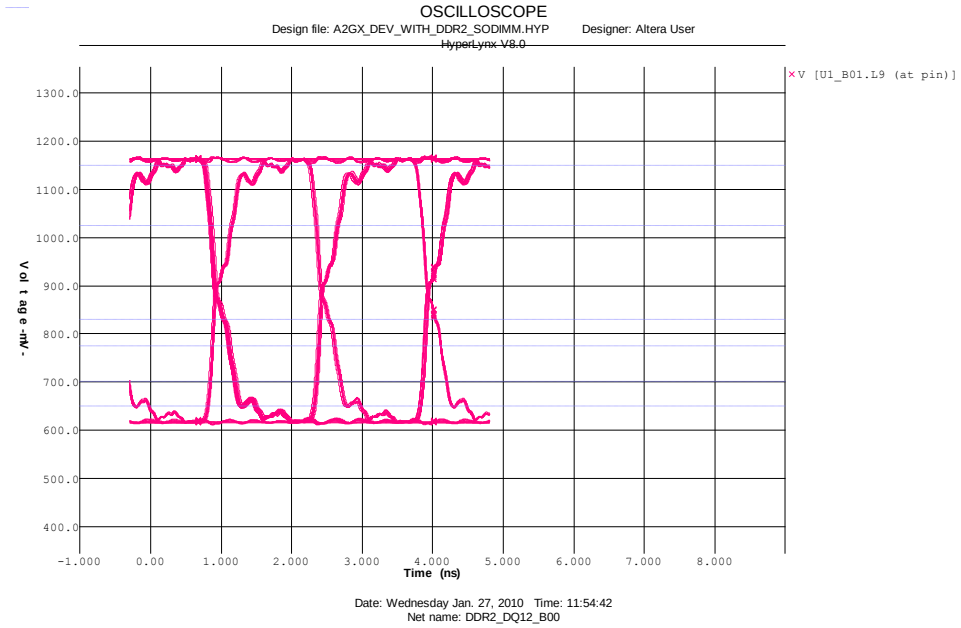
DDR2 A7 167MHz sstl18c1_cio_d10s3 falling



DDR2_DQ12 at via on SODIMM

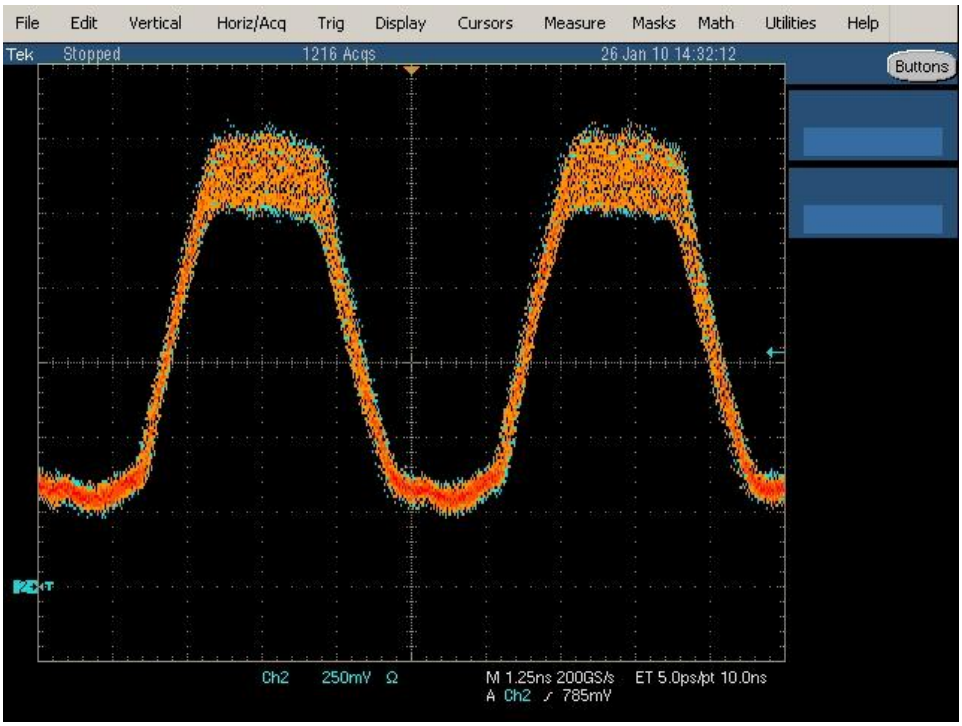


Sstl18c1_c1_d12s3

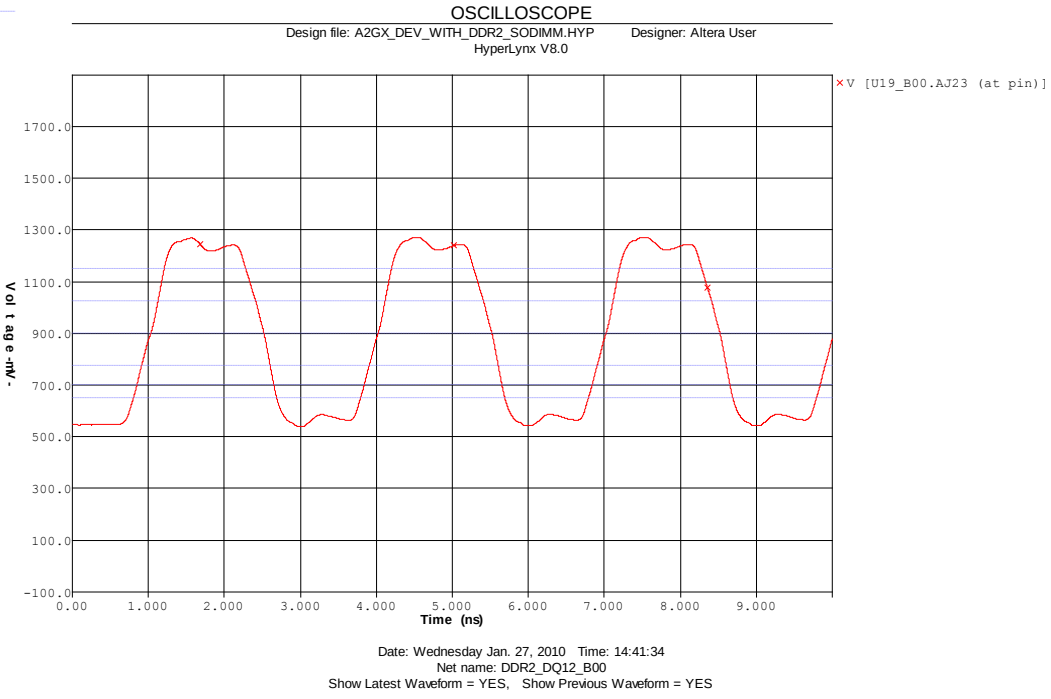


Good

DDR2_DQ12 at via below FPGA



Simulation



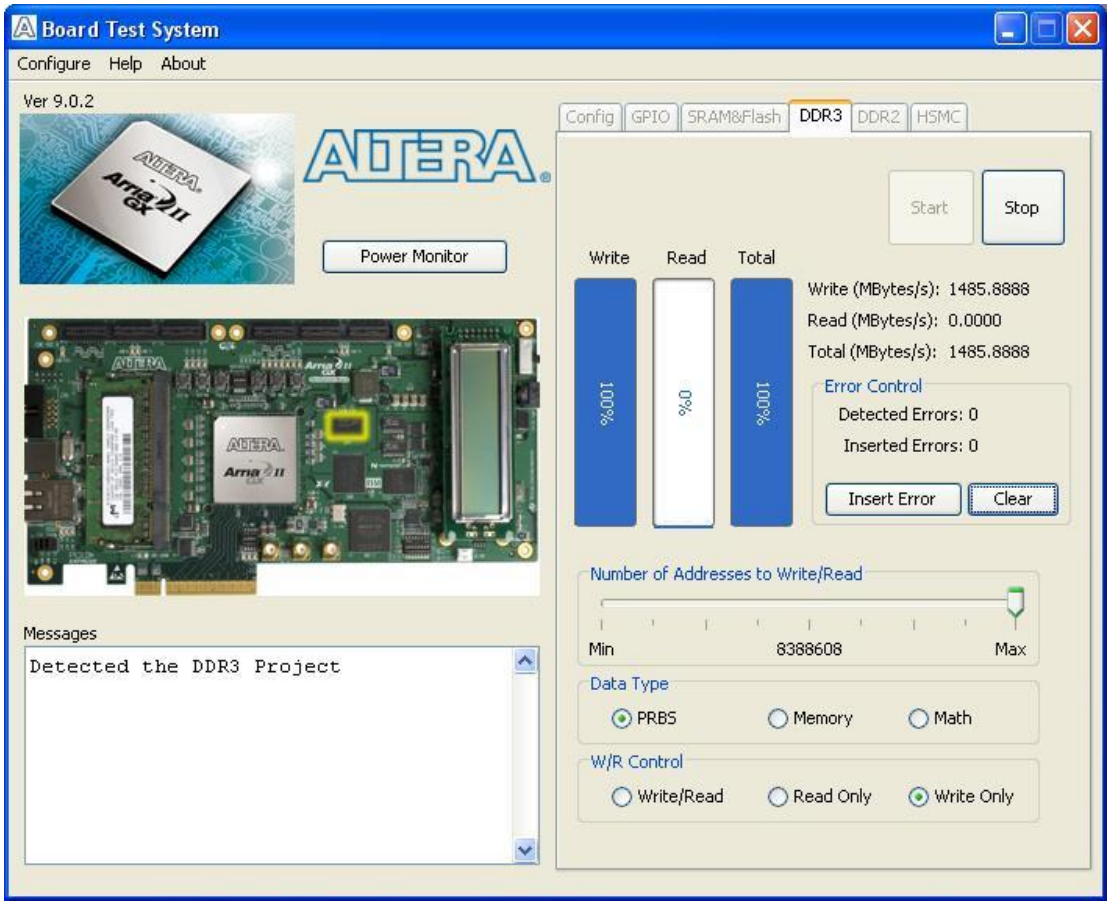
DDR3 Chip Interface

Measurements were made on the DDR3 chip interface by setting the slider labeled “Number of Addresses to Read / Write” to the maximum. Data for the Clock, Control and Data out are made selecting the “Write Only” radio button and “Start”. Data in is done using the “Read Only” button.

DDR3 runs at a clock frequency of 400MHz.

CAUTION

Be sure that the dipswitch is set up as indicated in the user guide and Reference manual.

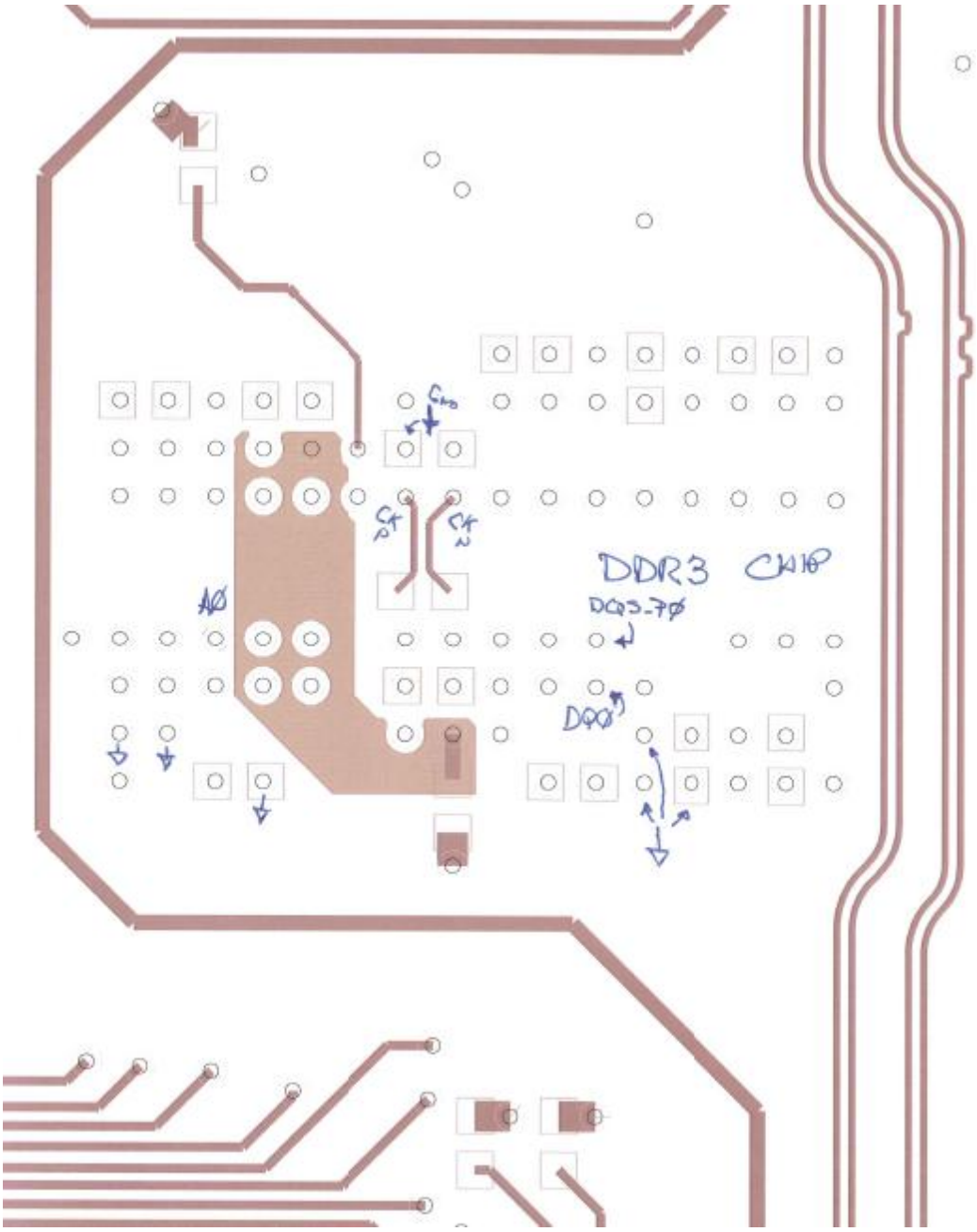


Simulations were done in HyperLynx on the finished artwork.

‘Scope shots were done on finished board.

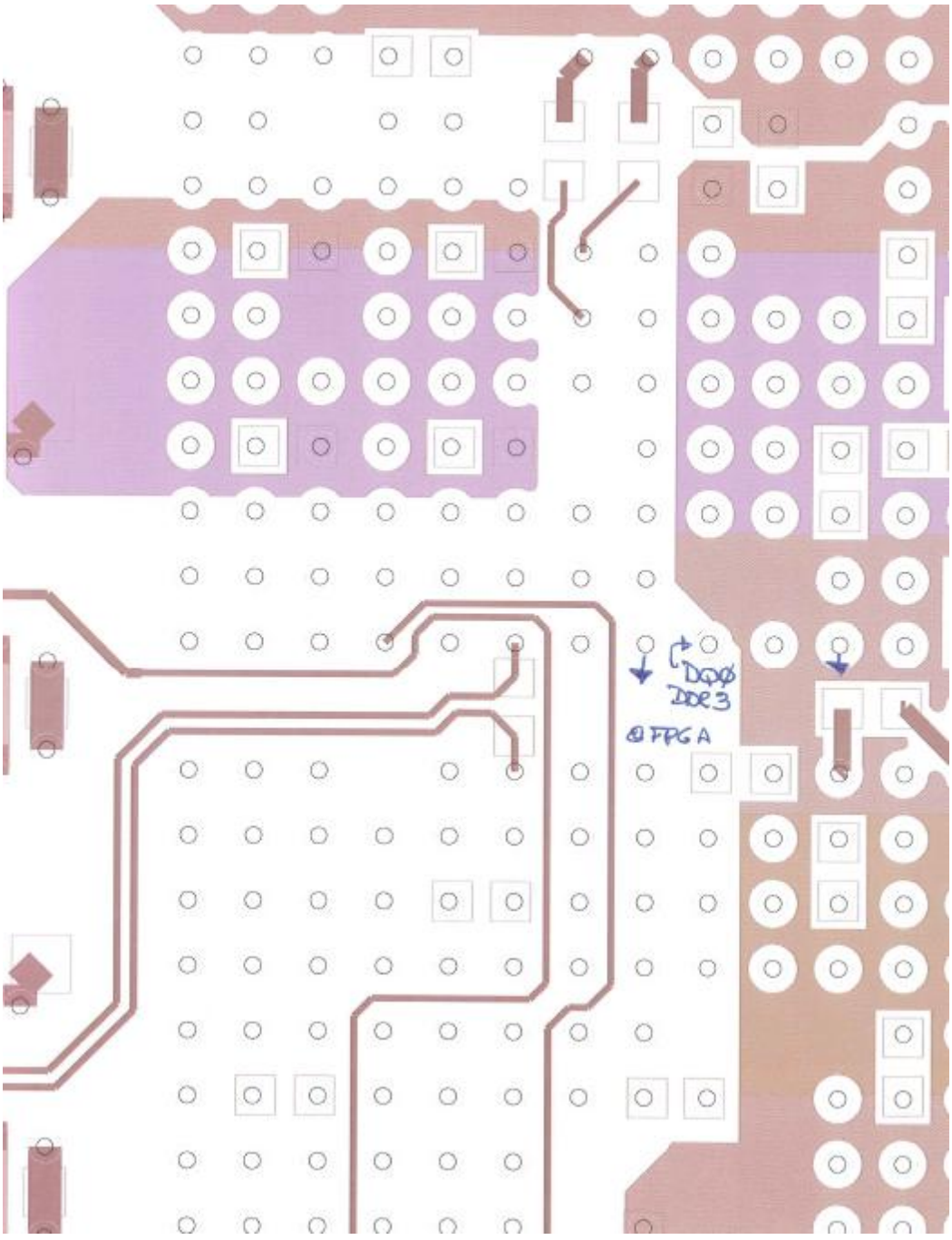
Probe Points for DDR3 Chip

The DDR3 chip was probed at the points indicated below, viewing from the bottom of the board.

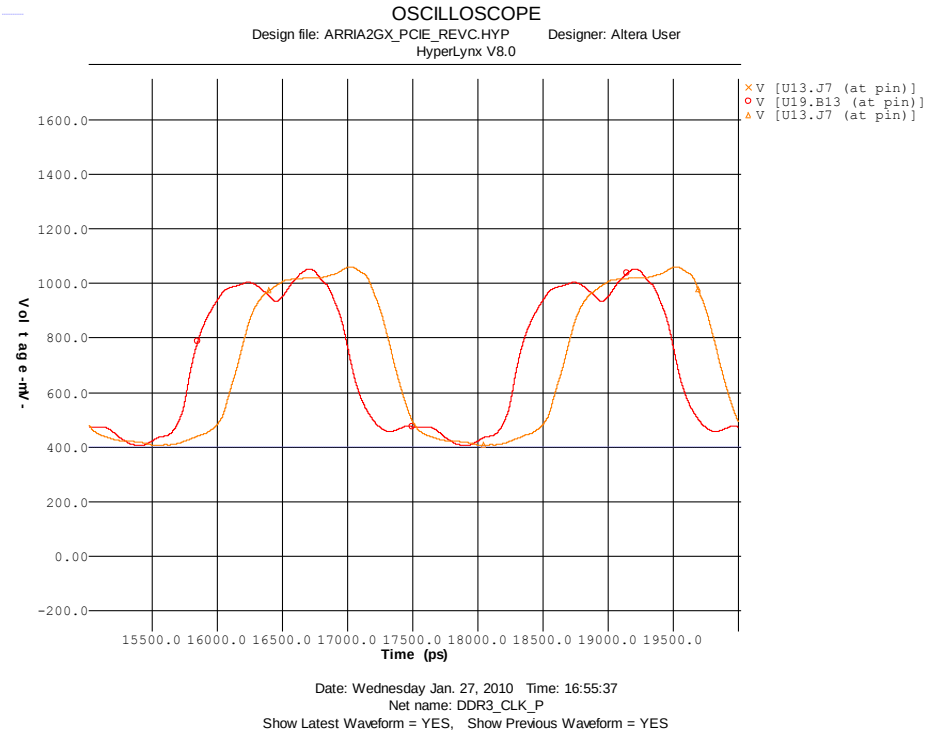


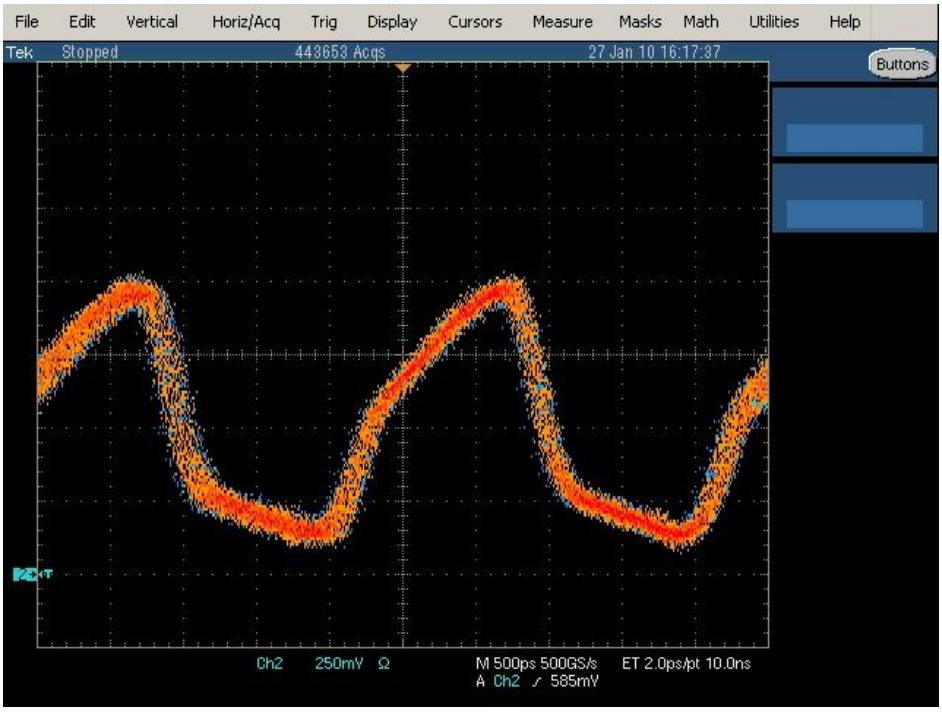
Probe points at the FPGA

Viewing the bottom of the board



DDR3_CLK

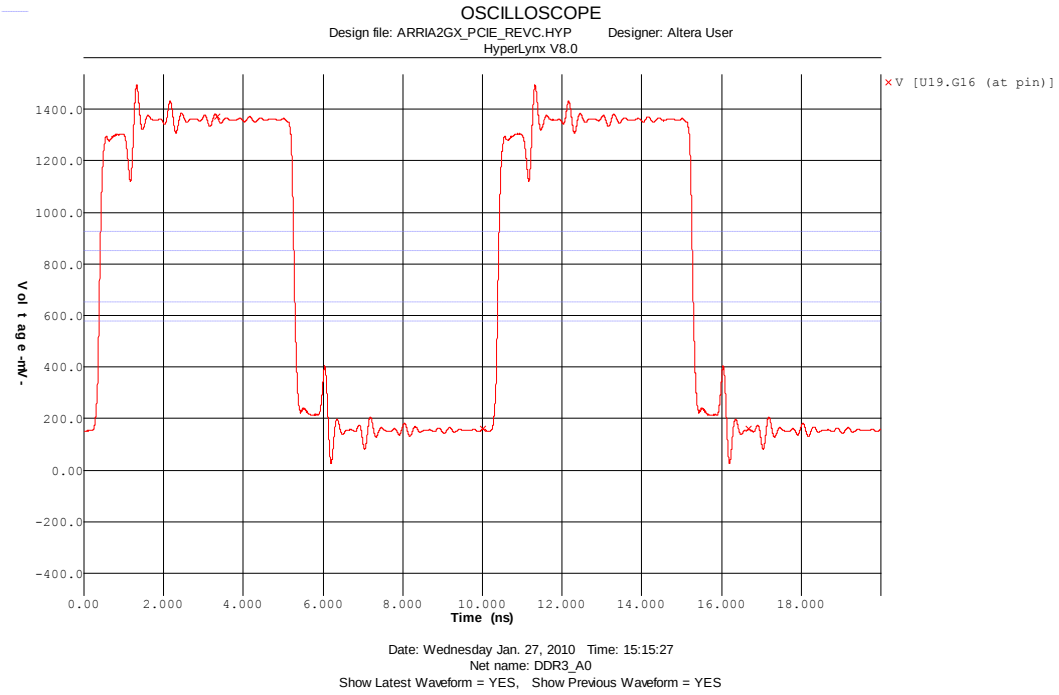


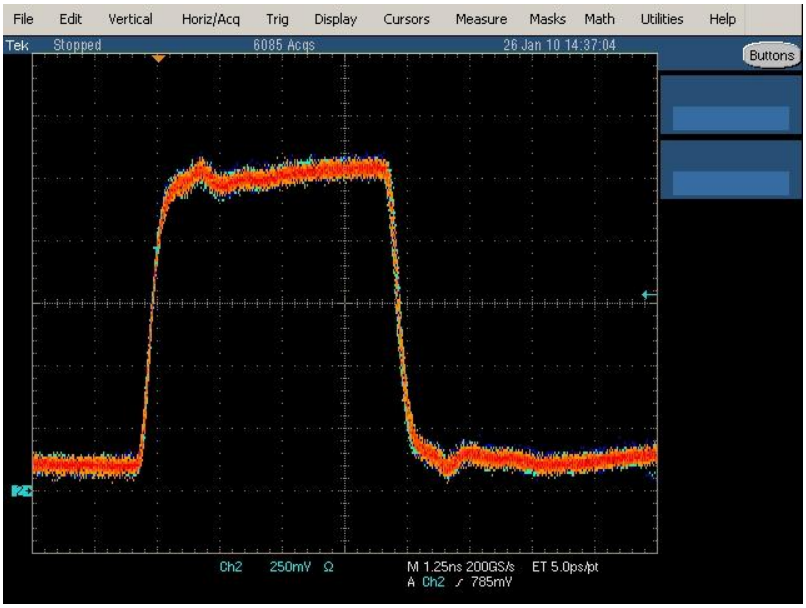


Compare to Orangge trace in Simulation for single ended measurement

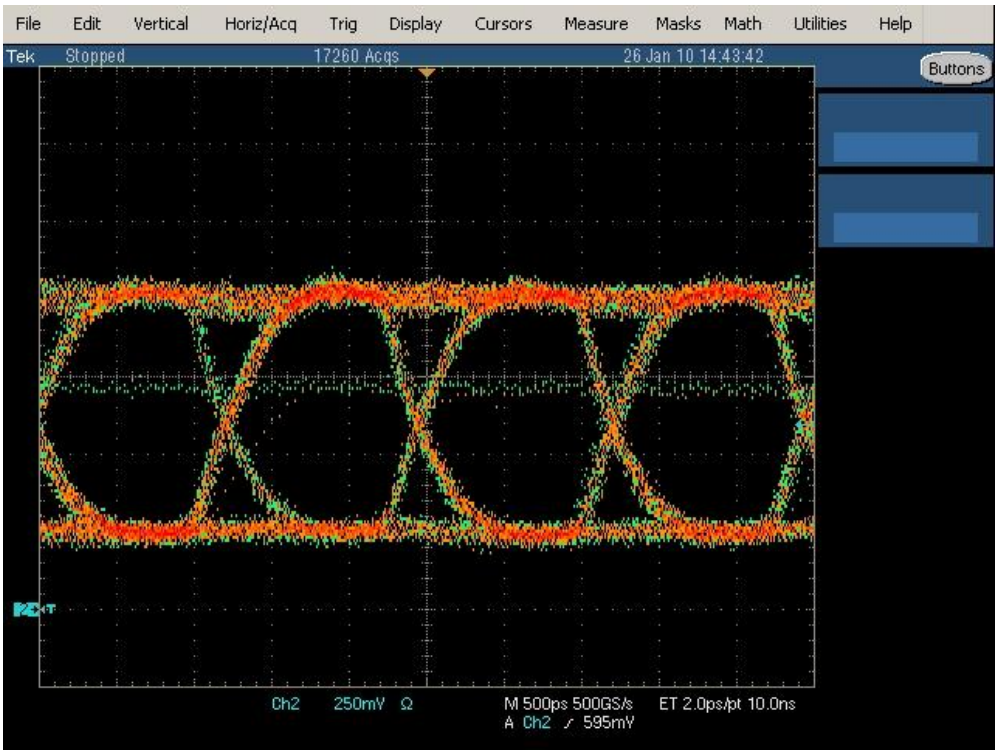
DDR3 chip interface A0 at DDR3

Simulation with sstl15c1_cio_d12s3

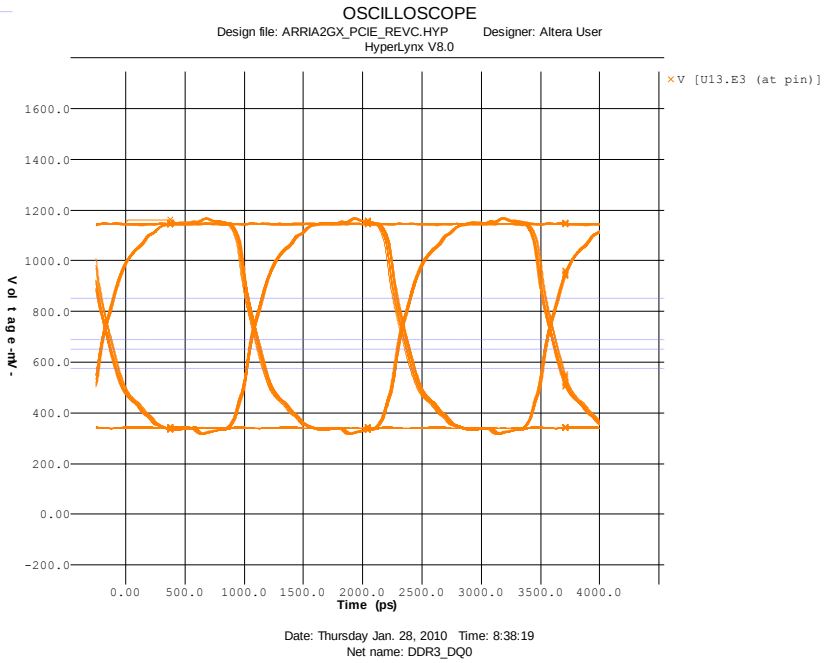




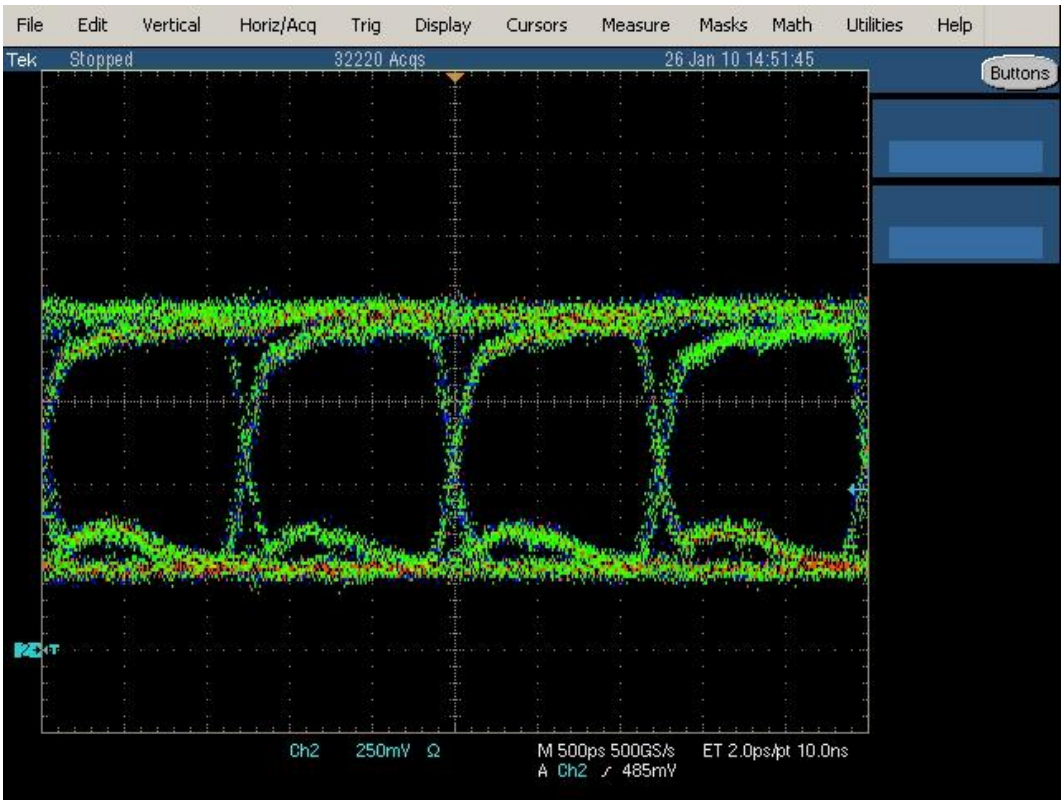
ddr3_400mhz_dq0_at_memory

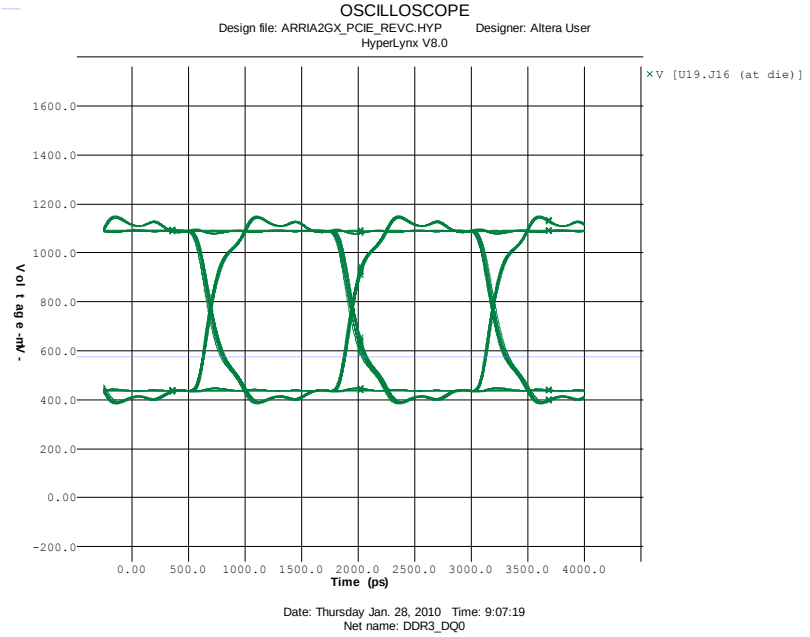


Simulation sstl15c1_cio_d12s3

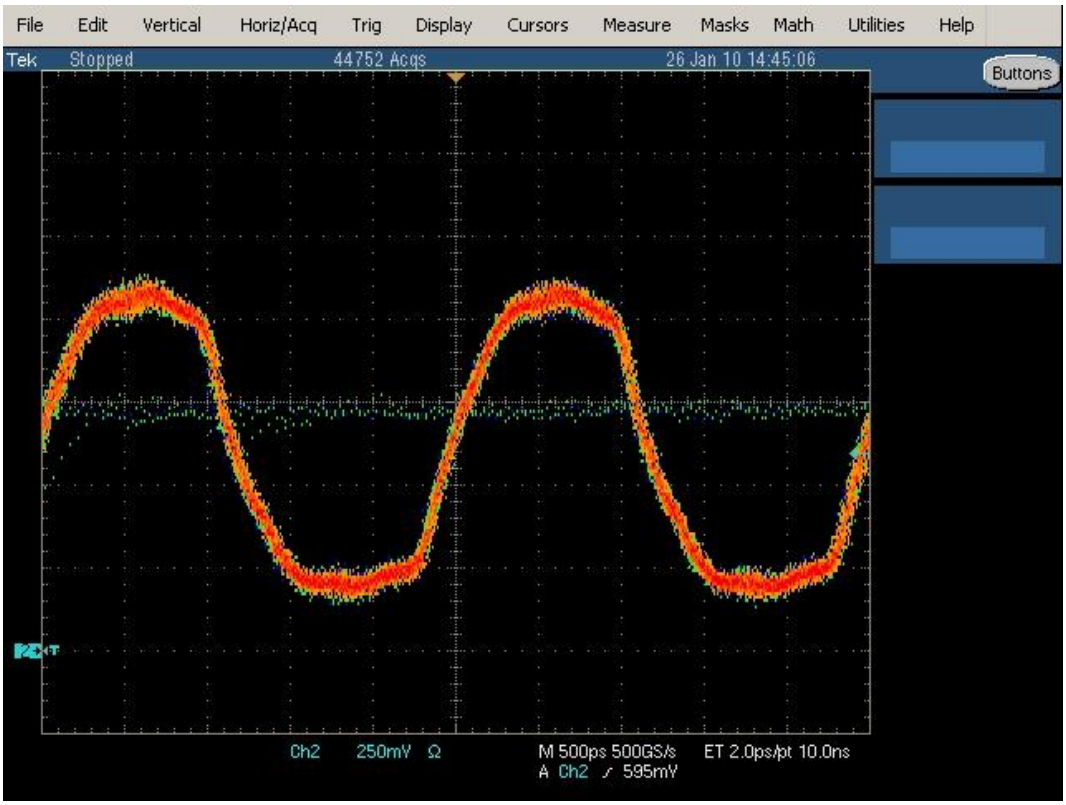


ddr3_400mhz_dq0_at_fpga

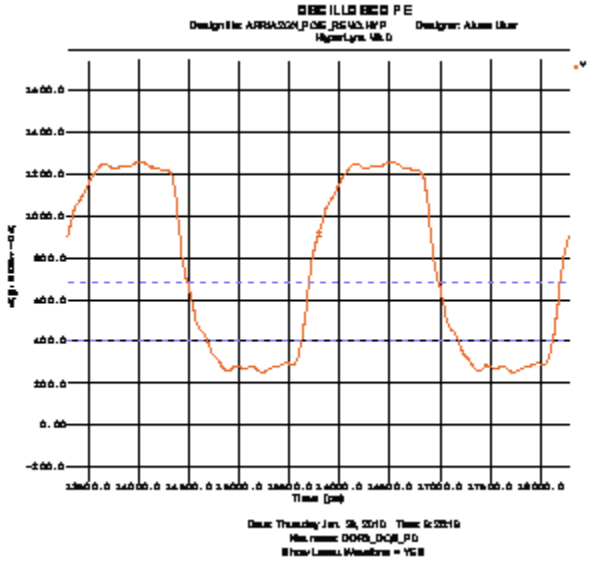




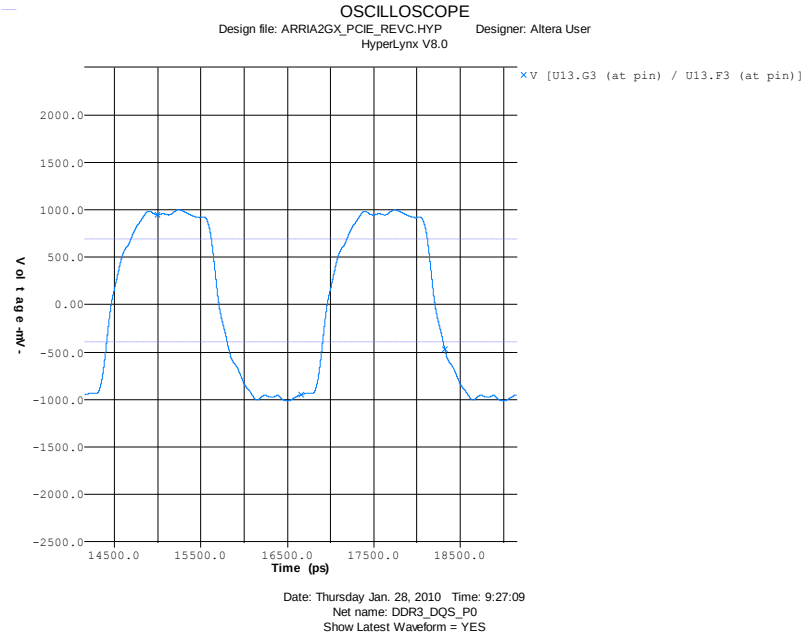
ddr3_400mhz_dqs0_p



Simulation Single Ended



Simulation Differential



Probing the board

It is often difficult to probe a board like this because of all the BGA parts. Any high density board will probably cause you the same problems. One easy way to find the right place to probe is to use a viewer that will allow you to look at the board artwork. For this board we have provided the layout in the Allegro .brd format. You can easily download a free viewer from:

http://www.cadence.com/products/pcb/Pages/Downloads.aspx

Select the Allegro/SIP Free Physical Viewer 16.2 (or later) and install it. You can then open the .brd file for the project. On the right hand side you will find the "Find" tab. You can enter a net name to select there and it will be highlighted.

Zoom in on the pin you want to look at. Then use the Visibility tab on the right to turn off all the layers except the bottom. You will then have a view of the bottom with the via you want to probe highlighted.

Set up the plot in the viewer under File > Plot Setup and select the Mirror Plot orientation. This will give you a print that is the same as looking at the bottom of the board. Next use File Plot to do the plot. It may take a couple of times through it to get something you can use. Make sure to mark where the grounds are around the via so you can find them easily.

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