Introduction

The BTS System is a demonstration of several tests that can be run from a Graphical User Interface. Included with this package is an external power monitor that can be used with an external USB Blaster to examine power usage of the FPGA running any given design. This document can be used for either the Arria-II GX PCIe Development Kit.

Requirements

- Full installation of either the
 - Quartus II 9.0 sp2 or Quartus Programmer 9.0 sp2
- For the BTS Demo
 - The Development Board, Power Supply and USB Cable all plugged together as they are at the end of going through the User Guide for the kit
- MAX-II should be ver8 or above

Installation:

- 1. Quartus II 9.0sp2 or Quartus Programmer 9.0sp2 is required. The latest Quartus II is available from Altera.com.
- 2. Locate BTS application where does not contain white space in its full path. For example, Desktop may contains white space, so please do not locate program at desktop.

Uninstalling:

- 1. Delete the installation files and folder
- 2. No registration change needed.

Setting up the board for the BTS System

The system should be set up as it was at the end of the processes outlined in the Kit User Guide as shown in figure 1-1



Figure 1-1-1

Dipswitch setting

User need to set JTAG chain to be able to see MAX-II device in it. In order to access MAX-II device, user need to set dipswitch on the back of the board.



Other dipswitches don't affect to this Power Monitor Tool.

Opening the BTS Graphical User Interface

To load the Graphical User Interface, browse to where the BTS section was installed and double click on BoardTestSystem.exe. You should see something similar to Figure 1-2.

🔊 Board Test System		
Configure Help About		
Ver 9.0.2	Config GPIO SRAMBFlash DDR8 DDR2 H5MC MAX II Registers PSO O Use PSR O Use PSS PSS: 0 OCR1: 100MHz SR5T	
	Board Information MAX-II rev: MAC:::	
Messages Connecting to the target java.lang.Exception: No BoardTestSyste m-compatible design exists in the FPGA . Please select a design from the conf igure menu.	Flash Memory Map Address Data 0x03FF.8000 - 03FF.FFFF top boot blocks unused 0x03FF.0000 - 03FF.7FFF top boot blocks unused 0x03FE.0000 - 03FE.FFFF top boot blocks unused 0x03FE.0000 - 03FE.7FFF top boot blocks unused 0x0282.0000 - 03FD.FFFF User Software 0x0202.0000 - 0281.FFFF Factory Software 0x0182.0000 - 0201.FFFF Zipfs	

Figure 1-2

With no FPGA design or without BTS design in FPGA, GUI will tell "Program could not find a system in FPGA. Please reconfigure" or "java.lang.Exception: Could not find configured device EP2AGX125" as you can see in the above figure 1-2.

Programming the FPGA with the BTS design

From the menu bar select "Configure" menu as shown in Figure 1-3

🔊 Board Test S	ystem		
Configure Help	About		
Configure with	SRAM/Flash/GPIO Design		
Configure with	DDR3 Design		
Configure with	DDR2 Design		624
Configure with	HSMC Design		PL
Exit		Ctrl+Q	
		Power M	onitor

Figure 1-3

Select project to configure.

The following window will pop-up as in Figure 1-4.



Figure 1-4

Click on the "Configure" button to start downloading. It will take about 60sec to download and configure the FPGA.





First, downloader will convert sof file to bitstream, then download the bitstream data to FPGA. Once the download started, the progress bar will show the current status. After finishing download, the button says Connecting.. and change to Close. Now all configuration process is done. Close the pop-up window.

sof downloader 🔀	sof downloader
Program is connecting to the target board now	Process Finished
Connecting,, Stop	Close Stop

Figure 1-6

The GUI program and board are synchronized and ready to use.

You should be able to see the information window displaying Detected "Projec name" similar to Figure 1-7 as well as JTAG Chain list in right window. In this picture, GPIO, SRAM, Flash project has detected in the FPGA.



Figure 1-7

The Config Tab

MAX-II Registers

MAX II Registers PSO C Use PSR C Use PSS	PSR: 0
OCR1: 125MHz	SRST

User can see the current registers and can control it from GUI. User can set SRST, PSR. PSO.

SRST : W only Software Reset 0: reconfigure request

	-		
PSR	: R/W	Page Select Register	0-7 pages to load from Flash

- PSO : R/W Page Select Override 0: register setting 1: rotary switch setting
- PSS : R only Page Select Switch 0 15 this is the value from rotary switch

When the RST bit is set to 0, alert will be pop up.

Re-confi	gure notice!!!		×
?	Do you really want it might disconnect	to change FPGA this program fro	program? Im the board
	Yes	No	

This is because if you change the program, you will loose the connection to the board. This GUI only can go with specific FPGA program.

Jtag Chain



All the device in a JTAG Chain will be displayed in here.

The Stratix-IV device is always on the top. By changing JTAG dipswitch, SW4, EPM2210 can be disappeared.

Board Information

MAX-II rev:6

rev:6 MAC de:ad:ca:fe:be:ef

MAX-II rev : this is a version information of MAX-II device.

MAC : this is the MAC address assigned to this board. The information is in Flash device.

Flash	Memory	Map

Flash memory map		
Address	Data	
0x03FF.FFFF - 03FF.800	0 top boot blocks unused	
0x03FF.7FFF - 03FF.000	0 top boot blocks unused	
0x03FE.FFFF - 03FE.800	0 top boot blocks unused	
0x03FD.7FFF - 03FD.000	10 top boot blocks unused	
0x0282.0000 - 03FC.FFF	F User Software	•

This map is currently hard coded. It may be read from Flash

The GPIO Tab



Read and Write function for the 16x2 character LCD display.

User can change it from GUI and reflect it to LCD display.

If something is already there, user can read it from LCD display and show it in GUI.

Message X		×
i) a	Can not exceed 16 charactors	
	OK	1

User can enter up to 16 characters for each line. If it exceed, you'll alert.

Dipswitch Read Value

User Dipswitch 1 (OFF) 1 2 3 4 0 (ON) 1 1 1 1 1 1 1

GUI reads User Dipswitch data constantly.

User LED



Displays current user LED status. Also, user can control LED by pressing button. Yellow is turning on, light gray is turning off.

Push buttons



Displays user push button status.

If button is pushed, the GUI button will be dent.

The SRAM&FLASH Tab

<u>SRAM</u>

Config GPIO	SRAM&Flash	DDR3 DD	R2 H5MC	
SRAM				
Start Address	Range:	: 0×000.0000) - 0×01F.FFF	F
0×00001200	Read	Write		
Address	0-3	4 - 7	8-B	C-F
0x0001200	0218a2c0	2a82ba23	b70ea2f4	a0d808e7
0x0001210	c6e8e880	b125289e	850623e6	7090664d
0x0001220	Oflcl0c5	Oc3fa4c8	caf7e050	9b5c4f6f
0x0001230	la6880d4	2718d965	92585e4e	91c638be
0x0001240	a72c0741	220da6fl	219893cl	75bbb921
0x0001250	060098Ъ2	81998ccf	756c345f	lebf5e3a
0x0001260	328580c9	1433ffda	1b534b32	63226Ъ74
0x0001270	b2802f00	6c260f21	5d7c8b39	23692623

User can read and write to SRAM.

Also, user can specify the start address to read/write.

User can change table. When the modification finishes, hit Write button to write data into SRAM.

The address range is currently 0x00000000 to 0x001FFF80

SRAM		· ·		
Start Address	Range:	0×000.0000) - 0×01F.FFF	F
0x04001200	Read	Write		
Address	0-3	4 - 7	8-B	C - F
0x0001200	0218a2c0	2a82ba23	b70ea2f4	a0d808
0x 0x 0x 0x 0x 0x 0x 0x 0x 0x	SSRAM add 0x0000000	ress range is D - 0x001FFF OK	80	× 66 4 f 38 b9 5e 6b 26

If the address is out of range, alert will pop up.

Flash

Start Address Range: 0x000.0000 - 0x3FF.FFFF						
0x0004c000	Read	Write				
Address	0-3	4 - 7	8-B	C-F		
0x004c000	40000000	00004000	04000440	00040000		
0x004c010	00000000	80000000	00008000	08000880		
0x004c020	00080000	00000000	00000000	00000000		
0x004c030	10001000	01100000	00000100	00000001		
0x004c040	00000000	20002000	02200000	00000200		
0x004c050	00000002	00000000	40004000	04400000		
0x004c060	00000400	00000004	00000000	80008000		
0x004c070	08800000	00000800	00000008	00000000		

User can read Flash data.

Currently write function is not yet implemented. The Flash address range is 0x000000 - 0x3FFF80



If the specified address is out of range, alert will pop up.

Also, flash writable address range is from 0x03FE0000 to 0x03FFFF80

riasii							
Start Address	Rang	Range: 0x000.0000 - 0x3FF.FFFF					
0×4004c000	Read	Write					
Address	0-3	4 - 7	8 - B	C			
0004000	4000000	00004000	04000440	6004			
Message			>	1 800			
Please assign address range of 0x03FE0000 - 0x03ffff80							
	L			00C			
		<u>K</u>		000			

The DDR2 Tab



Start button will start test process. Tx, Rx or both progress bar will go up and show the percentage to maximum possible performance.

Tx counter and Rx counter or both should display the Mega-Transaction per second that the current transaction performance.

Stop button will stop test process.

Error Section

Insert Error button will insert 1 word error at a time. User can check how many errors has inserted by user by checking Inserted error counter. The Detected error counter is actually detected errors at hardware.

Clear button will clear both Detected error and inserted error counters.

Data Size slider will enable user to select size of data to transmit at a time. User can select from size of 2 to 524288.

Data Type Section User can select data type from

- PRBS
- Memory
- Math

The HSMC Tab



Status Section

- PLL Lock Status
- Channel Lock Status
- Pattern Sync Status

Port Section

- 0. HSMA x4 Transceivers [0..3]
- 1. HSMA x17 LVDS SERDES
- 2. HSMA x3 Single Ended Loopback

Data Type Section

PRBS
Memory
Math

Error Control Section

Insert Error button will insert 1 word error at a time. User can check how many errors has inserted by user by checking Inserted error counter. The Detected error counter is actually detected errors at hardware.

LoopBack Section

Start button will start test process. Tx, Rx or both progress bar will go up and show the percentage to maximum possible performance.

Tx counter and Rx counter or both should display the Mega-Transaction per second that the current transaction performance.

Stop button will stop test process.

The DDR3 Tab



Performance Section

Start button will start test process. Tx, Rx or both progress bar will go up and show the percentage to maximum possible performance.

Tx counter and Rx counter or both should display the Mega-Transaction per second that the current transaction performance.

Stop button will stop test process.

Error Control Section

Insert Error button will insert 1 word error at a time. User can check how many errors has inserted by user by checking Inserted error counter. The Detected error counter is actually detected errors at hardware.

Data Size slider It will enable user to select size of data to transmit at a time. User can select from size of 2 to 524288. Data Type Section

- PRBS
- Memory
- Math

R/W Control

- Write after Read
- Read only
- Write only

The External Tool



User can start Stand alone Power Tool from this GUI.



The Connection error

When user change FPGA program or hit CPU_Reset button, the connection between GUI and the target board will be lost.

In this case, following alert will be pop up.

Power Monitor	OCR1: 125MHz	P55: 0
Connection Failure(Please check conne	Connection Failure(read data) Please check connections and restart program!! OK	
	MAX-II rev:8	MAC ff:ff:f
	Flash Memory Map	
	Address	Data
he GPIO, SRAM, Flash Project 🛋	0x03FF.8000 - 03FF.FFFF	top boot blocks u
. Failure(read data)	0x03FF.0000 - 03FF.7FFF	top boot blocks u

User need to closer or restart GUI.

Known Issues:

When you hit CPU RESET button, or Config button, program will stack and will no response.

If this happens you will not be able to close window at all.

In this case, open task manager, go to process tab. Find "javaw" process, and terminate it.