


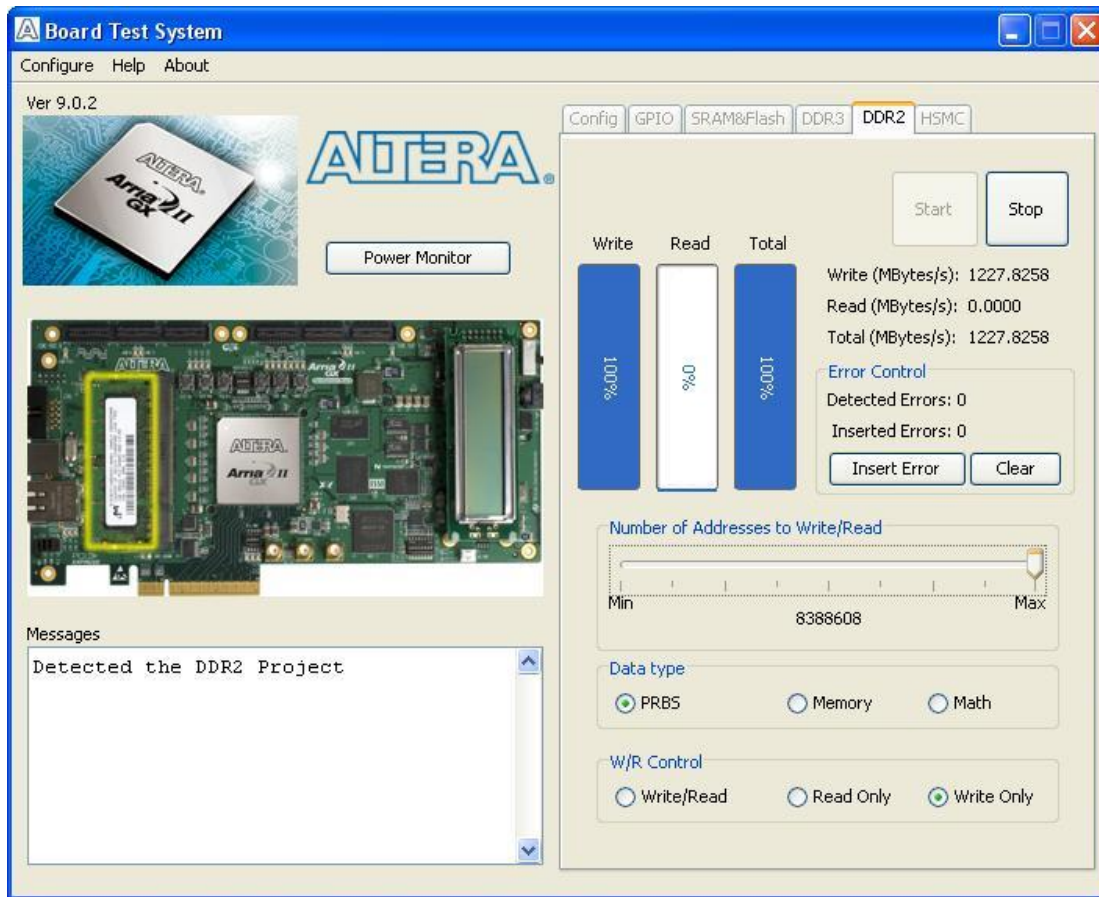
DDR2 SODIMM Interface

Measurements were made on the DDR2 SODIMM interface using the Board Test System user interface.

The Address, Control and Data Out measurements were made by setting the slider labeled “Number of Addresses to Read / Write” to the maximum. Data for the Clock, Control and Data out are made selecting the “Write Only” radio button and “Start”.

Data in to the FPGA is gathered using the “Read Only” button.

 Be sure that the dip switches are set up as indicated in the user guide and Reference manual.



Simulations were done in HyperLynx on the finished artwork using IBIS models for the ArriaII GX. These models are available on the Altera web site or generated from QuartusII after the design is finished.

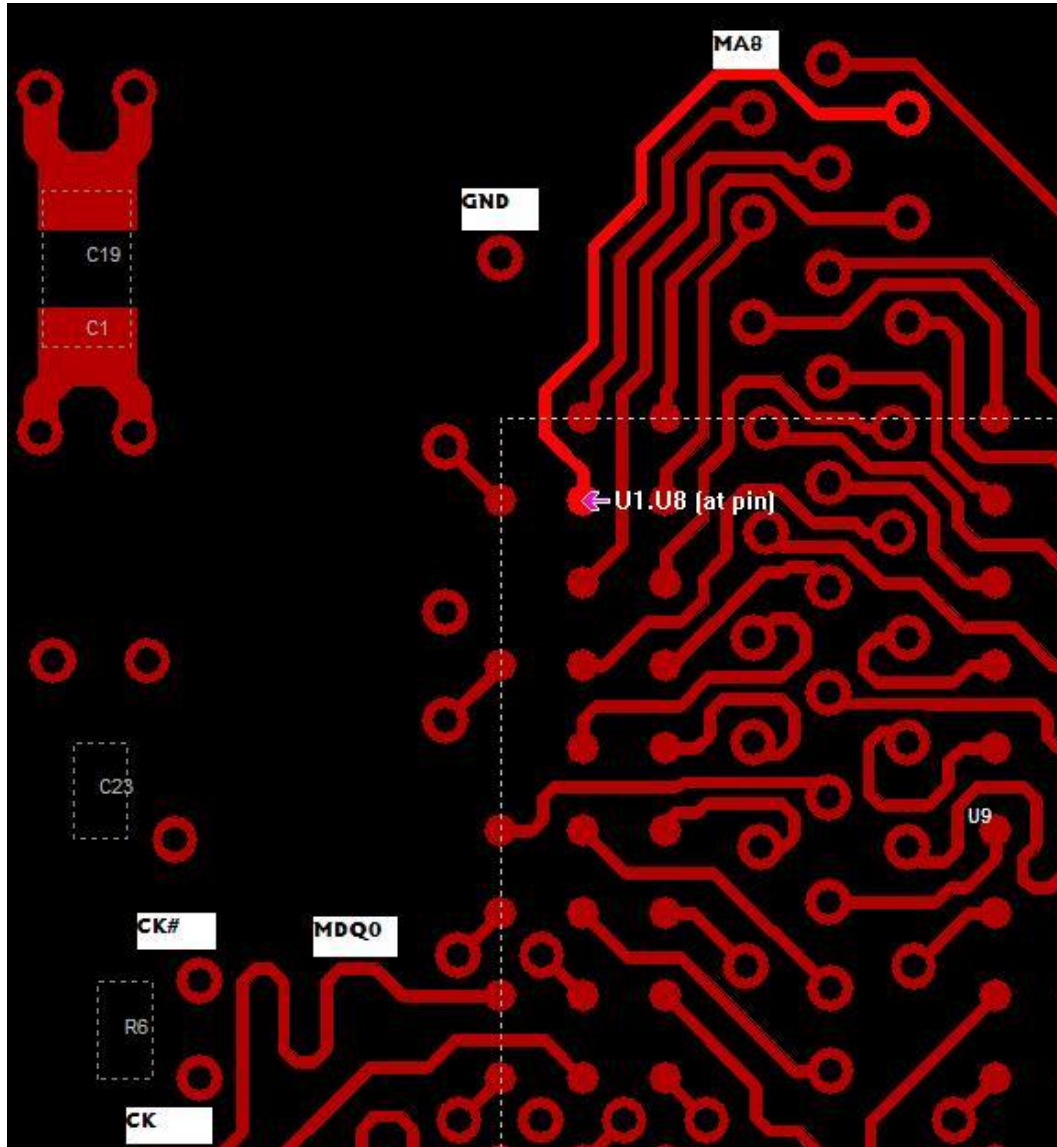
The drive strengths listed for the interface match the IBIS model naming convention. These are easily translated into settings in the design pin planner window.

Oscilloscope shots were done on finished board.

Many of the differential signals were also analyzed single ended for the benefit of users who do not have access to a differential probe.

Probe Points for SODIMM board

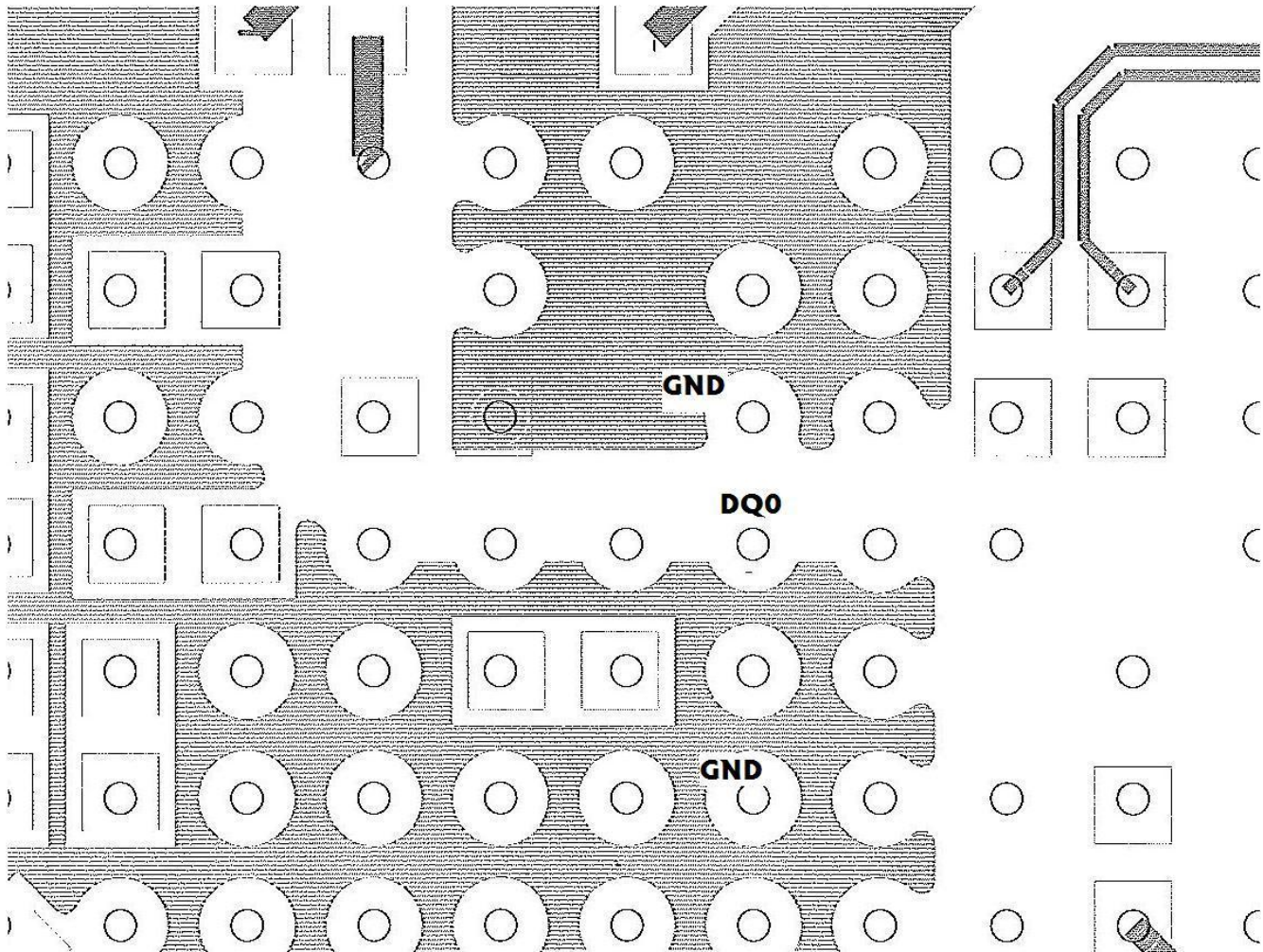
The SODIMM was probed at the points indicated below. The technique for creating this kind of map are explained at the end of this document



The signals we will examine are A8, DQ0 (during write) and CK0. The points of measurement were chosen to be convenient to probe. The signal will look different on the chip. It would be nice to probe the actual device but that is not possible. Probing correctly will require scraping some soldermask off of the MDQ0 trace. Also scraping some soldermask off of the ground plane near the places you want to probe may be needed to keep the ground connection as short as possible for signal integrity.

Probe points at the FPGA

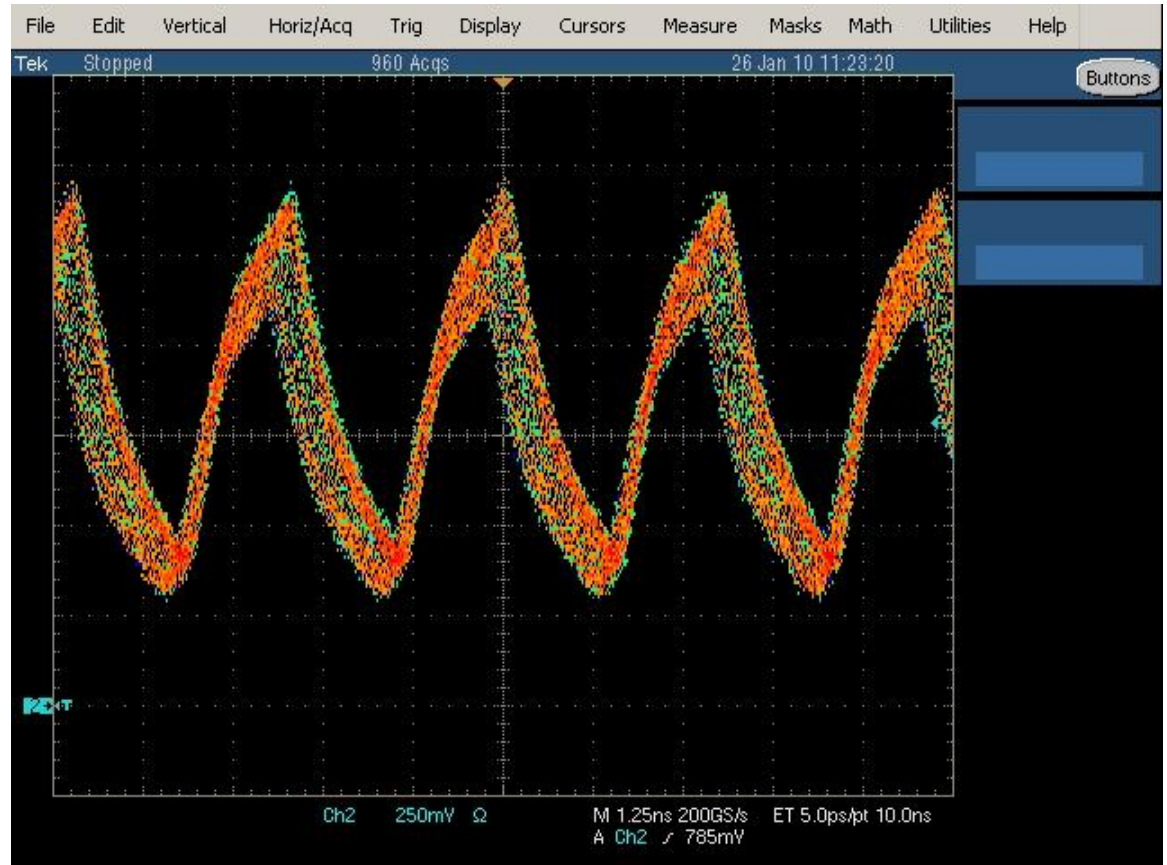
Viewing the bottom of the board



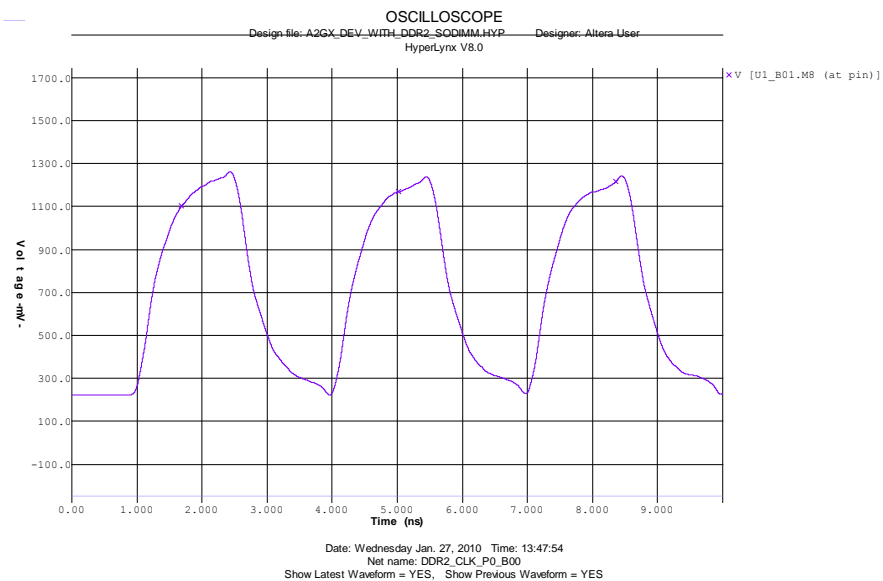
On this map we show where we probed signal DQ0 on the FPGA during read operation. This on the far side via. The signal will look different on the chip.

DDR2_CLK

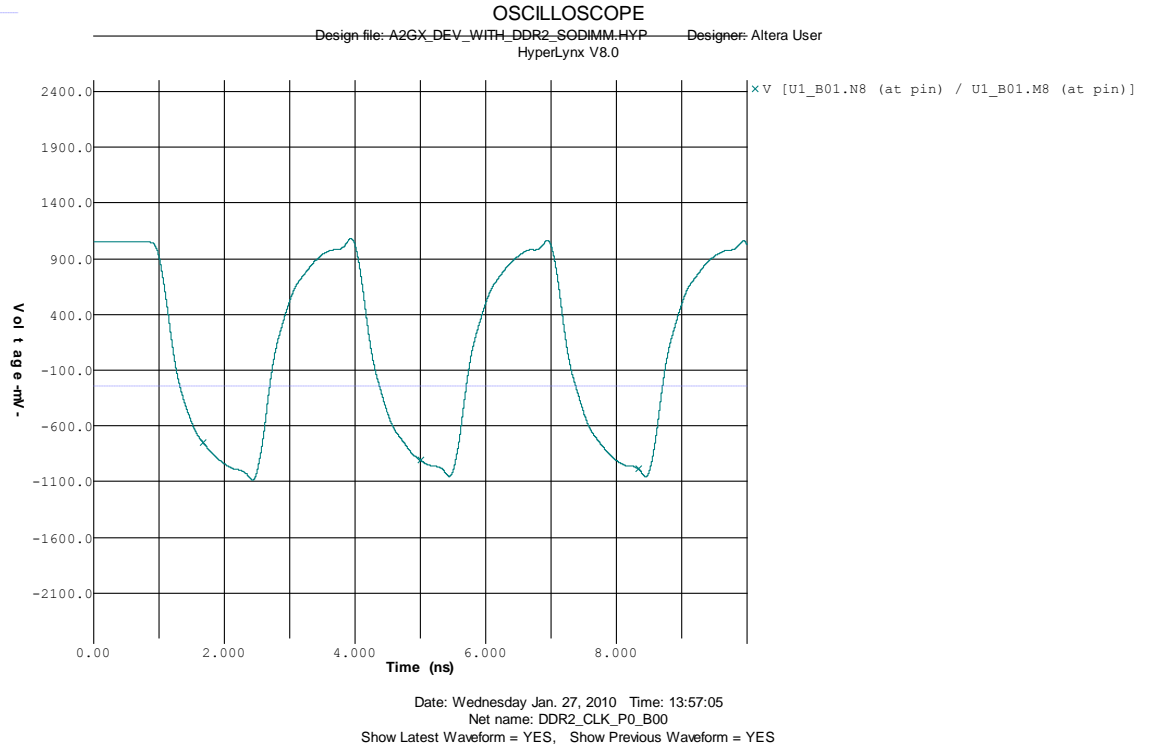
The DDR SODIMM system is clocked at 333MHz.



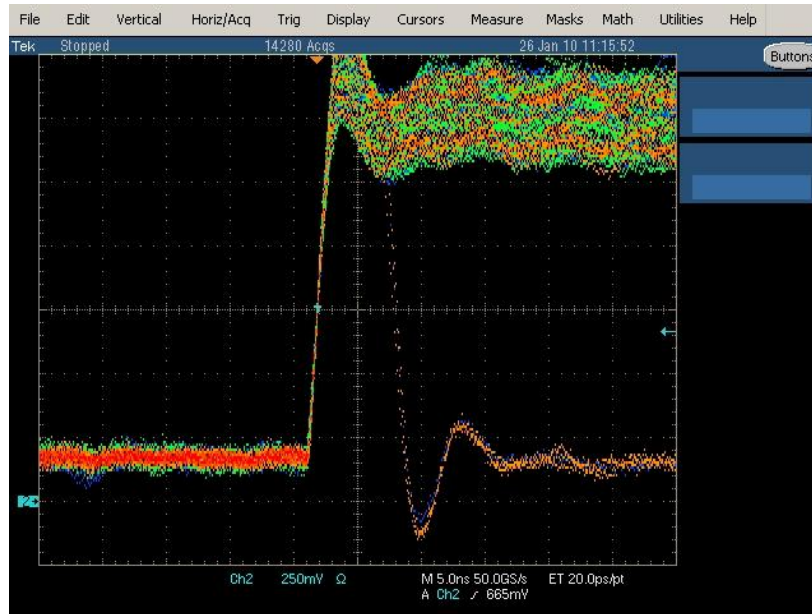
Compare to trace in Simulation for single ended measurement



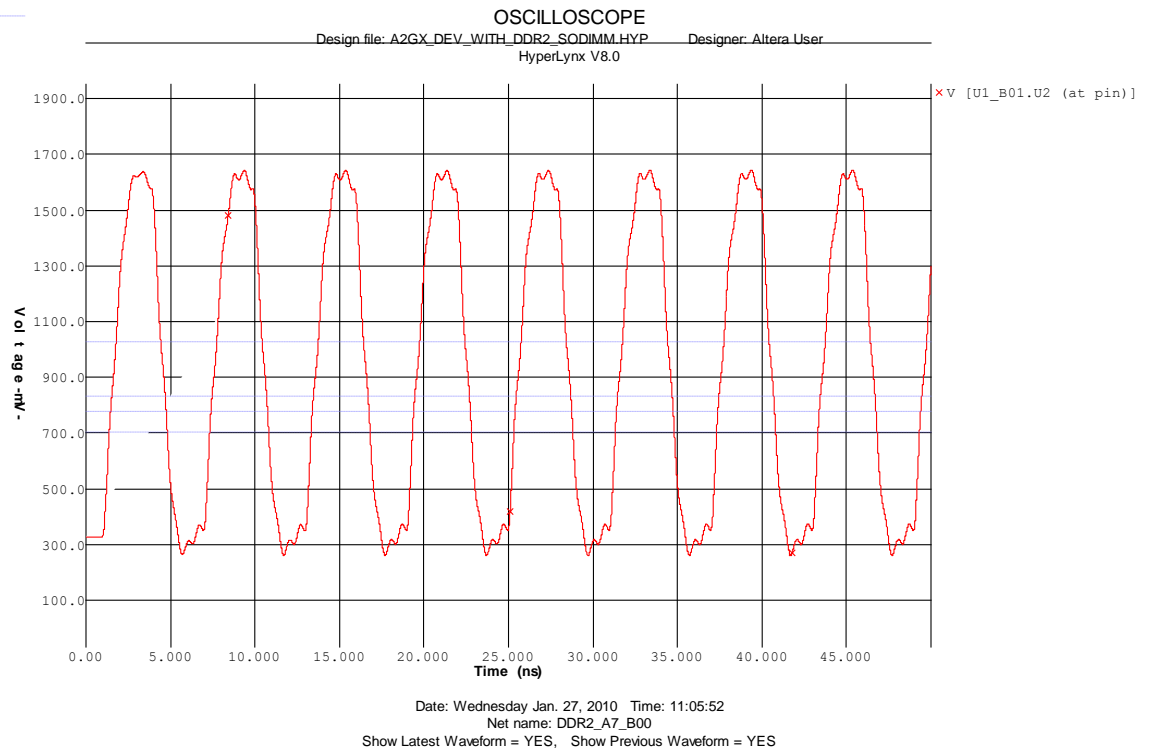
Differential Simulation



DDR2_A7 at via on SODIMM

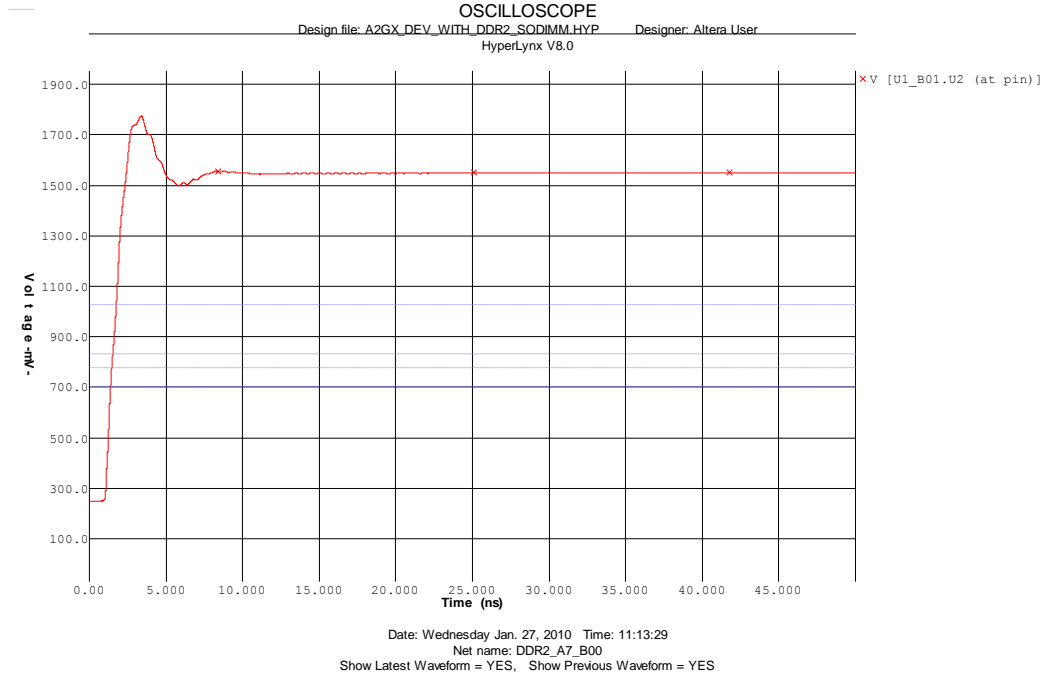


167MHz sstl18c1_cio_d8s3

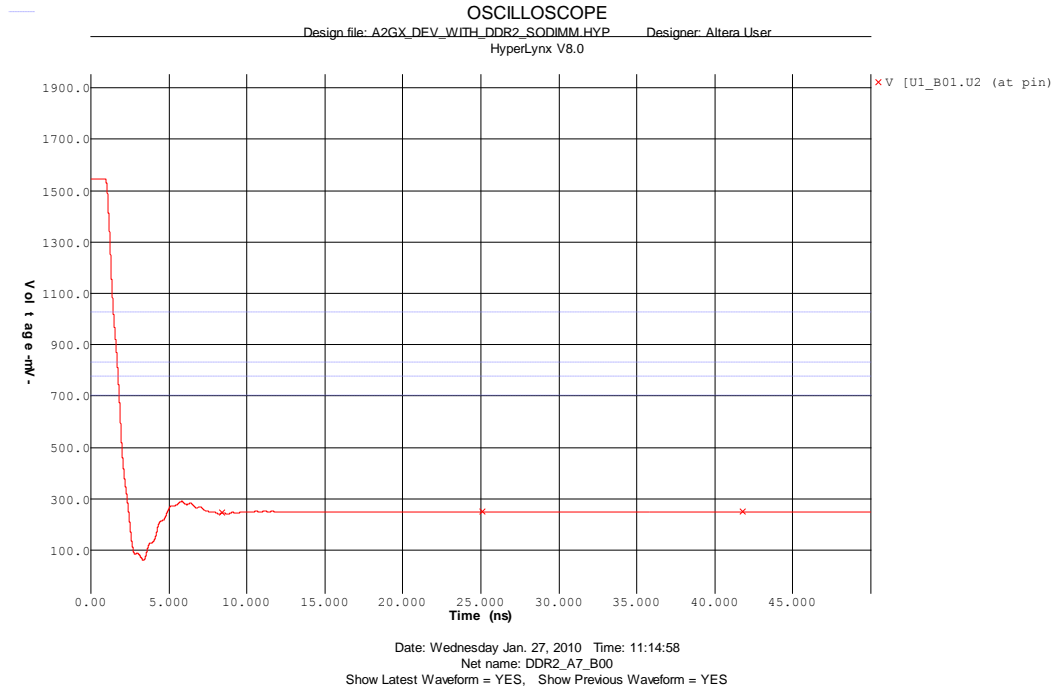


Here we are providing transient waveforms to show how the overshoot looks.

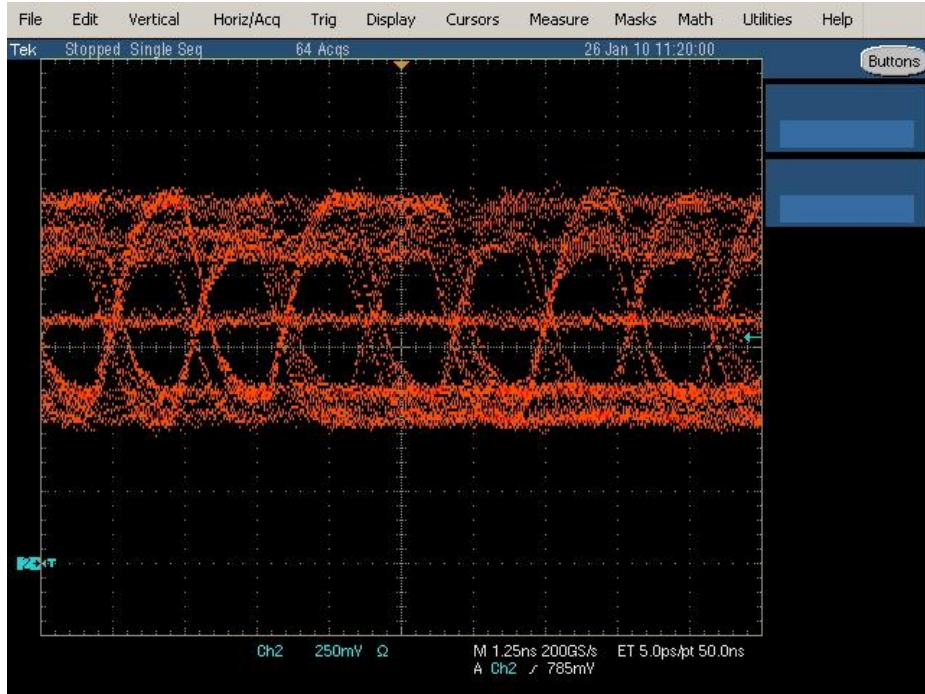
DDR2 A7 167MHz sst18c1_cio_d10s3 Rising



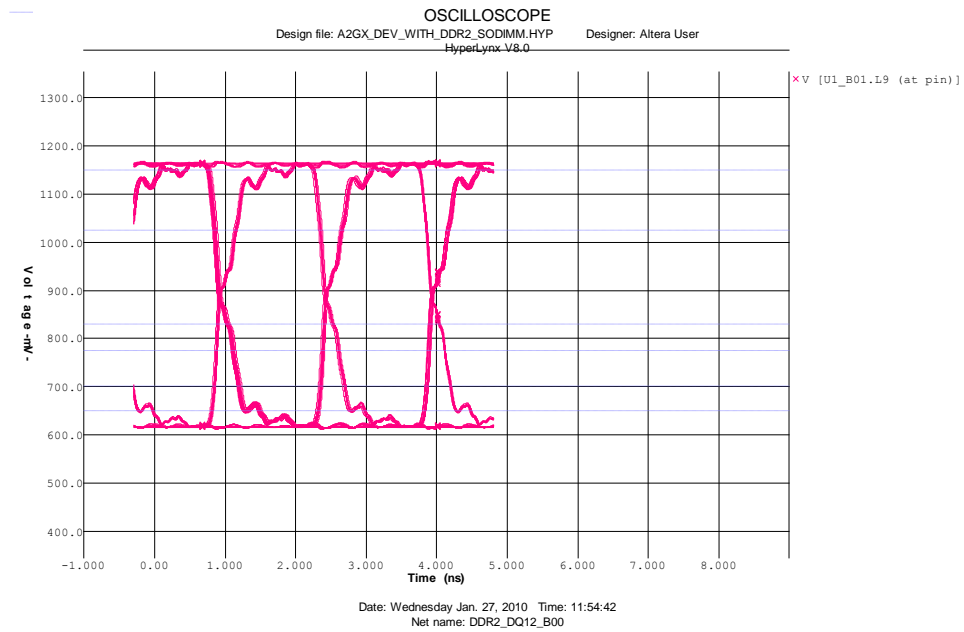
DDR2 A7 167MHz sst18c1_cio_d10s3 falling



DDR2_DQ12 at via on SODIMM

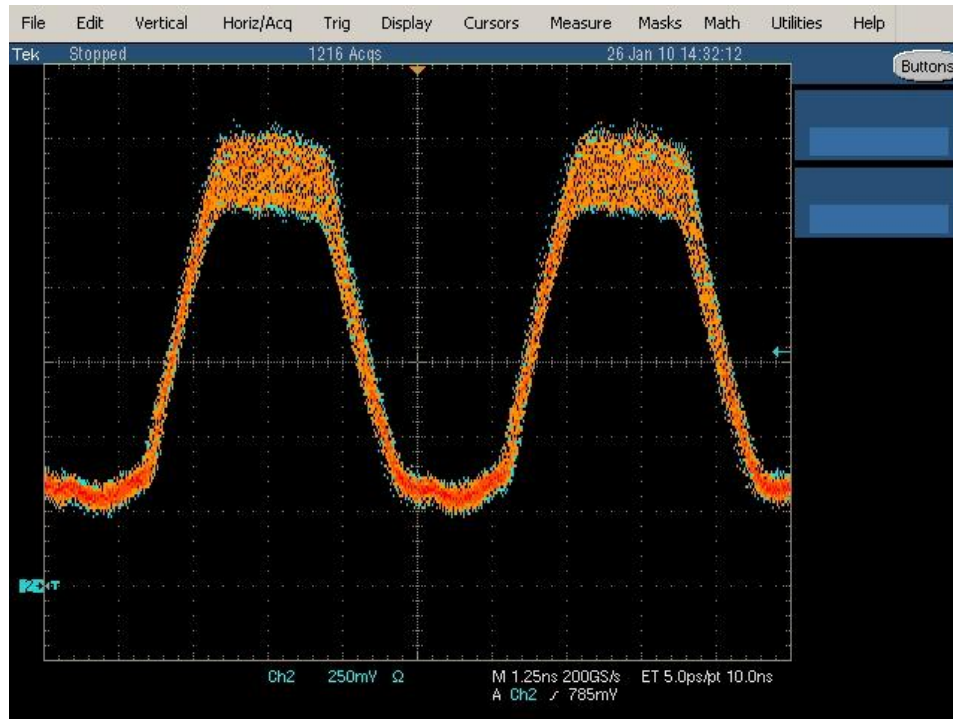


Sst18c1_c1_d12s3

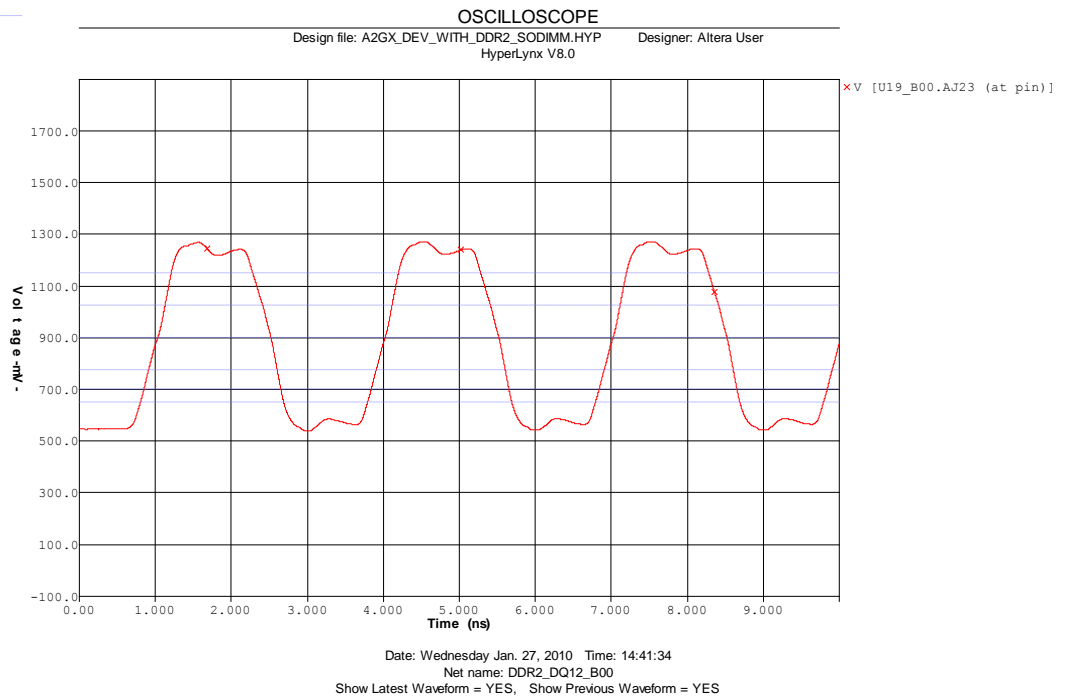


Good

DDR2_DQ12 at via below FPGA



Simulation



Probing the board

It is often difficult to probe a board like this because of all the BGA parts. Any high density board will probably cause you the same problems. One easy way to find the right place to probe is to use a viewer that will allow you to look at the board artwork. For this board we have provided the layout in the Allegro .brd format. You can easily download a free viewer from:

<http://www.cadence.com/products/pcb/Pages/Downloads.aspx>

Select the Allegro/SIP Free Physical Viewer 16.2 (or later) and install it. You can then open the .brd file for the project. On the right hand side you will find the “Find” tab. You can enter a net name to select there and it will be highlighted.

Zoom in on the pin you want to look at. Then use the Visibility tab on the right to turn off all the layers except the bottom. You will then have a view of the bottom with the via you want to probe highlighted.

Set up the plot in the viewer under File > Plot Setup and select the Mirror Plot orientation. This will give you a print that is the same as looking at the bottom of the board. Next use File Plot to do the plot. It may take a couple of times through it to get something you can use. Make sure to mark where the grounds are around the via so you can find them easily.



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