

2011

Arria II GX FPGA Development Board DDR3 Interface

Help Document

DDR3 Chip Interface

Measurements were made on the DDR3 chip interface by setting the slider labeled "Number of Addresses to Read / Write" to the maximum. Data for the Clock, Control and Data out are made selecting the "Write Only" radio button and "Start". Data in is done using the "Read Only" button.

DDR3 runs at a clock frequency of 400MHz.



Be sure that the dipswitch is set up as indicated in the user guide and Reference manual.

🔊 Board Test System				
Configure Help About				
Ver 9.0.2	Config GF	PIO SRAI	M&Flash	DDR3 DDR2 HSMC
Power Monitor	Write	Read	Total	
	100%	of Addres	100%	Write (MBytes/s): 1485.8888 Read (MBytes/s): 0.0000 Total (MBytes/s): 1485.8888 Error Control Detected Errors: 0 Inserted Errors: 0 Insert Error Clear
Messages	1	a 12	0	1 1 1 Y
Detected the DDR3 Project	Min		83	88608 Max
	Data Type ● PRBS			
	W/R Control Write/Read Read Only Write Only			

Simulations were done in HyperLynx on the finished artwork.

'Scope shots were done on finished board.

Probe Points for DDR3 Chip



The DDR3 chip was probed at the points indicated below, viewing from the bottom of the board.

Probe points at the FPGA

Viewing the bottom of the board



DDR3_CLK



Compare to Orangge trace in Simulation for single ended measurement

DDR3 chip interface A0 at DDR3

Simulation with sstl15c1_cio_d12s3







ddr3_400mhz_dq0_at_memory

Simulation sstl15c1_cio_d12s3



ddr3_400mhz_dq0_at_fpga





ddr3_400mhz_dqs0_p



Simulation Single Ended



Simulation Differential



Probing the board

It is often difficult to probe a board like this because of all the BGA parts. Any high density board will probably cause you the same problems. One easy way to find the right place to probe is to use a viewer that will allow you to look at the board artwork. For this board we have provided the layout in the Allegro .brd format. You can easily download a free viewer from:

http://www.cadence.com/products/pcb/Pages/Downloads.aspx

Select the Allegro/SIP Free Physical Viewer 16.2 (or later) and install it. You can then open the .brd file for the project. On the right hand side you will find the "Find" tab. You can enter a net name to select there and it will be highlighted.

Zoom in on the pin you want to look at. Then use the Visibility tab on the right to turn off all the layers except the bottom. You will then have a view of the bottom with the via you want to probe highlighted.

Set up the plot in the viewer under File > Plot Setup and select the Mirror Plot orientation. This will give you a print that is the same as looking at the bottom of the board. Next use File Plot to do the plot. It may take a couple of times through it to get something you can use. Make sure to mark where the grounds are around the via so you can find them easily.

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