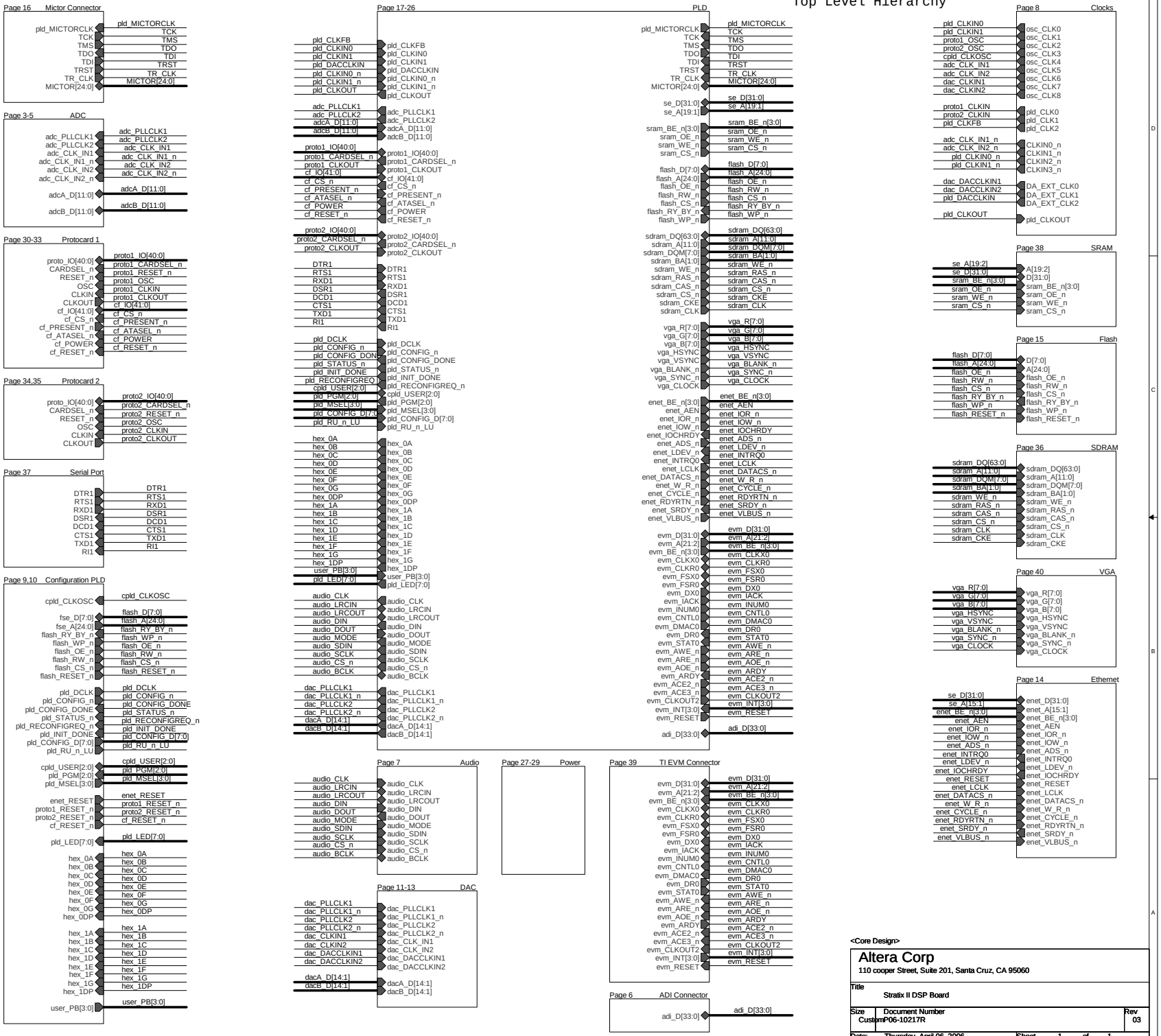
Top Level Hierarchy



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Title: Stratix II DSP Board		
Size: Custom	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

DSP Development Board

Stratix II RoHS Edition

Rev 03

Revision History

Date	Change Description	Rev
10/21/03	Started design	01
2/5/04	Sent out schematic for first design review	01
7/30/04	Started Rev02 changed per document Maine_board_bringup.doc	02
7/30/05	Rev03 is the RoHS version of the board. the only other changes is the clock circutriy got several more bypass caps and the VREF signals where pulled high in accorcance with stuffing the 2S180 chip on the board	03

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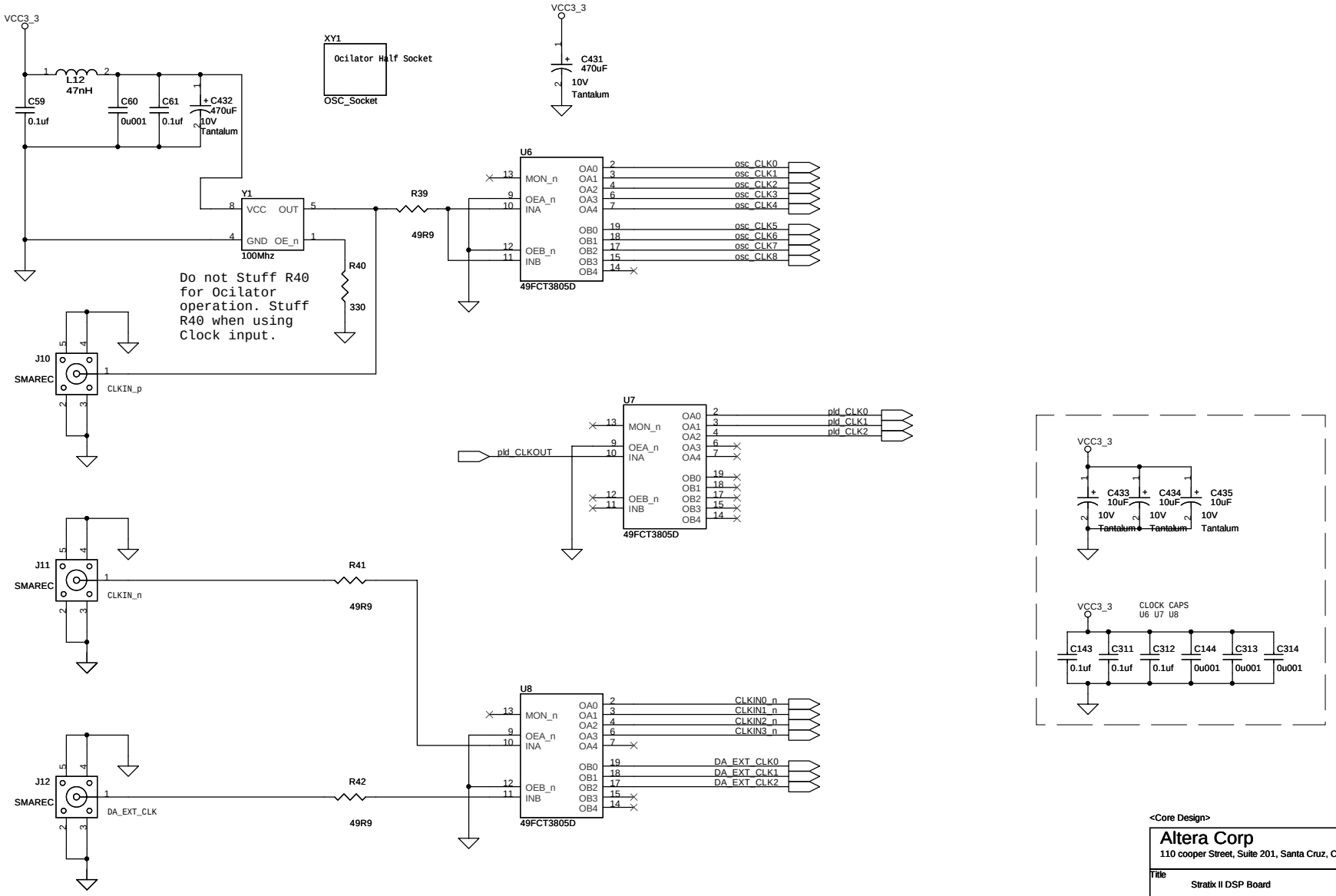
Title: Stratix II DSP Board

Size	Document Number	Rev
A	P06-10217R	03

Date: Thursday, April 06, 2006 Sheet 1 of 1

Clocks



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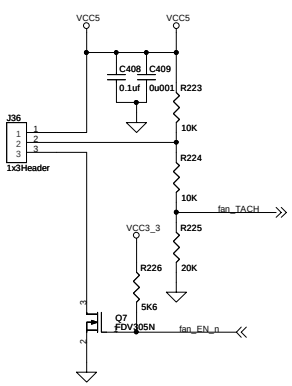
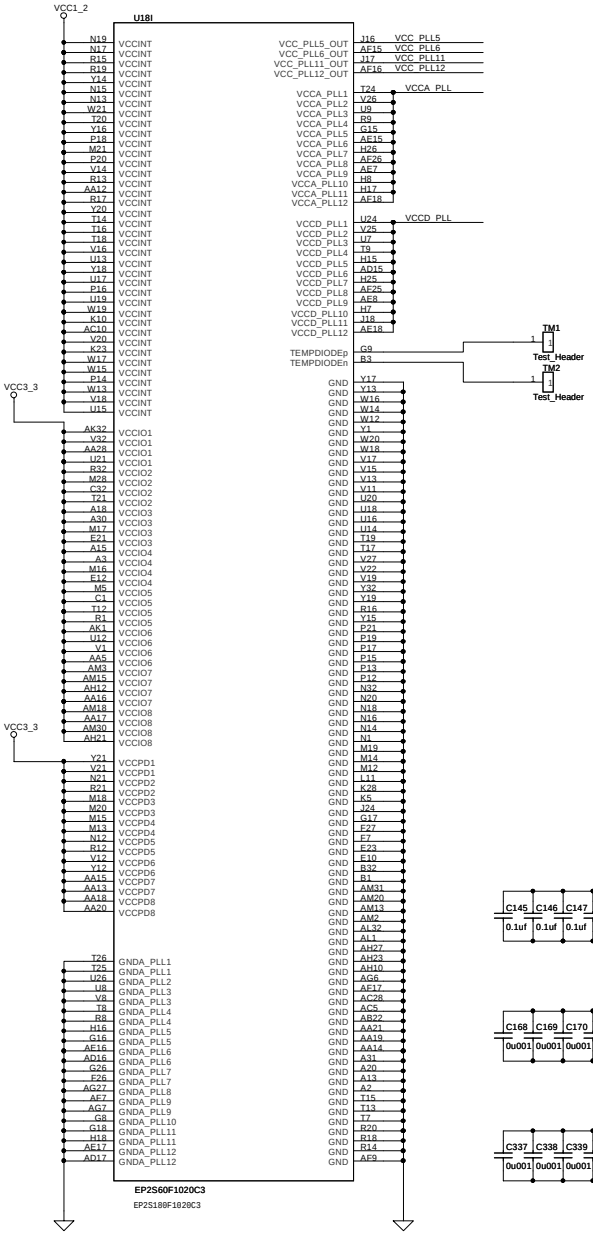
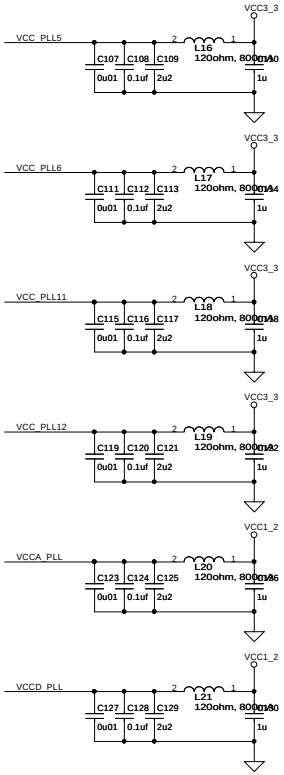
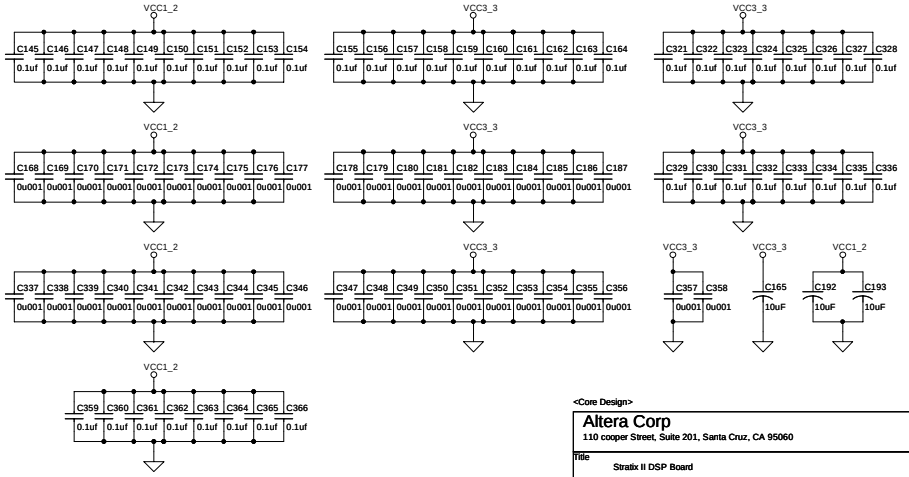
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	









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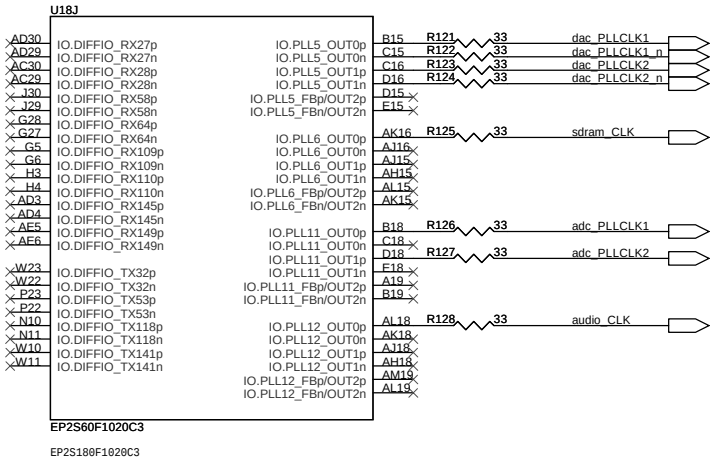
Title	Stratix II DSP Board	
Size C	Document Number P06-10217R	Rev 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

PLD Control Signals



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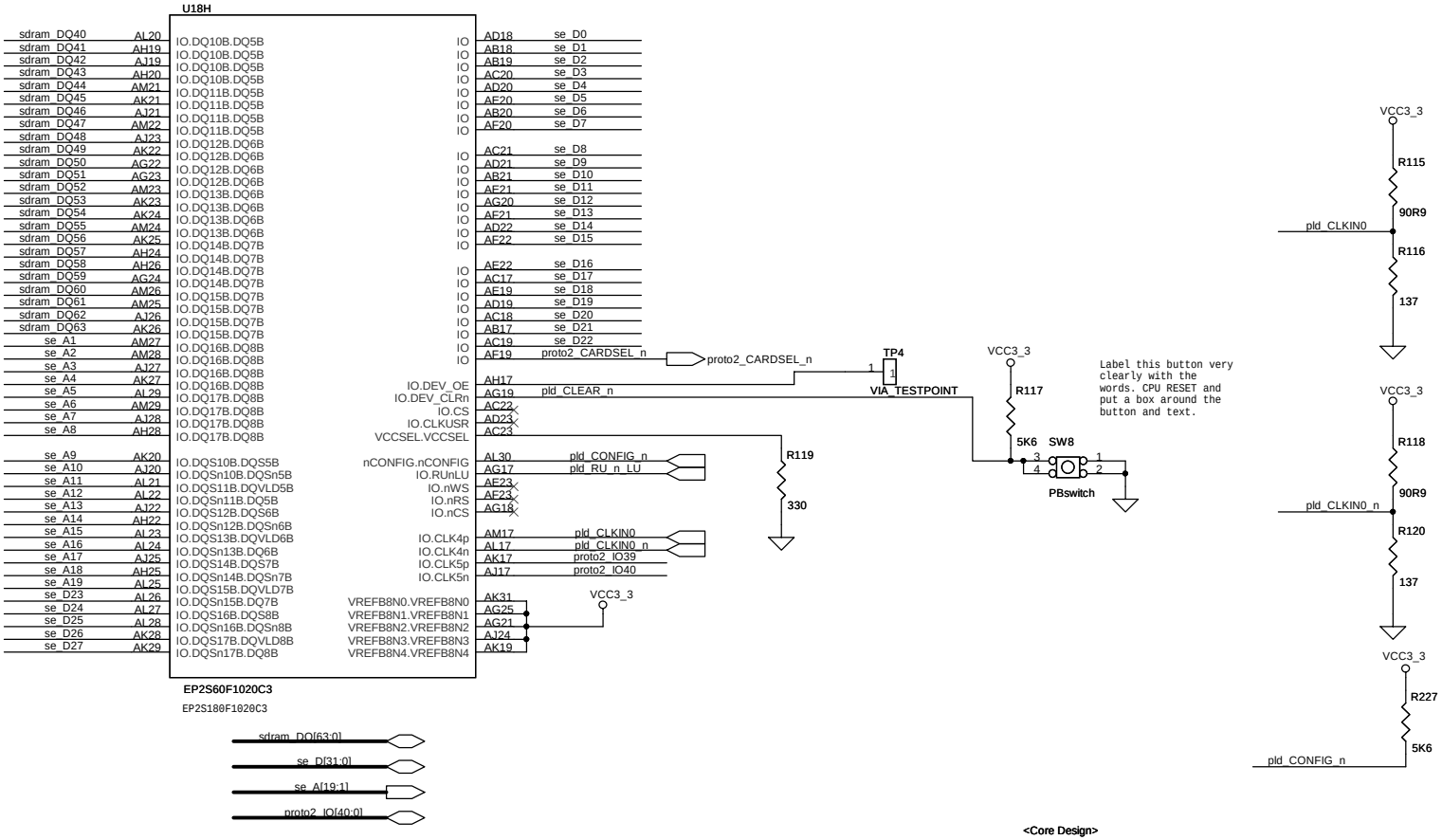
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

PLD Bank 8



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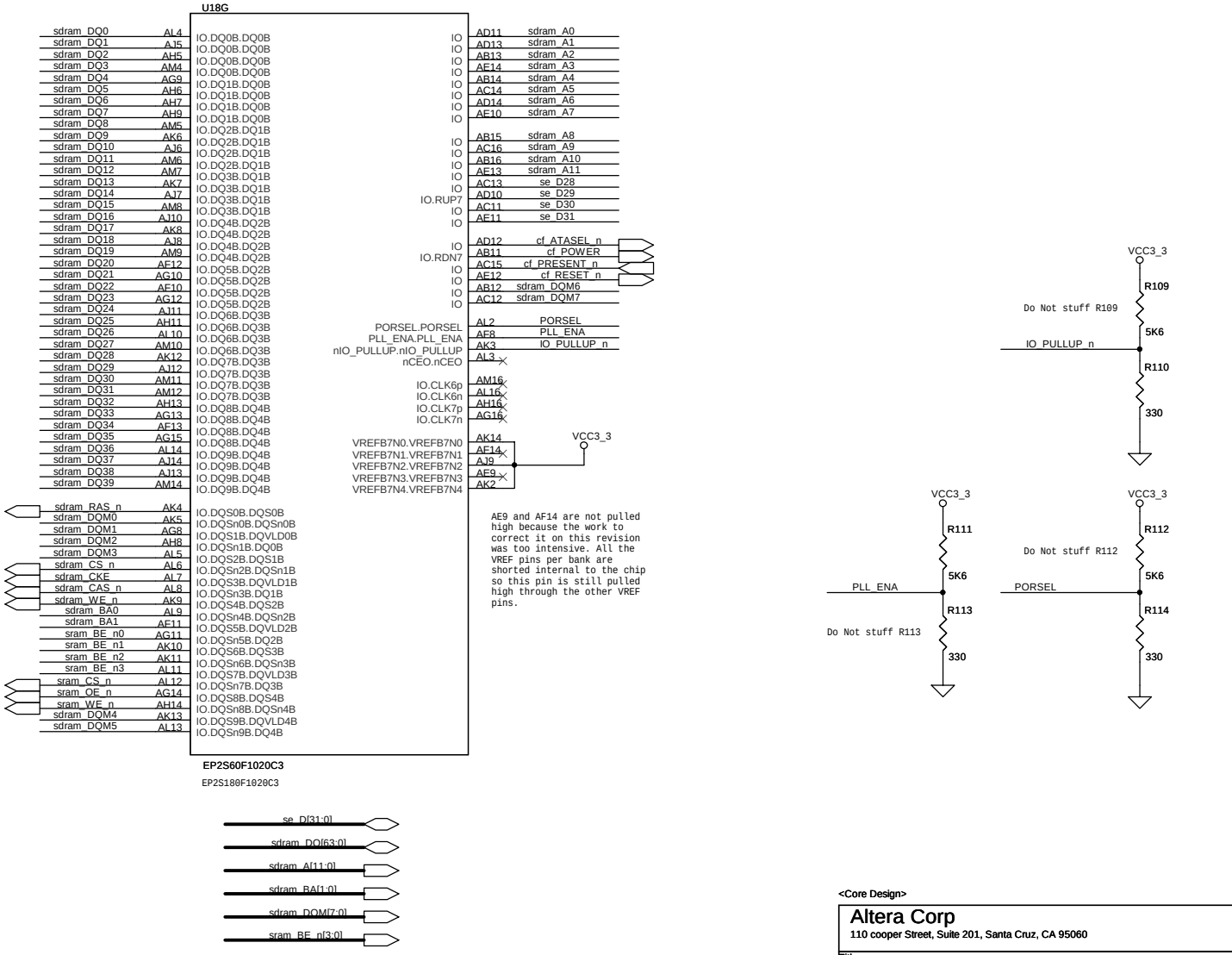
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

PLD Bank 7



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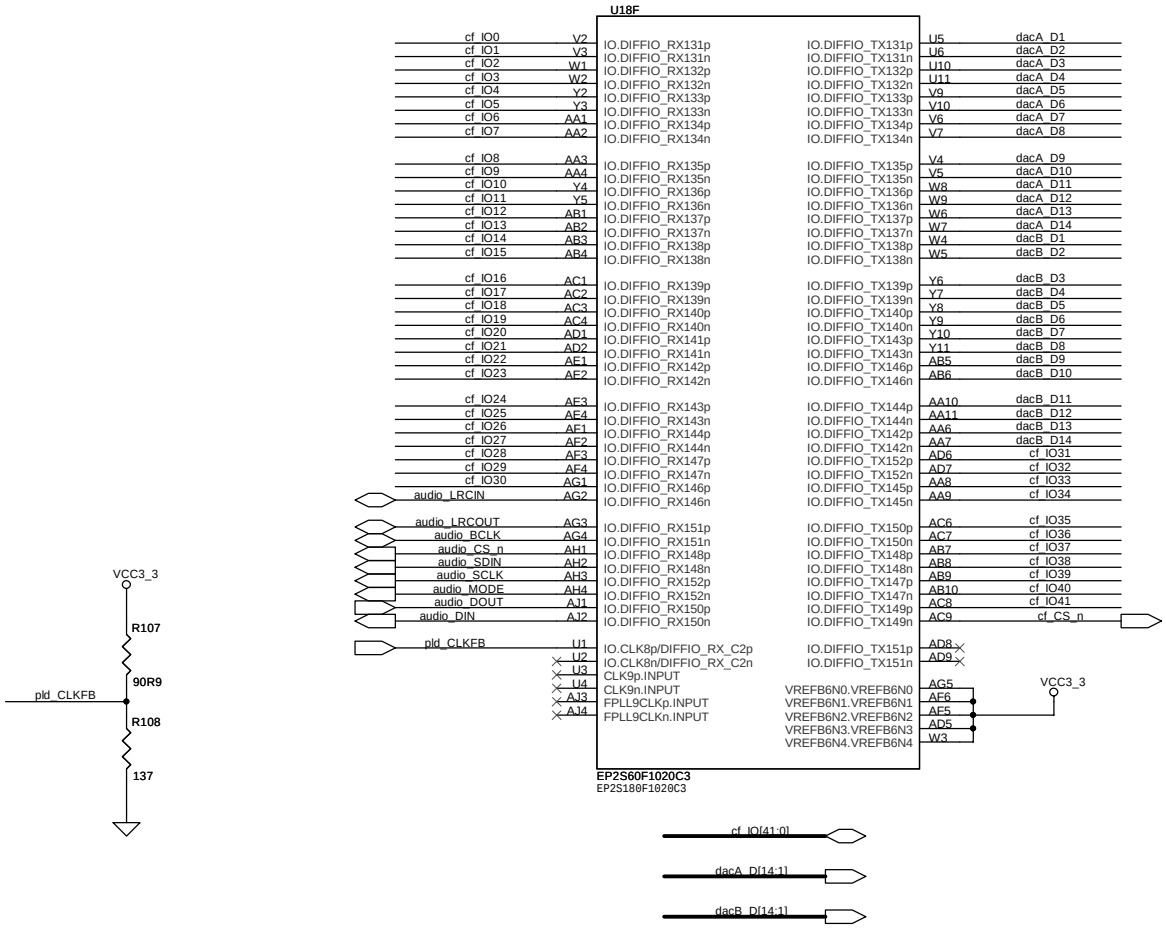
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

PLD Bank 6



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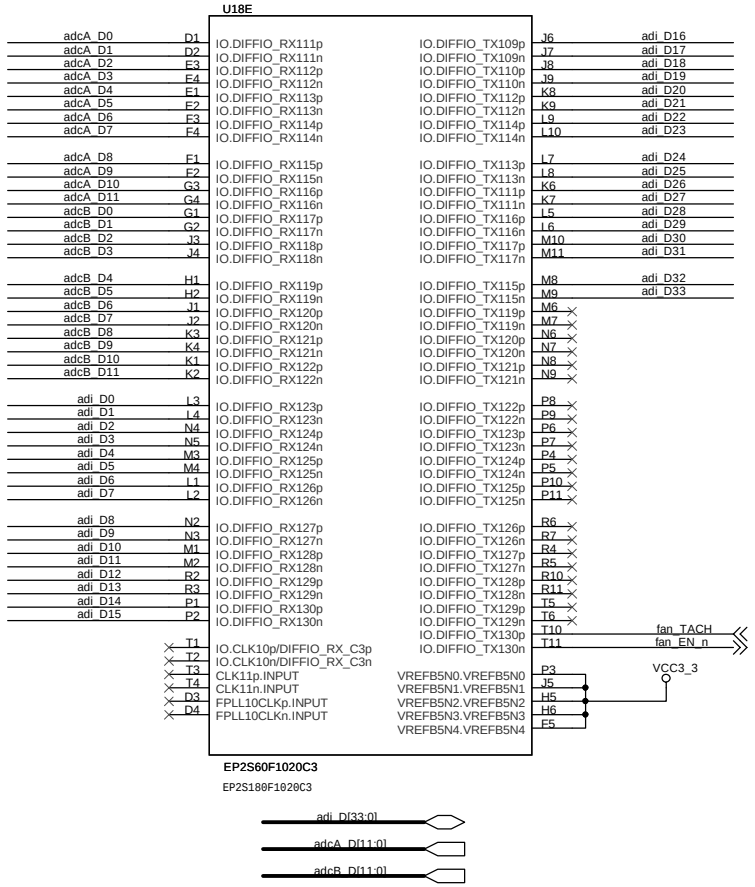
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

PLD Bank 5



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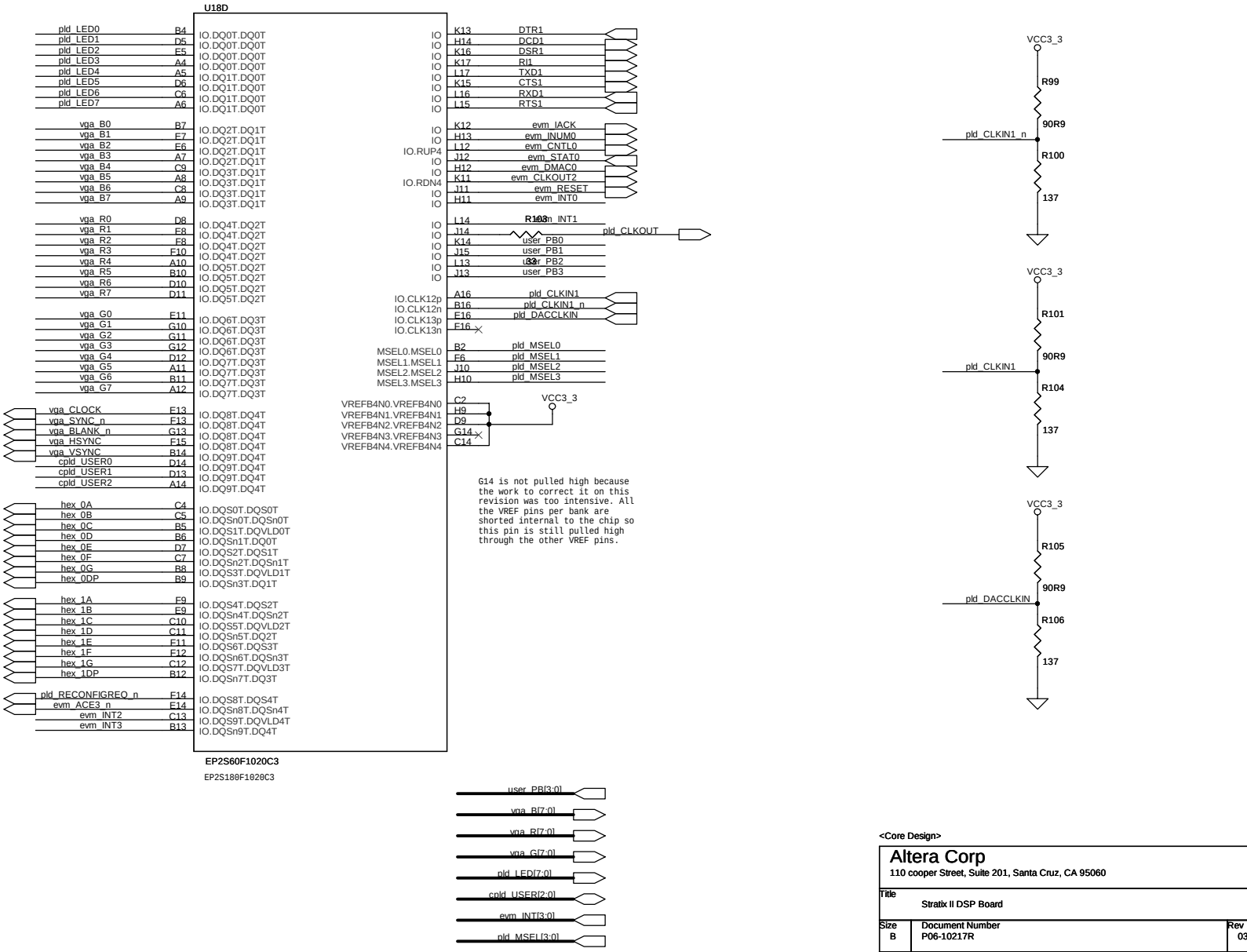
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

PLD Bank 4



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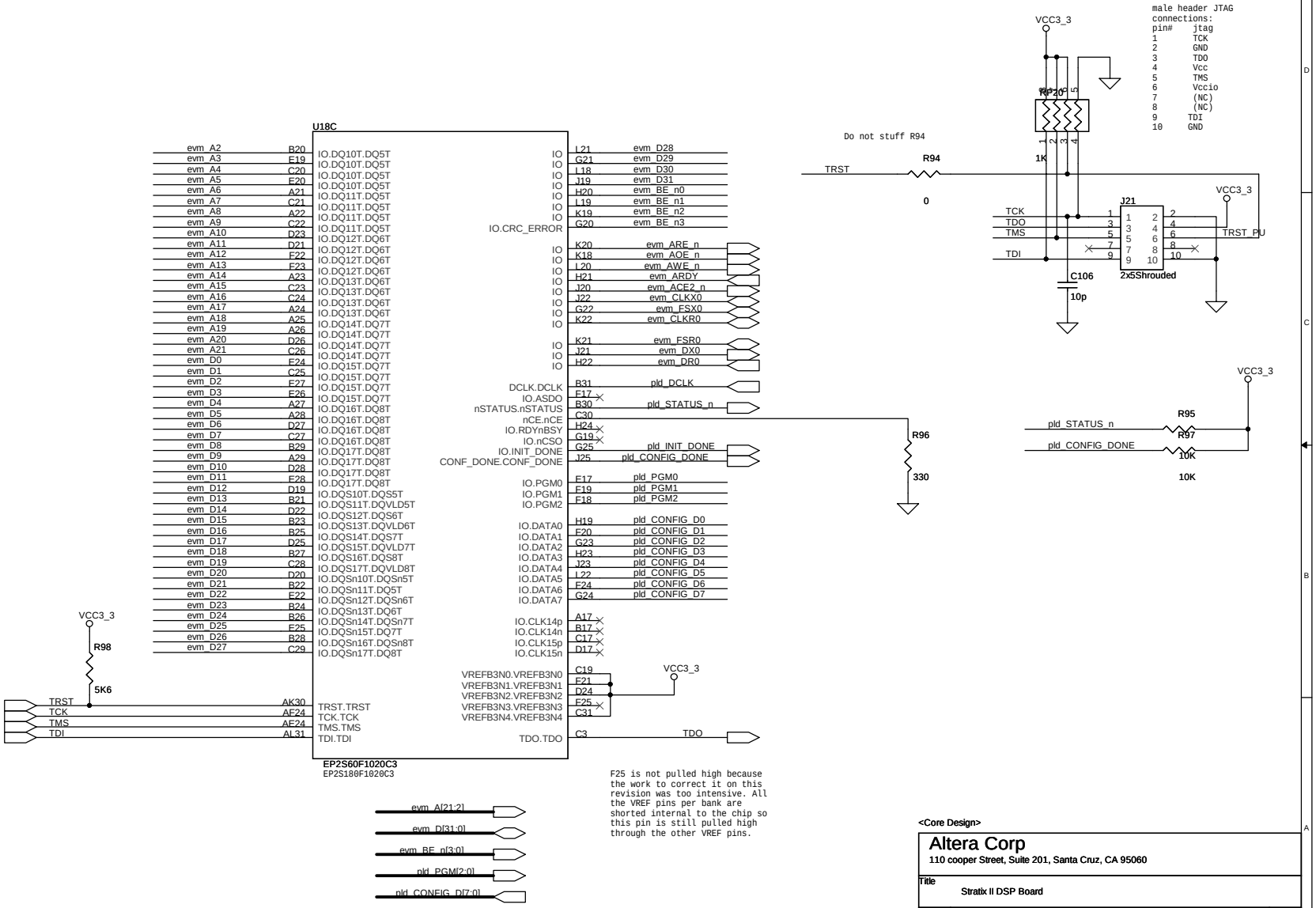
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

PLD Bank 3



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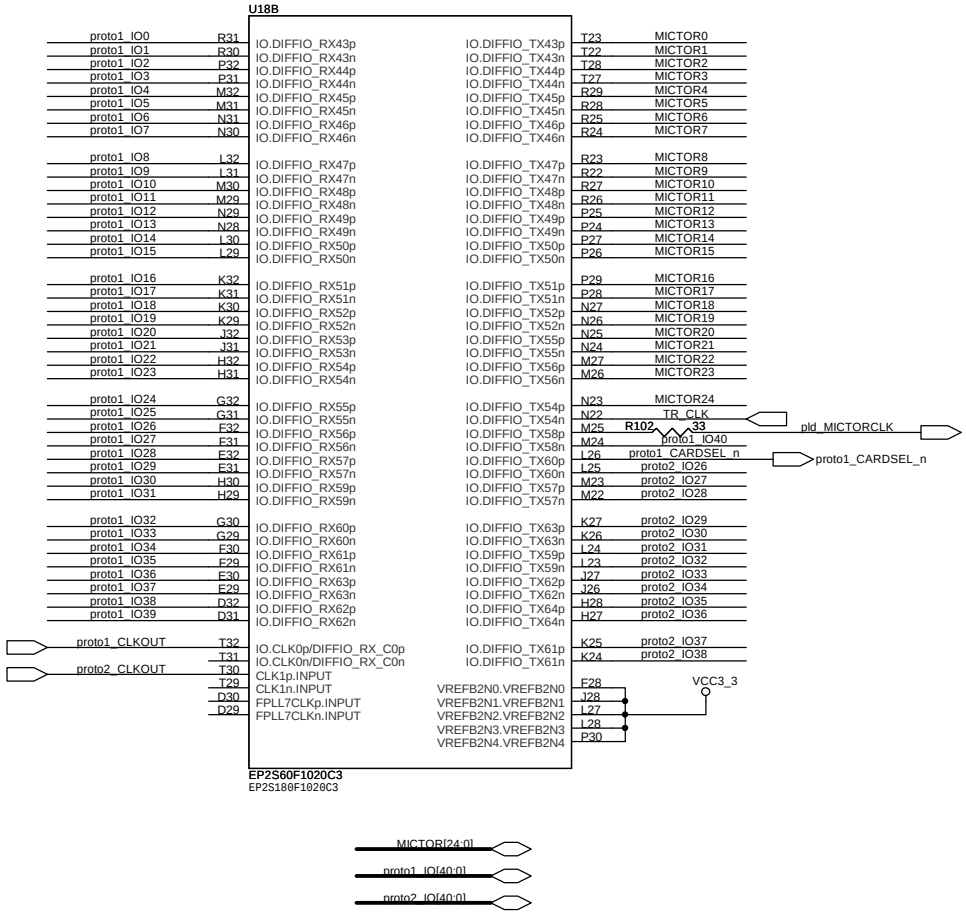
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

PLD Bank 2



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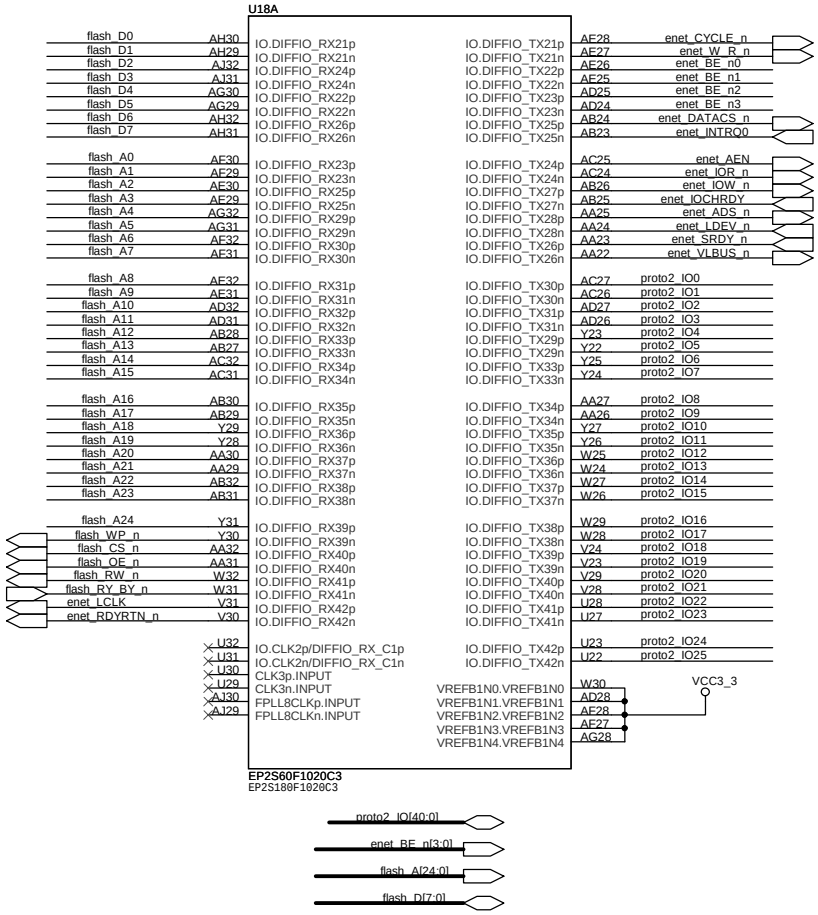
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	



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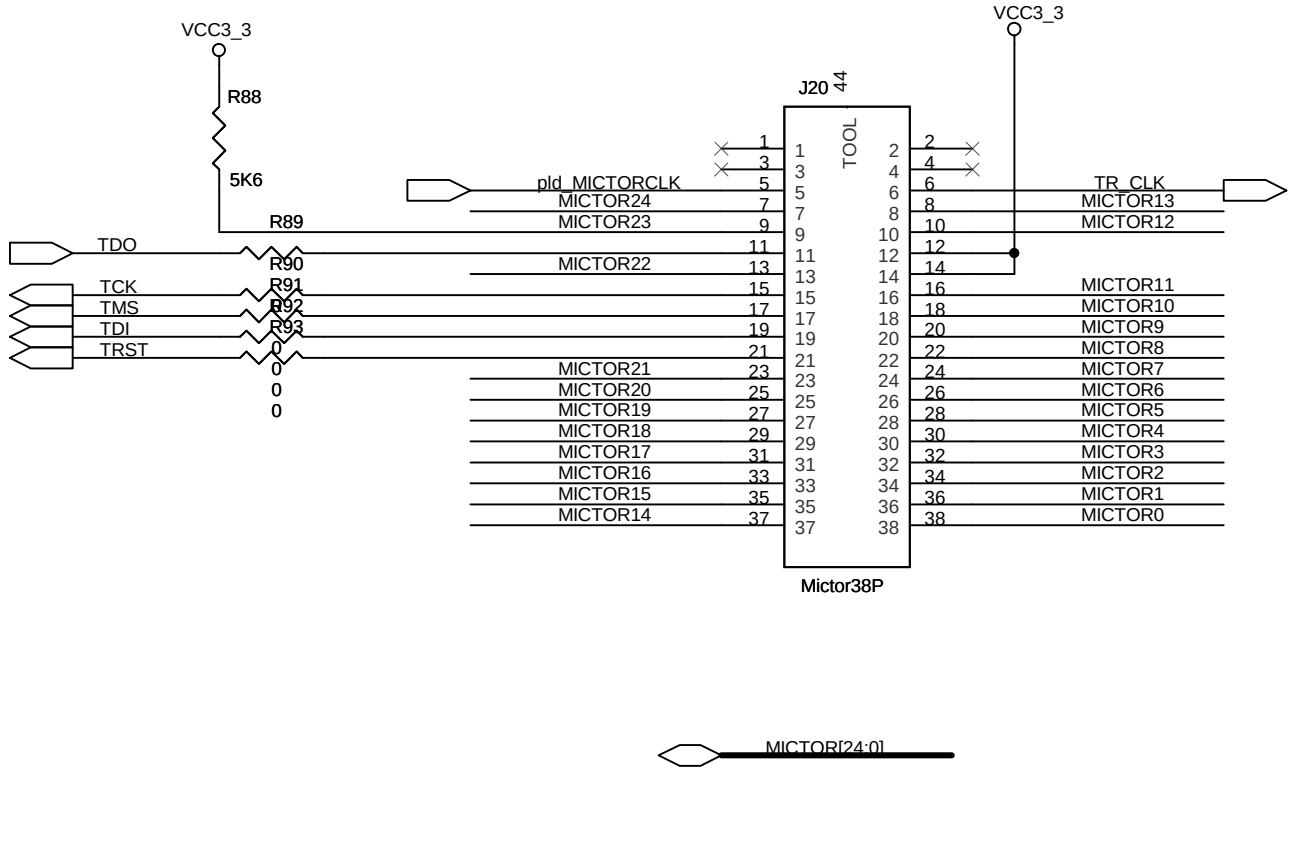
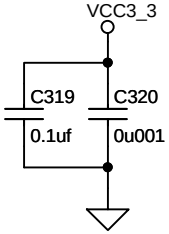
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Mictor Connector





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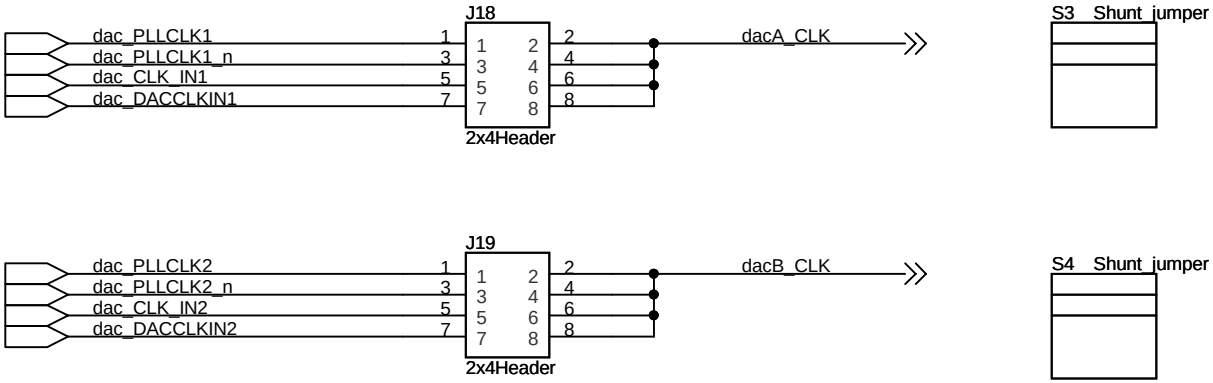
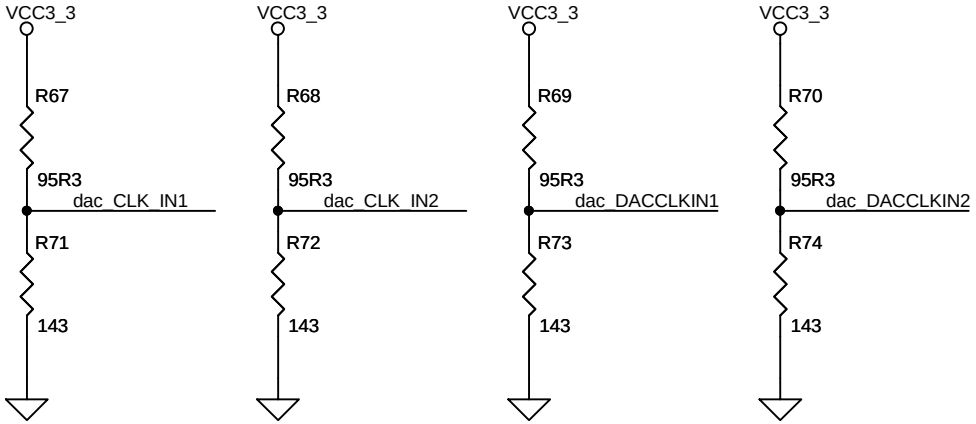
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

DAC Clock Jumper





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Altera Corp
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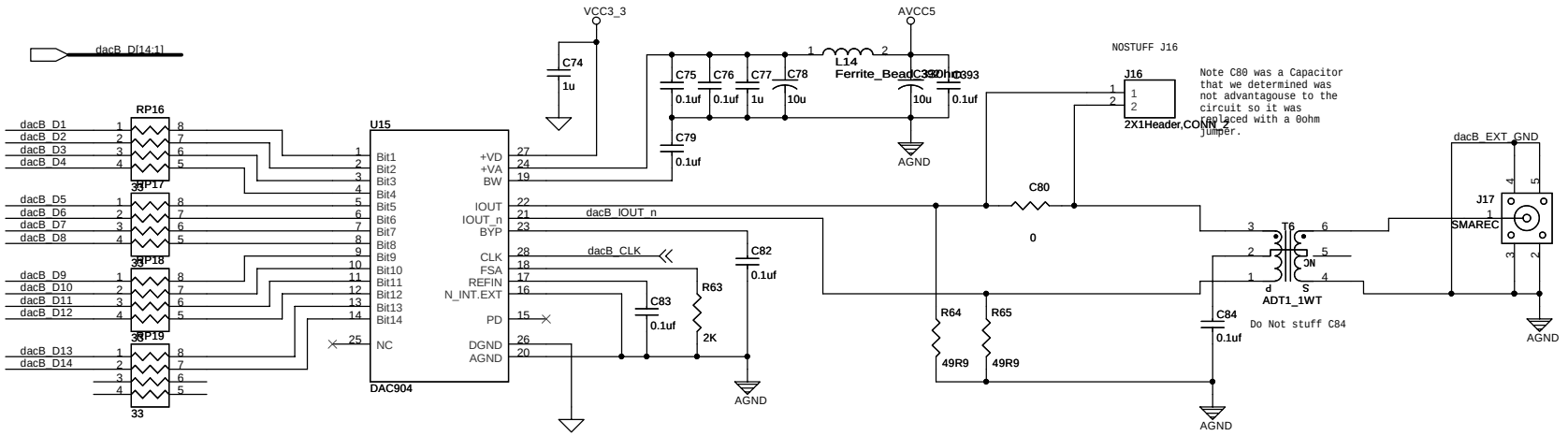
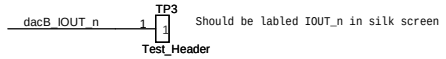
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

DAC B





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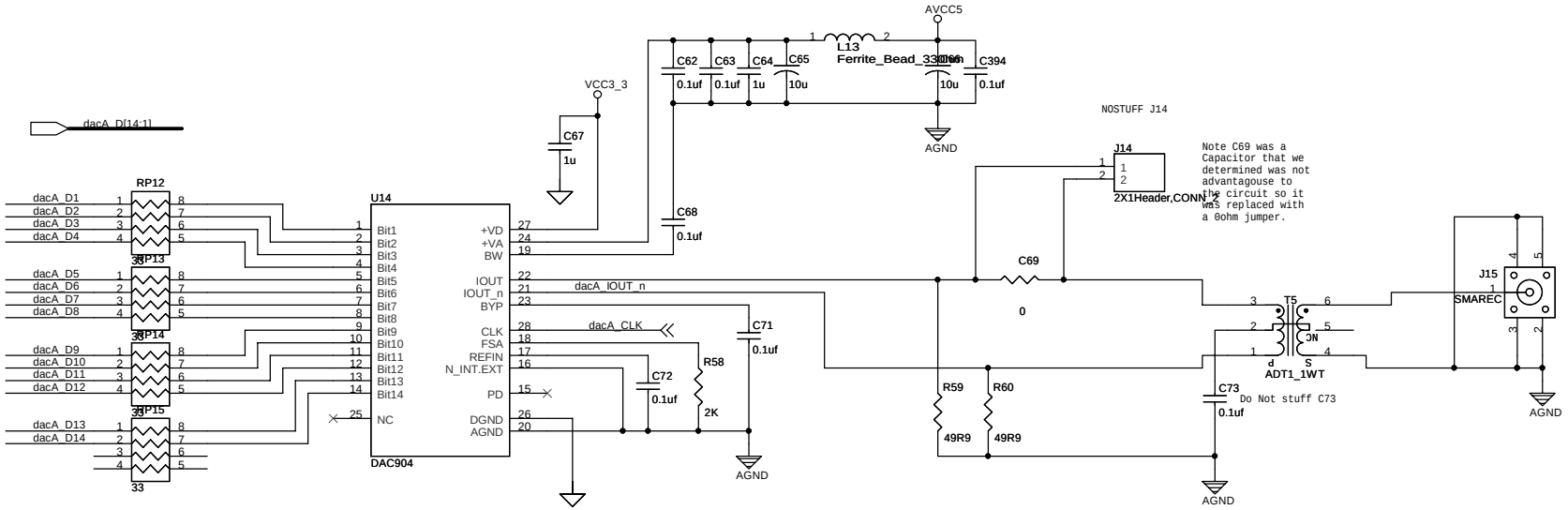
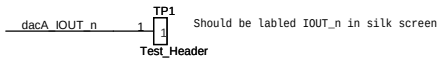
Altera Corp 110 cooper Street, Suite 201, Santa Cruz, CA 95060		
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

DAC A





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Altera Corp
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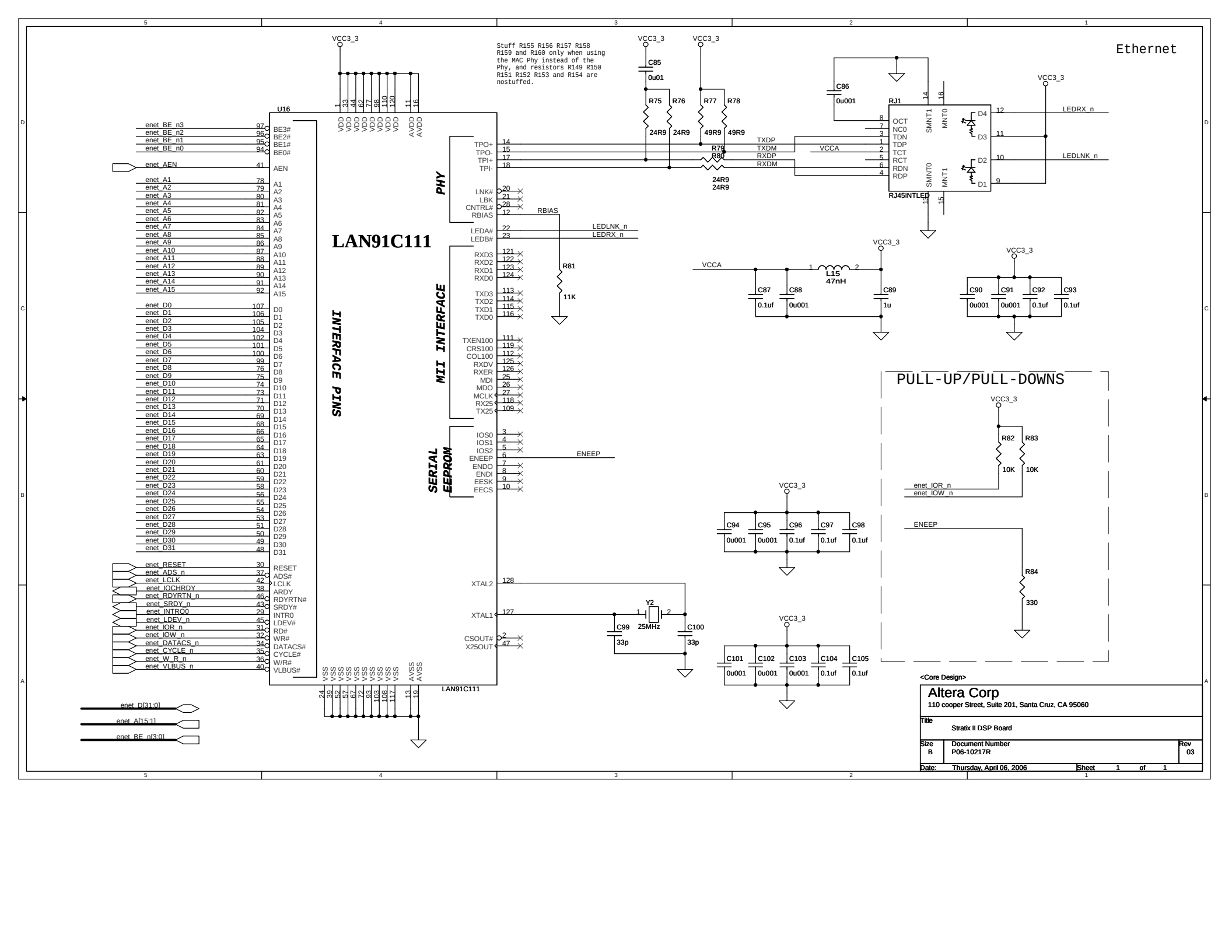
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	


Ethernet
Stuff R155 R156 R157 R158 R159 and R160 only when using the MAC Phy instead of the Phy, and resistors R149 R150 R151 R152 R153 and R154 are nostuffed.
LAN91C111
U16
PHY
MII INTERFACE
SERIAL EEPROM
INTERFACE PINS
RJ1
RJ45INTLED
PULL-UP/PULL-DOWNS
Y2
25MHz
L15
47nH
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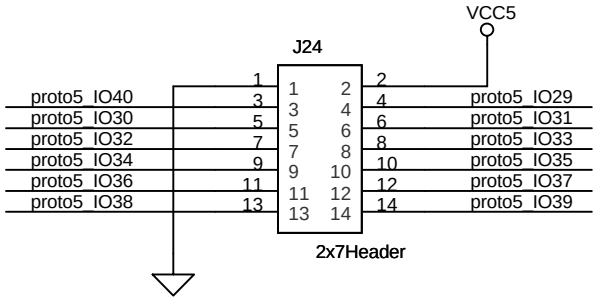
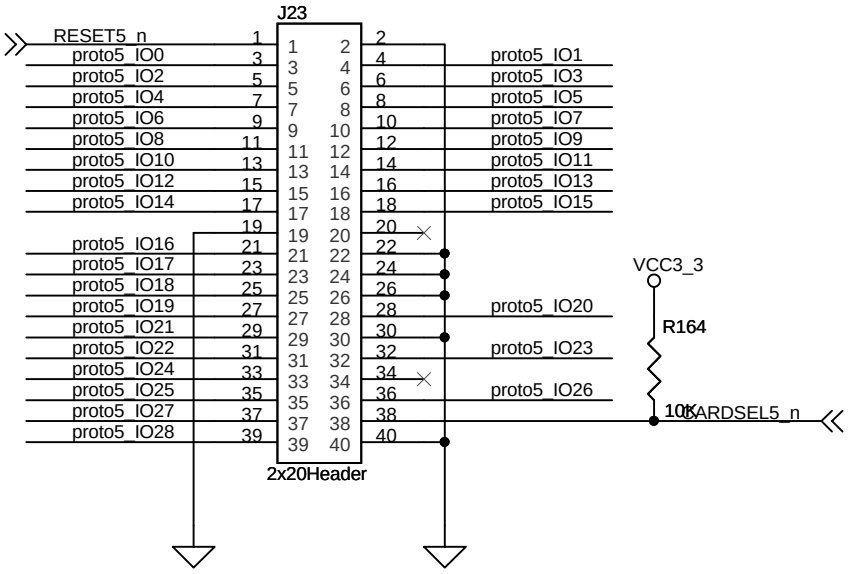
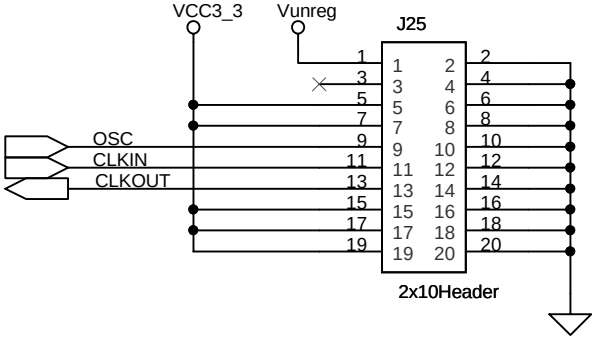
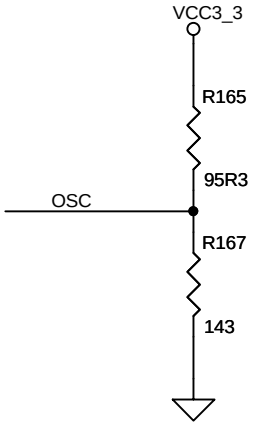
Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060
Title
Stratix II DSP Board
Size B
Document Number P06-10217R
Rev 03
Date: Thursday, April 06, 2006
Sheet 1 of 1

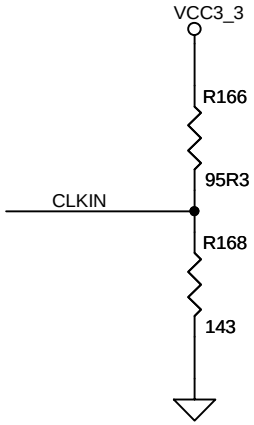
Protocard 1

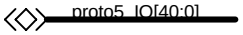


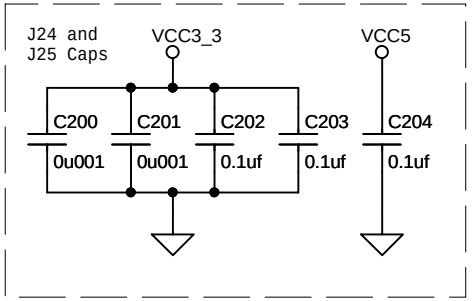












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Altera Corp
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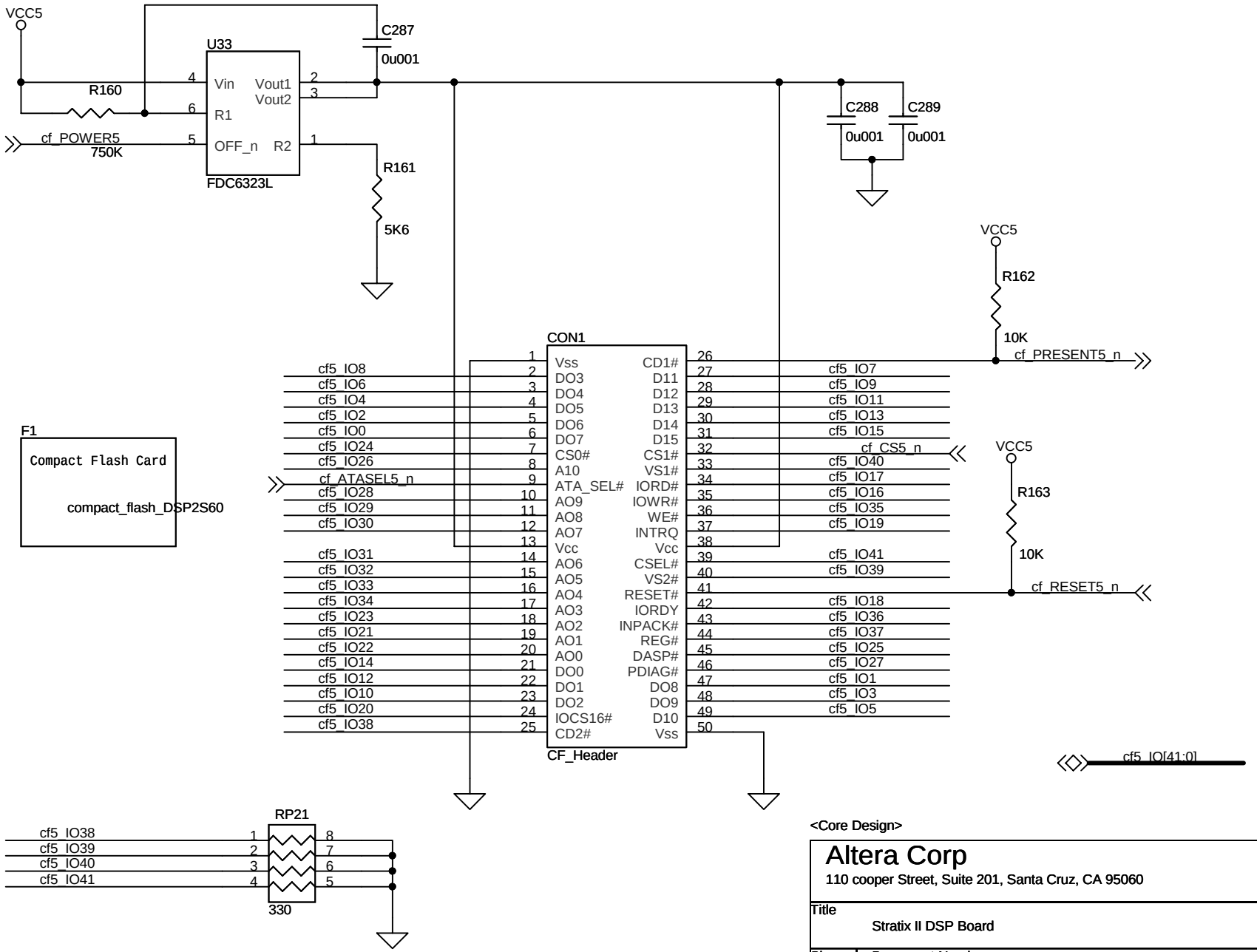
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Compact Flash Socket



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Altera Corp
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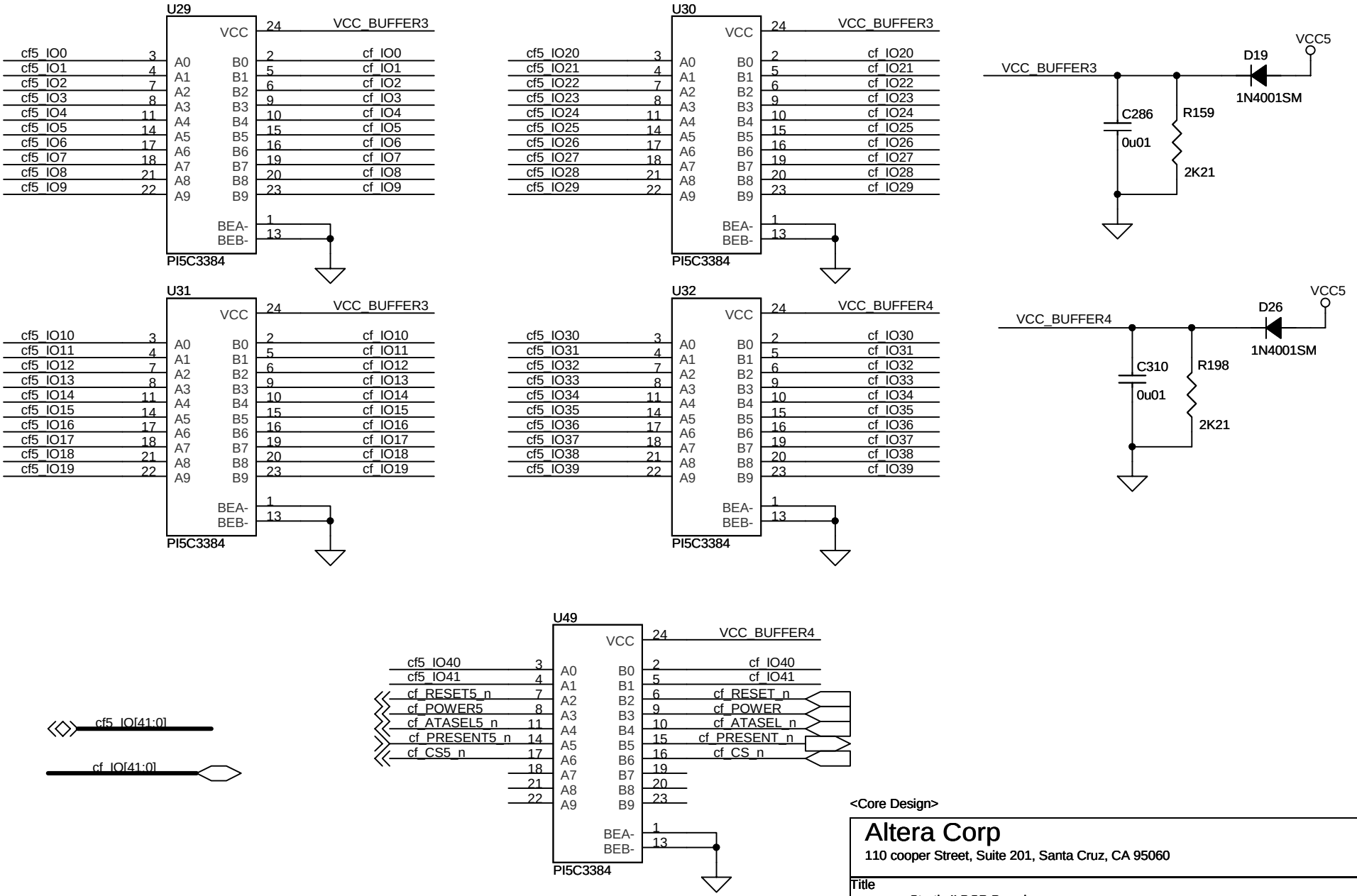
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Proto1 Buffers



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Altera Corp
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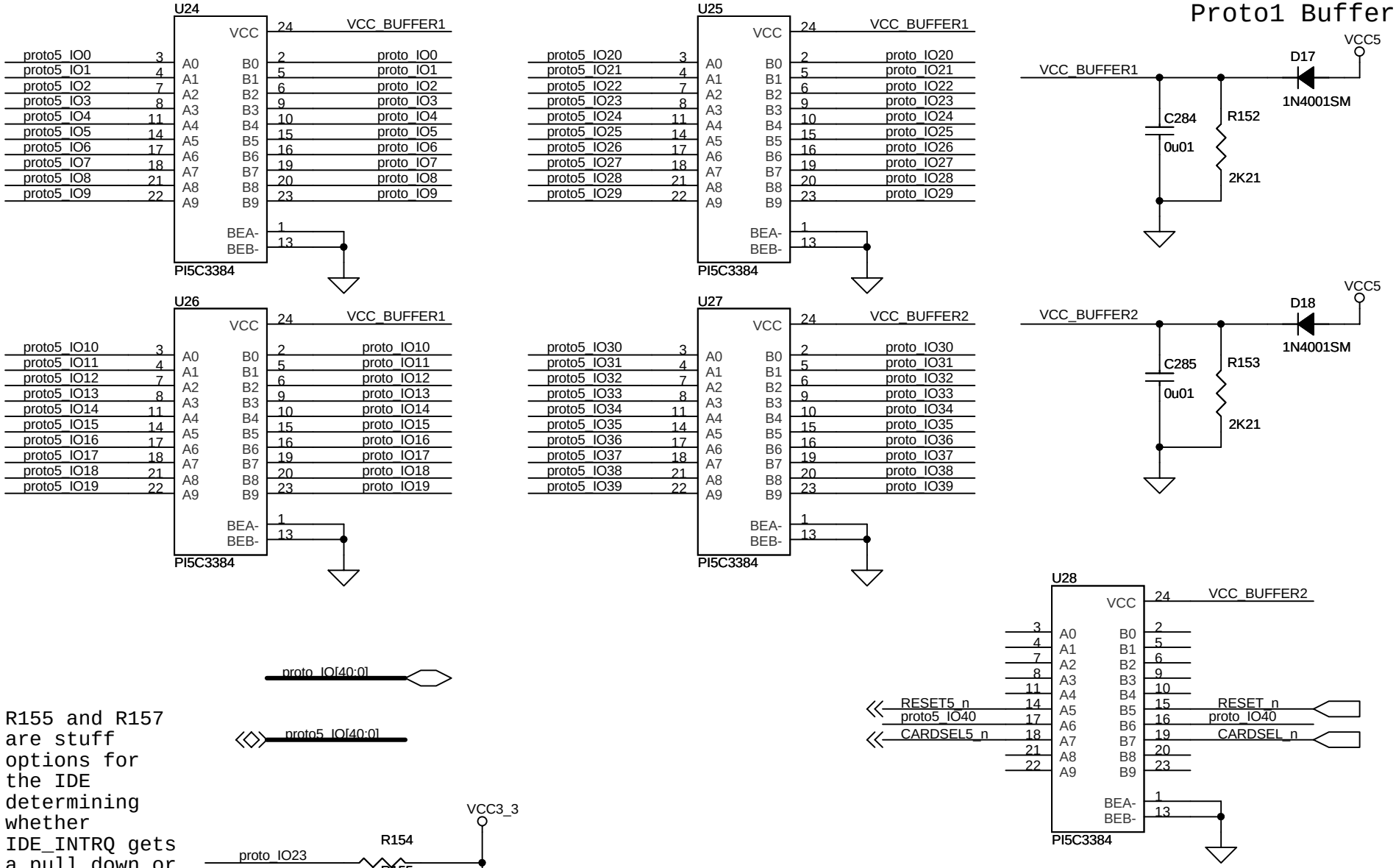
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Proto1 Buffers



R155 and R157 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R155 should be a nostuff for production.

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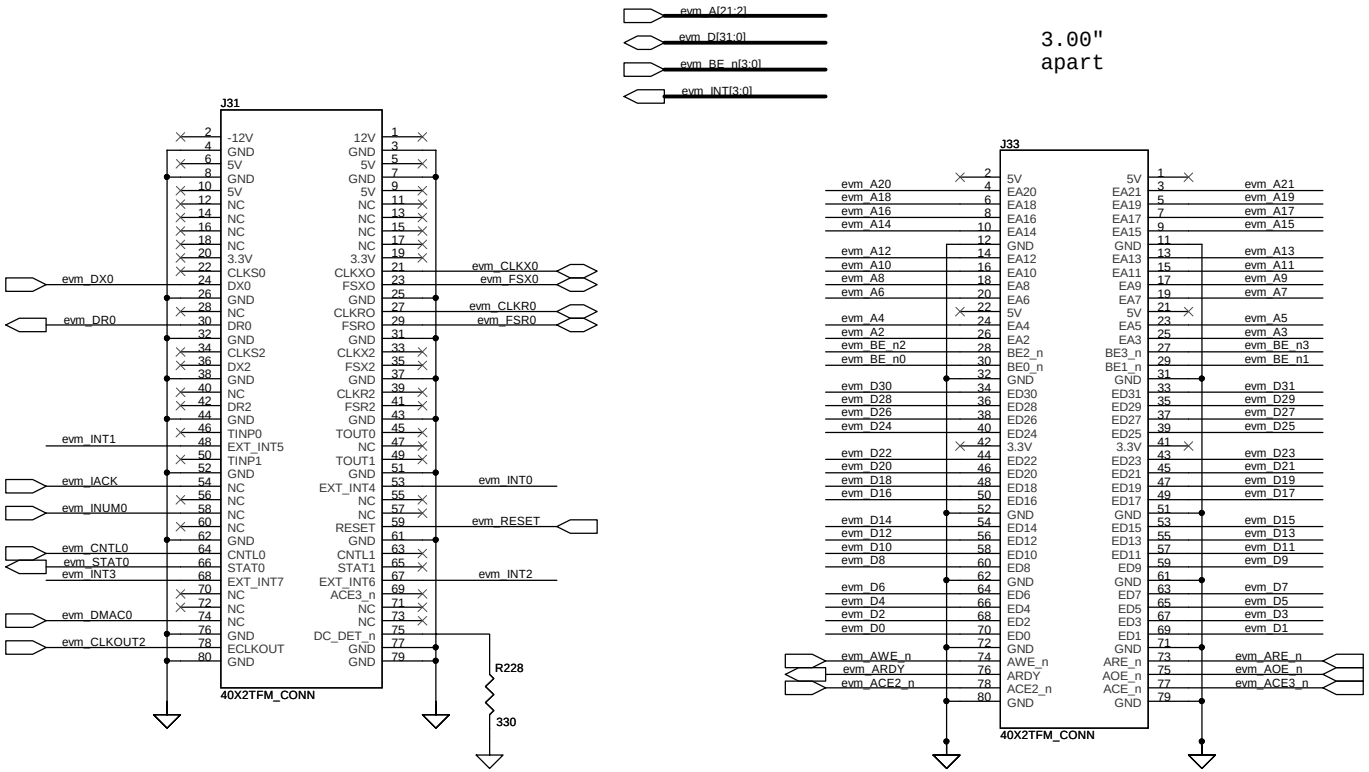
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

TI EVM Connector



These connectors reference the TI 6416 board

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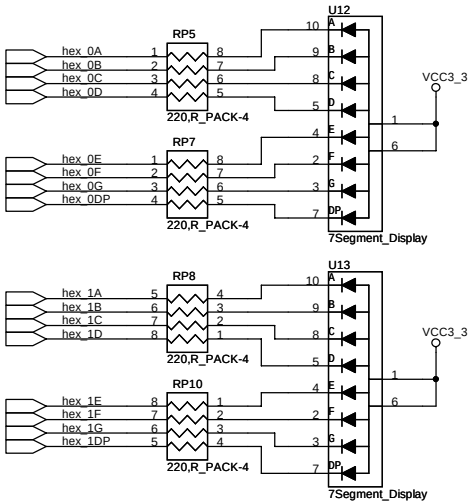
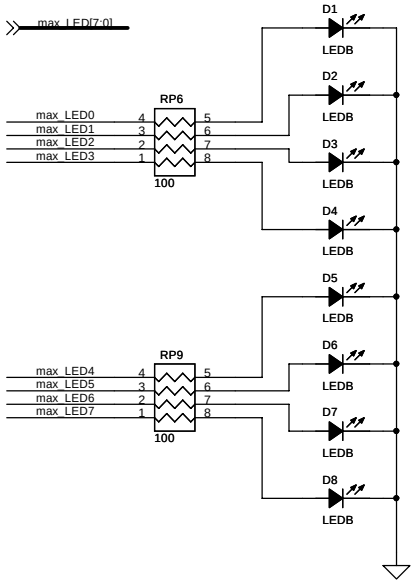
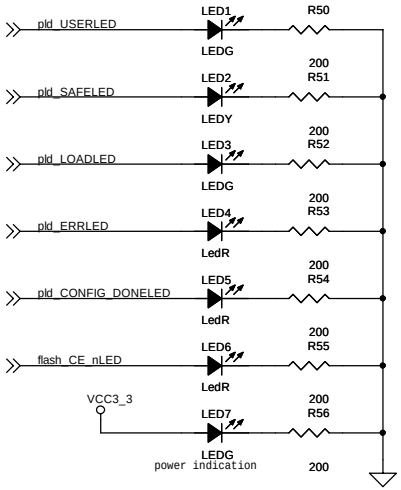
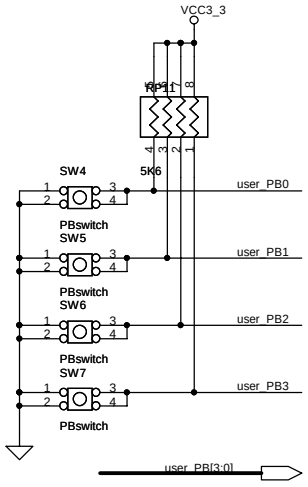
Altera Corp 110 cooper Street, Suite 201, Santa Cruz, CA 95060	
Title: Stratix II DSP Board	
Size: B	Document Number: P06-10217R — Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1









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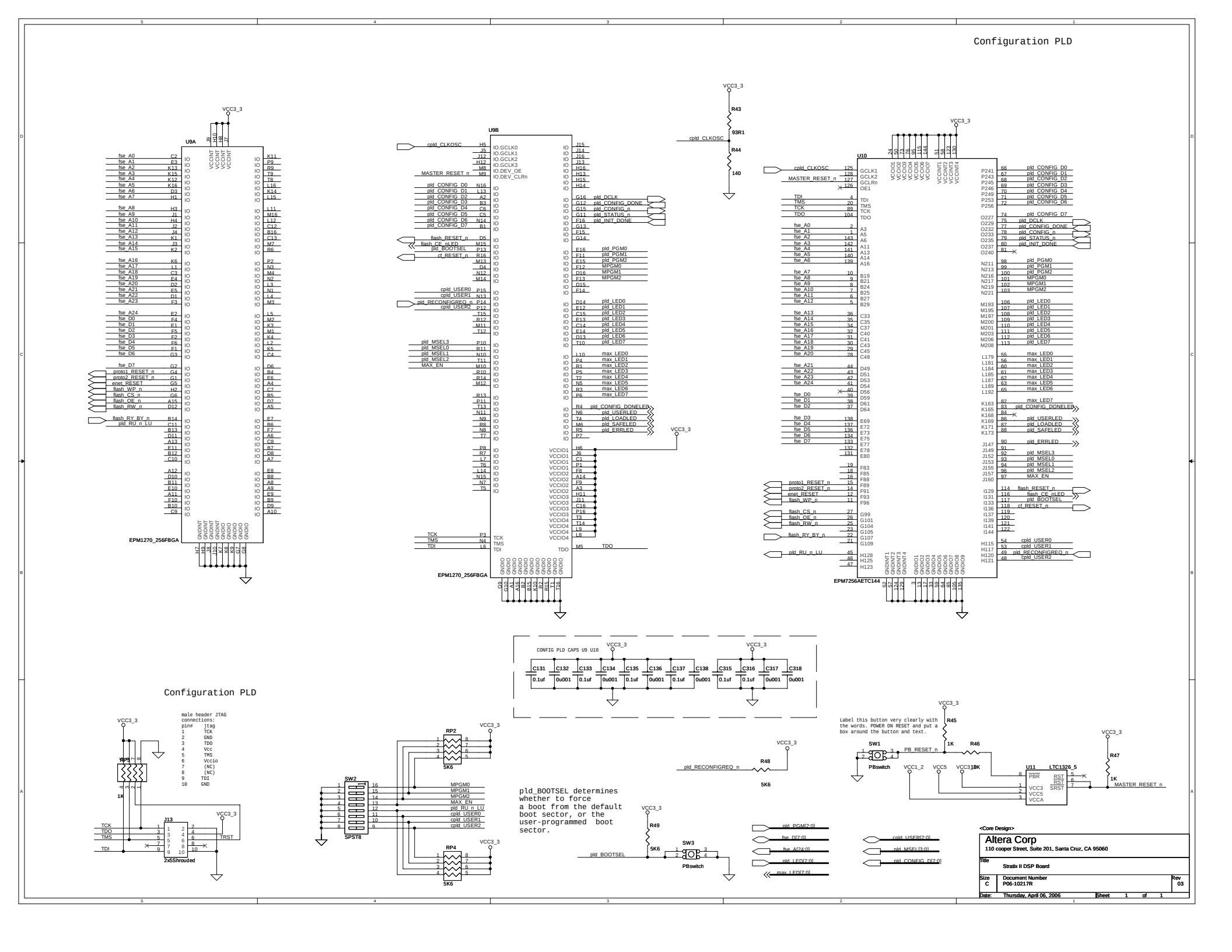
Altera Corp 110 cooper Street, Suite 201, Santa Cruz, CA 95060		
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	


Configuration PLD
U9A
U9B
U10
EPM1270_256FBGA
EPM7256AETC144
CONFIG PLD CAPS U9 U10
male header JTAG connections:
pin# jtag
1 TCK
2 GND
3 TDO
4 Vcc
5 TMS
6 Vccio
7 (NC)
8 (NC)
9 TDI
10 GND
2x5Shrouded
SPST8
PBswitch
pld_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.
Label this button very clearly with the words. POWER ON RESET and put a box around the button and text.
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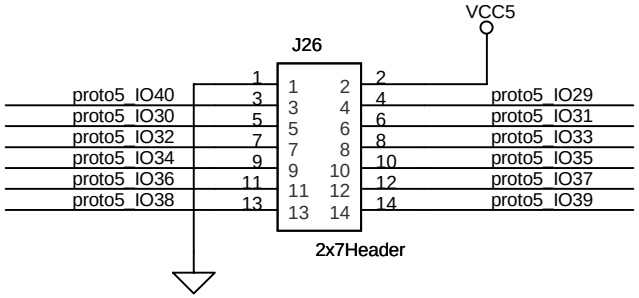
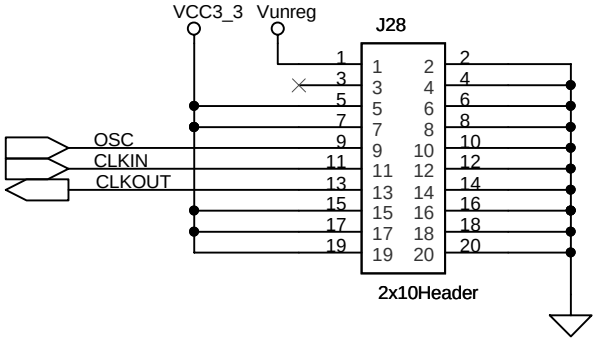
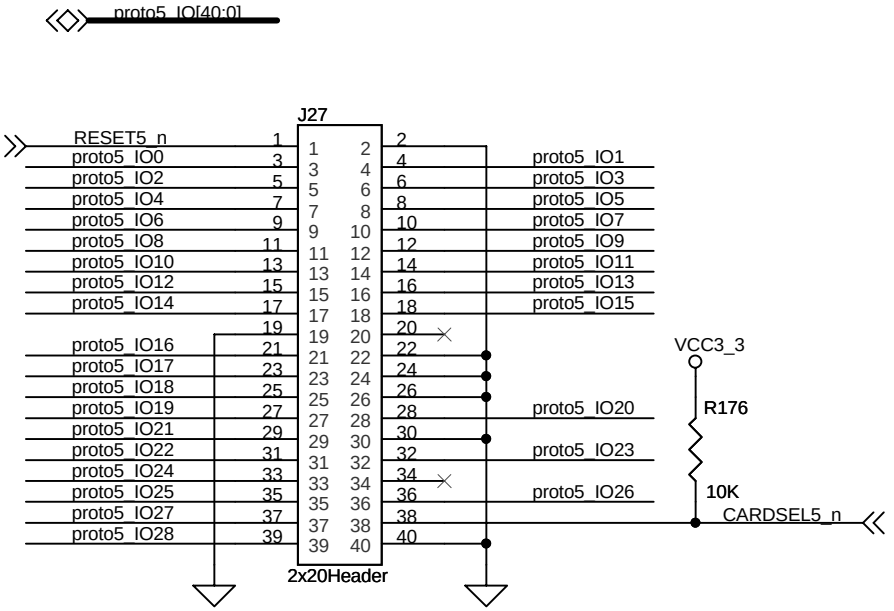
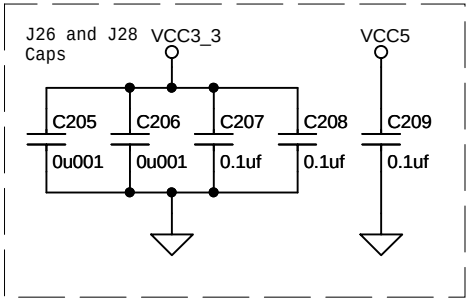
Stratix II DSP Board
Document Number P06-10217R
Rev 03
Thursday, April 06, 2006
Sheet 1 of 1

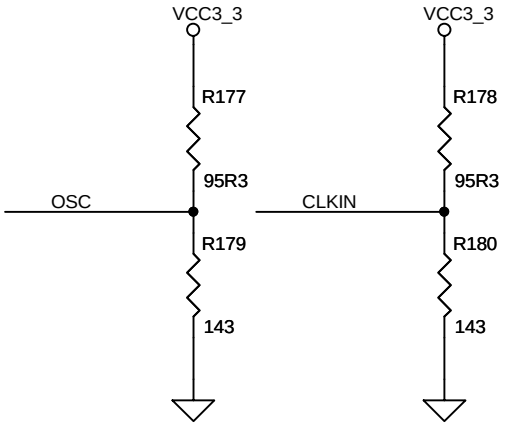
Proto2 Headers











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Altera Corp
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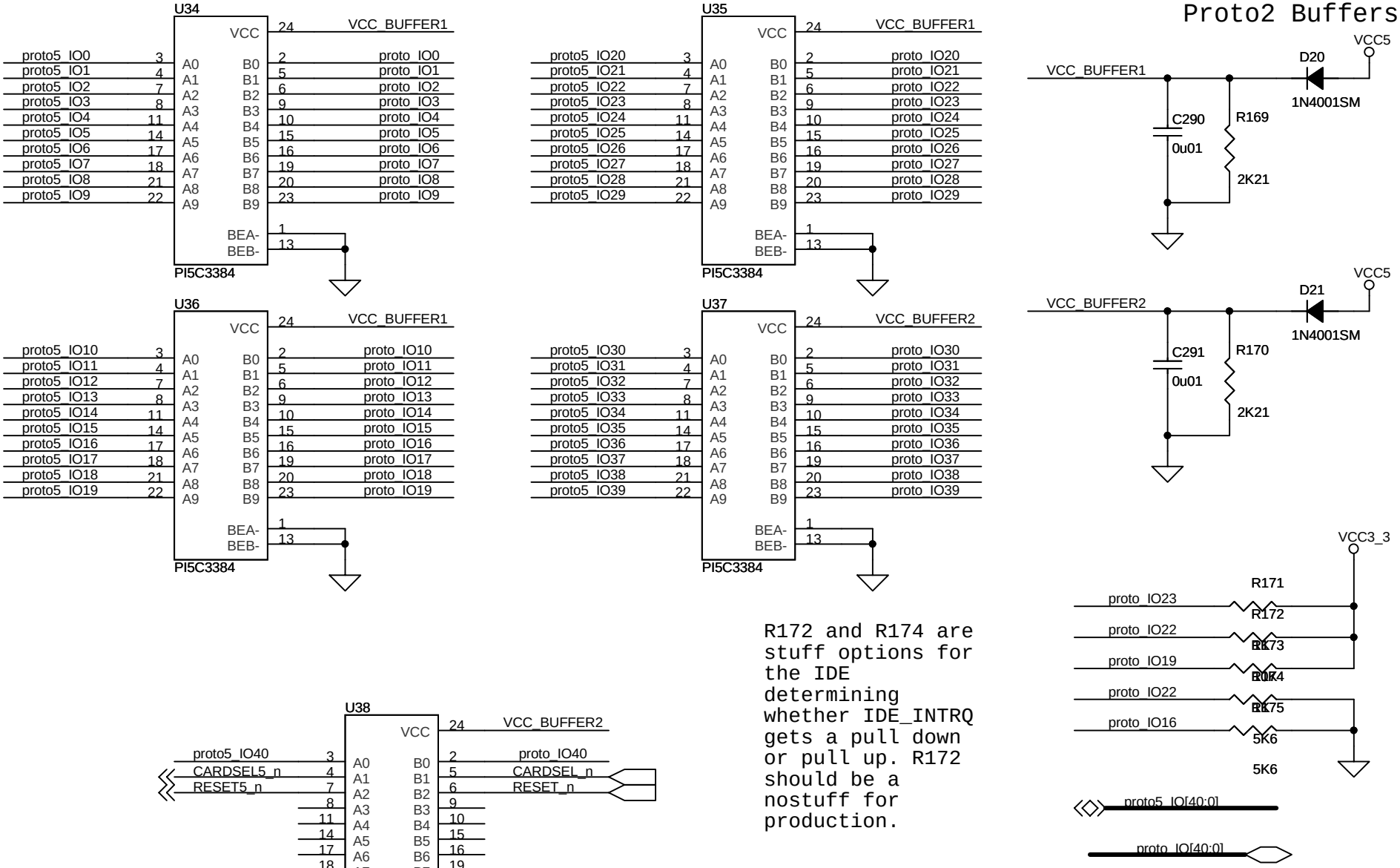
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Proto2 Buffers



R172 and R174 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R172 should be a nostuff for production.

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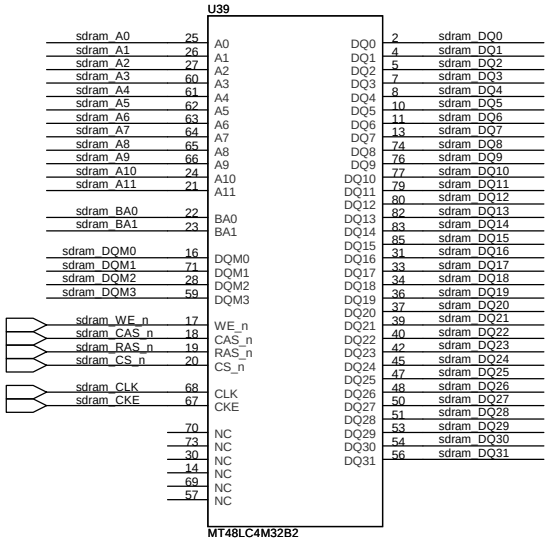
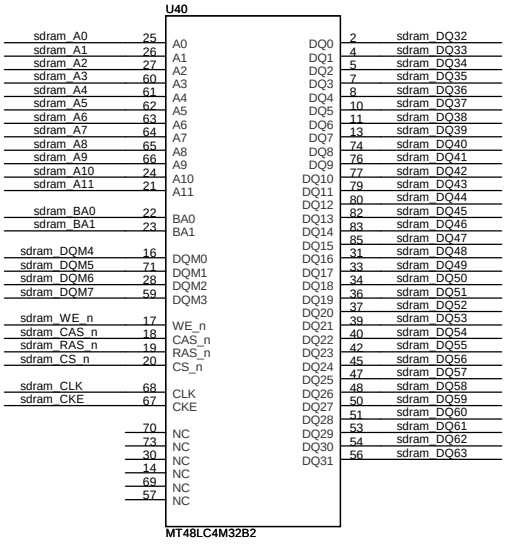
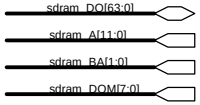
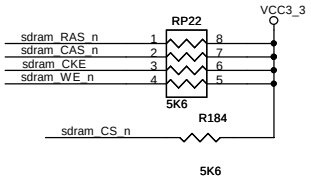
Altera Corp 110 cooper Street, Suite 201, Santa Cruz, CA 95060		
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

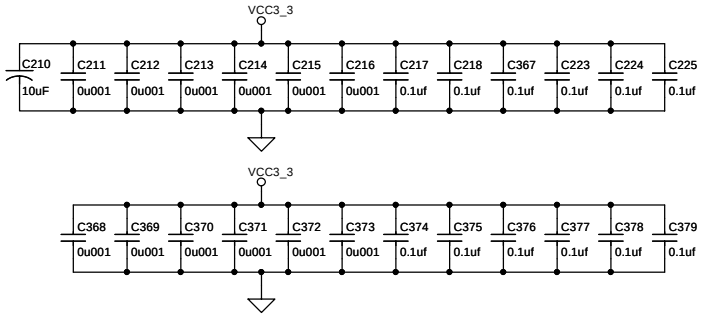
SDRAM











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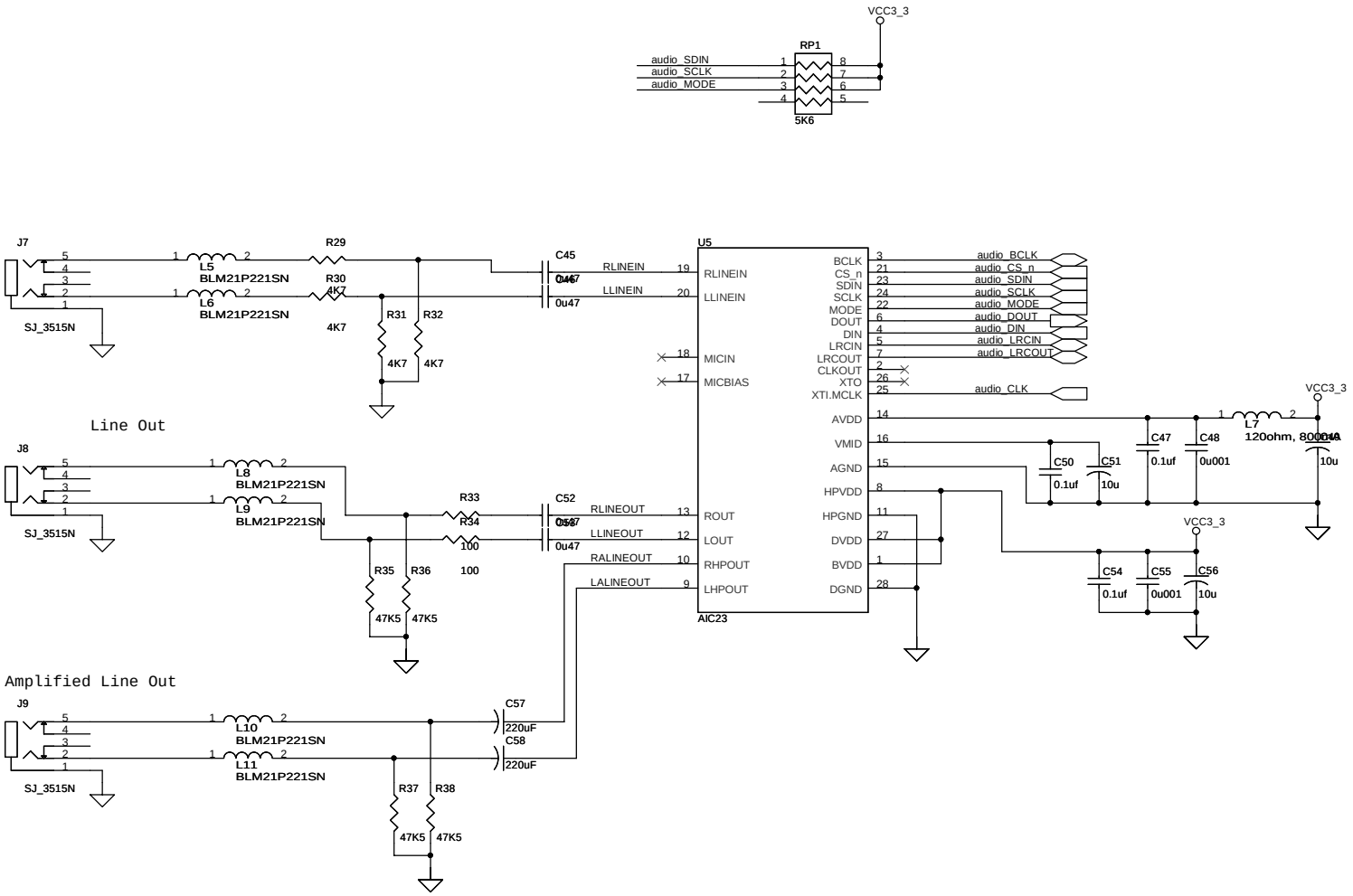
Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Audio



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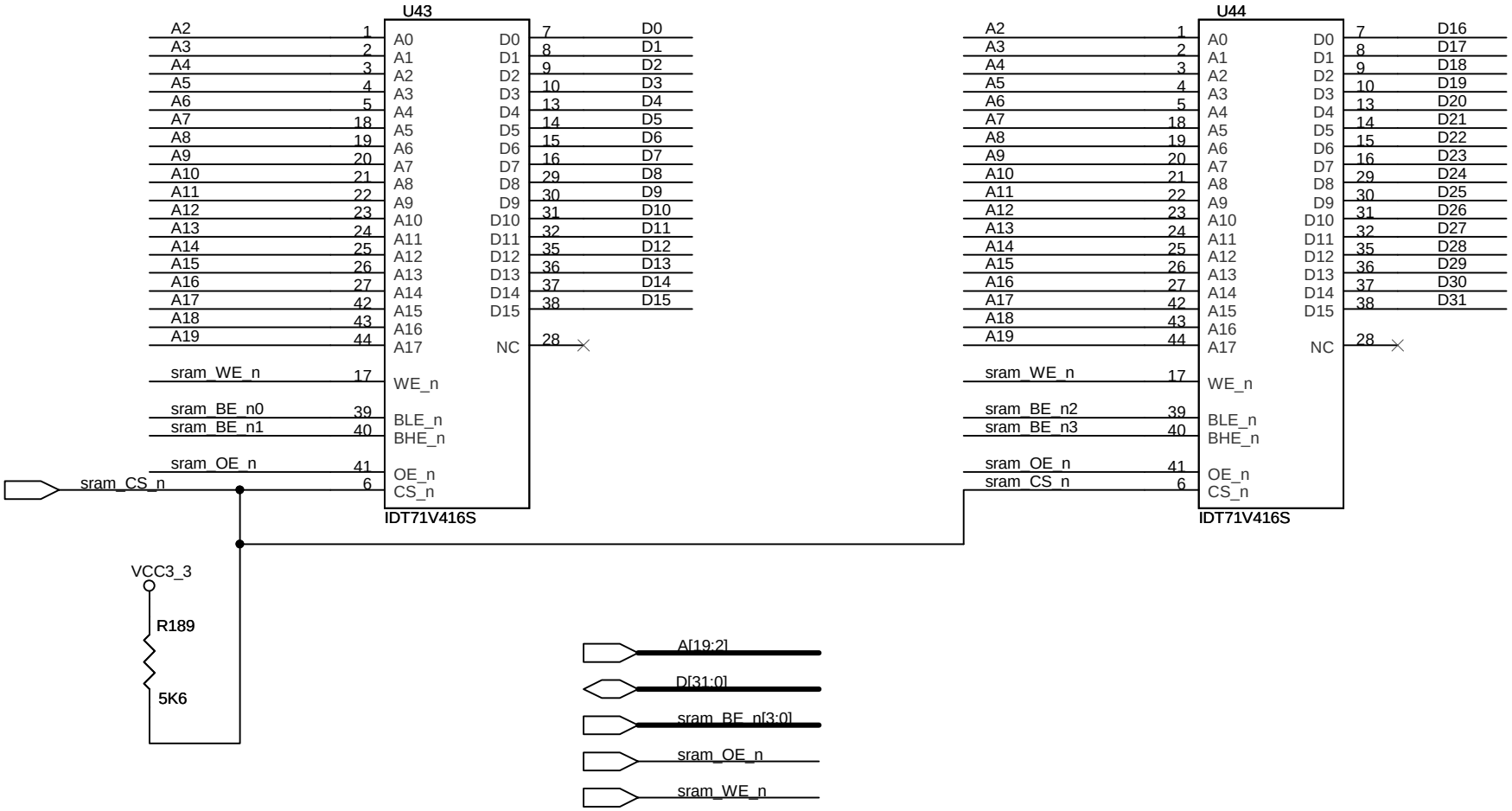
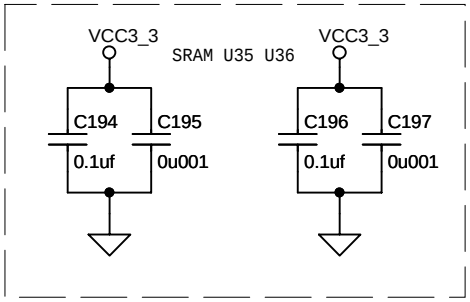
Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

SRAM





One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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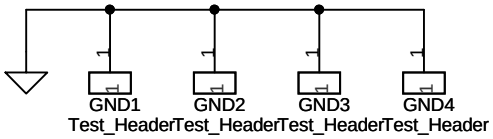
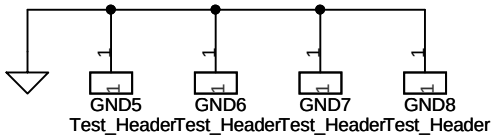
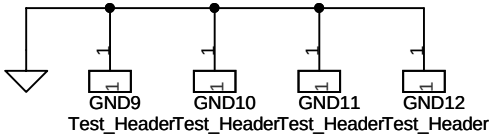
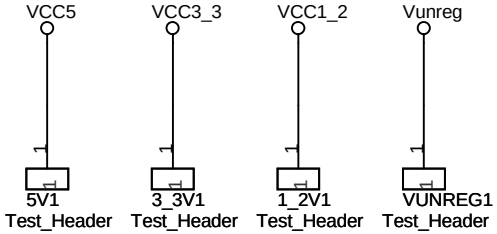
Altera Corp 110 cooper Street, Suite 201, Santa Cruz, CA 95060		
Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

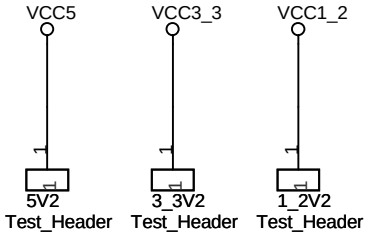
Reset and Test headers

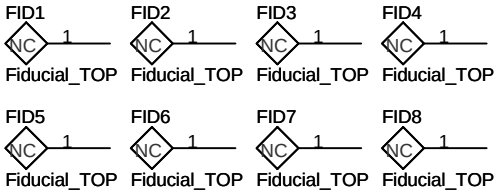


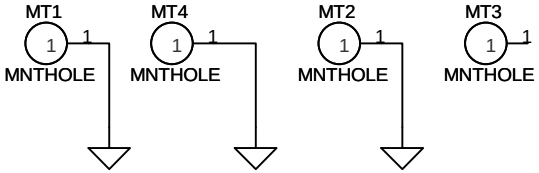


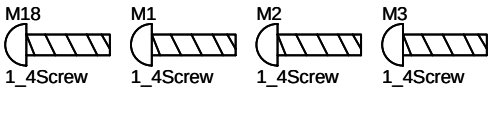


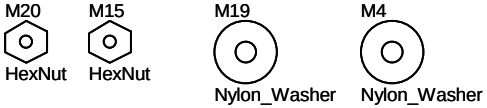


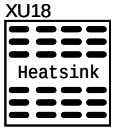


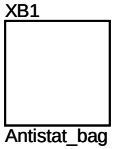


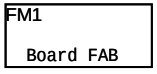












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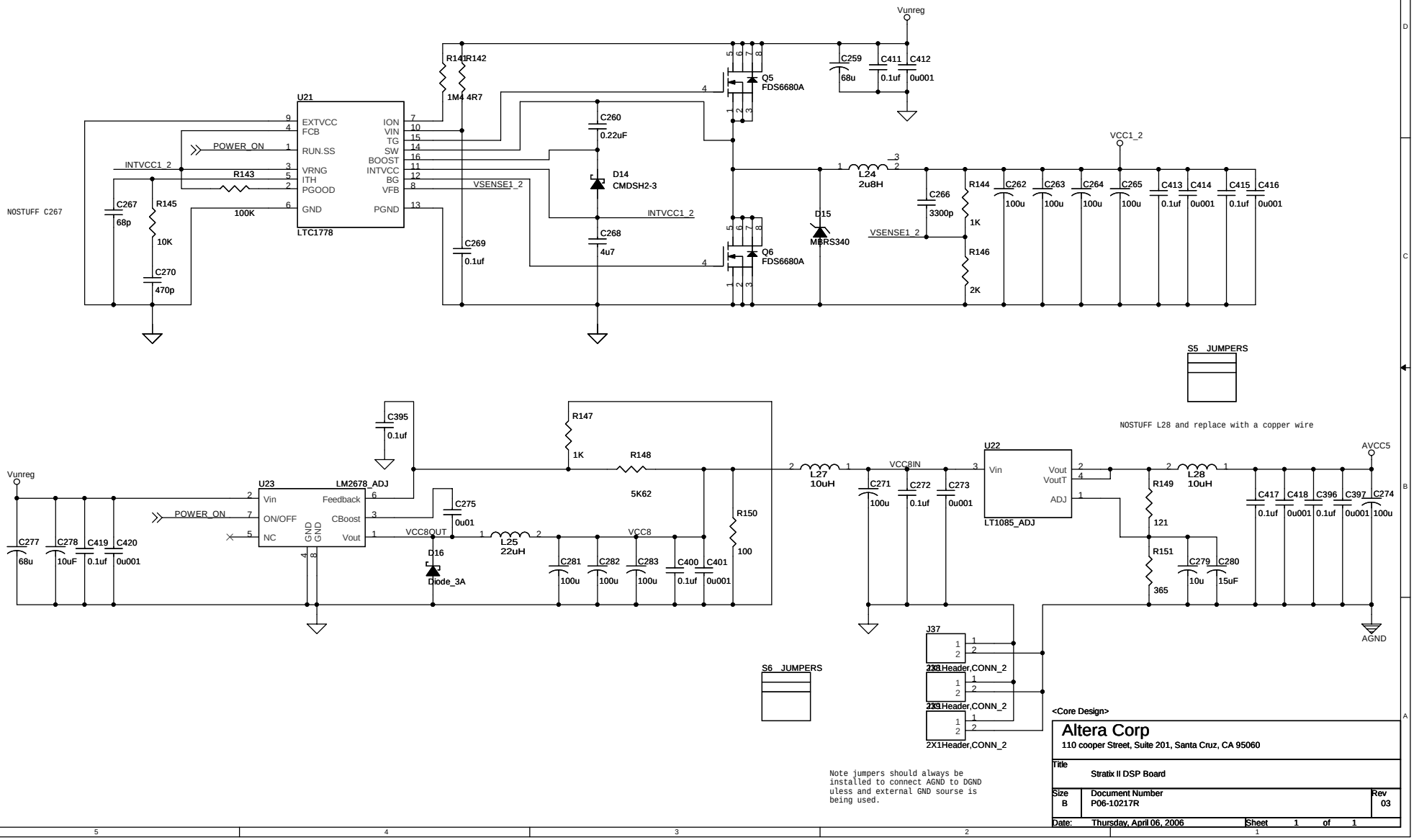
Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Power Connector



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Altera Corp
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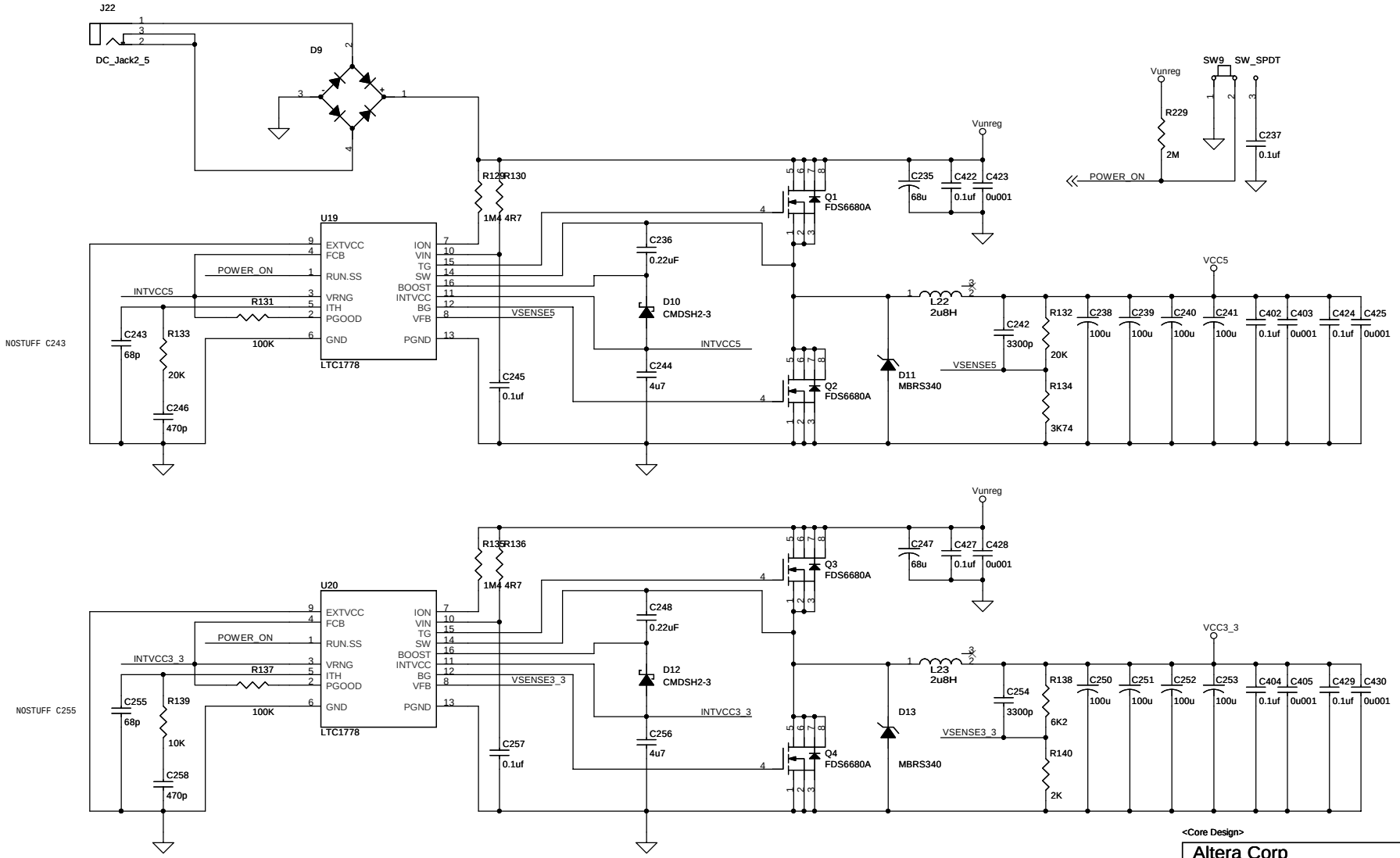
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Power 5V and 3.3V



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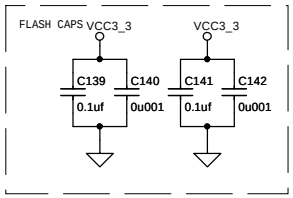
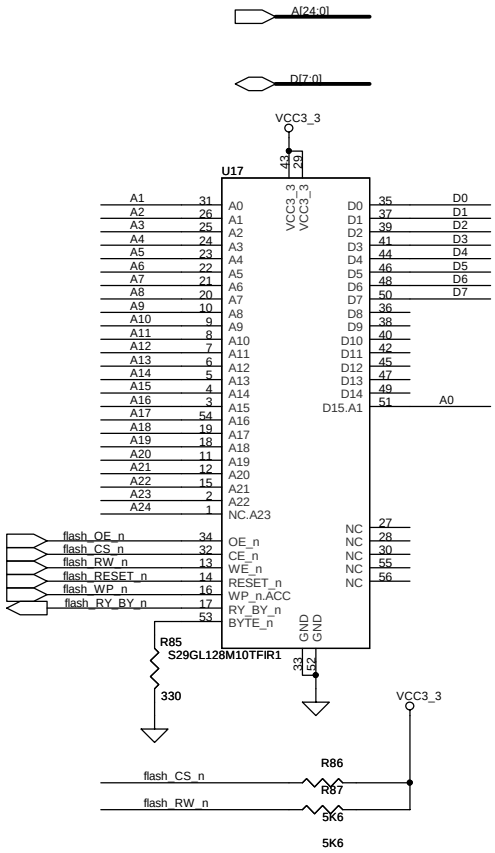
Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	





Flash chip is 16M x 8 for
16Mbytes of flash

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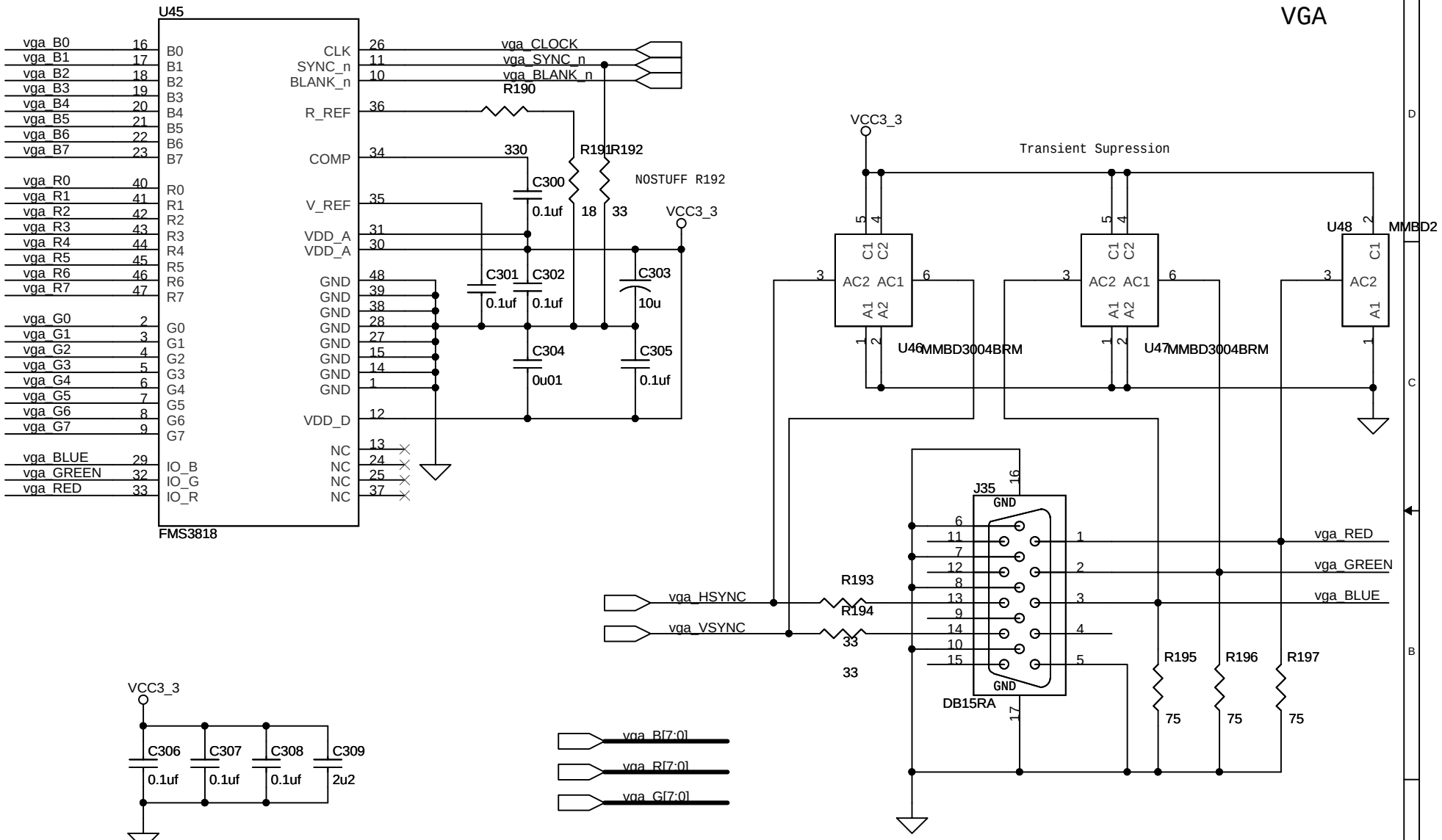
Altera Corp 110 cooper Street, Suite 201, Santa Cruz, CA 95060	
Title: Stratix II DSP Board	
Size: Custom	Document Number: P06-10217R — Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1

VGA



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Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

ADI Connector

adi_D[33:0]

J5

AD6645.9433.9430

2	GND	VCC.GND.GND	1	
4	GND	B13.BOR.NC	3	adi_D0
6	GND	B12.NC.DRX	5	adi_D1
8	GND	B11.NC.DXB	7	adi_D2
10	GND	B10.NC.DXA	9	adi_D3
12	GND	B9.B0.DX0	11	adi_D4
14	GND	B8.B1.DX1	13	adi_D5
16	GND	B7.B2.DX2	15	adi_D6
18	GND	B6.B3.DX3	17	adi_D7
20	GND	* .B4.DX4	19	adi_D8
22	GND	* .B5.DX5	21	adi_D9
24	GND	B5.B6.DX6	23	adi_D10
26	GND	B4.B7.DX7	25	adi_D11
28	GND	B3.B8.DX8	27	adi_D12
30	GND	B2.B9.DX9	29	adi_D13
32	GND	B1.B10.DX10	31	adi_D14
34	GND	B0.B11.DX11	33	adi_D15
36	GND	GND.GND.GND	35	
38	GND	GND.DR.DRA	37	adi_D16
40	GND	GND.GND.GND	39	

20X2Header

J6

AD6645.9433.9430

2	GND	VCC.GND.GND	1	
4	GND	B13.BOR.NC	3	adi_D17
6	GND	B12.NC.DRY	5	adi_D18
8	GND	B11.NC.DYB	7	adi_D19
10	GND	B10.NC.DYA	9	adi_D20
12	GND	B9.B0.DY0	11	adi_D21
14	GND	B8.B1.DY1	13	adi_D22
16	GND	B7.B2.DY2	15	adi_D23
18	GND	B6.B3.DY3	17	adi_D24
20	GND	* .B4.DY4	19	adi_D25
22	GND	* .B5.DY5	21	adi_D26
24	GND	B5.B6.DY6	23	adi_D27
26	GND	B4.B7.DY7	25	adi_D28
28	GND	B3.B8.DY8	27	adi_D29
30	GND	B2.B9.DY9	29	adi_D30
32	GND	B1.B10. DY10	31	adi_D31
34	GND	B0.B11.DY11	33	adi_D32
36	GND	GND.GND.GND	35	
38	GND	GND.DR.DRB	37	adi_D33
40	GND	GND.GND.GND	39	

20X2Header

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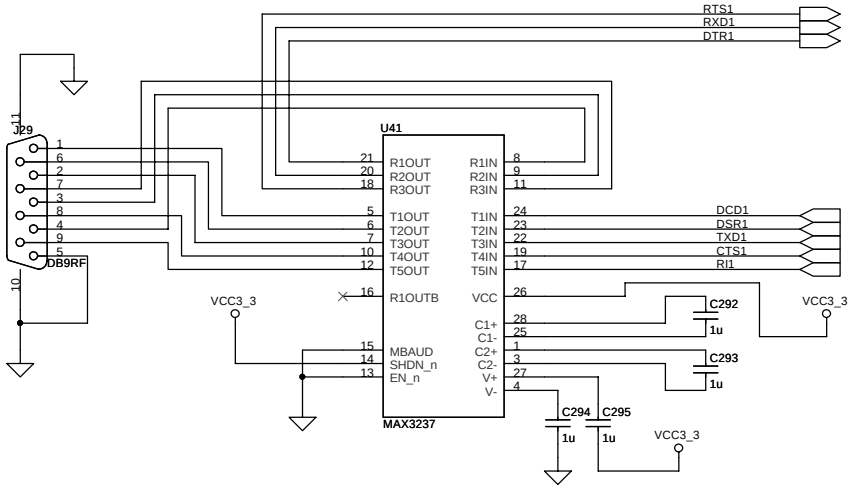
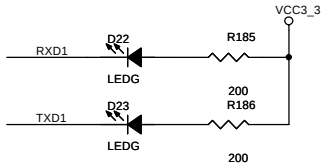
Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

Serial Ports





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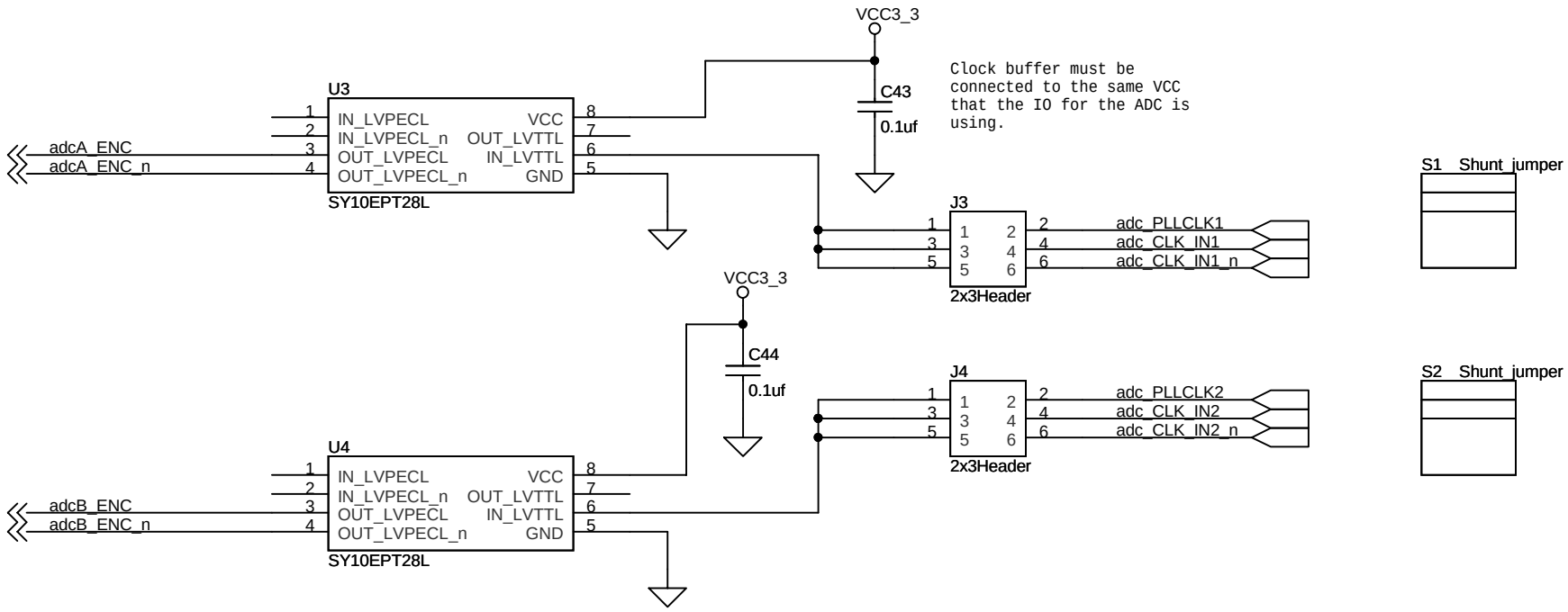
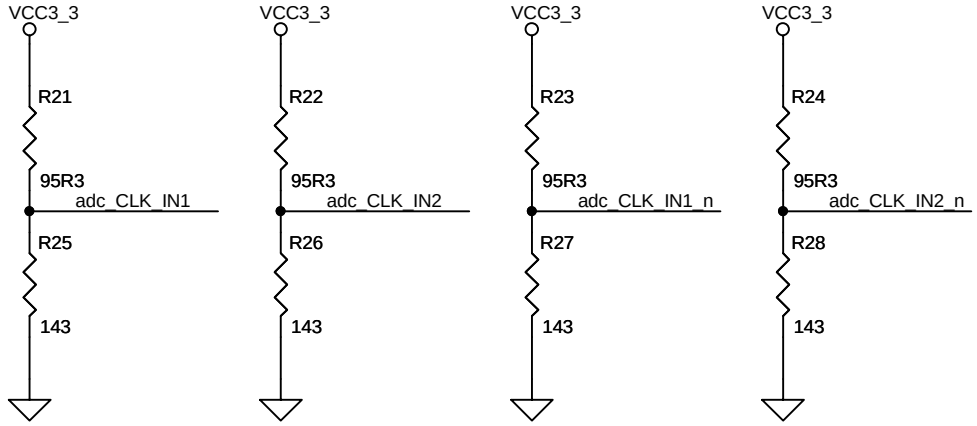
Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

ADC Clock Selection





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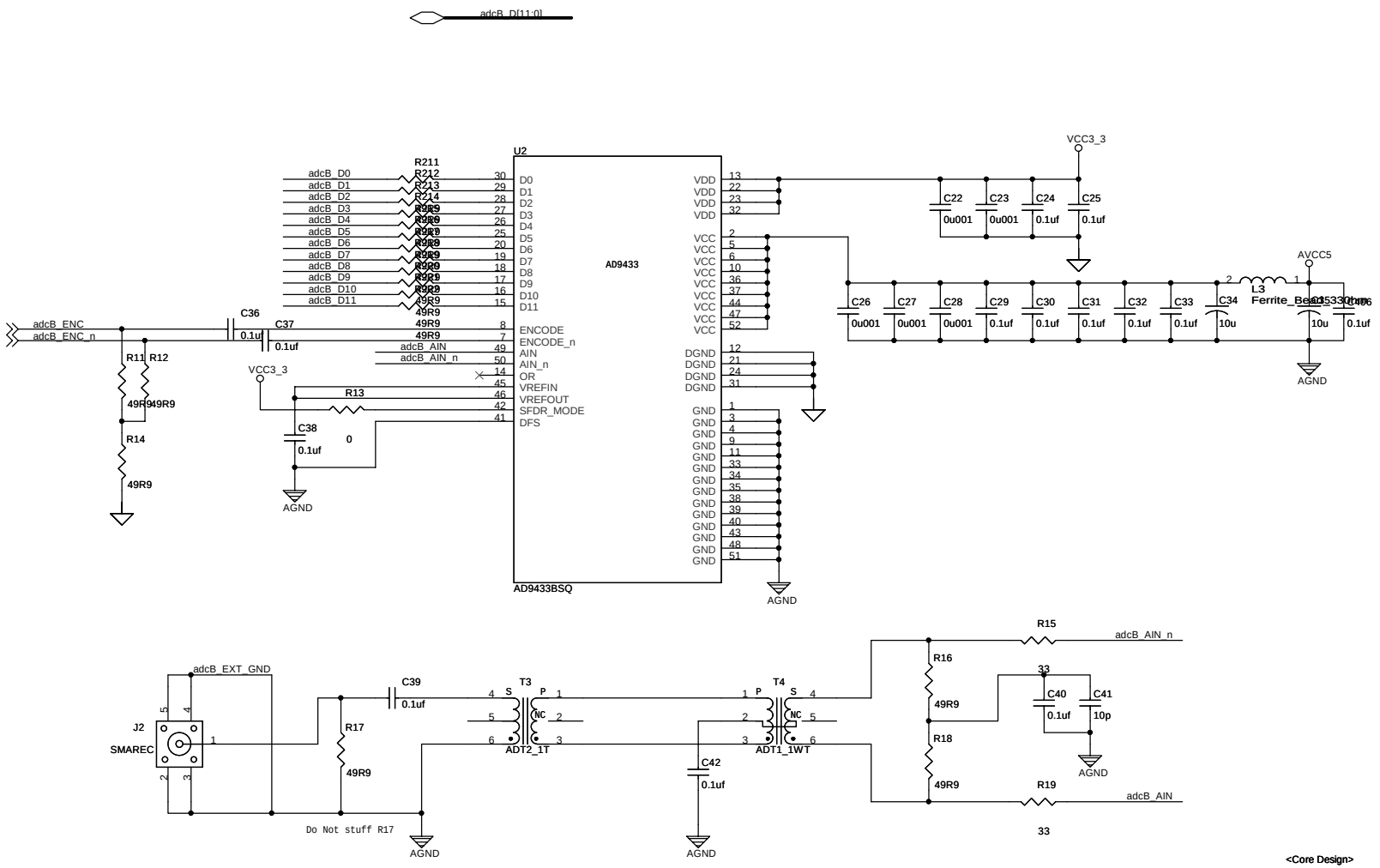
Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: A	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

ADC B



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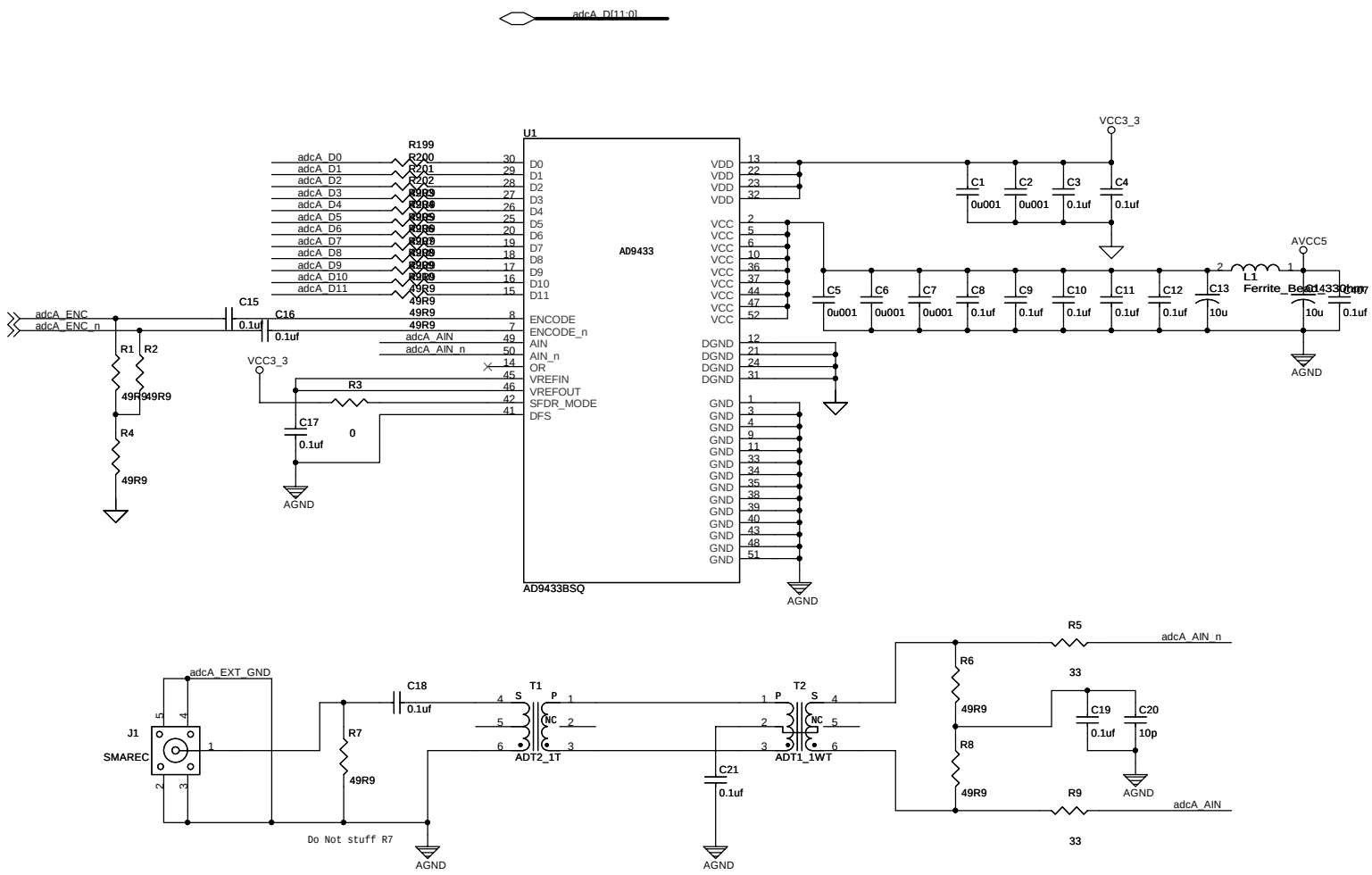
Altera Corp 110 cooper Street, Suite 201, Santa Cruz, CA 95060		
Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	

ADC A



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Altera Corp
110 cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Stratix II DSP Board		
Size: B	Document Number: P06-10217R	Rev: 03
Date: Thursday, April 06, 2006	Sheet 1 of 1	