The Programmable Solutions Company®

Stratix Memory Board 1

PCB Layout Guidelines
Rev 0.5

High Speed / End Applications
Tuesday, June 01, 2004

REVISION HISTORY

DATE	REV	Comments
11/25/2003	1.0	Released document

TABLE OF CONTENTS

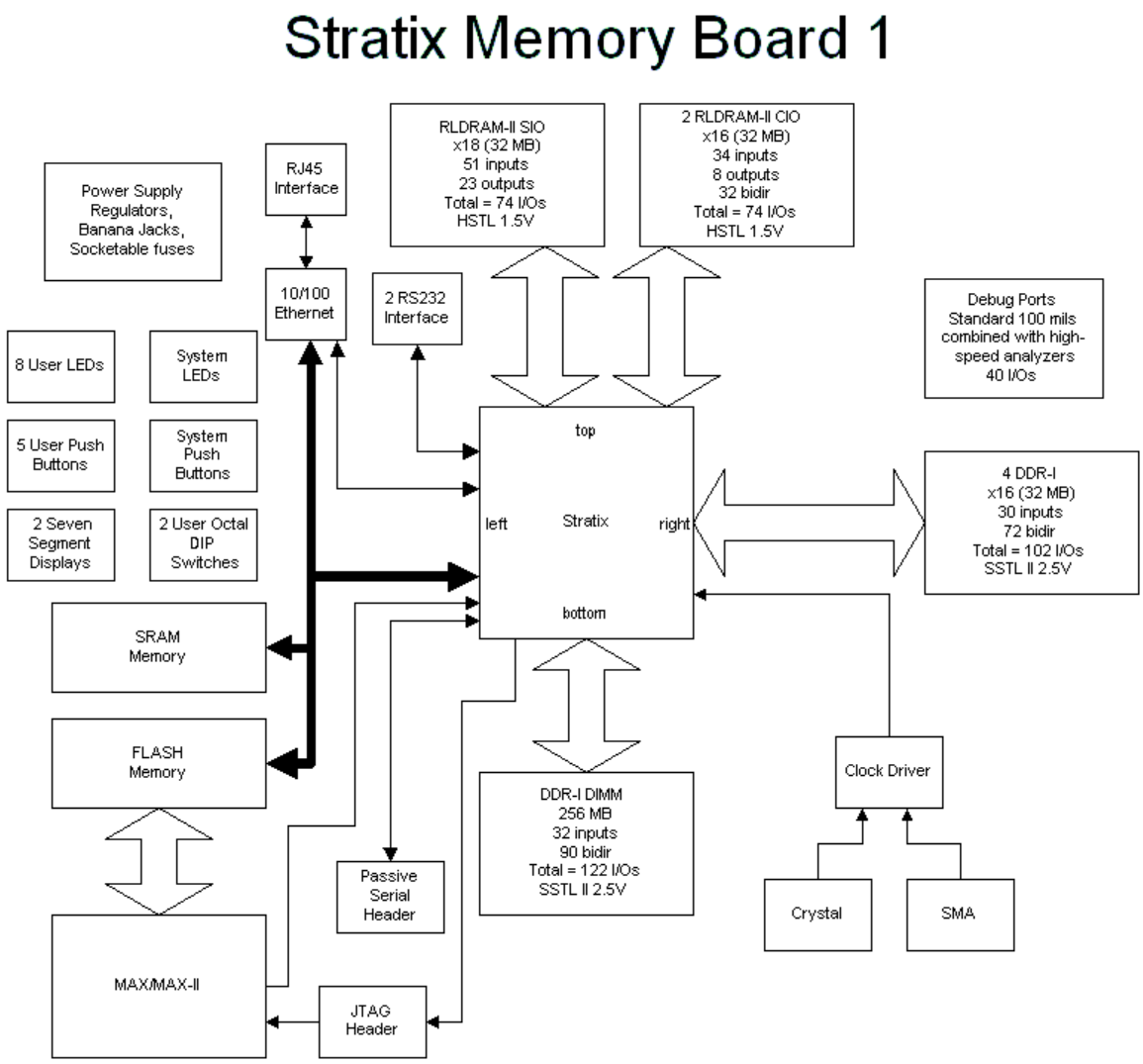


Figure I: Stratix Memory Board 1-Level Block Diagram

1 Form Factor

This board is stand-alone.

PCB Height: 8.0”
PCB Length: 9.0”

Thickness:	0.062”
Maximum Layers:	12
Board Material:	FR4
Impedance:	50 Ohm single-ended, 100 Ohm differential

2 Connectors, Switches, and Edge Components

2.1 DDR DIMM-184 Connector (XU1)

This 184-pin DDR DIMM Connector is a through hole connector that has a socket for DDR memory modules. The module is another board that inserts vertically to this PCB and contains memory chips on both top and bottom of it. The placement of the DIMM connector should be close to the Stratix device to accommodate the matched length requirements for the interfaced signals. Please follow Micron DDR routing guidelines document for details.

2.2 DB-9 RS-232 Edge Connectors (J12)

The dual RS-232 DB-9 connector should hang off of the PCB. The layout design in Allegro shows this placement.

Mounting holes are also required for each connector (sized per connector datasheet recommendations).

2.3 RJ-45 Ethernet Connector (RJ1)

The Ethernet RJ-45 connector assembly has surface-mount pins, through-hole pins, as well as two larger plastic mounting posts that require mounting holes as well.

The connector shall be mounted such that it protrudes slightly from the board edge. It should be placed close to the 10/100 Ethernet MAC/PHY device (U6). The signal names ENET* should be matched as close as possible.

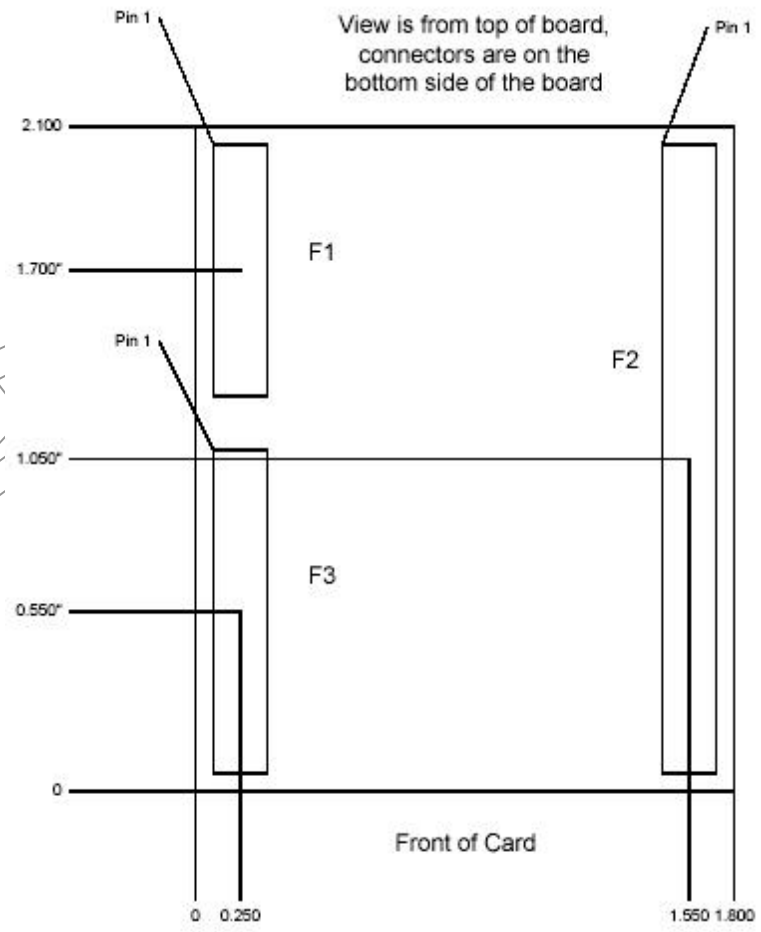
2.4 ByteBlaster JTAG Configuration Headers (J27)

The 10-pin ByteBlaster Header is made up of a right-angle keyed 2x5 100-mil through-hole header. It should be located on a board edge.

2.5 Altera 3.3V Proto1 Daughtercard Headers (J31, J32, J37)

The 3.3V Proto1 daughtercard headers are made up of three 100-mil headers. These are arranged in two columns. The two columns are made up of one combination of J32 a 2X7 header and J31 a 2X10 header. The other header J37 is made up of a single 2X20 header. These headers are surface mount headers that have a 100 mil pin pitch.

These headers are to be placed according to the *placement guidelines drawing* where J32 is F1, J31 is F3, and J37 is F2. Relative placement is according to the drawing below. The dimensions of the placement are detailed as well.



The dimension are shown in inches

Figure II: Proto1 Daughtercard Dimensions

3 Construction

The Stratix Memory board 1 is constructed using standard FR4 material. All vias on the board are through hole and are not blind or buried. The Stratix Memory board 1 utilizes dual stripline in its stack up, but signals on the adjacent layers are orthogonal to each other. All signals should avoid crossing split power planes on the adjacent layers as much as possible.

3.1 Geometries

3.1.1 Trace Geometries

For all dual-stripline layers power-signal-signal-power (P-S-S-P), ensure that the traces on the first signal layer are routed orthogonal to the traces on the second signal layer.

Signals should try to avoid crossing over split power planes on the adjacent layer. This may not be possible so it is recommended that this be minimized for the critical traces.

All unused via pads need to be removed from the board. Leaving the unused via pads in adds capacitance to the signal which in turn degrades the signal integrity.

Trace geometries are dictated by trace impedance requirements and the components used to deliver these high speed signals to the Stratix device.

General
- 5-mil traces
- 15-mil air gap
- 50-ohms impedance +/-5%

3.1.2 Via Geometries

- Via Masking:
  Component (top-side) vias masked (not exposed)
  Backside vias tinned (exposed for probing)

3.1.3 General routing rules

Angles: 45° or Rounded corners (no right-angles)

3.2 Stackup

3.1.4 Overview

This board will have the following stack up (component side is layer 1 on top). This stack up can be modified to ensure the correct impedances and board thickness is maintained.

1	TOP - SIGNAL (50-ohm)
2	POWER
3	SIGNAL (50-ohm)
4	SIGNAL (50-ohm)
5	GND
6	SIGNAL (50-ohm)
7	SIGNAL (50-ohm)
8	PLL_GND
9	SIGNAL (50-ohm)
10	SIGNAL (50-ohm)
11	POWER
12	BOTTOM - SIGNAL (50-ohm)

Figure III: General Stackup

3.1.5 Power and Ground Planes

Ground Planes
- GND
- PLL_GND

3.1.5.1 Solid Planes

The GND and PLL_GND are solid planes. The other power planes will be split power planes. The ground planes shall be tied together using multiple ferrite beads.

3.1.5.2 Power Nets

Power nets can be run on signal layers as needed. A **15-mil routing keepout** shall be associated around **ALL power nets** with respect to signal traces and other features. This is not possible underneath the BGA but do NOT "snake" a power net and a signal trace through the same via gaps as a pair.

The power nets can be embedded in the other Power and GND planes as makes sense in the design phase so long as no signals cross the gap or runs directly above it. If some signal **absolutely** must cross the gaps then we must go back and add a 0.01uF cap for every 4 nets that cross the plane gap to provide an AC return path for switching signals. This is not necessary for switches, LEDs, or push-button nets.

3.1.5.2.1 Switching Power Supply Layout

When laying out the Stratix Memory board 1 follow one of the two suggested approaches. The simple board layout requires a dedicated ground plane layer. Also, for higher currents, also use the multilayer board to help with heat sinking power components.

o The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs (Q2, Q3).

o Place CIN (C41, C46, C43), COUT (C34), MOSFETs (Q2, Q3), Diode (D9) and inductor (L4) all in one compact area. It may help to have some components on the bottom side of the board.

o Place LTC1778 chip with pins 9 to 16 facing the power components (Q2, and Q3). Keep the components connected to pins 1 to 8 close to LTC1778 (noise sensitive components).

o Use an immediate via to connect the components to ground plane including SGND and PGND of LTC1778. Use several bigger vias for power components.

o Use compact plane for switch node (3.3V_SOURCE) to improve cooling of the MOSFETs and to keep EMI down.

o Use planes for PWR_IN and 3.3V_OUT to maintain good voltage filtering and to keep power losses low.

o Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (PWR_IN, 3.3V_OUT, GND or to any other DC rail in your system).

3.1.5.2.2 Routing Requirements for All Power Regulators

Each regulator draws a calculated amount of current. A worst-case scenario was calculated and the minimum trace width has been associated for the power regulators shown in the table below.

Voltage	Function	Net Name	Reference Designator	Power	current	oz. per ft	internal	external	oz. per ft	internal	external
+16.0V	Input Power	PWR_IN	J3,U5,Q1	60W	3.75	1	243	70	0.5	486	140
+3.3V	VCCIO	3.3V_S_IO	U5,Q1,Q2,L9,F3,L7	11.6W	4.3	1	293	86	0.5	585	172
	VCC	3.3V	U5,Q1,Q2,L9,F4,L8		5	1	359	108	0.5	718	215
	VCC_PLL	3.3V_PLL	U5,Q1,Q2,L9,F5,L10		1	1	41	10	0.5	81	20
+1.5V	VCCINT	1.5V_INT	U39,F10	1.5W	2	1	104	28	0.5	207	55
	VCCPLL	1.5V_PLL	U38,F9	1.5W	1	1	41	10	0.5	81	20
+2.6V/+1.8V	VDD+Vtt	2.6V_TERM	U6,F8,L13	5.6W	2.16	1	115	31	0.5	230	62
	VCCIO	VCC_S_IO	U6,F7,L12	8.7W	3.4	1	213	61	0.5	425	121
		VCC_IO_RLDRAM	U6,Q3,F6,L11	3.2W	2	1	104	28	0.5	207	55
+1.25V	Vtt	VTT		1.25W	1						
+2.5V	Vext	2.5V	U9,F12	7.5W	3	1	180	51	0.5	359	101
+1.8V	VDD	1.8V	U8,F11	1.8W	1	1	41	10	0.5	81	20
+1.5V	VDDQ			1.5W	1						
+0.75V	Vtt	VTT	U1,F1	1.5W	2	1	104	28	0.5	207	55

4 Critical Traces

4.1 Stratix Signals (U20)

Match the following in length:
FSE_*
FLASH_*

Match the following in length:
PROTO1_IO*[40..0]

Match the following in length:
RS232A_*
RS232B_*

Match the following in length:
ENET_*

Match the following in length:
SRAM_*

Match the following in length:
MAX_LED*

Match the following in length:
PB*

4.2 DDR SDRAM Signals

These high-speed DDR SDRAM signals are single-ended signals. There are four termination schemes used to terminate the DDR devices and two schemes for the DDR DIMM. These termination schemes are shown in the figure below. Our **target impedance** for ALL signals in this interface should be **50-ohms**. The termination scheme shows a series damping resistor RS and a fly-by pull-up resistor to VTT.

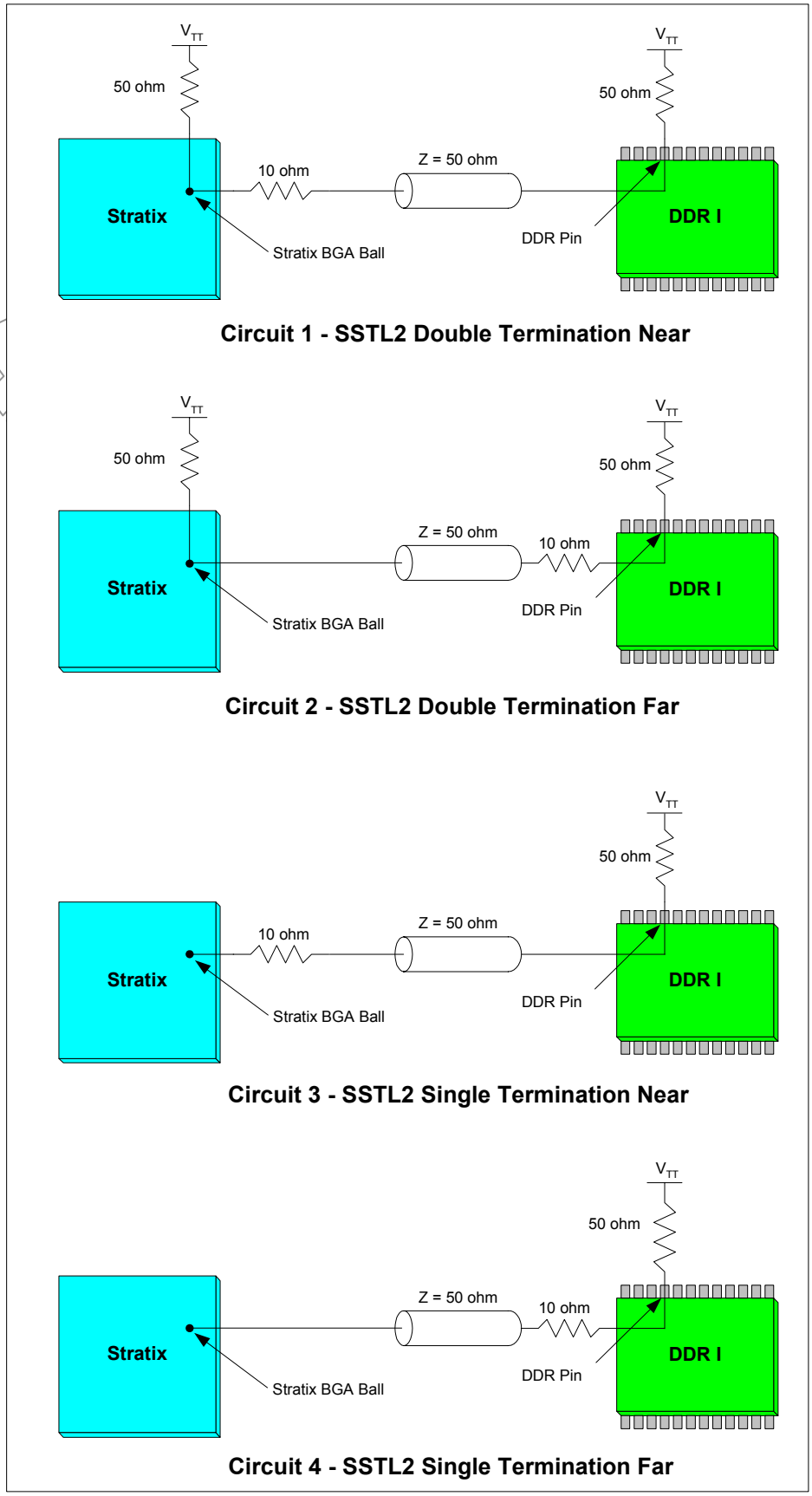

V_{TT}
50 ohm
10 ohm
Z = 50 ohm
Stratix
Stratix BGA Ball
DDR Pin
DDR I
Circuit 1 - SSTL2 Double Termination Near
Circuit 2 - SSTL2 Double Termination Far
Circuit 3 - SSTL2 Single Termination Near
Circuit 4 - SSTL2 Single Termination Far

Figure IV: SSTL-2 Termination

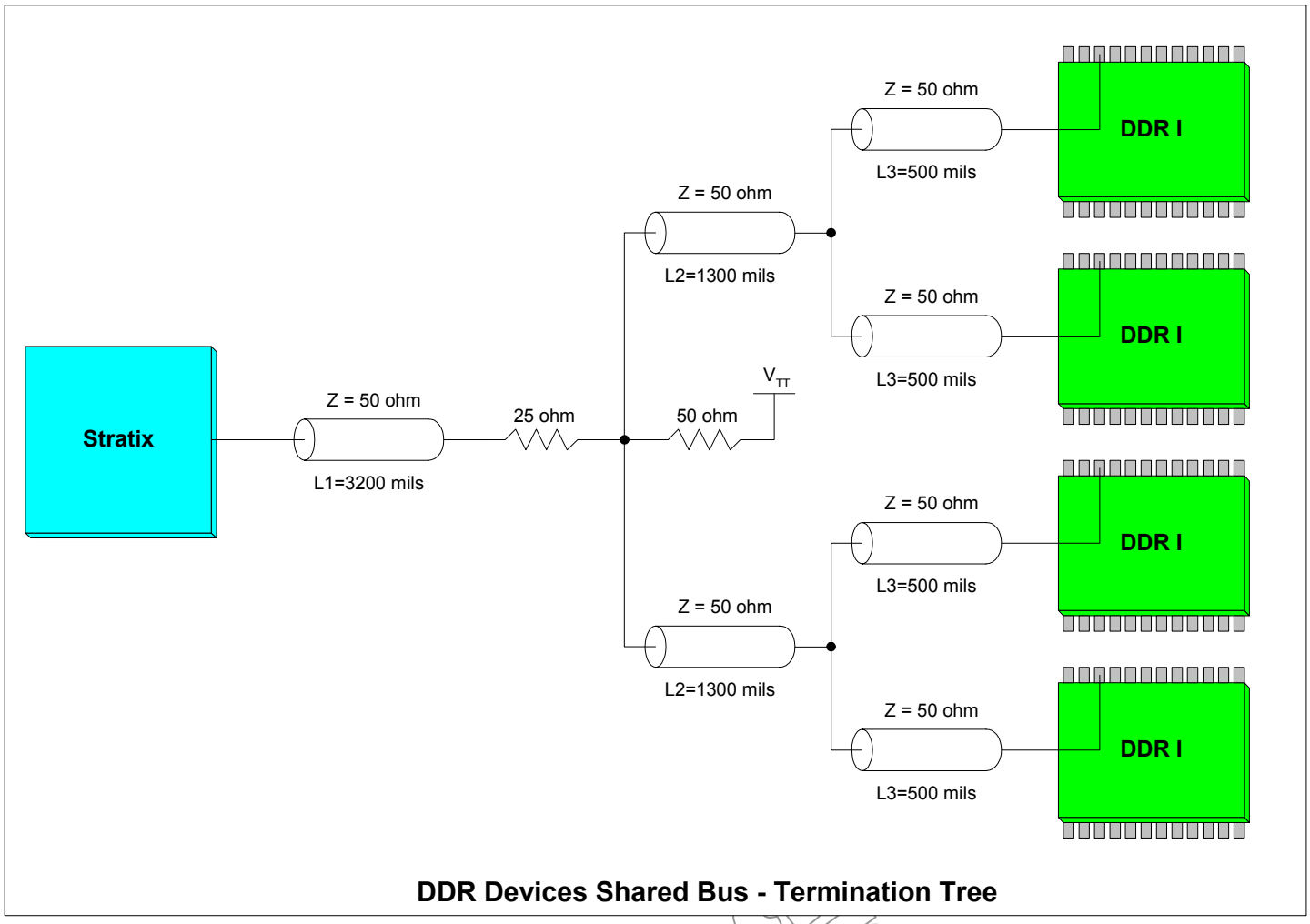


Figure V: SSTL-2 DDR Shared Termination

DDR I SDRAM DIMM interface signals:

Function	Stratix-side Net	DIMM-side Net	Termination Circuit
Data	DDRE_DQ[63:0]	DDRE_DATAQ[63:0]	Circuit 4
Check Bit	DDRE_CB[7:0]	DDRE_CKB[7:0]	Circuit 4
Data Mask	DDRE_DM[8:0]	DDRE_DMASK[8:0]	Circuit 4
Data Strobe	DDRE_DQS[8:0]	DDRE_STROBE[8:0]	Circuit 4
Address	DDRE_A[12:0]	DDRE_ADR[12:0]	Circuit 3
Bank Address	DDRE_BA[1:0]	DDRE_BANK[1:0]	Circuit 3
Row Command	DDRE_RASn	DDRE_ROWn	Circuit 3
Column Command	DDRE_CASn	DDRE_COLn	Circuit 3

Write Command	DDRE_WEn	DDRE_WRITEn	Circuit 3
Chip Select	DDRE_CSn	DDRE_SELn	Circuit 3
Clock Enable	DDRE_CKE	DDRE_CLKE	Circuit 3
Clock Enable1	DDRE_CKE1	DDRE_CLKE1	Circuit 3

Diff. Clocks = DDRE_CK_P0/N0, DDRE_CK_P1/N1, DDRE_CK_P2/N2

DDR I DIMM "Byte Lane Groups":
Data signals are grouped with their associated strobe and mask bit. These grouping of bits are called a "Byte Lane" and are routed such that an individual Byte Lane must have matched lengths within the 10 bits. However, each Byte Lane may vary in length from one another by +/- 0.25 inches. The bits that make up each Byte Lane are shown below.

Lane 0 = DDRE_DQ[7:0]	**DDRE_DATAQ[7:0]**	**DDRE_DM[0]**	**DDRE_DMASK[0]**	**DDRE_DQS[0]**	**DDRE_STROBE[0]**
Lane 1 = DDRE_DQ[15:8]	**DDRE_DATAQ[15:8]**	**DDRE_DM[1]**	**DDRE_DMASK[1]**	**DDRE_DQS[1]**	**DDRE_STROBE[1]**
Lane 2 = DDRE_DQ[23:16]	**DDRE_DATAQ[23:16]**	**DDRE_DM[2]**	**DDRE_DMASK[2]**	**DDRE_DQS[2]**	**DDRE_STROBE[2]**
Lane 3 = DDRE_DQ[31:24]	**DDRE_DATAQ[31:24]**	**DDRE_DM[3]**	**DDRE_DMASK[3]**	**DDRE_DQS[3]**	**DDRE_STROBE[3]**
Lane 4 = DDRE_DQ[39:32]	**DDRE_DATAQ[39:32]**	**DDRE_DM[4]**	**DDRE_DMASK[4]**	**DDRE_DQS[4]**	**DDRE_STROBE[4]**
Lane 5 = DDRE_DQ[47:40]	**DDRE_DATAQ[47:40]**	**DDRE_DM[5]**	**DDRE_DMASK[5]**	**DDRE_DQS[5]**	**DDRE_STROBE[5]**
Lane 6 = DDRE_DQ[55:48]	**DDRE_DATAQ[55:48]**	**DDRE_DM[6]**	**DDRE_DMASK[6]**	**DDRE_DQS[6]**	**DDRE_STROBE[6]**
Lane 7 = DDRE_DQ[63:56]	**DDRE_DATAQ[63:56]**	**DDRE_DM[7]**	**DDRE_DMASK[7]**	**DDRE_DQS[7]**	**DDRE_STROBE[7]**
Lane 8 = DDRE_CB[7:0]	**DDRE_CKB[7:0]**	**DDRE_DM[8]**	**DDRE_DMASK[8]**	**DDRE_DQS[8]**	**DDRE_STROBE[8]**

Routing Rules

1. All signals within a given "Byte Lane Group" should be matched length from the pin on FBGA U20 to the pin on DDR connector XU1. Maximum deviation is +/- 0.050 inches.
2. Keep the distance from the pin on XU1 to the termination resistor pack (to 1.25V) to less than 1.25 inches. This puts the length for the entire net up to <match_length_rule1> + <termination_max_length_rule2>.
3. All signals must match lengths between pins (as in (1) above) within +/- 0.250 inches (address, control, data, all byte groups, etc…). Only nets within a byte lane group must be matched tighter as in rule 1.
4. All signals (other than address) are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
   a. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
   b. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
   c. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
5. All DDR SDRAM signals are to maintain 25 mil separation from other
6. Total net length from the Stratix to the VTT termination resistor must not exceed 6 inches.
7. DDR Address lines DDRE_A[12:0] and DDRE_ADR[12:0] should maintain a spacing that is based on its parallelism with other nets but more stringent than in rule 4a/b/c above. This is as follows:
   a. 10 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
   b. 15 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
   c. 20 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
8. DDR Clocks in Clocking section

DDR I SDRAM "Device A, B, C, D" interface signals:

Function	Stratix-side Net	DIMM-side Net	Termination Circuit
Device A			
Data	DDRA_DQ[15:0]	DDRA_DATAQ[15:0]	Circuit 1, fly-by
Data Mask	DDRA_LDM, _UDM	DDRA_LDMASK, UDMASK	Circuit 1, fly-by
Data Strobe	DDRA_LDQS, _UDQS	DDRA_LSTROBE, USTROBE	Circuit 1, fly-by
Chip Select	DDRA_CSn	DDRA_SELn	Circuit 3
Clock Enable	DDRA_CKE	DDRA_CLKE	Circuit 3
Device B			

Data	DDRB_DQ[15:0]	DDRB_DATAQ[15:0]	Circuit 2, fly-by
Data Mask	DDRB_LDM, _UDM	DDRB_LDMASK, UDMASK	Circuit 2, fly-by
Data Strobe	DDRB_LDQS, _UDQS	DDRB_LSTROBE, USTROBE	Circuit 2, fly-by
Chip Select	DDRB_CSn	DDRB_SELn	Circuit 3
Clock Enable	DDRB_CKE	DDRB_CLKE	Circuit 3
Device C			
Data	DDRC_DQ[15:0]	DDRC_DATAQ[15:0]	Circuit 1, non-fly-by
Data Mask	DDRC_LDM, _UDM	DDRC_LDMASK, UDMASK	Circuit 1, non-fly-by
Data Strobe	DDRC_LDQS, _UDQS	DDRC_LSTROBE, USTROBE	Circuit 1, non-fly-by
Chip Select	DDRC_CSn	DDRC_SELn	Circuit 3
Clock Enable	DDRC_CKE	DDRC_CLKE	Circuit 3
Device D			
Data	DDRD_DQ[15:0]	DDRD_DATAQ[15:0]	Circuit 2, non-fly-by
Data Mask	DDRD_LDM, _UDM	DDRD_LDMASK, UDMASK	Circuit 2, non-fly-by
Data Strobe	DDRD_LDQS, _UDQS	DDRD_LSTROBE, USTROBE	Circuit 2, non-fly-by
Chip Select	DDRD_CSn	DDRD_SELn	Circuit 3
Clock Enable	DDRD_CKE	DDRD_CLKE	Circuit 3
Shared signals			
Address	DDRA_A[12:0]	DDRA_ADR[12:0]	Circuit DDR Shared
Bank Address	DDRA_BA[1:0]	DDRA_BANK[1:0]	Circuit DDR Shared
Row Command	DDRA_RASn	DDRA_ROWn	Circuit DDR Shared
Column Command	DDRA_CASn	DDRA_COLn	Circuit DDR Shared
Write Command	DDRA_WEn	DDRA_WRITEn	Circuit DDR Shared

Diff. Clocks = DDRA_CK_P/N, DDRE_CK_P1/N1, DDRE_CK_P2/N2

DDR I Device "Byte Lane Groups":
Data signals are grouped with their associated strobe and mask bit. These grouping of bits are called a "Byte Lane" and are routed such that an individual Byte Lane must have matched lengths within the 10 bits. However, each Byte Lane may vary in length from one another by +/- 0.25 inches. The bits that make up each Byte Lane are shown below.

Lane 0 = DDRA_DQ[7:0]	**DDRA_DATAQ[7:0]**	**DDRA_LDM**	**DDRA_LDMASK**	**DDRA_LDQS**	**DDRA_LSTROBE**
Lane 1 = DDRA_DQ[15:8]	**DDRA_DATAQ[15:8]**	**DDRA_UDM**	**DDRA_UDMASK**	**DDRA_UDQS**	**DDRA_USTROBE**
Lane 2 = DDRB_DQ[7:0]	**DDRB_DATAQ[7:0]**	**DDRB_LDM**	**DDRB_LDMASK**	**DDRB_LDQS**	**DDRB_LSTROBE**
Lane 3 = DDRB_DQ[15:8]	**DDRB_DATAQ[15:8]**	**DDRB_UDM**	**DDRB_UDMASK**	**DDRB_UDQS**	**DDRB_USTROBE**
Lane 4 = DDRC_DQ[7:0]	**DDRC_DATAQ[7:0]**	**DDRC_LDM**	**DDRC_LDMASK**	**DDRC_LDQS**	**DDRC_LSTROBE**
Lane 5 = DDRC_DQ[15:8]	**DDRC_DATAQ[15:8]**	**DDRC_UDM**	**DDRC_UDMASK**	**DDRC_UDQS**	**DDRC_USTROBE**
Lane 6 = DDRD_DQ[7:0]	**DDRD_DATAQ[7:0]**	**DDRD_LDM**	**DDRD_LDMASK**	**DDRD_LDQS**	**DDRD_LSTROBE**
Lane 7 = DDRD_DQ[15:8]	**DDRD_DATAQ[15:8]**	**DDRD_UDM**	**DDRD_UDMASK**	**DDRD_UDQS**	**DDRD_USTROBE**

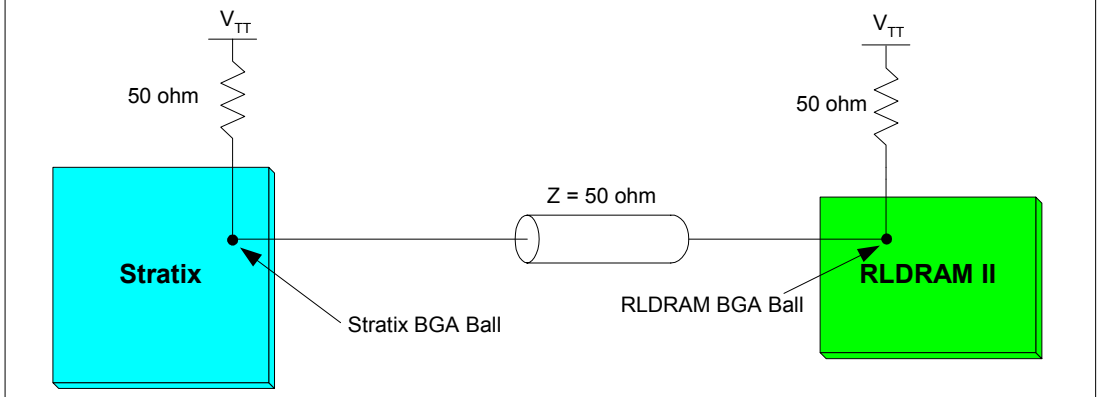
Routing Rules

9. All signals within a given "Byte Lane Group" should be matched length from the pin on FBGA U20 to the pin on DDR devices U15, U17, and U22. Maximum deviation is +/- 0.050 inches. Distance from U20 to U24 needs to be 1 inch longer.
10. Keep the distance from the pin on DDR devices U15, U17, and U22to the termination resistor pack (to 1.25V) to less than 1.25 inches. This puts the length for the entire net up to <match_length_rule1> + <termination_max_length_rule2>.
11. All signals must match lengths between pins (as in (9) above) within +/- 0.250 inches (address, control, data, all byte groups, etc…) Only nets within a byte lane group must be matched tighter as in rule 9.

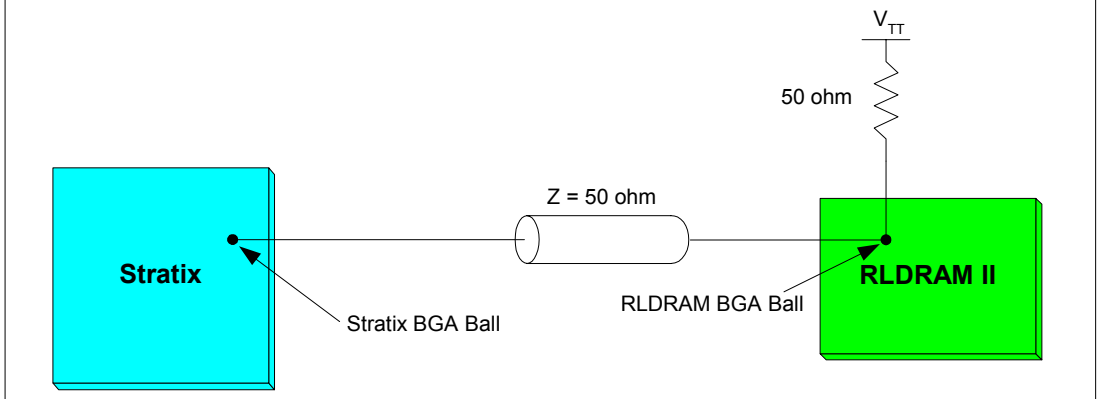
12. All signals (other than address) are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
    a. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
13. All DDR SDRAM signals are to maintain 25 mil separation from other
14. Total net length from the Stratix to the VTT termination resistor must not exceed 6 inches.
15. DDR Address lines DDRA_A[12:0] and DDRA_ADR[12:0] should maintain a spacing that is based on its parallelism with other nets but more stringent than in rule 12a/b/c above. This is as follows:
    a. 10 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 15 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 20 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
16. DDR Clocks in Clocking section

4.3 RLDRAM SDRAM Signals

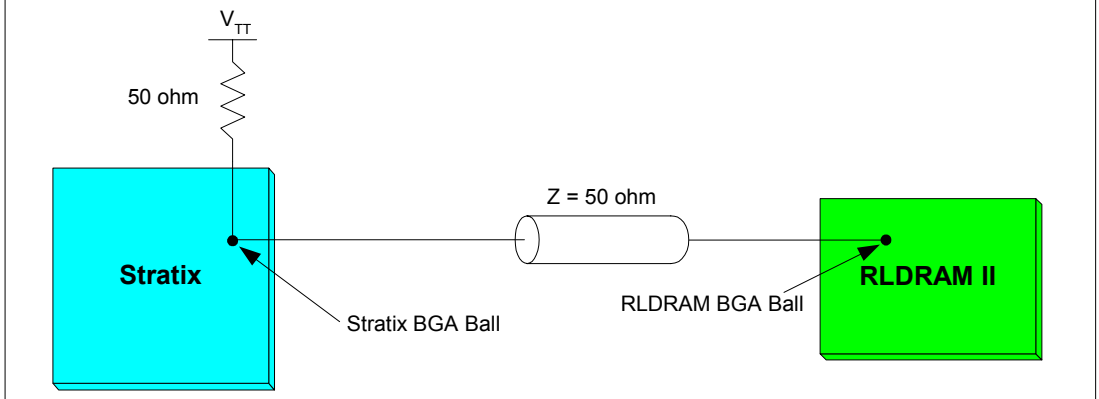
These high-speed RLDRAM SDRAM signals are single-ended signals. There are three termination schemes used to terminate the RLDRAM devices. These termination schemes are shown in the figure below. Our **target impedance** for ALL signals in this interface should be **50-ohms**. The termination scheme shows a fly-by pull-up resistor to VTT.



Circuit 5 - HSTL2 Double Termination



Circuit 6 - HSTL2 Single Termination Far



Circuit 7 - HSTL2 Single Termination Near

Figure VI: HSTL-2 Termination

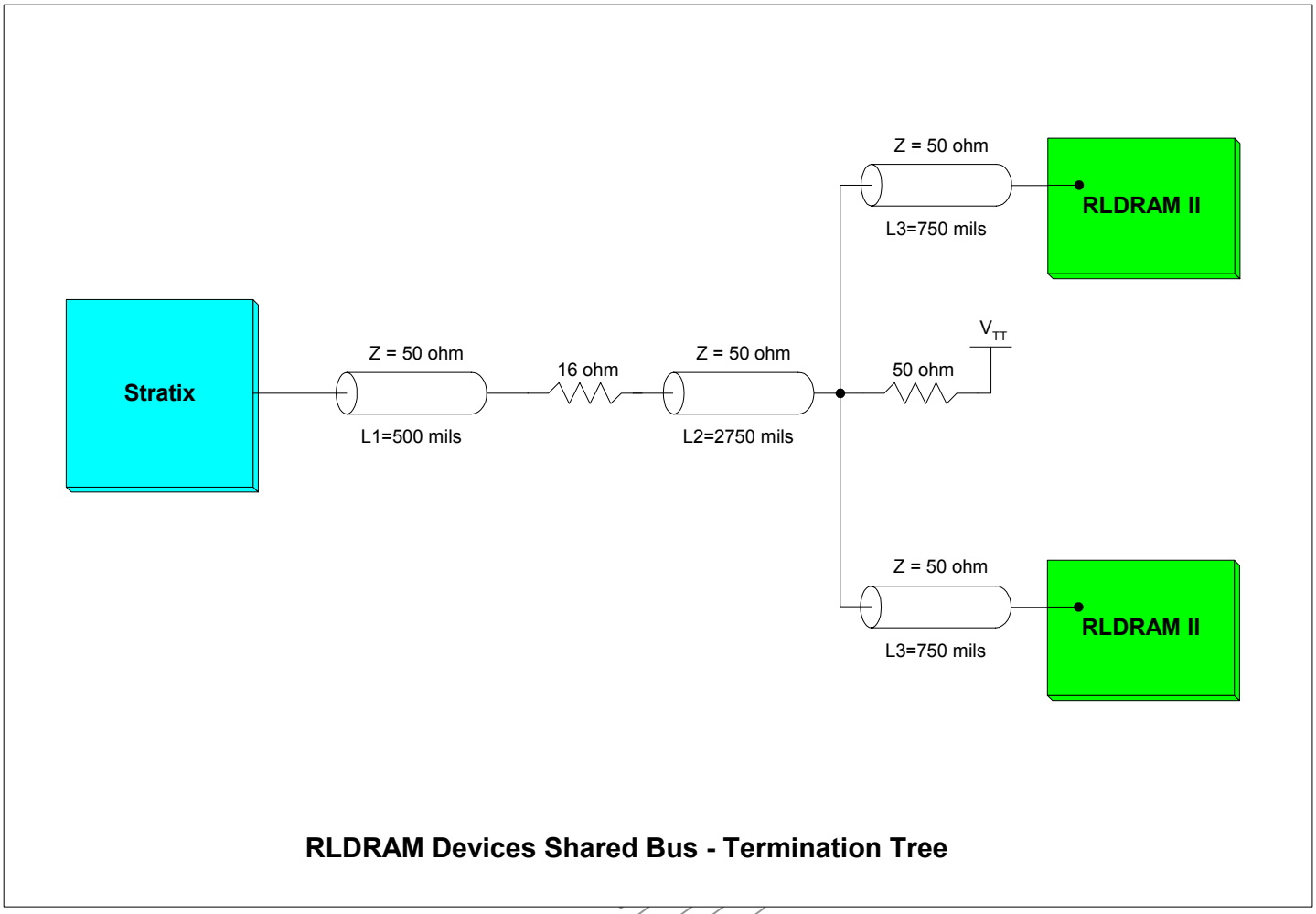


Figure VII: HSTL-2 RLDC Shared Termination

RLDRAM II SDRAM interface signals:

Function	Net	Termination Circuit
RLDRAM SIO		
Data (Read)	RLDS_Q[17:0]	Circuit 7
Data (Write) Mask	RLDS_DM	Circuit 6
Data (Read) Valid	RLDS_QVLD	Circuit 7
Data (Read) Clock	RLDS_QK_P[1:0], _N[1:0]	Differential RLDS
Data (Write)	RLDS_D[17:0]	Circuit 6
Data (Write) Clock	RLDS_CK_P, _N	Differential RLDS
Address	RLDS_A[22:0]	Circuit 6
Bank Address	RLDS_BA[2:0]	Circuit 6
Ref Command	RLDS_REFn	Circuit 6
Write Command	RLDS_WEn	Circuit 6
Chip Select	RLDS_CSn	Circuit 6
RLDRAM CIO 1		
Data	RLDC_DQ[15:0]	Circuit 5
Data Mask	RLDC_DM	Circuit 5

Data Valid	RLDC_QVLD	Circuit 7
Data Clock	RLDC_QK_P[1:0], _N[1:0]	Differential RLDC
Chip Select	RLDC_CSn	Circuit 6
RLDRAM CIO 2		
Data	RLDC2_DQ[15:0]	Circuit 5
Data Mask	RLDC2_DM	Circuit 5
Data Valid	RLDC2_QVLD	Circuit 7
Data Clock	RLDC2_QK_P[1:0], _N[1:0]	Differential RLDC
Chip Select	RLDC2_CSn	Circuit 6
Shared CIO signals		
Address	RLDC_A[12:0]	Circuit RLDC Shared
Bank Address	RLDC_BA[2:0]	Circuit RLDC Shared
Ref Command	RLDC_REFn	Circuit RLDC Shared
Write Command	RLDC_WEn	Circuit RLDC Shared

RLDRAM II Device "Byte Lane Groups":
Data signals are grouped with their associated strobe and mask bit. These grouping of bits are called a "Byte Lane" and are routed such that an individual Byte Lane must have matched lengths within the 10 bits. However, each Byte Lane may vary in length from one another by +/- 0.25 inches. The bits that make up each Byte Lane are shown below.

Lane 0 SIO (Read) = RLDS_Q[8:0] RLDS_QVLD RLDS_QK_P0, _N0
Lane 0 SIO (Write) = RLDS_D[8:0] RLDS_DM RLDS_CK_P, _N
Lane 1 SIO (Read) = RLDS_Q[17:9] RLDS_QK_P1, _N1
Lane 1 SIO (Read) = RLDS_D[17:9]

Lane 0 CIO = RLDC_DQ[8:0] RLDC_DM RLDC_QVLD RLDC_QK_P0, _N0
Lane 1 CIO = RLDC_DQ[17:9] RLDC_QK_P1, _N1
Lane 2 CIO = RLDC2_DQ[8:0] RLDC2_DM RLDC2_QVLD RLDC2_QK_P0, _N0
Lane 3 CIO = RLDC2_DQ[17:9] RLDC2_QK_P1, _N1

Routing Rules

17. All signals within a given "Byte Lane Group" should be matched length from the pin on FBGA U20 to the pin on RLDRAM devices U11, U12, and U13. Maximum deviation is +/- 0.050 inches.
18. Keep the distance from the pin on RLDRAM devices U11, U12, and U13 to the termination resistor pack (to 1.25V) to less than 1.25 inches. This puts the length for the entire net up to <match_length_rule1> + <termination_max_length_rule2>.
19. All signals must match lengths between pins (as in (17) above) within +/- 0.250 inches (address, control, data, all byte groups, etc…). Only nets within a byte lane group must be matched tighter as in rule 17.
20. All signals (other than address) are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
    a. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
21. All RLDRAM SDRAM signals are to maintain 25 mil separation from other
22. Total net length from the Stratix to the VTT termination resistor must not exceed 6 inches.
23. RLDRAM Address lines RLDS_A[22:0], RLDC_A[22:0] should maintain a spacing that is based on its parallelism with other nets but more stringent than in rule 20a/b/c above. This is as follows:
    a. 10 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 15 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 20 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
24. RLDRAM Clocks in Clocking section

4.4 Clocks

- Each clock trace segment should be minimal length (less than 1 inch if possible).
- Total trace length of any one clock trace (all segments) including passive components should be less than 3 inches.
- If a clock net has a series resistor, make sure the resistor is closest to the source.
- For clocks with differential pairs, they should be routed in close proximity throughout the trace length. The trace width should be 5 mils and spacing between the positive and negative traces should be 5 mils. Spacing between these traces and other signals should be a minimum of 30 mils. They should be matched in length.
- Placement should be adjusted to fix these issues.

4.4.1 Stratix Clock Inputs

Oscillators

- J36/Y1/U21 (net = CLKB_OSC_B)
  - Place J36 and Y1 on top of each other.
  - Place U21 close to J36/Y1.
  - Place SMA connector J41 close to U21 and place J36/Y1, U21, and J41 and its associated components close to the Stratix device (U20).
  - Place termination resistors (R42, R45, R46, R196, R205, R207, R208, R212, R216, and R481) near U21.
  - Place TP5 and TP6 close to each other and near R196.
- Y2 (net = CLK_OSC_A)
  - Place U23 and Y2 and its associated components close to the Stratix device (U20), however, net CLK_OSC_B has priority.
  - Place termination resistors (R265 and R268) near U23.
- X1 (net CLK_25MHz)
  - Place near U6 Ethernet chip as this is the only load for this oscillator.

SMA Clock Input

- SMA J41 to route clock to U21 input and then terminate to R206 after route.

SMA_CLK_P, SMA_CLK_N

- Same rules as differential clock.

SMA_FB_P, SMA_FB_N

- Same rules as differential clock.

CLK_FROM_SCRUZ

- No specific routing rules. This is least important of all clock nets and is actually rarely used. Keep R80 close to J31.

CLK1_OUT_S, CLK1_OUT_MAX, SCRUZ_CLK_OSC_A

- No specific routing rules.

CLK2_OUT_S1, CLK2_OUT_S2, CLK2_OUT_MAX, CLK2_OUT_S3, CLK2_OUT_S4

- No specific routing rules.

4.4.2 Stratix Clock Outputs

DDR Module Clocks (U27)

- These clocks should be matched in length within +/- 0.050".
  - DDRE_CK_P0 / DDRE_CK_N0 (differential)
  - DDRE_CK_P1 / DDRE_CK_N1 (differential)
  - DDRE_CK_P2 / DDRE_CK_N2 (differential)
  - DDRE_FBCLK (single-ended)
  - DDRE_DLL_CLK (single-ended)
  - DDRE_SMA_DLL_CLK (single-ended from SMA)
- The first three from the above list are differential pairs. They are to be routed "loosely coupled" with a separation of 2 track widths. Their lengths should be the same as the DDRE_DQS lines.
- The next net (DDRE_FBCLK) needs to match the combined length of DDRE_DQS lines plus the length of the DDRE_DQ lines plus 2.42 inches for unregistered DIMMs.
- The next net (DDRE_DLL_CLK) needs only to route between the two pins on the Stratix device.
- The last net (DDRE_SMA_DLL_CLK) needs only to route from the SMA to the Stratix device (length of trace is not critical).

DDR Devices Clocks (U15, U17, U22, U24)

- These clocks should be matched in length within +/- 0.050".
  - DDRA_CK_P / DDRA_CK_N (differential)
  - DDR_FBCLK (single-ended)
- The first net (DDRA_CK_P/DDRA_CK_N) is a differential pair. It is to be routed in a unique way because this clock pair is driving all DDR devices. Its length should be the same as the DDRA_DQS lines.
- The next net (DDR_FBCLK) needs to match the combined length of the DDRA_CK lines plus the length of the DDRA_DQS lines.

RLDRAM CIO Devices Clocks (U11, U12) (see figure and table below)

- These clocks should be matched in length within +/- 0.050".
  - RLDC_CK_P / RLDC_CK_N (differential)
  - RLDC_DK_P / RLDC_DK_N (differential)
  - RLDC2_CK_P / RLDC2_CK_N (differential)
  - RLDC2_DK_P / RLDC2_DK_N (differential)
  - RLDC_QK_P0 / RLDC_QK_N0 (differential)
  - RLDC_QK_P1 / RLDC_QK_N1 (differential)
  - RLDC2_QK_P0 / RLDC2_QK_N0 (differential)
  - RLDC2_QK_P1 / RLDC2_QK_N1 (differential)
  - RLD_FBCLK (single-ended with termination)
  - RLD_DLL_CLK (single-ended with termination)
  - RLD_SMA_DLL_CLK (single-ended from SMA)
- The first two nets are differential pairs. Route these nets "loosely coupled" (spacing of 2 track widths) from U16 to U11 and then to the termination resistors.
- The next two nets are differential pairs. Route these nets "loosely coupled" (spacing of 2 track widths) from U16 to U12 and then to the termination resistors.
- The next two nets are also differential pairs. Route these nets "loosely coupled" (spacing of 2 track widths) from U11 to the Stratix device and then to the termination resistors.
- The next two nets are also differential pairs. Route these nets "loosely coupled" (spacing of 2 track widths) from U12 to the Stratix device and then to the termination resistors.
- The next net (RLD_FBCLK) needs to match two times the length of the RLDC_CK clocks from the Stratix to the RLDRAM device. Route this net from U20 pin B12 to U20 pin B15 then to R152 and R153. The length from U20 pins B12 to B15 needs to be two times the length of the RLDC_CK clocks.
- The next net (RLD_DLL_CLK) needs only to route between the two pins on the Stratix device.
- The last net (RLD_SMA_DLL_CLK) needs only to route from the SMA to the Stratix device (length of trace is not critical).

RLDRAM SIO Devices Clocks (U13) (see figure and table below)

- These clocks should be matched in length within +/- 0.050".
  - RLDS_CK_P / RLDS_CK_N (differential)
  - RLDS_QK_P0 / RLDS_QK_N0 (differential)
  - RLDS_QK_P1 / RLDS_QK_N1 (differential)
- The first net (RLDS_CK_P / RLDS_CK_N) is a differential pair and should be routed as such. RLDS_CK_P is to be routed from U20 pin F22 to U13 pin J12 to U13 pin K1 then to R84. RLDS_CK_N is to be routed from U20 pin G20 to U13 pin K12 to U13 pin K2 then to R77. Its length should be the same as the RLDS_D lines.
- The next two nets are also differential pairs. Route these nets from U13 to the Stratix device and then to the termination resistors.

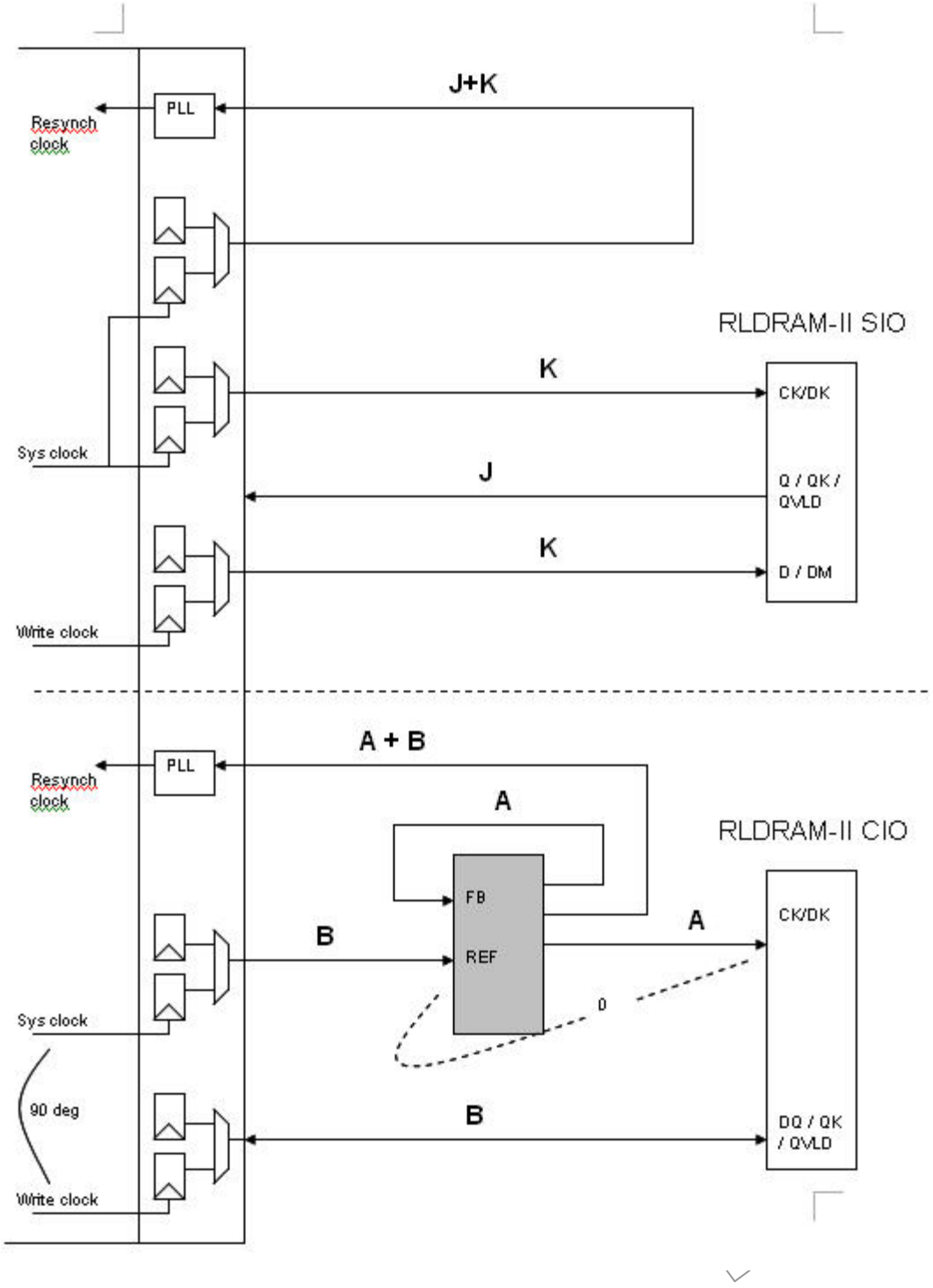


Figure VIII: RLDRAM II Clocks

As was stated before, all lengths for RLDRAM II devices and for that matter and high-speed memory interface should be 5 inches +/-.250 inches. From the figure below, this would correspond to J and K for RLDRAM SIO and B for RLDRAM CIO. For RLDRAM CIO length A can be any length. The following table describes how each clock net corresponds with the RLDRAM II clock figure regarding their lengths.

Function	Net Name	Net Length
RLDS II Device Input Clock	RLDS_CK_P, _N	K
RLDS II Device Output Clocks	RLDS_QK_P[1:0], _N[1:0]	J
RLDRAM II Device Feedback Clock	RLD_FBCLK	J + K
RLDC II Clock Buffer Input Clocks	RLDC_REFCLK_P,_N	B
	RLDC_CK_OUT	B
RLDC II Clock Buffer Output Clocks	RLDC_CK_P,_N	A
	RLDC_DK_P,_N	A
	RLDC2_CK_P,_N	A
	RLDC2_DK_P,_N	A
RLDC II Clock Buffer Feedback Clock	BUF_FB_P,_N	A
RLDC II Clock Buffer Output Feedback Clock	RLD_BUF_FBCLK_P,_N	A + B

Notes:

J does not have to equal K, but in this case J = K = 5 inches.
B does not have to equal A, but B = 5 inches.

CLK_TO_SCRUZ

- No specific routing rules. This is least important of all clock nets and is actually rarely used.

S_SMB_CLK

- No specific routing rules.

ENET_LCLK

- No specific routing rules.

CLKOUT_P, CLKOUT_N

- Same rules as differential clock.

4.5 Configuration

General Rule: Route signals on 5 mil traces with 3 to 1 spacing

JTAG Configuration

1) Routing of nets for the JTAG interface
   a. Route JTAG_TCK, and JTAG_TMS in matched length in a starburst fashion from J27 to U20, U10, and J51. Make the route as short as possible.
      i. For U10 make sure that the routed length of the individual nets JTAG_TCK and JTAG_TMS match the length of the sum of the two nets JTAG_CONN_TDO + JTAG_MAX_TDI.
      ii. For U20 make sure that the routed length of the individual nets JTAG_TCK and JTAG_TMS match the length of the sum of the two nets JTAG_STRATIX_TDI + JTAG_MAX_TDO.
      iii. For J51 make sure that the routed length of the individual nets JTAG_TCK and JTAG_TMS match the length of the sum of the two nets JTAG_EXP_TDI + JTAG_CONN_TDO.
   b. Route the following net JTAG_EXP_TDO, as short as possible.

Passive Configuration

2) Routing of nets for the Fast Passive Parallel Configuration using the MAX/FLASH circuitry

a. Route the following nets from U10 to U19, U20 to U19. All address, data and control lines need to be matched in length within +/- 100 mils between the Max and Flash, and the Flash and Stratix devices. The following itemized nets need to be matched within +/- 100 mils and be routed as short as possible.
    i. CONFIG_DCLK(U10 – U20)
    ii. EP1S_CONF_DONE (U10 – U20)
    iii. EP1S_CONFIGn (U10 – U20)
    iv. EP1S_STATUSn (U10 – U20)
    v. CONFIG_D[7:0](U10 – U20)
b. Route the following nets from J51 to U20. The following itemized nets need to be matched within +/- 100 mils and be routed as short as possible.
    i. CONFIG_DCLK(J51 – U20)
    ii. EP1S_CONF_DONE (J51 – U20)
    iii. EP1S_CONFIGn (J51 – U20)
    iv. EP1S_STATUSn (J51 – U20)
    v. CONFIG_D[7:0](J51 – U20)

5