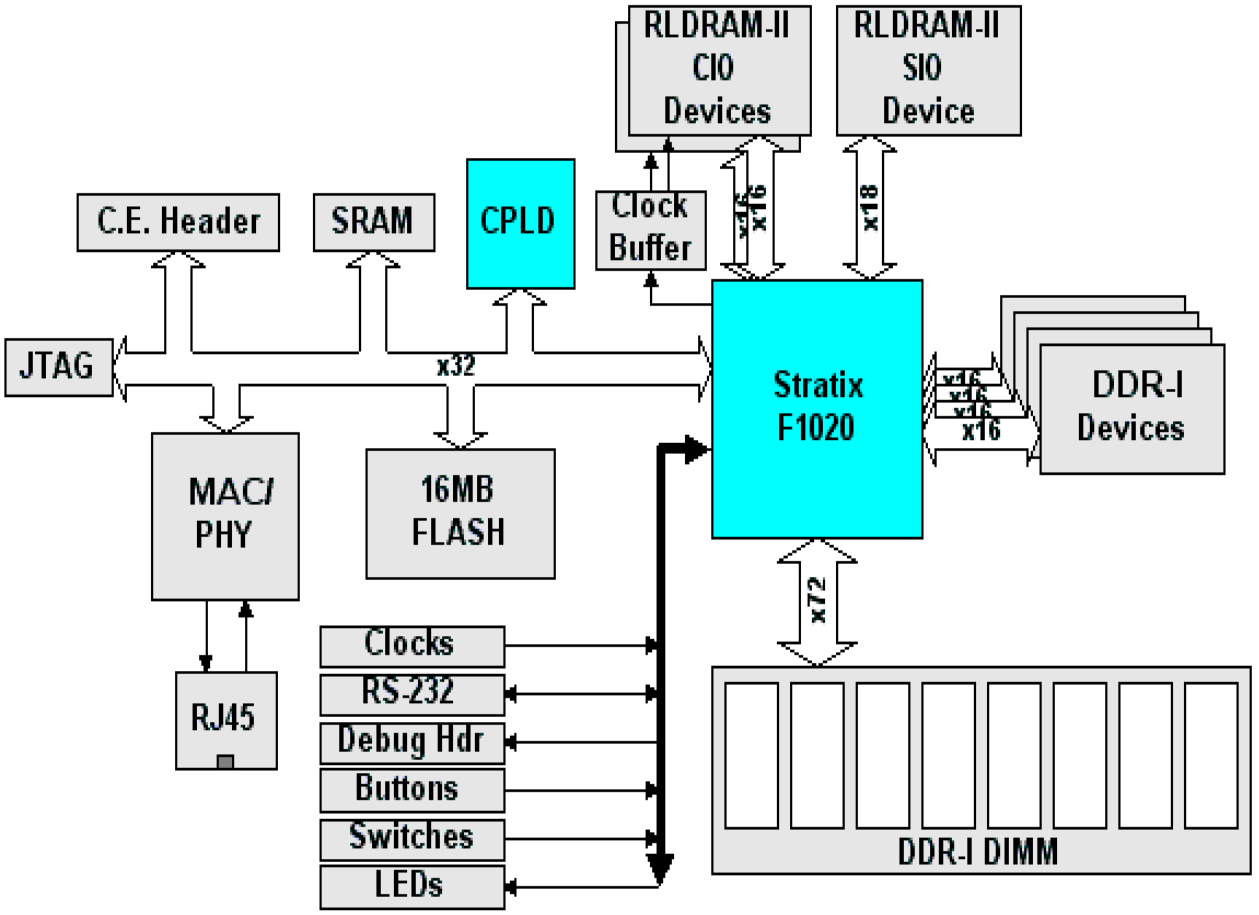
NOTES:

1. Altera Stratix Schematic Symbol Breakdown:
   - (a) Bank1 - GENERAL PURPOSE I/O
   - (b) Bank2 - GENERAL PURPOSE I/O
   - (c) Bank3 - RLDRAM-II SIO DEVICE
   - (d) Bank4 - RLDRAM-II CIO DEVICES
   - (e) Bank5 - DDR-I DEVICES
   - (f) Bank6 - DDR-I DEVICES
   - (g) Bank7 - DDR-I DIMM
   - (h) Bank8 - DDR-I DIMM
   - (i) Configuration/GPIO
   - (j) Clocks/GPIO
   - (k) VCCINT/GND
   - (l) VCCIO/GND

Stratix Memory Board Block Diagram

REV	DATE	PAGES	DESCRIPTION
A-1	04/13/2004	3,6,7,8,12,14,25, 26,27, and 28	Added changes for RLDRAM, Power, Configuration, MAX, LEDs, and Santa Cruz.



PAGE	DESCRIPTION
1	TITLE, NOTES, REVISION HISTORY
2	IO BANK DIAGRAM
3	MAIN POWER SOURCE
4	STRATIX PLL AND POWER
5	STRATIX DECOUPLING
6	CPLD and CONFIGURATION
7	CLOCK CIRCUITRY
8	STRATIX BANK 3, 4
9	RLDRAM II SIO
10	RLDRAM II SIO TERMINATIONS
11	RLDRAM II CIO 1
12	RLDRAM II CIO 1 TERMINATIONS
13	RLDRAM II CIO 2
14	RLDRAM II CIO 2 TERMINATIONS
15	STRATIX BANK 1, 2
16	DDR I SDRAM PAGE 1
17	DDR I SDRAM TERM PAGE 1 (SHARED)
18	DDR I SDRAM A AND B TERMINATIONS
19	DDR I SDRAM PAGE 2
20	DDR I SDRAM C AND D TERMINATIONS
21	STRATIX BANK 7, 8
22	DDR I SDRAM DIMM
23	DDR I SDRAM DIMM TERM PAGE 1
24	DDR I SDRAM DIMM TERM PAGE 2
25	STRATIX BANK 5, 6
26	DEBUG PROTO HEADERS
27	10/100 ETHERNET
28	SEVEN SEGMENT DISPLAYS AND LEDS
29	PUSH BUTTONS / DIP SWITCHES
30	RS-232
31	SRAM and FLASH

PLL Ground

Ground

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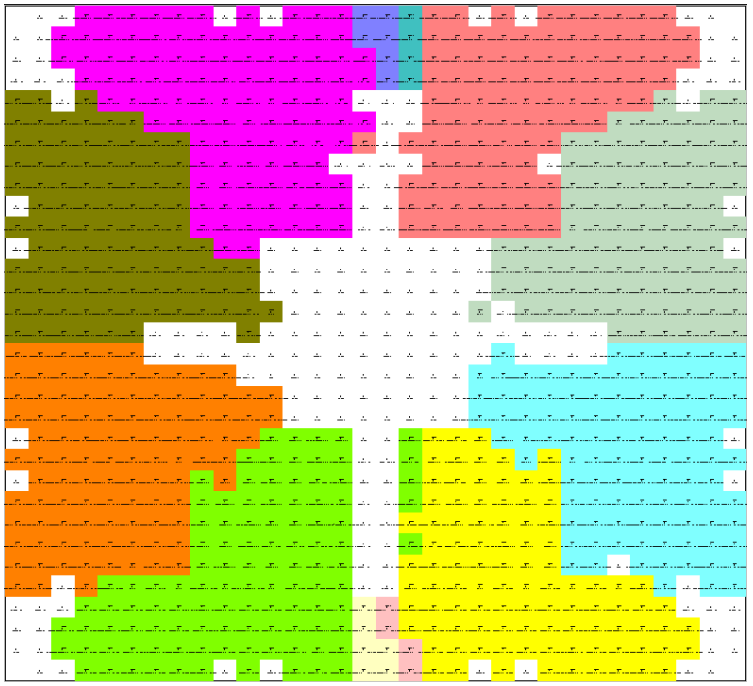
Stratix Memory Board IO Bank Diagram

Stratix F1020 Package Top View

BANK 4
VCCIO = 1.5V / 1.8V
RLDRAM CIO DEVICES

BANK 3
VCCIO = 1.5V / 1.8V
RLDRAM-II SIO DEVICE



BANK 5
VCCIO = 3.3V
x32 SHARED DATA BUS
x26 SHARED ADDRESS BUS
FLASH SIGNALS
SRAM SIGNALS
USER LEDs

BANK 2
VCCIO = 2.6V
DDR-I DEVICES

BANK 6
VCCIO = 3.3V
PUSH BUTTON INPUTS
ETHERNET SIGNALS
DEBUG PORT SIGNALS
RS-232 SIGNALS
7-SEGMENT DISPLAYS

BANK 1
VCCIO = 2.6V
DDR-I DEVICES

BANK 7
VCCIO = 2.6V
DDR-I DIMM

BANK 8
VCCIO = 2.6V
DDR-I DIMM

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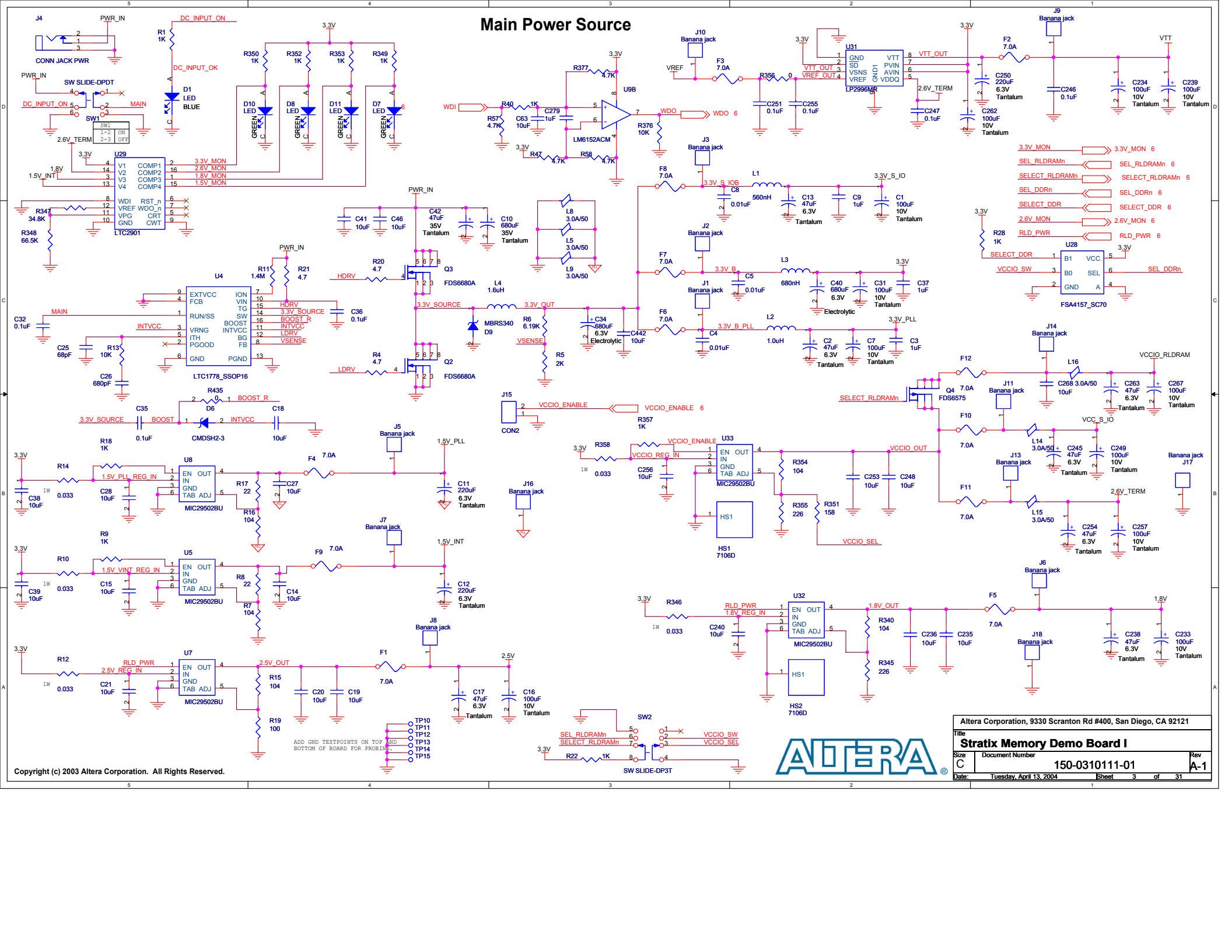
Main Power Source



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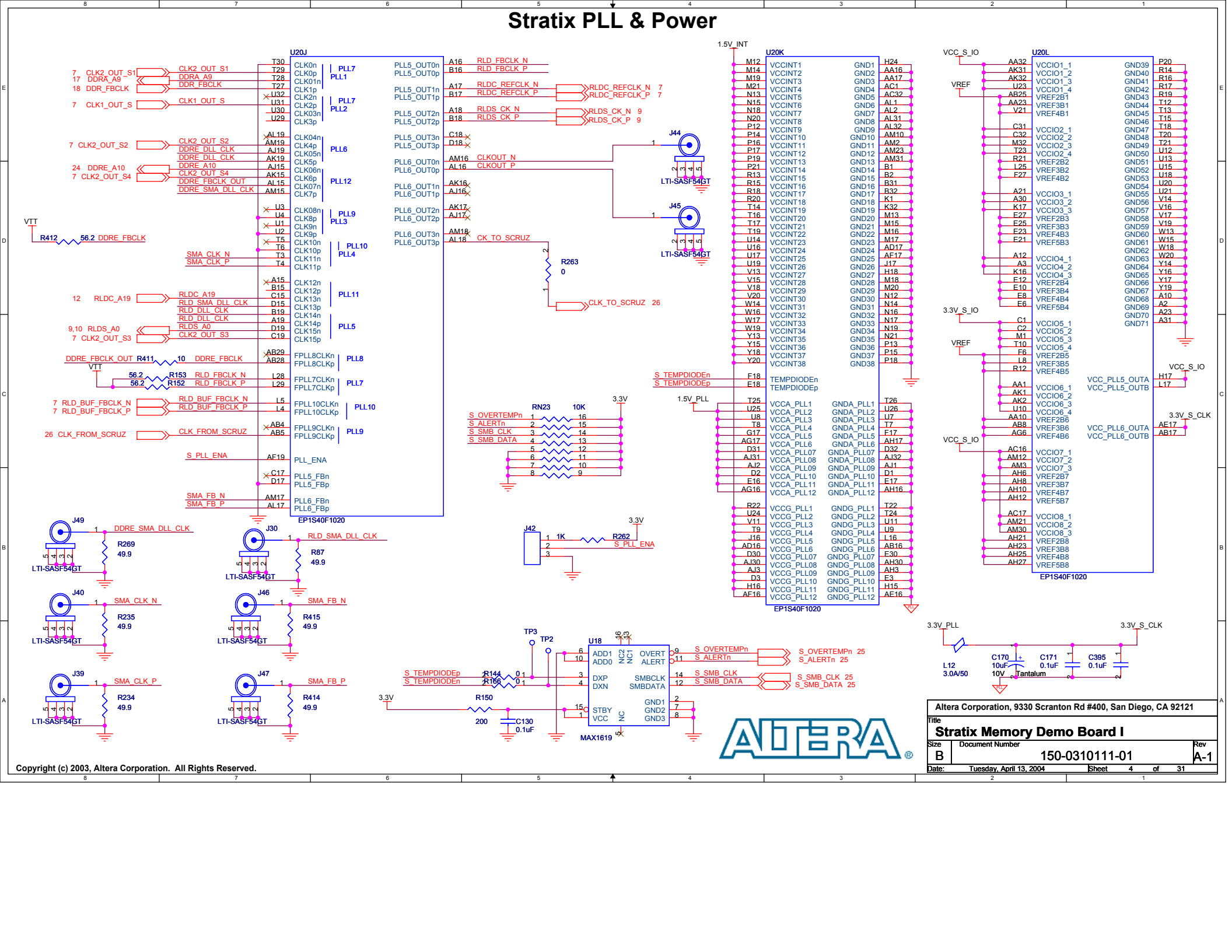
Stratix PLL & Power



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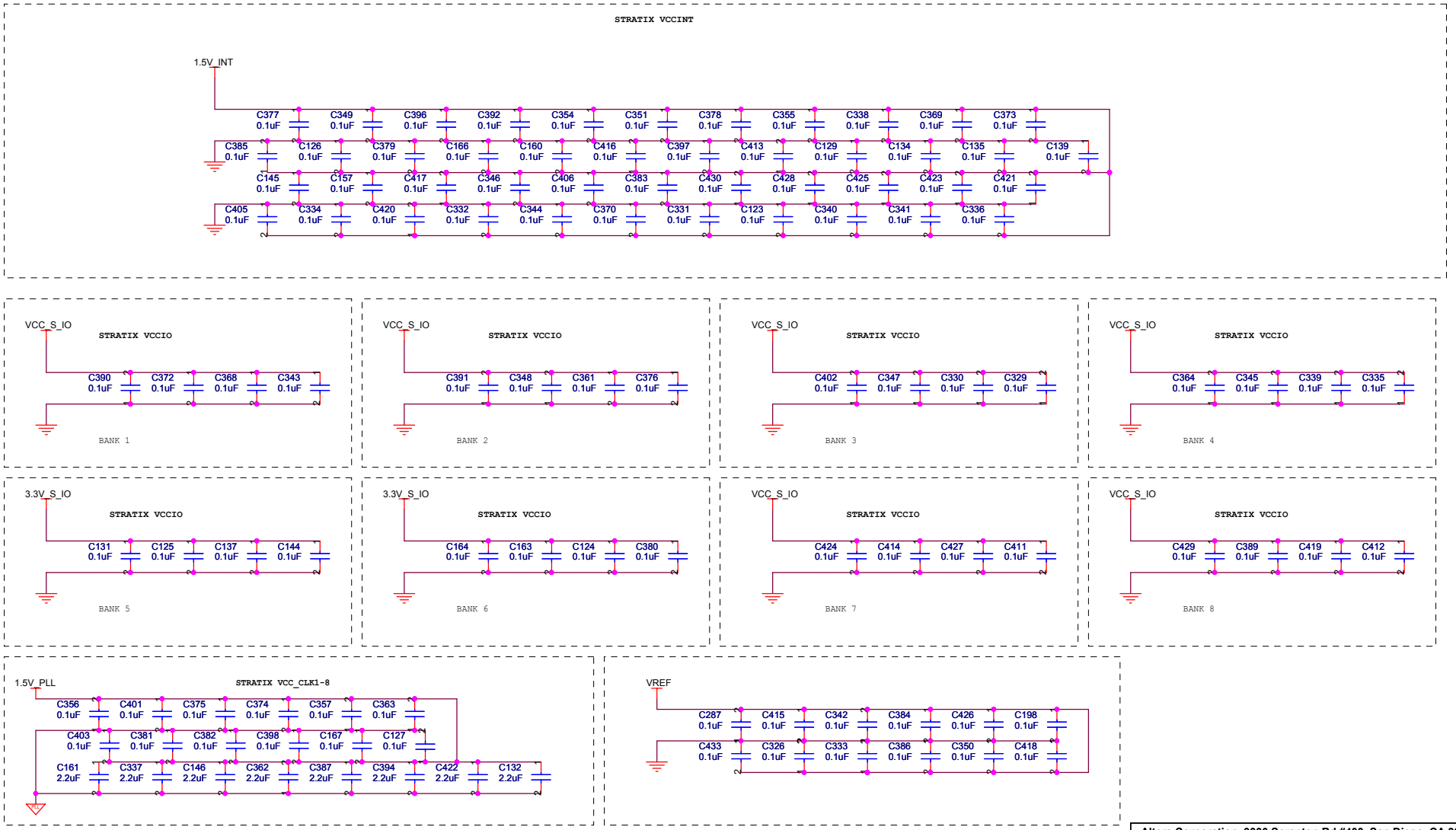
Stratix Decoupling Capacitors



NOTE: PLACE ALL CAPACITORS ON THIS PAGE AS CLOSE AS POSSIBLE TO THE PINS OF THE STRATIX DEVICE.

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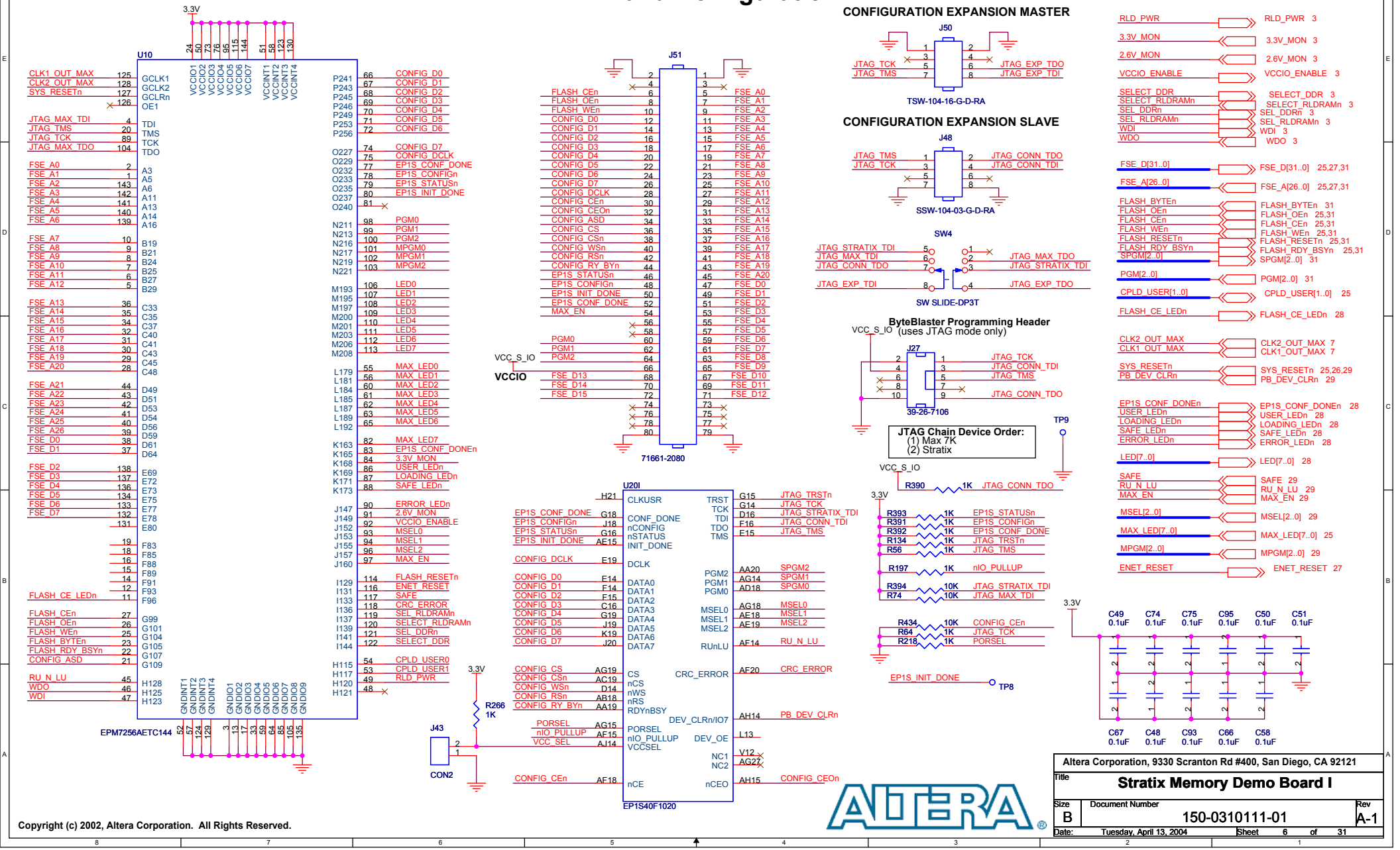
CPLD and Configuration



CONFIGURATION EXPANSION MASTER

CONFIGURATION EXPANSION SLAVE

ByteBlaster Programming Header
(uses JTAG mode only)

Off-page connectors

RLD_PWR 3
3.3V_MON 3
2.6V_MON 3
VCCIO_ENABLE 3
SELECT_DDR 3
SELECT_RLDRAMn 3
SEL_DDRn 3
SEL_RLDRAMn 3
WDI 3
WDO 3
FSE_D[31..0] 25,27,31
FSE_A[26..0] 25,27,31
FLASH_BYTEn 31
FLASH_OEn 25,31
FLASH_CEn 25,31
FLASH_WEn 25,31
FLASH_RESETn 25,31
FLASH_RDY_BSYn 25,31
SPGM[2..0] 31
PGM[2..0] 31
CPLD_USER[1..0] 25
FLASH_CE_LEDn 28
CLK2_OUT_MAX 7
CLK1_OUT_MAX 7
SYS_RESETn 25,26,29
PB_DEV_CLRn 29
EP1S_CONF_DONEn 28
USER_LEDn 28
LOADING_LEDn 28
SAFE_LEDn 28
ERROR_LEDn 28
LED[7..0] 28
SAFE 29
RU_N_LU 29
MAX_EN 29
MSEL[2..0] 29
MAX_LED[7..0] 25
MPGM[2..0] 29
ENET_RESET 27

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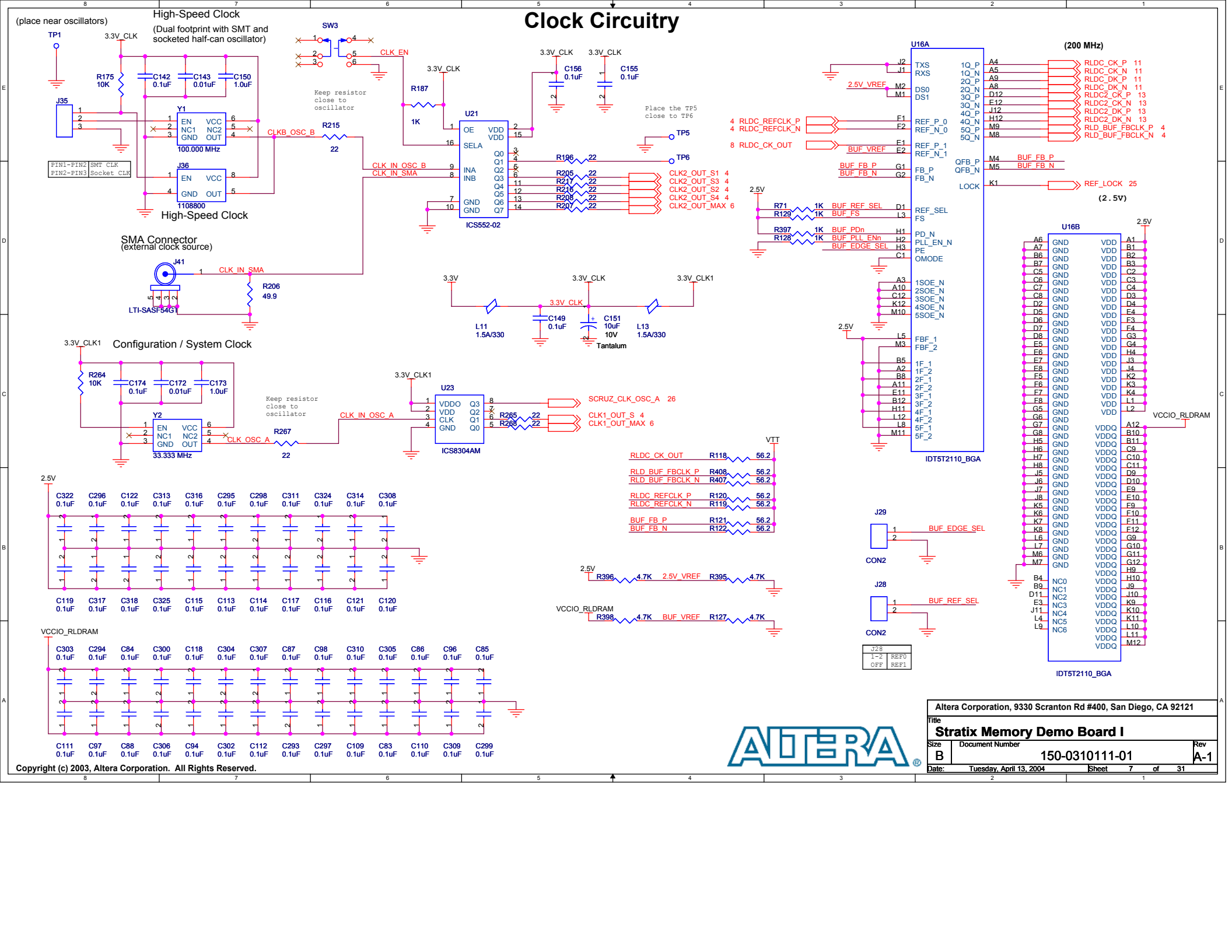
Clock Circuitry



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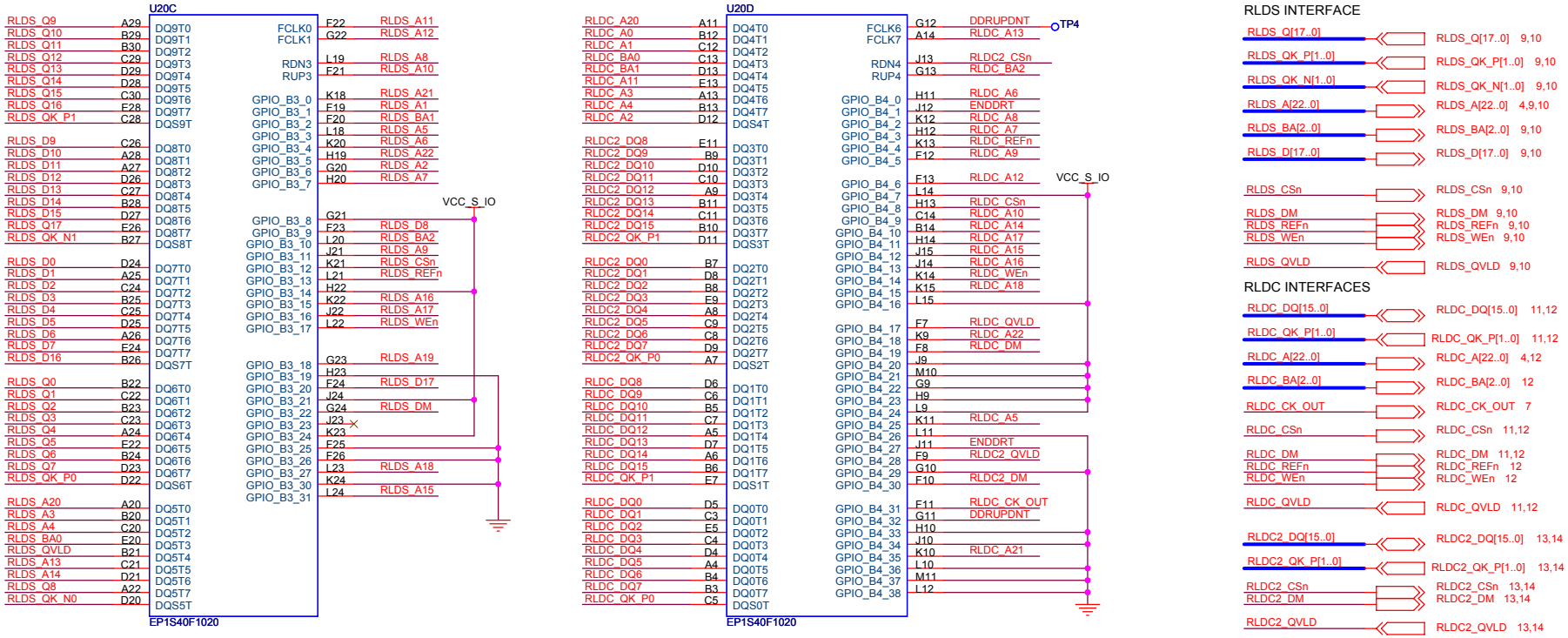
Stratix Bank 3, Bank 4



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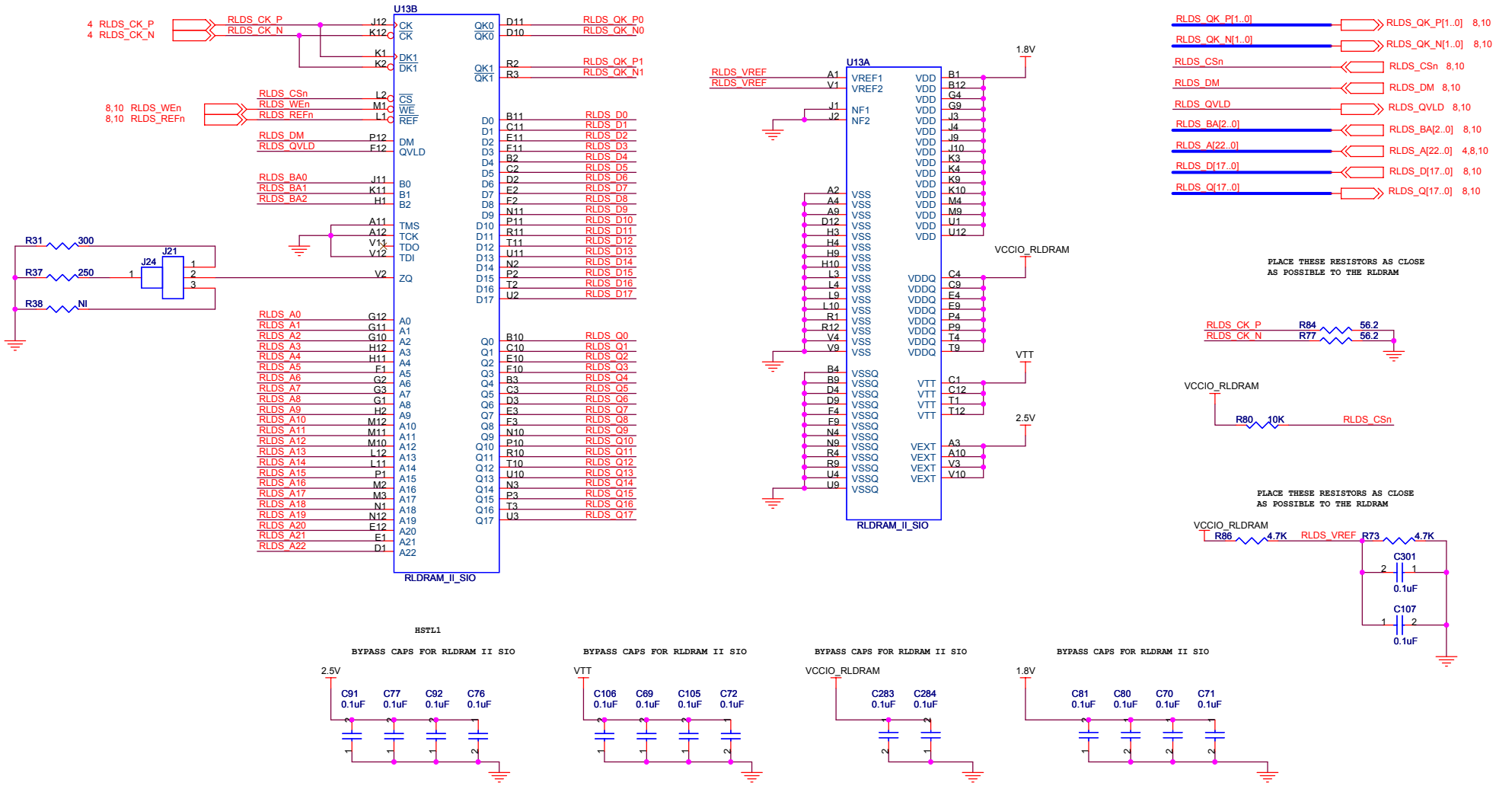
RLDRAM II SIO



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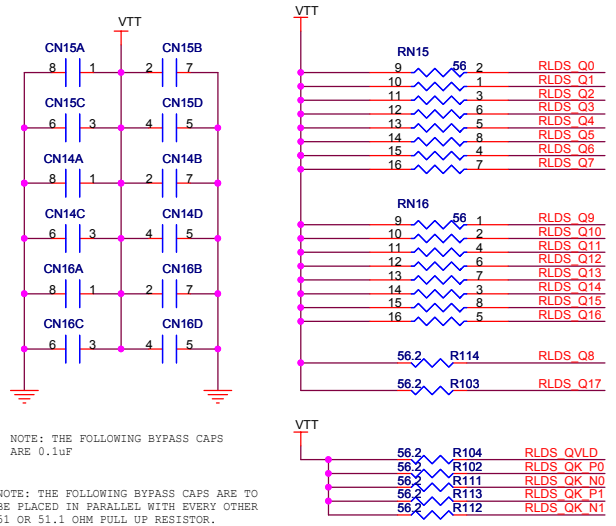
RLDRAM II SIO Terminations

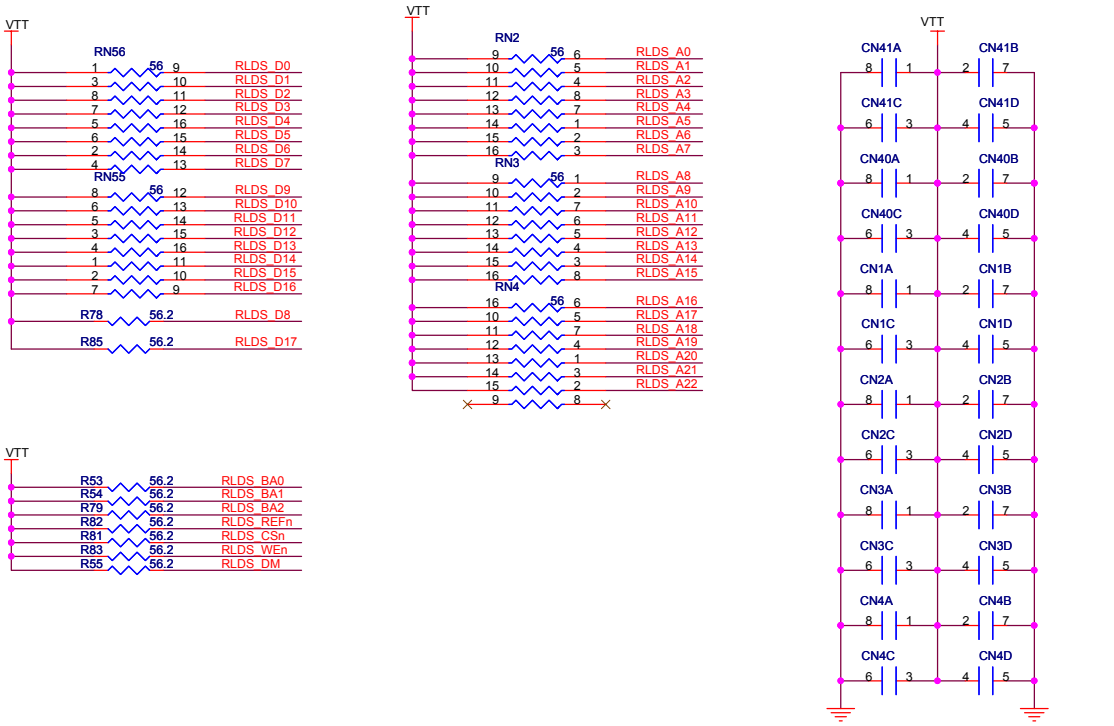
PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE STRATIX DEVICE



NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF

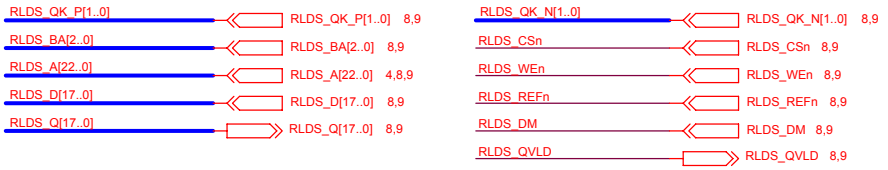
NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51 OR 51.1 OHM PULL UP RESISTOR.

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE RLDRAM II SIO



NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 49.9 OR 51 OHM PULL UP RESISTOR.



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RLDRAM II CIO 1

PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM

VTT

RLDC_CK_P — R380 — 56.2
RLDC_CK_N — R383 — 56.2
RLDC_DK_P — R60 — 56.2
RLDC_DK_N — R59 — 56.2

U11B

7 RLDC_CK_P
7 RLDC_CK_N
7 RLDC_DK_P
7 RLDC_DK_N
VCCIO_RLDRAM
R63
10K
12,13 RLDC_WRITE_En
12,13 RLDC_REF_INn
R29 300
R32 250
R33 NI
J19
J22

RLDC_CK_P J12 CK
RLDC_CK_N K12 CK
RLDC_DK_P K1 DK1
RLDC_DK_N K2 DK1
RLDC_QK_P0 D11 QK0
RLDC_QK_N0 D10 QK0
RLDC_QK_P1 R2 QK1
RLDC_QK_N1 R3 QK1
RLDC_CSn L2 CS
RLDC_WRITE_En M1 WE
RLDC_REF_INn L1 REF
RLDC_DM P12 DM
RLDC_QVLD F12 QVLD
RLDC_BANK0 J11 B0
RLDC_BANK1 K11 B1
RLDC_BANK2 H1 B2
A11 TMS
A12 TCK
V11 TDO
V12 TDI
V2 ZQ

RLDC_ADR0 G12 A0
RLDC_ADR1 G11 A1
RLDC_ADR2 G10 A2
RLDC_ADR3 H12 A3
RLDC_ADR4 H11 A4
RLDC_ADR5 F1 A5
RLDC_ADR6 G2 A6
RLDC_ADR7 G3 A7
RLDC_ADR8 G1 A8
RLDC_ADR9 H2 A9
RLDC_ADR10 M12 A10
RLDC_ADR11 M11 A11
RLDC_ADR12 M10 A12
RLDC_ADR13 L12 A13
RLDC_ADR14 L11 A14
RLDC_ADR15 P1 A15
RLDC_ADR16 M2 A16
RLDC_ADR17 M3 A17
RLDC_ADR18 N1 A18
RLDC_ADR19 N12 A19
RLDC_ADR20 E12 A20
RLDC_ADR21 F1 A21
RLDC_ADR22 D1 A22

DNU0 B11
DNU1 C11
DNU2 E11
DNU3 F11
DNU4 B2
DNU5 C2
DNU6 D2
DNU7 E2
DNU8 F2
DNU9 N11
DNU10 P11
DNU11 R11
DNU12 T11
DNU13 U11
DNU14 N2
DNU15 P2
DNU16 T2
DNU17 U2

DQ0 B10 RLDC_DQ0
DQ1 C10 RLDC_DQ1
DQ2 E10 RLDC_DQ2
DQ3 F10 RLDC_DQ3
DQ4 B3 RLDC_DQ4
DQ5 C3 RLDC_DQ5
DQ6 D3 RLDC_DQ6
DQ7 E3 RLDC_DQ7
DQ8 F3
DQ9 N10 RLDC_DQ8
DQ10 P10 RLDC_DQ9
DQ11 R10 RLDC_DQ10
DQ12 T10 RLDC_DQ11
DQ13 U10 RLDC_DQ12
DQ14 N3 RLDC_DQ13
DQ15 P3 RLDC_DQ14
DQ16 T3 RLDC_DQ15
DQ17 U3

RLDRAM_II_CIO

U11A

RLDC_VREF A1 VREF1
RLDC_VREF V1 VREF2
J1 NF1
J2 NF2
GND A2 VSS
A4 VSS
A9 VSS
D12 VSS
H3 VSS
H4 VSS
H9 VSS
H10 VSS
L3 VSS
L4 VSS
L9 VSS
L10 VSS
R1 VSS
R12 VSS
V4 VSS
V9 VSS
B4 VSSQ
B9 VSSQ
D4 VSSQ
D9 VSSQ
F4 VSSQ
F9 VSSQ
N4 VSSQ
N9 VSSQ
R4 VSSQ
R9 VSSQ
U4 VSSQ
U9 VSSQ

1.8V
VDD B1
VDD B12
VDD G4
VDD G9
VDD J3
VDD J4
VDD J9
VDD J10
VDD K3
VDD K4
VDD K9
VDD K10
VDD M4
VDD M9
VDD U1
VDD U12

VCCIO_RLDRAM
VDDQ C4
VDDQ C9
VDDQ E4
VDDQ E9
VDDQ P4
VDDQ P9
VDDQ T4
VDDQ T9

VTT
VTT C1
VTT C12
VTT T1
VTT T12

2.5V
VEXT A3
VEXT A10
VEXT V3
VEXT V10

RLDRAM_II_CIO

RLDC_QK_P[1..0] RLDC_QK_P[1..0] 8,12
RLDC_QK_N[1..0] RLDC_QK_N[1..0] 12
RLDC_CSn RLDC_CSn 8,12
RLDC_DM RLDC_DM 8,12
RLDC_QVLD RLDC_QVLD 8,12
RLDC_BANK[2..0] RLDC_BANK[2..0] 12,13
RLDC_ADR[22..0] RLDC_ADR[22..0] 12,13
RLDC_DQ[15..0] RLDC_DQ[15..0] 8,12

PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM

VCCIO_RLDRAM
R76 4.7K RLDC_VREF R72 4.7K
C89 0.1uF
C59 0.1uF

HSTL1

BYPASS CAPS FOR RLDRAM II CIO

1.8V
C68 0.1uF
C53 0.1uF
C100 0.1uF
C282 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

VCCIO_RLDRAM
C278 0.1uF
C286 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

2.5V
C99 0.1uF
C52 0.1uF
C101 0.1uF
C54 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

VTT
C78 0.1uF
C60 0.1uF
C292 0.1uF
C276 0.1uF

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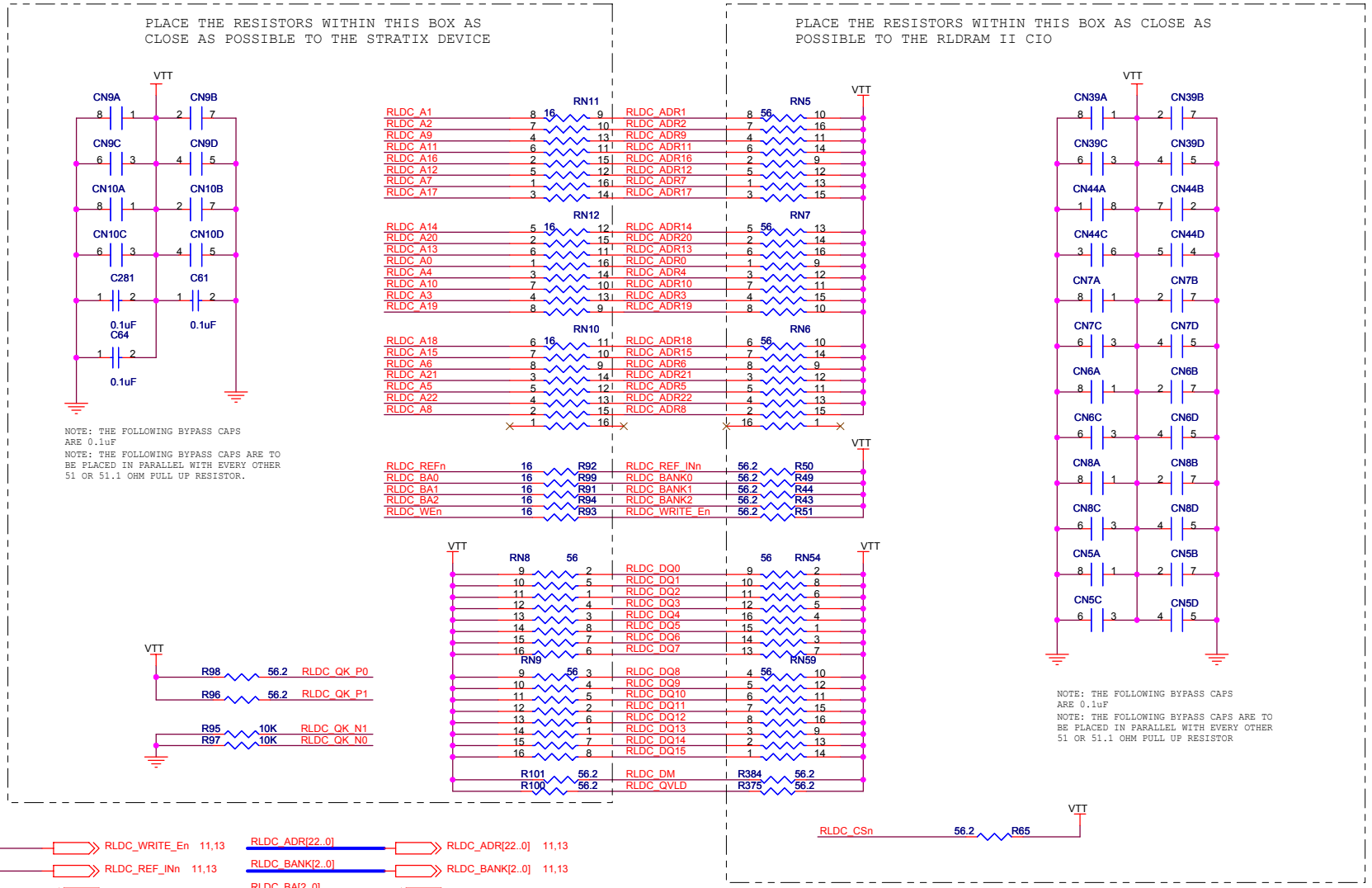
RLDRAM II CIO 1 Terminations



RLDC_WRITE_En — RLDC_WRITE_En 11,13
RLDC_REF_INn — RLDC_REF_INn 11,13
RLDC_CSn — RLDC_CSn 8,11
RLDC_WEn — RLDC_WEn 8
RLDC_REFn — RLDC_REFn 8
RLDC_DM — RLDC_DM 8,11
RLDC_QVLD — RLDC_QVLD 8,11

RLDC_ADR[22..0] — RLDC_ADR[22..0] 11,13
RLDC_BANK[2..0] — RLDC_BANK[2..0] 11,13
RLDC_BA[2..0] — RLDC_BA[2..0] 8
RLDC_A[22..0] — RLDC_A[22..0] 4,8
RLDC_DQ[15..0] — RLDC_DQ[15..0] 8,11
RLDC_QK_P[1..0] — RLDC_QK_P[1..0] 8,11
RLDC_QK_N[1..0] — RLDC_QK_N[1..0] 11

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RLDRAM II CIO 2

PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM

VTT

RLDC2_CK_P R61 56.2
RLDC2_CK_N R62 56.2
RLDC2_DK_P R378 56.2
RLDC2_DK_N R379 56.2

U12B

7 RLDC2_CK_P
7 RLDC2_CK_N
7 RLDC2_DK_P
7 RLDC2_DK_N
RLDC2_QK_P0
RLDC2_QK_N0
RLDC2_QK_P1
RLDC2_QK_N1
RLDC2_CSn
11,12 RLDC_WRITE_En
11,12 RLDC_REF_INn
RLDC2_DM
RLDC2_QVLD
RLDC_BANK0
RLDC_BANK1
RLDC_BANK2
RLDC_ADR0
RLDC_ADR1
RLDC_ADR2
RLDC_ADR3
RLDC_ADR4
RLDC_ADR5
RLDC_ADR6
RLDC_ADR7
RLDC_ADR8
RLDC_ADR9
RLDC_ADR10
RLDC_ADR11
RLDC_ADR12
RLDC_ADR13
RLDC_ADR14
RLDC_ADR15
RLDC_ADR16
RLDC_ADR17
RLDC_ADR18
RLDC_ADR19
RLDC_ADR20
RLDC_ADR21
RLDC_ADR22

CK CK DK1 DK1 QK0 QK0 QK1 QK1 CS WE REF DM QVLD B0 B1 B2 TMS TCK TDO TDI ZQ A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22

DNU0 DNU1 DNU2 DNU3 DNU4 DNU5 DNU6 DNU7 DNU8 DNU9 DNU10 DNU11 DNU12 DNU13 DNU14 DNU15 DNU16 DNU17

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17

RLDC2_DQ0 RLDC2_DQ1 RLDC2_DQ2 RLDC2_DQ3 RLDC2_DQ4 RLDC2_DQ5 RLDC2_DQ6 RLDC2_DQ7 RLDC2_DQ8 RLDC2_DQ9 RLDC2_DQ10 RLDC2_DQ11 RLDC2_DQ12 RLDC2_DQ13 RLDC2_DQ14 RLDC2_DQ15

RLDRAM_II_CIO

VCCIO_RLDRAM
R382 10K
R30 300
R35 250
R36 NI
J20 J23 CON1 CON3

U12A

RLDC2_VREF
RLDC2_VREF
VREF1 VREF2 NF1 NF2 VSS VDD VDDQ VSSQ VTT VEXT

1.8V
VCCIO_RLDRAM
VTT
2.5V

RLDRAM_II_CIO

RLDC2_QK_P[1..0] RLDC2_QK_P[1..0] 8,14
RLDC2_QK_N[1..0] RLDC2_QK_N[1..0] 14
RLDC2_CSn RLDC2_CSn 8,14
RLDC2_DM RLDC2_DM 8,14
RLDC2_QVLD RLDC2_QVLD 8,14
RLDC_BANK[2..0] RLDC_BANK[2..0] 11,12
RLDC_ADR[22..0] RLDC_ADR[22..0] 11,12
RLDC2_DQ[15..0] RLDC2_DQ[15..0] 8,14

PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM

VCCIO_RLDRAM R39 4.7K RLDC2_VREF R34 4.7K
C274 0.1uF
C291 0.1uF

HSTL1

BYPASS CAPS FOR RLDRAM II CIO

2.5V
C57 0.1uF C104 0.1uF C55 0.1uF C102 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

VTT
C62 0.1uF C90 0.1uF C275 0.1uF C290 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

VCCIO_RLDRAM
C277 0.1uF C285 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

1.8V
C103 0.1uF C65 0.1uF C280 0.1uF C56 0.1uF

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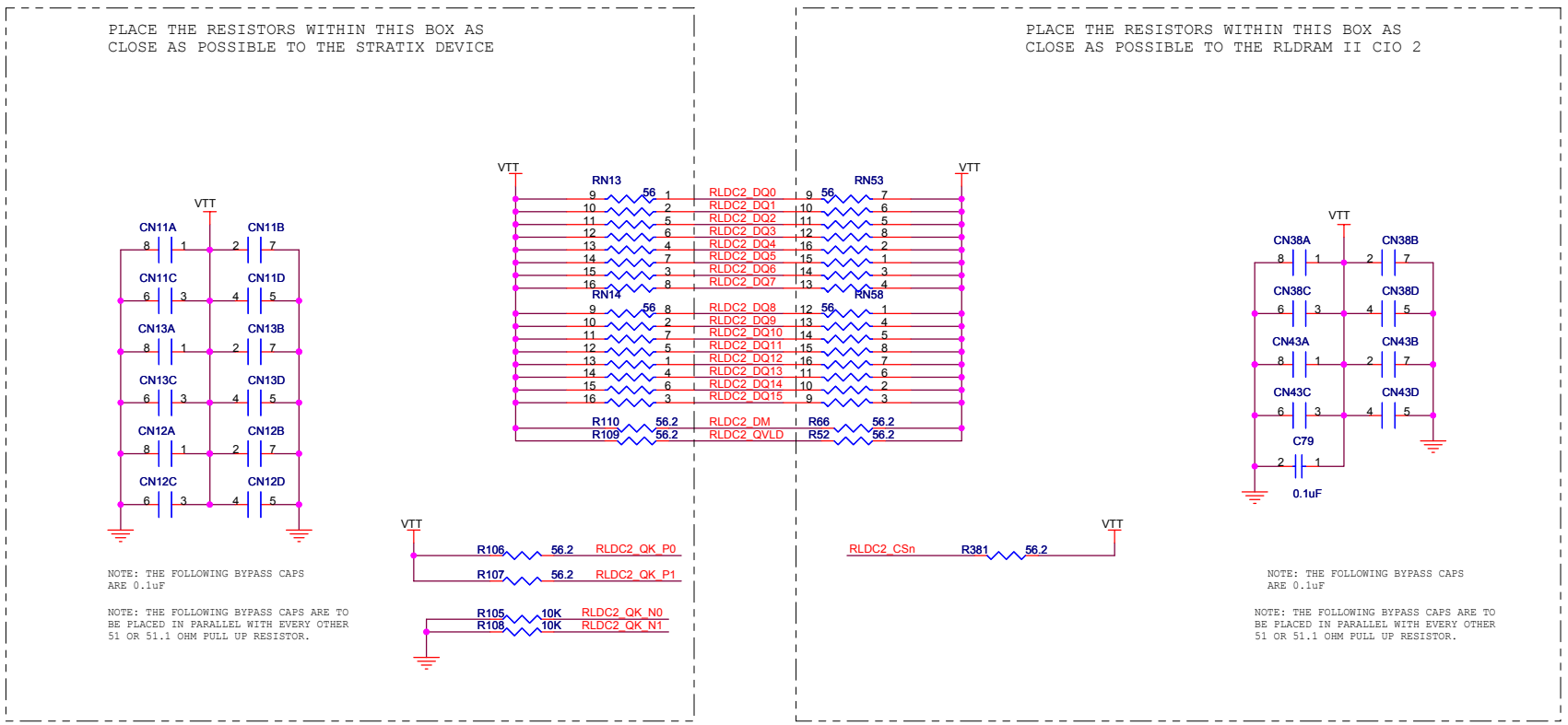
RLDRAM II CIO 2 Terminations



RLDC2_DM — RLDC2_DM 8,13
RLDC2_CSn — RLDC2_CSn 8,13
RLDC2_QVLD — RLDC2_QVLD 8,13
RLDC2_DQ[15..0] — RLDC2_DQ[15..0] 8,13
RLDC2_QK_P[1..0] — RLDC2_QK_P[1..0] 8,13
RLDC2_QK_N[1..0] — RLDC2_QK_N[1..0] 13

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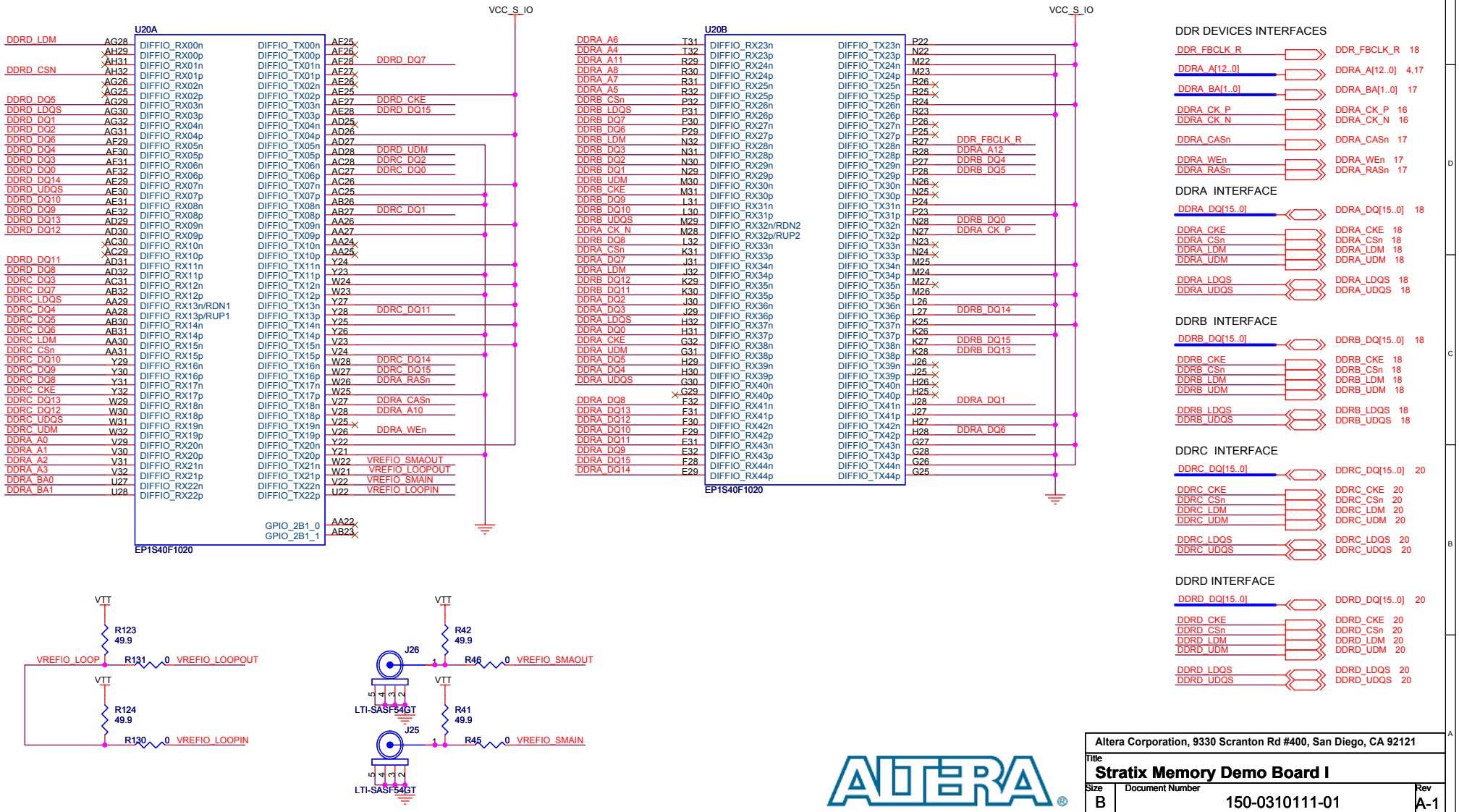
Stratix Bank 1, Bank 2



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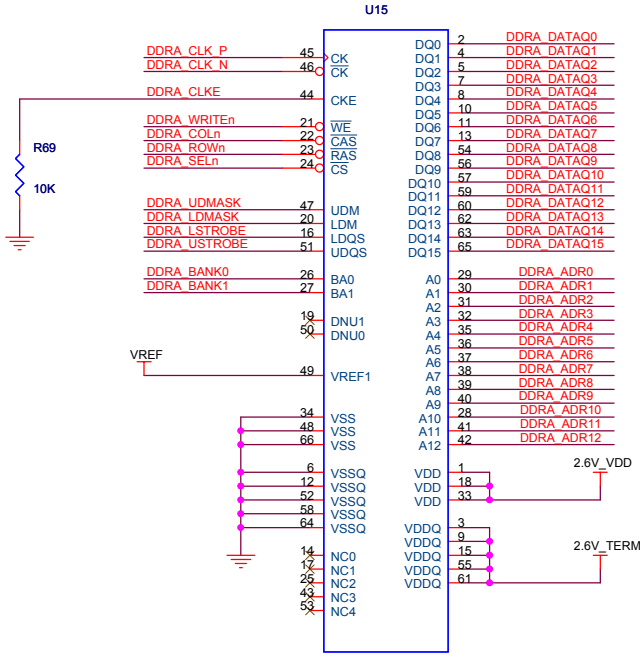
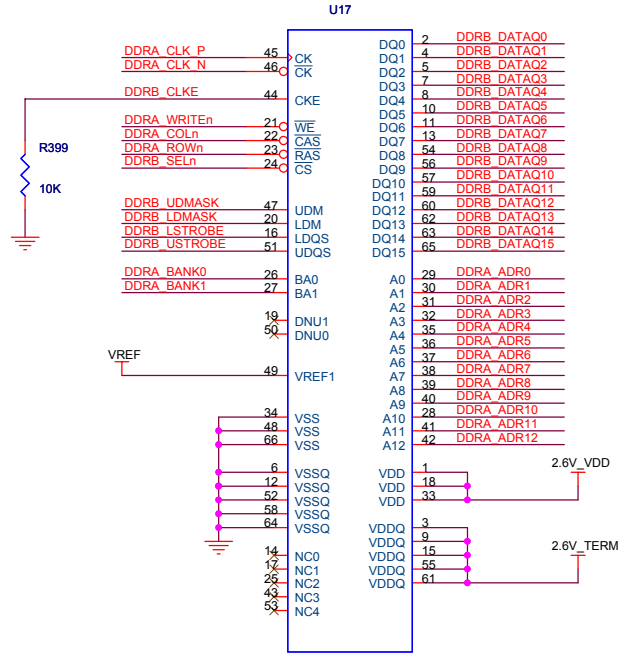
DDR I SDRAM Page 1

Place this resistor as close
to the DDR as possible

DDRA_CK_P R142 24.9 DDRA_CLK_P R143 100 DDRA_CLK_N
DDRA_CK_N R141 24.9 DDRA_CLK_N



SSTL2



DDR I SDRAM SHARED SIGNALS INTERFACE

DDRA_ADR[12..0] — DDRA_ADR[12..0] 17,19
DDRA_BANK[1..0] — DDRA_BANK[1..0] 17,19
DDRA_CLK_P — DDRA_CLK_P 19
DDRA_CLK_N — DDRA_CLK_N 19
DDRA_CK_P — DDRA_CK_P 15
DDRA_CK_N — DDRA_CK_N 15
DDRA_WRITEn — DDRA_WRITEn 17,19
DDRA_COLn — DDRA_COLn 17,19
DDRA_ROWn — DDRA_ROWn 17,19

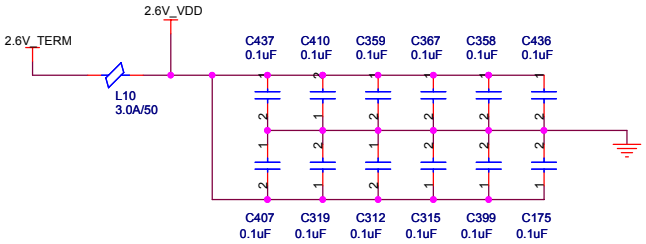
DDRA INTERFACE

DDRA_DATAQ[15..0] — DDRA_DATAQ[15..0] 18
DDRA_CLKE — DDRA_CLKE 18
DDRA_SELn — DDRA_SELn 18
DDRA_UDMASK — DDRA_UDMASK 18
DDRA_LDMASK — DDRA_LDMASK 18
DDRA_USTROBE — DDRA_USTROBE 18
DDRA_LSTROBE — DDRA_LSTROBE 18

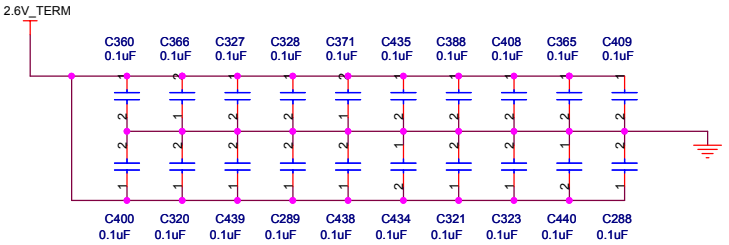
DDRB INTERFACE

DDRB_DATAQ[15..0] — DDRB_DATAQ[15..0] 18
DDRB_CLKE — DDRB_CLKE 18
DDRB_SELn — DDRB_SELn 18
DDRB_UDMASK — DDRB_UDMASK 18
DDRB_LDMASK — DDRB_LDMASK 18
DDRB_USTROBE — DDRB_USTROBE 18
DDRB_LSTROBE — DDRB_LSTROBE 18

BYPASS CAPS FOR DDR-I



BYPASS CAPS FOR DDR-I



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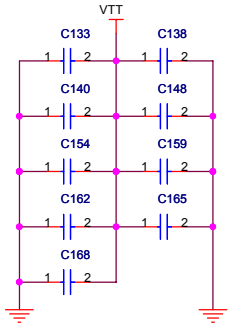
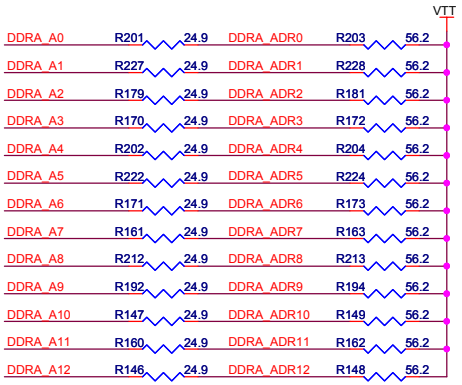
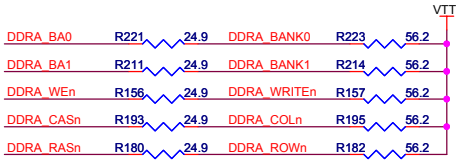
DDR I SDRAM Terminations, Page 1 (Shared Signals Between All DDR SDRAMS)



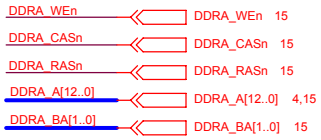
NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51.1 OHM PULL UP RESISTOR.

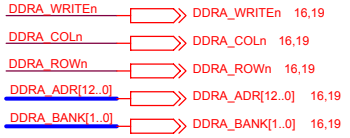




STRATIX SIGNALS



DDR I SDRAM SHARED SIGNALS



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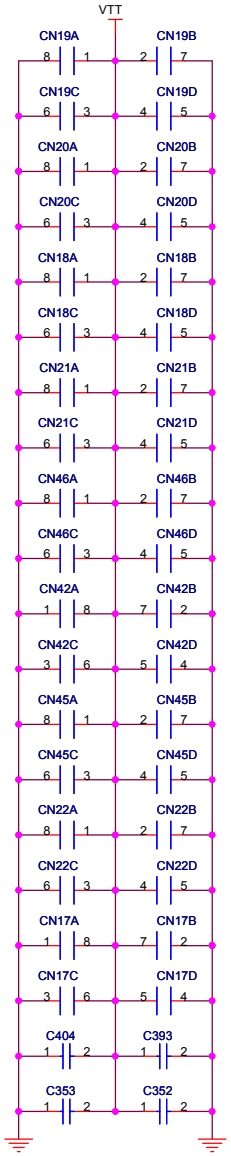
DDR I SDRAM A & B Terminations, Page 2



NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF
NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51 OR 51.1 OHM PULL UP RESISTOR.

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE STRATIX DEVICE

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE DDR'S

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE STRATIX DEVICE

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE DDR'S

STRATIX SIGNALS

DDR_FBCLK_R — DDR_FBCLK_R 15
DDR_FBCLK — DDR_FBCLK 4
DDRA_UDM — DDRA_UDM 15
DDRA_LDM — DDRA_LDM 15
DDRB_UDM — DDRB_UDM 15
DDRB_LDM — DDRB_LDM 15
DDRA_UDQS — DDRA_UDQS 15
DDRA_LDQS — DDRA_LDQS 15
DDRA_DQ[15..0] — DDRA_DQ[15..0] 15
DDRB_UDQS — DDRB_UDQS 15
DDRB_LDQS — DDRB_LDQS 15
DDRB_DQ[15..0] — DDRB_DQ[15..0] 15
DDRA_CKE — DDRA_CKE 15
DDRB_CKE — DDRB_CKE 15
DDRA_CSn — DDRA_CSn 15
DDRB_CSn — DDRB_CSn 15

DDR I SDRAM A & B SIGNALS

DDRA_UDMASK — DDRA_UDMASK 16
DDRA_LDMASK — DDRA_LDMASK 16
DDRB_UDMASK — DDRB_UDMASK 16
DDRB_LDMASK — DDRB_LDMASK 16
DDRA_USTROBE — DDRA_USTROBE 16
DDRA_LSTROBE — DDRA_LSTROBE 16
DDRA_DATAQ[15..0] — DDRA_DATAQ[15..0] 16
DDRB_USTROBE — DDRB_USTROBE 16
DDRB_LSTROBE — DDRB_LSTROBE 16
DDRB_DATAQ[15..0] — DDRB_DATAQ[15..0] 16
DDRA_CLKE — DDRA_CLKE 16
DDRB_CLKE — DDRB_CLKE 16
DDRA_SELn — DDRA_SELn 16
DDRB_SELn — DDRB_SELn 16

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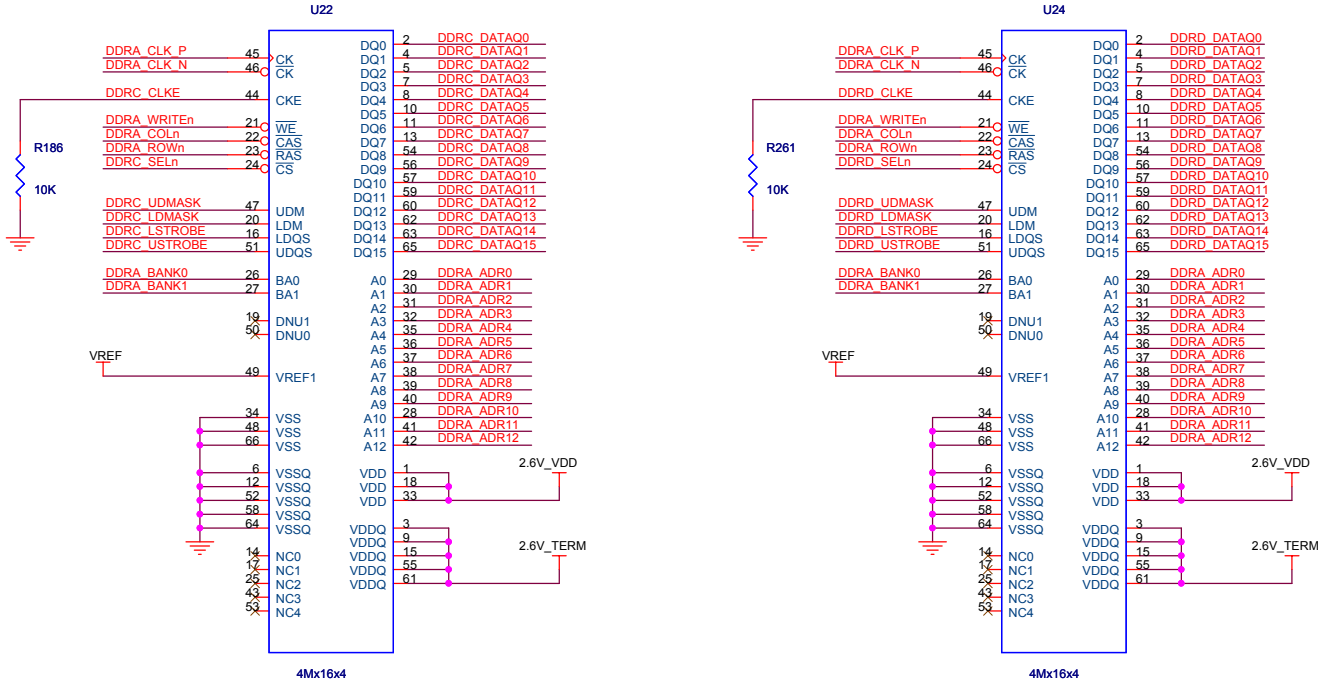
DDR I SDRAM Page 2



DDR I SDRAM SHARED SIGNALS INTERFACE

DDRA_ADR[12..0] — DDRA_ADR[12..0] 16,17
DDRA_BANK[1..0] — DDRA_BANK[1..0] 16,17
DDRA_CLK_P — DDRA_CLK_P 16
DDRA_CLK_N — DDRA_CLK_N 16
DDRA_WRITEn — DDRA_WRITEn 16,17
DDRA_COLn — DDRA_COLn 16,17
DDRA_ROWn — DDRA_ROWn 16,17

DDRC INTERFACE

DDRC_DATAQ[15..0] — DDRC_DATAQ[15..0] 20
DDRC_CLKE — DDRC_CLKE 20
DDRC_SELn — DDRC_SELn 20
DDRC_UDMASK — DDRC_UDMASK 20
DDRC_LDMASK — DDRC_LDMASK 20
DDRC_USTROBE — DDRC_USTROBE 20
DDRC_LSTROBE — DDRC_LSTROBE 20

DDRD INTERFACE

DDRD_DATAQ[15..0] — DDRD_DATAQ[15..0] 20
DDRD_CLKE — DDRD_CLKE 20
DDRD_SELn — DDRD_SELn 20
DDRD_UDMASK — DDRD_UDMASK 20
DDRD_LDMASK — DDRD_LDMASK 20
DDRD_USTROBE — DDRD_USTROBE 20
DDRD_LSTROBE — DDRD_LSTROBE 20

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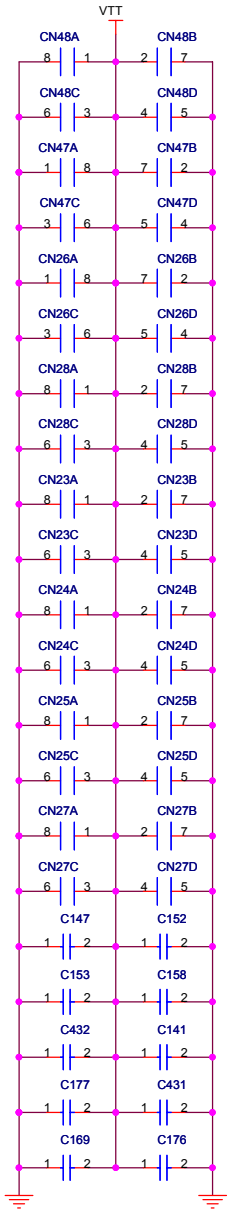
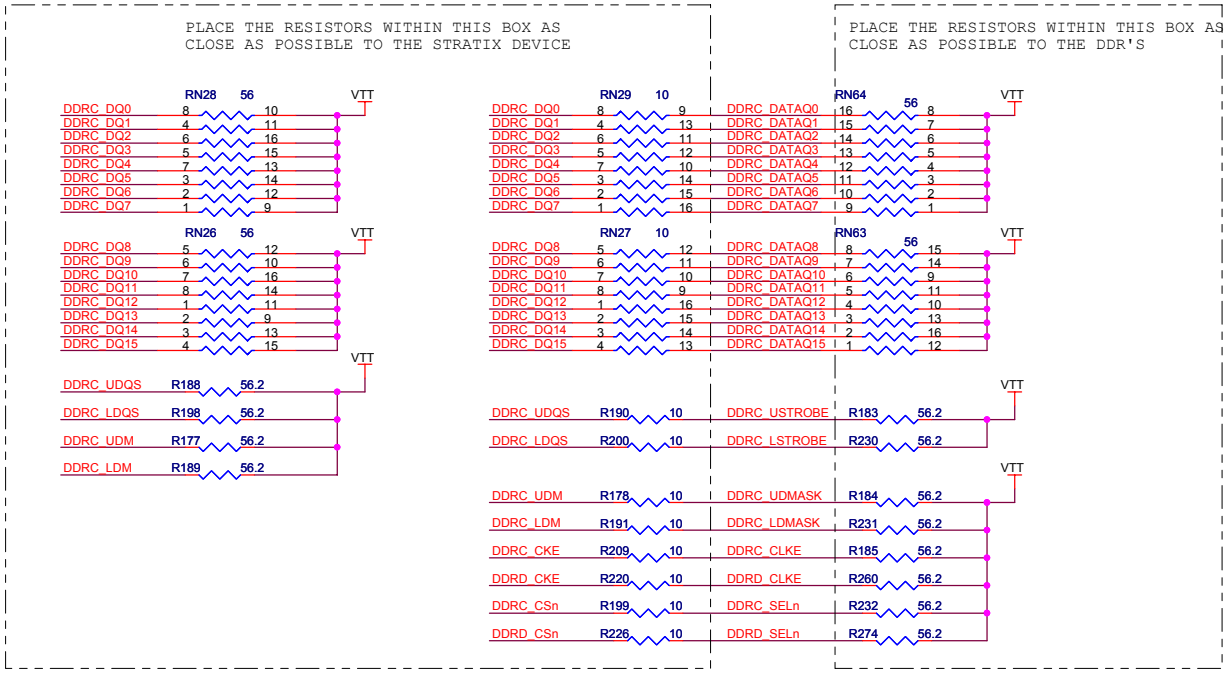
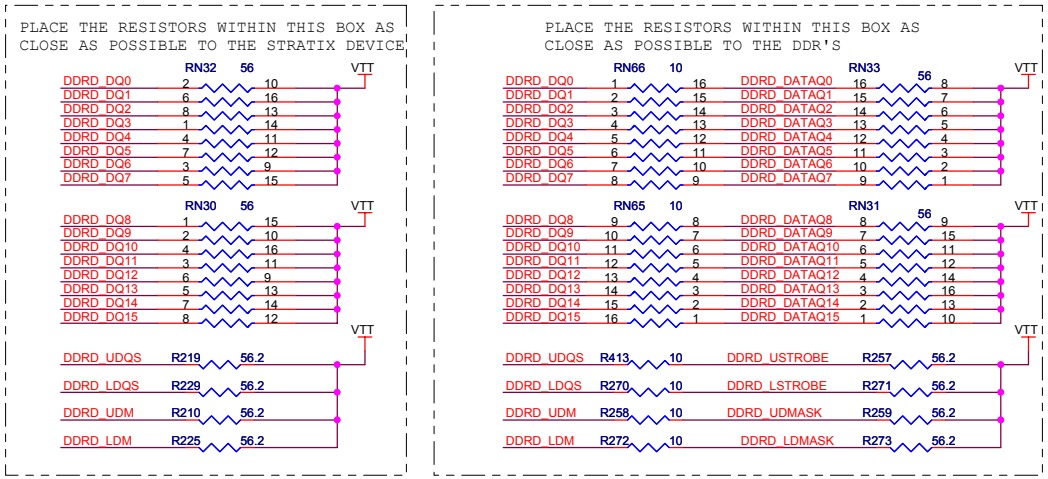
DDR I SDRAM C & D Terminations, Page 3







STRATIX SIGNALS

DDRC_UDM — DDRC_UDM 15, DDRC_LDM 15, DDRD_UDM 15, DDRD_LDM 15

DDRC_UDQS — DDRC_UDQS 15, DDRC_LDQS 15

DDRC_DQ[15..0] — DDRC_DQ[15..0] 15

DDRD_UDQS — DDRD_UDQS 15, DDRD_LDQS 15

DDRD_DQ[15..0] — DDRD_DQ[15..0] 15

DDRC_CKE — DDRC_CKE 15, DDRD_CKE 15

DDRC_CSn — DDRC_CSn 15, DDRD_CSn 15

DDR I SDRAM C & D SIGNALS

DDRC_UDMASK — DDRC_UDMASK 19, DDRC_LDMASK 19, DDRD_UDMASK 19, DDRD_LDMASK 19

DDRC_USTROBE — DDRC_USTROBE 19, DDRC_LSTROBE 19

DDRC_DATAQ[15..0] — DDRC_DATAQ[15..0] 19

DDRD_USTROBE — DDRD_USTROBE 19, DDRD_LSTROBE 19

DDRD_DATAQ[15..0] — DDRD_DATAQ[15..0] 19

DDRC_CLKE — DDRC_CLKE 19, DDRD_CLKE 19

DDRC_SELn — DDRC_SELn 19, DDRD_SELn 19

NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51 OR 51.1 OHM PULL UP RESISTOR.

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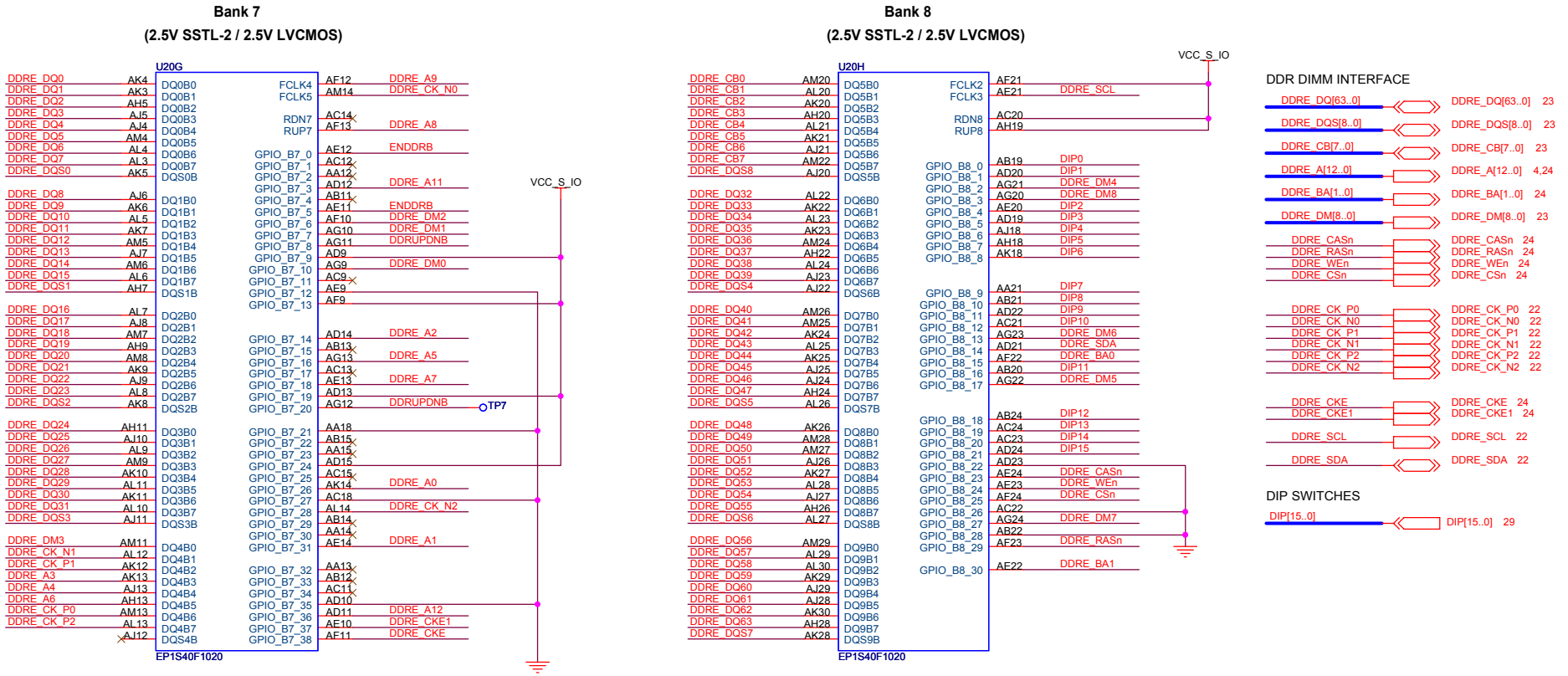
Stratix Bank 7, Bank 8



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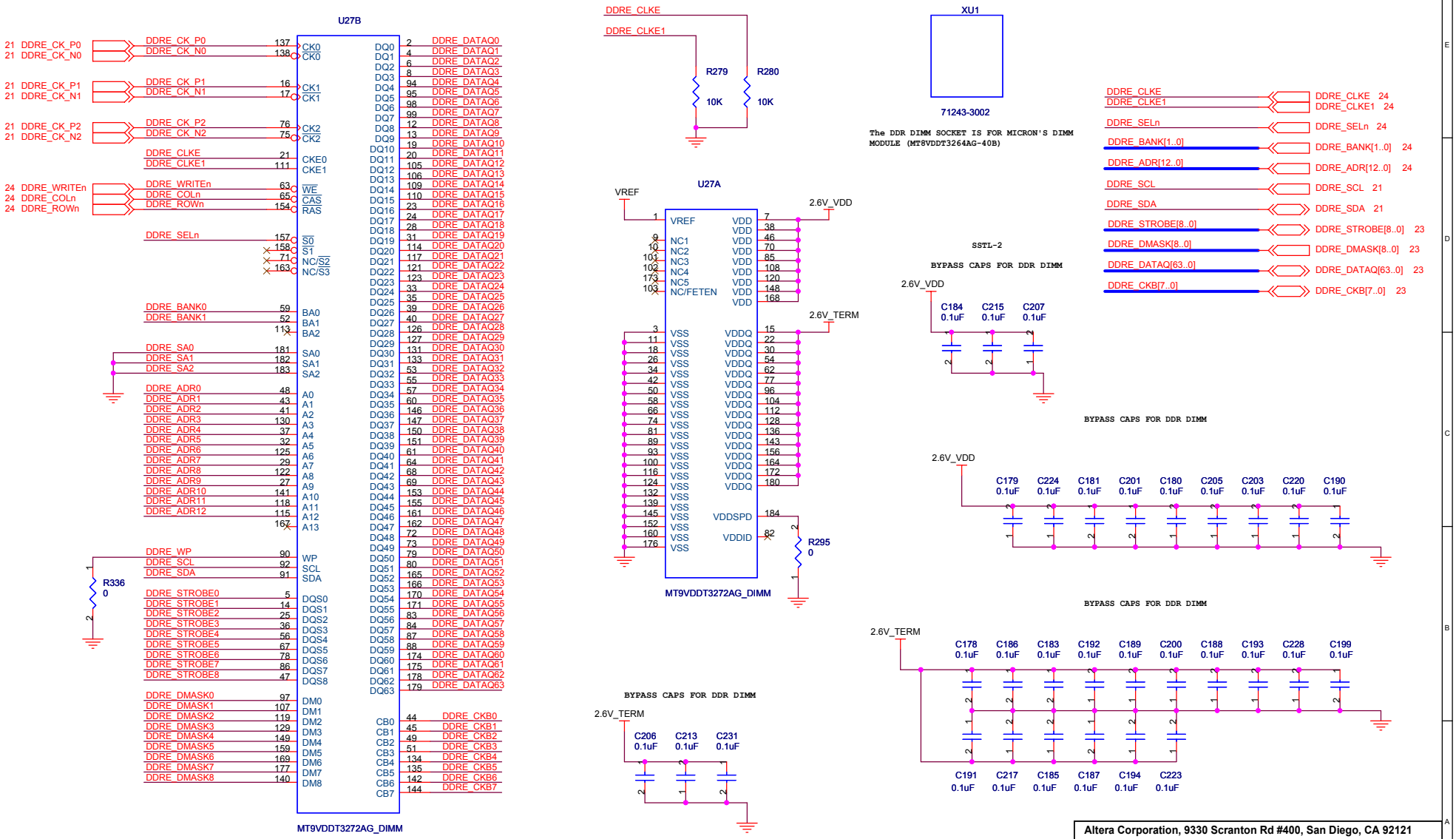
DDR I SDRAM DIMM



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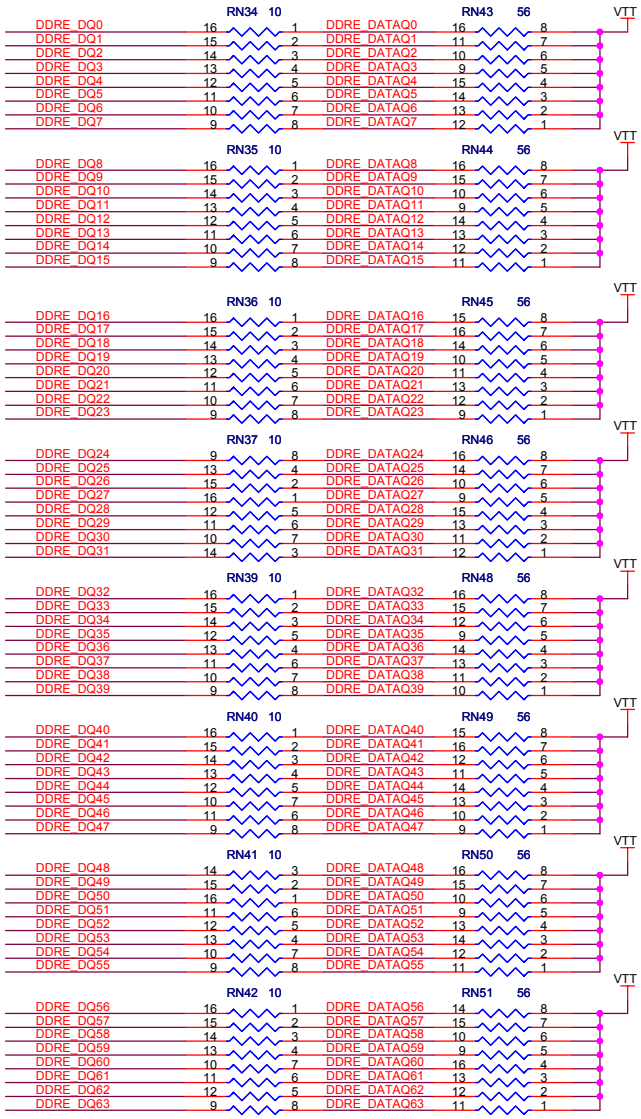
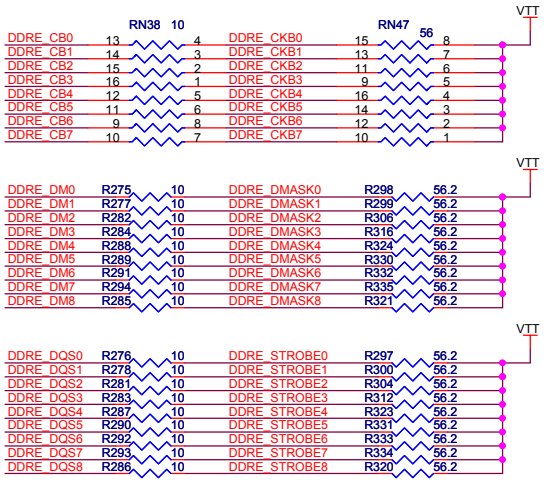
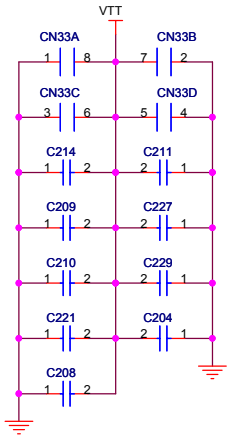
DDR I SDRAM DIMM Terminations Page 1

PLACE THESE COMPONENTS AS CLOSE
AS POSSIBLE TO THE DDR DIMM

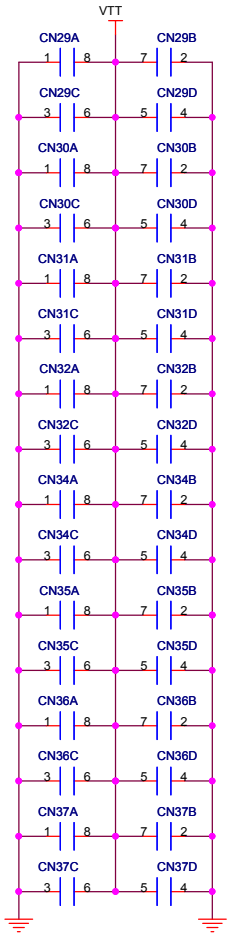






NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 56 OR 56.2 OHM PULL UP RESISTOR.



DDRE_CKB[7..0] DDRE_CKB[7..0] 22
DDRE_STROBE[8..0] DDRE_STROBE[8..0] 22
DDRE_DMASK[8..0] DDRE_DMASK[8..0] 22

DDRE_CB[7..0] DDRE_CB[7..0] 21
DDRE_DQS[8..0] DDRE_DQS[8..0] 21
DDRE_DM[8..0] DDRE_DM[8..0] 21

DDRE_DATAQ[63..0] DDRE_DATAQ[63..0] 22
DDRE_DQ[63..0] DDRE_DQ[63..0] 21

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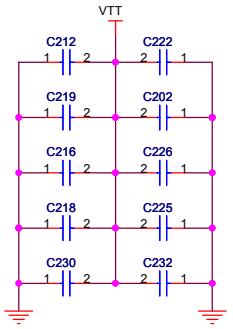
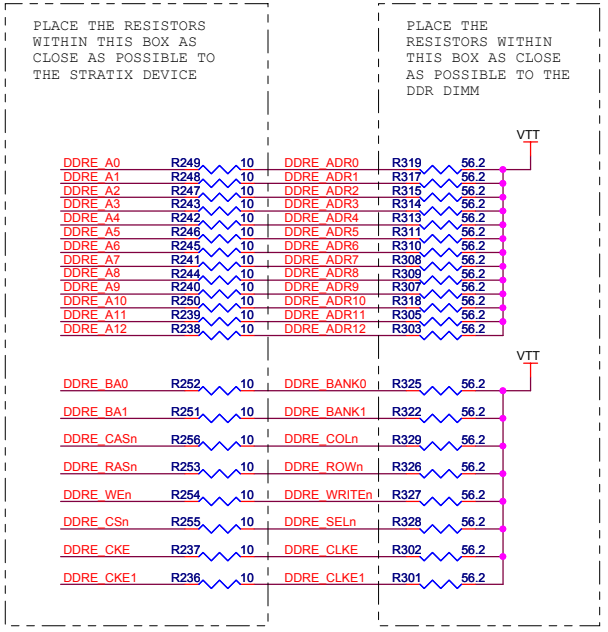
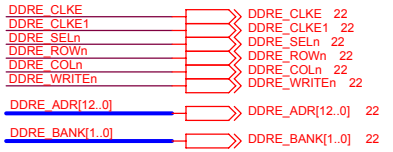


NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF

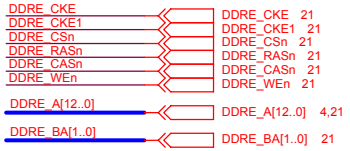
NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 56.2 OHM PULL UP RESISTOR.



STRATIX INTERFACE



DDR I SDRAM DIMM INTERFACE



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Stratix Bank 5, Bank 6

BANK 5
(3.3V LVTTL)

U20E

FSE_A0	F5	DIFFIO_RX45n	DIFFIO_TX45n	G7	FSE_D0
FSE_A1	E4	DIFFIO_RX45p	DIFFIO_TX45p	G8	FSE_D1
FSE_A2	E2	DIFFIO_RX46n	DIFFIO_TX46n	G6	FSE_D2
FSE_A3	E1	DIFFIO_RX46p	DIFFIO_TX46p	G5	FSE_D3
FSE_A4	F3	DIFFIO_RX47n	DIFFIO_TX47n	H8	FSE_D4
FSE_A5	F4	DIFFIO_RX47p	DIFFIO_TX47p	H7	FSE_D5
FSE_A6	G3	DIFFIO_RX48n	DIFFIO_TX48n	H5	FSE_D6
FSE_A7	G4	DIFFIO_RX48p	DIFFIO_TX48p	H6	FSE_D7
FSE_A8	F1	DIFFIO_RX49n	DIFFIO_TX49n	J7	FSE_D8
FSE_A9	F2	DIFFIO_RX49p	DIFFIO_TX49p	J8	FSE_D9
FSE_A10	H3	DIFFIO_RX50n	DIFFIO_TX50n	J5	FSE_D10
FSE_A11	H4	DIFFIO_RX50p	DIFFIO_TX50p	J6	FSE_D11
FSE_A12	G1	DIFFIO_RX51n	DIFFIO_TX51n	K8	FSE_D12
FSE_A13	G2	DIFFIO_RX51p	DIFFIO_TX51p	K7	FSE_D13
FSE_A14	H1	DIFFIO_RX52n	DIFFIO_TX52n	K5	FSE_D14
FSE_A15	H2	DIFFIO_RX52p	DIFFIO_TX52p	K6	FSE_D15
FSE_A16	J3	DIFFIO_RX53n	DIFFIO_TX53n	L6	FSE_D16
FSE_A17	J4	DIFFIO_RX53p	DIFFIO_TX53p	L7	FSE_D17
FSE_A18	K4	DIFFIO_RX54n	DIFFIO_TX54n	M6	FSE_D18
FSE_A19	K3	DIFFIO_RX54p	DIFFIO_TX54p	M7	FSE_D19
FSE_A20	J2	DIFFIO_RX55n	DIFFIO_TX55n	M8	FSE_D20
FSE_A21	J1	DIFFIO_RX55p	DIFFIO_TX55p	M9	FSE_D21
FSE_A22	L1	DIFFIO_RX56n	DIFFIO_TX56n	N10	FSE_D22
FSE_A23	K2	DIFFIO_RX56p	DIFFIO_TX56p	N9	FSE_D23
FSE_A24	M4	DIFFIO_RX57n/RDN5	DIFFIO_TX57n	N5	FSE_D24
FSE_A25	M5	DIFFIO_RX57p/RUP5	DIFFIO_TX57p	N6	FSE_D25
FSE_A26	L2	DIFFIO_RX58n	DIFFIO_TX58n	P9	FSE_D26
FLASH_RESETn	L3	DIFFIO_RX58p	DIFFIO_TX58p	P10	FSE_D27
FLASH_CEn	M2	DIFFIO_RX59n	DIFFIO_TX59n	N7	FSE_D28
FLASH_OEn	M3	DIFFIO_RX59p	DIFFIO_TX59p	N8	FSE_D29
FLASH_WEn	N3	DIFFIO_RX60n	DIFFIO_TX60n	P6	FSE_D30
FLASH_RDY_BSYn	N4	DIFFIO_RX60p	DIFFIO_TX60p	P5	FSE_D31
SRAM_BEn0	N1	DIFFIO_RX61n	DIFFIO_TX61n	R10	MAX_LED0
SRAM_BEn1	N2	DIFFIO_RX61p	DIFFIO_TX61p	R9	MAX_LED1
SRAM_BEn2	P3	DIFFIO_RX62n	DIFFIO_TX62n	R5	MAX_LED2
SRAM_BEn3	P4	DIFFIO_RX62p	DIFFIO_TX62p	R6	MAX_LED3
SRAM_CSn	P1	DIFFIO_RX63n	DIFFIO_TX63n	P7	MAX_LED4
SRAM_OEn	P2	DIFFIO_RX63p	DIFFIO_TX63p	P8	MAX_LED5
SRAM_WEn	R3	DIFFIO_RX64n	DIFFIO_TX64n	R7	MAX_LED6
ENET_SRDYn	R4	DIFFIO_RX64p	DIFFIO_TX64p	R8	MAX_LED7
ENET_VLBUSn	R1	DIFFIO_RX65n	DIFFIO_TX65n	P11	S_SMB_CLK
S_OVERTEMPn	R2	DIFFIO_RX65p	DIFFIO_TX65p	N11	S_SMB_DATA
S_ALERTn	T2	DIFFIO_RX66n	DIFFIO_TX66n	T11	REF_LOCK
	T1	DIFFIO_RX66p	DIFFIO_TX66p	R11	SCRUZ_CARDSELn

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BANK 6
(3.3V LVTTL)

U20F

PROTO1_IO39	U5	DIFFIO_RX67n	DIFFIO_TX67n	W11	ENET_AEN
PROTO1_IO38	U6	DIFFIO_RX67p	DIFFIO_TX67p	W12	ENET_ADSn
PROTO1_IO37	V2	DIFFIO_RX68n	DIFFIO_TX68n	Y11	ENET_BEn0
PROTO1_IO36	V1	DIFFIO_RX68p	DIFFIO_TX68p	Y12	ENET_BEn1
PROTO1_IO35	V4	DIFFIO_RX69n	DIFFIO_TX69n	AB10	ENET_BEn2
PROTO1_IO34	V3	DIFFIO_RX69p	DIFFIO_TX69p	AA11	ENET_BEn3
PROTO1_IO33	W2	DIFFIO_RX70n	DIFFIO_TX70n	W8	ENET_CYCLEn
PROTO1_IO32	W1	DIFFIO_RX70p	DIFFIO_TX70p	W7	ENET_DATACSn
PROTO1_IO31	W4	DIFFIO_RX71n	DIFFIO_TX71n	V8	ENET_INTRQ0
PROTO1_IO30	W3	DIFFIO_RX71p	DIFFIO_TX71p	V7	ENET_IOCHRDY
PROTO1_IO29	Y2	DIFFIO_RX72n	DIFFIO_TX72n	V5	ENET_IORn
PROTO1_IO28	Y1	DIFFIO_RX72p	DIFFIO_TX72p	V6	ENET_IOWn
PROTO1_IO27	Y4	DIFFIO_RX73n	DIFFIO_TX73n	V9	ENET_LCLK
PROTO1_IO26	Y3	DIFFIO_RX73p	DIFFIO_TX73p	V10	ENET_LDEVn
PROTO1_IO25	AA3	DIFFIO_RX74n	DIFFIO_TX74n	W10	
PROTO1_IO24	AA2	DIFFIO_RX74p	DIFFIO_TX74p	W9	ENET_RDYRTNn
PROTO1_IO23	AB3	DIFFIO_RX75n	DIFFIO_TX75n	Y10	ENET_W_Rn
PROTO1_IO22	AB2	DIFFIO_RX75p	DIFFIO_TX75p	Y9	RS232A_TXD
PROTO1_IO21	AA4	DIFFIO_RX76n/RDN6	DIFFIO_TX76n	W5	RS232A_RTS
PROTO1_IO20	AA5	DIFFIO_RX76p/RUP6	DIFFIO_TX76p	W6	RS232A_RXD
PROTO1_IO19	AC2	DIFFIO_RX77n	DIFFIO_TX77n	Y7	RS232A_CTS
PROTO1_IO18	AB1	DIFFIO_RX77p	DIFFIO_TX77p	Y8	RS232B_TXD
PROTO1_IO17	AD2	DIFFIO_RX78n	DIFFIO_TX78n	Y5	RS232B_RTS
PROTO1_IO16	AD1	DIFFIO_RX78p	DIFFIO_TX78p	Y6	RS232B_RXD
PROTO1_IO15	AD3	DIFFIO_RX79n	DIFFIO_TX79n	AA9	RS232B_CTS
PROTO1_IO14	AD4	DIFFIO_RX79p	DIFFIO_TX79p	AA8	DIG_1_DP
PROTO1_IO13	AC3	DIFFIO_RX80n	DIFFIO_TX80n	AA6	DIG_1_G
PROTO1_IO12	AC4	DIFFIO_RX80p	DIFFIO_TX80p	AA7	DIG_1_F
PROTO1_IO11	AE2	DIFFIO_RX81n	DIFFIO_TX81n	AB7	DIG_1_E
PROTO1_IO10	AE1	DIFFIO_RX81p	DIFFIO_TX81p	AB6	DIG_1_D
PROTO1_IO9	AE4	DIFFIO_RX82n	DIFFIO_TX82n	AC7	DIG_1_C
PROTO1_IO8	AE3	DIFFIO_RX82p	DIFFIO_TX82p	AC8	DIG_1_B
PROTO1_IO7	AF2	DIFFIO_RX83n	DIFFIO_TX83n	AC5	DIG_1_A
PROTO1_IO6	AF1	DIFFIO_RX83p	DIFFIO_TX83p	AC6	DIG_2_DP
PROTO1_IO5	AF4	DIFFIO_RX84n	DIFFIO_TX84n	AD8	DIG_2_G
PROTO1_IO4	AF3	DIFFIO_RX84p	DIFFIO_TX84p	AD7	DIG_2_F
PROTO1_IO3	AG1	DIFFIO_RX85n	DIFFIO_TX85n	AE6	DIG_2_E
PROTO1_IO2	AG2	DIFFIO_RX85p	DIFFIO_TX85p	AE5	DIG_2_D
PROTO1_IO1	AG4	DIFFIO_RX86n	DIFFIO_TX86n	AD6	DIG_2_C
PROTO1_IO0	AG3	DIFFIO_RX86p	DIFFIO_TX86p	AD5	DIG_2_B
	AG7	DIFFIO_RX87n	DIFFIO_TX87n	AE7	DIG_2_A
PB0	AG8	DIFFIO_RX87p	DIFFIO_TX87p	AE8	PROTO1_IO40
PB1	AH2	DIFFIO_RX88n	DIFFIO_TX88n	AF5	
PB2	AH1	DIFFIO_RX88p	DIFFIO_TX88p	AF6	
SYS_RESETn	AG5	DIFFIO_RX89n	DIFFIO_TX89n	AF8	CPLD_USER0
	AH4	DIFFIO_RX89p	DIFFIO_TX89p	AF7	CPLD_USER1
	AB9	GPIO_B6_0	GPIO_B6_1	AC10	

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3.3V_S_IO

SEVEN SEGMENT DISPLAY

DIG_1_DP	DIG_1_DP 28
DIG_1_G	DIG_1_G 28
DIG_1_F	DIG_1_F 28
DIG_1_E	DIG_1_E 28
DIG_1_D	DIG_1_D 28
DIG_1_C	DIG_1_C 28
DIG_1_B	DIG_1_B 28
DIG_1_A	DIG_1_A 28
DIG_2_DP	DIG_2_DP 28
DIG_2_G	DIG_2_G 28
DIG_2_F	DIG_2_F 28
DIG_2_E	DIG_2_E 28
DIG_2_D	DIG_2_D 28
DIG_2_C	DIG_2_C 28
DIG_2_B	DIG_2_B 28
DIG_2_A	DIG_2_A 28

S_SMB_CLK	S_SMB_CLK 4
S_SMB_DATA	S_SMB_DATA 4
REF_LOCK	REF_LOCK 7
SCRUZ_CARDSELn	SCRUZ_CARDSELn 26
S_OVERTEMPn	S_OVERTEMPn 4
S_ALERTn	S_ALERTn 4

SRAM INTERFACE

SRAM_BEn[3..0]	SRAM_BEn[3..0] 31
SRAM_CSn	SRAM_CSn 31
SRAM_OEn	SRAM_OEn 31
SRAM_WEn	SRAM_WEn 31

CPLD INTERFACE

CPLD_USER[1..0]	CPLD_USER[1..0] 6

SHARED BUS AND FLASH INTERFACE

FSE_D[31..0]	FSE_D[31..0] 6,27,31
FSE_A[26..0]	FSE_A[26..0] 6,27,31
FLASH_CEn	FLASH_CEn 6,31
FLASH_OEn	FLASH_OEn 6,31
FLASH_WEn	FLASH_WEn 6,31
FLASH_RDY_BSYn	FLASH_RDY_BSYn 6,31
FLASH_RESETn	FLASH_RESETn 6,31

DEBUG PORT

PROTO1_IO[40..0]	PROTO1_IO[40..0] 26

RS-232 INTERFACE

RS232A_TXD	RS232A_TXD 30
RS232A_CTS	RS232A_CTS 30
RS232A_RXD	RS232A_RXD 30
RS232A_RTS	RS232A_RTS 30
RS232B_TXD	RS232B_TXD 30
RS232B_CTS	RS232B_CTS 30
RS232B_RXD	RS232B_RXD 30
RS232B_RTS	RS232B_RTS 30

LED, DIPSWITCH INTERFACE

MAX_LED[7..0]	MAX_LED[7..0] 6
PB[2..0]	PB[2..0] 29
SYS_RESETn	SYS_RESETn 6,26,29

ETHERNET/MAC INTERFACE

ENET_BEn[3..0]	ENET_BEn[3..0] 27
ENET_ADSn	ENET_ADSn 27
ENET_AEN	ENET_AEN 27
ENET_IORn	ENET_IORn 27
ENET_IOWn	ENET_IOWn 27
ENET_IOCHRDY	ENET_IOCHRDY 27
ENET_LDEVn	ENET_LDEVn 27
ENET_CYCLEn	ENET_CYCLEn 27
ENET_INTRQ0	ENET_INTRQ0 27
ENET_RDYRTNn	ENET_RDYRTNn 27
ENET_DATACSn	ENET_DATACSn 27
ENET_W_Rn	ENET_W_Rn 27
ENET_LCLK	ENET_LCLK 27
ENET_SRDYn	ENET_SRDYn 27
ENET_VLBUSn	ENET_VLBUSn 27

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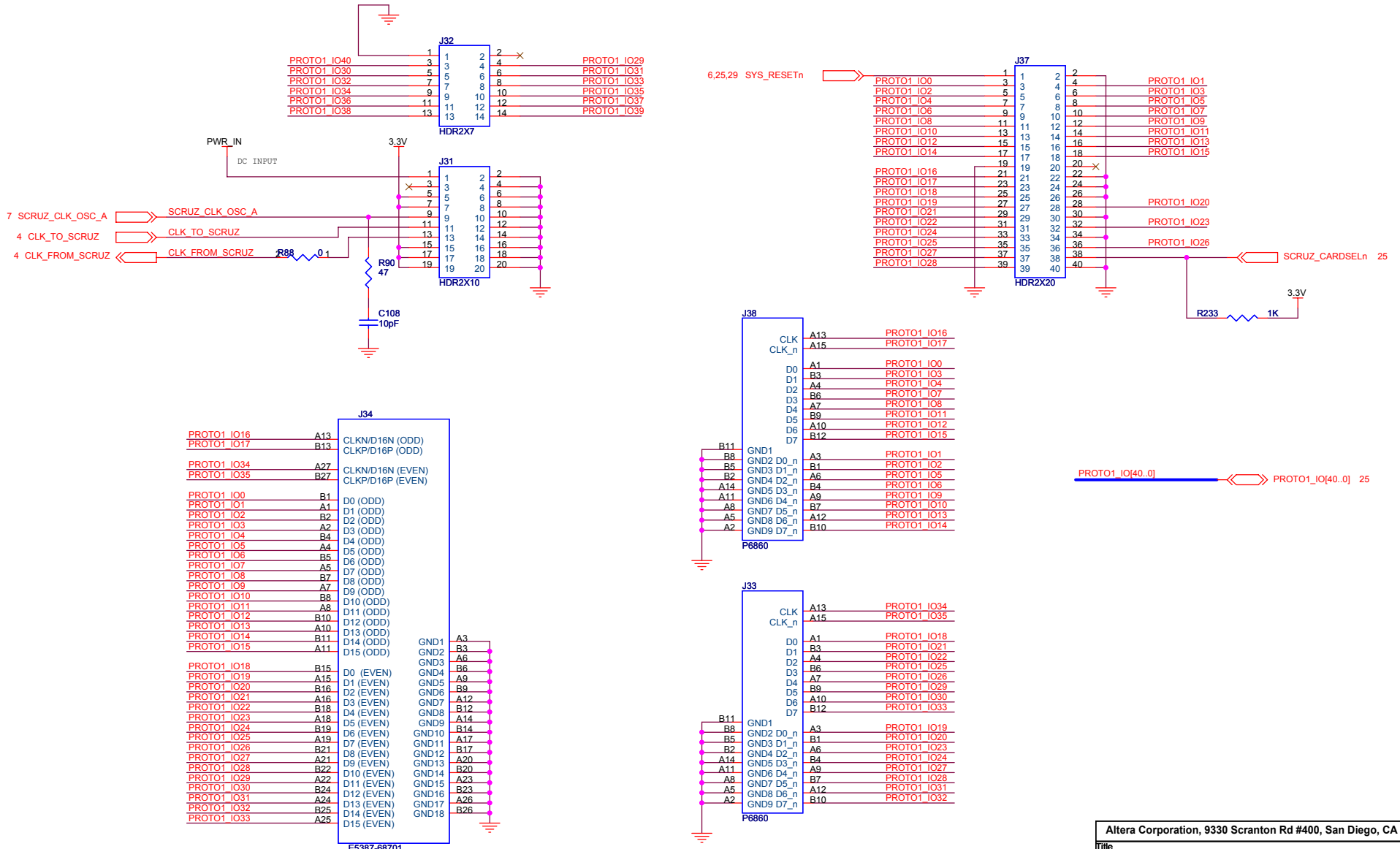
Debug Proto Headers



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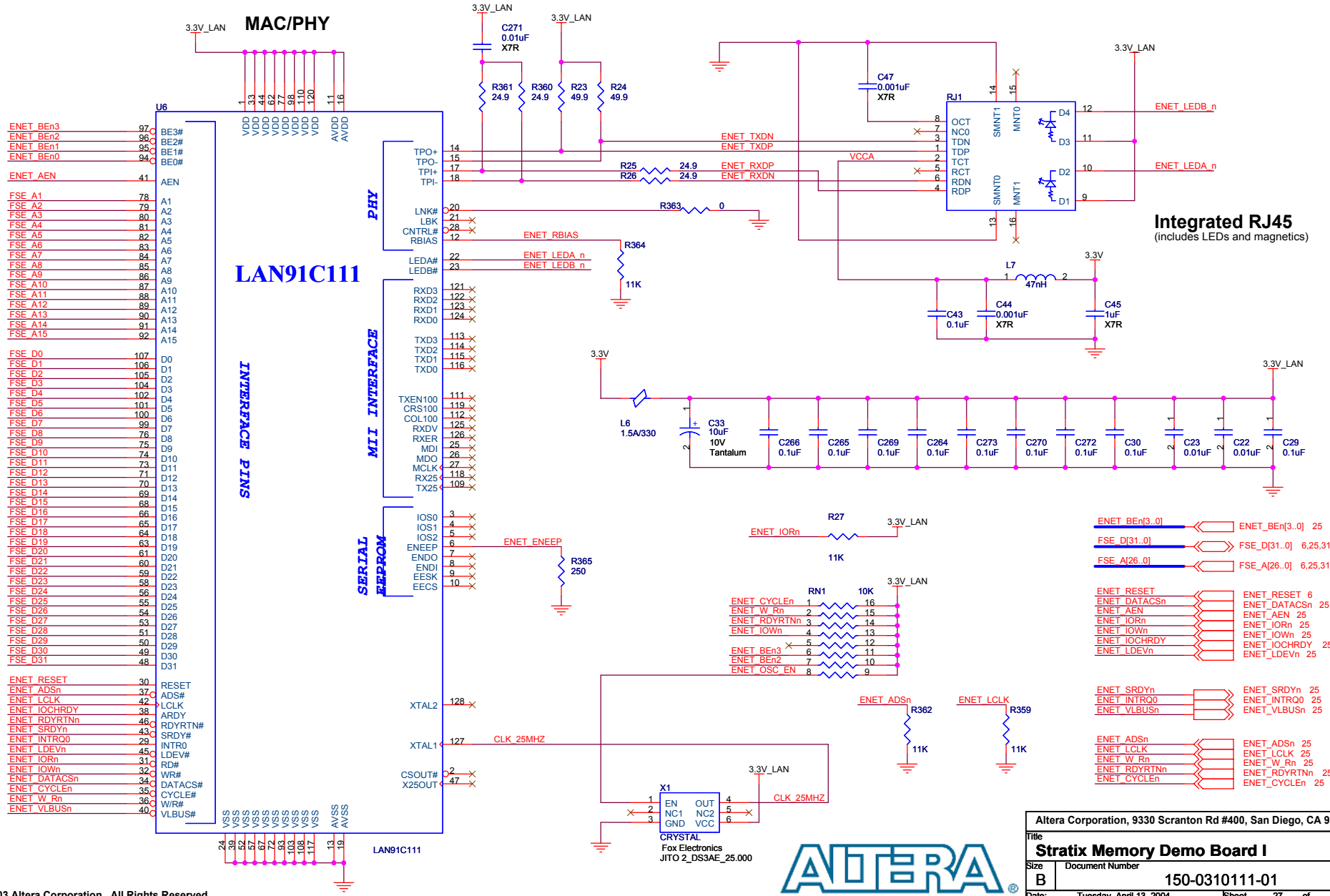
10/100 Ethernet Interface



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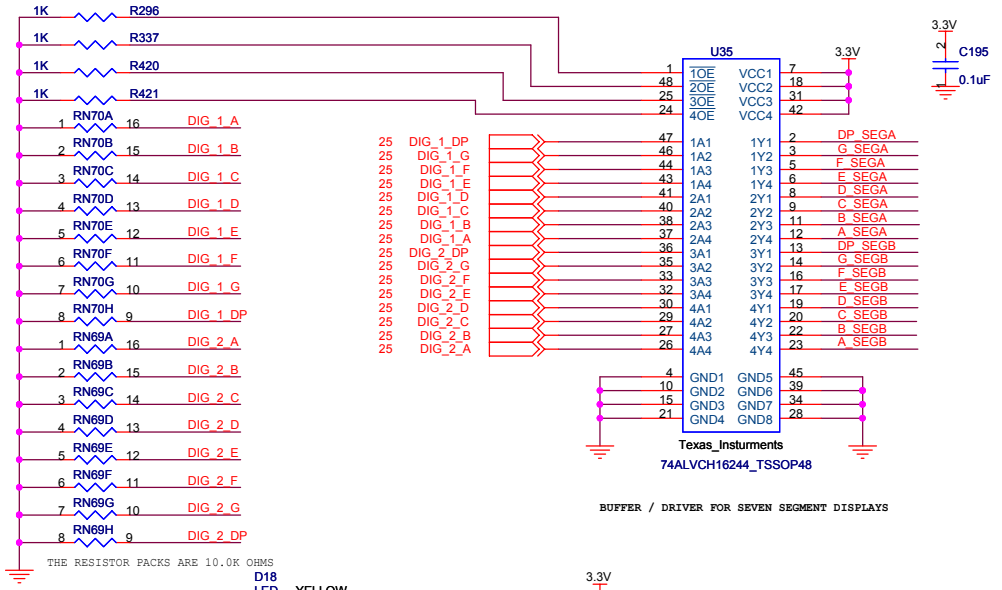
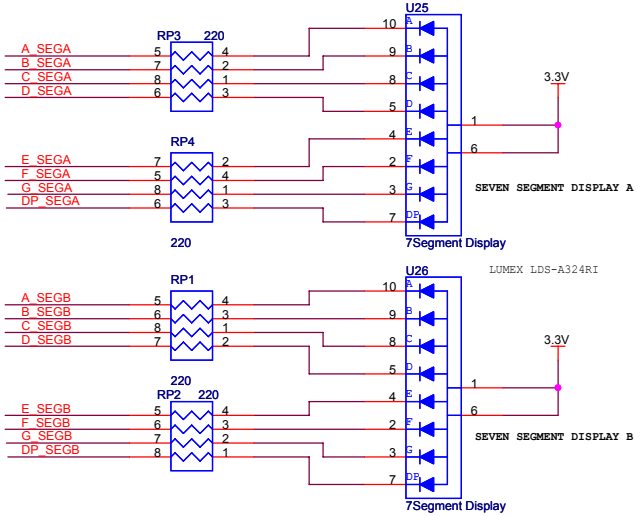
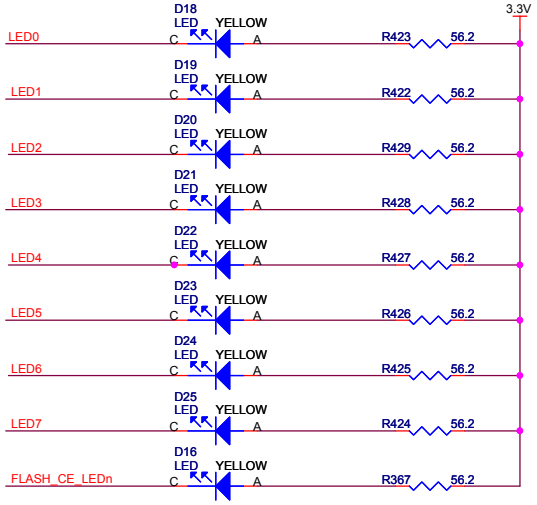
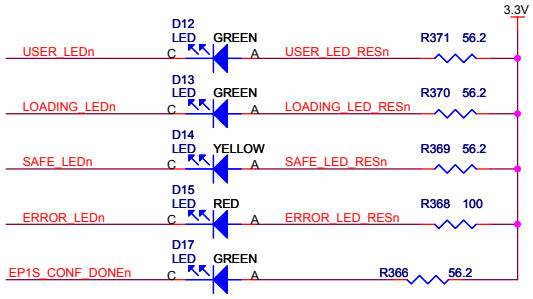
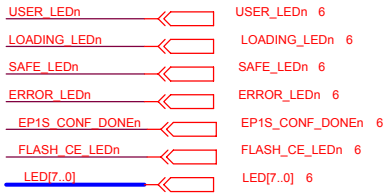
Seven Segment Displays & LEDs











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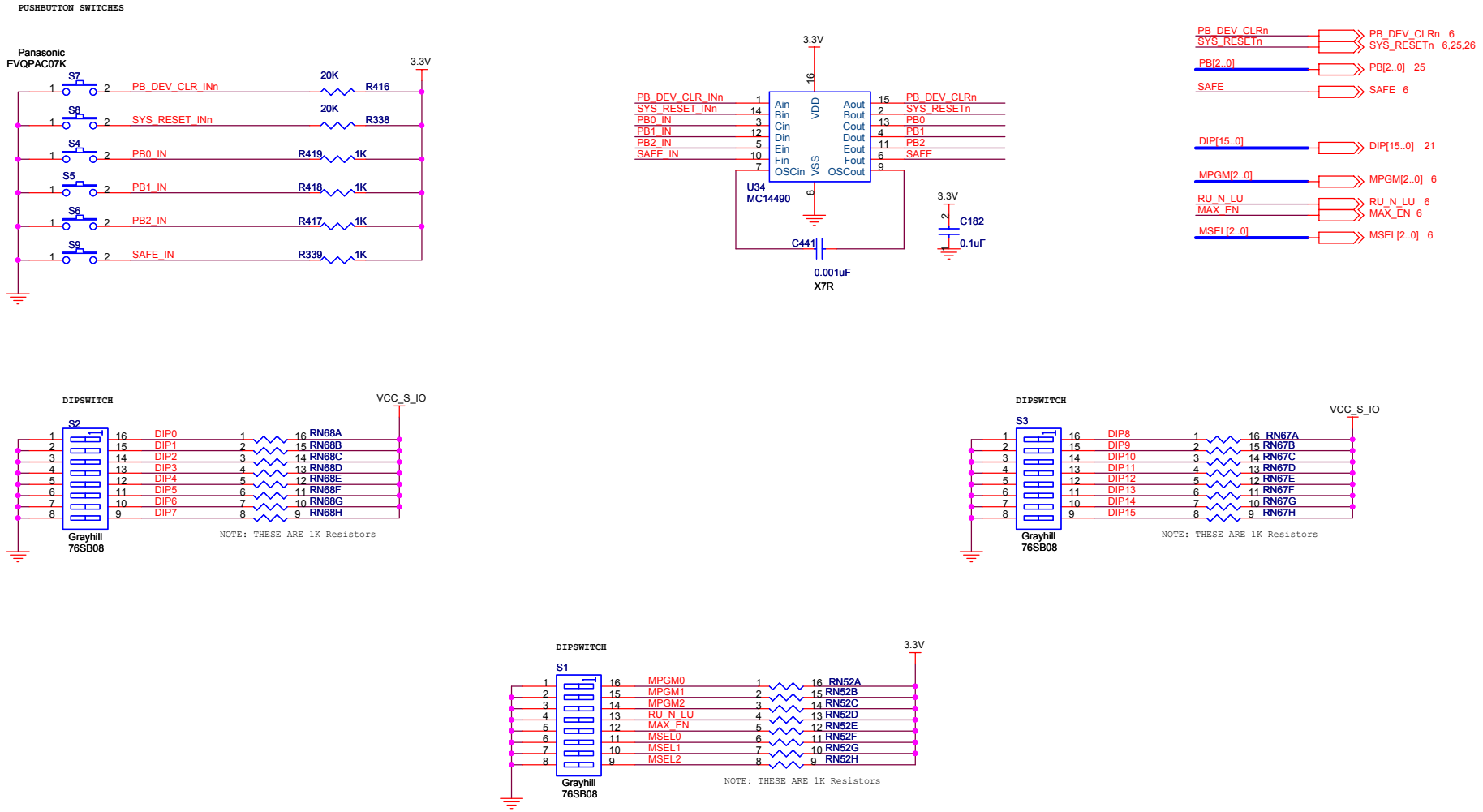
Push Buttons / Dip Switches



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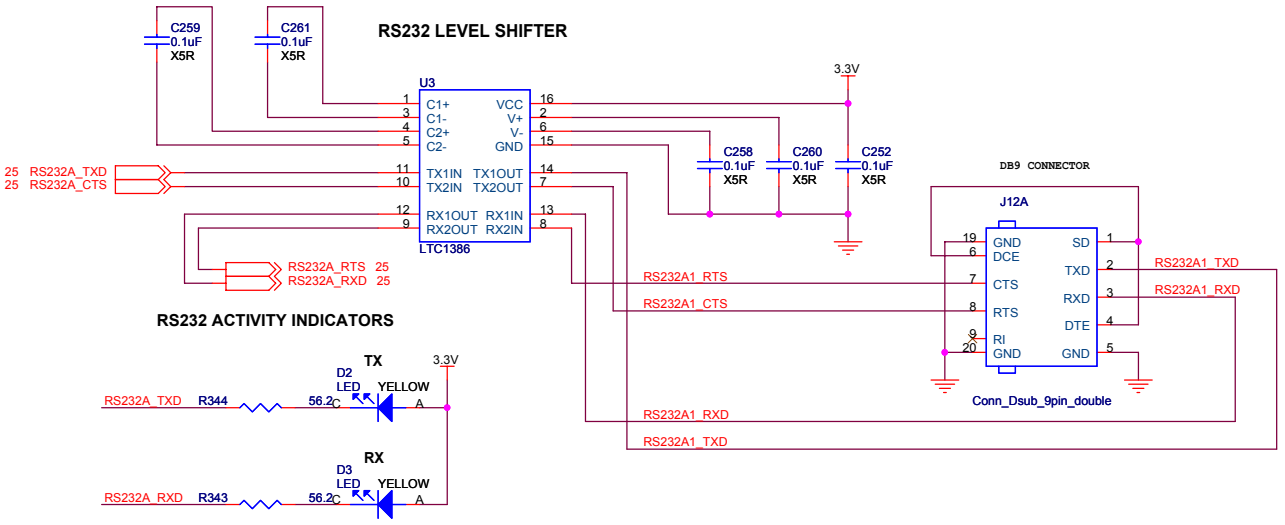
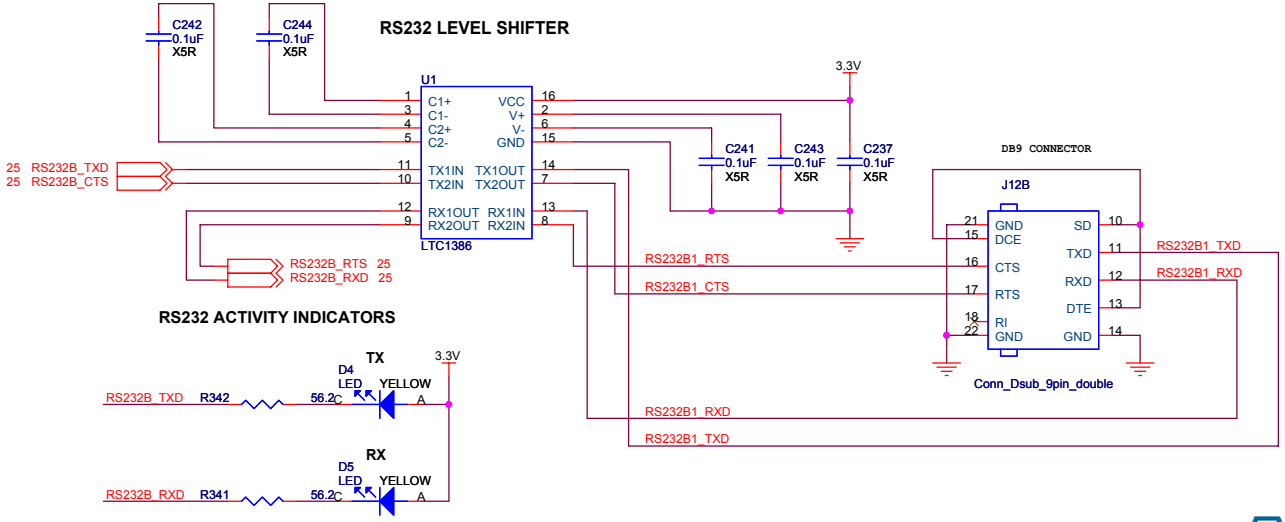
RS-232

PORT A



RS232 ACTIVITY INDICATORS

PORT B



RS232 ACTIVITY INDICATORS

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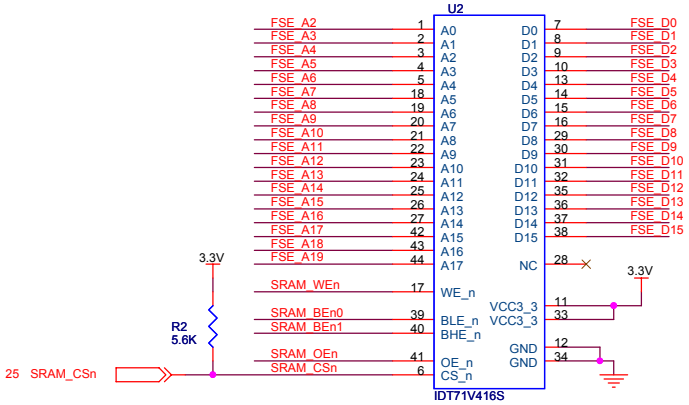
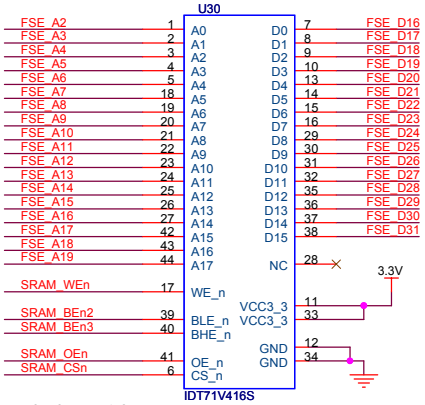
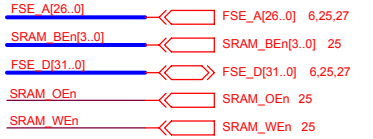
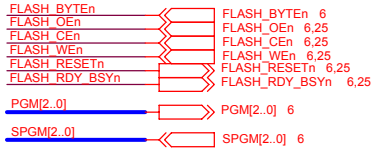
SRAM and Flash Memory

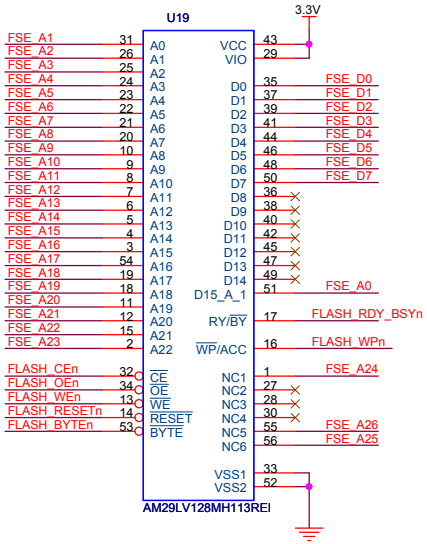


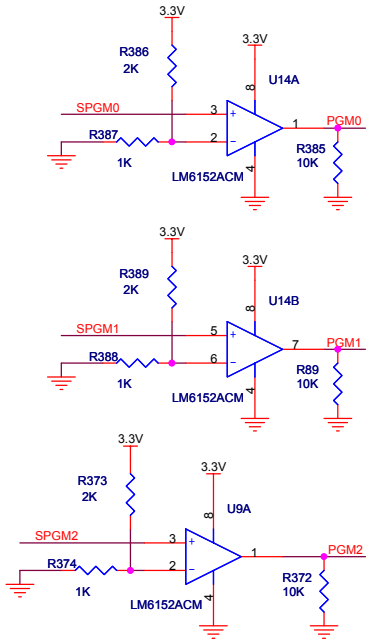


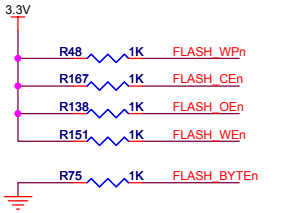


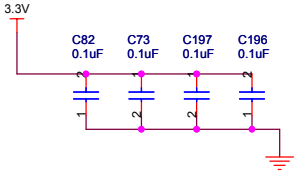


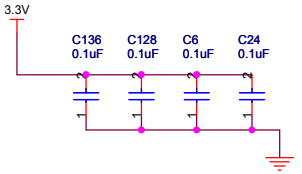
One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM











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