The Programmable Solutions Company®

Stratix™ Memory Board 1 Rev B

User Guide
Rev 0.1

High Speed / End Applications Team
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Altera Confidential

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1 Introduction

This document describes the diagnostic test designs included with revision B of the Stratix Memory Board I (SMBI). It also covers the hardware and software requirements for running the designs.

The SMB1 is a demonstration board designed to showcase high-speed memories (DDR-I and RLDRAM-II) with Altera's current high end device, Stratix, using Altera developed Intellectual Property (IP). The main function of this board is to provide in-house hardware verification and demonstration platforms for the Stratix RLDRAM-II and DDR-I (non-DQS mode and DQS mode) memory controller IP.

For detailed information on the SMB1 please refer to the SMB1 board datasheet.

1.1 Hardware requirements

- PC – A medium performance personal computer with standard features and Windows XP installed is used as the host system. It serves as the user interface to run the designs and stores all of the software and files required.
- Programming Device – A programming device is required to program/configure the Altera devices on the SMB1. A Byte Blaster with a parallel cable interface is the standard device. The SMB1 is also compatible with a USB Blaster with USB cable interface. The USB Blaster provides a faster download speed.
- Power supply – The SMB1 uses an IBM ThinkPad laptop compatible power supply as the main power source for the board. It produces a 16 volt DC output and supplies 60W of power.
- RS 232 cable – An RS232 serial cable is required for communication between the host system and the board.
- Ethernet connection w/cable – An Ethernet connection and cable is required to verify the Ethernet port on the SMB1. As the design is currently configured, the SMB1 attempts to use DHCP to acquire an Ethernet address.
- DDR DIMM – Use a 256 MByte PC3200 200 MHz ECC DDR 1 module such as Micron part number MT9VDDT3272AG-40B or equivalent.

1.2 Software requirements

- Quartus II 4.0 – Quartus II 4.0 SP1 is the assumed software environment. This provides the programming software used to configure the Altera devices.
- Board Test System (BTS) code – The BTS code is a collection of Tool Control Language (TCL) scripts, batch files and compiled C programs used to automate the testing process.
- .sof files – Several .sof and .pof files are used to configure the Altera devices on the SMB1 to run the design.

2 Configuration

2.1 Board switch and jumper settings and other setup

SMB1 requires a number of jumpers, switch settings, and other hardware setup before testing should begin. See figure 1 for the location of the switches and jumpers. See figure 2 for the location of cables and test card. This work should be performed **before** applying power.

Table 2-1 DIP Switch settings		
DIP Switch	**Name**	**Setting**
S1 - 8	MSEL2	Closed
S1 – 7	MSEL1	Closed
S1 – 6	MSEL0	Closed
S1 – 5	MAX_EN	Open
S1 – 4	RU_N_LU	Open
S1 – 3	MPGM2	Closed
S1 – 2	MPGM1	Closed
S1 – 1	MPGM0	Closed
S2 – 1 to 8	USER DIP 0 -7	Closed
S3 – 1 to 8	USER DIP 8 – 15	Closed

Table 2-2 Other Switch Settings			
SW1 – POWER	SW2	SW3 - CLK_EN	SW4
OFF	DDR	ENABLE	S/M

Table 2-3 Jumper settings								
J15	J19,J22	J20,J23	J21,J24	J28	J29	J35	J42	J43
Off*	J22p1–J19p2	J23p1-J20p2	J24p1-J21p2	p1-p2	p1-p2	p1-p2	p1-p2	Off*

* Off means no jumper installed

- NIOS Proto1 test card w/ modified resister value – A NIOS Proto1 test card is used to help verify the Proto 1 interface. It must have a resistor value modified before the card is connected to a powered up SMB2 or the resistor will overheat and fail. The resistor is R8. The new value needs to be approximately 4-5k Ohms.
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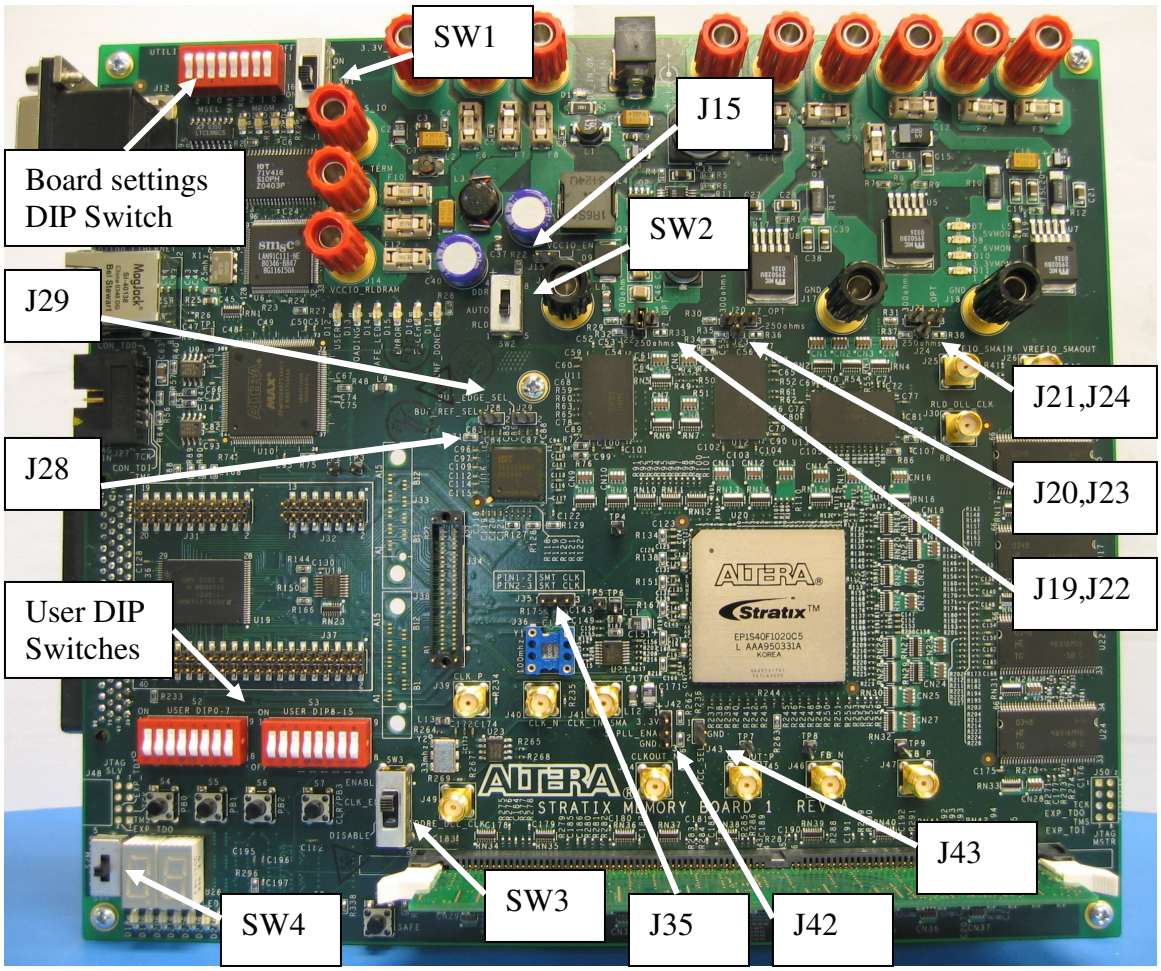


Figure 1 Switch and Jumper Locations

DDR DIMM – Insert the DDR DIMM carefully if needed. Try not to flex the board if possible.

RS232 Serial Cable – Connect one end of the serial cable to the COM 1 port on the PC and the other to upper RS232 connector (RS232 A).

Parallel cable - Connect one end of the parallel cable to the Parallel port on the PC and the other end to the parallel port interface of the Byte Blaster cable. Connect the other end of the Byte Blaster cable to the JTAG connector on the SMB1.

Ethernet cable – Connect one end of the Ethernet cable to an active Ethernet port and the other end to the RJ45 connector on the SMB1.

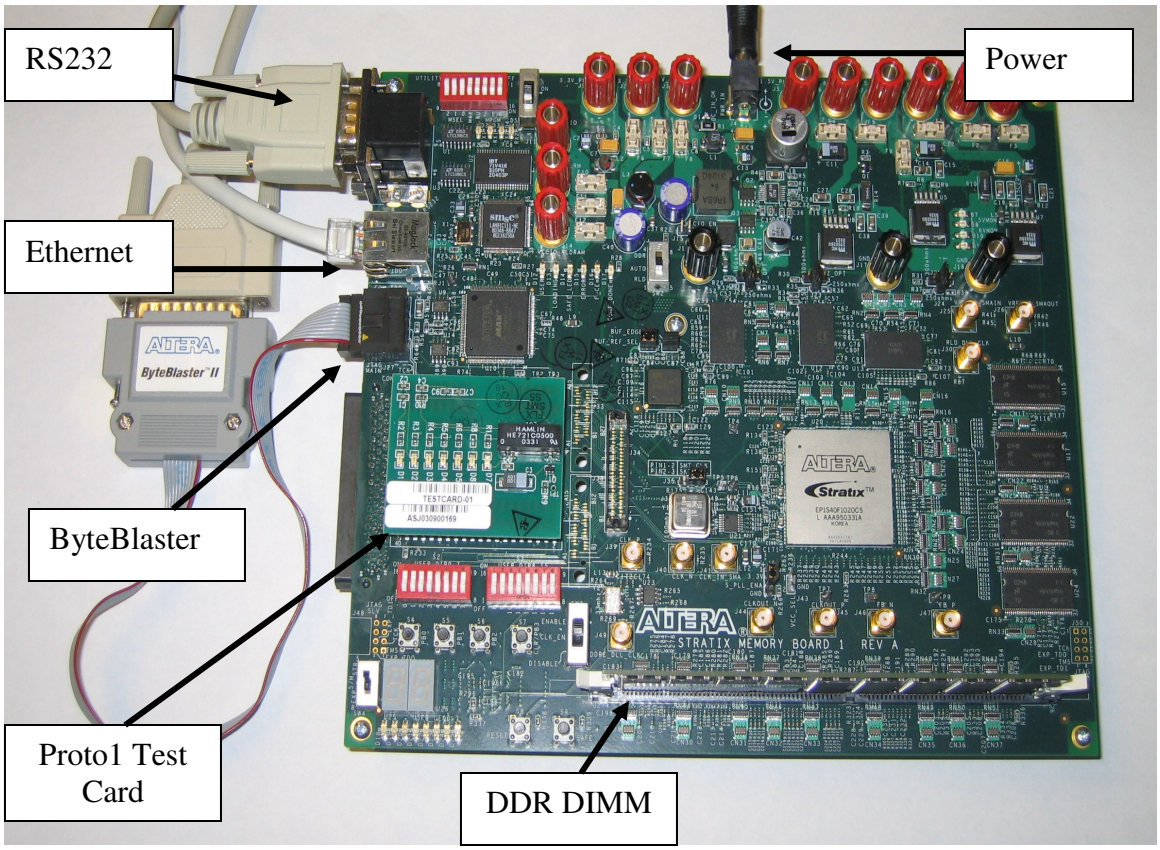


Figure 2 SMB1 with cables

2.2 Power up procedure

Insert the power connector into the socket. Move the power switch to the ON position. A bright blue LED (D1) next to the power connector and several LEDs on the SMB1 should light up. Verify that the voltage monitor LEDS are lit. D7 for 1.5V and D10 for 3.3V are always on. D8 is lit when the 2.6 Volt power supply is active and D11 is for 1.8 Volts.

Move SW2 from DDR to RLD. LED D11 (1.8VMON) goes on and LED D8 (2.6VMON) goes off. Move SW2 back to DDR.

3 Pre Loaded Diagnostic Tests

The User IO and NIOS stamp functions are exercised using a prototype of the Board Test System (BTS). This design is the "safe" image that is loaded by pressing the SAFE button. This loads a NIOS based system design that will communicate with the host using a RS232 link. The user interface is TCL based. The GUI has several "pages" for the various features that are tested.

The memory tests are hardware based at this point and are stored as pages in the on-board flash memory. These are loaded by setting the MPGM DIP switch settings then pressing pushbutton S8 (RESET). The memory tests consist of a state machine

that writes PRBS data to the memory device at max speed then reads back the data and compares it to an expected value. If an error is detected an LED will go on or off as indicated in the detailed instruction for that test. The data is written to the full address range of the device before it is read back. Each time the full write then read cycle is completed, it is considered one test. The designs have counters that keep track of how many times the test has cycled and reports the two least significant digits in hex format on the 7 segment displays. The DDR designs run a finite number of times, up to 1K, controlled by entering a value using the user DIP switches 6 – 15. If 0 is entered the test will run 64K times. This can take several hours. For the RLDRAM designs the tests will run forever. The count value is hard coded to stop at 80. This indicates that 128 cycles/tests have been run.

3.1 User IO

- Run the batch file by double clicking on the file name: smb1_bts_run.bat. This starts downloading the NIOS programming and, when finished, loads the user interface GUI.
- Wait until the Board Test System GUI window opens:
- Use the BTS pulldown menu to open the COM1 port.
  BTS ->Open Port -> RS232 Com1
- Click on the UserIO page.
- Click on the Enable Polling button.
- You can vary the Seven Segment displays by slowly moving the slider using your mouse and verifying that the displays on the board match the digits displayed in the GUI.
- You can set the User LEDs by pressing the LEDs On button followed by the LEDs Off button in the GUI. Then click on the LED checkboxes one at a time while verifying the User LEDs on the board turn off and on.
- You can check the DIP switches are working by turning them all open then back to closed while watching the switch indicators in the GUI.
- Check the User Push Buttons by pressing switches S4, S5 and S6 (PB0, PB1 and PB2) while watching the status in the GUI. Do not press S7 (PB3) as this will reset the system. If you accidentally press this button you will need to exit the GUI and rerun the BTS run file.

3.2 NIOS Stamp features

The next section demonstrates the NIOS stamp features. This will exercise the onboard Proto 1 IO port, SRAM, Flash Memory, and Ethernet port. If the GUI is still running you can just click on the NIOS Stamp page otherwise you will need to restart the system from the beginning.

- The **Proto1 IO** test is designed to work with the Proto 1 test card developed by the NIOS group. The NIOS Proto1 test card needs a resister value modified before the card is connected to a powered up SMB1 or a resistor

will overheat and fail. The resistor is R8. The new value needs to be approximately 4k-5k Ohms.

- Click on the Start Test button in the Santa Cruz IO section.
  - Test Results should show
    Starting Santa Cruz Test
    Santa Cruz IO Test Complete

- Click on the Start Tests button in the **SRAM** section. This will run the "Walking Ones on Address" and "Walking Ones on Data" tests.
  - Test Results should show
    Starting Test
    Walking Ones on Data
    Walking Ones on Address
    There were 0 error(s).
    Test Complete

- Warning: Running the **flash** tests will corrupt the designs in flash memory. You will have to reprogram the flash to the factory image after running these tests. You can click on the Start Tests button in the Flash section. This will run the "Walking Ones on Address" and "Walking Ones on Data" and Flash Erase tests. This may take 3 - 4 minutes to finish.
  Verify the tests complete without errors.
  - Test Results should show
    Starting Test
    Walking Ones on Data
    Starting Flash Erase of sector offset 0
    Finished Flash Erase
    Walking Ones on Address
    Starting Flash Erase
    Test Complete

- To test the **Ethernet** connection you can click on the Get DHCP address in the Ethernet section. If the board is connected to a live network this should return an IP address. The actual IP address returned will be different.
  - Test Results should show
    Getting DHCP Address
    DHCP Address obtained. Address is 137.57.185.70.

  - Click on the Blink Ethernet LEDs button. Verify that the LEDs on the Ethernet connector blink several times.

  - If the SMB2 board is not connected to a live network the Ethernet tests will not work correctly. Instead look for the following message in the BTS message window in the bottom of the GUI. It takes about 1 minute before you get the first timing out message

    [lan91c111] nr_lan91c111_reset: chip id = LAN91C111

[lan91c111] r_lan91c111_detect_phy: found lan83C183 (lan91C111 internal)

[lan91c111] r_lan91c111_init_phy: phy negotiation timed out
[lan91c111] r_lan91c111_init_phy: 10bt

[lan91c111] r_lan91c111_init_phy: half duplex

[dhcp] 1 timing out

This finishes the NIOS Stamp section of the tests. The rest of the tests are hardware based at this point and load from the flash memory as user designs 0-3.

3.3 DDR DIMM

Verify SW2 is set to DDR and LEDs D7, D8 and D10 are on.

Set the MPGM switches to 000 (UTILITY SWITCHES 1- 3 to closed). . Press the RESET (S8) push button. This will load Page 0 from the flash memory. Wait for LED D17 (CONF_DONEn) and LED D12 (USER) to come on.

Set dip switch S2-5 (USER DIP 4) to OPEN. You can enter a test count number, the number of time you wish to run the tests, via the User DIP Switches 6-15. This will stop the test once the count value is reached. Set dip switch S3-5, S3-6, S3-7, and S3-8 (USER DIP 12-15) to OPEN. All other DIP switch positions should be in the CLOSED position. Press pushbutton S7 (CLR/PB3) to reset the design. LED 7 goes on as S7(CLR/PB3) is pushed. Press pushbutton S4 (PB0). The Seven Segment Display should count up to F, after which user LED 0 should turn off. LED 1 is the error indicator. If it turns off the test has failed.

3.4 DDR devices

Verify SW2 is set to DDR and LEDs D7, D8 and D10 are on.

Set the MPGM switches to 100 (UTILITY SWITCHES 1 open, 2, 3 to closed). . Press the RESET (S8) push button. This will load Page 1 from the flash memory. Wait for LED D17 (CONF_DONEn) and LED D12 (USER) to come on.

Set dip switch S2-5 (USER DIP 4) to OPEN. Set dip switch S3-5, S3-6, S3-7, and S3-8 (USER DIP 12-15) to OPEN. All other DIP switch positions should be in the CLOSED position. Press pushbutton S7 (CLR/PB3) to reset the design. LED 7 goes on as the S7 is pushed. Press pushbutton S4 (PB0). The Seven Segment Display should count up to F, after which user LED 0 should light turn off. LED 1 is the error indicator. If it turns off the test has failed.

3.5 RLDRAM devices

- CIO

Verify SW2 is set to RLD and LEDs D7, D10 and D11 are on.

Set the MPGM switches to 010 (UTILITY SWITCHES 2 open, 1, 3 to closed). . Press the RESET (S8) push button. This will load Page 2 from the flash memory. Wait for LED D17 (CONF_DONEn) and LED D12 (USER) to come on.

Press pushbutton S7 (CLR/PB3) to reset the design. LED 7 and LED0 goes off as the push button S7 is pushed. Press pushbutton S4 (PB0). User LED 7 should light up and the 7 segment display should count to 80. LED 0 will turn on after the test is complete. If led 1 turns on, the test has failed.

- SIO (actual test is TBD)

Verify SW2 is set to RLD and LEDs D7, D10 and D11 are on.

Set the MPGM switches to 110 (UTILITY SWITCHES 1,2 open, 3 to closed). . Press the RESET (S8) push button. This will load Page 3 from the flash memory. Wait for LED D17 (CONF_DONEn) and LED D12 (USER) to come on.

Press pushbutton S7 (CLR/PB3) to reset the design. LED 7 and LED0 go off as the push button S7 is pushed. Press push button S4 (PB0). User LED 7 should light up and the 7 segment display should count to 80. LED 0 will turn on after the test is complete.

3.6 Downloading Factory Image

If you have corrupted the factory image pre-loaded into the on board flash memory you will have to reload the data. Set ALL DIP switch positions on S2 and S3 to the OFF position.

Set SW2 to the “DDR” position. Connect up a USB cable to a USB Blaster and connect the USB Blaster to the JTAG port on the SMB1 board.

Run the “smb1_factory_image.bat” batch file. This will download the factory image to the board. The process takes several minutes. The FCE LED will blink until the download is complete.

After this is complete, turn the board power off by switching SW1 to the OFF position. Turn SW1 back to the ON position. The Loading LED should blink, and the process should end with the SAFE_LED (D14) and the CONF_DONEn (D17) should be on. If this is not the case, retry the process ONCE.

4 Troubleshooting

Refer to the following table (table 3-1) for solutions to problems with the board, if they should occur, for power-up, configuration, and errors with test designs.

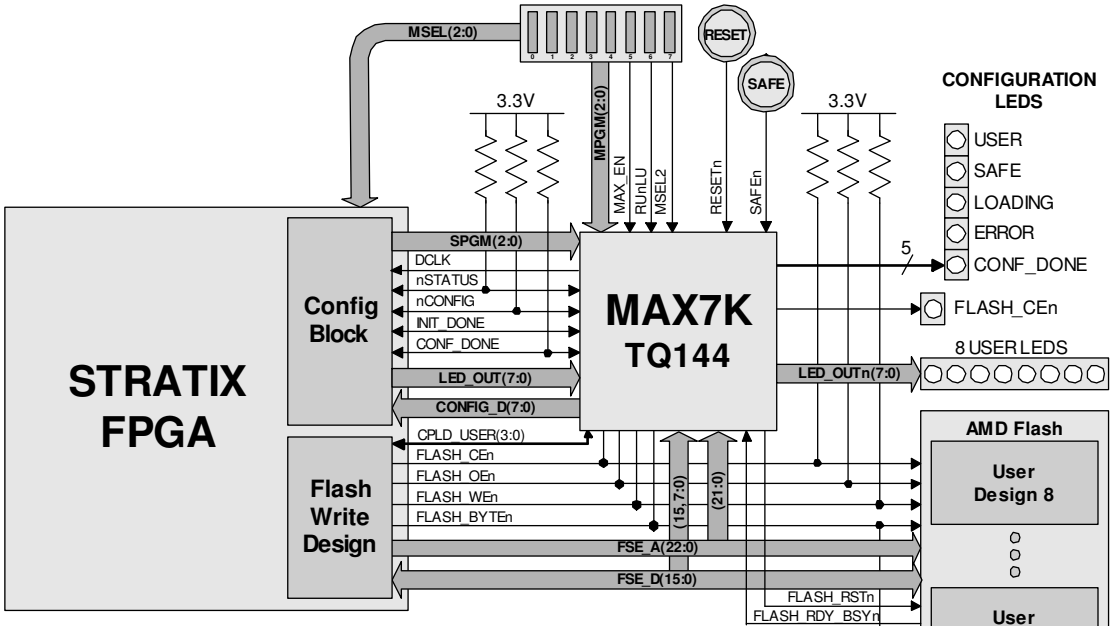
Problems	Possible Solutions
LEDs fail to come on when power is applied	Check that main connector power supply is properly connected to J4. Check that switch SW1 is turned on (all the way up). Check that the power supply is plugged in to wall. Check that switch (SW2) is in proper position (up for RLD and down for DDR).
Devices fail to configure	Check that correct program file is chosen. Check that the Byteblaster II/USB cable is installed correctly to J27 (check pin one indicator on cable) Check that configuration switch (SW4) is set appropriately.
Design does not work properly	If using on-board oscillators, check that jumper (J35) is placed across pins 1 and 2. Check that switch (SW3) is in the ENABLE position (all the way up). If using external oscillators, check that switches (SW6 and SW9) are set to EXT (down position) Check that cables are installed correctly. Check that correct program file is chosen. Check that correct push buttons and dip switches are being used. Check that dip switches, if used, are at the correct values. Ensure that the cards are fully seated (DDR) Check that the PROTO1 Test Card is installed and fully seated. Check that switch (SW2) is in proper position (up for RLD and down for DDR).
RS-232 connection not working	Check that RS-232 connector is plugged into correct port (on board and on PC)

Table 3-1: Troubleshooting

5 MAX Configuration Controller

This section provides an explanation of the code that is used to program the EPM7256AE device which is used, in conjunction with the NIOS uP interface, to configure the Stratix device. This design is based on the Common Configuration Specification's "A-spec" that outlines a general CPLD-based flash configuration controller for Stratix Boards.

Figure 5-1 shows the block diagram of the MAX configuration circuitry of the Stratix Memory Board II. The design uses 129 of 256 macrocells in the EPM7256AE device. There are 104 of 120 I/Os used in the design. The controller utilizes the fast passive parallel (FPP) configuration mode of the Stratix device family to quickly configure the device with the configuration data stored into the Flash memory device.



NOTES:

(1) CONFIG_D(7:0) bus from MAX to Stratix only required if banks 3 and 4 are require low-voltage VCCio and Flash cannot meet Vin.
(2) FSE_D(7:0) link to MAX7K only needed if note (1) applies. Only exception is that FSE_D(15) always required for byte-addressing.
(3) FSE_D(15:8) not required if 16-bit flash interface not desired.
(4) Supports up to 8 design files + factory default design.
(5) RUnLU and MSEL2 require DIP switch -ONLY- if remote configuration modes are to be supported (remote or local).
(6) Flash Address Bus may vary based on Flash device size
(7) Adding CPLD_USER(3:0) signals with pull-ups highly recommended. Can be as little as two signals. Used for control to/from MAX and Stratix as needed for applications not covered in this specification.
(8) FLASH_CEn LED is optional but recommended.
(9) CRC_ERROR signal between MAX and Stratix only needed if support for CRAM error detection is required.
(10) MAX3K device can be used for MAX7K where applicable.

Figure 5-1 C³ Block Diagram (A-spec)

The main configuration control signals are connected between the MAX and Stratix devices to allow the MAX device to control the configuration inputs and monitor the Stratix configuration status outputs.

The below memory map is used for Stratix Memory Board II. The large 16MB flash has more then enough room to store items useful for demos such as image files and small video files in the "PLD Design X / Other" areas while keeping enough space to store a large amount of NIOS software and even a website in the "User Code Space". Alternatively the flash can be loaded with up to 6 user or demo designs and a large amount of software and a website in the "User Code Space". Compression cannot be used with Stratix devices (Stratix-II only).

It is assumed that the "Safe" design would support flash programming and web server support for potential documentation for the board and/or the target FPGA or demo designs.

Stratix 1S40 / 16MB Flash Memory Map	
Block Name	**Address**
PLD Design 5 / Other	0x0FFF.FFFF 0x0E00.0000
PLD Design 4 / Other	0x0DFF.FFFF 0x0C00.0000
PLD Design 3 / Other	0x0BFF.FFFF 0x0A00.0000
PLD Design 2 / Other	0x09FF.FFFF 0x0800.0000
PLD Design 1	0x07FF.FFFF 0x0600.0000
PLD Design 0	0x05FF.FFFF 0x0400.0000
Safe Design	0x03FF.FFFF 0x0200.0000
User Code Space	0x01FF.FFFF 0x0000.0000

Table 5-1 Stratix 1S40 / 16MB Flash Map

The general function of the MAX Configuration Controller is as follows:

- **SAFE** button loads the Factory default design (BTS design)
- **SYS_RESET** button loads user design file located in the page pointed to by **MPGM(2:0)** or **SPGM(2:0)** based on **MSEL2** (remote configuration enable)
- **SAFE** design will be loaded if the User Design fails to load.
- **USER LEDs** are driven through the MAX from the Stratix
- **LD LED** blinks during a configuration attempt
- **SF LED** lights when the Factory Default image was loaded
- **USR LED** lights when a User Design was loaded from any page
- **ER LED** lights when configuration failed.

Table 5-2 shows the operation of the MAX design in more detail.

max_en	sys_resetn	pb_safe_page	use_spgm / MSEl	mpgm	spgm	output state
0	X	X	X	XXX	XXX	USER, SAFE, ERROR LOADING LEDs are on. No Configuration occurs.
1	Push	1	0	000	XXX	Loads Page 0, User LED on
1	1	Push	0	XXX	XXX	Loads Safe Page, Safe LED is on.
1	Push	1	1	XXX	000	Loads Page 0, User LED on
1	Push	1	1	XXX	001	Loads Page 1, User LED on
1	Push	1	1	XXX	010	Loads Page 2, User LED on
1	Push	1	1	XXX	011	Loads Page 3, User LED on
1	Push	1	1	XXX	100	Loads Page 4, User LED on
1	Push	1	1	XXX	101	Loads Page 5, User LED on
1	Push	1	1	XXX	110	Loads Page 6, User LED on
1	Push	1	1	XXX	111	Loads Page 7, User LED on
1	1	Push	1	XXX	XXX	Loads Safe Page, Safe LED is on.

Table 5-2