Stratix to QDR-II Memory Devices Interface Analysis

High Speed / End Applications Team
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Revision History

Date	Version	Author	Description
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1 Introduction

This document presents the results of the simulation done for the HSTL-II I/O standard used in memory device interfaces designed by the Altera High Speed I/O / End Applications Team in San Diego. This document also recommends termination schemes based on the review of the simulation results. Agilent ADS is used for simulation and IBIS models of Stratix/Stratix GX devices and Micron DDR memories are used.

1.1 Background

The new QDR-II memory has been incorporated in new high end designs where independent I/O pins are designated for better performance. Several boards that feature QDR-II memories are being designed both inside and outside Altera. The increased data transfer on systems based on QDR-II devices requires a higher degree of awareness to the signal integrity and the factors the degrade it, tighter tolerances, faster rise and fall time translates to higher bandwidths. Thus it is important to have good signal integrity on the board. This, in turn, implies the termination scheme needs to be good to avoid reflections. The JEDEC specification for the HSTL-II standard only provides general guidelines which may not always be the best choice to implement in a real system. Hence a need for a document which compares several termination schemes exists. This document aims to fulfill that need.

1.2 Simulation Overview

Simulations are performed using the ADS tool from Agilent. IBIS models are used to model the Stratix device and the Cypress QDR-II memory device. The memory device used is QDR-II x16 (part number Cypress CY7C1313V18-200BZC). Simulation frequency is 200 MHz or 400 Mega Transfers per second. Simulation for both write and read cycles are performed for data bits since the bus is bidirectional. For the address bus, simulation for only the write direction is needed since the bus in unidirectional. The data is a point to point interface, while the address is a point to multipoint interface. This is because each address bit is serving more than one memory device.

The total routing length from the FPGA to the memory device is set to 6.0” which is a conservative estimate in the majority of systems.

The placement of parallel termination resistors at the ends of the line can be achieved in two modes: fly-by and non-fly-by. In fly-by mode, the resistor is at the end of the transmission line and the connection to the device pin is made through a short stub off the transmission line. In non-fly-by configuration, the transmission line ends at the device pin, and the resistor is placed before the end of the transmission line is reached. For configurations which have parallel resistors at the source/destination pins, fly-by and non-fly-by topologies are achievable while laying out the board.

Figure 1-1 Non Fly-By (top), Fly-By (middle) and on device termination ODT (bottom) placement of parallel termination resistor. Figure 1-1 shows the fly-by versus non-fly-by placement of parallel resistors. In general fly-by placement is preferred over non-fly-by because the distance

from the pin to the resistor is not very critical for fly-by placement. In the cases that follow, both fly-by and non-fly-by simulations are performed as much as possible. In addition, we incorporated series resistor similar to the SSTL standard for comparison to the DDR-I and DDR-II interfaces.

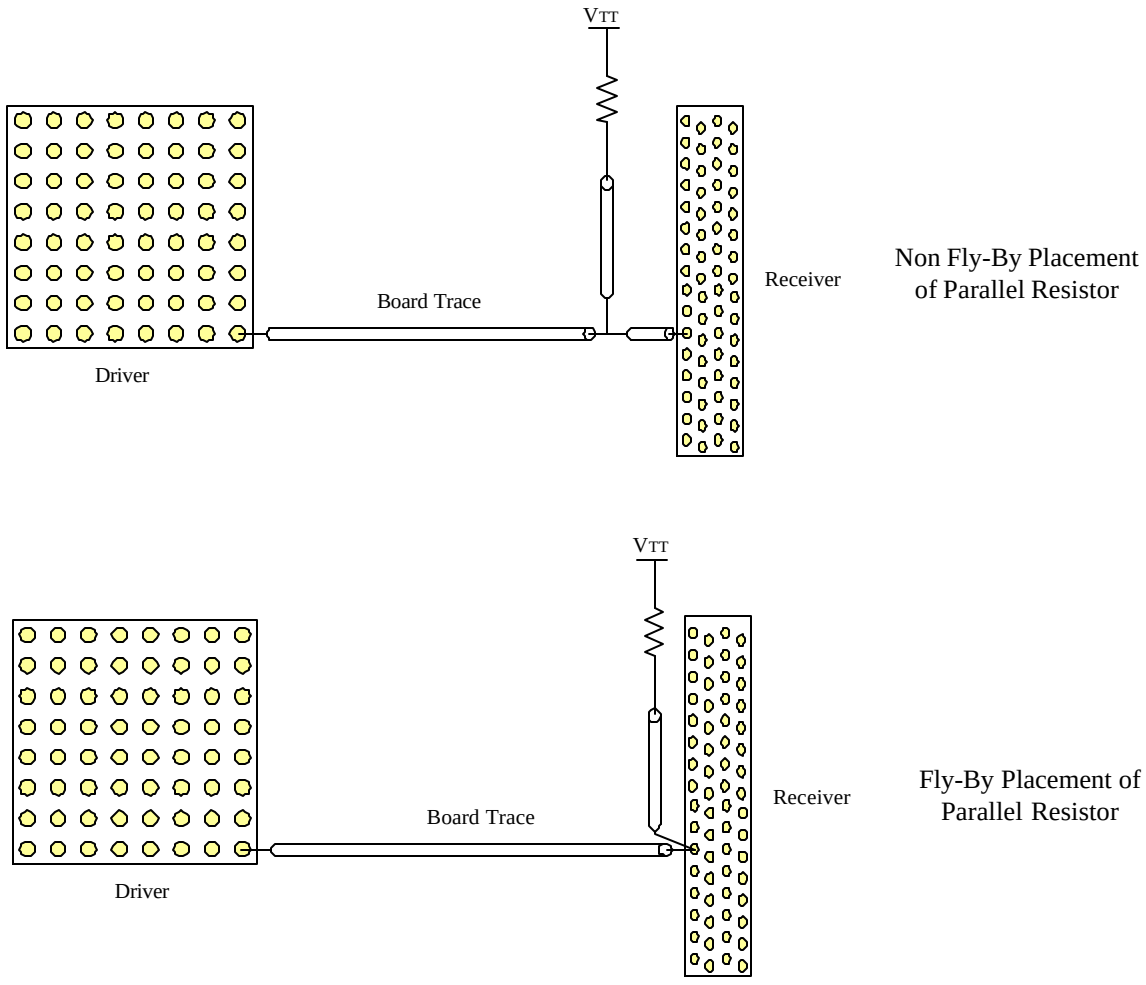

Figure 1-1 Non Fly-By (top), Fly-By (middle) and on device termination ODT (bottom) placement of parallel termination resistor.

2 Simulation Results

This section presents the results of the simulation for the data, address and clock interfaces using a variety of configurations.

2.1.1 Dual Series/Dual Parallel Termination (Fly-By)

This topology, depicted in Figure 2-1, requires two series resistors and two parallel resistors. The series resistors are needed to match the output impedance of the driver to the transmission line and the parallel resistor is the actual termination of the transmission line. The performance of this topology shows a similar response between the read and the write cycles due to its symmetric construction. The small differences between the read and write cycles are due to the differences in the driver/receiver characteristics models.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-2 Figure 2-3and Figure 2-4 respectively. Looking at the waveforms, it is clear that the signal integrity is very good, however, the signal suffers from some attenuation due to the series resistors.
The eye closure at the Stratix during the read cycle is about 0.932 and the eye closure at the QDR-II during the write cycle is 0.913. These levels are good for HSTL-II and this scheme would work fine for the read and write cycles.

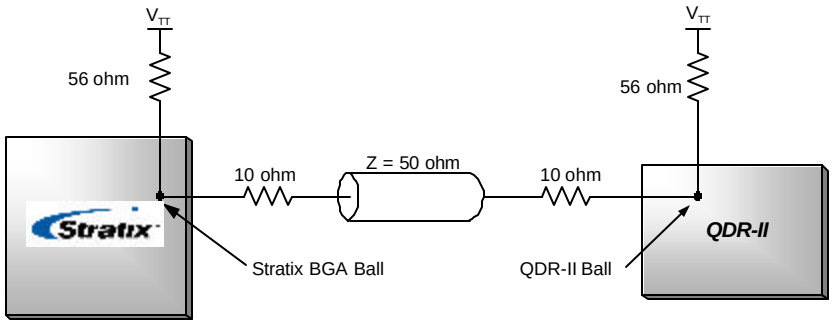

Figure 2-1 Dual Series/Dual Parallel Termination, Fly-By.

In order to understand the eye analysis plots some definition are required.
Eye Amplitude.- The "1" level mean subtracted from the "0" level mean.
Eye Height.- Is the inner bound of the eye.
Eye Closure.- Is the ratio of the Eye Height to the Eye Amplitude.
Eye Closure (dB).- 20log (Eye Closure)

The jitter analysis plots should be read on the left scale the eye amplitude, on the right scale the frequency (number of hits) between the reference levels "A" and "B" for the read cycles, "D" and "E" for the write cycles. The cursors C1, C2, F1 and F2 set the boundaries for the total jitter during the read and write cycles respectively.
From the jitter analysis plots the total jitter during the write cycle is 83.3 pS and the total jitter during the red cycle is 100pS.

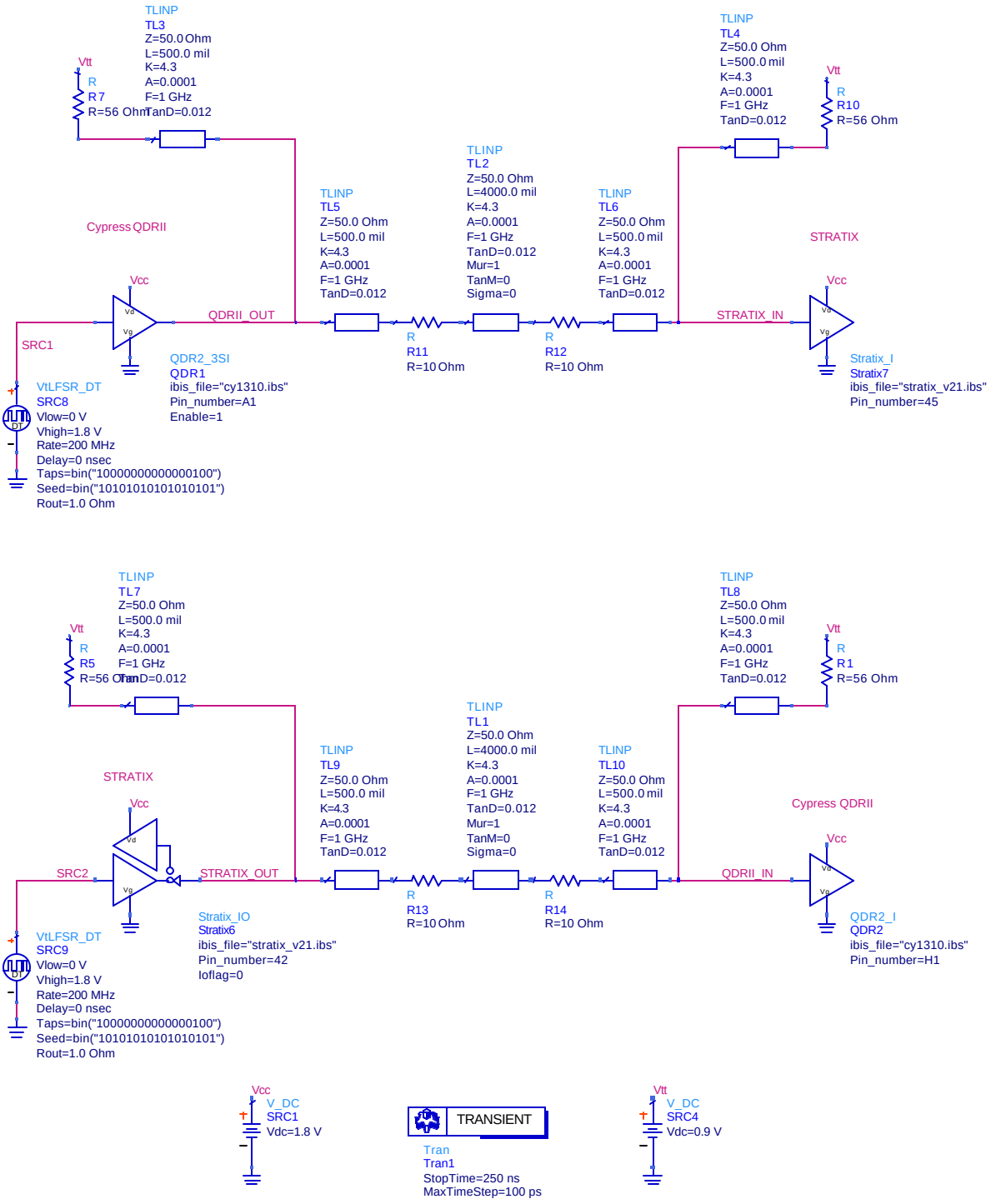

Figure 2-2 Dual Series/Dual Parallel Termination Simulation Setup (Fly-By).

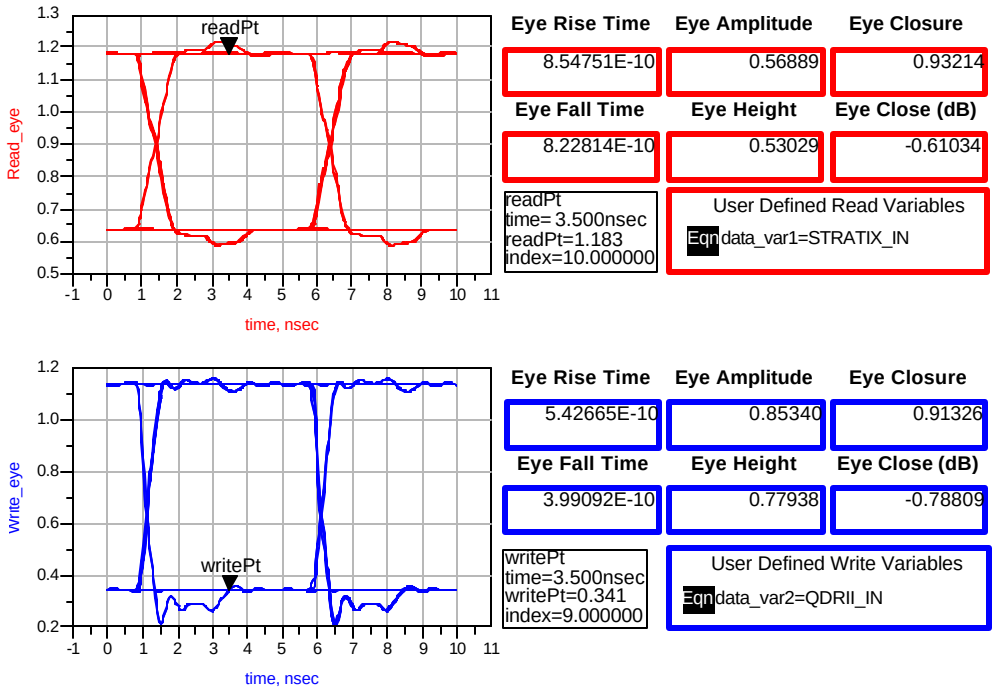

Figure 2-3 Dual Series/Dual Parallel Eye analysis Fly-By.

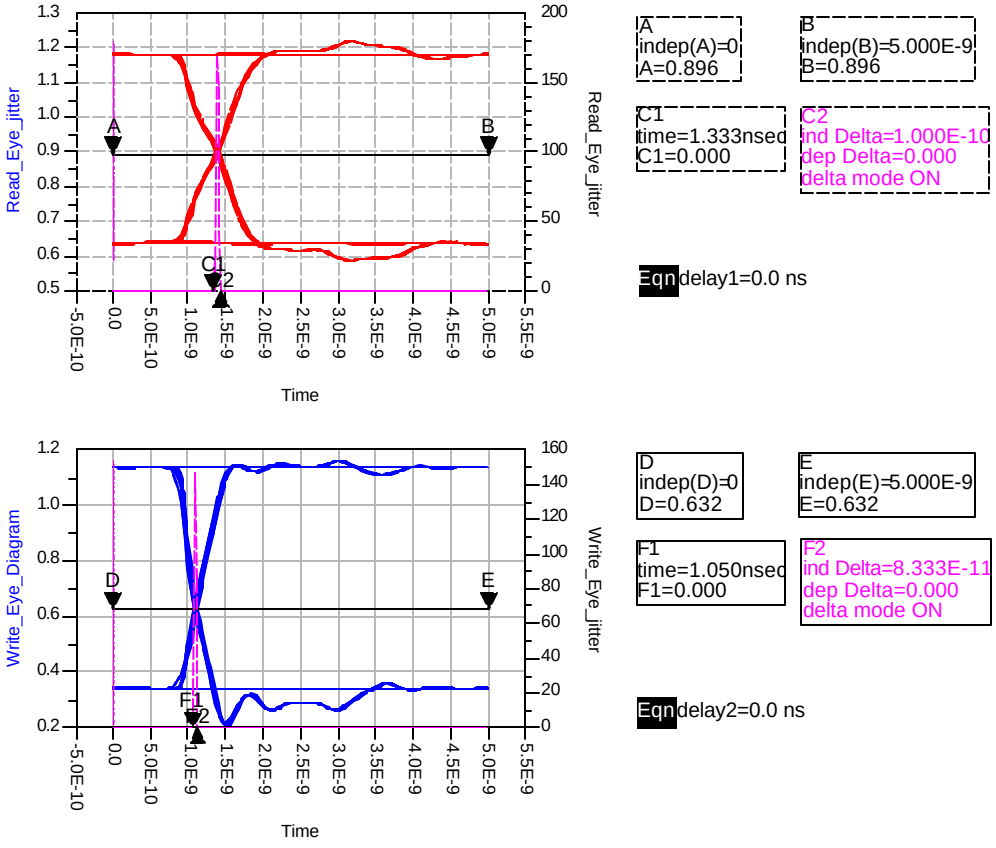

Figure 2-4 Dual Series/Dual Parallel Jitter Analysis Fly-By.

2.1.2 Dual Series/Dual Parallel Termination (Non-Fly-By)

This topology, depicted in Figure 2-5, requires two series resistors and two parallel resistors.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-6, Figure 2-7 and Figure 2-8 respectively. Looking at the waveforms, it is clear that the signal integrity is good, however, the signal suffers from the effects of high impedance (open stub) at the DDR-I side during the write cycles and at the Statix side during the read cycle. These open stubs (500 mils in simulation) represent an unterminated system which shows some degree of reflections during each cycle that creates a standing wave. This standing wave could be additive or subtractive depending on the delay and/or location of the discontinuity. The eye closure at the Stratix during the read cycle is 0.832 and at the QDR-II during the write cycle is 0.923 respectively. The performances of this topology will warranties the functionality of the link during the read and write cycles.

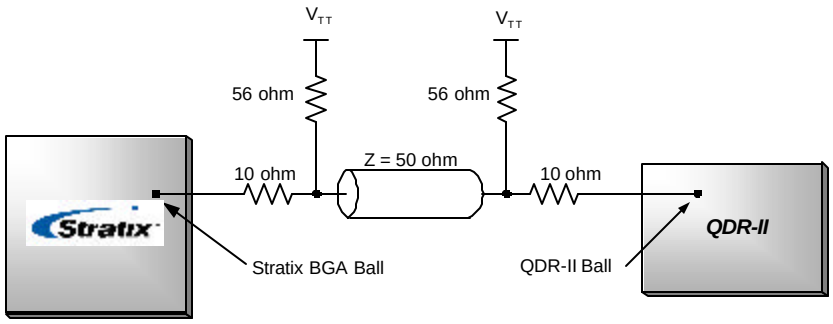

Figure 2-5 Dual Series/Dual Parallel Termination, Non-Fly-By.

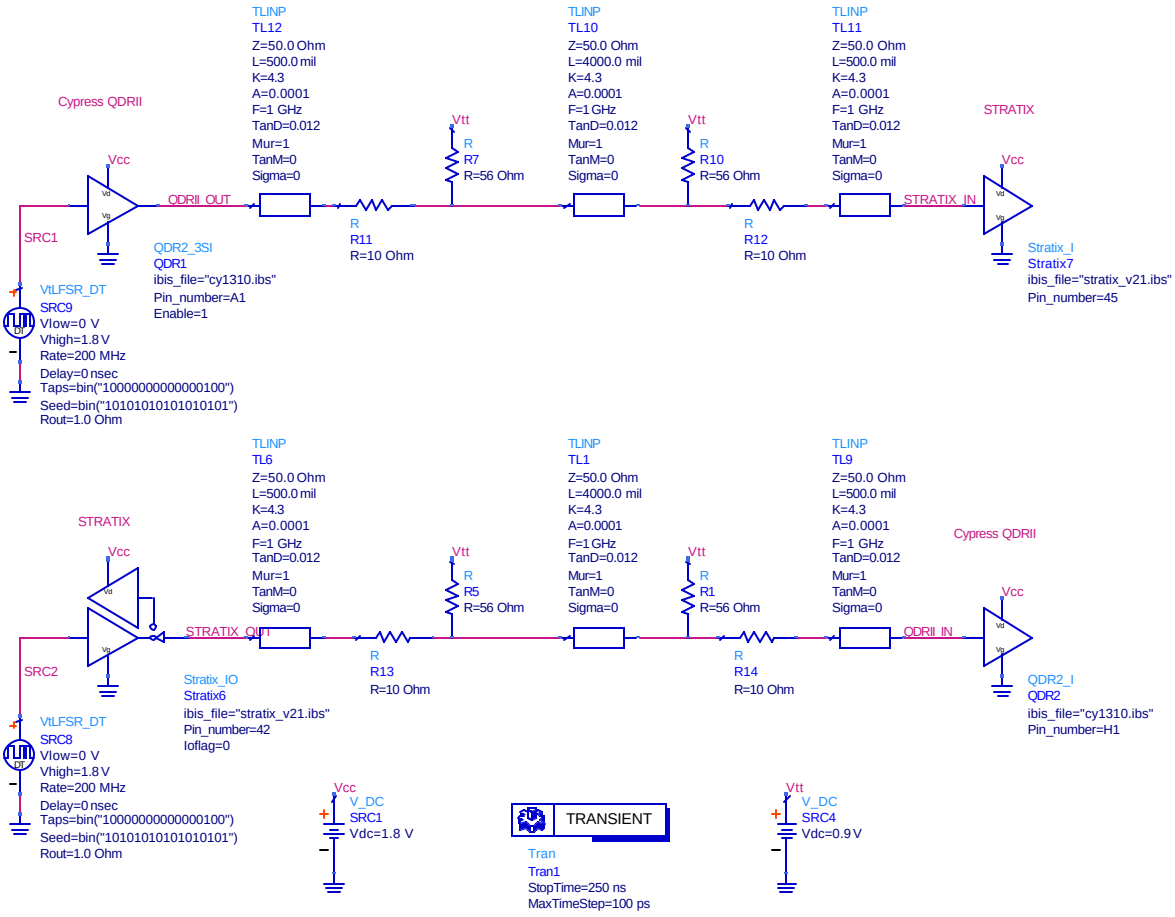

Figure 2-6 Dual Series/Dual Parallel Termination Simulation Setup Read/Write Cycles, Non Fly-By.

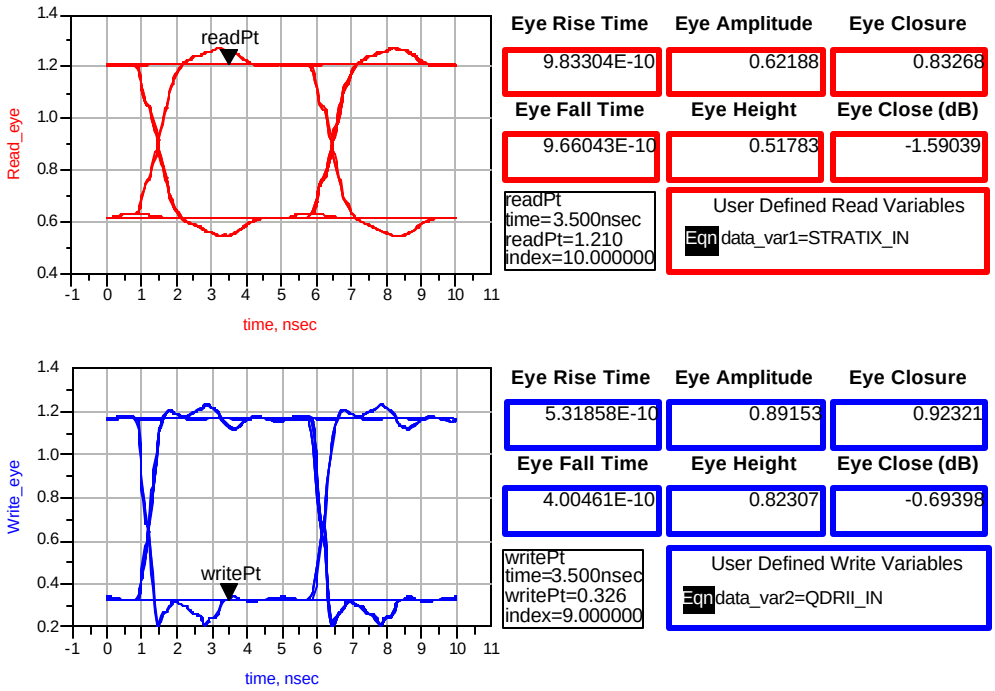

Figure 2-7 Dual Series/Dual Parallel Termination Simulation Eye Analysis, Non Fly-By

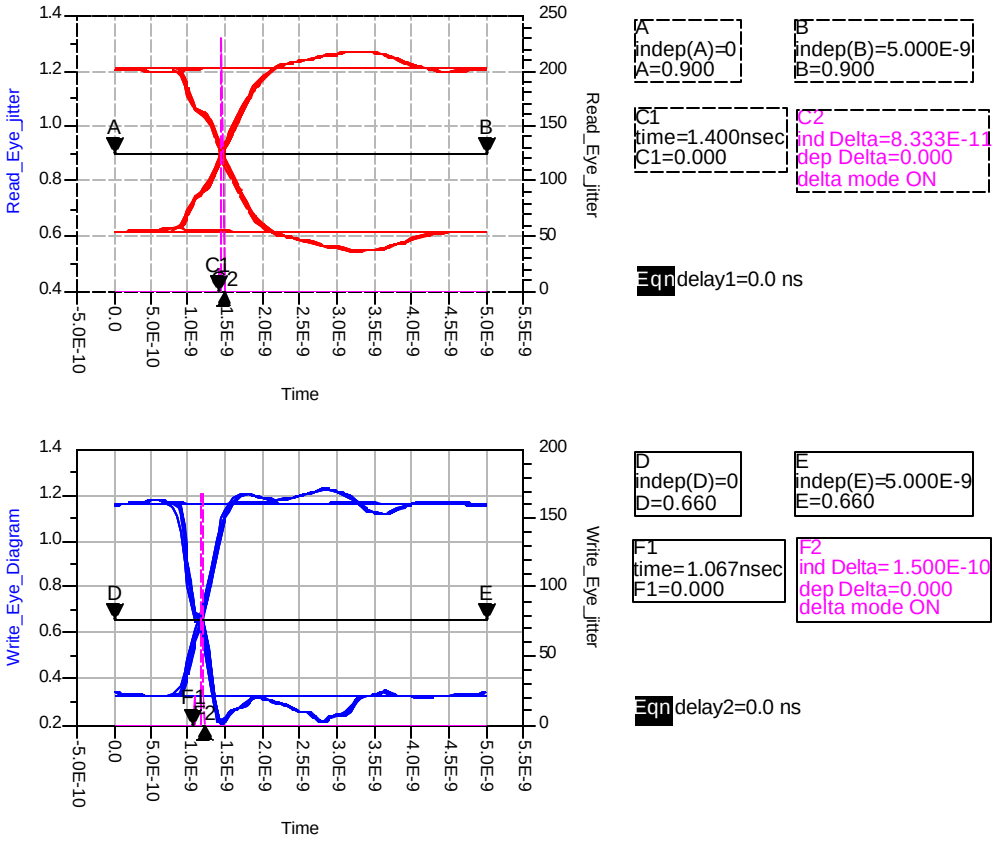

Figure 2-8 Dual Series/Dual Parallel Termination Simulation Jitter Analysis, Non Fly-By

2.1.3 Dual Parallel Termination (Fly-By)

This topology, depicted in Figure 2-9, requires two series resistors and two parallel resistors.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-10, Figure 2-11 and Figure 2-12 respectively. Looking at the waveforms, it is clear that the signal integrity is good, however, the signal suffers from the effects of the miss match between the driver device, Stratix or QDR-II, and the transmission line during the read or write cycles. The output impedance of an active device is in the order of 30 ohms that does not match the transmission line impedance of 50 ohms creating a standing wave.
The high input impedance of an active device makes the Fly-By option well suited for minimum components and good performance topology. The eye closure at the Stratix during the read cycle is 0.882 and at the QDR-II during the write cycle is 0.916 respectively. The performances of this topology will warranties the functionality of the link during the read and write cycles.

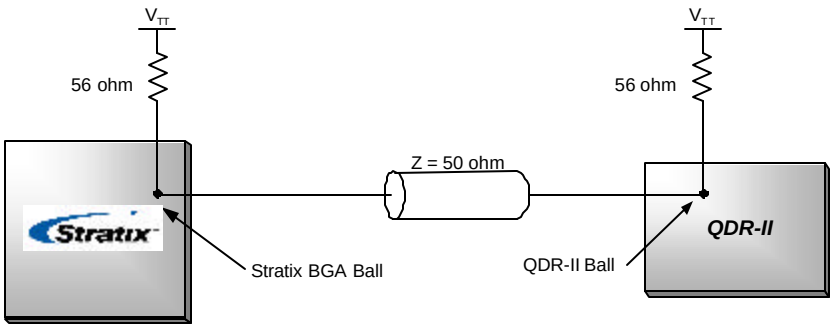

Figure 2-9 Dual Parallel Termination (Fly-By)

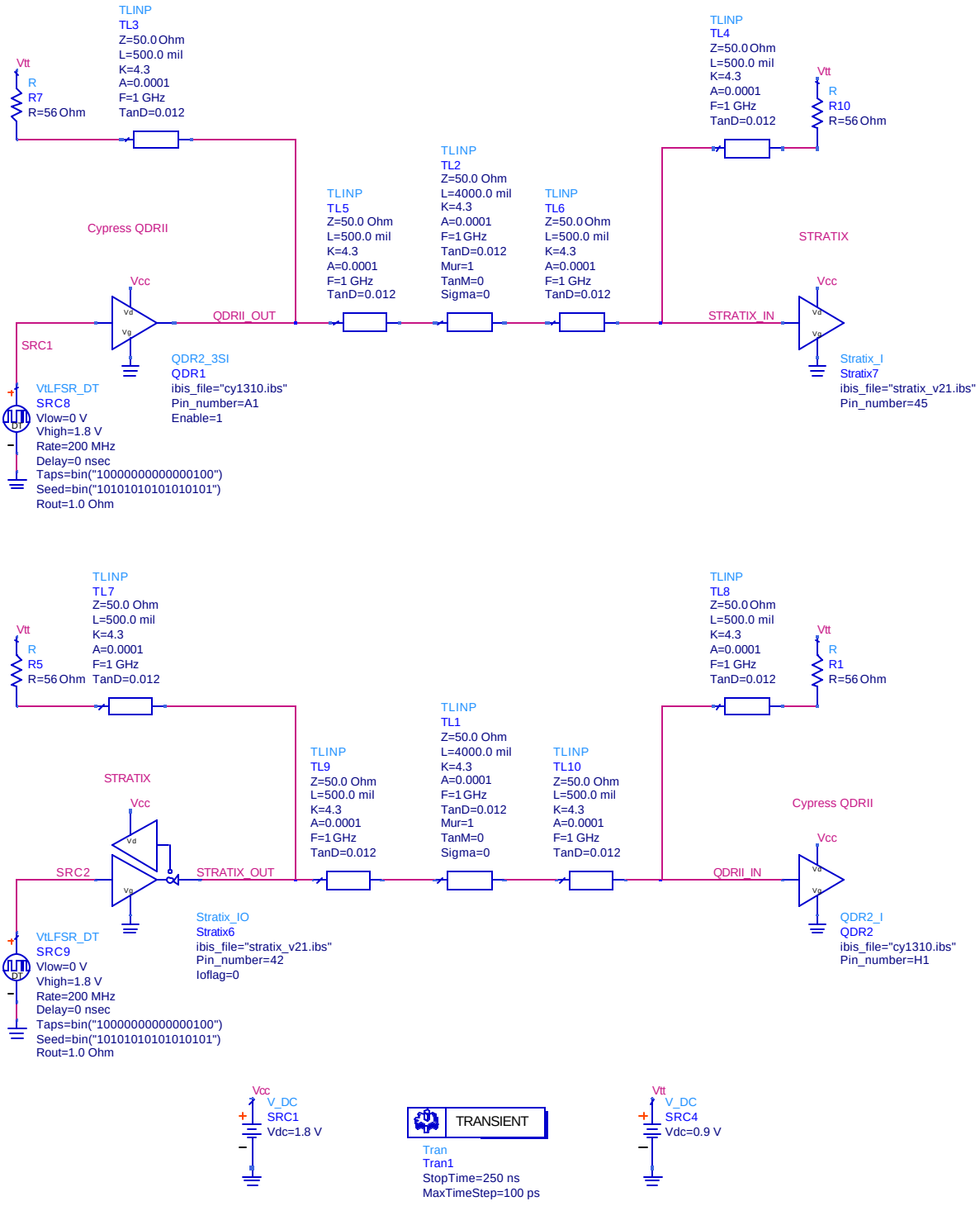

Figure 2-10 Dual Parallel Termination Simulation Setup Read/Write Cycles, Scheme 1.

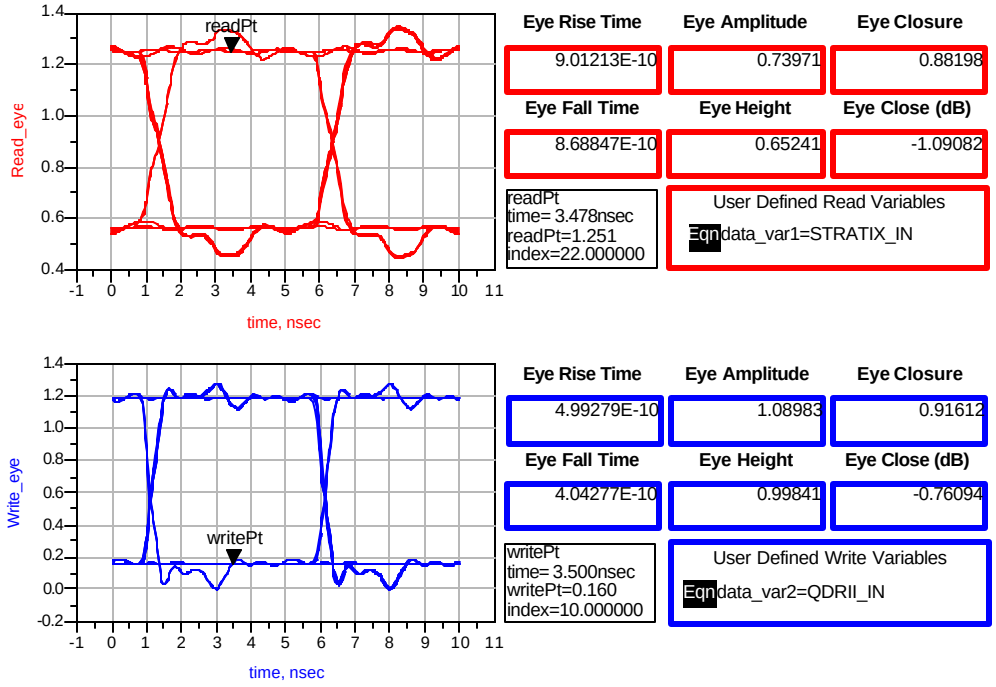

Figure 2-11 Dual Parallel Termination Eye Analysis, Fly-By.

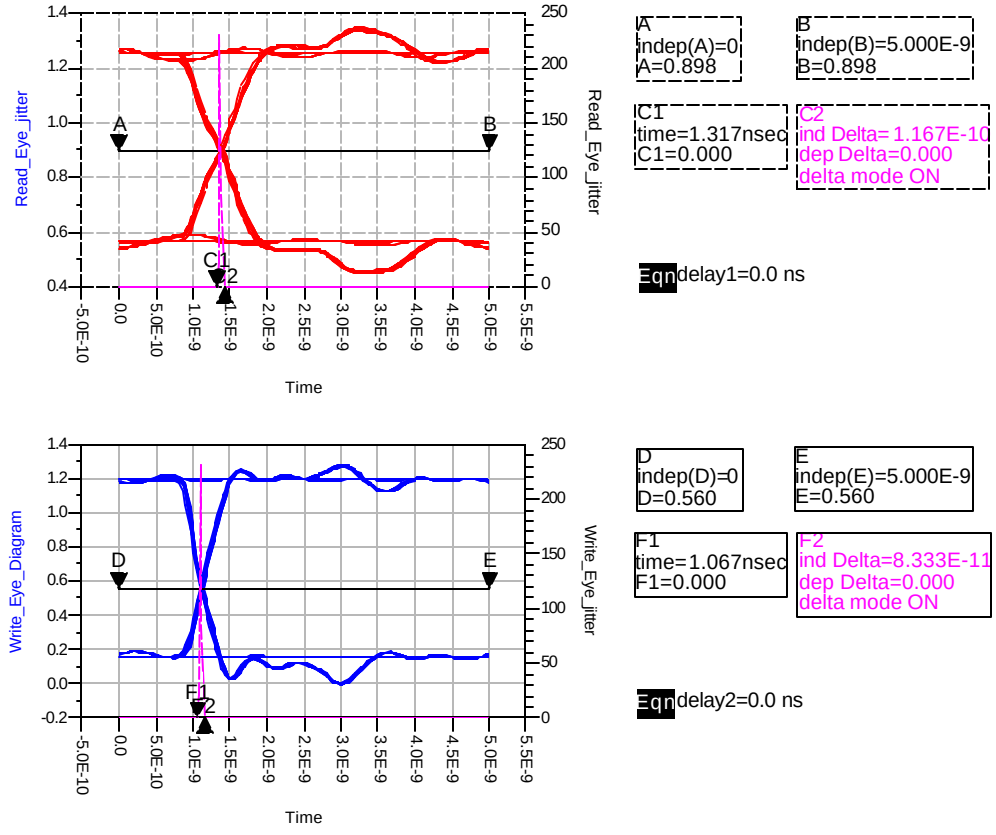

Figure 2-12 Dual Parallel Termination Jitter Analysis, Fly-By

2.1.4 Dual Parallel Termination (Non-Fly-By)

This topology, depicted in Figure 2-13, requires two series resistors and two parallel resistors.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-14, Figure 2-15 and Figure 2-16 respectively. Looking at the waveforms, it is clear that the signal integrity is good, however, the signal suffers from the effects of the open stub at the end of the transmission line during the read or write cycles. The input impedance of an active device is in the order of few Kohms that does not match the transmission line impedance of 50 ohms creating a standing wave.
This topology is recommended for systems where routing layers and components have to be kept to the minimum. The performance of this topology is similar to the Fly-by one but this required less routing and complexity. The most important parameters that have to be kept to the minimum is the distance from the termination resistor to the input of the device. The eye closure at the Stratix during the read cycle is 0.786 and at the QDR-II during the write cycle is 0.885 respectively. The performances of this topology will warranties the functionality of the link during the read and write cycles.

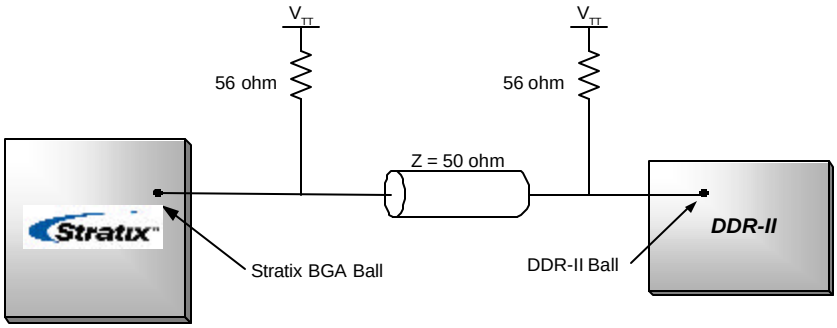

Figure 2-13 Dual Parallel Termination Non Fly-by

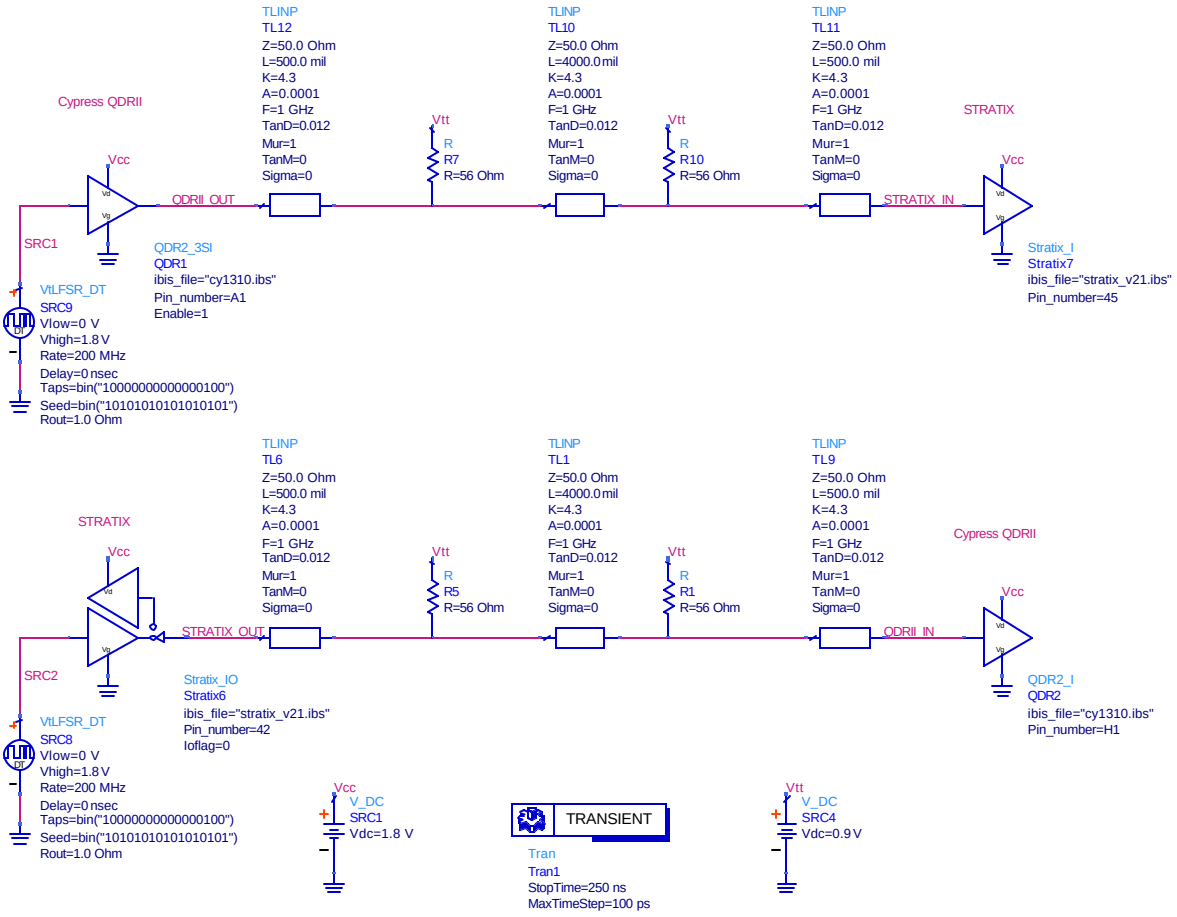

Figure 2-14 Dual Parallel Termination Simulation Setup Read/Write Cycles, Non Fly-By.

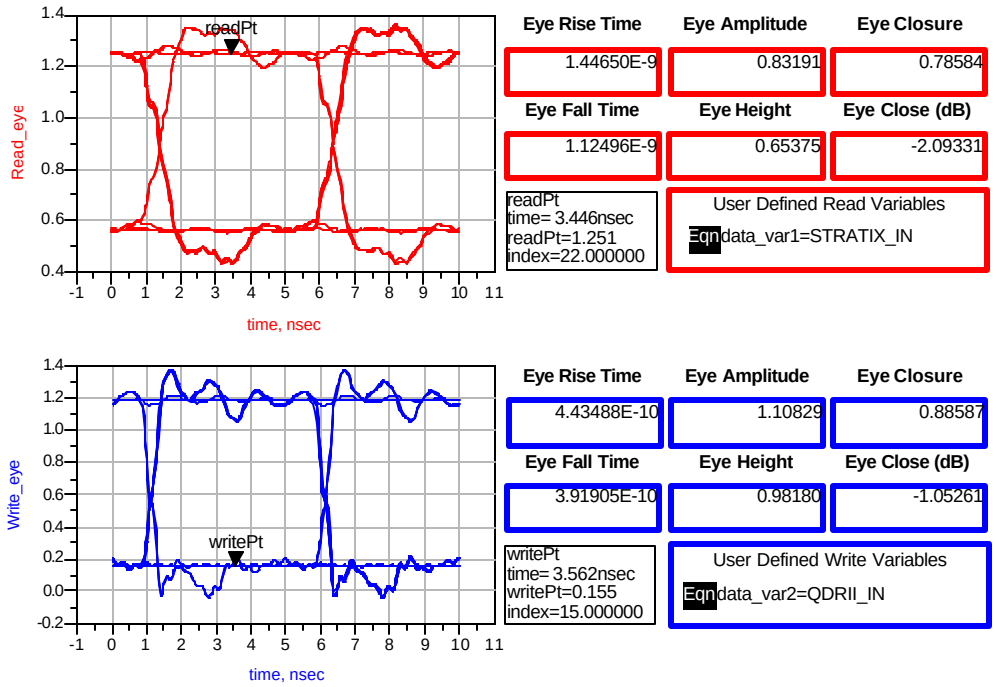

Figure 2-15 Dual Parallel Termination Eye Analysis Results, Non Fly-By

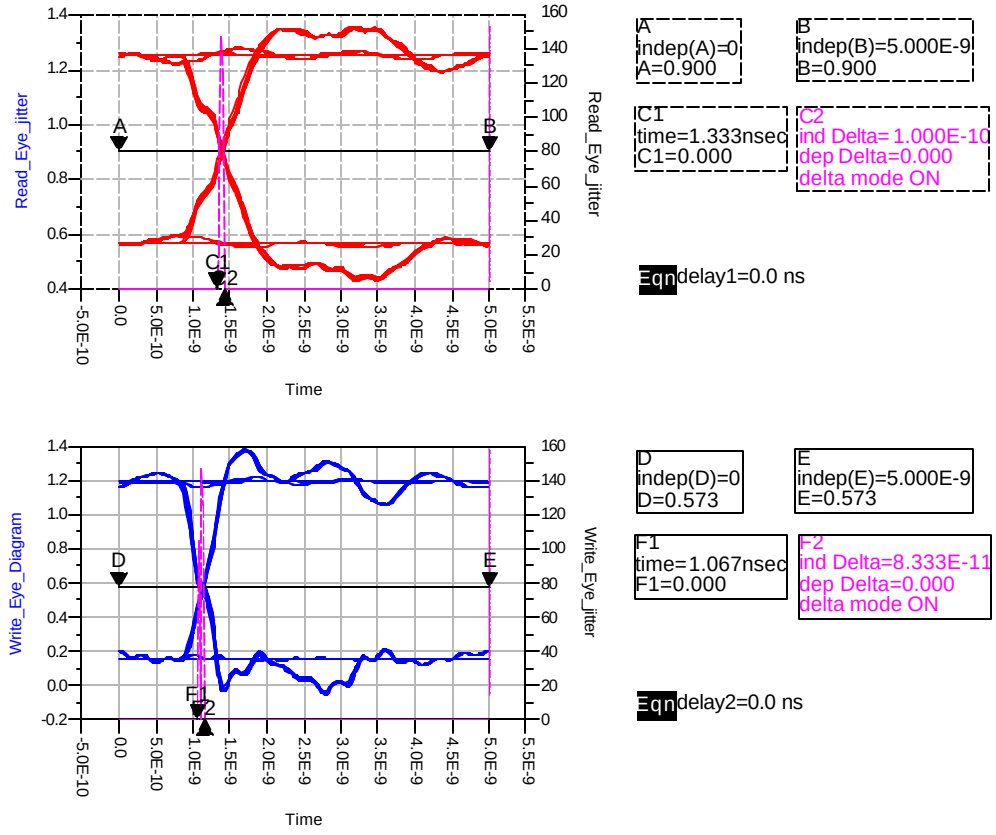

Figure 2-16 Parallel Termination Jitter Analysis Results, Non Fly-By.

2.1.5 Near End Single Series / Dual Parallel Termination (Fly-By)

This topology, depicted in Figure 2-17, requires one series resistors and two parallel resistors.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-18, Figure 2-19 and Figure 2-20 respectively. This topology is useful when output drive strength or output impedance of both devices is different. The addition of one resistor makes this topology asymmetrical, so the performance during the read/write cycles will be different adding flexibility to the system. This characteristic can be used to optimized one of the read or write cycles. Looking at the waveforms, it is clear that the signal integrity during the write cycle is better that the read cycle. The high impedance shown at the input of an active device makes the Fly-By option well suited for minimum components, good performance and low sensitivity to termination resistor location. The eye closure at the Stratix during the read cycle is 0.892 and at the QDR-II during the write cycle is 0.933 respectively. The performances of this topology will warranties the functionality of the link during the read and write cycles.

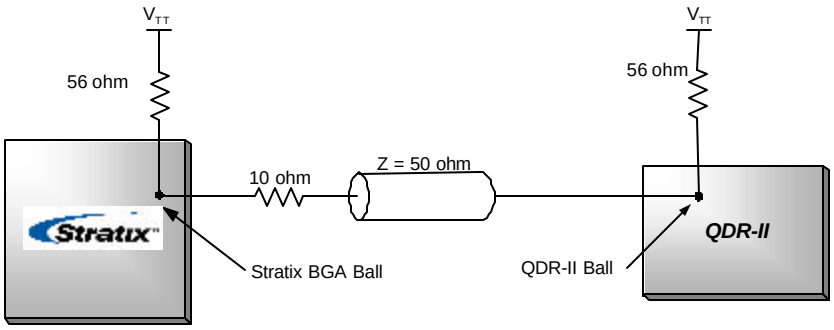

Figure 2-17 Near End Single Series / Dual Parallel Termination (Fly-By).

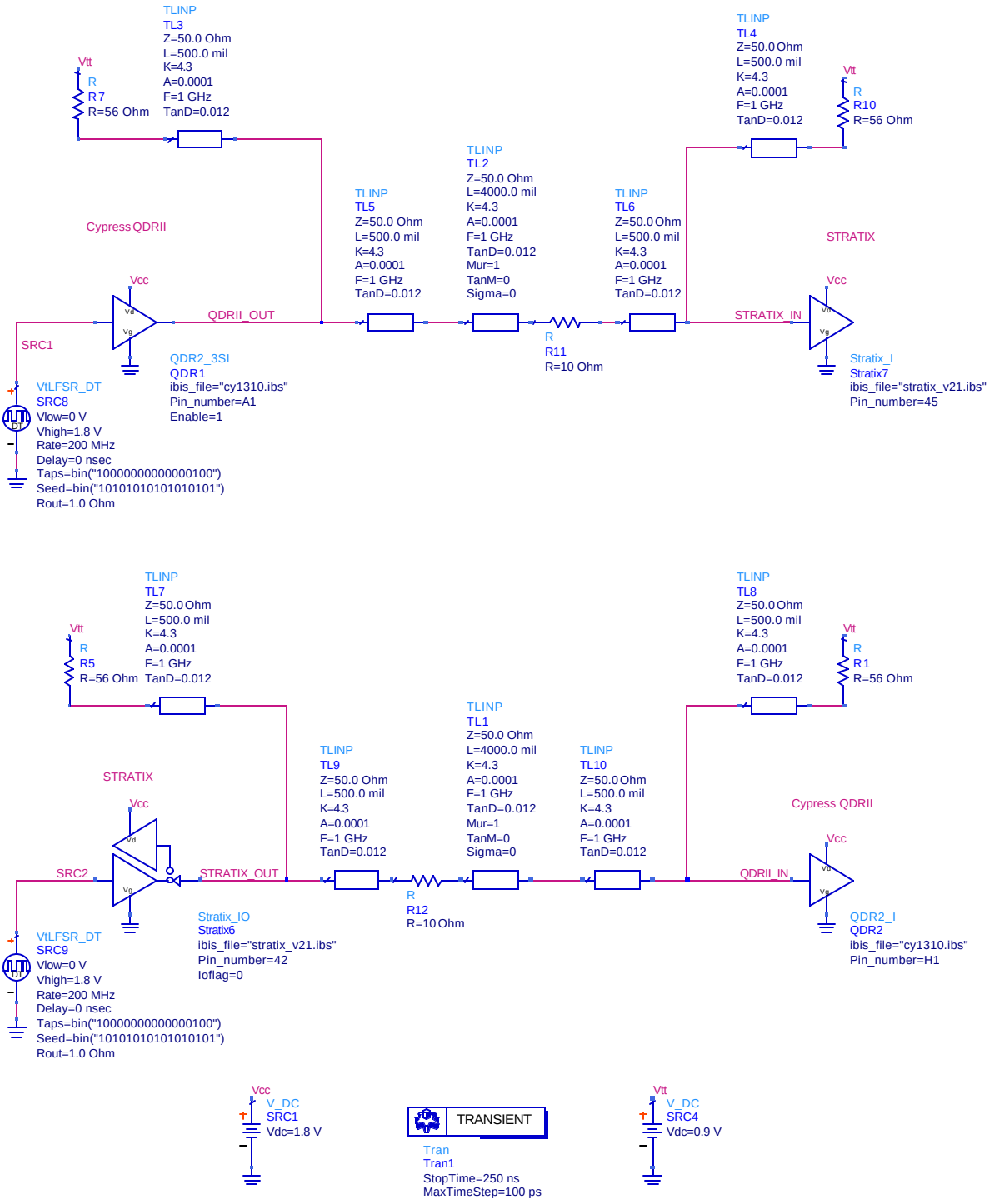

Figure 2-18 Near End Single Series / Dual Parallel Termination Simulation Setup Read/Write Cycles (Fly-By)

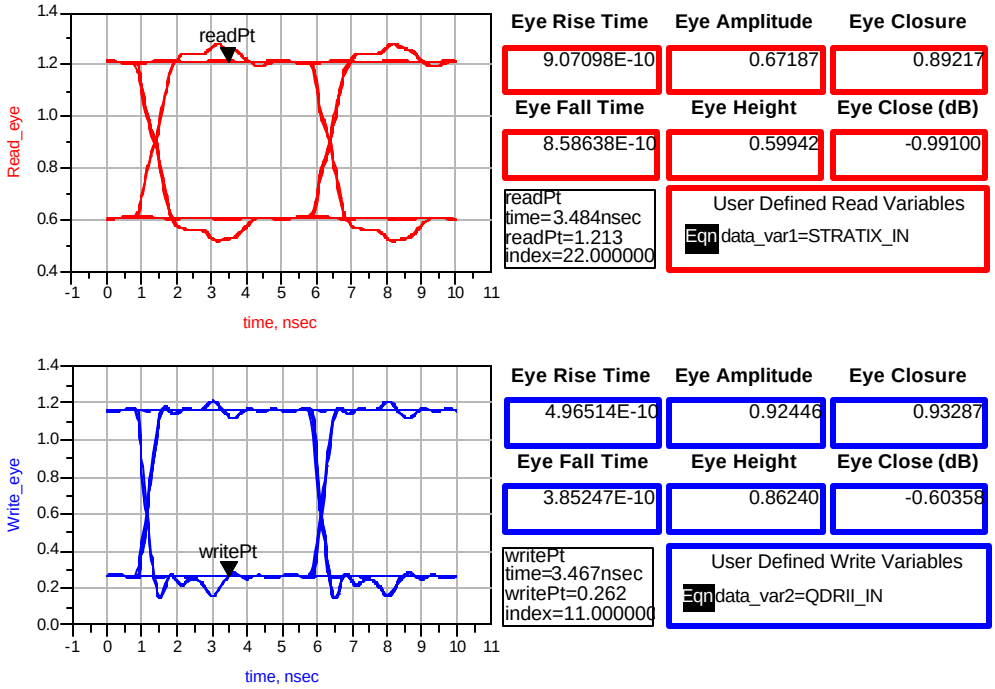

Figure 2-19 Stratix Near End Single Series / Dual Parallel Termination Eye Analysis Results

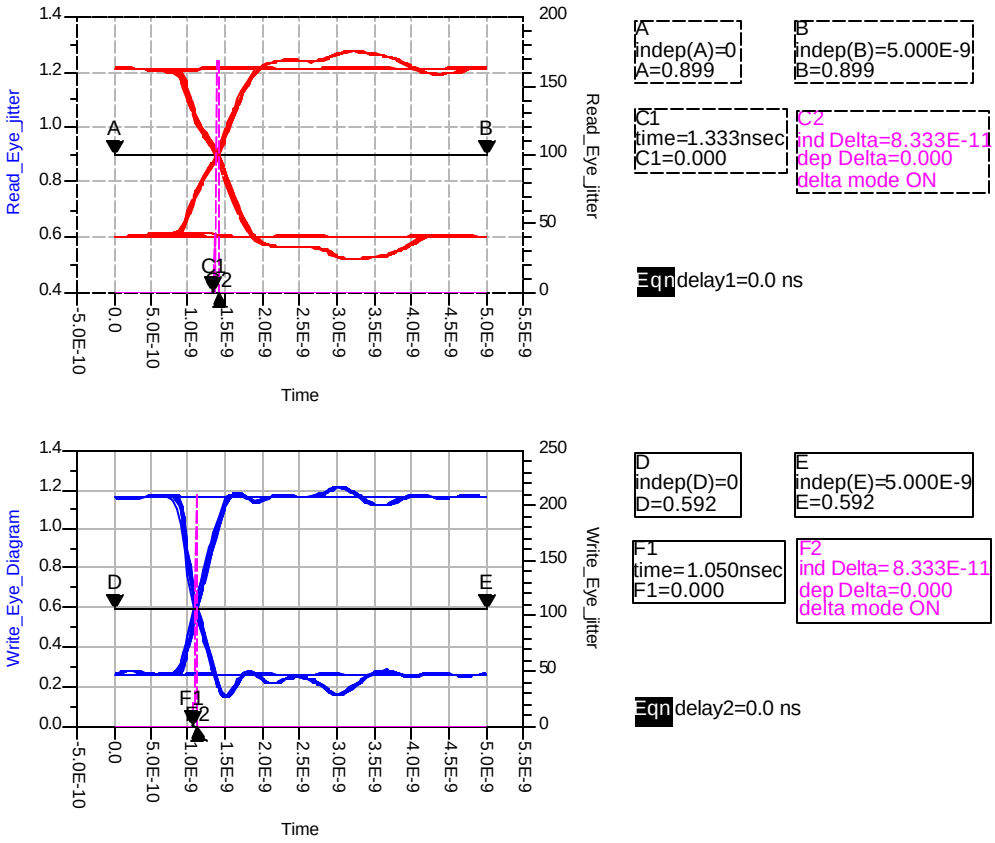

Figure 2-20 Stratix Near End Single Series/Dual Parallel Termination Jitter Analysis Results

2.1.6 Near End Single Series / Dual Parallel Termination (Non-Fly-By)

This topology, depicted in Figure 2-21, requires one series resistors and two parallel resistors.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-22, Figure 2-23 and respectively. This topology and the previews one are useful when output drive strength or output impedance of both devices is different. The addition of one resistor makes this topology asymmetrical, so the performance during the read/write cycles will be different. This characteristic can be used to optimized one of the read or write cycles. Looking at the waveforms, it is clear that the signal integrity during the write cycle is better that the read cycle.
The approach depicted in Figure 2-21 is an option when the routing in high density areas makes the previews topology difficult to achieve. The most important parameter that have to be considered to minimize undesired standing waves is the distance from the termination resistor to the input of the device. The eye closure at the Stratix during the read cycle is 0.847 and at the QDR-II during the write cycle is 0.883 respectively. The performances of this topology will warranties the functionality of the link during the read and write cycles.

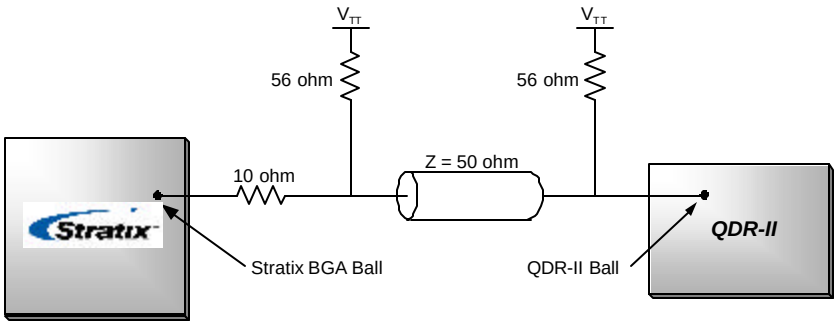

Figure 2-21 Near End Single Series / Dual Parallel Termination (Non-Fly-By)

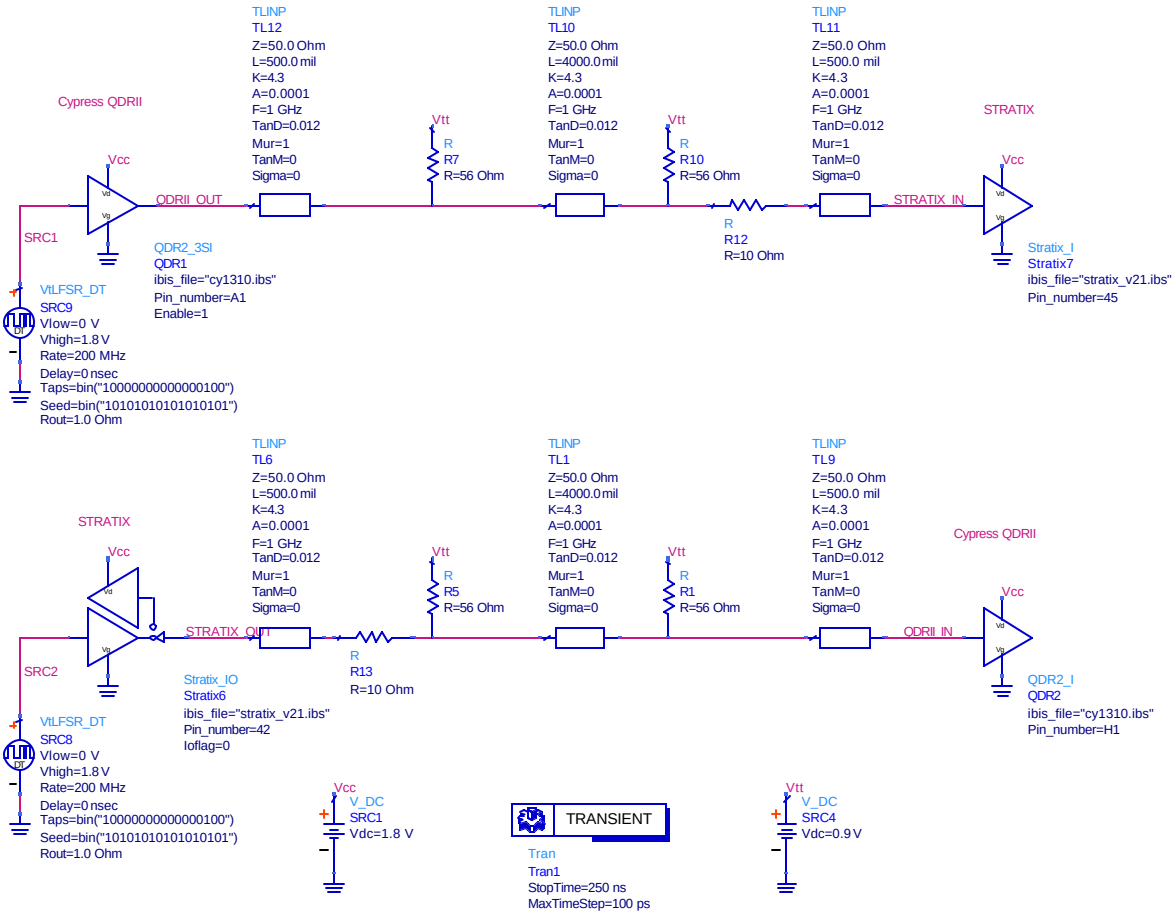

Figure 2-22 Near End Single Series/Dual Parallel Termination Simulation Setup Read/Write Cycles , (Non-Fly-By)

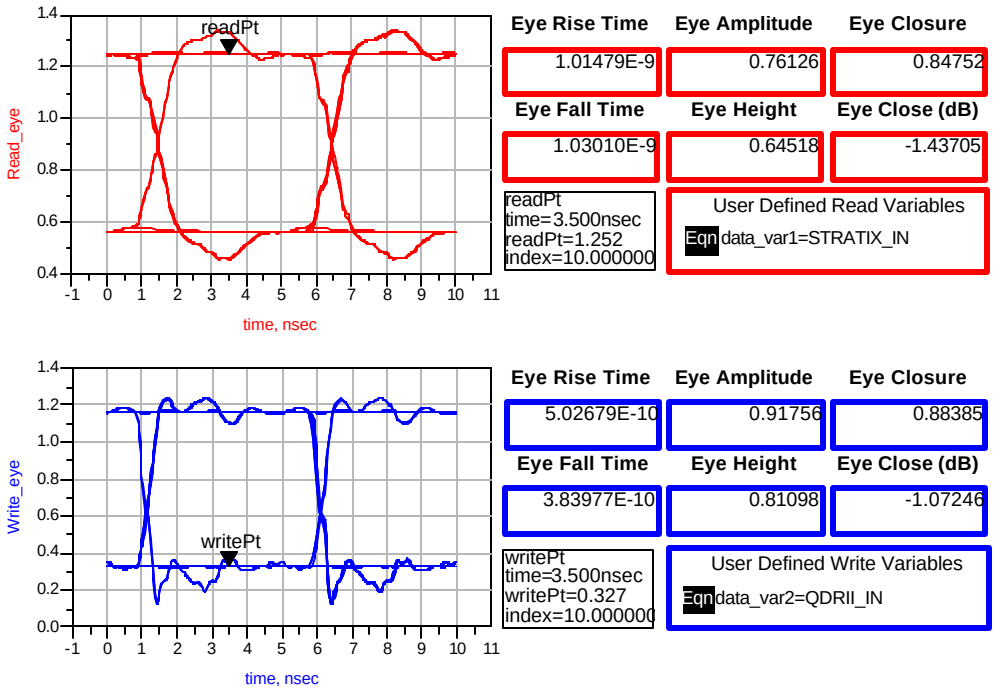

Figure 2-23 Near End Single Series / Dual Parallel Termination Eye Analysis Results, Non Fly-By.

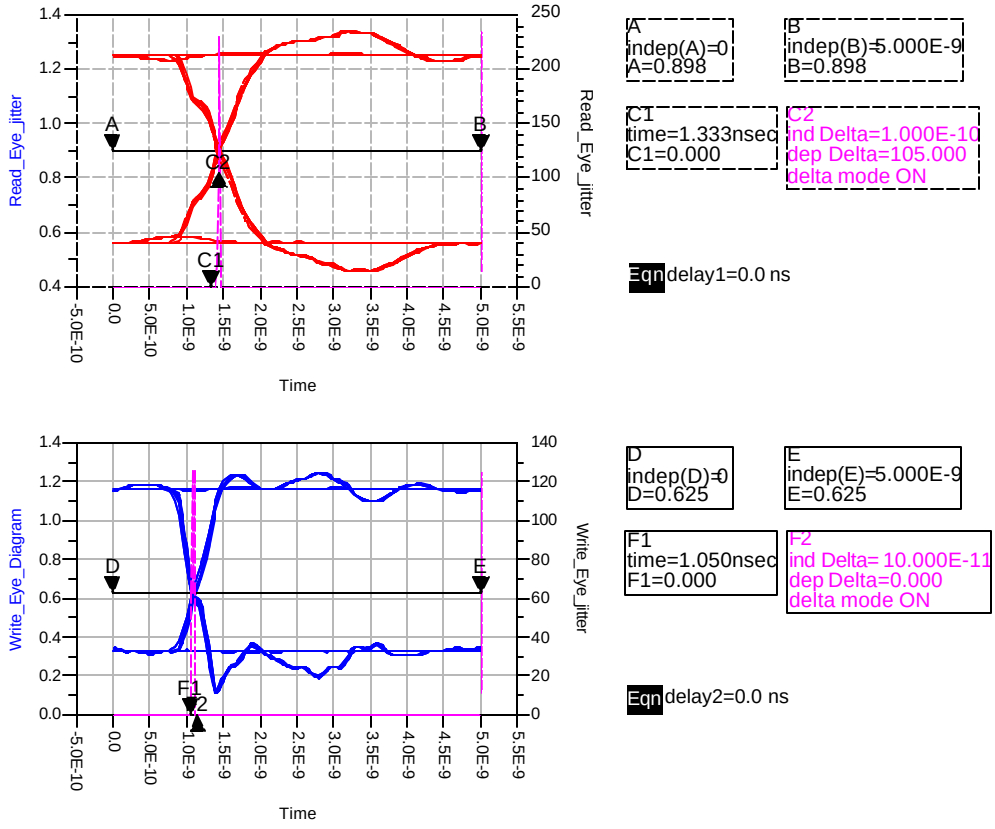

Figure 2-24 Near End Single Series / Dual Parallel Termination Jitter Analysis Results, Fly-By.

2.1.7 Far End Single Series / Dual Parallel Termination (Fly-By)

This topology, depicted in Figure 2-25, requires one series resistors and two parallel resistors.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-26, Figure 2-27 and Figure 2-28 respectively. This topology is useful when output drive strength or output impedance of both devices is different. The addition of one resistor makes this topology asymmetrical, so the performance during the read/write cycles will be different. This characteristic can be used to optimized one of the read or write cycles. Looking at the waveforms, it is clear that the signal integrity during the read cycle is better that the write cycle.
The high impedance shown at the input of an active device makes the Fly-By option well suited for minimum components, good performance and low sensitivity topology. The eye closure at the Stratix during the read cycle is 0.947 and at the QDR-II during the write cycle is 0.870 respectively. The performances of this topology will warranties the functionality of the link during the read and write cycles.

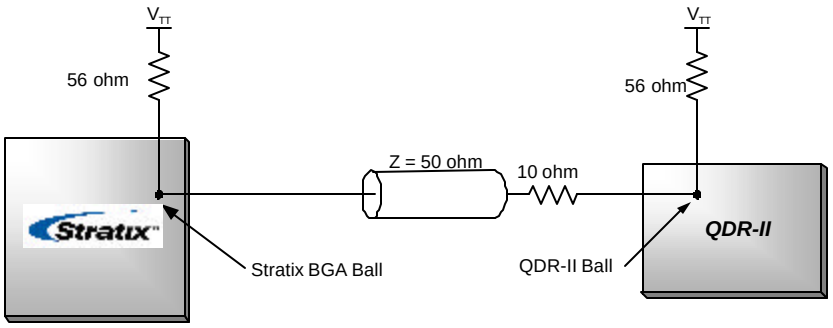

Figure 2-25 Far End Single Series / Dual Parallel Termination (Fly-By)

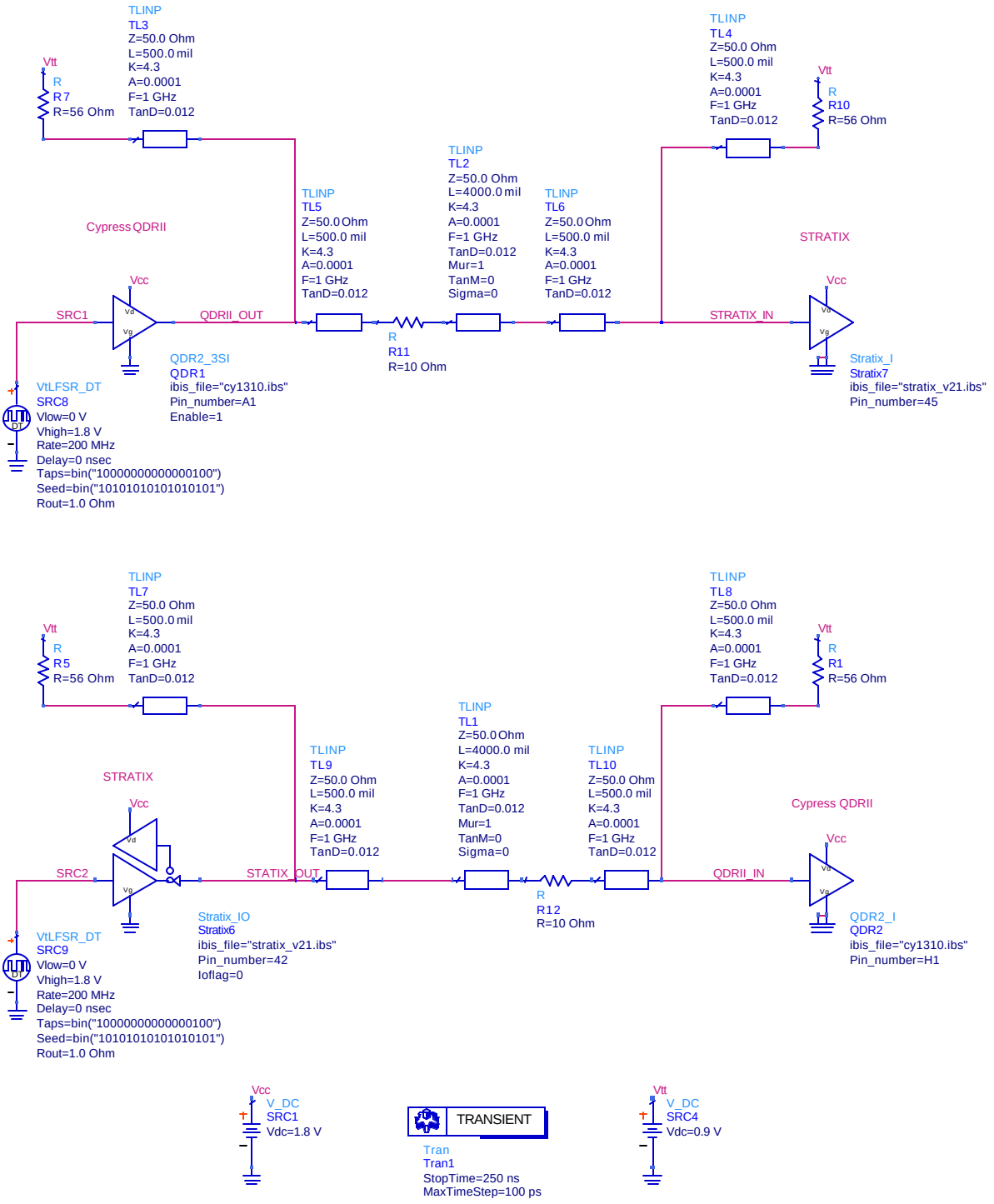

Figure 2-26 Far End Single Series / Dual Parallel Termination Simulation Setup Read/Write Cycles (Fly-By)

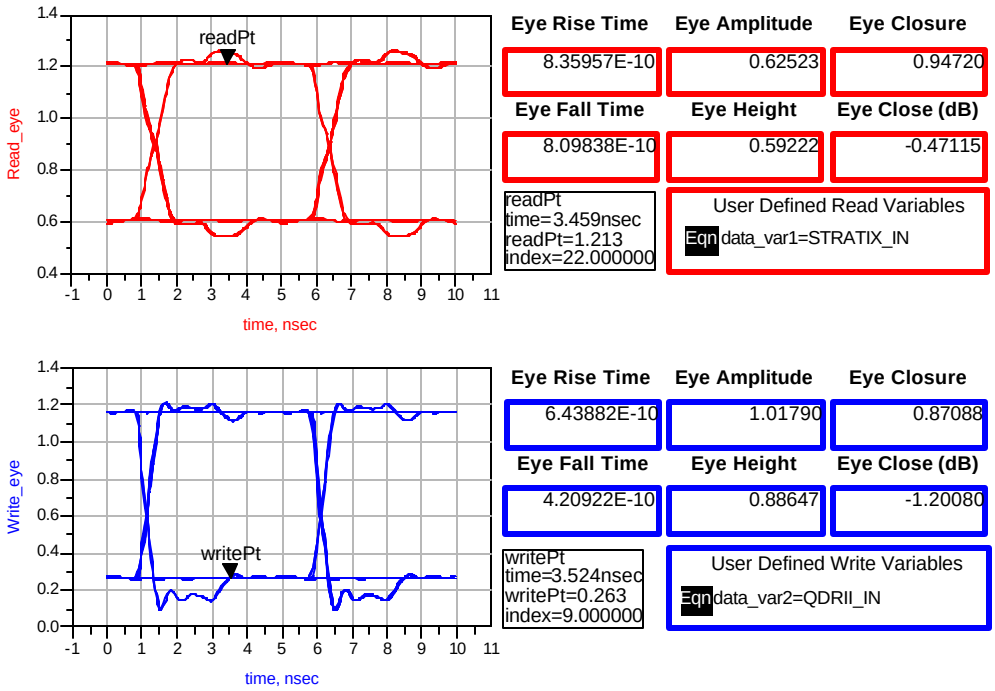

Figure 2-27 Near End Single Series / Dual Parallel Termination Eye Analysis Results, Fly-By

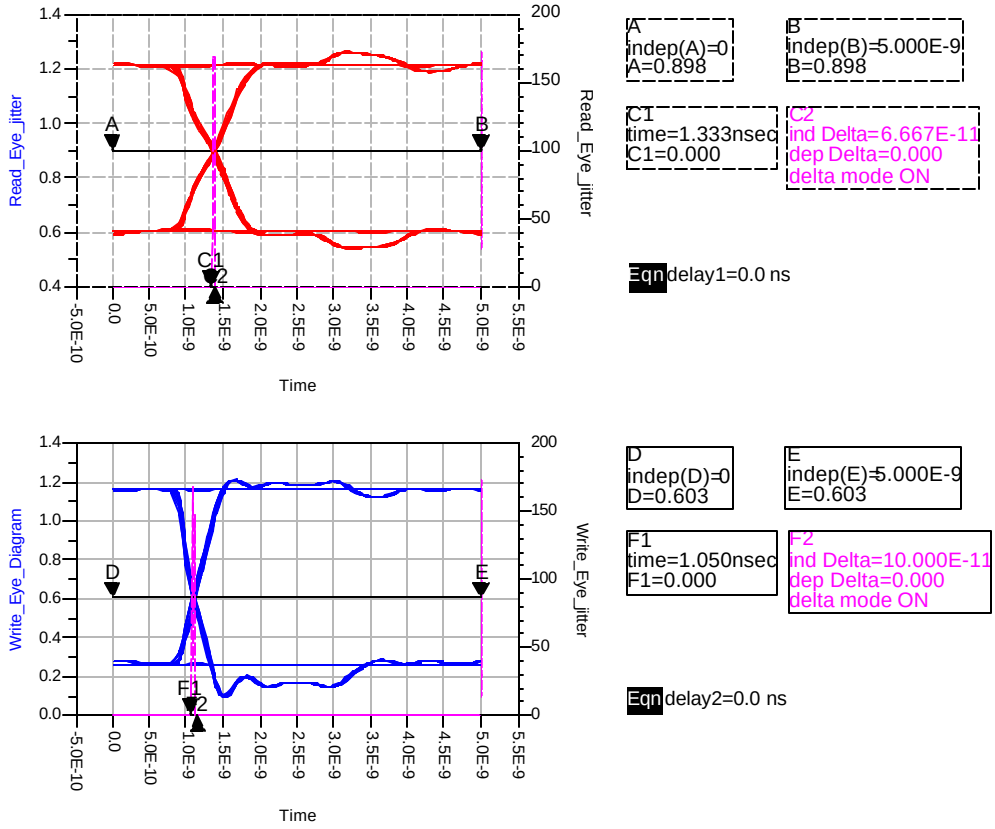

Figure 2-28 Far End Single Series / Dual Parallel Termination Jitter Analysis Results, Fly-By

2.1.8 Far End Single Series / Dual Parallel Termination (Non-Fly-By)

This topology, depicted in Figure 2-29, requires one series resistors and two parallel resistors.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-30, Figure 2-31 and Figure 2-32 respectively. This topology and the previews one are useful when output drive strength or output impedance of both devices are different. The addition of one resistor makes this topology asymmetrical, so the performance during the read/write cycles will be different. This characteristic can be used to optimized one of the read or write cycles. Looking at the waveforms, it is clear that the signal integrity during the write cycle is better than the read cycle.
The approach depicted in Figure 2-29 is an option when the routing in high density areas makes the previews topology difficult to achieve. The most important parameter to consider is the distance from the termination resistor to the input of the device in order to minimize undesired standing waves. The eye closure at the Stratix during the read cycle is 0.834 and at the QDR-II during the write cycle is 0.906 respectively. The performances of this topology will warranties the functionality of the link during the read and write cycles.

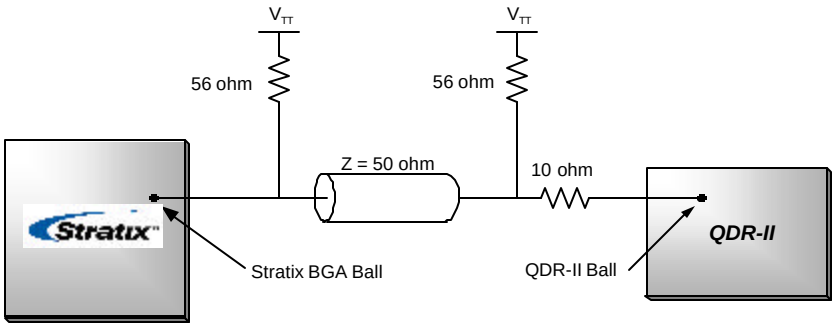

Figure 2-29 Far End Single Series / Dual Parallel Termination (Non-Fly-By)

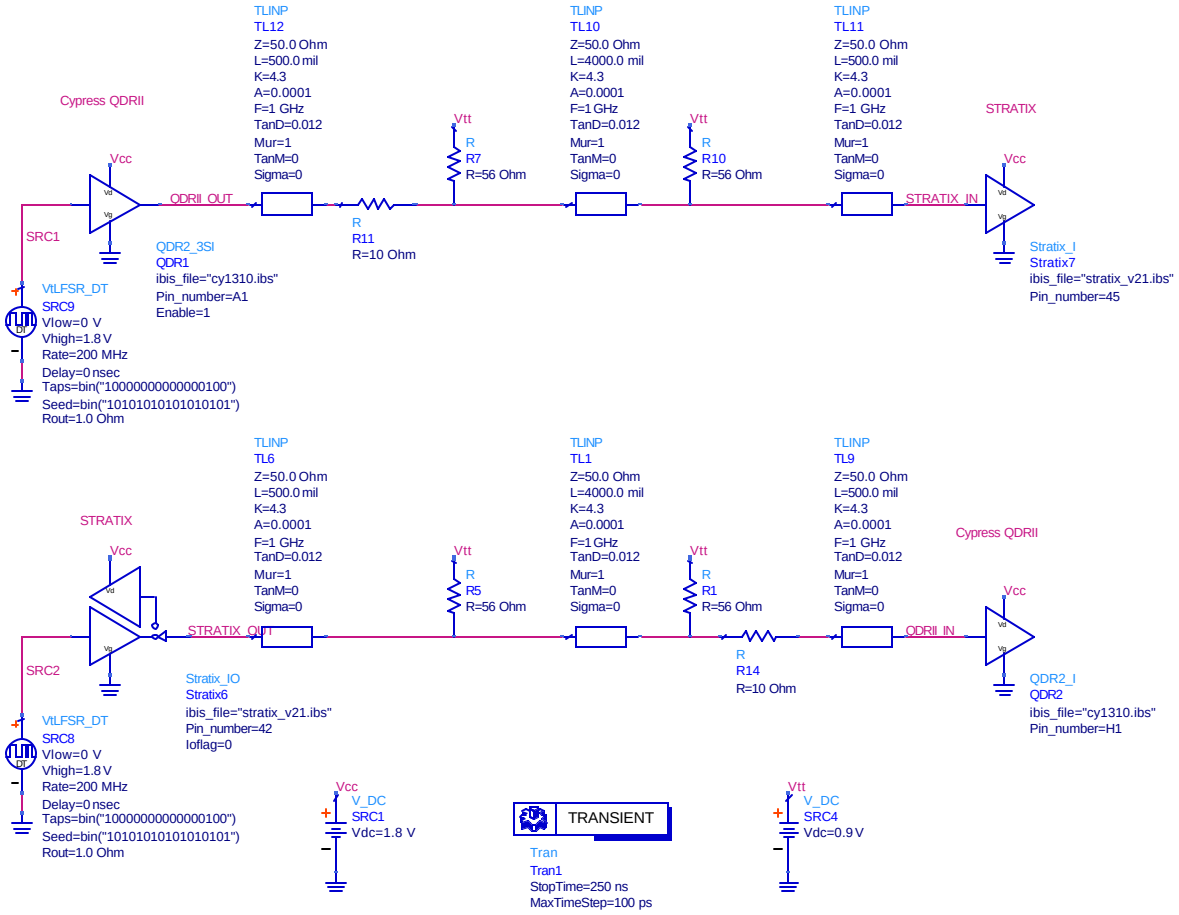

Figure 2-30 Far End Single Series / Dual Parallel Termination Simulation Setup Read/Write Cycles, Non Fly-By

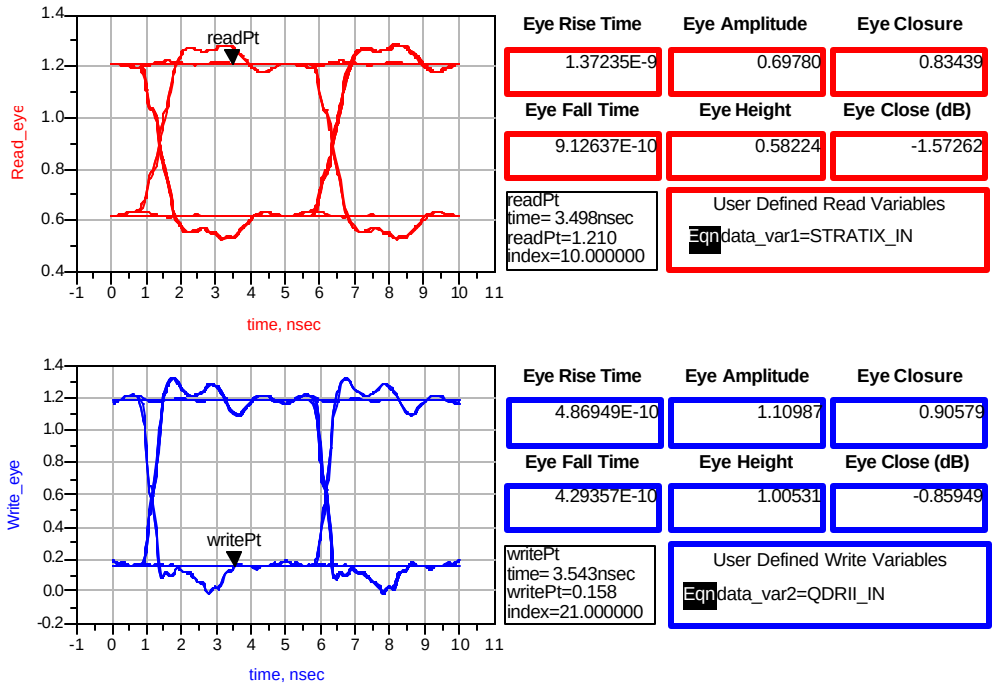

Figure 2-31 Far End Single Series / Dual Parallel Termination Eye Analysis Results, Non Fly-By.

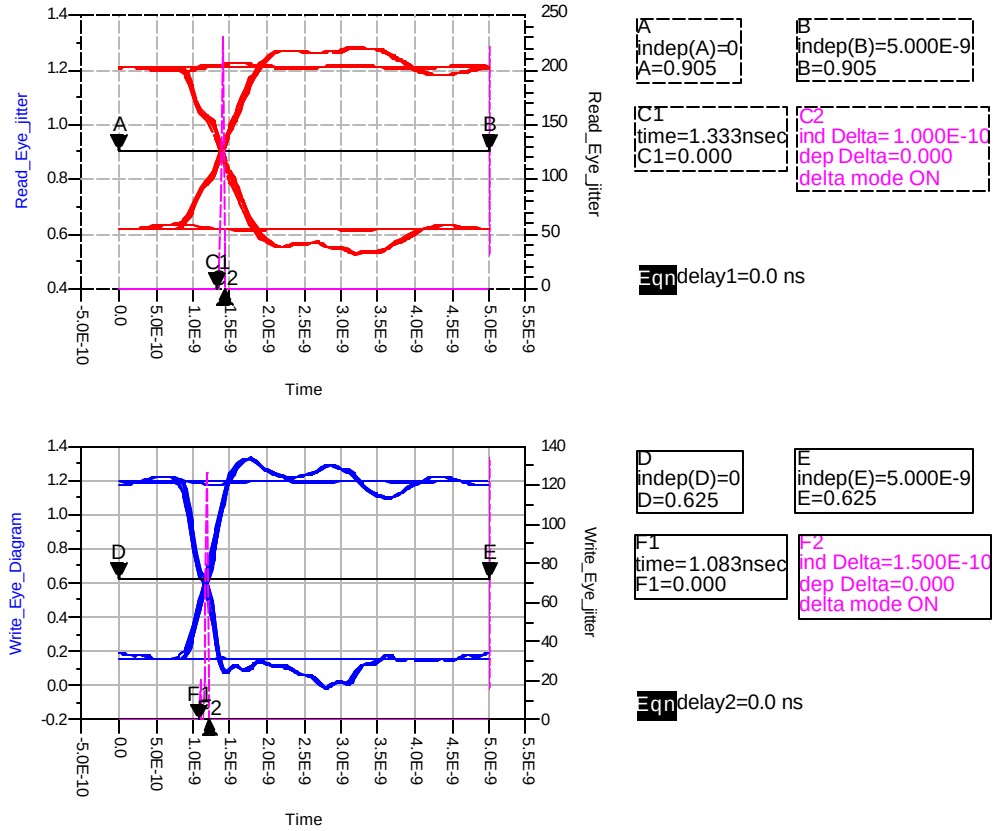

Figure 2-32 Far End Single Series / Dual Parallel Termination Jitter Analysis Results, Non Fly-By

2.1.9 Single Near End Series / Far End Parallel Termination, (Fly-By)

This topology, depicted in Figure 2-33, requires one series resistors and one parallel resistors.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-34, Figure 2-35 and Figure 2-36 respectively.

The approach depicted in Figure 2-33 is an option when unidirectional signals, low component count and short distances are the goal. The series resistor should be located close to the driver and the parallel termination close to the destination (receiver). Looking at the waveforms, it is clear that the signal integrity during the write cycle is much better than the read cycle making this configuration especially well suited for write cycles. The use of this topology in bi-directional transmission lines requires the verification of the min/max input voltage at the device. The eye closure at the Stratix during the read cycle is 0.705 and at the QDR-II during the write cycle is 0.836 respectively. The performances of this topology will warranties the functionality of the link during for write cycles.

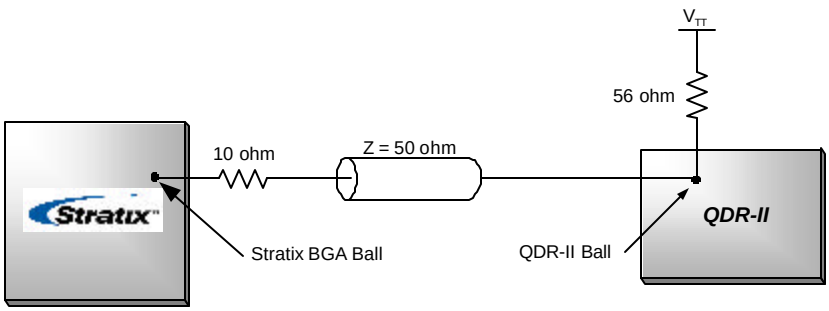

Figure 2-33 Single Near End Series / Far End Parallel Termination (Fly-By)

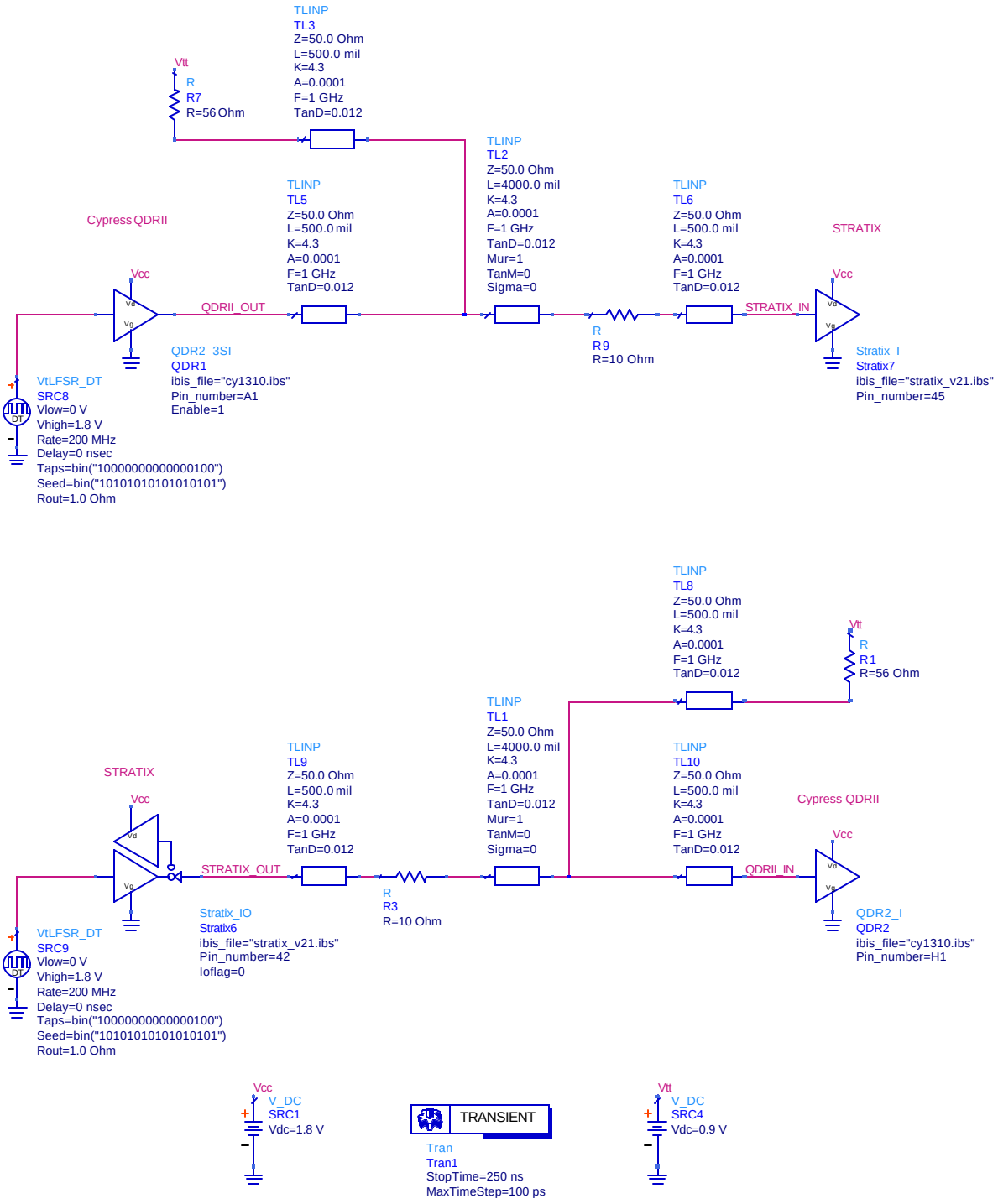

Figure 2-34 Single Near End Series / Far End Parallel Termination Simulation Setup Read/Write Cycles (Fly-By)

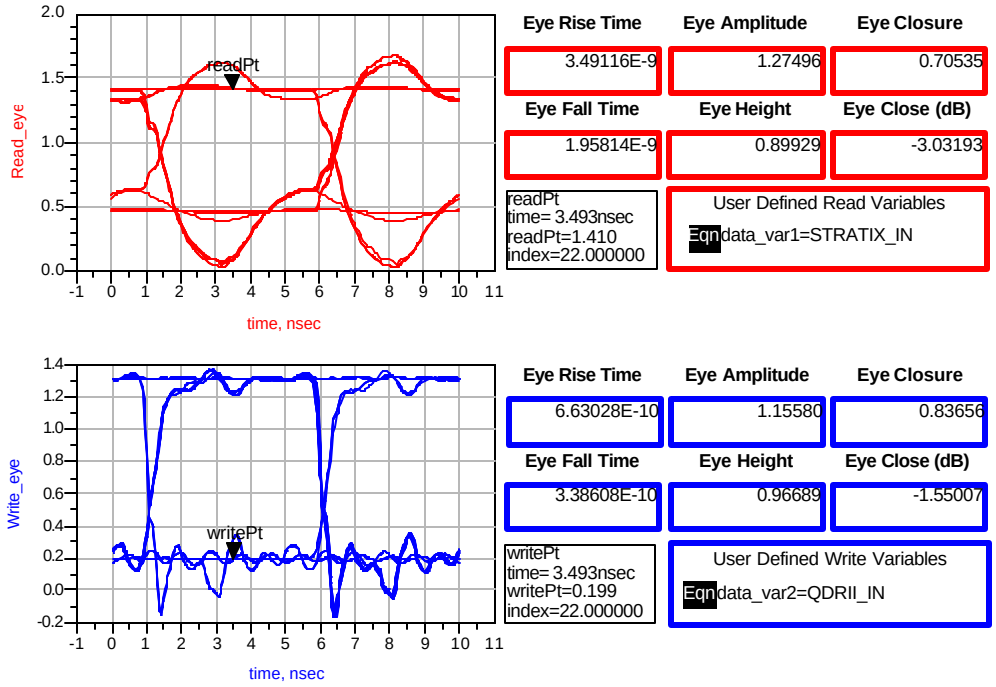

Figure 2-35 Single Near End Series / Far End Parallel Termination Eye Analysis Results, Fly-By.

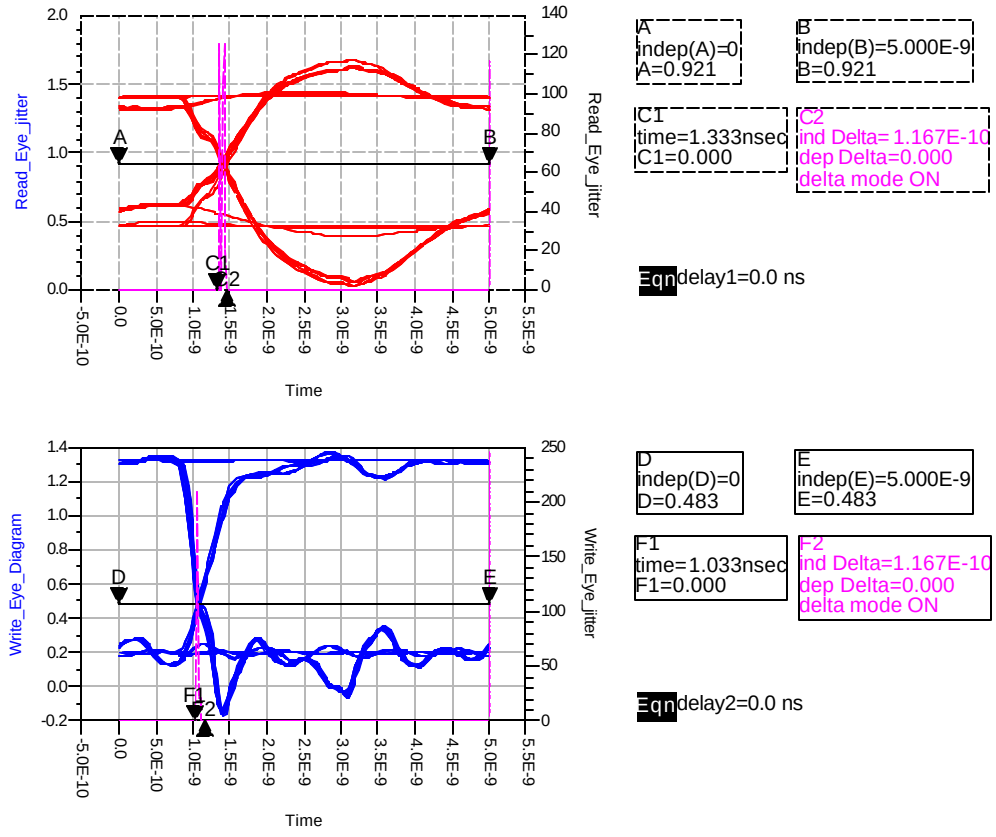

Figure 2-36 Single Near End Series / Far End Parallel Termination Jitter Analysis Results, Fly-By

2.1.10 Single Near End Series / Far End Parallel Termination (Non-Fly-By)

This topology, depicted in Figure 2-37, requires one series resistors and one parallel resistor.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-38, Figure 2-39 and Figure 2-40 respectively.

The approach depicted in Figure 2-37 is an option when unidirectional signals, low component count and short distances are the goal. The series resistor should be located close to the driver and the parallel termination close to the destination (receiver). Looking at the waveforms, it is clear that the signal integrity during the write cycle is much better than the read cycle making this configuration especially well suited for write cycles. The use of this topology in bi-directional transmission lines requires the verification of the min/max input voltage at the device. The eye closure at the Stratix during the read cycle is 0.680 and at the QDR-II during the write cycle is 0.861 respectively. The performances of this topology will warranties the functionality of the link during for write cycles.

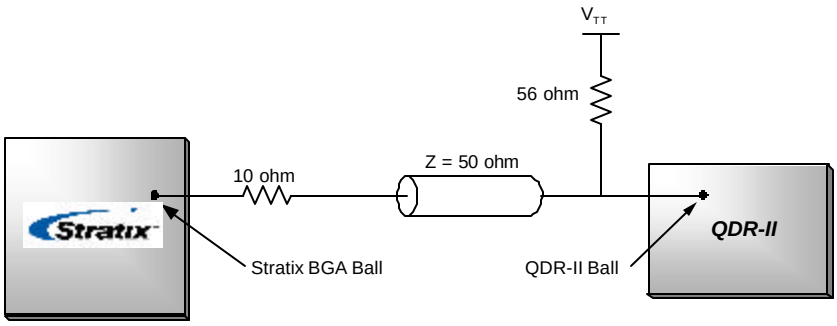

Figure 2-37 Single Near End Series / Far End Parallel Termination (Non-Fly-By)

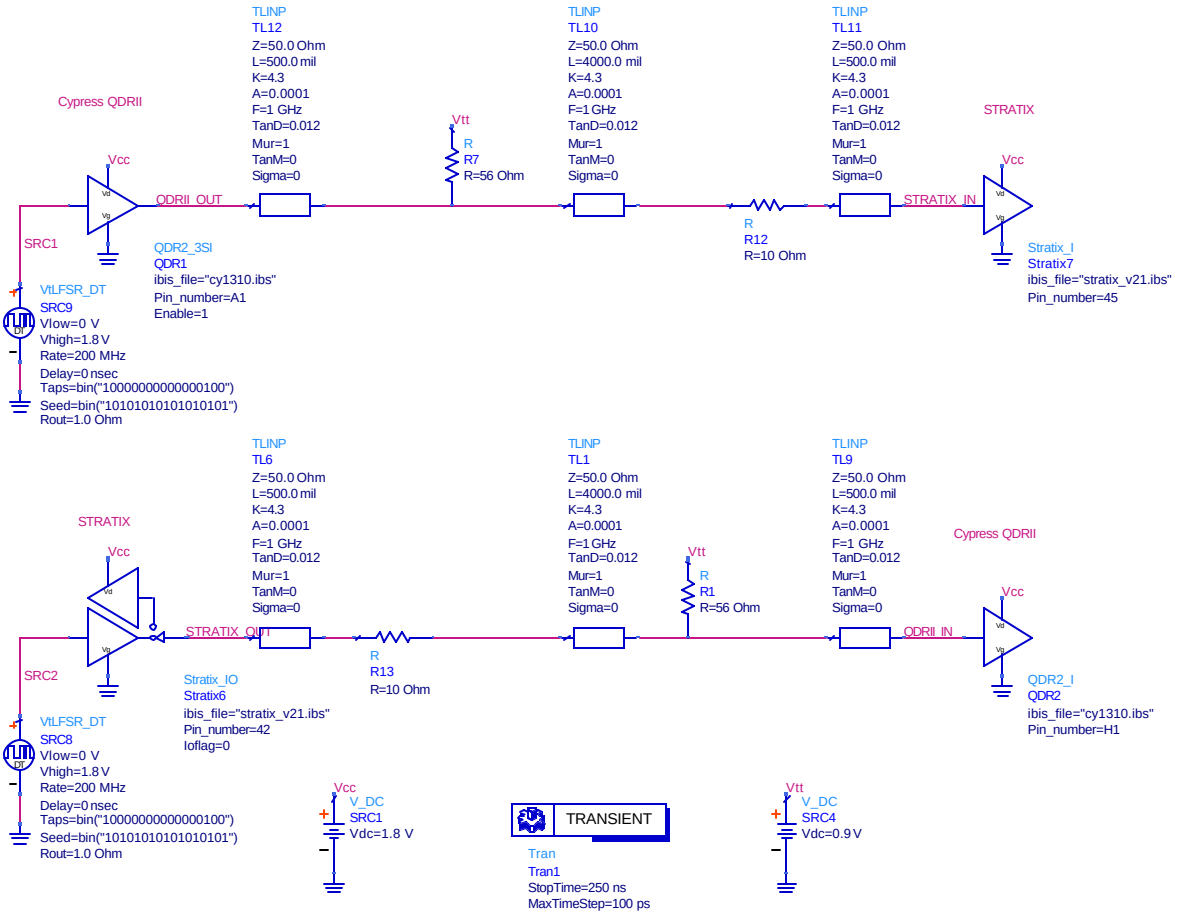

Figure 2-38 Single Near End Series/Far End Parallel Termination Simulation Setup Read/Write Cycles (Non-Fly-By)

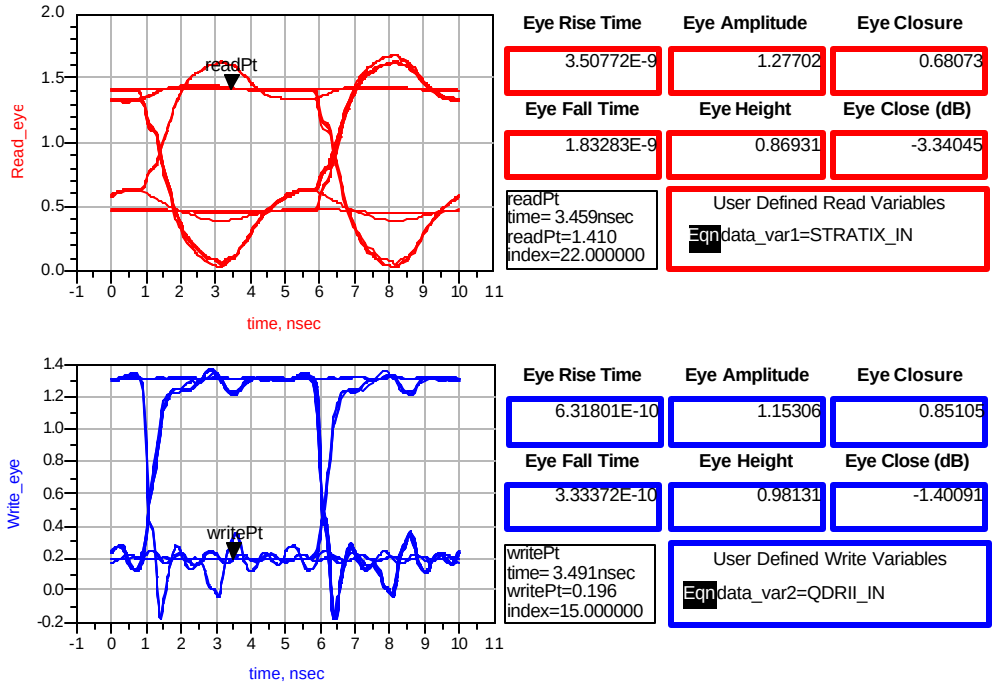

Figure 2-39 Single Near End Series / Far End Parallel Termination Eye Analysis Results.

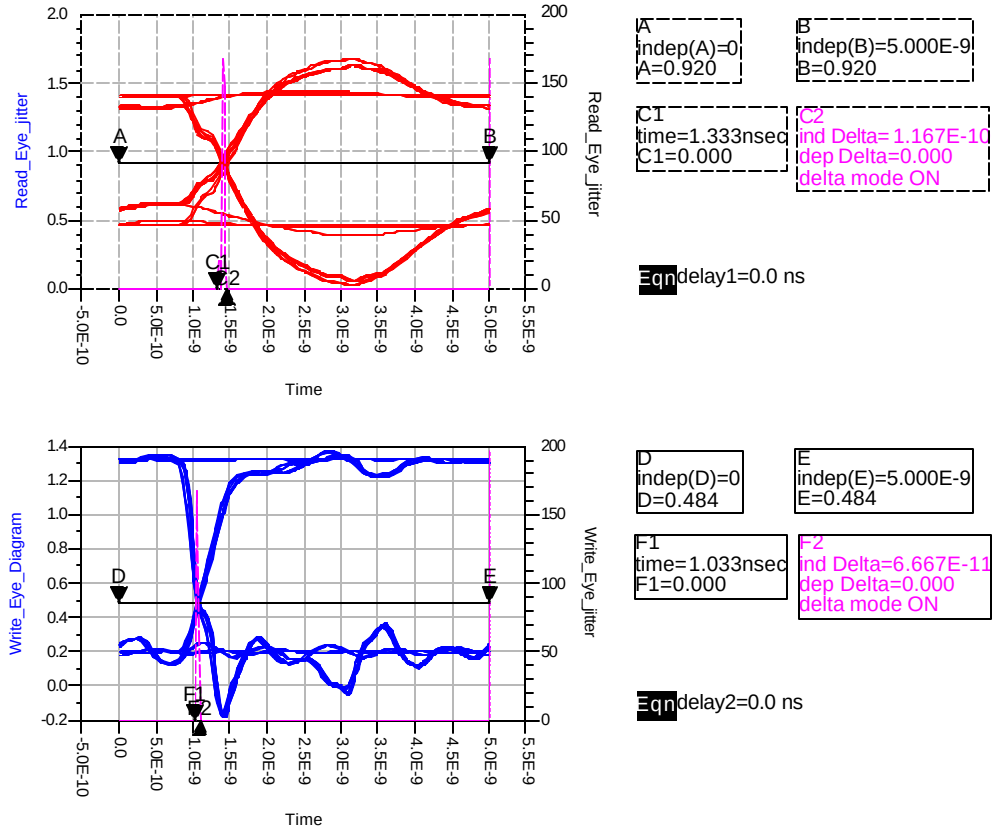

Figure 2-40 Single Near End Series / Far End Parallel Termination Jitter Analysis Results.

2.1.11 Single Near End Series / Far End Parallel Termination, (Fly-By)

This topology, depicted in Figure 2-41, requires two series resistors and one parallel resistor.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-42, Figure 2-43 and Figure 2-44 respectively.

The approach depicted in Figure 2-41 would work fine for "write" direction only, but overall due to the poor performance of the read direction, this scheme should be avoided. In addition the component count is higher with any improve in performance. The eye closure at the Stratix during the read cycle is 0.855 and at the QDR-II during the read cycle is 0.601 respectively. The performances of this topology will warranties the functionality of the link during for read cycles but with very limited performance during the write cycles.

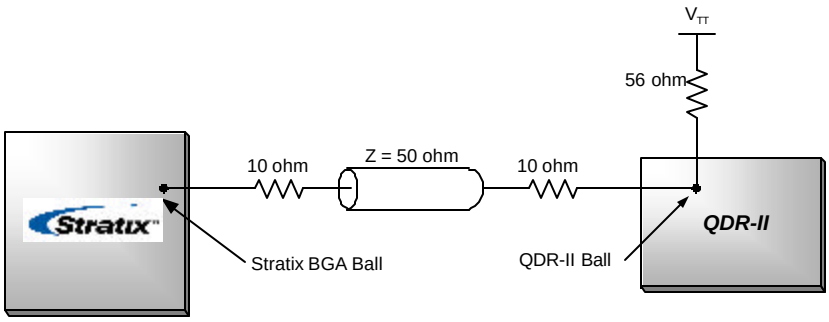

Figure 2-41 Single Near End Series / Far End Parallel Termination, (Fly-By)

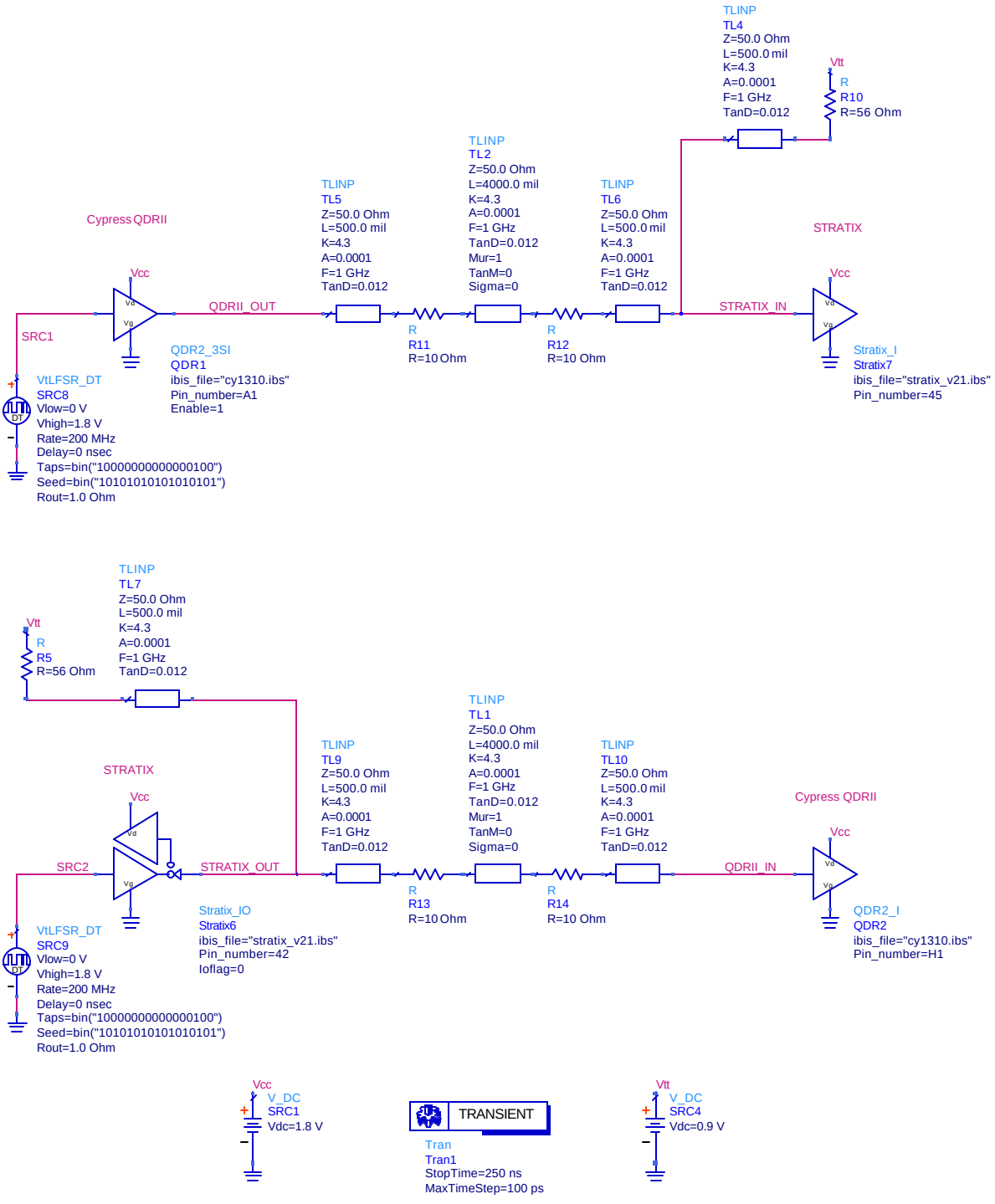

Figure 2-42 Single Near End Series/Far End Parallel Termination Simulation Setup Read/Write Cycles , (Fly-By)

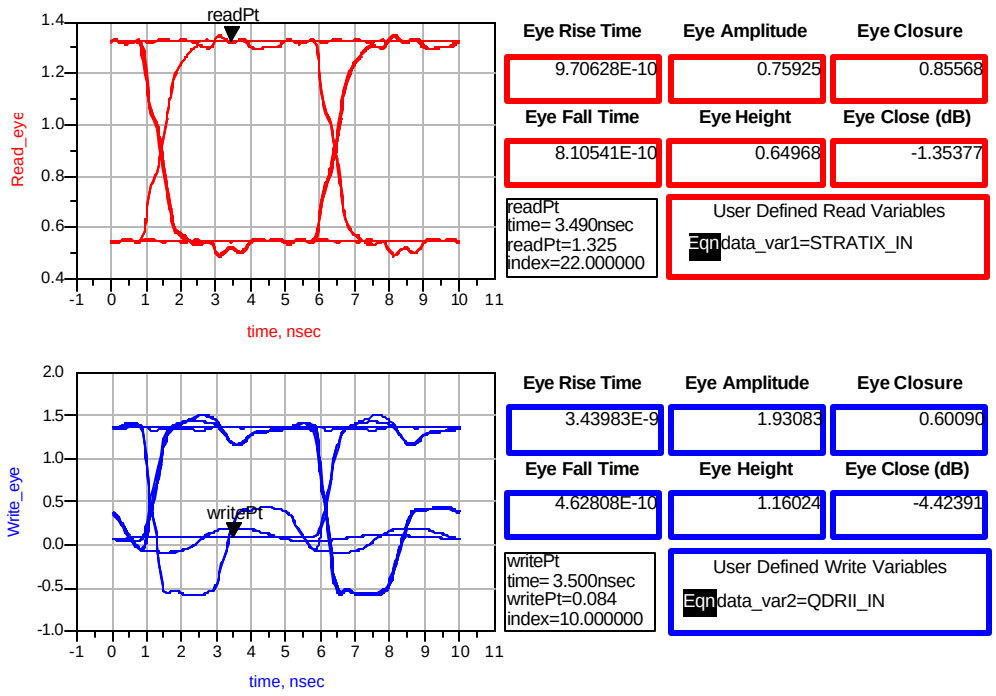

Figure 2-43 Single Near End Series / Far End Parallel Termination Eye Analysis Results, Fly-By

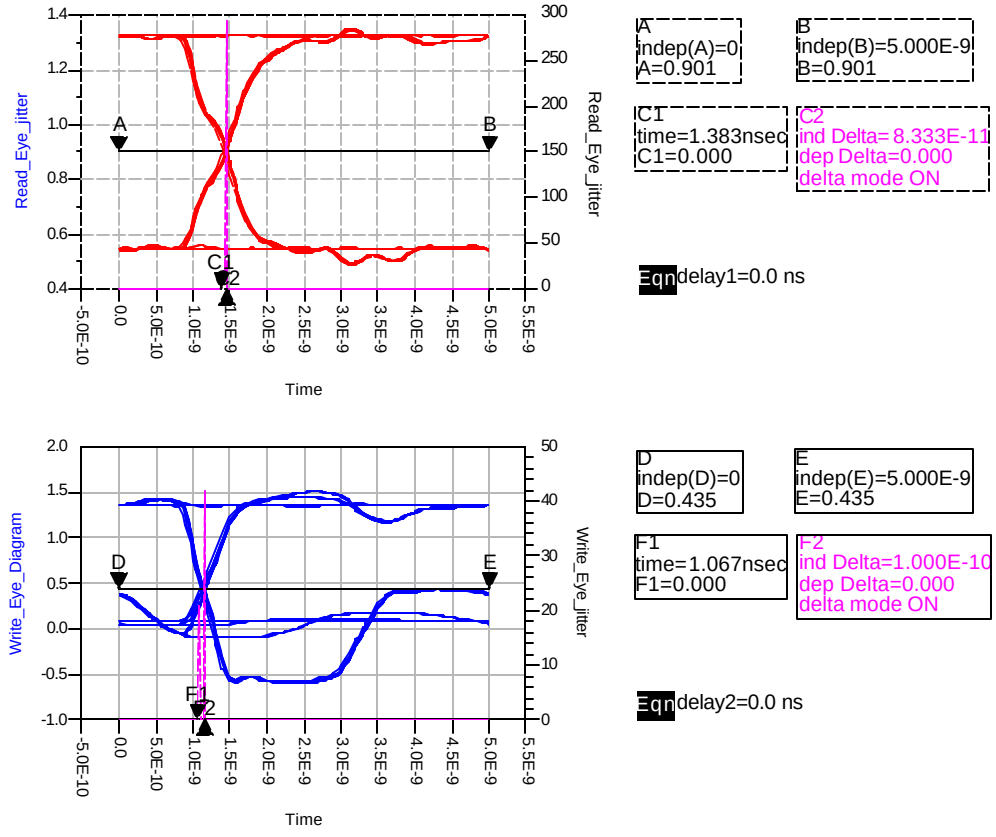

Figure 2-44 Single Near End Series / Far End Parallel Termination Jitter Analysis Results, Fly-By

2.1.12 Dual End Series / Near End Parallel Termination, (Non-Fly-By)

This topology, depicted in Figure 2-45, requires two series resistors and one parallel resistor.

The ADS test setup, eye analysis and jitter analysis for the read/write cycles are shown in Figure 2-46, Figure 2-47 and Figure 2-48 respectively.

The approach depicted in Figure 2-45 would work fine for "read" direction only, but overall due to the poor performance of the write direction, this scheme should be avoided. In addition the component count is higher with any improve in performance. The eye closure at the Stratix during the read cycle is 0.708 and at the QDR-II during the read cycle is 0.887 respectively. The performances of this topology will warranties the functionality of the link during for write cycles but with very limited performance during the read cycles.

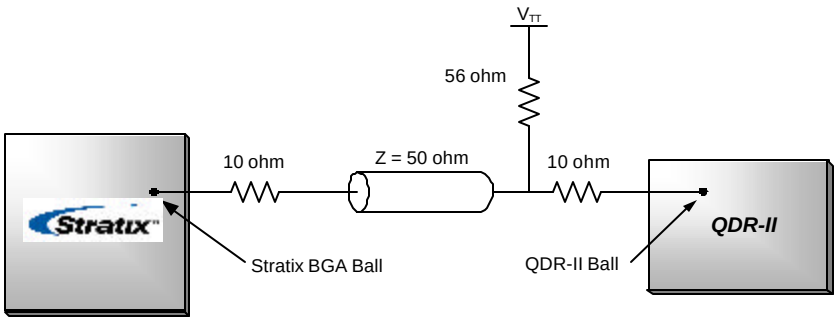

Figure 2-45 Dual End Series / Far End Parallel Termination, (Non-Fly-By)

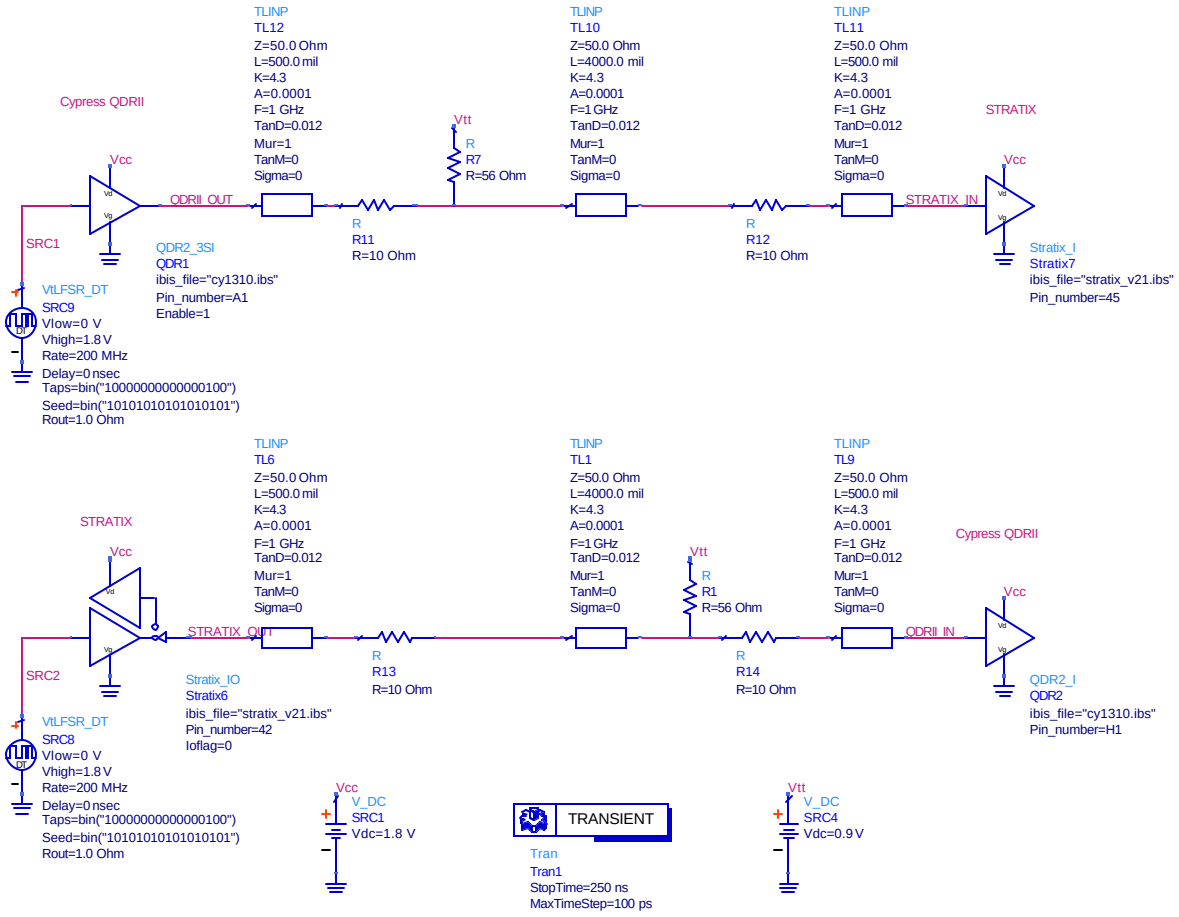

Figure 2-46 Single Near End Series/Far End Parallel Termination Simulation Setup Read/Write Cycles, (Non-Fly-By)

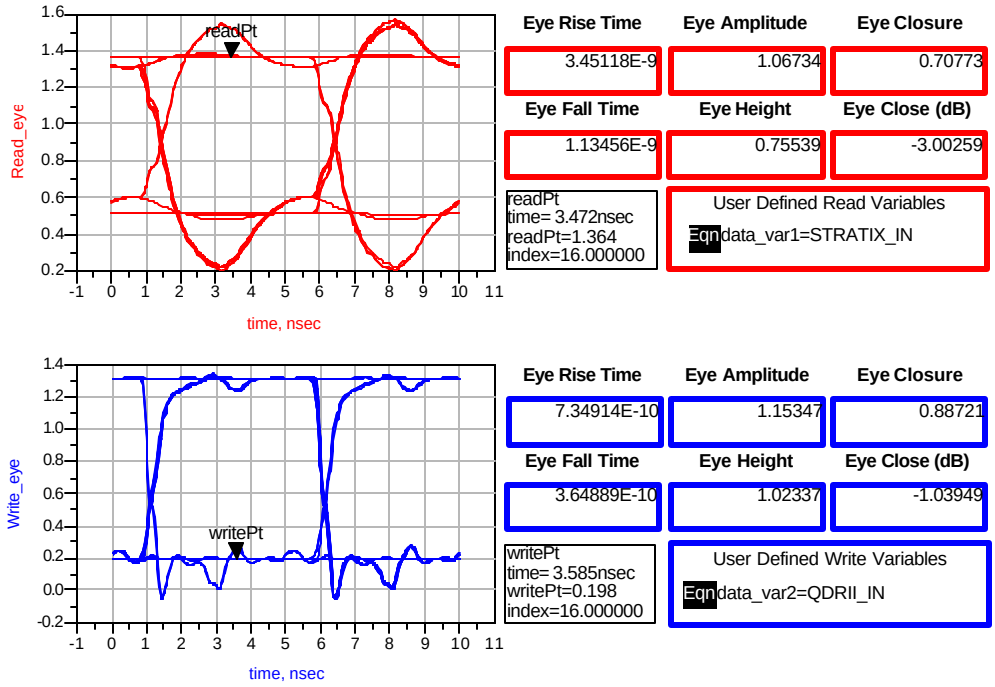

Figure 2-47 Single Near End Series / Far End Parallel Termination Eye Analysis Results

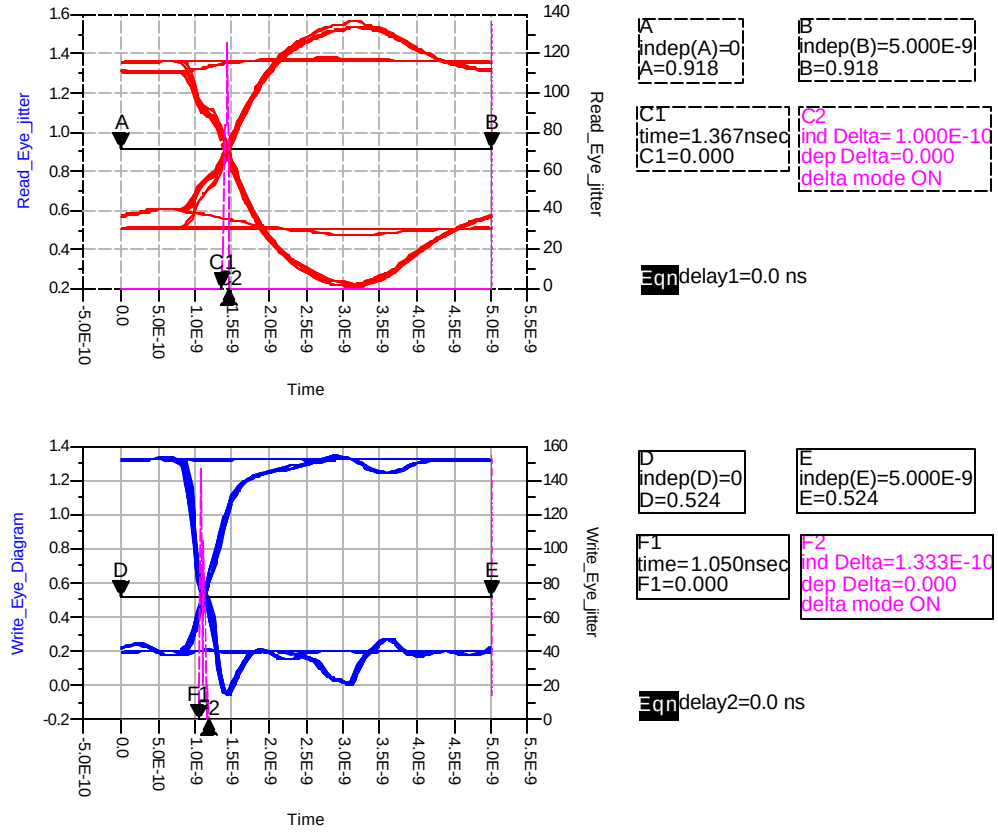

Figure 2-48 Single Near End Series / Far End Parallel Termination Jitter Analysis Results

2.1.13 HSTL-II Multi load Data Interface

The address bus and clocks are often shared among several DDR devices on the board, so it is harder to achieve good signal integrity on the address bus. This section shows a typical dual device system for increased memory. The bit routing topology and a proposed termination scheme is shown in Figure 2-49 **Stratix-QDR-II data write Interface.**.

Figure 2-49 shows the block diagram of this dual device scheme. Figure 2-50, Figure 2-51 shows the ADS test setup and Figure 2-52 shows the simulated waveform at the QDR-II memory pins. While there is overshoot, the overall eye closure is 0.546 at the QDR-II device terminals during the write and .0.719 at the Stratix during the read cycle.

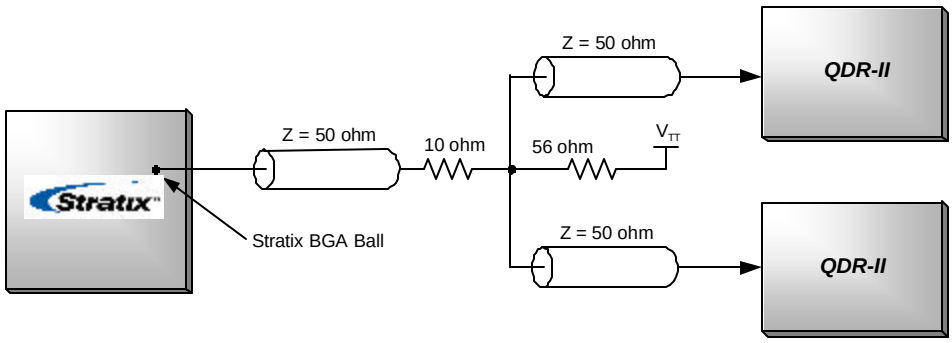

Figure 2-49 Stratix-QDR-II data write Interface.

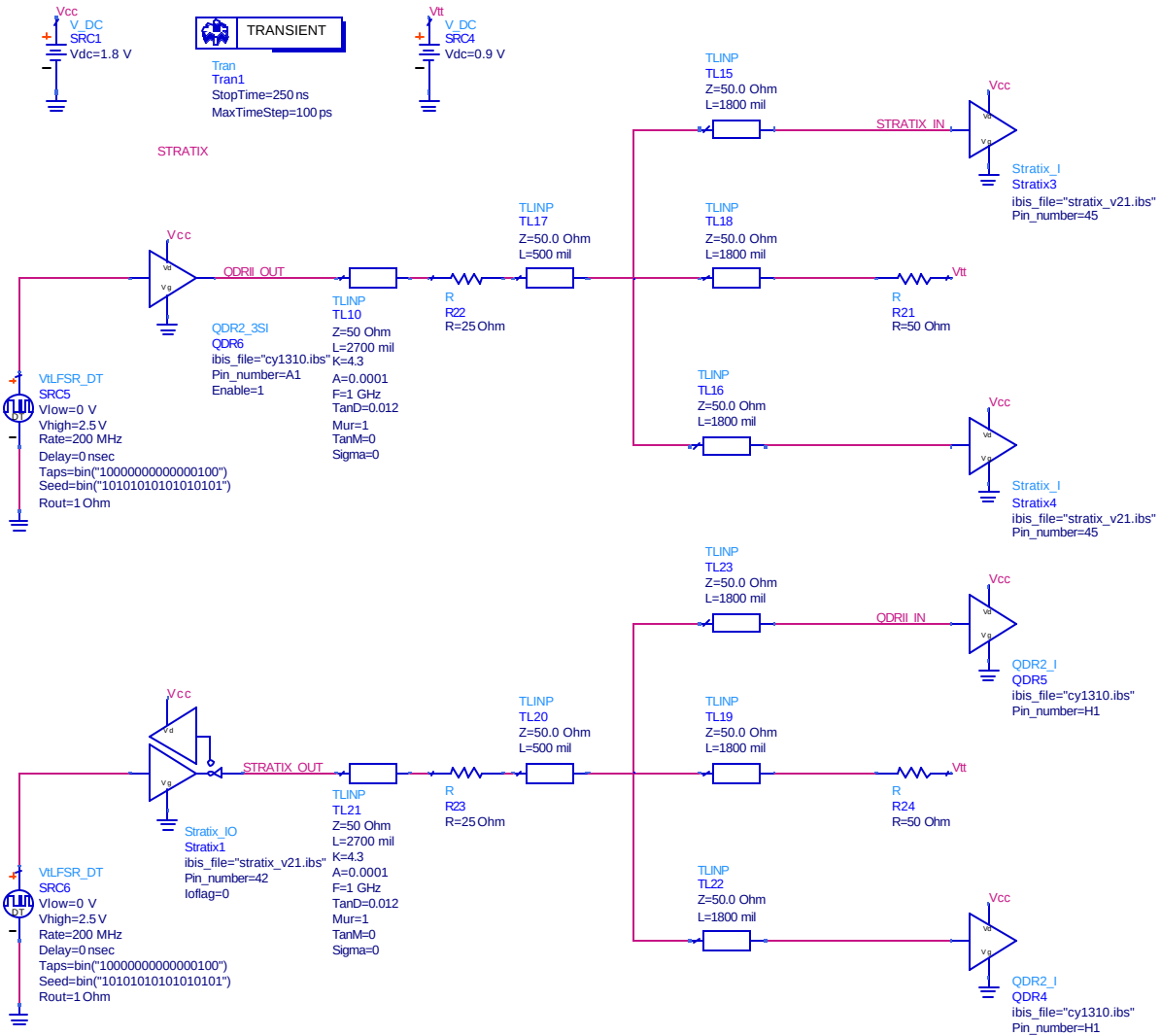

Figure 2-50 Stratix-QDR-II Data Read/Write Interface, Simulation Setup.

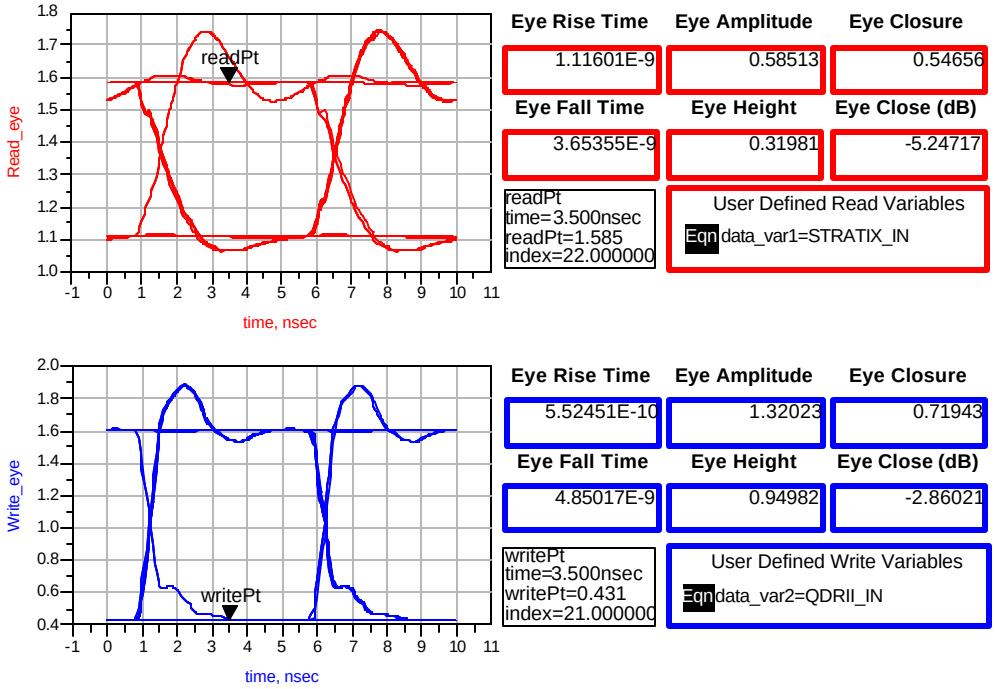

Figure 2-51 Stratix-QDR-II Data Interface, Eye Analysis.

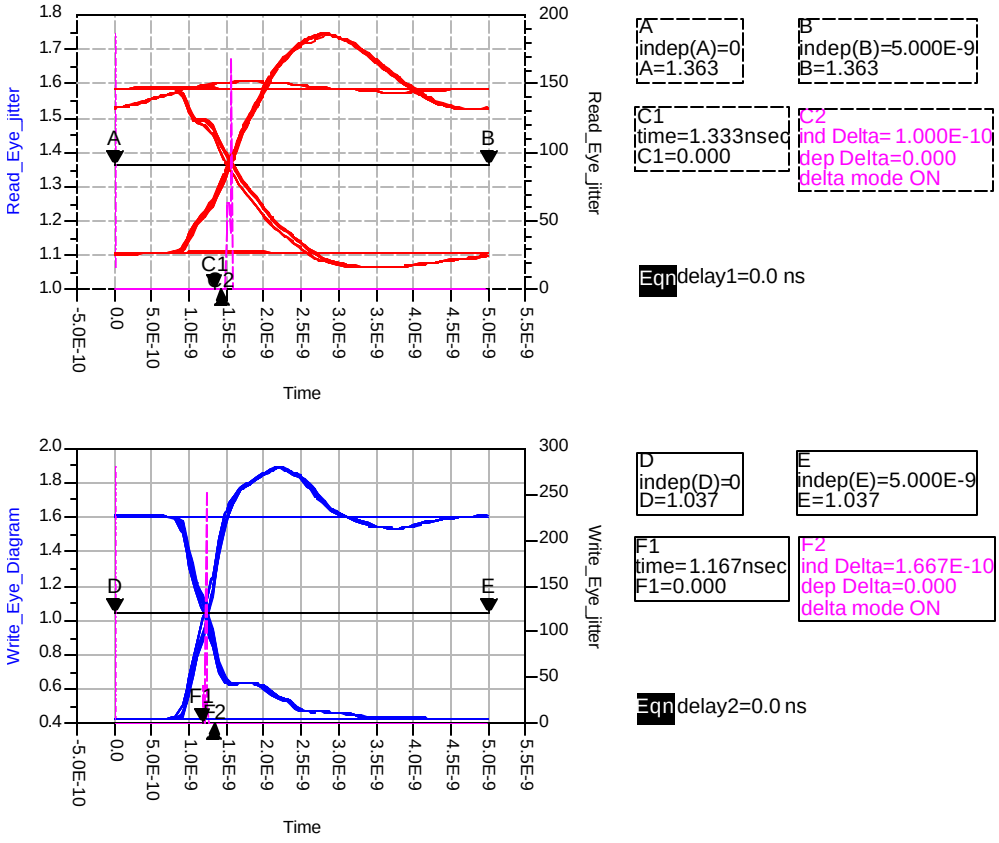

Figure 2-52 Stratix-QDR-II Data Interface, Jitter Analysis.

3 POST LAYOUT SIMULATIONS

When the layout is complete, a post layout simulation is performed on the critical sections of the board to ensure there are no major signal integrity problems. Based on the results of the post-layout simulation, any changes required are incorporated in the layout and the layout is released to the fabrication house for board manufacturing.

The post layout simulation process requires the Gerbers files of all active layers on the board, the actual permitivity, loss tangent and thickness of the all dielectrics layers, the copper thickness in every layer as long as the relevant solder mask information.

3.1 QDRII Q0

The post-layout simulations for the QDR-II Q0 in based on the S-Parameters of the data path from the Stratix I/O to the QDR-II I/O pins. The S-Parameters were obtained from 10MHz to 2GHz and included as a black box in the simulation set up shown in Figure 3-3.

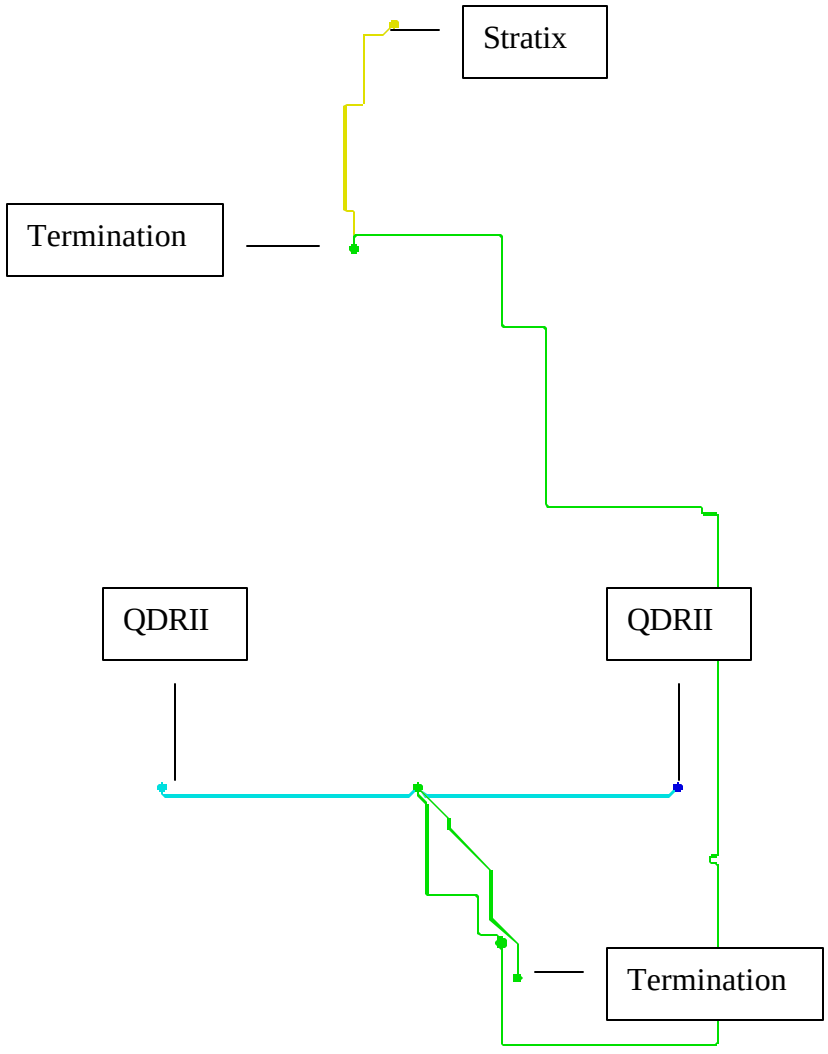

Figure 3-1 Stratix-QDR-II Data Q0 Interface Layout.

3.2 QDRII D0

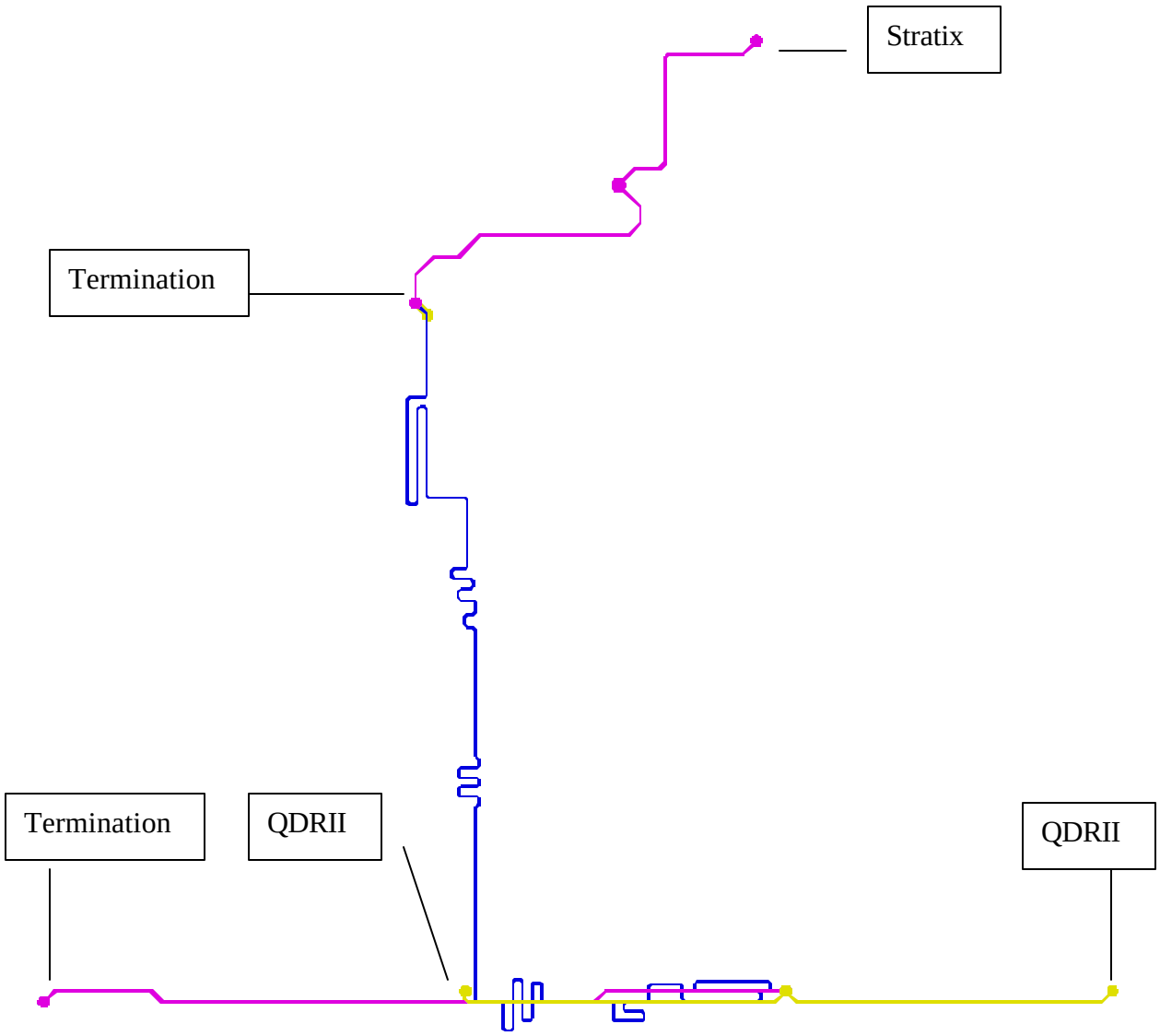

Figure 3-2 Stratix-QDR-II Data D0 Interface Layout.

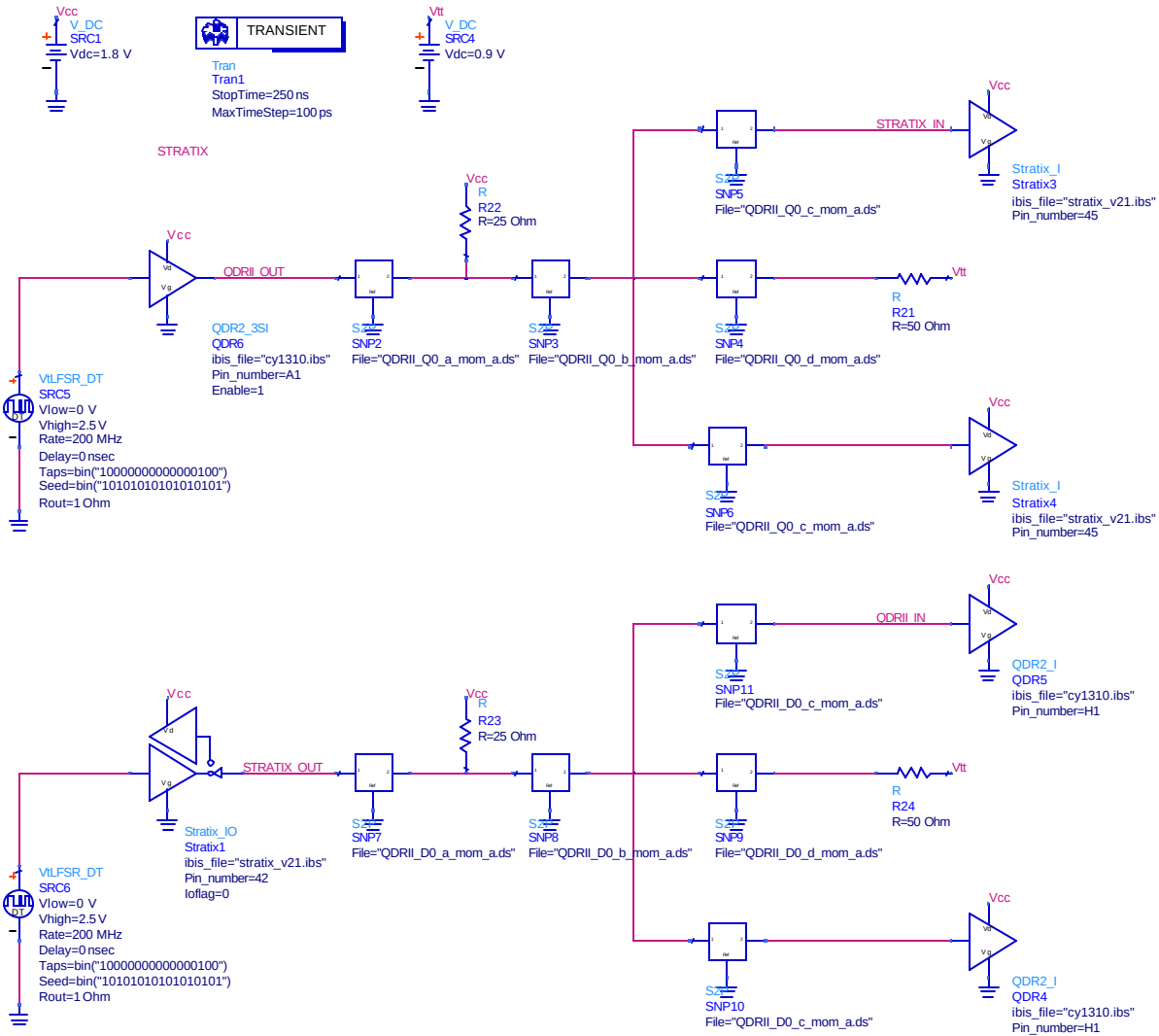

Figure 3-3 Stratix-QDR-II Data Read/Write (D0 and Q0) Interface, Post Layout Simulation Setup.

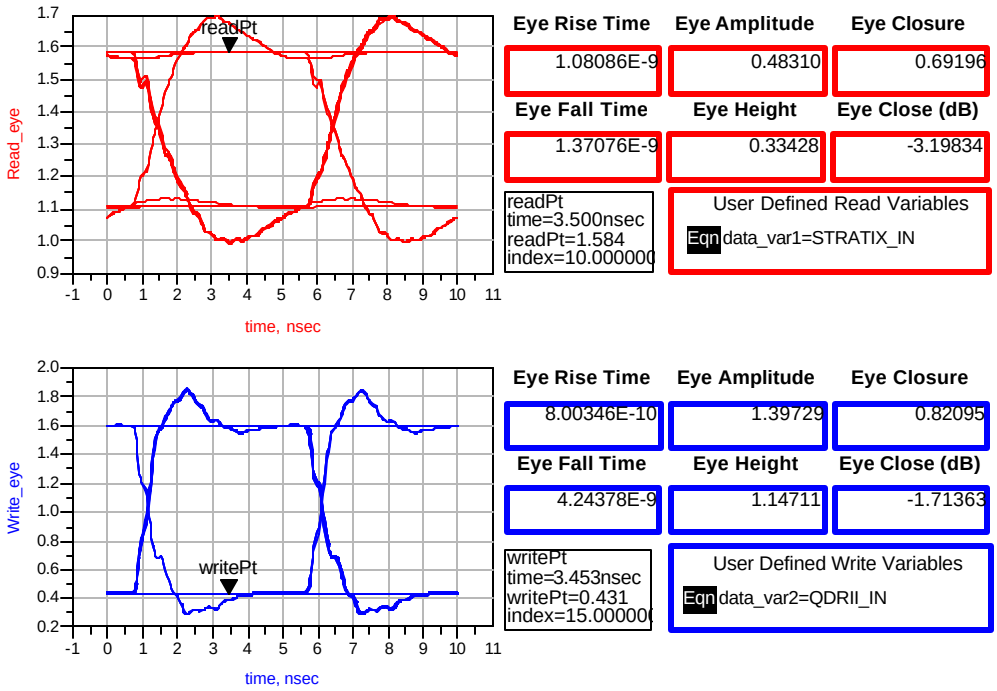

Figure 3-4 Stratix-QDR-II Data Read/Write Interface, Post Layout Eye Analysis.

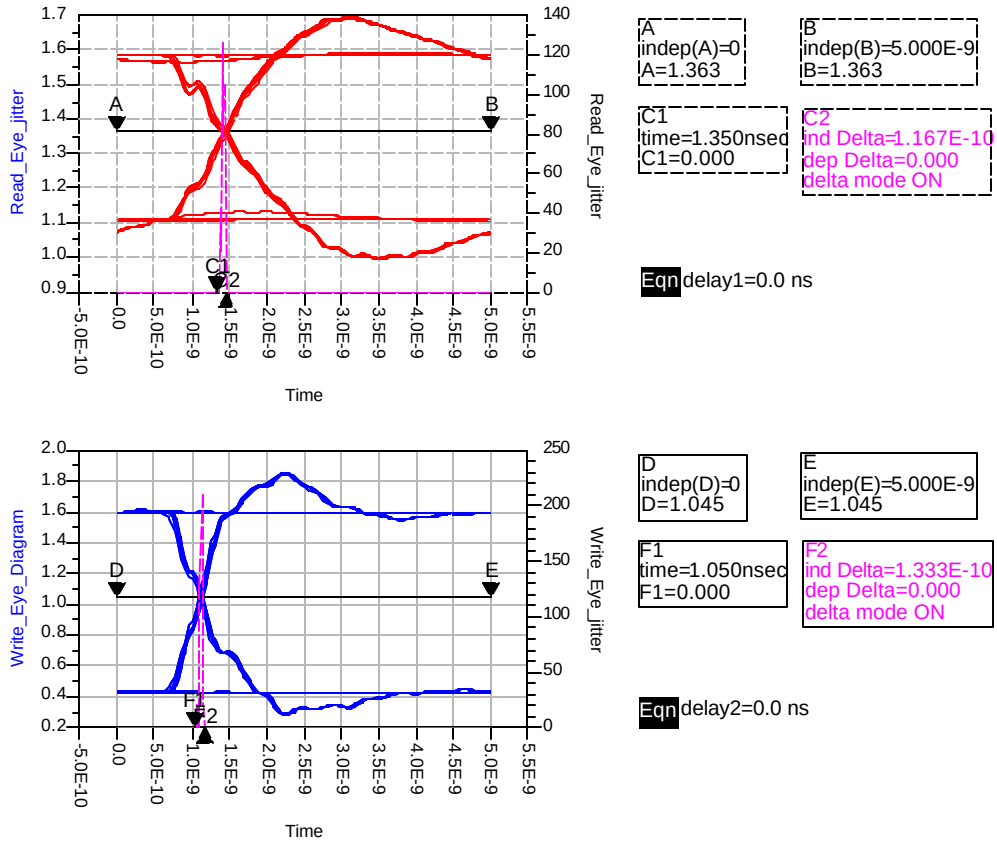

Figure 3-5 Stratix-QDR-II Data Read/Write Interface, Post Layout Jitter Analysis.

4 CONCLUSION

Based on the simulation results, the following schemes show the best performance for Stratix to QDR-II memory device bi-directional buses:

2.1.1 Dual Series/Dual Parallel Termination (Fly-By)
2.1.2 Dual Series/Dual Parallel Termination (Non-Fly-By)
2.1.3 Dual Parallel Termination (Fly-By)
2.1.4 Dual Parallel Termination (Non-Fly-By)

Based on the simulation results, the following schemes show the best performance for Stratix to QDR-II memory device unidirectional buses:

2.1.9 Single Near End Series / Far End Parallel Termination, (Fly-By)
2.1.10 Single Near End Series / Far End Parallel Termination (Non-Fly-By)

The best scheme based on performance/component ratio and memory size appears to be 2.1.13. The Stratix Memory Board 2 (SMB2) uses this.

5 FURTHER WORK

These simulations should correlate with the measurements.