The Programmable Solutions Company®

Stratix™ Memory Board II Rev A

User Guide
Rev 0.2

High Speed / End Applications Team
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1 Introduction

This document describes the Pre loaded diagnostic test designs and procedures for revision A of the Stratix Memory Board II (SMB2). It also covers the hardware and software requirements for the tests.

The SMB2 is a demonstration board designed to showcase high-speed memories (DDR-II and QDR-II) with Altera's current high end device, Stratix, using Altera developed Intellectual Property (IP). The main function of this board is to provide in-house hardware verification and demonstration platforms for the Stratix QDR-II and DDR-II (non-DQS mode and DQS mode) memory controller IP. For further details see the SMB2 data sheet.

1.1 Hardware requirements

- PC – A medium performance personal computer with standard features and Windows XP installed is used as the host system for the test process. It serves as the user interface for the designs and stores all of the software and files required for the tests.
- Programming Device – A programming device is required to program/configure the Altera devices on the SMB2. A Byte Blaster with a parallel cable interface is the standard device. The SMB2 is also compatible with a USB Blaster with USB cable interface. The USB Blaster provides a slightly faster download speed.
- Power supply – The SMB2 uses an IBM Thinkpad laptop compatible power supply as the main power source for the board. It produces a 16 volt DC output and supplies 60W of power.
- RS 232 cable – An RS232 serial cable is required for communication between the host system and the board being tested.
- Ethernet connection w/cable – An Ethernet connection and cable is required to verify the Ethernet port on the SMB2. As the test is currently configured, the SMB2 attempts to use DHCP to acquire an Ethernet address.
- DDR II DIMM – Use a 256 MByte 200 MHz DDR II CL3 ECC module such as Micron part number MT9HTF3272AG-40EB3.

1.2 Software requirements

- Quartus II 4.0 – Quartus II 4.0 SP1 or newer is the assumed software environment. This provides the programming software used to configure the Altera devices.
- Board Test System (BTS) code – The BTS code is a collection of TCL scripts, batch files and compiled C programs used to automate the testing process.
- .sof files – Several .sof and .pof files are used to configure the Altera devices on the SMB2 to run the tests.

2 Board configuration and Power Up

2.1 Board switch and jumper settings and other setup

SMB2 requires a number of jumpers, switch settings, and other hardware setup before testing should begin. See figure 1 for the location of the switches and jumpers. See figure 2 for the location of cables and test card. This work should be performed **before** applying power.

Table 2-1 DIP Switch settings		
DIP Switch	**Name**	**Setting**
S1 - 8	MSEL2	Closed
S1 – 7	MSEL1	Closed
S1 – 6	MSEL0	Closed
S1 – 5	MAX_EN	Open
S1 – 4	RU_N_LU	Open
S1 – 3	MPGM2	Closed
S1 – 2	MPGM1	Closed
S1 – 1	MPGM0	Closed
S2 – 1 to 8	USER DIP 0 -7	Closed

Table 2-2 Other Switch Settings
SW1 – POWER
OFF

Table 2-3 Jumper settings				
J11	J23, J24	J29	J32, J33, J34, J35, J36, J37, J38, J39, J48	J49
p1-p3, p2-p4	p1-p2	p2-p3	p1-p2	p3-p4

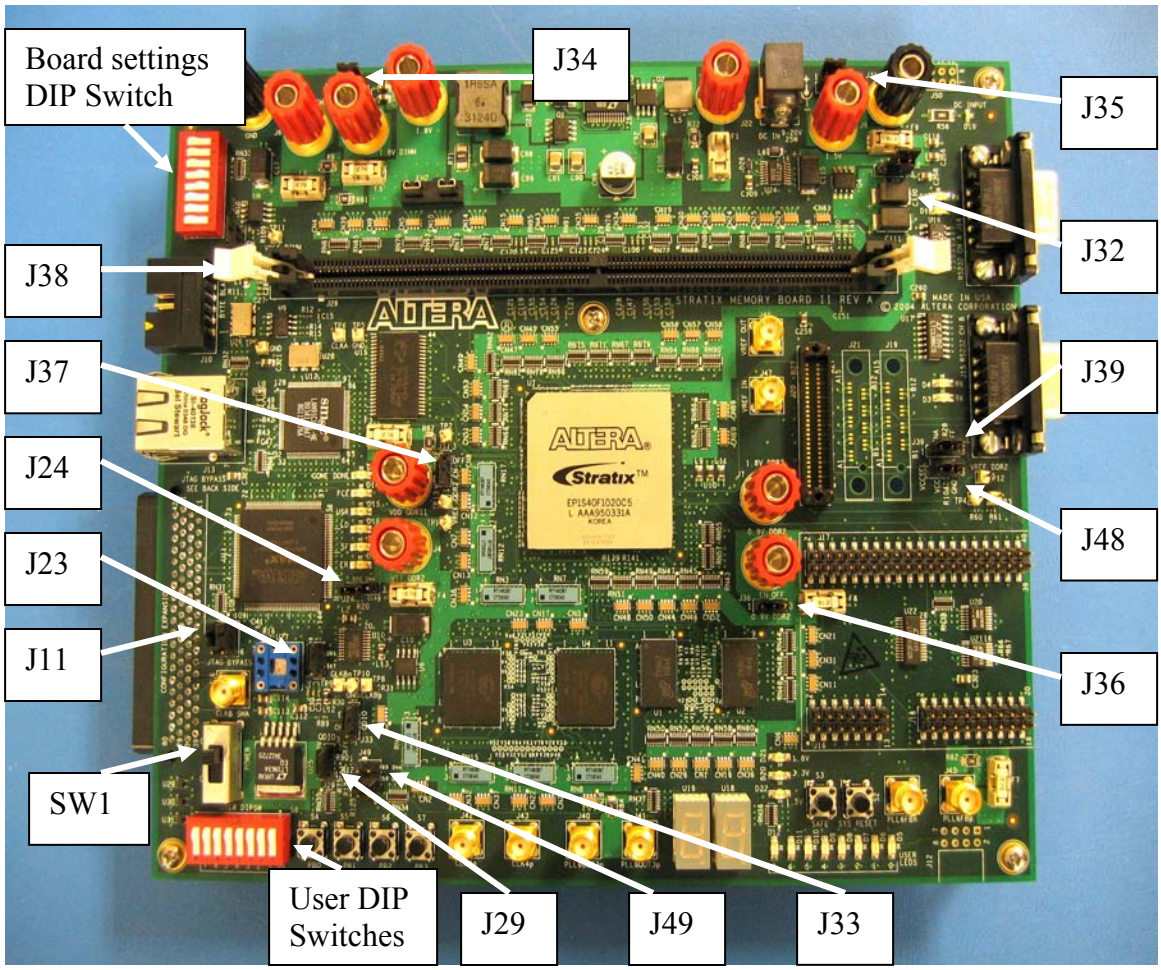

Figure 1 Switch and Jumper Locations

DDR II DIMM – Insert the DDR II DIMM carefully if needed. Try not to flex the board if possible.

RS232 Serial Cable – Connect one end of the serial cable to the COM 1 port on the PC and the other to the channel A RS232 connector (J14). This is required to run the BTS user interface

Parallel cable - Connect one end of the parallel cable to the Parallel port on the PC and the other end to the parallel port interface of the Byte Blaster cable. Connect the other end of the Byte Blaster cable to the JTAG connector on the SMB2. If you have a USB blaster you can use a USB cable. Connect the cable to the Blaster and the cable to the JTAG interface.

Ethernet cable – Connect one end of the Ethernet cable to an active Ethernet port and the other end to the RJ45 connector on the SMB2. This is required to verify the Ethernet interface portion of the SMB2.

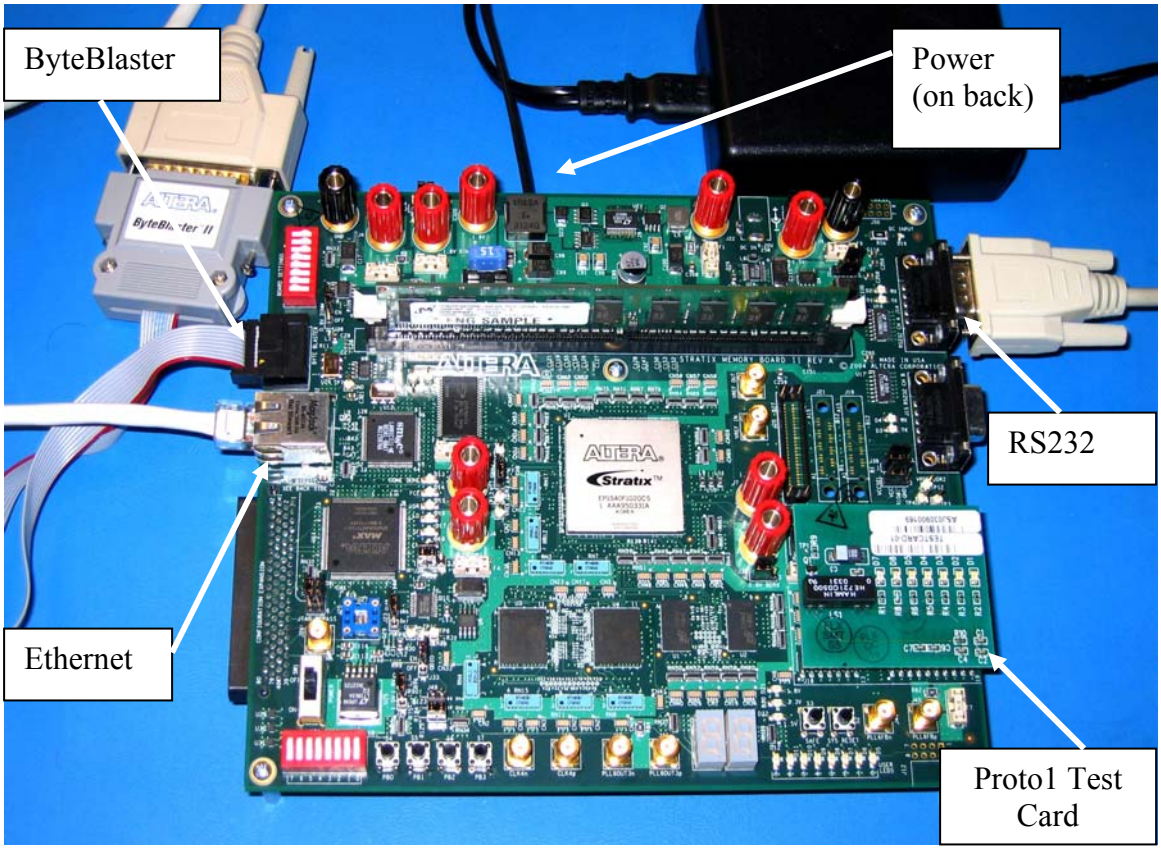

Figure 2 SMB2 with cables

2.2 Power up procedure

Insert the power connector into the socket on the back side of the board. A bright blue LED (D19) on the corner of the board should light up. This indicates that power is available to the board.

Move the power switch (SW1) to the ON position. Several LEDs on the SMB2 come on.

3 Pre Loaded Diagnostic Tests

The User IO and NIOS stamp functions are exercised using a prototype of the Board Test System (BTS). This design is the "safe" image that is loaded by pressing the SAFE button. This loads a NIOS based system design that will communicate with the host using a RS232 link. The user interface is TCL based. The GUI has several "pages" for the various features that are tested.

The memory tests are hardware based at this point and are stored as pages in the on-board flash memory. These are loaded by setting the MPGM DIP switch settings then pressing pushbutton S2 (SYS_RESET). The memory tests consist of a state

machine that writes PRBS data to the memory device at max speed then reads back the data and compares it to an expected value. If an error is detected an LED will go on or off as indicated in the detailed instruction for that test. The data is written to the full address range of the device before it is read back. Each time the full write then read cycle is completed, it is considered one test. The designs have counters that keep track of how many times the test has cycled and reports the two least significant digits in hex format on the 7 segment displays. The DDR II and QDR II designs the tests will run forever. The counter is hard coded to stop at 80. This indicates that 128 cycles/tests have been run.

3.1 User IO

The User IO and NIOS stamp functions are tested using a prototype of the Board Test System (BTS). The procedure starting up the system is just running a DOS batch file. This script will load the NIOS program and start up the GUI.

Run the batch file by double clicking on the file name: smb2_bts_run.bat

A DOS command window opens and the scripts start executing.

- Wait until the Board Test System GUI window opens:
- Use the BTS pulldown menu to open the COM1 port.
  BTS ->Open Port -> RS232 Com1
- Click on the UserIO page.
- Click on the Enable Polling button.
- Test the Seven Segment display by slowly moving the slider using your mouse and verifying that display on the board match the digits displayed in the GUI.
- Test the User LEDs by hitting the LEDs On button followed by the LEDs Off button. Then click on the LED check boxes one at a time while verifying the User LEDs on the board turn off and on.
- Check the DIP switches are working by turning them all open then back to closed while watching the switch indicators in the GUI.
- Check the User Push Buttons by pressing switches S4, S5 and S6 (PB0,PB1 and PB2) while watching the status in the GUI. Do not press S7 (PB3) as this will reset the system. If you accidentally press this button you will need to exit the GUI and start over.

This completes the User IO test section.

3.2 NIOS Stamp features

The next section to be test is the NIOS stamp features. This will test the Proto 1 IO port, onboard SRAM, Flash Memory, and the Ethernet port. If the GUI is still running you can just click on the NIOS Stamp page otherwise you will need to restart the BTS system.

- The **Proto1 IO** test is designed to work with the Proto 1 test card developed by the NIOS group. The NIOS Proto1 test card needs a resister value modified before the card is connected to a powered up SMB2 board or a resistor will overheat and fail. The resistor is R8. The new value needs to be approximately 4k-5k Ohms.

- Click on the Start Test button in the Santa Cruz IO section.
  - Test Results should show
    Starting Santa Cruz Test
    Wrote 0x100000 but Read 0x0
    Santa Cruz IO Test Complete

- Click on the Start Tests button in the **SRAM** section. This will run the "Walking Ones on Address" and "Walking Ones on Data" tests.
  Verify the tests complete without errors.
  - Test Results should show
    Starting Test
    Walking Ones on Data
    Walking Ones on Address
    There were 0 error(s).
    Test Complete

- Warning: Running the **flash** tests will corrupt the designs in flash memory. You will have to reprogram the flash to the factory image after running these tests. Click on the Start Tests button in the Flash section. This will run the "Walking Ones on Address" and "Walking Ones on Data" and Flash Erase tests. This may take 3 -4 minutes to finish.
  - Verify the tests complete without errors.
    Starting Test
    Walking Ones on Data
    Starting Flash Erase of sector offset 0
    Finished Flash Erase
    Walking Ones on Address
    Starting Flash Erase
    Test Complete

- Click on the Get DHCP address in the **Ethernet** section. If the board is connected to a live network this should return an IP address. The actual IP address returned will be different.
  - Test Results should show if connected to network.
    Getting DHCP Address
    DHCP Address obtained. Address is 137.57.185.70.

  - Click on the Blink Ethernet LEDs button.
    Verify that the LEDs on the Ethernet connector blink several times.

  - If the SMB2 board is not connected to a live network the Ethernet tests will not work correctly. Instead look for the following message in the BTS message window in the bottom of the GUI. It takes about

1 minute before you get the first timing out message. At this point just close the GUI.

[lan91c111] nr_lan91c111_reset: chip id = LAN91C111
[lan91c111] r_lan91c111_detect_phy: found lan83C183 (lan91C111 internal)

[lan91c111] r_lan91c111_init_phy: phy negotiation timed out
[lan91c111] r_lan91c111_init_phy: 10bt

[lan91c111] r_lan91c111_init_phy: half duplex

[dhcp] 1 timing out

This finishes the NIOS Stamp section of the tests.

3.3 DDR II DIMM

Set the MPGM switches to 000 (UTILITY SWITCHES 3 – 1 to OPEN). . Press the RESET (S2) push button. This will load Page 0 from the flash memory. Wait for LED D13 (CONF_DONE) and LED D15 (USR) to come on.

Press pushbutton S7 (PB3) to reset the design. LED 0 goes on as the S7 is pushed. When S7 is released the test starts running. User LED 6 should light up, LED 7 starts blinking and the 7 segment display should start counting. LED 0 is the error indicator. If it goes out the test has failed. The counter will run until the seven segment display reads 80. At this point if LED 0 is still on the test has passed.

3.4 DDR II devices

Set the MPGM switches to 001 (UTILITY SWITCHES 1 to closed, 2, 3 to OPEN). Press the RESET (S2) push button. This will load Page 1 from the flash memory. Wait for LED D13 (CONF_DONE) and LED D15 (USR) to come on.

Press pushbutton S7 (PB3) to reset the design. . LED 0 goes on as the S7 is pushed. When S7 is released the test starts running. User LED 6 should light up, LED 7 starts blinking and the 7 segment display should start counting. LED 0 is the error indicator. If it goes out the test has failed. The counter will run until the seven segment display reads 80. At this point if LED 0 is still on the test has passed.

3.5 QDR II devices

Set the MPGM switches to 010 (UTILITY SWITCHE 2 to closed, 1, 3 to OPEN). . Press the RESET (S2) push button. This will load Page 2 from the flash memory. Wait for LED D13 (CONF_DONE) and LED D15 (USR) to come on.

Press pushbutton S7 (PB3) to reset the design. . LED 6 goes on as the S7 is pushed. When S7 is released the test starts running. User LED 6 should light up and the 7

segment display should start counting. LED 0 is the error indicator. If it goes out the test has failed. The counter will run until the seven segment display reads 80. At this point if LED 0 is still on the test has passed.

3.6 Downloading Factory Image

If you have corrupted the factory image pre-loaded into the on board flash memory you will have to reload the data. Set ALL DIP switch positions on S8 to the OFF position.

Connect up a USB cable to a USB Blaster and connect the USB Blaster to the JTAG port on the SMB1 board.

Run the "smb2_factory_image.bat" batch file. This will download the factory image to the board. The process can take several minutes. The FCE (flash chip enable) LED will blink until the download is complete.

After this is complete, turn the board power off by switching SW1 to the OFF position. Turn SW1 back to the ON position. Push the SAFE push button (S3). The Loading LED should blink, and the process should end with the SF (D14) and the CONF_DONE (D13) should be on. If this is not the case, retry the process ONCE.

4 Trouble shooting

Refer to the following table (table 3-1) for solutions to problems with the board, if they should occur, for power-up, configuration, and errors with test designs.

Problems	Possible Solutions
LEDs fail to come on when power is applied	Check that main connector power supply is properly connected to J22 on the back side of the board. Check that switch SW1 is turned on (all the way down). Check that the power supply is plugged in to wall.
Devices fail to configure	Check that correct program file is chosen. Check that the Byteblaster II/USB cable is installed correctly to J10 (check pin one indicator on cable) Check that configuration jumpers (J11) are set appropriately.
Design does not work properly	If using on-board oscillators, check that jumper (J23) is placed across pins 1 and 2. Check that jumper (J23) is in the ENABLE position. If using an external oscillator, check that jumper J33 is set to EXT. Check that cables are installed correctly. Check that correct program file is chosen. Check that correct push buttons and dip switches are being used. Check that dip switches, if used, are at the correct values. Ensure that the cards are fully seated (DDR II) Check that the PROTO1 Test Card is installed and fully seated.
RS-232 connection not working	Check that RS-232 cable is plugged into correct ports (on the board and on the PC)
If cygwin1.dll not found when running nios-run.exe	Add ;%QUARTUS_ROOTDIR%\bin\cygwin\bin To your path variable

Table 3-1: Troubleshooting