The Programmable Solutions Company®

Stratix Memory Board II

Termination Specification
Rev 0.3

High-Speed End Applications
1/12/2003

REVISION HISTORY

DATE	REV	Comments
12/17/2003	0.1	Created
01/12/2004	0.2	Added SSTL and HSTL overview and termination figures.
01/12/2004	0.3	Fixed typographical errors, some figures updated.

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1. Introduction

1.1. Overview

With increasing speeds of memory devices good termination is important in maintaining memory performance. This document defines the termination techniques being proposed for all high-speed memories of the Stratix Memory Board II (SMB2), which include DDR-II DIMMs, DDR-II Devices, and QDR-II Devices.

1.2. Objectives

The primary purpose of this document is to detail in a relatively short format how each memory type will be terminated without sending out extremely long functional specifications covering the entire board's design. This document will be the primary vehicle for discussion and approval of termination schemes used in this board by the various stakeholders within Altera prior to tape-out.

2. Related I/O Standards

2.1. SSTL_18

On SMB2 the DDR-II memories use a standard called SSTL_18. This standard is maintained under JEDEC JESD8-15A (referencing Addendum 15 to JESD8 dated Sept. 2003). This standard is the 1.8V version of the SSTL-family of push-pull voltage referenced I/O implementations. In general, SSTL is "particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers." (JESD8-15A quote).

Within JESD8-15A many different resistor termination schemes are shown. Figure 2-1 below shows the typical DC load an SSTL_18 buffer should see on a board. The R_{ON} of the driver is assumed to be no greater than 21Ω.

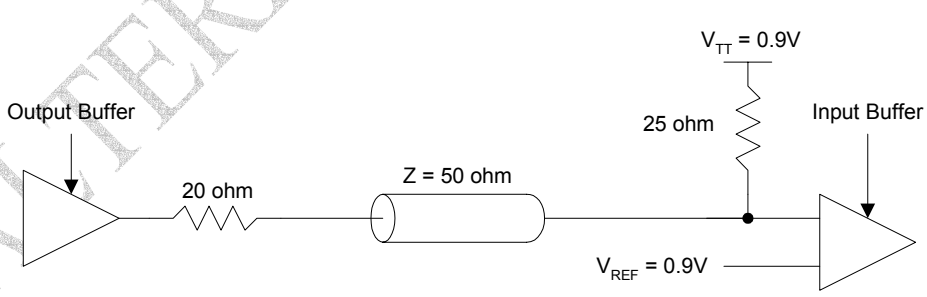

Figure 2-1 Typical DC Output Driver Load

From this model the output buffers can be designed to meet the following DC levels as generated at the termination resistors when the buffer is pushing and pulling. Table 2-1 outlines the required levels for both DC and AC operation.

SSTL_18 DC and AC Conditions				
Symbol	**Parameter**	**Min.**	**Nom.**	**Max.**
V_{DDQ}	Output Supply Voltage	1.7V	1.8V	1.9V
V_{REF}	Input Reference Voltage	833mV	900mV	969mV
V_{TT}	Termination Voltage	V_{REF} – 40mV	V_{REF}	V_{REF} + 40mV
$V_{IH\ (DC)}$	DC Input High	V_{REF} + 125mV	-	V_{DDQ} + 300mV
$V_{IL\ (DC)}$	DC Input Low	-300mV	-	V_{REF} - 125mV
$V_{IH\ (AC)}$	AC Input High	V_{REF} + 250mV	-	-
$V_{IL\ (AC)}$	AC Input Low	-	-	V_{REF} - 250mV
$V_{SWING\ (MAX)}$	Input Signal Swing	-	-	$1.0V_{pk-pk}$
Slew	Input Signal Slew Rate	1.0V/ns	-	-

Table 2-1 SSTL_18 DC and AC Conditions

Using the values from Table 2-1 one can derive the requirements for buffer design to meet the specification DC and AC levels.

For $I_{OH,}$ Table 2-2 outlines these values assuming V_{DDQ} = 1.7V, V_{OUT} = 1420mV and that (V_{OUT} - V_{DDQ}) / I_{OH} ≤ 21Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} D – 280mV.

For $I_{OL,}$ Table 2-2 outlines these values assuming V_{DDQ} = 1.7V, V_{OUT} = 280mV and that V_{OUT} / I_{OH} ≤ 21Ω for values of V_{OUT} between 0.0V and 280mV.

SSTL_18 Output DC Current Drive				
Symbol	**Parameter**	**Min.**	**Nom.**	**Max.**
$I_{OH\ (DC)}$	Output Source Current	13.4mA	-	-
$I_{OL\ (DC)}$	Output Sink Current	-13.4mA	-	-

Table 2-2 SSTL_18 Output DC Current Drive

The following figures show various reference circuits that are provided for various termination schemes that can be employed to design a circuit to meet the specification's requirements. It is important to note that board-specific implementation can vary and that under certain board-specific conditions any of the following circuits can meet the specification requirements.

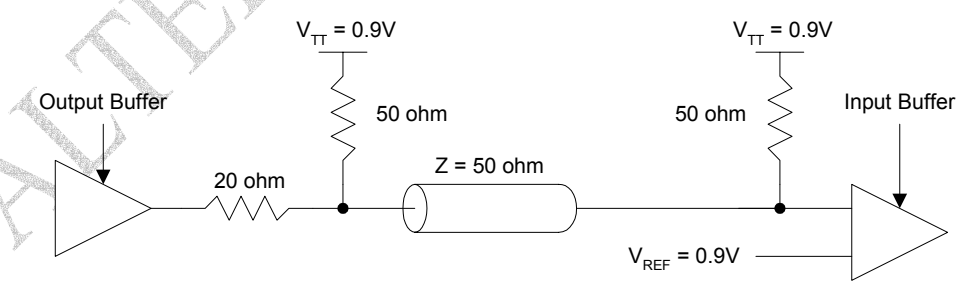

Figure 2-2 Double Parallel Termination with Series Resistor

The circuit in figure 2-3 is generally the best for bi-directional signals where the 20Ω series resistor is there to isolate the stub to the memory controller and/or impedance-match the board trace. This can be advantageous for bi-directional data signals in a system with multiple DIMMs or multiple sets of devices (similar to multiple DIMMs but on the same board). In this case the bus is truly just the connection between the DIMMs and the connection to the memory controller can be considered another stub in the system.

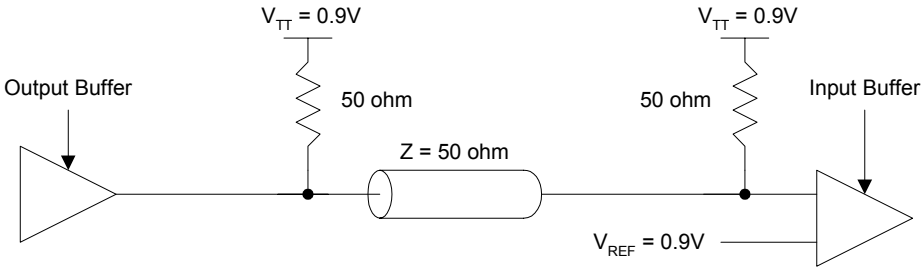

Figure 2-3 Double Parallel Termination without Series Resistor

The circuit in figure 2-4 is just like figure 2-2 except that the source series has been removed because it was not deemed necessary. This is typical where the source signal is not at the end of a long stub. One example of this is the bi-directional data signals in a system with a single DIMM or single set of devices.

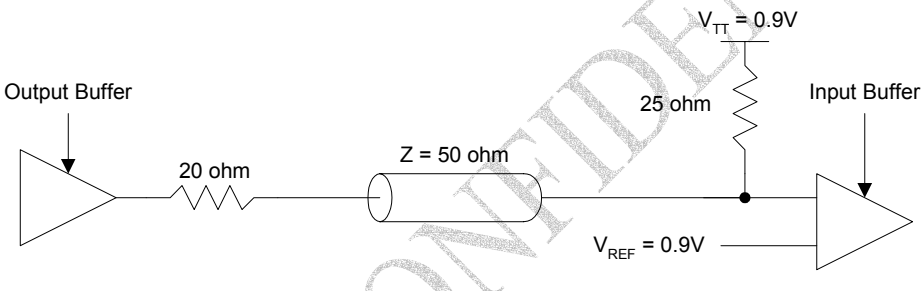

Figure 2-4 Single Parallel Termination with Series Resistor

The circuit in figure 2-5 can be useful for signals that are output-only from the memory controller's point of view. This scheme can also be used for bi-directional signals though it's read performance is not as great as the write performance due to the stub between the series resistor and the driver on the left.

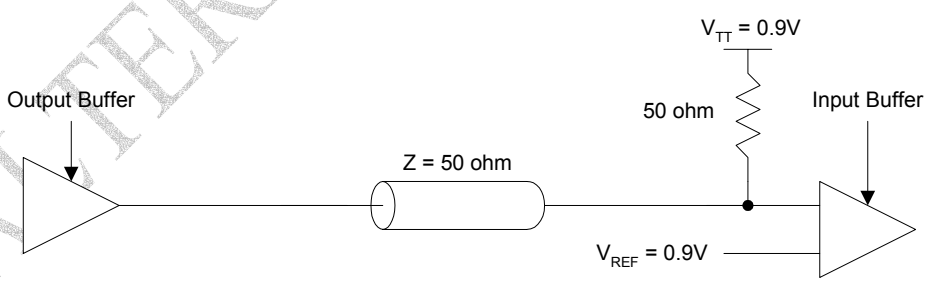

Figure 2-5 Single Parallel Termination without Series Resistor

The circuit in figure 2-5 is also useful for signals that are output-only from the memory controller's point of view. Furthermore it can also be used for bi-directional signals where simulation has deemed the trace topology short enough to tolerate the lack of read-side termination of any kind. In systems where only a single DIMM exists there is a series resistor on the DIMM that can act as an impedance matching resistor for both read and writes. In this case there is no long stub due to a second DIMM in the system.

2.2. HSTL

On SMB2 the QDR-II memories use an I/O standard called HSTL. This standard is maintained under JEDEC JESD8-6. This standard outlines certain voltage levels for signaling but attempts to remain independent of a particular VDDQ voltage rail. As with SSTL, the HSTL standard is based on push-pull voltage referenced I/O implementations. The specification goes on to outline four "classes" of output buffer loading. These range from an unterminated board-level signal to a double-parallel resistive termination scheme. The DC and AC conditions for HSTL compliance are outlined

HSTL DC and AC Conditions				
Symbol	**Parameter**	**Min.**	**Nom.**	**Max.**
V_{DDQ}*	Output Supply Voltage	1.4V	1.5V	1.5V
V_{REF}*	Input Reference Voltage	680mV	750mV	900mV
V_{TT}	Termination Voltage	-	-	-
$V_{IH\ (DC)}$	DC Input High	V_{REF} + 100mV	-	V_{DDQ} + 300mV
$V_{IL\ (DC)}$	DC Input Low	-300mV	-	V_{REF} - 100mV
$V_{IH\ (AC)}$	AC Input High	V_{REF} + 200mV	-	-
$V_{IL\ (AC)}$	AC Input Low	-	-	V_{REF} - 200mV
$V_{SWING\ (MAX)}$	Input Signal Swing	-	-	$1.0V_{pk\text{-}pk}$
Slew*	Input Signal Slew Rate	1.0V/ns	-	-

Table 2-3 HSTL DC and AC Conditions

- There is no specific V_{DDQ} level required for HSTL compliance. The 1.5V level is shown for reference only. V_{REF} is expected to be ½ of V_{DDQ} and track variations in V_{DDQ} with within 2%.
- Signal edge rate (slew rate) is expected to be maintained in the 20% to 80% of the input signal swing.

Although there are four classes defined in JESD8-6, this review will only cover Class I and Class II schemes. These are the most popular for high-speed memory interconnects. The Class III and Class IV schemes involve resistive termination to the VDDQ rail (as opposed to ½ VDDQ) and are called "asymmetric parallel terminated", involving drive strengths of 24 and 48 mA to achieve the same V_{OL} levels as the Class I and Class II circuits. Several reference loads for Class I and Class II circuits are shown in the figures below.

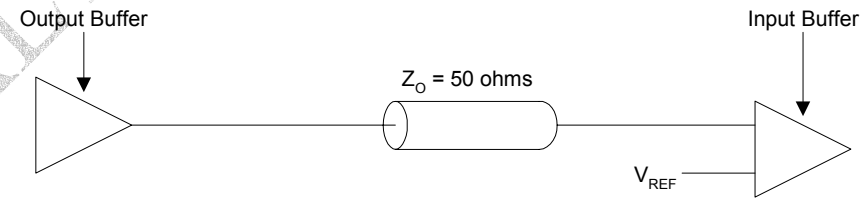

Figure 2-6 HSTL Class I – unterminated load

This

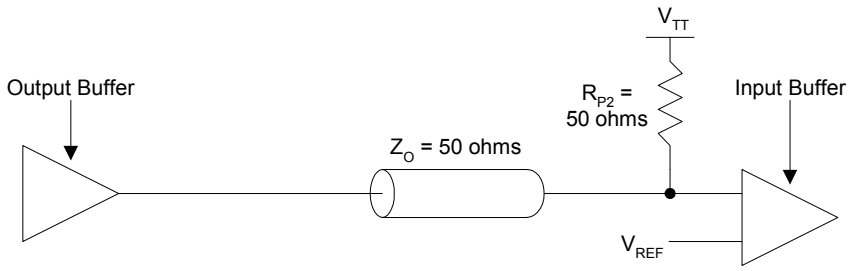

Figure 2-7 HSTL Class I – singe parallel load

The circuits and loads shown in Figure 2-6 and Figure 2-7 above are for Class I drivers. A class I compliant driver is expected to meet the voltage levels in Table 2-3 above. Appropriate DC current drives required to meet this Class-I specification for either termination conditions shown above are outlined in Table 2-4 below.

HSTL Class I Output DC Current Drive				
Symbol	**Parameter**	**Min.**	**Nom.**	**Max.**
$I_{OH\ (DC)}$	Output Source Current	8.0 mA	-	-
$I_{OL\ (DC)}$	Output Sink Current	-8.0mA	-	-

Table 2-4 HSTL Class I Output DC Current Drive

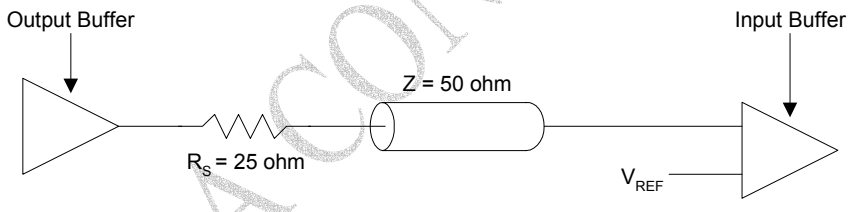

Figure 2-8 HSTL Class II – single series load

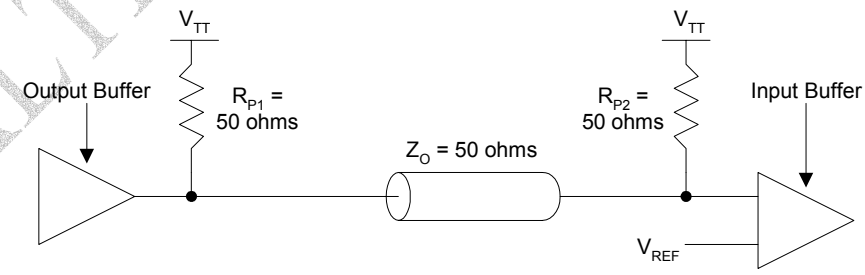

Figure 2-9 HSTL Class II – double parallel load

The circuits and loads shown in Figure 2-8 and Figure 2-9 above are for Class II drivers. A class II compliant driver is expected to meet the voltage levels in Table 2-3 above. Appropriate DC

current drives required to meet this Class II specification for either termination conditions shown above are outlined in Table 2-5 below.

HSTL Class II Output DC Current Drive				
Symbol	**Parameter**	**Min.**	**Nom.**	**Max.**
$I_{OH\ (DC)}$	Output Source Current	16.0 mA	-	-
$I_{OL\ (DC)}$	Output Sink Current	-16.0mA	-	-

Table 2-5 HSTL Class II Output DC Current Drive

3. Board-Specific Implementation

3.1. DDR-II DIMM

On SMB2 there is a single DDR-II DIMM interface. For single-sided modules there will be a single load for every DQ, DQS, and DM (Data, Strobe, and Mask). For double-sided modules there will be two loads for every DQ, DQS, and DM (Data, Strobe, and Mask). The two loads are directly on top of one another so no real stub exists between single and double-sided modules.

The approximate lengths for these signals are shown in Figure 3-1 below for the Stratix-to-DIMM interface (mainboard termination resistors not shown). The mainboard signal lengths are estimates and the DIMM signal lengths are from the JEDEC specs for registered DIMMs. The listed loadings are for the single-sided DIMM.

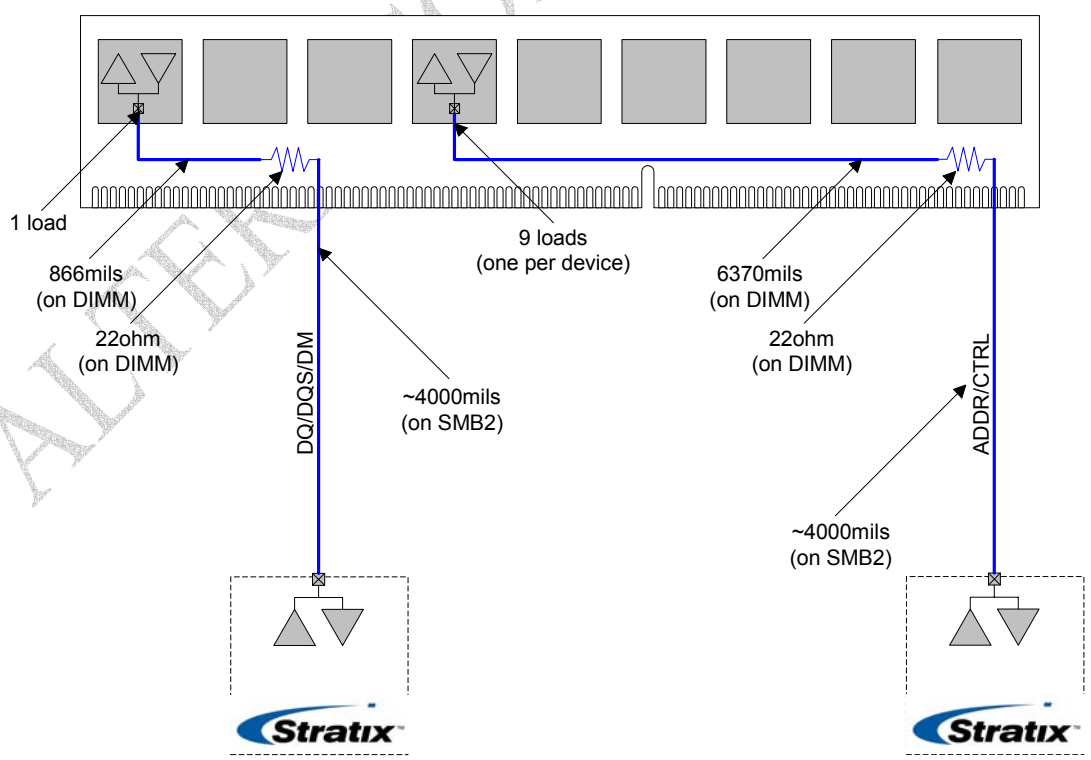

Figure 3-1 DDR-II DIMM Signal Lengths

The termination circuit being used for the DDR-II DIMM circuit depends on the signal group within the DIMM. In general they can be broken into four distinct groups:

- **Address/Command Group**
  - BA(2:0) bank address
  - A(15:0) address
  - RASn command input (row address strobe)
  - CASn command input (column address strobe)
  - WEn command input (write enable)
- **Control Group**
  - Sn(1:0) chip select
  - CKE(1:0) clock enable
  - ODT(1:0) on-die termination enable
- **Data Group**
  - DQS(8:0) data strobe
  - DM(8:0) data mask
  - DQ(63:0) data bits
  - CB(7:0) check bits
- **Clock Group**
  - CKp(2:0) positive-side of diff. system clock
  - CKn(2:0) negative-side of diff. system clock

Address/Command Group

The Address/Command Group signals are all outputs from the Stratix device. Micron recommends that these signals be terminated to Vtt (0.9V nominally). This termination should be placed just past the DIMM with respect to the Stratix (i.e. fly-by termination style). This resistor would be best placed at the end of the trace on the DIMM but since that is not possible it is best placed near the DIMM as mentioned.

There is a 22Ω series resistor on the DIMM for each and every one of these signals. The purpose of the series resistor is not impedance matching as much as stub isolation. In typical systems there can be one or two DIMMs and sometimes up to four. Series resistors dampen the in-coming signal from Stratix and also dampen the ensuing reflection from the 6” stub on the DIMM.

A series resistor will be placed near the Stratix output pins to be used for impedance matching the output buffer to the trace impedance. In general this resistor is not needed because the DIMM has a series resistor on it already. However, it may be useful to test the impedance matching (current drive adjustment) on the Stratix output buffers versus the off-chip series termination resistors.

Micron also recommends adding a compensation capacitor within ½” of the DIMM on the Stratix-side. The value of this capacitor should be based on simulations of the system loading and lengths.

Figure 3-2 below shows the planned termination scheme for the DDR-II DIMM for the Address/Command Group. The series resistor value will be varied for testing purposes.

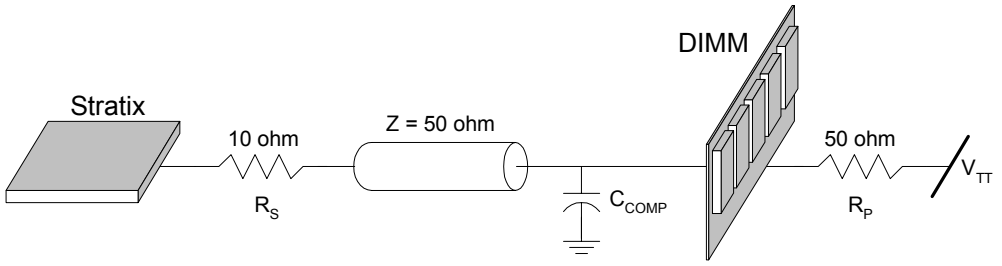

Figure 3-2 Address/Command Termination

Control Group
As with the Address/Command Group, the Control Group signals are all outputs from the Stratix and should be terminated to Vtt (0.9V nominally). This termination should be placed just past the DIMM with respect to the Stratix (i.e. fly-by termination style).

There is a 22Ω series resistor on the DIMM for each and every one of these signals. The purpose of the series resistor is not impedance matching as much as stub isolation. The Control Group signals have the same loading for either a single-sided or double-sided DIMM. This is because the Control Group is connected to only one of two possible sides (also called rank) of the DIMM.

A series resistor will be placed near the Stratix output pins to be used for impedance matching the output buffer to the trace impedance. In general this resistor is not needed because the DIMM has a series resistor on it already. However, it may be useful to test the impedance matching (current drive adjustment) on the Stratix output buffers versus the off-chip series termination resistors.

A compensation capacitor is not required on SMB2 for the Control Group signals because one is already in place on the unbuffered DIMM.

Figure 3-3 below shows the planned termination scheme for the DDR-II DIMM for the Control Group. The series resistor value will be varied for testing purposes.

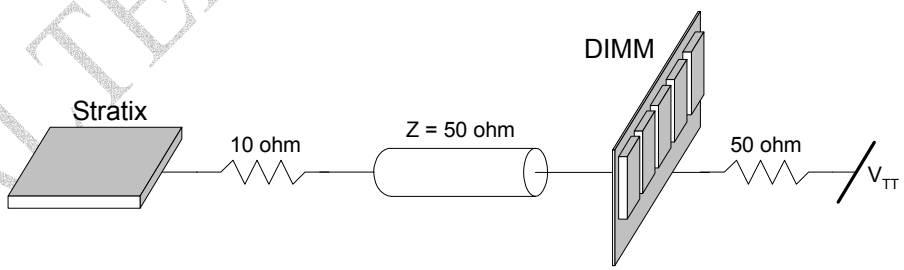

Figure 3-3 Control Termination

Data Group
The Data Group signals are all bi-directional except for the data mask bits. The DDR-II silicon on the DIMM has on-die termination (ODT) capabilities. These are intended to be turned on and off dynamically based on the bus transaction and the system load. The ODT will emulate either a

75Ω resistor or a 150Ω resistor and only when the ODT signal corresponding to the DIMM and proper side (or rank) is asserted. Table 3-1 below outlines the intended functionality.

DDR-II On-Die-Termination			
Bus Transaction	**Controller (Stratix)**	**DIMM (front)**	**DIMM (back)**
Read (front bank)	75Ω	High-Impedance	High-Impedance
Read (back bank)	75Ω	High-Impedance	High-Impedance
Write (front bank)	High-Impedance	150Ω	High-Impedance
Write (back bank)	High-Impedance	High-Impedance	150Ω

Table 3-1 Recommended On-Die Termination Use

Again as with the Address/Command Group and the Control Group there is a 22Ω series resistor on the DIMM for each and every one of the signals in the Data Group for stub isolation. The signals in the Data Group have a considerably shorter stub than those in the Address/Command Group. In addition these signals have single loads or, at most, two loads in a double-sided DIMM. SMB2 only has a single DIMM but in systems with more the number of loads would increase linearly (up to 36 loads).

The typical DDR-II routing rules from Micron and other vendors assume the ability to use the above mentioned ODT in a dynamic fashion on the controller-side as well. Because the Stratix device does not have the ability to dynamically switch its termination, one of several approaches must be taken:

(1) Use a series resistor close to the Stratix and ODT for DIMM
   a. This would be the easiest to route and the lowest power consumption.
   b. Higher values for Rs would reduce reflections but also reduce edge-rate and thus speed.

(2) Use a parallel termination resistor close to the Stratix and ODT for DIMM
   a. This is harder to route because of the need for a Vtt power island and the addition of many Vtt decoupling caps near the Stratix
   b. Because it is impractical to dynamically switch the termination for the entire read-side Vtt power island it must always be left enabled.
   c. Micron recommended in this case that a 150Ω parallel resistor be placed and left on constantly (connected to an active Vtt power island) though they recommended simulation before finalizing on the circuit.

(3) Use a parallel termination resistor close to the Stratix and another close to the DIMM and do not use ODT on the DIMM.
   a. This will allow testing of both ODT-enabled (de-populate the far end) and ODT-disabled (populate both) circuits by changing the resistor population and values.

(4) Use a parallel termination resistor close to the DIMM and do not use ODT
   a. This is similar to DDR-I termination schemes as done on the Stratix PCI and Stratix GX boards.
   b. Micron said this should work without issue at 200MHz (max target speed for the Stratix device) and most likely at 267MHz (max target speed for the Stratix-II device) but would become problematic at 333MHz and beyond.

The approach that seems the most reasonable is to use solution (3) above. This will not allow for testing of different series termination values but it will allow for testing of the output impedance adjustment and current strength of the Stratix device using Quartus. Lab testing done at Altera has revealed that a series resistor value of 0Ω gave the highest performance in a DDR-I system with two Vtt terminations (a.k.a. Class-II). The gain from both a parallel and series resistor is minimal with respect to the routing congestion. In addition it has been noted that the parallel

termination on the Stratix-side is better for read signal quality than to have a series resistor that creates fairly long stubs. This parallel resistor's affect to the write signal quality is negligible. In addition, using approach (3) also gives us the ability to test approach (4) by de-populating the near-side termination resistor and changing the far-side termination resistor values. The PCB design target to allow this is shown in Figure 3-4 below. Other circuits to test are shown in Figure 3-5 and Figure 3-6 below.

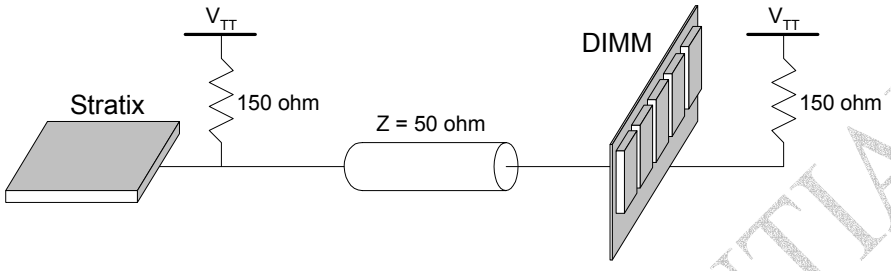

Figure 3-4 Data Termination (approach 3, not using ODT)

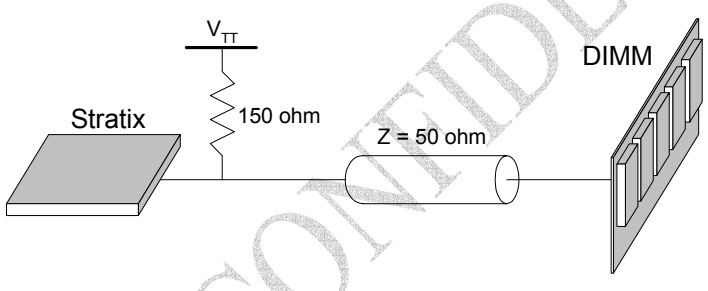

Figure 3-5 Data Termination (approach 2, uses ODT)

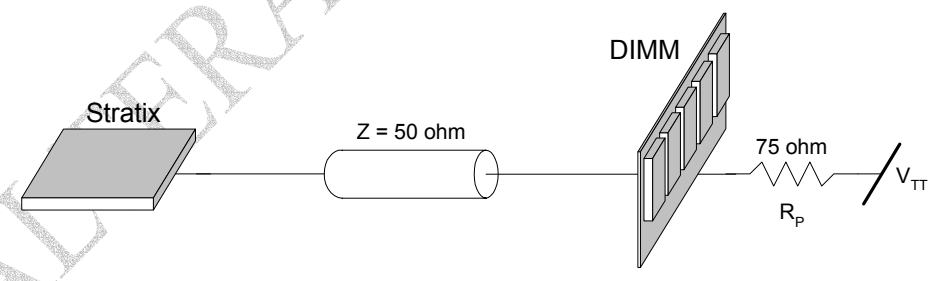

Figure 3-6 Data Termination (approach 4, not using ODT)

Clock Group

The Clock Group signals are all differential outputs from the Stratix device and are terminated on the DIMM with a 120Ω resistor across the pair.

3.2. DDR-II Devices

On SMB2 there will be an interface to two 16-bit-wide DDR-II devices. These devices have the same groups of signals as outlined in Section 3.1 for the DIMM. These include the Address/Command Group, the Control Group, the Data Group, and the Clock Group.

These devices will be wired in parallel so as to present a single 32-bit interface to the Stratix. This will make a system that has two loads on every signal in the Address/Command Group and the Control Group. This is roughly ¼ the load as compared with the DIMM circuit in Section 3.1 for a typical single-sided DIMM with 9 DDR-II devices. There is a single load for each signal in the Data Group. This is similar to the loading on the single DIMM circuit in Section 3.1 for the Data Group and Clock Group (point-to-point).

Address/Command Group

The Address/Command Group signals are all outputs from the Stratix device. Micron recommends that these signals be terminated to Vtt (0.9V nominally). This termination should be placed just past the devices with respect to the Stratix (i.e. fly-by termination style).

A series resistor will be placed near the Stratix output pins to be used for impedance matching the output buffer to the trace impedance. This series resistor will be useful to test the impedance matching (current drive adjustment) on the Stratix output buffers versus the off-chip series termination resistors.

Due to the relatively short traces between the Stratix and the DDR-II devices there is no need for a compensation capacitor. The route lengths are expected to be around 4" point-to-point and will not have the 833mil stub as exists on the DIMM interface.

Figure 3-7 below shows the planned termination scheme for the DDR-II Devices for the Address/Command Group. The series resistor value will be varied for testing purposes.

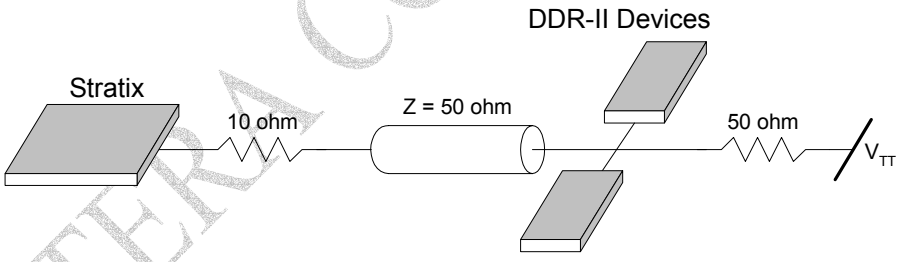

Figure 3-7 Address/Command Termination

Control Group

As with the Address/Command Group, the Control Group signals are all outputs from the Stratix and should be terminated to Vtt (0.9V nominally). This termination should be placed just past the DDR-II Devices with respect to the Stratix (i.e. fly-by termination style).

A series resistor will be placed near the Stratix output pins to be used for impedance matching the output buffer to the trace impedance. This series resistor will be useful to test the impedance matching (current drive adjustment) on the Stratix output buffers versus the off-chip series termination resistors.

Figure 3-8 below shows the planned termination scheme for the DDR-II Devices for the Control Group. This is the same as for the Address/Command Group. The series resistor value will be varied for testing purposes.

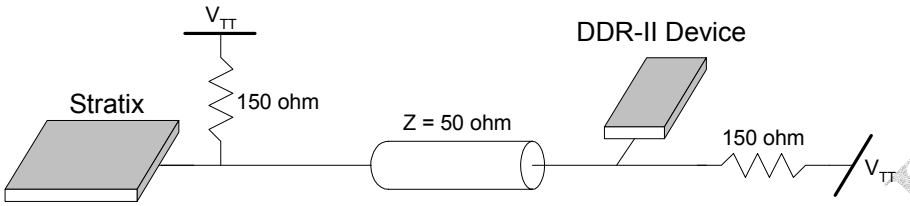

Figure 3-8 Control Termination

Data Group

The Data Group signals are all bi-directional except for the data mask bits. The DDR-II silicon has on-die termination (ODT) capabilities. These are intended to be turned on and off dynamically based on the bus transaction and the system load. The ODT will emulate either a 75Ω resistor or a 150Ω resistor and only when the ODT signal corresponding to the specific device is asserted. Table 3-2 below outlines the intended functionality.

DDR-II On-Die-Termination		
Bus Transaction	**Controller (Stratix)**	**DDR-II Devices**
Read	75Ω	High-Impedance
Write	High-Impedance	150Ω

Table 3-2 Recommended On-Die Termination Use

The typical DDR-II routing rules from Micron and other vendors assume the ability to use the above mentioned ODT in a dynamic fashion on the controller-side as well. Because the Stratix device does not have the ability to dynamically switch its termination, one of several approaches must be taken:

(1) Use a series resistor close to the Stratix and ODT for DDR-II Devices.
   a. This would be the easiest to route and the lowest power consumption.
   b. Higher values for Rs would reduce reflections but also reduce edge-rate and thus speed.

(2) Use a parallel termination resistor close to the Stratix and ODT for DDR-II Devices
   a. This is harder to route because of the need for a Vtt power island and the addition of many Vtt decoupling caps near the Stratix
   b. Because it is impractical to dynamically switch the termination for the entire read-side Vtt power island it must always be left enabled.
   c. Micron recommended in this case that a 150Ω parallel resistor be placed and left on constantly (connected to an active Vtt power island) though they recommended simulation before finalizing on the circuit.

(3) Use a parallel termination resistor close to the Stratix and another close to the DDR-II Devices and do not use ODT on the DDR-II Devices.
   a. This will allow testing of both ODT-enabled (de-populate the far end) and ODT-disabled (populate both) circuits by changing the resistor population and values.

(4) Use a parallel termination resistor close to the DDR-II Devices and do not use ODT
   a. This is similar to DDR-I termination schemes as done on the Stratix PCI and Stratix GX boards.
   b. Micron said this should work without issue at 200MHz (max target speed for the Stratix device) and most likely at 267MHz (max target speed for the Stratix-II device) but would become problematic at 333MHz and beyond.

As with the DIMM, the approach that seems the most reasonable is solution (3). The PCB design target to allow this is shown in Figure 3-9 below. Other circuits to test are shown in Figure 3-10 and Figure 3-11 below.

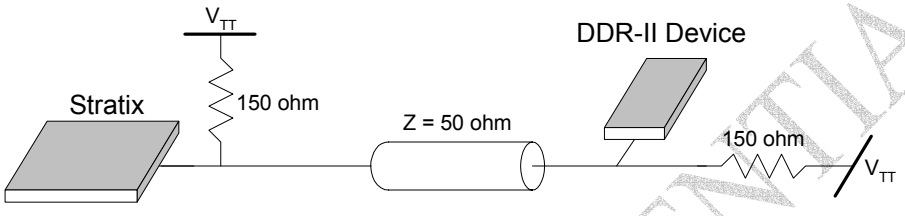

Figure 3-9 Data Termination (approach 3, not using ODT)

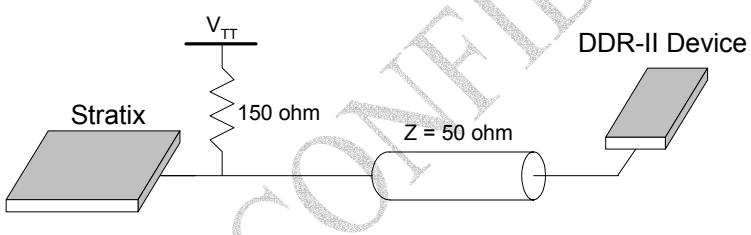

Figure 3-10 Data Termination (approach 2, uses ODT)

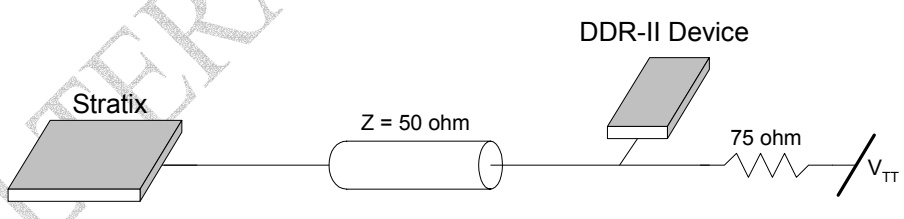

Figure 3-11 Data Termination (approach 4, not using ODT)

Clock Group

The Clock Group signals are all differential outputs from the Stratix device and are terminated on the board with a 100Ω resistor across the pair.

3.3. QDR-II Devices

On SMB2 there is a single interface to two 18-bit-wide QDR-II devices. These devices have similar groups of signals to the DDR-II devices but slightly different as there is no bi-directional data bus and a simple SRAM addressing system. These signal groups are listed below.

- **Address Group**
  - A(18:0) address
- **Control Group**
  - WPS(1:0) write port select
  - RPS(1:0) read port select
  - BWS(1:0) byte write select
- **Data Group**
  - D(17:0) write data
  - Q(17:0) read data
- **Clock Group**
  - Kp(1:0) positive-side of diff. write clock
  - Kn(1:0) negative-side of diff. write clock
  - Cp(1:0) positive-side of diff. read clock
  - Cn(1:0) negative-side of diff. read clock
  - CQp(1:0) positive-side of diff. echo clock
  - CQn(1:0) negative-side of diff. echo clock

These two QDR-II devices will be wired in series such that the overall data bus is 18-bits for read and 18-bits for write whether there are two devices or just one on the board. When both devices are populated there will be two loads on the Address Group and Data Group. If a single device is installed then there will be only one load. There is a single load on the Control Group in any configuration.

Address Group, Data Group

The Address Group signals are all outputs from the Stratix device. The Data Group signals are outputs from Stratix for write data and inputs to Stratix for read data. Cypress recommends that these signals be terminated to Vtt (0.9V nominally). To facilitate further testing of single parallel and double parallel termination SMB2 will use a double parallel termination scheme as shown in Figure 3-12 below.

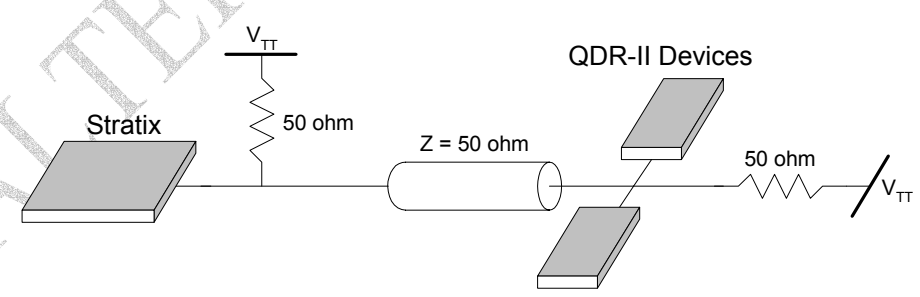

Figure 3-12 Address Group, Data Group Termination

Control Group

The Control Group signals are all outputs from the Stratix device. Cypress recommends that these signals be terminated to Vtt (0.9V nominally). To facilitate further testing of single parallel and double parallel termination SMB2 will use a double parallel termination scheme as shown in Figure 3-11 below.

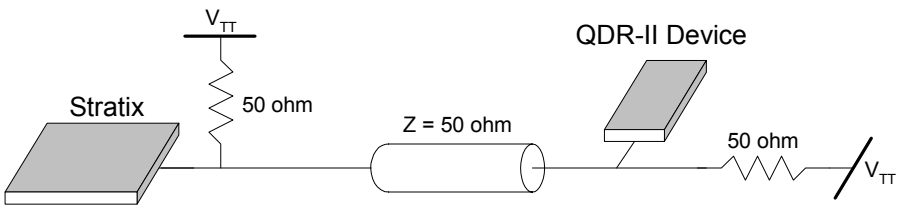

Figure 3-13 Control Group Termination

Clock Group

The Clock Group signals consist of some input signals and some outputs signals from the Stratix device. The read and write clocks are outputs and the echo clocks are inputs. These are differential HSTL signals. Cypress recommends that these signals be terminated to Vtt (0.9V nominally). The termination for the read and write clocks as shown in Figure 3-14 below. The termination for the echo clocks is similar but with the 50-ohm resistors to ground being close to the Stratix.

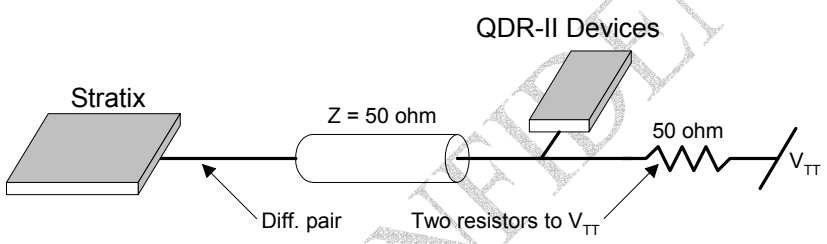

Figure 3-14 Clock Group Termination

4. Conclusion

In general the SSTL and HSTL specs leave much room for interpretation as far as termination circuits go. The main idea of each spec is to lay out the DC and AC conditions and typical loads to assist in CMOS buffer design and leave the board-specific implementation up to the board designer.

The termination circuits for all three memory subsystems are “over-designed” to facilitate testing beyond what a “minimum” circuit would perhaps be. For DDR-II DIMM and Devices there is the issue of ODT usage that will require testing of a minimum of there different scenarios (Class II without ODT, Class II with ODT, and Class I without ODT). For QDR-II Devices there are two circuits to be tested (Class I and Class II).

In addition to these different topologies is the testing or programmable drive strength and impedance matching with the Stratix buffer as well as comparisons made to various resistor values for on-board series termination.

After the testing and characterization is complete Altera should be able to recommend one or two simple scenarios so that customers can use the best method right from the start and not need to do their own characterizations for boards with similar designs.