AMD

BIOS Requirements for AMD PowerNow!™ Technology Application Note

Featuring...

AMD PowerNow!™ TECHNOLOGY

Publication # **25264** Rev: **1.01**
Issue Date: **April 2002**

Contents

List of Figures

List of Tables

Revision History

Date	Rev	Description
April 2002	1.01	Added Chapter 5
August 2001	1.00	Initial Release

1 Introduction

AMD PowerNow!™ technology is a system solution for power management. It requires specific implementation in the processor, chipset, motherboard, and BIOS. This document describes how to implement certain BIOS-related aspects of support for AMD PowerNow! technology. Use this document in conjunction with the applicable data sheet for the mobile AMD Athlon™ processor. The main topics covered in this document are:

- A brief overview of the hardware and software components required to support AMD PowerNow! technology
- An overview of BIOS responsibility for supporting AMD PowerNow! technology
- Model-Specific Registers (MSRs) that a BIOS writer must understand to implement support for the AMD PowerNow! technology
- BIOS responsibilities for mobile AMD processors during Power-On Self Test (POST)
- BIOS tables required for support of the AMD PowerNow! technology
- Determination of whether the processor supports AMD PowerNow! state transitions

2 Audience and Intended Use

The primary audience for this document is the firmware developer who provides BIOS support for the mobile AMD Athlon and mobile AMD Duron™ processors. This document provides information to help the software developers understand:

- the processor registers that control AMD PowerNow! technology transitioning of processor performance states on the mobile AMD Athlon processor and what BIOS needs to do with these registers during POST.
- how to identify whether or not a processor supports AMD PowerNow! technology.
- implementation of the BIOS tables that are required for support of AMD PowerNow! control software.
- how to determine that support in all of these areas has been correctly implemented.

3 Overview of AMD PowerNow!™ Software and Hardware

AMD PowerNow!™ technology allows software to control the performance of the processor by adjusting the processor frequency based on the real-time needs of the operating system, applications, and drivers. When the processor is configured to a frequency that is lower than the rated maximum frequency, the processor voltage may also be lowered. Lowering the voltage results in an additional power savings over simply reducing the frequency alone. When the system needs more processing power, both processor frequency and voltage are increased to the rated maximums for the processor. Running at the maximum rated frequency and voltage provides the full processing power to run applications faster. AMD PowerNow! technology is completely independent of ACPI, APM, or any other existing power management system. It works seamlessly and in parallel with all of these legacy power management schemes to enhance the power usage efficiency of portable systems. AMD PowerNow! technology consists of four main components that are described in the following subsections.

3.1 BIOS-Based PSB and Processor Initialization

The Performance State Block (PSB) is basically a set of tables that are stored in the BIOS ROM. These individual tables within the PSB are called Performance State Tables (PSTs). Each of the PSTs holds all supported frequency and voltage combinations for a given speed grade of a given processor design that is manufactured in a given silicon process. A complete description of this table is given later in this document. In addition to this table, some simple initialization of the processor is required during POST in order to support the AMD PowerNow! technology. This initialization is also detailed in a later section of this document.

3.2 AMD PowerNow!™ Technology Driver

AMD provides the AMD PowerNow! driver and this driver is part of the OEM-installable software package for AMD PowerNow! technology support. Its main function is to provide access to mobile-specific processor hardware for which ring 0 privilege is required. The driver is also responsible for finding the PSB in the BIOS image and for selecting the correct PST for the installed processor. The driver feeds the table data back to the AMD PowerNow! daemon (see section 3.3 on page 12 for more information). All performance state changes after BIOS POST are handled by the AMD PowerNow! technology driver.

3.3 AMD PowerNow!™ Technology Daemon

The AMD PowerNow! daemon, or background task, is provided by AMD. It is the performance state policy controller for AMD PowerNow! technology. This software decides when it's time to change performance state and sends commands to the AMD PowerNow! driver to make the state change.

3.4 Processor, Chipset, and Board-Level Hardware

AMD PowerNow! technology requires specific chipset and board support. It is *not* possible to upgrade an older system unit to allow performance state changes simply by upgrading the processor and control software. Certain new board signals and interconnections are required and the chipsets must understand how to handle the new special cycles available on the mobile AMD Athlon processors. Refer to the applicable data sheets for more information on this subject.

4 BIOS Responsibilities

The BIOS support requirements for AMD PowerNow! technology have been simplified for the mobile AMD Athlon processor as compared to the mobile AMD-K6® processors series. The main improvement is that the mobile AMD Athlon processors no longer require the use of System Management Mode (SMM) to change states. Entry to and exit from SMM is a relatively slow process that degrades performance. Without an SMM requirement for AMD PowerNow! software, BIOS no longer requires an AMD PowerNow! software-specific addition to the system SMI handler. This SMI handler has historically been problematic to develop and debug. The following subsections provide details on the BIOS support requirements for mobile AMD Athlon processors.

4.1 Performance State Block (PSB) Overview

As mentioned earlier, the PSB contains one or more Performance State Tables (refer to Section 4.2 on page 13 for more information on PSTs). The PSB contains header data that allows the AMD PowerNow! driver to locate it in the memory map. The driver scans memory between addresses 0xC0000 and 0xFFFF0 on paragraph boundaries looking for this signature. When the signature is found, the driver scans the structure for a PST entry that matches parameters of the installed processor. After POST is completed, the PSB must reside in memory-mapped address space in an uncompressed format. A BIOS that supports non-shadowed operation must ensure that the PSB is uncompressed on the ROM as well.

While there is no requirement regarding the listing order of PSTs within a PSB, the source code is much easier to manage if all PSTs that apply to a particular CPUID that are grouped together. On a per-CPUID basis, maintain an ascending speed grade order in the PSB. This order makes the code easier to read and maintain.

4.2 Performance State Table (PST) Overview

Each PST is a set of Voltage ID (VID) and Frequency ID (FID) combinations supported by a particular processor type and speed grade. Each PST contains header data that allows the AMD PowerNow! driver to locate the PST that matches the currently installed processor. The header data that are used for this comparison operation are the:

- CPUID (EAX value returned from extended function 8000_0001h)
- Frontside bus speed (in MHz)
- Maximum FID of the processor (see Section 4.3 for FID description)
- Start VID of the processor (see Section 4.3 for VID description)

The AMD PowerNow! driver must search the PSB for a PST that matches all four of these values to the currently installed processor. If a complete match is not found, the driver will unload itself from memory with no error reported.

4.3 FID (Frequency ID) and VID (Voltage ID) Codes

As described earlier, the BIOS must contain at least one PST that gives all valid processor *frequency/core voltage* combinations for the platform. However, the voltage/frequency data in these tables are not given in units of MHz or volts, but rather in terms of FIDs and VIDs.

A FID is a binary code that identifies a Frontside Bus (FSB) multiplier. While the standard FSB clock for mobile systems is 100 MHz, AMD PowerNow! technology 2.1 does have provisions for supporting other FSB clock speeds if needed. Refer to the applicable processor data sheet for the table of FID codes to processor frequency translations.

A VID is a binary code that identifies a particular voltage. The VID code is fed to the voltage regulator on the motherboard where a digital-to-digital converter uses this VID code to generate the processor core voltage. These voltage regulators come in two types: desktop and mobile. The VID codes differ between these two types, so BIOS must know what type of voltage regulator is installed on the motherboard. Desktop motherboard VIDs are beyond the scope of this document. Mobile systems are *required* to use mobile voltage regulators. Refer to the applicable processor data sheet for the table of VID codes to voltage definitions.

4.4 Determination of PST Data

Mobile AMD processor data sheets give the performance states that are supported for a particular processor type and speed grade. However, PST data is not only processor specific, but can also be platform specific. The platform can require upward voltage adjustments for a given processor operating frequency. *It is the responsibility of the platform designer to determine the values that are used in the PST for a given platform.* The platform designer can start with the values provided in the processor data sheet and then test that each voltage/frequency combination given in that document works properly on the target platform. If a given FID/VID combination does not work properly, the designer can increase the processor voltage by the minimum possible increment and then retest. This process can be repeated until either the system passes the OEM's diagnostic suite or until a determination is made that the given frequency is not supported on the platform. Under no circumstances must the table contain any FID or VID values higher than the maximum FID and maximum VID values that are read from the FidVidStatus MSR. All PST values *must* be ascertained using the actual speed grade of the processor for which PST data determination testing is being done. For example, it is incorrect to use a 1-GHz processor to determine the PST settings for an 850-MHz device even if the testing is limited to 850 MHz.

4.5 PSB Structure

The PSB (PST Block) consists of two main sections. The first is the PSB header section. The fields in Table 1 on page 16 shaded light gray belong to the PSB header. This section contains the search string that the driver uses to find the PSB on paragraph boundaries within the memory-mapped range of C0000h–FFFF0h. The PSB header also contains other fields that are global to the entire PSB. There is only one PSB in the entire BIOS image.

The second section of the PSB starts with the CPUID field and continues for the remainder of the PSB. This second section contains the actual processor-specific PSTs. There may be multiple PSTs in the PSB, each corresponding to a particular processor. *Any new processor speed grade requires a completely new PST to be added to the PSB.* Each PST is broken down into two more sections: PST header and PST data. The PST header is used to identify which PST must be used for the currently installed processor. In Table 1 on page 16, the PST header fields are shaded in a dark gray. The PST data is the variable length portion of the table. It contains the FID and VID combinations for the processor performance states and is shown in Table 1 on page 16 with no shading.

Table 1. Performance State Block Structure (PSB version 1.2)

Name	Length (bytes)	Field Purpose
PSB Header		
Signature	10	Start of the PST block — Always set this field to "AMDK7PNOW!"
TableVersion	1	The version of the table as defined by AMD — Set to 12h for version 1.2.
Flags	1	Only bit 0 is currently defined. See section 4.5.1.3 on page 18 for more information.
SettlingTime	2	Worst-case amount of time that board voltage regulator needs to settle after a FID/VID change — This value is expressed in microseconds (µs). A setting of 100d (64h) (i.e., 100 µs) is pretty typical here, but check with the board designer to be sure.
Reserved1	1	Reserved for later use by AMD — Must be initialized to 00h in table version 1.2.
NumPST	1	The total number of PSTs in the PSB.
PST Header		
CPUID	4	CPUID (EAX of CPUID extended function 8000_0001h) of the processor that this PST belongs to.
FSBSpeed	1	FSB frequency, in MHz of the system. Example, 100 MHz = 100d (64h).
MaxFID	1	The maximum FID of the processor to which the PST applies.
StartVID	1	The starting VID of the processor to which the PST applies.
NumPStates	1	The number of FID,VID combinations in the PST. This field must be $\geq$ 1.
FID	1	FID code — Refer to the applicable processor data sheet for the FID codes.
VID	1	VID code — Refer to the applicable processor data sheet for mobile VID codes.
----------	---------	FID,VID pairs are concatenated here so that the total number of pairs is equal to the value in the NumPStates field.

For PSBs that contain more than one PST (e.g., NumPST > 1), a new PST is concatenated immediately following the last VID code of the last performance state of the table. Table 2 shows the PST block format when NumPST > 1.

Table 2. Performance State Table (PST) Block Format When NumPST >1

Name	Length (bytes)	Function
PST Header		
CPUID	4	CPUID of the processor that this PST belongs to.
FSBSpeed	1	FSB frequency (in MHz) of the system. Example: 100 MHz = 64h.
MaxFID	1	The maximum FID of the processor to which the PST applies.
StartVID	1	The starting VID of the processor to which the PST applies.
NumPStates	1	The number of FID-VID combinations in the PST. This field must be ≥ 1.
FID	1	FID code
VID	1	VID code
----------	----------	FID,VID pairs are concatenated here so that the total number of pairs is equal to the value in the NumPStates field.

4.5.1 PST Field Descriptions

The following subsections describe the fields in the PST.

4.5.1.1 Signature

The signature field allows the driver to find the table in memory by searching in the range of C0000h–FFFF0h. This field must always be set to "AMDK7PNOW!" for mobile AMD Athlon processor-based platforms.

4.5.1.2 TableVersion

The TableVersion field determines how a particular table is formatted. Unexpected future events may require the addition of information that is not in the table described here. In this case, a new version of the table will have to be defined. The major revision of the table is in the high nibble and the minor revision is in the low nibble. For example, version 1.0 of the table will have a 10h in this field, version 1.5 will have a 15h in this field, etc. The values in this field will only change based on guidance from AMD.

4.5.1.3 Flags

The flags field for version 1.0 of the PST block only defines a meaning for bit 0. All other bits must be configured by BIOS to read back as zeros. Bit 0 is called VR_TYPE and identifies the type of voltage regulator installed on the motherboard. A value of 0 indicates a mobile voltage regulator is installed**.** *All mobile platforms must boot up with VR_TYPE = 0*. This bit is provided in case AMD PowerNow! technology is ever used to support a "green" desktop system. If the motherboard uses a desktop voltage regulator, this bit must be initialized to 1 by the BIOS. The only purpose for this bit is so higher layers of software can correctly translate the VID codes to their corresponding voltages for display to the end user (demos, etc.).

4.5.1.4 SettlingTime

The SettlingTime field is the worst case amount of time that the board voltage regulator needs to settle after a FID/VID change. This value in this field is expressed in µs. A setting of 100 (i.e., 100 µs) is typical here, but check with the board designer. This field has nothing to do with the settling time of the internal processor PLL. The PLL settling time is handled automatically by the AMD PowerNow! driver.

4.5.1.5 Reserved1

The Reserved1 field is reserved for future use by AMD. BIOS must configure this field to read back as 00h in table versions 1.2 and earlier.

4.5.1.6 NumPST

The NumPST field indicates the number of PSTs that appear in the performance state block. The first PST starts immediately after the NumPST field. This field must be $\geq$ 1. Increment this field when adding a new PST due to support of a new speed grade.

4.5.1.7 CPUID

This is the CPU ID as returned in EAX after executing a CPUID, extended function 1 instruction. Upon loading, the driver will perform a CPUID instruction and then use the results returned in EAX by the instruction as part of the PST selection criteria:

```
MOV       EAX, 80000001h      ; Select CPUID extended function 1.
CPUID                         ; Execute the CPUID instruction.
```

After executing this code, EAX contains the CPU ID that can be stored in the table. EBX, ECX, and EDX are all overwritten as a result of the CPUID instruction. Refer to *AMD Processors Recognition Application Note*, order# 20734 for more information.

4.5.1.8 FSBSpeed

The FSB speed is the speed of the frontside bus clock in MHz. For example, a system with a 100-MHz FSB clock will have a value of 100d (64h). AMD Athlon processors are marketed as having a 200 or 266-MHz frontside bus and these values take into account the fact that the bus transfers data on both clock edges (i.e., "double pumped"). The FSB clock is 100 and 133 MHz for the 200 and 266 FSB devices respectively. To help remember this, the FSB clock is the processor frequency divided by the FSB multiplier. For example, a 1-GHz AMD Athlon processor with the FID set to 10x multiplier, results in the FSB = 100 MHz. This value is used by the driver when selecting the proper PST for the system.

4.5.1.9 MaxFID

This is the maximum FID for the device to which this table applies. This value is used by the driver when selecting the proper PST for the system.

4.5.1.10 StartVID

This is the Startup VID for the device to which this table applies. The driver when selecting the proper PST for the system uses this value. Note that the StartVID will always be the same as the MaxVID.

4.5.1.11 NumPStates

This is the number of performance states that are to be associated with a given speed grade of a particular series of processor.

4.5.1.12 FID, VID

These fields hold the actual performance state data in terms of FID and VID. They do *not* hold frequency values (i.e., values expressed in MHz) and voltage values (i.e., values expressed in DC volts). The order of the data is very important. The FID,VID pair that follows the NumPStates field is the lowest performance state that the processor/platform is capable of. The remaining entries must be provided in ascending performance order.

4.5.2 Checking For Correct PSB Implementation

Follow these steps to ensure that the PSB has been coded correctly:

1. Allow the BIOS to boot to the installed operating system (assumes Microsoft® DOS or Windows® operating system).

2. If running Windows, open a DOS box.

3. Run DOS debug and enter the following commands:

```
S C000:0 FFFF 'AMDK7PNOW!' [Enter]
S D000:0 FFFF 'AMDK7PNOW!' [Enter]
S E000:0 FFFF 'AMDK7PNOW!' [Enter]
S F000:0 FFFF 'AMDK7PNOW!' [Enter]
```

One of the memory searches in step 3 should locate the PSB in memory. If none of the searches finds the "AMDK7PNOW!" string, the PSB has not been correctly implemented. If the string is found, check to see that it starts on a paragraph boundary. If not, the AMD PowerNow! technology driver may not find it.

If the table appears to be properly located, install the AMD PowerNow! software package (i.e., the driver and daemon pieces). Then install the AMD PowerNow! demo. This additional software is available from AMD. The demo program allows manual control of the performance states. Manually force the system to each performance state, and then ensure that the processor frequency is correct for that state. The demo program has a built-in processor frequency display for this purpose. Finally, measure the frequency core voltage for each performance state. Ensure that the voltage for each performance state is within tolerance for processor and for the board. Refer to the processor data sheet for electrical tolerances.

4.6 BIOS Must Identify the Processor

The BIOS is required to set the processor to the maximum processor performance state during POST. The BIOS must ascertain that the processor is mobile capable before doing this or a general protection fault (GPF) will result. This requires the BIOS to specifically identify the processor. Mobile AMD Athlon processor identification starts off exactly the same as the desktop AMD Athlon processors. For a detailed initial identification procedure, refer to the following documents:

AMD Processor Recognition Application Note, order# 20734

AMD Athlon™ and AMD Duron™ Processors Recognition Application Note Addendum, order# 21922

As part of the foregoing procedure, execute CPUID standard function 1 as follows:

```
MOV EAX, 1h
CPUID
```

- If EAX returns from CPUID standard function 1 with 6 (0110b) in the *instruction family* field, and 3 (0011b) in the *model* field, then the processor is a mobile AMD Duron™ processor model 3. This processor has no mobile application-specific hardware support for BIOS to be concerned with.
- If EAX returns from CPUID standard function 1 with 6 (0110b) in the *instruction family* field, and 7 (0111b) in the *model* field, then the processor is an AMD Duron processor model 7.
- If EAX returns from CPUID standard function 1 with 6 (0110b) in the *instruction family* field, and 6 (0110b) in the *model* field, then the processor is an AMD Athlon processor model 6.

Both the AMD Duron processor model 7 and the AMD Athlon processor model 6 come in desktop and mobile configurations. Use CPUID extended function 8000_0007h to determine whether the device is intended for desktop or mobile applications. Note that CPUID extended function 8000_0007h is not supported on earlier devices. Even though both the AMD Duron processor model 7 and the AMD Athlon processor model 6 support CPUID extended function 8000_0007h, you can perform an optional "sanity check" step to verify this. To determine whether or not the processor supports the new CPUID extended function 8000_0007h, execute extended function 0 of the CPUID instruction as follows:

```
MOV EAX, 8000_0000h
CPUID
```

If EAX returns with the value of 7, then the new CPUID extended function 8000_0007h (Get Advanced Power Management Feature Flags) is supported. To determine whether it is the desktop or mobile version of the part, execute CPUID extended function 8000_0007h on parts that support it. For example:

```
MOV EAX, 80000007h
CPUID
```

Upon return, EDX will contain the extended capabilities of the processor as follows:

EDX[2] – If set, device supports VID control.

EDX[1] – If set, device supports FID control.

EDX[0] – If set, temperature-sensing diode is present.

At the time of this writing, the only bit patterns returned are as follows:

- 0000_0001h = Device only has the sensing diode (i.e., a part intended for desktop use)
- 0000_0007h = Device has VID and FID support as well as the sensing diode (i.e., a part intended for mobile use). FID and VID support is required for implementing AMD PowerNow! technology.

4.7 BIOS Must Set Up the ClkCtl MSR

The ClkCtl MSR (C001_001Bh) is a 32-bit register that controls certain characteristics of the CPUs internal PLLs. The ClkCtl MSR is set up one time during POST based on the processor identified in the system and does not change as a result of AMD PowerNow! technology-initiated FID changes.

Mobile AMD Athlon processor model 6 and mobile AMD Duron processor model 7 use a different value than the desktop version of the processor. The ClkCtl MSR is configured to a value of 6007_9263h on mobile processors as follows:

```
MOV        ECX, 0C001001Bh
MOV        EAX, 60079263h
WRMSR
```

For BIOS implementations that must support several generations of AMD Athlon and AMD Duron processors, use the above supplied ClkCtl MSR values in conjunction with the initialization code example supplied in the *AMD Athlon™ Processor BIOS Developers Guide,* order# 21656.

4.8 BIOS Must Set the Processor to the Maximum Performance State During POST

BIOS must configure the mobile AMD Athlon processor to run at the maximum supported processor performance state early in the BIOS initialization process. This action not only speeds up POST, but is an absolute requirement of the AMD PowerNow! software. If the processor is a mobile version, the new MSRs provided in the mobile AMD Athlon processor model 6 and mobile AMD Duron processor model 7 provide an easy way to determine the maximum processor voltage and FSB multiplier that may be used. The following two registers are part of the new mobile support provided in the mobile AMD Athlon™ 4 processor model 6. Full details on these registers are provided in the processor data sheet. Accessing either of these MSRs on a processor that does not have the mobile features enabled (i.e., laser cut to be a desktop part) will result in a general protection fault. For more information on this, refer to the applicable data sheet. For decoding FID and VID codes, refer to Section 4.3 on page 14.

4.8.1 MSR C001_0041h: FidVidCtl[63:0]

This MSR is used to activate and control FID/VID transitions and is accessible only on mobile AMD processors. For all bit fields defined as being read/write, the values read back after a cold reset (assertion of RESET#) are undefined. INIT# assertion does not change their state. Figure 1 shows the FidVidCtl register and Table 3 lists the register bit definitions.

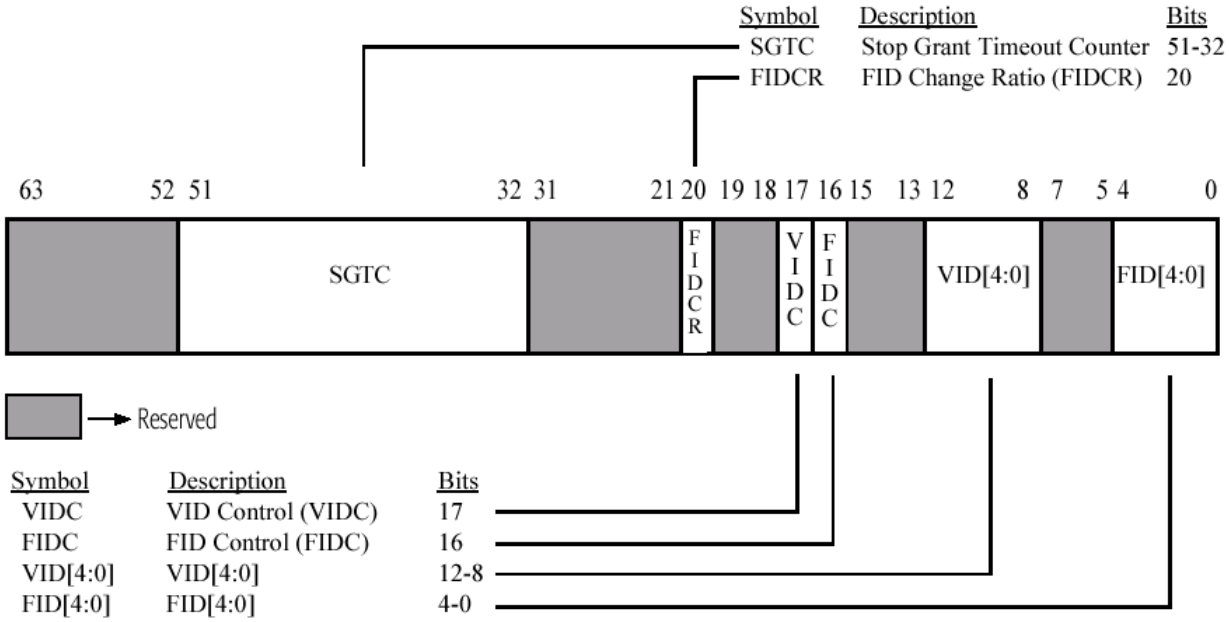

Figure 1. FidVidCtl Register - MSR C001_0041h

Table 3. FID and VID Control Register Bit Definitions

Bits	Access	Name	Function
63–52	WrtOnly		Reserved
51–32	WrtOnly	SGTC	Stop Grant Timeout Counter Set this field to a non-zero value to effect a change to the performance state dictated by the VID and FID bit fields of this register. The value written is a delay (in units of 10 ns for mobile applications) that the processor will wait after changing voltage and frequency before commencing operation at the new performance state (max delay is 10.48 ms). This delay is necessary to allow the processor PLL and motherboard voltage regulator to stabilize. The recommended settling time is 100 µs but may be longer based on the voltage regulator used. Program this 20-bit field with 02710h (10000 decimal). This delay will occur even if other fields of this MSR disallow any mode change. This field reads back as zero.
31–21	WrtOnly		Reserved
20	RdWrite	FIDCHG RATIO	FID Change Ratio During Stop Grant For mobile platforms that do not incorporate an APIC, BIOS must set this bit whenever writing to the FidVidCtl register.
19–18	WrtOnly		Reserved
17	RdWrite	VIDC	VID Transition Control 0 – VID transition is disabled. When this bit is clear, VID changes will not occur. 1 – VID transition is enabled. When this bit is set, writing a non-zero value to the SGTC field will result in a VID change based on what is in VID[4:0] of this register.
16	RdWrite	FIDC	FID Transition Control 0 – FID transition is disabled. When this bit is clear, FID changes will not occur.. 1 – FID transition is enabled. When this bit is set, writing a non-zero value to the SGTC field will result in a FID change based on what is in FID[4:0] of this register.
15–13	WrtOnly		Reserved

Table 3. FID and VID Control Register Bit Definitions (continued)

Bits	Access	Name	Function
12–8	RdWrite	VID[4:0]	A 5-bit VID code for new core processor voltage to use. This bit field controls the bit pattern driven from the processor VID pins to the processor voltage regulator on the motherboard. Attempts by software to configure the processor to run at a higher voltage setting than listed in the MVID field of MSR C001_0042h will fail. If this is attempted, the highest allowable VID will be programmed (i.e., CVID of MSR C001_0042h will be set to MVID). Changes requested through this register have no effect unless the SGTC field is simultaneously written to a non-zero value.
7–5	WrtOnly		Reserved
4–0	RdWrite	FID[4:0]	A 5-bit FID code for new FSB multiplier to use. This bit field controls the operational frequency of the processor. Specifying a value that is higher than highest frequency supported by the processor, as reported by the MFID field of the FidVidStatus register, causes the processor to run at that highest supported frequency. Changes requested through this register have no effect unless the SGTC field is simultaneously written to a non-zero value.

4.8.2 MSR C001_0042h: FidVidStatus[63:0]

This read-only MSR is used to report the current FID and VID settings in effect. It also allows read back of the default FID and VID startup settings and of the maximum FID and VID settings. Figure 2 shows the FidVid Status Register and Table 4 lists the register bit definitions.

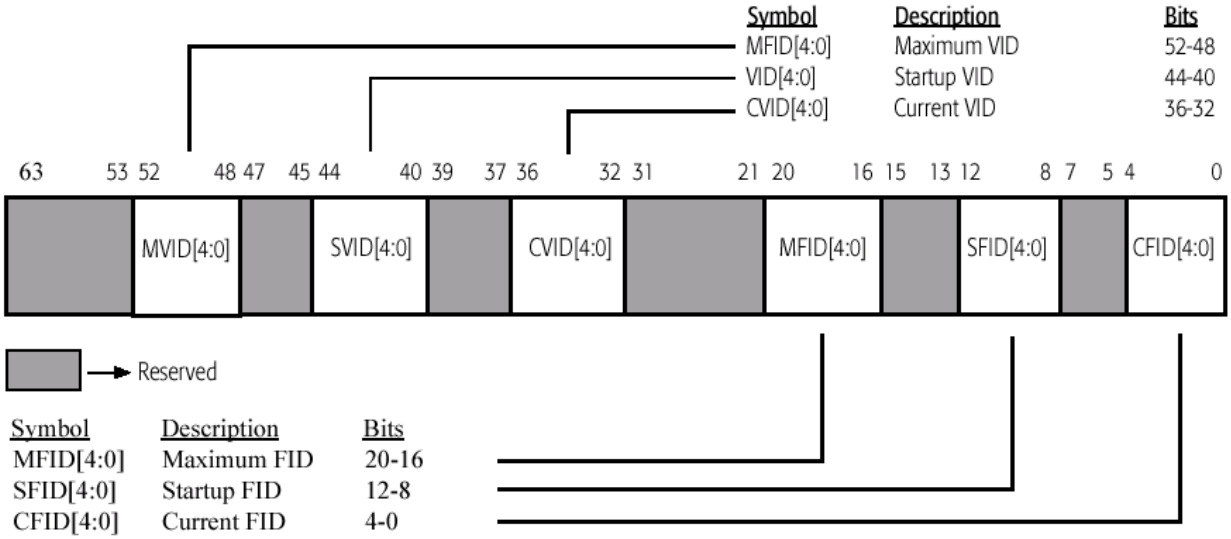

Figure 2. FidVid Status Register – MSR C001_042h

Table 4. FID and VID Status Register Bit Definitions

Bits	Access	Name	Function
63–53	RdOnly		Reserved
52–48	RdOnly	MVID[4:0]	Maximum VID Code This 5-bit field is hardwired at the time of manufacture and represents the maximum rated voltage for the processor. Refer to the applicable processor data sheet for the VID-to-voltage conversion table.
47–45	RdOnly		Reserved

Table 4. FID and VID Status Register Bit Definitions (continued)

Bits	Access	Name	Function
44–40	RdOnly	SVID[4:0]	Startup VID Code This 5-bit field is hardwired at the time of manufacture and is the 5-bit VID code in effect after assertion of cold processor reset (RESET#). Asserting INIT# does not force this VID to be invoked.
39–37	RdOnly		Reserved
36–32	RdOnly	CVID[4:0]	Current VID Code This is the 5-bit VID code currently in effect. In other words, it reads back the bit pattern that the processor VID output pins are driving to the processor voltage regulator. Upon the assertion of RESET#, this bit field will read back the same as the SVID field of this register. After that, software may change the VID output pins (and the value of this bit field) using MSR C001_0041h.
31–21	RdOnly		Reserved
20–16	RdOnly	MFID	Maximum FID Code This 5-bit field is hardwired at the time of manufacture and represents the highest FSB multiplier possible for the processor. To determine the highest possible operating frequency for this processor, decode this field into its multiplier value and then multiply by 100 MHz.
15–13	RdOnly		Reserved
12–8	RdOnly	SFID[4:0]	Startup FID Code This 5-bit field is hardwired at the time of manufacture and is the 5-bit FID code in effect after assertion of cold processor reset (RESET#). Asserting INIT# does not force this FID to be invoked.
7–5	RdOnly		Reserved
4–0	RdOnly	CFID[4:0]	Current FID Code This is the 5-bit FID code currently in effect. To determine the current operating frequency of this processor, decode this field into its multiplier value (see the applicable processor data sheet) and then multiply it by 100 MHz.

4.8.3 Setting the Processor to Maximum Performance

Use the following code to force the processor to the maximum performance state. Two MSR writes are performed to the FID_VID_CTL register. The MSR writes are always required any time that both the processor frequency and processor voltage need to be changed to a new performance state. If the performance state is being increased, the voltage must be increased first, followed by an increase in frequency. If the performance state is being reduced, the frequency must be lowered first, followed by a reduction in voltage. Since BIOS is increasing the performance state, it must first update the VID and then, as a separate operation, update the FID. This code should be implemented such that it is executed *after* the ClkCtl and Northbridge registers have been initialized. Failure to maintain this ordering will result in system lock up. This code must be executed *before* the BIOS runs its processor speed determination algorithm so that the full-rated speed of the processor is shown on the BIOS boot screen. The OEM must ensure that the BIOS displays the full-rated speed of the processor during POST. This will be the indication that the initial speed set operation has been correctly implemented.

```
; ----------------- Equates ------------------------------------
FID_VID_CONTROL EQU     0C0010041h
FID_VID_STATUS          EQU     0C0010042h

FIDC                    EQU     00010000h               ; Fid  Change Enable Bit
VIDC                    EQU     00020000h               ; Vid Change enable Bit
FidChgRatio             EQU     00100000h               ; Defined by AMD
SGTC_DELAY              EQU     00002710h               ; 10,000ns = 100 microseconds
; ------------------------------------------------------------------
;
; Read CPU's MaxFID and MaxVID settings and set current VID & FID to those settings.
;

mov     ecx, FID_VID_STATUS         ;  FidVidStatus
RDMSR                               ;  Read the MSR into EDX:EAX

shr     eax, (16-0)                     ;  Move MFID bits [20:16] to FID field [4:0]
and     ax, 001Fh                           ;  Mask non-MFID bits

shr     edx, (16-8)                 ;  Move MVID bits [20:16] to VID field [12:8]
and     edx, 1F00h                  ;  Mask non-MVID bits

or      eax, edx                      ; Combine MFID and MVID bits into EAX
or      eax, (VIDC+FidChgRatio)       ; FidChgRatio is defined by AMD
mov     edx, SGTC_DELAY               ; Set up SGTC for 100us delay

mov     ecx, FID_VID_CONTROL        ; Set up to write to FID_VID_CTRL MSR
WRMSR                               ; Frequency going up so change VID first

                                                ; Note:  ecx, edx:eax unchanged by WRMSR
xor     eax, (VIDC or FIDC)  ; Clear VIDC, set FIDC bits
WRMSR                               ;Now change  FID as a separate step
```

5 Caveats Associated with Changing Performance States

When changing performance states using AMD PowerNow!™ technology, consideration should be given to the use of the Time Stamp Counter (TSC) and performance state transition latency.

5.1 Use of the Time Stamp Counter (TSC) on AMD PowerNow!™ Technology-Enabled Processors

The Time Stamp Counter (TSC) is a 64-bit counter of all processor clock cycles that have occurred since processor reset. For example, on a 600-MHz processor, this counter would increment 600 million times in one second. This counter is sometimes used to make high-resolution timing measurements on small sections of code. In this type of application, the counter would read the TSC (using the RDTSC instruction) before and after the section of code to be timed, and then the counter readings would be subtracted from each other to obtain elapsed time. Effective use of the TSC is not trivial even on a system that is not enabled with AMD PowerNow! technology. The user must understand and apply serializing techniques to make up for out of order instruction execution, etc. While an exhaustive discussion of TSC use is beyond the scope of this document, the user must be aware that AMD PowerNow! technology-enabled platforms add complexity to the use of the TSC.

TSC readings are inaccurate after AMD PowerNow! technology performance state transitions. During the transition, the processor's PLL loses phase and frequency lock. During the time that the lock is lost, the TSC does not increment as it would under normal operation. For this reason, it is recommended that TSC measurements be done in a critical section. AMD PowerNow! technology transitions are software driven events, and are never performed as the result of a hardware event driven SMI. As such, they do not interrupt code that is performed within a critical section.

Before TSC readings can be converted to time values, the processor frequency must be known. Since AMD PowerNow! technology has the ability to dynamically control the processor frequency, software is responsible for reading the current processor frequency before taking TSC readings. The current processor frequency must be read within the critical section previously mentioned. The current processor frequency may be ascertained by reading MSR C001_0042[4:0] to obtain the current FID setting. The FID can be converted to the processor frequency using information given in "FID (Frequency ID)" listed in the appropriate AMD Athlon processor or AMD Duron processor data sheet.

5.2 AMD PowerNow!™ Technology Performance State Transition Latency

Some specialized applications which have extremely tight real time requirements may be affected by performance state transitions that occur under AMD PowerNow! technology control. For mobile AMD Athlon and mobile AMD Duron processors, the time overhead of a performance state change is much less than for a Mobile AMD-K6® processor-based system since there is no requirement to enter into SMM to make the transition. The period during which interrupts can not be used to service devices with real-time processing needs is limited to the latency of the hardware itself. This performance state transition latency breaks down as follows:

- Northbridge disconnect time. Before a performance state transition can occur, the processor must inform the Northbridge of the fact via a special cycle, and the Northbridge must perform a disconnect from the processor. If cache probes are pending, the Northbridge device should be designed to wait for them to complete before disconnecting.
- The PLL and voltage regulator stabilization times. These must be accounted for by programming an appropriate value in SGTC[19:0] of the FidVidCtl MSR. The counter begins counting RESETCLK periods after the AMD system bus disconnect is achieved and the new FID and VID are loaded. Each RESETCLK period is typically equal to the system clock period which is 10 ns (1/100 MHz) for mobile applications. The PLL requires approximately 50 µs to re-lock. However, it is anticipated that the transition time of the processor voltage regulator on the motherboard be the limiting factor since this requires approximately 100 µs to reach the new VID setting.
- The AMD system bus reconnect latency. This time is primarily associated with ramping the processor's internal clock grid back up to full frequency from its programmed low power divide down ratio. Depending on the configuration, the latency may be as high as 30 µs.

While the latency can vary slightly based on whether cache probes are pending, e.g., at the time the SGTC is written, the variance is quite small as compared to the main latency contributor, namely the VR settling time. As mentioned above, this is designed to be 100 µs.