AMD Geode™ GX1 Processor ADL Stability Issue at 333 MHz

1.0 Scope

Customers have reported a system stability issue with the Geode™ GX1 processor at 333 MHz. AMD has determined that the problem is excessive core voltage noise, which creates instability in the internal core clock generator. AMD has further determined that it is difficult to design a low noise circuit board using standard engineering practices.

This technical bulletin describes the issue and what measures can be taken to mitigate core voltage noise and additional measures that can be taken in the GX1 processor's operational environment to reduce susceptibility to this noise.

2.0 Discussion

2.1 Description of Problem

The GX1 processor core clock is generated from the 33 MHz system clock using a circuit called the Analog Delay Loop (ADL). The ADL has delay elements that can be added or subtracted in order to keep the processor core clock as close to nominal frequency as possible. As the silicon warms, it slows down, requiring delay elements to be removed. Conversely, as the silicon cools, it speeds up, requiring delay elements to be added. The ability to add delay elements is controlled by a circuit called the Incrementor.

At certain temperatures and high core voltage noise, the Incrementor can make an incorrect adjustment and a processor core clock is skipped, resulting in a system hang. The case temperature is typically around 50°C, but can vary by as much as 15°C from part to part.

The fundamental characteristic of the core voltage noise is instantaneous change in current demand. Processor pipeline stalls, executing floating point instructions, and executing the Halt (HLT) instruction are examples that cause these current impulses. Inductance of the processor package, board, and processor die combine to create voltage dips and rises depending on the direction of the impulse (instantaneous increase or decrease of current). Capacitance acts to reduce the effect of the impulse by delivering some of the current impulse.

2.2 System Board Core Voltage Noise Mitigation

AMD uses the Geode SP4GX10 development/validation platform to perform stress and stability testing on the 333 MHz SKU. Because this platform was designed for a PGA package, AMD designed an interposer board that has a PBGA footprint to mount the EBGA package. This interposer has two ground planes, a 3.3V plane, a core voltage plane, and two signal layers. It has four 220 µF core voltage capacitors and four 220 µF 3.3V capacitors. Additionally it has many high frequency capacitors. It turns out that this interposer board has a high degree of noise immunity. The stress and stability testing was successful and the 333 MHz SKU went into production.

Standard board design techniques do not impose a two ground plane, a 3.3V plane, and a core voltage plane requirement on the system designer. Of course building a six layer board instead of a four layer board increases cost. However, based on AMD's stress and stability testing and the inability of several 333 MHz customers to achieve system reliability due to excessive system noise, AMD believes that a six layer board with two ground planes, a 3.3V plane, and a core voltage plane surrounding the GX1 8.2.2 revision part will offer additional noise immunity.

This recommendation is due to the success of the interposer board to reduce the core voltage noise to an acceptable level. AMD has not built a board with this recommendation. Therefore, at this time, AMD cannot guarantee that this recommendation will provide the necessary margin in all cases.

2.3 Operational Environment Core Voltage Noise Sensitivity Mitigation

If the system board mitigation efforts prove to be unsuccessful, there are two programming changes that can be implemented to reduce the effect.

2.3.1 Disable “Suspend-On-Halt”

It has been observed that enabling the Suspend-On-Halt feature exacerbates the problem. As the processor goes in and out of Halt, the current consumption changes rapidly causing a fluctuation in V_{CORE} on the die. To incrementally reduce the system noise, it is recommended that Suspend-On-Halt be disabled.

2.3.2 Disable the Incrementor

If the problem still exists when Suspend-On-Halt has been disabled, it is recommended that the Incrementor be disabled. Disabling the Incrementor has shown to be effective in eliminating the instability problem with the ADL, but there is a limitation in the maximum temperature change allowed in the negative direction. This configuration currently has limited validation time.

The GX1 temperature specification is 0° to 85°C. Without the Incrementor enabled, a unit that is heated to 85°C and then cooled to 0°C will be out of specification, because the core clock will run too fast. Preliminary determination from the design is that the minimum core clock period allowed at 333 MHz is 2.60 ns. Empirical data suggests that the maximum temperature change that satisfies this requirement is 50°C. This was determined by heating the GX1 processor to 85°C on an SP4GX00/SP4GX10 development platform and then cooling the part and measuring the temperature at which the worse case period is less than 2.60 ns.

For example, a unit heated to 85°C, should not be cooled below 35°C in the same session. A part that needs to run at 0°C should not first be warmed above 50°C. The maximum and minimum temperatures supported are not changed. Once the part is rebooted through a Power-On-Reset, the restriction is reset.

Although disabling the Incrementor is thought to be a robust solution, it is the responsibility of the customer to test this configuration for stability in order to assess their own risk.

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