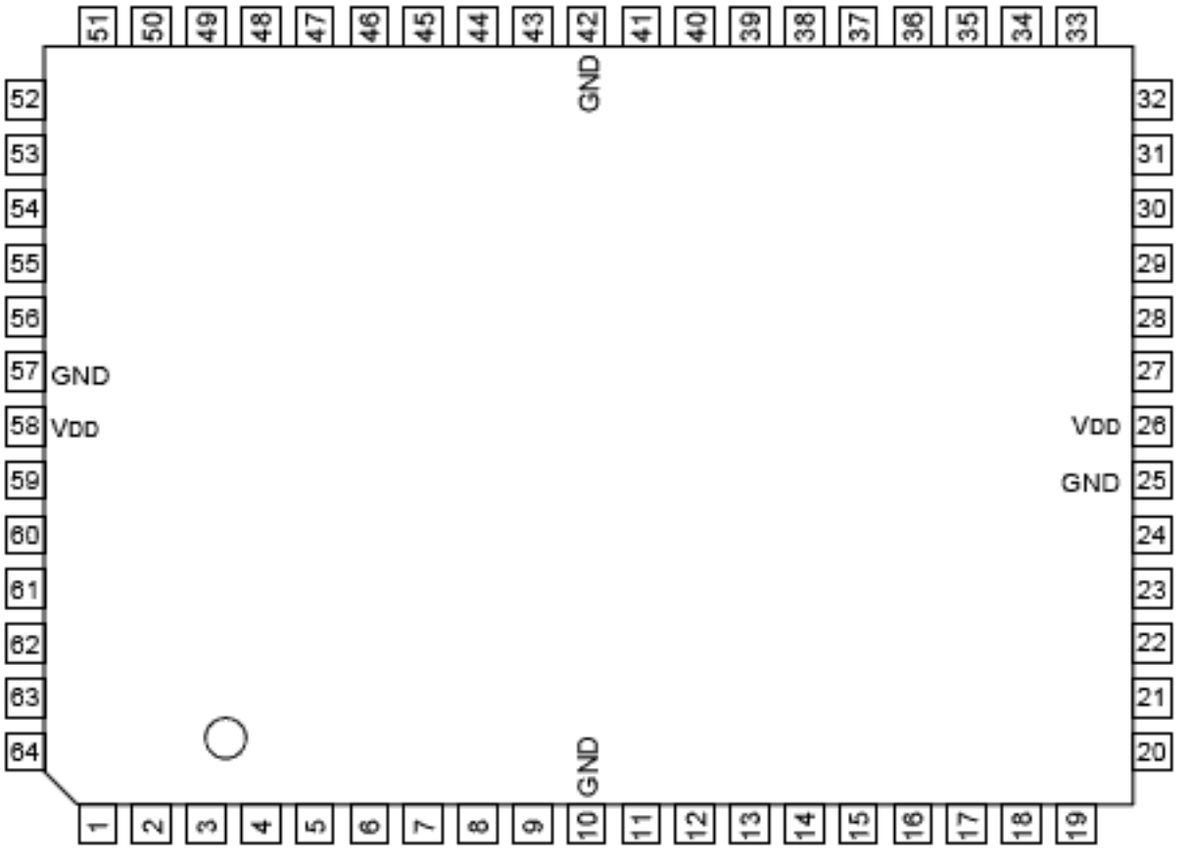
C-MOS I/O PORT EXPANDER

—TOP VIEW—

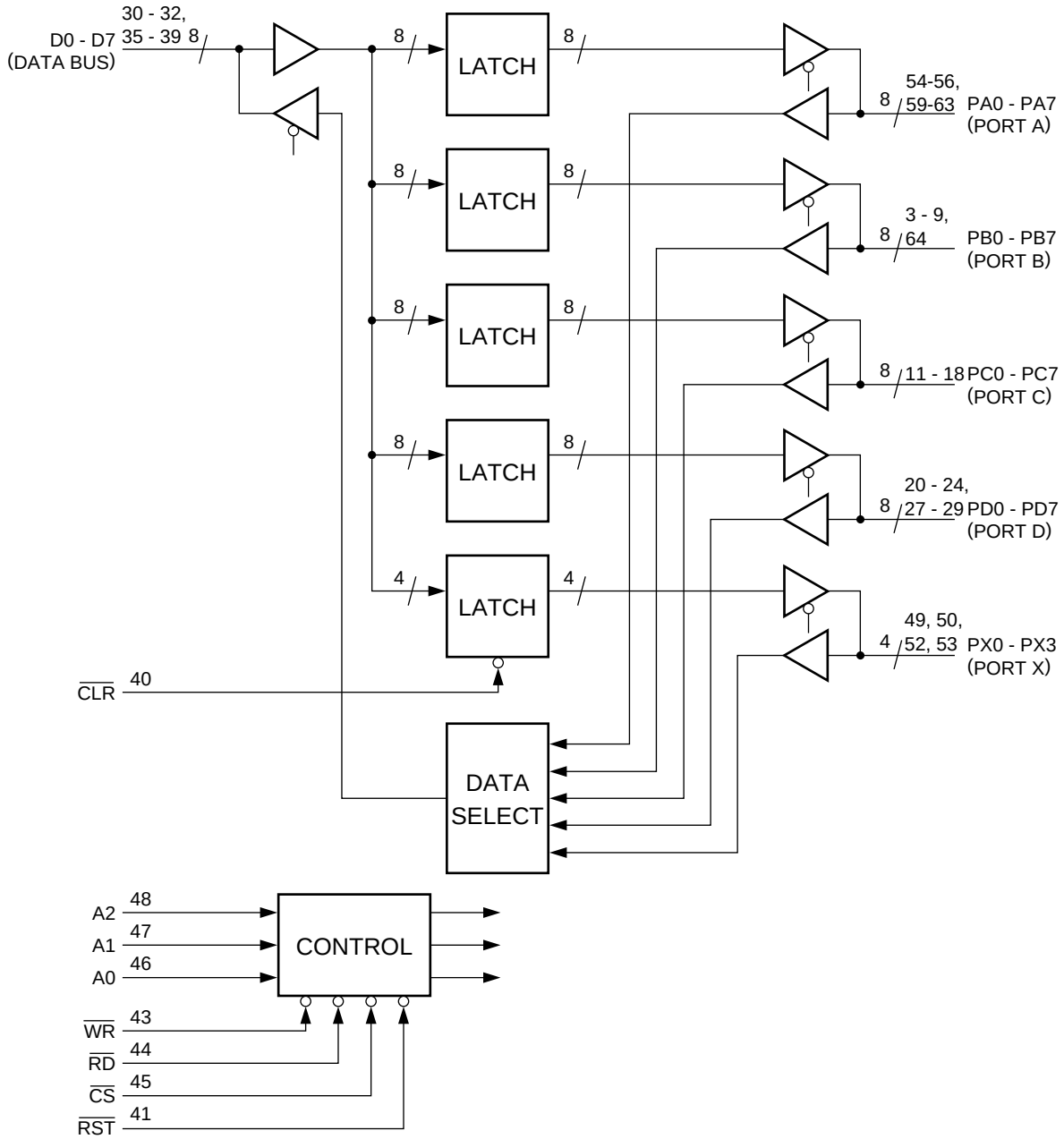


PIN No.	I / O	SIGNAL	PIN No.	I / O	SIGNAL	PIN No.	I / O	SIGNAL	PIN No.	I / O	SIGNAL
1	—	NC	17	I/O	PC6	33	—	NC	49	I/O	PX0
2	—	NC	18	I/O	PC7	34	—	NC	50	I/O	PX1
3	I/O	PB1	19	—	NC	35	I/O	D3	51	—	NC
4	I/O	PB2	20	I/O	PD0	36	I/O	D4	52	I/O	PX2
5	I/O	PB3	21	I/O	PD1	37	I/O	D5	53	I/O	PX3
6	I/O	PB4	22	I/O	PD2	38	I/O	D6	54	I/O	PA0
7	I/O	PB5	23	I/O	PD3	39	I/O	D7	55	I/O	PA1
8	I/O	PB6	24	I/O	PD4	40	I	$\overline{CLR}$	56	I/O	PA2
9	I/O	PB7	25	—	GND	41	I	$\overline{RST}$	57	—	GND
10	—	GND	26	—	VDD	42	—	GND	58	—	VDD
11	I/O	PC0	27	I/O	PD5	43	I	$\overline{WR}$	59	I/O	PA3
12	I/O	PC1	28	I/O	PD6	44	I	$\overline{RD}$	60	I/O	PA4
13	I/O	PC2	29	I/O	PD7	45	I	$\overline{CS}$	61	I/O	PA5
14	I/O	PC3	30	I/O	D0	46	I	A0	62	I/O	PA6
15	I/O	PC4	31	I/O	D1	47	I	A1	63	I/O	PA7
16	I/O	PC5	32	I/O	D2	48	I	A2	64	I/O	PB0

CS	RD	WR	A2	A1	A0	MODE
0	0	1	0	0	0	PORT A → DATA BUS
0	0	1	0	0	1	PORT B → DATA BUS
0	0	1	0	1	0	PORT C → DATA BUS
0	0	1	0	1	1	PORT D → DATA BUS
0	0	1	1	0	0	PORT X → DATA BUS
0	0	1	1	0	1	———
0	0	1	1	1	0	———
0	0	1	1	1	1	———
0	1	0	0	0	0	DATA BUS → PORT A
0	1	0	0	0	1	DATA BUS → PORT B
0	1	0	0	1	0	DATA BUS → PORT C
0	1	0	0	1	1	DATA BUS → PORT D
0	1	0	1	0	0	DATA BUS → PORT X
0	1	0	1	0	1	———
0	1	0	1	1	0	DATA BUS → CTL REG. 1
0	1	0	1	1	1	DATA BUS → CTL REG. 2
1	×	×	×	×	×	DATA BUS ; HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
× ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

D0 - D7 ; DATA BUS INPUTS/OUTPUTS
$\overline{CS}$; CHIP SELECT INPUT
$\overline{RD}$; READ STROBE INPUT
$\overline{WR}$; WRITE STROBE INPUT
A0 - A2 ; ADDRESS INPUT
$\overline{RST}$; RESET INPUT
$\overline{CLR}$; CLEAR INPUT
PA0 - PA7 ; PORT A INPUTS/OUTPUTS
PB0 - PB7 ; PORT B INPUTS/OUTPUTS
PC0 - PC7 ; PORT C INPUTS/OUTPUTS
PD0 - PD7 ; PORT D INPUTS/OUTPUTS
PX0 - PX3 ; PORT X INPUTS/OUTPUTS


30 - 32,
35 - 39
D0 - D7
(DATA BUS)
8
LATCH
LATCH
LATCH
LATCH
LATCH
4
54-56,
59-63
PA0 - PA7
(PORT A)
3 - 9,
64
PB0 - PB7
(PORT B)
11 - 18
PC0 - PC7
(PORT C)
20 - 24,
27 - 29
PD0 - PD7
(PORT D)
49, 50,
52, 53
PX0 - PX3
(PORT X)
CLR
40
DATA
SELECT
A2
A1
A0
48
47
46
CONTROL
WR
RD
CS
RST
43
44
45
41