INSTRUCTION MANUAL

B+K PRECISION 530

Semiconductor Tester

B+K PRECISION

A Product of DYNASCAN CORPORATION • 6460 W. Cortland St. • Chicago, Illinois 60635

PRICE $5.00

INSTRUCTION MANUAL

FOR

B & K-PRECISION

MODEL 530

SEMICONDUCTOR TESTER

DYNASCAN CORPORATION
6460 West Cortland Street
Chicago, Illinois 60635

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INTRODUCTION

The **B&K-Precision** Model 530 Semiconductor Tester is designed for in-circuit and out-of-circuit semiconductor testing, with special features for making additional tests on devices out-of-circuit. It uses a high-current, low duty-cycle pulse technique to test transistors in the presence of shunting circuitry, and a low-current drive system which enables the user to identify the terminals of the device in most in-circuit tests and all out-of-circuit checks.

An exceptional feature is provision for measurement of the frequency at which transistor gain is one or unity. This is the $f\tau$ rating for a transistor and is applied to bipolar devices.

For out-of-circuit measurements of transistor beta and FET gm, the low duty-cycle, high-power pulse technique provides for testing high current devices at rated current, up to 2 amperes, without over-dissipation.

The instrument is designed for a minimum amount of control manipulation, facilitating rapid testing of most devices.

SPECIAL FEATURES

1. Patented limited-energy pulse circuit permits highly successful use of in-circuit testing in the presence of low shunt impedances with complete safety for the device under test.

2. Six-position TEST switch sequentially connects the device being tested in all possible configurations making it unnecessary to know the device terminal identification. Can be left in GOOD position so that additional tests can be made without memorizing test position.

3. Base or gate lead identified by color as Test Switch is operated when testing with HI drive. All leads of transistor are identified when testing with LO drive. Gate lead is identified on FET's.

4. Automatic polarity indication to identify NPN or PNP bipolar devices and N-channel or P-channel for FET's.

5. Audible tone tells when the device under test is good – no need to take eyes off circuit board while testing hard-to-get-at devices.

6. Measures beta of low-power and high-power transistors in two ranges. A special 300 μSEC, 1% duty-cycle, high-current (I_c = 2 amp for β = 200) pulsing circuit for accurate testing of power transistors without overdissipation.

7. Measures $f\tau$ (gain-bandwidth product) of bipolar transistors.

8. Measures g_m of low-power and high-power FET's. Both depletion-mode and enchancement-mode power FET's can be tested.

9. Measures voltage breakdown and reverse voltage leakage ratings up to 100V. Automatic current limiting prevents damage to devices under test.

10. Has a compressed leakage meter scale, which displays a wide leakage current range on a single meter.

11. Clip-on test leads make positive connections to devices in difficult locations. Frees operator's hands to make further tests.

12. Choice of test leads or front panel sockets for out-of-circuit tests.

SPECIFICATIONS

IN-CIRCUIT:

- GOOD/BAD test for transistors, FET's, or SCR's.
- Identifies transistor as NPN or PNP and FET as N or P channel.
- Identifies gate lead of FET or base lead of transistor (HI drive).
- Identifies all leads of transistor when using LO drive.
- Identifies all leads of SCR.
- Identifies polarity of diodes.

OUT-OF-CIRCUIT:

- GOOD/BAD test for transistors, FET's or SCR's.
- Identifies transistor as NPN or PNP and FET as N or P channel.
- Identifies gate lead of FET by test lead color.
- Identifiers all leads of transistor or SCR by test lead color.
- Measures breakdown voltage up to 100V for transistors, SCR's and diodes.
- Measures reverse LEAKAGE from 0.5 μA to 5 mA for transistors, SCR's and diodes.
- Measures I_{DSS} and gate leakage of FET's.
- Measures β for low- and high-power transistors.
- Measure g_m for low- and high-power FET's.
- Measures $f\tau$ (gain-bandwidth-product of bipolar transistors) up to 1.5 GHz.

APPLIED TEST CURRENTS:

- Base drive: 200 mA (HI drive) or 1 mA (LO drive) at 4% duty-cycle.
- Collector Drive: 100 mA at 4% duty-cycle.
- Test Repetition Rate: 7 per second.
- Reverse Voltage for Leakage Test: 0 to 10 V (5 mA) and 10 V to 100 V (100 μA).
- Beta Base Drive Current: LOW PWR @ 50 μA continuous; HIGH PWR @ 10 mA pulsed at approximately 1% duty-cycle.

LIMITING IN-CIRCUIT SHUNT VALUES FOR VALID GOOD/BAD TEST:

- Resistance: Down to 10 ohms with HI drive.
  Down to 1.5k ohms with LO drive.
- Capacitance: Up to 15 mfd with HI drive.
  Up to .3 mfd with LO drive.

$f\tau$ MEASUREMENTS:

- Test voltage: 8 volts.
- Test current (fixed) 10 mA.
- Test ranges:
  1. $f\tau$ = 0 to 100 MHz; test frequency = 1 MHz.
  2. $f\tau$ = 0 to 500 MHz; test frequency = 10 MHz.
  3. $f\tau$ = 0 to 1500 MHz; test frequency = 30 MHz.

ACCURACY OF TEST MEASUREMENTS

Measurement	Typical	Guaranteed	
	@ 25° C.	@ 25° C.	@ 0-50° C.
Beta (High- and Low-Power)	7%	10%	15%
g_m (High- and Low-Power)	7%	10%	15%
Leakage Current	10%	20%	25%
$f\tau$	10%	20%	30%

ACCESSORIES:

- Three test leads with mini-lock clips supplied.
- Short test leads for $f\tau$ measurements, supplied.
- FP-5 Dynaflex Probe (optional).

SIZE:

13-3/8" x 10-1/8" x 4".
(34 cm x 25.7 cm x 10.2 cm.)

WEIGHT:

5.9 lbs. (2.67 Kg).

BRIEF SUMMARY OF WHAT THE 530 WILL DO

1. Determines good or bad transistors, FET's or SCR's, in- or out-of-circuit.
2. Determines good or bad diodes in- or out-of-circuit.
3. Identifies Emitter-Base-Collector leads of transistors.
4. Identifies gate lead of FET.
5. Indicates polarity of good devices (NPN or PNP; N or P channel).
6. Identifies Cathode-Gate-Anode leads of SCR's.
7. Measures all breakdown and leakage parameters of transistors.
8. Measures I_{DSS} and gate leakage of FET's.
9. Measures BV_{CES} of transistors and PIV of diodes up to 100 V.
10. Measures reverse leakage current of diodes.
11. Measures f_T of bipolar transistors, in 3 ranges: 0-100 MHz, 0-500 MHz, 0-1500 MHz.
12. Determines whether device is a transistor, FET or SCR.
13. Will test new power FET's, both enhancement and depletion types.

HINTS AND KINKS

IDENTIFYING TRANSISTORS AND DIODES

1. Nearly all germanium transistors come in metal cases, either the tubular type with flexible leads, or in the standard TO-5 package.
2. Power transistors in stud packages or in the TO-5 or TO-3 can be either germanium, silicon or FET. Two- and three-digit 2N-numbers are mostly germanium.
3. The TO-66 power transistors and the plastic power tab packages are nearly always silicon. The collector is usually, but not always, connected to the mounting tab and the center lead. This always can be verified by a continuity check between the collector pin and the mounting tab.
4. The base lead of most modern plastic-type transistors is either the center lead or the right-hand lead when facing the flat side with the leads down. In the latter case, the collector lead is in the middle.
5. Most plastic FET's have the gate lead on the right side when facing the flat side with the leads down and the source in the middle, but there are exceptions. In nearly all junction FET's, the source and drain can be interchanged with no adverse effects.
6. All transistors will have some gain with the collector and emitter leads interchanged, with the exception of Darlingtons.
7. Germanium signal diodes usually can be recognized by their transparent hollow glass cases with either three or four color bands, or type numbers printed on them. Silicon diodes usually are painted because silicon is light-sensitive and must be protected from ambient light. The "moose" types, such as the stud package, can be either germanium or silicon.
8. Power FET's in TO-3 packages generally have lead configurations similar to bipolar transistors, with the following comparisons:

FET	Transistor
Drain	Collector (case)
Gate	Base
Source	Emitter

9. The APPENDIX to this instruction manual provides the schematic symbols for devices tested by the Model 530. This information should be used to identify the device prior to testing.
10. An extensive list of semiconductor test and operating parameters is provided in the APPENDIX also.

THINGS TO KNOW ABOUT THE MODEL 530

1. There are certain semiconductor devices that look like transistors which the 530 *cannot* test. These include: triacs, diacs and diode arrays.

2. In HI drive, most transistors that test *good* will do so in *two* adjacent Test Switch positions. This is because transistors have some gain (reverse beta) when the collector and emitter are interchanged. If the circuit is heavily shunted, or the "reverse beta" of the transistor is very low, the transistor will test good in only *one* test switch position. In either case, the transistor can be considered *good*.

3. In LO drive, most transistors that test *good* will do so in only *one* Test Switch position. In some rare cases, high-frequency transistors or transistors with unusually high "reverse beta" may test good in *two* adjacent Test Switch positions having the same BASE color in the Lead Identification Window. This is still a valid *good* test, but only the base lead of the transistor can be identified.

4. FET's can be tested in either LO or HI drive, but only FET's with a high g_m will test good in LO drive. Therefore, to insure a valid good/bad test for all junction FET's, the DRIVE switch should be set to HI when the device being tested is known to be a FET. The Model 530 detection circuit is more sensitive in the HI drive position.

5. For low-power transistor beta tests, base current (I_b) is approximately 50 μA, constant current. Also, the low-power beta test is a dynamic test (square wave, small signal, superimposed upon DC bias) simulating many in-circuit conditions, not just a static DC gain test. For high-power transistor beta tests, I_b is about 10 mA, pulsed for approximately 300 μSEC and 1% duty cycle. Because the base drive (I_b) is constant, the observed collector current (I_c) varies according to the beta of the device under test.

6. In performing beta and Gm tests of transistors and FET's, it is possible to determine the collector or drain current for power devices under the test conditions, by reference to LEAKAGE/GAIN meter. The HI power beta scale is proportional to the amount of collector current (for transistors) or drain current (for FET's) under test. The 0-200 scale of the HI range can be converted to actual milliamperes by a multiplication of ten. In other words, the full scale reading of 200 corresponds to 2000 milliamperes, or 2 amps. Refer to Fig. 2 under "CONTROLS AND INDICATORS" for detailed LEAKAGE/GAIN meter scale details.

7. The LEAKAGE VOLTS test voltage that is applied to devices under test is provided with automatic current limiting, to eliminate the possibility of damage to a device under test. Up to a test voltage of 10 volts the current is automatically limited to 5 mA. Above 10 volts the current is limited to 100 μA. If a device junction breaks down below ten volts, the meter will indicate approximately full scale, regardless of the voltage setting of the LEAKAGE VOLTS adjustment. If the device breaks down above 10 volts the indicated current will not exceed 100 μA.

8. The voltage scale on the control panel is an approximation. To obtain the exact breakdown voltage, as observed by a sudden increase or change in LEAKAGE/GAIN meter current reading, a high-impedence voltmeter should be connected across the terminals of the device under test.

NOTE

DO NOT LEAVE THE METER CONNECTED TO THE DEVICE TERMINALS DURING THE LEAKAGE MEASUREMENT; OTHERWISE, AN ERRONEOUS LEAKAGE READING MAY RESULT.

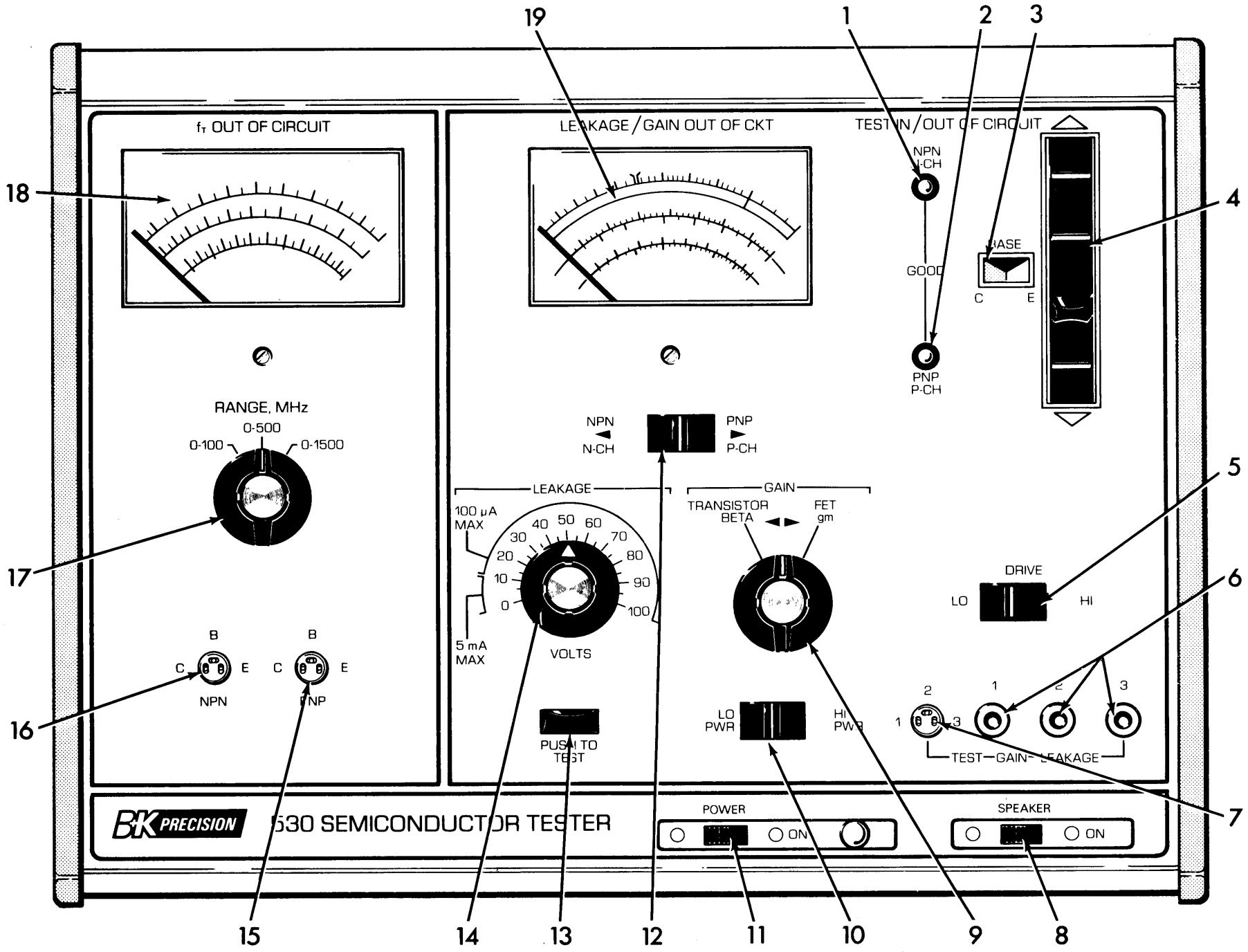


Fig. 1. Model 530 controls and indicators.

CONTROLS AND INDICATORS
(Refer to Fig. 1)

1. **NPN/N-CH Light.**
   Lights when an NPN transistor or N-channel FET tests good.

2. **PNP/P-CH Light.**
   Lights when a PNP transistor or P-channel FET tests good.

3. **Lead Identification Window.**
   Identifies leads of device under test. Colors in the window are keyed to those of the Test Lead Sockets (6).

4. **Test Switch.**
   Selects proper device connections for testing and lead identification.

5. **DRIVE Switch.**
   Selects drive levels required for the identification tests.

6. **Test Lead Sockets.**
   These sockets are receptacles for the test leads provided with the unit. The colors are keyed to the lead identification window (3) for identification of device terminals.

7. **Device Test Socket.**
   Out-of-circuit tests can be performed by inserting the device into this socket. The terminals of this socket are internally connected in parallel with those of Test Lead Sockets (6).

8. **SPEAKER-ON Switch.**
   Used to turn on or disable the audible test signal provided, as desired.

9. **TRANSISTOR BETA/FET gm Test Selector Switch.**
   Selects required test conditions for transistor or FET tests.

10. **LO PWR/HI PWR Test Selector Switch.**
    Selects test conditions for low-power or high-power devices. This applies to bipolar transistors as well as FET's.

11. **POWER-ON Switch.**
    Turns unit power on or off. The adjacent indicator lights up when unit is turned on.

12. **NPN/PNP Test Selector Switch.**
    Selects proper test conditions for out-of-circuit leakage and gain measurements. The required switch position is determined by which light, (1) or (2), is lighted in the good-bad test.

13. **PUSH-TO-TEST Switch.**
    This switch must be depressed to obtain leakage and voltage breakdown measurements when using the LEAKAGE VOLTS control (14).

14. **LEAKAGE VOLTS Control.**
    Used to adjust the test voltage for leakage and voltage breakdown tests (PUSH-TO-TEST Switch must be depressed for application).

15. **PNP Transistor Test Socket for f_T.**
    Used for f_T measurements of PNP transistors only.

16. **NPN Transistor Test Socket for f_T.**
    Used for f_T measurements of NPN transistors only.

17. **RANGE, MHz Switch for f_T.**
    Selects frequency range for f_T measurements.

18. **f_T OUT-OF-CIRCUIT Meter.**
    Provides f_T indication for transistor under test when used in conjunction with range switch (17).

19. **LEAKAGE/GAIN OUT-OF-CKT Meter.**
    Indicator for all out-of-circuit leakage and gain measurements. (See Fig. 2.)

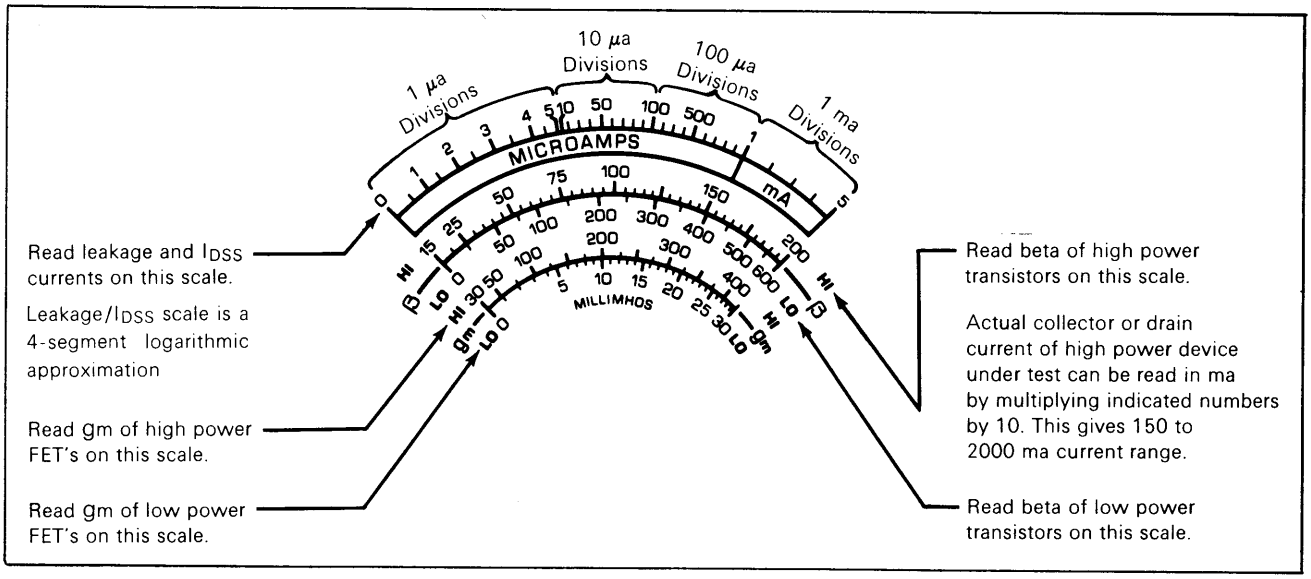


Fig. 2. Leakage/gain meter scales.

USING THE MODEL 530

IN-CIRCUIT TESTING

CAUTION

Make sure all power is turned off in the circuit being tested, and that all capacitors are discharged.

A. Transistors and FET's:

1. Set the DRIVE Switch (5) to the LO position.

2. Connect the three test leads (in any manner) to the three leads of the device you wish to test. The test leads must be plugged into their respective color Test Lead Sockets (6).

3. Move the Test Switch (4) slowly through its six positions until one of the two red lamps (1) or (2), glows. A tone also will be heard if SPEAKER Switch (8) is ON. The lamp that glows indicates whether the device is NPN (1) or PNP (2) or N or P channel. In LO drive, most transistors that test good will do so in only *one* Test Switch position (see "THINGS TO KNOW ABOUT THE 530"). In this Test Switch position, all the leads of the transistor can be identified as shown in the Lead Identification Window (3). Most FET's will test good (LO or HI drive) in *two* Test Switch positions having the same BASE color shown in the Lead Identification Window (3), since practically all junction FET's are symmetrical. The BASE color indicated is the *gate* lead of the FET.

4. If there is *no* good indication (neither of the two lamps glows) as the Test Switch (4) is slowly moved through its six positions, in LO drive, then the device under test is one of the following:

   a. Device with high leakage or very low gain (may not function properly in circuit).

   b. Device with open/shorted elements.

   c. Device with excessive circuit shunting (see "SPECIFICATIONS").

   d. FET that will not test with LO drive.

5. Re-test the device, using HI drive. In HI drive, most transistors that test good will do so in *two* adjacent Test Switch positions having the same BASE color shown in the Lead Identification Window. Only the base lead of the transistor can then be identified.

6. If the device tests good using HI drive, then 4(a) or 4(d) above could be true.

7. If the device does not test good in any Test Switch position, in HI drive, remove the device from the circuit and re-test using OUT-OF-CIRCUIT procedures.

B. SCR's:

1. Set the DRIVE switch (5) to the HI position.

2. Connect the three test leads (in any manner) to the three leads of the SCR you wish to test.

3. Move the Test Switch (4) slowly through its six positions until the NPN lamp (1) glows in one position and PNP lamp (2) glows in another position having a different BASE color as shown in the Lead Identification Window (3).

4. The SCR is good *only* if the following indications are obtained:
   a. One NPN.
   b. One PNP.

NOTE: indications must not have same BASE color.

LEAD IDENTIFICATION:

   a. The BASE color shown in the Lead Identification Window (3) is the *gate* lead when the NPN lamp (1) glows.

   b. The BASE color shown in the Lead Identification Window is the *cathode* lead when the PNP (2) lamp glows.

5. If the SCR tests *bad,* then it should be removed from the circuit and tested again (may be subject to excessive shunting in-circuit), using out-of-circuit procedures.

C. Diodes:

1. Set LEAKAGE VOLTS control (14) to zero.

2. Set Test Switch (4) to top position (Green base identification).

3. Set NPN/PNP Switch (12) to PNP.

4. Connect the blue and yellow test leads across the diode to be tested.

5. Adjust the LEAKAGE VOLTS Control (14) to approximately 10 volts, as indicated on the control panel.

6. Depress the PUSH-TO-TEST Switch (13) and, while keeping this switch depressed, rotate the Test Switch (4) to each of the upper two positions. (Green base identification.)

7. While performing step 6, observe the results on LEAKAGE/GAIN Meter (19). The meter reading will be approximately full scale for one position of Test Switch (4) while the other position of the Test Switch will give a lower reading, depending on the shunting effect of the circuitry. In the position giving the highest reading, the *cathode* of the diode under test is connected to the test lead having the collector (C) color in the Lead Identification Window (3). If both positions produce full-scale readings the diode is either shorted or heavily shunted by low-resistance circuitry; for example, a transient suppressor diode across a relay or a solenoid coil. In this case the diode should be disconnected from the circuit and re-tested using OUT-OF-CIRCUIT procedures.

D. **"Hands Off" Testing:**

When the base lead of devices being tested can be identified, leave the Test Switch in the uppermost position. The transistors can then be probed one-by-one, by connecting the green lead to the base, and the blue and yellow leads to the collector and emitter, respectively. The audible tone will tell you when the transistor is good. Occasionally, the collector and emitter leads may have to be interchanged to produce a tone.

The "Hands Off" method is useful when it is necessary to test a number of transistors in a circuit, or when it is impossible to connect all three leads to the device being tested. If one lead can be clipped onto the device, both hands will be free to probe the remaining two leads. With this feature, you can also use the **B & K-Precision** DYNAFLEX MODEL FP-5 PROBE (optional) to test devices from either side of the P.C. board.

E. **Intermittent Testing:**

Often the Model 530 can be used to identify intermittent transistors in a circuit. Connect the test leads to the suspected transistors and move the TEST Switch until the tone is heard. Then, leaving the 530 in this position, the transistor can be subjected to various physical tests such as tapping, heating, or cooling. An intermittent transistor will be indicated by an intermittent tone. A can of "Instant Cold Spray" is quite useful for providing rapid cooling of discrete components.

OUT-OF-CIRCUIT TESTING

A. **Transistors:**

1. Good-Bad Tests (power and signal transistors).

   a. Set the DRIVE Switch (5) to the LO position.

   b. Insert the transistor into Device Test Socket (7), or connect the three test leads (in any manner) to the three leads of the transistor you wish to test. The test leads must be plugged into their respective color Test Lead Sockets (6).

   c. Move the Test Switch (4) slowly through its six positions until one of the two red lamps, (1) or (2), glows. A tone also will be heard if SPEAKER Switch (8) is ON. The lamp that glows indicates whether the device is NPN (1) or PNP (2). In LO drive, most transistors that test good will do so in only *one* Test Switch position (see "THINGS TO KNOW ABOUT THE 530"). In this Test Switch position, all the leads of the transistor can be identified as shown in the Lead Identification Window (3).

   d. If there is *no* good indication (neither of the two lamps glows) as the Test Switch (4) is slowly moved through its six positions, in LO drive, then the device under test is one of the following:

      (1) Transistor with high leakage or very low gain (may not function properly in circuit).

      (2) Device with open/shorted elements.

      (3) FET that will not test with LO drive. Verify before proceeding.

      (4) Device is a Power Darlington type, which requires high base drive voltage. Re-test, using HI drive, after verifying that device is a Darlington.

   e. A transistor which tests *good* can be further evaluated for beta, f_T and voltage breakdown.

2. Beta Tests:

   a. Place the Test Switch (4) in the position in which all transistor leads are properly identified.

   b. Set the NPN/PNP Switch (12) to the position indicated by *good* test light (1) or (2).

   c. Place the LO PWR/HI PWR Switch (10) in the appropriate position, depending on the type of transistor to be tested. If no information is available for the transistor under test, the physical size generally indicates whether it is intended for high-power or low-power applications; regardless, the transistor will not be damaged if tested in both positions. In fact, a high-current and low-current beta test can be performed for any transistor.

   d. Turn the TRANSISTOR BETA/FET g_m Switch (9) to the TRANSISTOR BETA position and observe the LEAKAGE/GAIN Meter (19). Read the transistor gain on the LO or HI beta (β) scale of meter (19) depending upon whether the LO PWR or HI PWR position, respectively, of switch (10) is selected. The beta reading is given directly on each scale.

   e. If there is any doubt about the proper lead identification, note the beta reading of step "d" above and then place the Test Switch (4) in the adjacent position which has the same base color identification as observed in the Lead Identification Window (3). Hold the TRANSISTOR BETA/FET g_m Switch (9) in the TRANSISTOR BETA position and observe the beta reading obtained on meter (19). The higher reading corresponds to the proper position of Test Switch (4). The Test Switch position giving the lower beta reading is the reverse beta (collector and emitter interchanged).

   f. As a further aid in device identification, the Model 530 is designed so that no reading is obtained in step "d" if the device under test is a FET. If a reading is obtained with the TRANSISTOR BETA/FET g_m Switch (9) in the FET g_m position, the device under test is a FET and the gain or g_m, is observed on the appropriate g_m scale of the LEAKAGE/GAIN

meter (19).

3. $f\tau$ Tests:

Measurement of the $f\tau$ parameters of bipolar transistors is complex in theory and performance. A detailed explanation of $f\tau$ measurements is provided in the appendix of this manual.

When measuring $f\tau$, it is important to know that, with some transistors, the same meter deflection may occur on two ranges, such as the 0-100 MHz and the 0-500 MHz ranges. The $f\tau$ of the transistor is *always* the range reading that gives the highest numerical value (in this example, the reading on the 0-500 range applies).

a. To obtain reliable information regarding the frequency characteristics of the transistor under test, the lead identification and polarity of the device must be known as determined in the previous tests.

b. Insert the transistor under test into the appropriate $f\tau$ test socket (15) or (16). The transistor leads must properly match the socket lead designations. If the device cannot be made to fit into the socket provided, use the three-lead adapter provided to make the connections to the transistor. Note that any additional lead length can be detrimental to the accuracy of this test; therefore, the three-lead adapter should be used only if absolutely necessary.

c. Set the $f\tau$ RANGE MHz Switch (17) to the 0-1500 range and read the value on the $f\tau$ meter (18) on the 1500 MHz scale.

d. If the reading is greater than 300, this is the $f\tau$ of the transistor under test.

e. If the observed reading is less than 300, set the RANGE, MHz switch (17) to the 0-500 range and observe the meter (18). If the reading is greater than 50, this is the $f\tau$ of the transistor under test.

f. If the observed reading is less than 50, set the RANGE, MHz switch (17) to the 0-100 range and observe meter (18). This is the $f\tau$ reading of the transistor under test. The accuracy of readings below 5 on this range is questionable.

g. If there is a difference in readings on two ranges where the scales overlap, the largest absolute value for $f\tau$ is the most accurate.

NOTE ON VOLTAGE AND BREAKDOWN TESTS

All voltage and breakdown tests outlined here eliminate the need to know the device lead identification when beginning the test. In cases when the device lead identification *is* known, the following table indicates the connections required for the device tests. The indicated positions of Test Switch (4) correspond to the uppermost for position 1 and the adjacent position for position 2. Both of these Test Switch positions have the green base identification in Lead Identification Window (3). Connections can be made to the test leads provided or the device can be inserted into Test Socket (7). The required connections are indicated by an "X". Where no connection is required, "NC" is entered.

TEST LEAD COLOR AND NUMBER

Device Tests	Yellow (3) Emitter	Green (2) Base	Blue (1) Collector	Test Switch Position
BV_{CES}, I_{CES}	X	X	X	1
BV_{CEO}, I_{CEO}	X	NC	X	1
BV_{CBO}, I_{CBO}	NC	X	X	1
BV_{ECS}, I_{ECS}	X	X	X	2
BV_{ECO}, I_{ECO}	X	NC	X	2
BV_{EBO}, I_{EBO}	X	X	NC	2

4. BV_{CES} (Collector-Emitter Breakdown Voltage With Base Shorted to Emitter):

a. Connect transistor to the test leads or plug it into the test socket (7).

b. Make sure the DRIVE switch (5) is in the LO position.

c. Move the Test Switch (4) to the position which produces a *good* indication, as indicated by the polarity lights (1) or (2).

NOTE

If the good-bad test of paragraph "A-1" results in a *good* indication in two adjacent positions of Test Switch (4), the collector can be identified by observations during the leakage test as follows:

- Set the LEAKAGE VOLTS Control (14) to about 10 volts.
- Depress the PUSH-TO-TEST Switch (13) and move the Test Switch (4) between the two positions which gave a good indication.
- The Test Switch (4) position which gives the lowest indicated current on LEAKAGE/ GAIN Meter (19) is the position in which all transistor leads can be identified.

d. Set the NPN/PNP Switch (12) to the position corresponding to the polarity light (1) or (2) which lights.

e. Set the LEAKAGE VOLTS Control (14) to zero.

f. Depress the PUSH-TO-TEST button (13) and slowly increase the LEAKAGE VOLTS Control until a sharp increase or sudden change in current is observed on LEAKAGE/GAIN Meter (19). The voltage indicated on the panel is the collector-emitter breakdown voltage with the base shorted to the emitter (BV_{ces}). For an exact measurement of this voltage, connect a high-impedance voltmeter across the collector and emitter terminals of the device under test. Do not leave the voltmeter connected after the voltage measurement.

5. I_{CES} (Collector-Emitter Current With Base Shorted to Emitter):

This current is a specified limit at a specified test voltage. If these values are known, proceed as follows:

a. Leave Test Switch (4) in the test position used in the previous test.

b. The transistor connections are the same as in the previous test.

c. If only an approximate voltage indication is required, the panel calibration of the LEAKAGE VOLTS Control (14) can be used. If the exact test voltage is desired, connect a high-impedance voltmeter to the emitter and collector terminals of the device under test.

d. Depress the PUSH-TO-TEST Button (13) and set the LEAKAGE VOLTS Control (14) to the specified test voltage.

e. Disconnect the voltmeter, if used, after the test voltage has been set; otherwise the leakage current measurement will be in error.

f. With the PUSH-TO-TEST button (13) depressed, observe the leakage current as indicated on LEAKAGE/GAIN meter (19). This is the I_{CES} value of the device under test.

6. BV_{CEO} (Collector-Emitter Breakdown Voltage With Base Open):

a. After determining the proper position of Test Switch (4) in paragraph "2" above, disconnect the base lead, either by disconnecting the test lead if so connected, or by bending the base lead and inserting the transistor in the test socket (7) so that only the emitter and collector leads are connected. *Be sure that the unconnected lead does not touch the panel.*

b. Set LEAKAGE VOLTS Control (14) to zero.

c. Depress the PUSH-TO-TEST button (13) and slowly increase the LEAKAGE VOLTS control (14) until a sharp increase or sudden change in current is observed on LEAKAGE/GAIN meter (19). The voltage indicated on the panel is the BV_{CEO} value.

7. I_{CEO} (Collector-Emitter Current With Base Open):

This current is a specified limit at a specified test voltage. If these values are known, proceed as follows:

a. Leave Test Switch (4) in the test position used in the previous test.

b. The transistor connections are the same as in the previous test.

c. If only an approximate voltage indication is required, the panel calibration of the LEAKAGE VOLTS control (14) can be used. If the exact test voltage is desired, connect a high-impedance voltmeter to the emitter and collector terminals of the device under test.

d. Depress the PUSH-TO-TEST button (13) and set the LEAKAGE VOLTS control to the specified test voltage.

e. Disconnect the voltmeter, if used, after the test voltage has been set; otherwise the leakage current measurement will be in error.

f. With the PUSH-TO-TEST button (13) depressed, observe the leakage current as indicated on LEAKAGE/GAIN meter (19). This is the I_{CEO} value of the device under test.

8. BV_{CBO} (Collector-Base Breakdown Voltage With Emitter Open):

a. After determining the proper position of Test Switch (4) in paragraph "2" above, connect to, or insert the transistor under test into test socket (7) so that only the collector and base leads are connected.

b. Set the LEAKAGE VOLTS control (14) to zero.

c. Depress the PUSH-TO-TEST button (13) and slowly increase the LEAKAGE VOLTS control (14) until a sharp increase or sudden change in current is observed on LEAKAGE/GAIN meter (19). The voltage indicated on the panel is the BV_{CBO} value.

9. I_{CBO} (Collector-Base Current With Emitter Open):

This current is a specified limit at a specified test voltage. If these values are known, proceed as follows:

a. Leave Test Switch (4) in the test position used in the previous test.

b. The transistor connections are the same as in the previous test.

c. If only an approximate voltage indication is required, the panel calibration of the LEAKAGE VOLTS control (14) can be used. If the exact test voltage is desired, connect a high-impedance voltmeter to the base and collector terminals of the device under test.

d. Depress the PUSH-TO-TEST button (13) and set the LEAKAGE VOLTS control (14) to the specified test voltage.

e. Disconnect the voltmeter, if used, after the test voltage has been set; otherwise the leakage current measurement will be in error.

f. With the PUSH-TO-TEST button (13) depressed, observe the leakage current as indicated on LEAKAGE/GAIN meter (19). This is the I_{CBO} value of the device under test.

10. BV_{EBO} (Reverse Emitter-Base Breakdown Voltage With Collector Open):

a. Set the LEAKAGE VOLTS Control (14) to zero.

b. Set the Test Switch (4) to the position adjacent to that used for the BV_{CES} test of paragraph "2" which has the same base color indication in Lead Identification Window (3).

c. Disconnect the collector lead, either by disconnecting the test lead if so connected, or by bending the collector lead and inserting the transistor in Test Socket (7) so that only the emitter and base leads are connected.

d. Depress the PUSH-TO-TEST switch (13) and adjust the LEAKAGE VOLTS Control (14) until a sharp increase or sudden change in current is observed on LEAKAGE/GAIN meter (19). This is the BV_{EBO} voltage of the device under test. This voltage can be measured accurately by connecting a high-impedance voltmeter across the base and emitter terminals of the device under test. Do not leave the voltmeter connected after the voltage is adjusted.

11. I_{EBO} (Reverse Emitter-Base Current With Collector Open):

This current is a specified limit at a specified test voltage. If these values are known, proceed as follows:

a. Leave Test Switch (4) in the test position used in the previous test.

b. The transistor connections are the same as in the previous test.

c. If only an approximate voltage indication is required, the panel calibration of the LEAKAGE VOLTS control (14) can be used. If the exact test voltage is desired, connect a high-impedance voltmeter to the emitter and base terminals of the device under test.

d. Depress the PUSH-TO-TEST button (13) and set the LEAKAGE VOLTS control (14) to the specified test voltage.

e. Disconnect the voltmeter, if used, after the test voltage has been set; otherwise the leakage current measurement will be in error.

f. With the PUSH-TO-TEST button (13) depressed, observe the leakage current as indicated on LEAKAGE/GAIN meter (19). This is the I_{EBO} value of the device under test.

12. BV_{ECO} (Reverse Emitter-Collector Breakdown Voltage With Base Open):

a. Set the LEAKAGE VOLTS Control (14) to zero.

b. Set the Test Switch (4) to the position adjacent to that used for the BV_{CES} test of paragraph "2" which has the same base color indication in Lead Identification Window (3).

c. Disconnect the base lead, either by disconnecting the test lead if so connected, or by bending the base lead and inserting the transistor in Test Socket (7) so that only the emitter and collector leads are connected.

d. Depress the PUSH-TO-TEST switch (13) and adjust the LEAKAGE VOLTS control (14) until a sharp increase or sudden change in current is observed on LEAKAGE/GAIN meter (19). This is the BV_{ECO} voltage of the device under test. This voltage can be measured accurately by connecting a high-impedance voltmeter across the collector and emitter terminals of the device under test. Do not leave the voltmeter connected after the voltage is adjusted.

13. I_{ECO} (Reverse Emitter-Collector Current With Base Open):

This current is a specified limit at a specified test voltage. If these values are known, proceed as follows:

a. Leave Test Switch (4) in the test position used in the previous test.

b. The transistor connections are the same as in the previous test.

c. If only an approximate voltage indication is required, the panel calibration of the LEAKAGE VOLTS control (14) can be used. If the exact test voltage is desired, connect a high-impedance voltmeter to the emitter and collector terminals of the device under test.

d. Depress the PUSH-TO-TEST button (13) and set the LEAKAGE VOLTS control (14) to the specified test voltage.

e. Disconnect the voltmeter, if used, after the test voltage has been set; otherwise the leakage current measurement will be in error.

f. With the PUSH-TO-TEST button (13) depressed, observe the leakage current as indicated on LEAKAGE/GAIN meter (19). This is the I_{ECO} value of the device under test.

14. BV_{ECS} (Reverse Emitter-Collector Breakdown Voltage With Base Shorted to Collector):

a. Set the LEAKAGE VOLTS Control (14) to zero.

b. Set the Test Switch (4) to the position adjacent to that used for the BV_{CES} test of paragraph "2" which has the same base color indication in Lead Identification Window (3).

c. Connect the transistor to the test leads or plug it into Test Socket (7).

d. Depress the PUSH-TO-TEST switch (13) and adjust the LEAKAGE VOLTS control (14) until a sharp increase or sudden change in current is observed on LEAKAGE/GAIN meter (19). This is the BV_{ECS} voltage of the device under test. This voltage can be measured accurately by connecting a high-impedance voltmeter across the collector and emitter terminals of the device under test. Do not leave the voltmeter connected after the voltage is adjusted.

15. I_{ECS} (Reverse Emitter-Collector Current With Base Shorted to Collector):

This current is a specified limit at a specified test voltage. If these values are known, proceed as follows:

a. Leave Test Switch (4) in the test position used in the previous test.

b. The transistor connections are the same as in the previous test.

c. If only an approximate voltage indication is required, the panel calibration of the LEAKAGE VOLTS control (14) can be used. If the exact test voltage is desired, connect a high-impedance voltmeter to the emitter and collector terminals of the device under test.

d. Depress the PUSH-TO-TEST button (13) and set the LEAKAGE VOLTS control (14) to the specified test voltage.

e. Disconnect the voltmeter, if used, after the test voltage has been set; otherwise the leakage current measurement will be in error.

f. With the PUSH-TO-TEST button (13) depressed, observe the leakage current as indicated on LEAKAGE/GAIN meter (19). This is the I_{ECS} value of the device under test.

B. **FET's:**

1. Good-Bad Test (Power and Signal FET's):

a. Set the DRIVE switch (5) to the HI position.

b. Connect the device to the test leads at Test Lead Sockets (6) or insert in Test Socket (7).

c. Slowly move Test Switch (4) until the Model 530 indicates a good FET. Lamp (1) or (2) will light and a tone will be heard if the SPEAKER switch (8) is ON.

d. J-FET's will indicate good in *two* adjacent Test Switch position which have the same BASE color. (Most J–FET's are symmetrical).

e. The BASE color shown in the Lead Identification Window (3) is the *gate.*

f. If no good indication is received, then the FET under test is defective.

g. A FET which tests good can be further evaluated as indicated in the following steps. Before proceeding, make sure the device polarity has been determined as indicated by lights (1) or (2).

2. g_m Tests:

a. Move the Test Switch (4) to a position which produces a good indication.

b. Set the NPN/PNP switch (12) to the device polarity indicated by light (1) or (2).

c. Place the LO PWR/HI PWR switch (10) in the appropriate position, depending on the type of FET to be tested. If no information is available for the FET under test, the physical size generally indicates whether it is intended for high-power or low-power applications; regardless, the device will not be damaged if tested in both positions. In fact, a high-current and low-current g_m test can be performed for any FET.

d. Turn the TRANSISTOR BETA/FET g_m switch (9) to the FET g_m position.

e. Read the g_m for the FET on the appropriate g_m scale of LEAKAGE/GAIN meter (19).

CAUTION

Junction FET's can be driven into conduction and reverse breakdown by the Model 530, without damage. MOS FET's however, *can* be permanently damaged if breakdown voltages are exceeded. To avoid damage to a FET which is not positively identified as a Junction type or MOS type, do not exceed 10 volts in any of the following tests. Where the device is properly identified and test data is available, the device can be tested to specified limits as outlined in the following tests.

3. I_{DSS} Current:

Currents up to 5 milliamps can be measured below 10 volts; the current indication is limited to 100 microamps when testing above 10 volts. Although the I_{DSS} values for many J-FET's are specified at drain-to-source voltages above 10 volts, the I_{DSS} values obtained between 5 and 10 volts can be considered accurate because the drain current characteristic usually is constant above a few volts (See. Fig. 3). Most power FET's will provide full-scale readings because the I_{DSS} values are considerably higher than 5 milliamps. If a full-scale reading is obtained below 5 volts, the actual I_{DSS} value is greater than 5 milliamps and cannot be measured accurately with the Model 530.

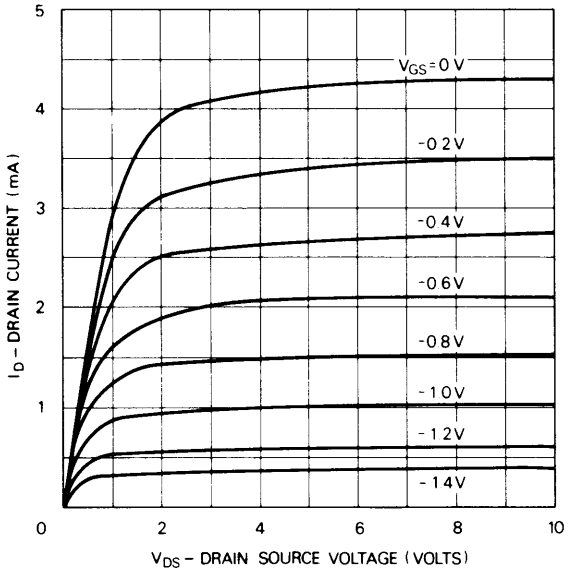


Fig. 3. Typical depletion mode FET characteristics.

a. Set the LEAKAGE VOLTS control (14) to zero.

b. Move Test Switch (4) to a position which produces a good indication.

c. Set the NPN/PNP switch (12) to the position indicated by GOOD test lights (1) or (2).

d. Depress the PUSH-TO-TEST button (13).

e. Increase LEAKAGE VOLTS control (14) and observe LEAKAGE/GAIN meter (19). Do not exceed 10 volts unless the FET type and test parameters are known. A high-impedance voltmeter can be connected across the drain and source of the device under test to determine the exact voltage corresponding to an observed I_{DSS} reading. Once the observed current exceeds 5 milliamps below 10 volts or exceeds 100 microamps above 10 volts, the panel voltage calibration does *not* apply because of the built-in current limiting circuitry.

f. The LEAKAGE/GAIN meter (19) will read I_{DSS}. I_{DSS} of FET's can range from a few microamperes to several milliamperes, and in some cases will be limited to 5 mA.

4. FET Gate Leakage: Drain-to-Gate and/or Source-to-Gate Leakage.

a. Note the polarity indicated by lights (1) or (2) in the GOOD test.

b. Set the NPN/PNP Switch (12) to the *opposite* polarity of that indicated in (a).

c. Set LEAKAGE VOLTS Adjust (14) to 10 volts, approximately, or the desired test voltage, if known.

d. Depress the PUSH-TO-TEST button switch (13) and move the Test Switch (4) through all six positions and watch LEAKAGE/GAIN meter (19). If the device is good, the meter will indicate zero current in two of the six Test Switch positions.

5. FET Drain-to-Gate or Source-to-Gate Leakage (Junction Diodes):

a. With the FET connected to the test leads or inserted in test socket (7) place DRIVE Switch (5) in the HI position and operate Test Switch (4) until a good indication is obtained. Lamp (1) or (2) will light.

b. Note the base color which appears in the Lead Identification Window (3). This identifies the connection to the gate of the FET under test.

c. Set LEAKAGE VOLTS control (14) to zero.

d. Set the NPN/PNP switch (12) to match the polarity indicated by lights (1) or (2).

e. Position the Test Switch (4) so that the color associated with the gate lead is indicated as the collector lead in the Lead Identification Window (3).

f. Depress the PUSH-TO-TEST switch (13) and slowly adjust the LEAKAGE VOLTS control (14) starting at zero and gradually increasing until a sudden increase in leakage current is indicated on LEAKAGE/GAIN meter (19). The current and the corresponding voltage have the following meaning for two types of FET's:

J-FET: Forward bias current and voltage for the gate-to-channel P-N junction.

MOS-FET: The Breakdown voltage for the combined currents of the gate-to-channel leakage current and the protection diode if present on device.

6. Depletion Mode FET's (low-power):

Drain-to-source leakage of low-power depletion mode FET's cannot be measured reliably by the Model 530, as this requires that the gate be reverse-biased while testing. Merely disconnecting the gate lead leaves the device subject to stray pickup and/or leakage currents, and with the extremely high gate impedance there is no way of assuring that the gate will pinch off.

7. Enhancement Mode FET's (Good-Bad Test):

   Enhancement mode FET's can be tested in the same way as transistors (paragraph "A-l").

C. **Diodes:**

1. Lead Identification: The anode and cathode leads of the diode can be identified.

   a. Set the POLARITY switch to the PNP position.

   b. Set the VOLTAGE ADJUST control (14) to about 5 volts.

   c. Connect the blue and yellow test leads to the diode leads.

   d. Depress the PUSH-TO-TEST Switch (13), move the Test Switch (4) to whichever of the two green BASE positions produces an upscale reading on LEAKAGE/GAIN meter (19). The diode *cathode* is connected to the test lead color indicated as the COLLECTOR (c) in the Lead Identification Window (3).

2. Leakage:

   a. Connect the blue and yellow test leads to the two ends of the diode under test.

   b. Set Test Switch (4) to the uppermost position (green base lead indication).

   c. Set NPN/PNP Switch (12) to the PNP position.

   d. Set the LEAKAGE VOLTS control (14) to about 5 volts.

   e. Depress PUSH-TO-TEST button (13) and operate test switch (4) between the upper two test positions (gree base indication).

   f. Observe LEAKAGE/GAIN meter (19) and note that in one of the two test switch positions the indicated current is high and in the other it is lower.

   g. Leave Test Switch (4) in the test position which gives the minimum or zero reading on meter (19).

   h. Adjust LEAKAGE VOLTS control (14) clockwise until a sudden increase or change in the indicated meter reading occurs. This corresponds to the breakdown voltage threshold for the diode. Any current indication indicated below the breakdown point of the diode is the leakage current for the device.

D. **Zener Diodes:**

1. Lead Identification:

   a. Connect the blue and yellow test leads to the two leads of the diode.

   b. Set the NPN/PNP Switch (12) to the PNP position.

   c. Set the LEAKAGE VOLTS Control (14) to about 5 volts.

   d. Depress the PUSH-TO-TEST Switch (13) and, while alternating between the two top positions of the Test Switch (4), note which Test Switch position gives the higher reading on the LEAKAGE/GAIN meter (19).

   e. Now the leads can be identified by the Lead Identification Window (3). The color corresponding to collector (c) is the cathode and the emitter color corresponds to the anode.

2. Zener Voltage:

   a. Connect the blue and yellow test leads to the two leads of the diode.

   b. Set the LEAKAGE VOLTS Control (14) to about 5 volts.

   c. Operate the PUSH-TO-TEST Switch (13) and select one of the two top positions of the Test Switch (4) that gives the lowest current reading as observed on LEAKAGE/GAIN meter (19).

   d. With the PUSH-TO-TEST Switch (13) depressed, increase the LEAKAGE VOLTS control (14) until a sharp increase or sudden change in current is observed on LEAKAGE/GAIN meter (19). This is the zener voltage of the device under test and at the current reading indicated.

   e. The exact zener voltage can be determined by connecting a high-impedance voltmeter to the diode terminals.

E. **SCR's:**

1. Set the DRIVE switch (5) to the HI position.

2. Connect the three test leads (in any manner) to the three leads of the SCR you wish to test.

3. Move the Test Switch (4) slowly through its six positions until the NPN Lamp (1) glows in one position and the PNP lamp (2) glows in another position having a different BASE color as shown in the Lead Identification Window (3).

4. The SCR is good *only* if all the following are obtained.

   a. One NPN indication.

   b. One PNP indication.

   c. Indications must not have same BASE color.

LEAD IDENTIFICATION:

a. The BASE color shown in the Lead Identification Window (3) is the *gate* lead when the NPN lamp (1) glows.

b. The BASE color shown in the Lead Identification Window is the *cathode* lead when the PNP lamp (2) glows.

MODEL 530 CIRCUIT DESCRIPTION

A. Test Switch

1. The 530 semiconductor tester uses a six-position lever switch located at the top right corner of the front panel. This switch is used to connect the device being tested in the correct manner for testing. As this test switch is moved through its positions, the device that is connected either to the three test leads or plugged into the test socket is connected in all possible configurations for further testing. The uppermost position is the "normal" connection, that is the test socket is connected in the standard triangle configuration to the testing circuits and the blue, green and yellow test leads are connected to the collector, base, and emitter circuits respectively (drain, gate and source for FET's).

2. In two of the six positions, using HI drive, the device is connected properly for the basic test circuitry. This is true since all bipolar transistors have gain, although usually very little, when the collector and emitter are interchanged, and most junction FET's are symmetrical. These two test switch positions are always adjacent and always display the same base color in the Lead Identification Window whenever the 530 is indicating a good device.

3. In LO drive, a transistor should indicate good in only one test switch position since limited base drive and lower detection sensitivity allow the detector to test the device as good only in its high gain connection. A device that indicates good in a single test switch position in LO drive is connected properly for further gain testing with the Model 530.

B. Good/Bad Test Circuitry

1. The Model 530 test circuitry uses two clock generators that produce a series of pulses designed to test a device periodically, about seven times per second. These short, high-current pulses are applied to the collector (drain); the first is positive for testing NPN/N-CH devices, followed by a negative pulse for testing PNP/P-CH devices. During these pulses, a shorter pulse of the same polarity is applied to the base (gate) of the device, which drives the collector (drain) voltage toward saturation. (See Fig. 4, pulses A and B.)

   Taking a closer look at the basic test circuitry, refer to Fig. 4 and schematic. The slow clock, which runs at approximately 7 Hz, initiates each test period while simultaneously resetting flip-flop 1 and flip-flop 2. The fast clock runs at approximately 500 Hz and controls the pulse-forming circuits.

2. The pulse-forming circuit uses a combination of toggles and RS flip-flop to produce the proper sequence of pulses for the collector (drain) drive circuit, and the base (gate) drive circuit.

   The collector (drain) and the base (gate) drive circuits are level-shifting complementary drivers which can deliver several hundred milliamperes at +5V and -5V, or return to zero volts.

3. A properly connected NPN or N-channel device will see both waveforms 'A' and 'B' of (Fig. 4). The collector (drain) will see waveform 'A', and the base (gate) of the device under test will see waveform 'B'.

   Note that during the positive excursion of the collector (drain) voltage, the base (gate) is driven first negative and then positive.

   If the device being tested is NPN or N-channel, the collector (drain) voltage will drop abruptly when its base (gate) is driven positive. This negative-going transition, which will only occur if gain action is present (a good device), is differentiated and the signal produced is used to latch flip-flop 1 of Fig. 4.

   If a PNP or P-channel device is tested, the turn-on transition occurs during the second half of waveform 'A' of Fig. 4, and in the opposite direction. This transition (positive-going) is differentiated and the produced signal is inverted and used to latch flip-flop 2 of Fig. 4.

   Of course, other pulses appear at the differentiator output, since all voltage transitions of pulse 'A' are similarly differentiated, but the synchronized gating circuits prevent the unwanted pulses from reaching flip-flops 1 and 2, thus eliminating wrong indications.

   The input to flip-flop 1 is enabled only during the

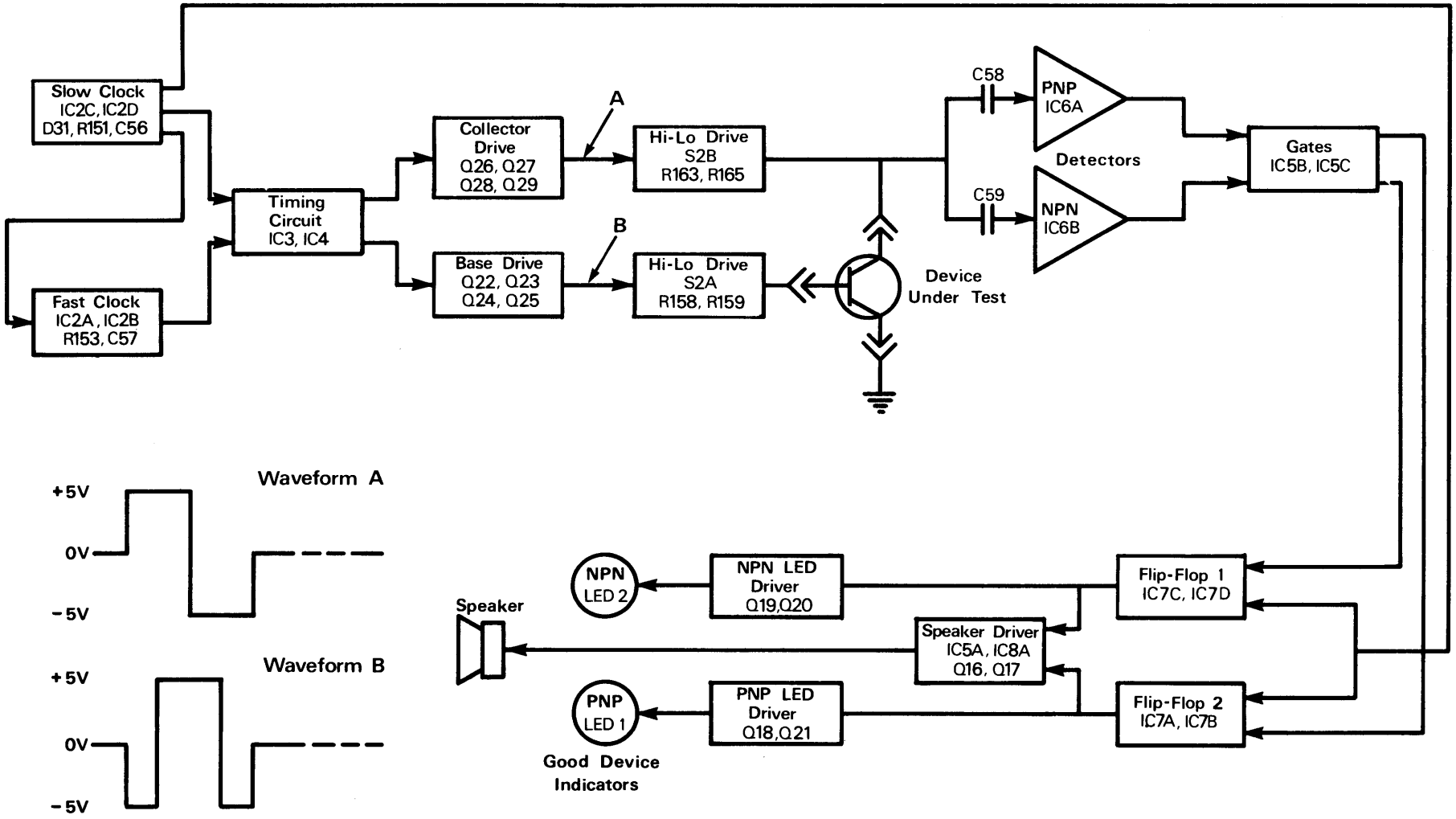


Fig. 4. Block diagram, basic test circuitry.

time period in which a NPN or N-channel device can be detected and similarly flip-flop 2 is enabled only when a PNP or P-channel device can be detected. Only the flip-flop which corresponds to the type of device being tested can be latched.

4. The outputs of flip-flops 1 and 2 of Fig. 4 are either +5V or -5V, depending on whether the device tested was a good NPN/P-channel or PNP/P-channel. The output from the activated flip-flop drives a LED DRIVER which produces enough current to turn on the corresponding front panel indicator, the NPN/N-channel or the PNP/P-channel LED.

   When either flip-flop 1 or 2 is latched, the speaker driver is activated and audible tone is heard through the speaker, indicating a good device.

C. Leakage/Breakdown Test Circuitry

1. The 530 leakage/breakdown voltage circuitry uses an externally controlled DC power supply. Voltage and current sensors control automatically, via feedback, the voltage regulator that feeds the external load (See Fig. 5 and schematic).

   A four-stage amplifier circuit is used to drive a meter driver which in turn drives the meter, on a 0 to 5 mA non-linear scale.

2. Taking a closer look at the leakage/breakdown voltage circuitry, refer to Fig. 5 and schematic.

   A voltage-adjust potentiometer is connected to a DC power supply. This potentiometer which is the front panel LEAKAGE VOLTS control, drives a series regulated circuit, and it can vary from zero to 100V. The voltage regulator is fed back through voltage and current sensors, which automatically control the voltage and current outputs to the external load.

3. The external load (device under test) is connected to the voltage regulator through the polarity switch (NPN N-channel/PNP P-channel), the lever TEST SWITCH, and is activated when the PUSH-TO-TEST switch is pressed.

   When the LEAKAGE VOLTS control on the front panel is turned clockwise, the external load voltage can go up to 100V DC, but this is ture as long as the load current is 100 μA or less. As the load impedance drops, the voltage regulator which is fed back through the voltage and current sensors, starts to reduce the voltage to maintain 100 μA through the load. This output voltage reduction and constant current of 100 μA will continue until the voltage across the external load drops to about 10V. If the load impedance is reduced to lower the external voltage below about 10 volts, the low voltage current-limiting circuit takes over and the indicated current on the LEAKAGE/GAIN meter will increase to 5 milliamperes.

   Further reduction of the load impedance, up to a complete short, will reduce the load voltage to zero. The voltage regulator is current-limited and can deliver only 5 mA to the external load.

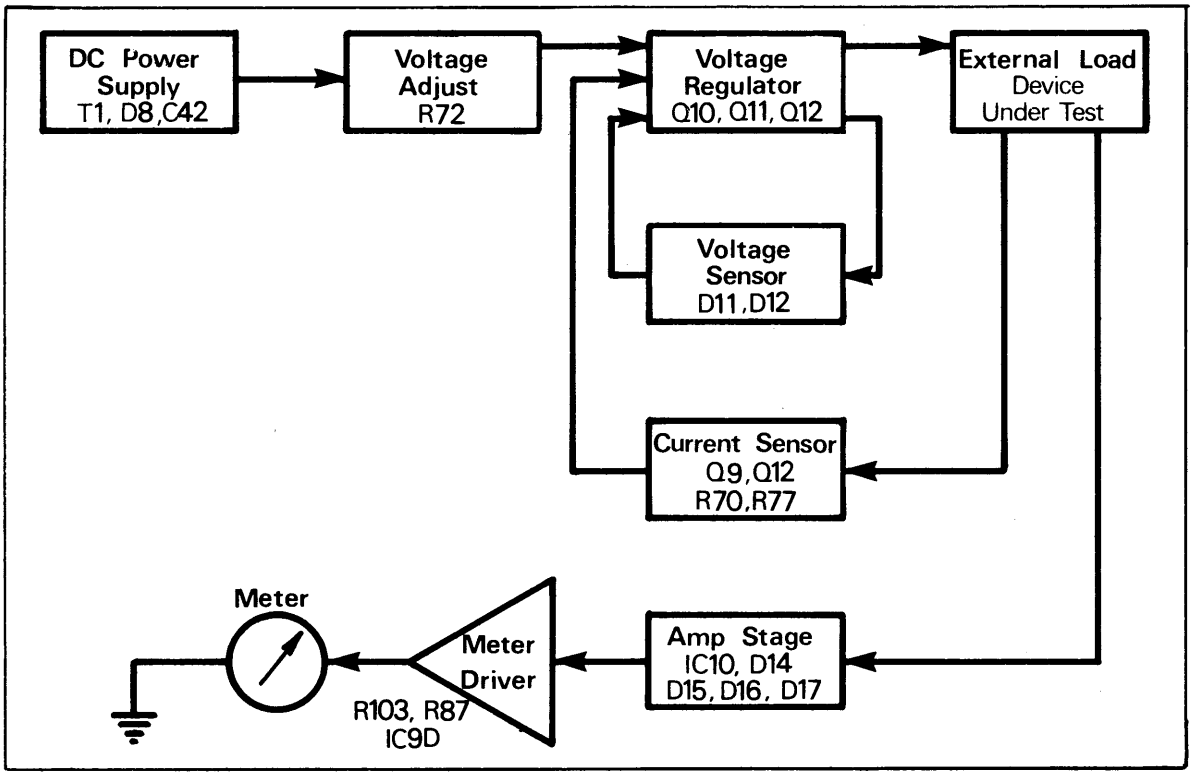


Fig. 5. Block diagram, leakage/breakdown circuitry.

4. The special voltage and current characteristics of the leakage/breakdown voltage circuitry described above is designed to protect the device under test from being damaged. This power supply automatically controls the power delivered to the device under test to ensure safe testing.

   It should be emphasized that the LEAKAGE VOLTS control potentiometer on the front panel has only limited control over the actual voltage and current seen by the external load. As long as this LEAKAGE VOLTS control is set below the 10V mark on the front panel, the circuit can deliver up to 5 mA. When the LEAKAGE VOLTS control is turned clockwise, above the 10V mark, the actual voltage across the load will rise according to the front panel marking, as long as the load current is 100 μA or less. Whenever breakdown occurs, the internal circuit controls override the front panel voltage control. The LEAKAGE VOLTS control may be set on 100V, with the front panel indication of 100 μA maximum; but the actual voltage seen by the external load may be considerably less than indicated on the front panel. The actual voltage across the external load can be measured with a high-impedance voltmeter. The actual current through the load or device under test can be seen on the top scale of the 530 leakage meter.

5. The current through the device under test drives a four-stage amplifier. This amplifier drives the METER DRIVER which in turn drives the meter.

   Each of the four stages of the amplifier drives a small portion of the meter top scale, so that the final result is a segmentally linear wide-range current indicator.

NOTES

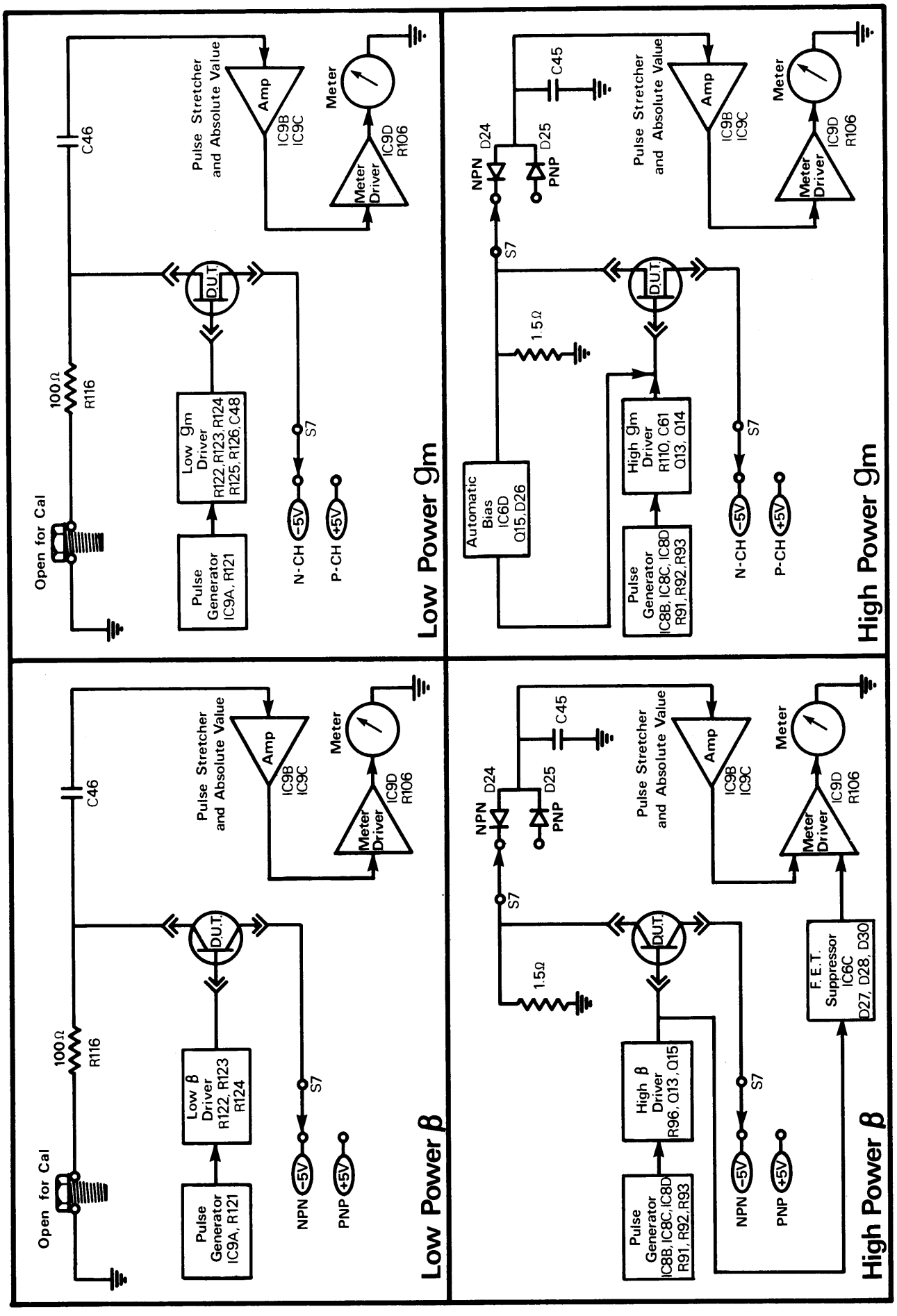


Fig. 6. Block diagram, gain function circuitry.

D. Gain Test Circuitry

The 530 gain test circuitry measures the amplification factors of the devices under test. These measurements include β ("Beta") for transistors, and g_m ("Transconductance") for field effect transistors; for both low-power and high-power devices.

For a closer look at the gain test circuitry, refer to Fig. 6 and the schematic.

1. Low-Power β

The low-power β uses a square-wave pulse generator which runs at approximately 500 Hz. This generator drives the LOW β DRIVER which in turn drives the base of the transistor under test. The transistor under test is connected to the β test circuitry through a series of front panel switches, which are set according to the user instructions in the manual. The emitter of an NPN transistor is connected to the -5V supply (+5V for PNP). The collector is connected to ground through 100Ω resistor, and AC-coupled to the low β detection and amplification circuitry.

The transistor under low β test has a fixed bias of 50 μA, over which the LOW β DRIVER superimposes a pulsating 10 μA. The collector current generates voltage across the 100Ω resistor. This voltage level will vary, depending on the gain capability of the transistor. The collector voltage is coupled to the pulse stretcher and the absolute value amplifier. The amplified pulses feed the METER DRIVER which in turn drives the LEAKAGE/GAIN OUT-OF-CIRCUIT meter.

The dynamic low-beta parameter of the transistor is read directly on the compressed Lo β scale.

2. Low-Power g_m

The low-power g_m uses the same square-wave pulse generator used for the low-power β (described in part 1 above). This generator drives the LOW g_m DRIVER which in turn drives the gate of the FET under test (See Fig. 6 and the schematic).

The FET is connected to the g_m test circuitry through a series of front panel switches, which are set according to the user instructions in this manual. The source of an N-channel FET is connected to the -5V supply, (+5V for P-channel). The drain is connected to ground through 100Ω resistor, and AC-coupled to the low g_m detection and amplification circuitry.

The FET under low g_m test is biased for its Zero Gate-Voltage Drain Current (I_{DSS}), and the LOW g_m DRIVER drives the gate with a pulsating .2V.

The drain current generates voltage across the 100Ω resistor. This voltage level will vary, depending on the gain capability of the FET. The drain voltage is coupled to the pulse stretcher and the absolute value amplifier. The amplified pulses feed the METER DRIVER which in turn drives the LEAKAGE/GAIN OUT-OF-CIRCUIT meter.

The dynamic low transconductance parameter of the FET is read directly on the compressed Lo g_m scale.

3. High Power β

The high-power β uses a PULSE GENERATOR which runs at approximately 33 Hz, with pulses having a 1% duty cycle, which corresponds to a 300 μSEC pulse every 30 mSEC. The PULSE GENERATOR drives the HIGH β DRIVER which in turn drives the base of the transistor under test. (See Fig. 6 and the schematic.). The transistor is connected to the β test circuitry through a series of front panel switches which are set according to the user instructions in this manual. The emitter of an NPN transistor is connected to the -5V supply (+5V for PNP). The collector is connected to ground through a 1.5Ω resistor. This voltage pulse height will vary, depending on the gain capability of the transistor. The integrated collector pulses are amplified to feed the METER DRIVER, which in turn drives the LEAKAGE/GAIN OUT-OF-CIRCUIT meter. The dynamic high-beta parameter of the transistor is read directly on the Hi β scale.

To disable any erroneous meter indications whenever a FET is tested in this position, a FET SUPPRESSOR circuit senses the base emitter junction voltage. The typical base emitter drop of a transistor is .6 VDC; if this voltage is higher than 3 VDC, the device under test is probably a FET or a defective transistor; and the FET SUPPRESSOR circuit suppresses the METER DRIVER amplifier to prevent a meter indication.

4. High-Power g_m

The high-power g_m uses the same pulse generator used for the high power β (described in part 3 above). This generator drives the HIGH g_m DRIVER which in turn drives the gate of the FET under test. (See Fig. 6 and the schematic.).

The FET is connected to the g_m test circuitry through a series of front panel switches which are set according to the user instructions in this manual.

The source of an N-channel FET is connected to the -5V supply, (+5V for P-channel). The drain is connected to ground through 1.5Ω resistor, and also through a germanium diode to the high g_m pulse stretcher and absolute value amplifier.

The FET under high g_m test is driven by a pulsating 4.7V gate-to-source voltage, at 1% duty cycle. The drain current generates voltage across the 1.5Ω resistor; this voltage pulse height will vary depending on the gain capability of the FET.

To insure proper testing of both depletion and enhancement mode power FET's, an AUTOMATIC BIAS circuit senses the drain current and, through feedback, adjusts the gate voltage for a "just on" condition. Depending on the device under test, this bias voltage can vary from -11V to +12V, on top of which the HIGH g_m DRIVER

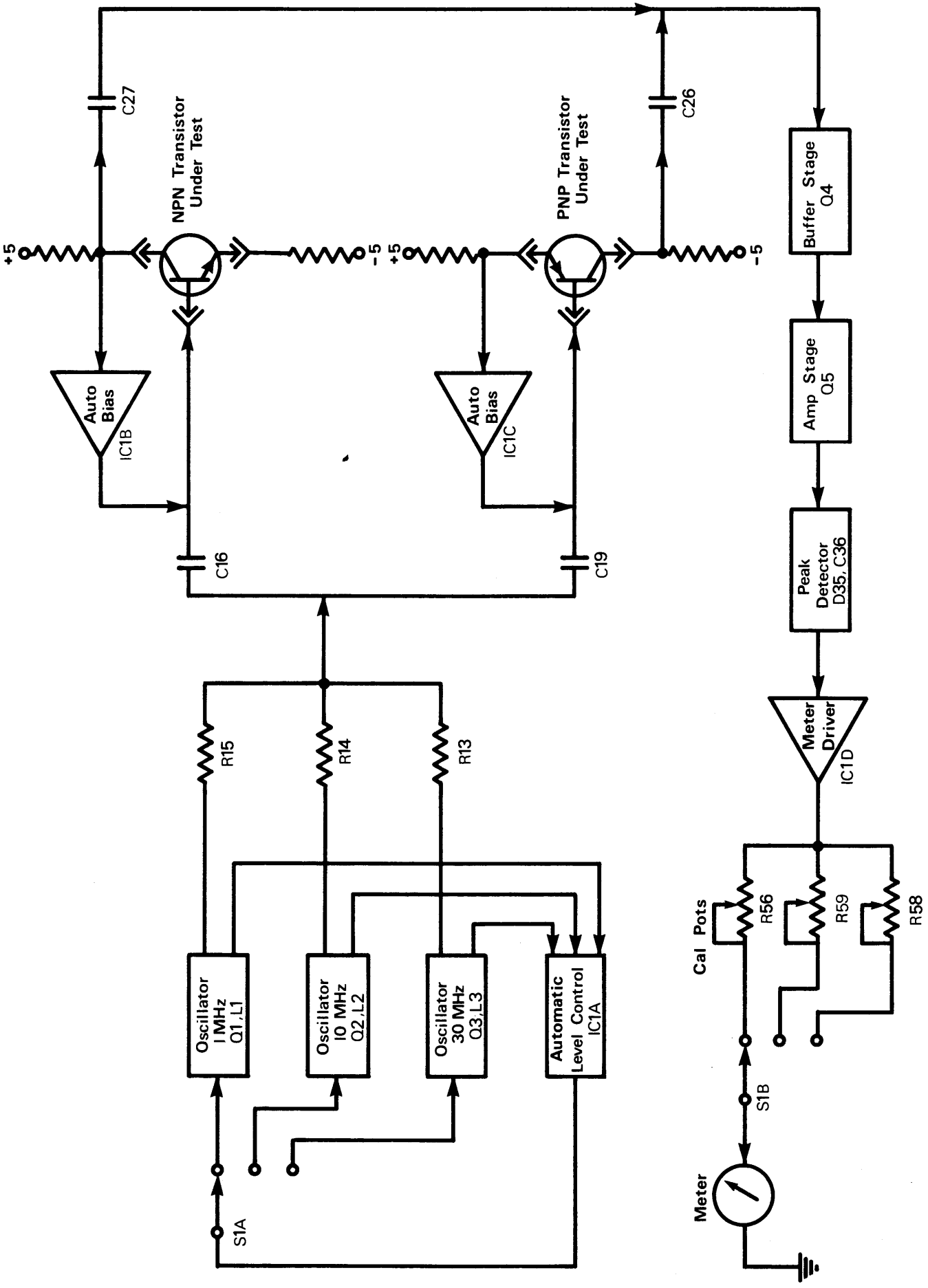


Fig. 7. Block diagram, fr test circuitry.

superimposes the 4.7V pulsating gate-to-source voltage.

The integrated drain pulses are amplified to feed the METER DRIVER which in turn drives the LEAKAGE/GAIN OUT-OF-CIRCUIT meter. The dynamic high transconductance parameter of the FET is read on the Hi g_m scale.

E. f_T Circuitry

The 530 f_T circuitry measures the gain-bandwidth product of bipolar transistors. This high frequency characteristic of transistors is measured on three separate frequency levels, which correspond to the three switch positions and the three meter scales. For a closer look at the f_T circuitry, refer to Fig. 7 and the schematic.

Three tuned oscillators generate three f_T base frequencies: 1, 10 and 30 MHz. An AUTOMATIC LEVEL CONTROL provides feedback to the oscillators to regulate the outputs to a fixed level. The signal output of the oscillator in use is fed through a resistor and a coupling capacitor to the base of the transistor under test.

An AUTO BIAS circuit senses the collector current of the transistor under test and automatically varies the base drive for 10 mA collector current.

The amplified collector signal is fed through a coupling capacitor to a current-to-voltage converter BUFFER STAGE. The buffer signal drives the transistor AMPLIFIER STAGE. The amplified signal is rectified in the PEAK DETECTOR and the DC voltage level is fed to the METER DRIVER, which in turn drives the meter for the f_T value on the range used.

NOTES

MAINTENANCE AND CALIBRATION

A. Leakage/Gain Meter "Zero" Calibration

1. Turn the Model 530 power off. If LEAKAGE/GAIN meter (19) does not indicate zero, insert a suitable screwdriver in the hole just below the meter and adjust it to indicate zero on top scale.

2. Turn the Model 530 power on, if the LEAKAGE/GAIN meter (19) indicates zero on top scale, proceed to step #4. If the LEAKAGE/GAIN meter (19) does not indicate zero, turn the 530 power off, unplug the unit and remove the 530 bottom panel by removing the five screws (three on bottom panel and two on back panel).

3. Plug in the unit and turn power on. Adjust the zero control trimpot R-87 with suitable screwdriver so that meter is at zero. Refer to Fig. 8 for trimpot location.

4. With power on, set the HI PWR/LO PWR switch (10) to "LO PWR" position. Turn TRANSISTOR BETA/FET g_m switch (9) to "TRANSISTOR BETA" position. LEAKAGE/GAIN meter (19) should read zero on top scale; if not, remove bottom panel of the 530 and adjust zero β CAL trimpot R-106 with suitable screwdriver (while holding the TRANSISTOR BETA/FET g_m switch (9) in "TRANSISTOR BETA" position) so that the LEAKAGE/GAIN meter (19) reads zero on top scale. Refer to Fig. 8 for trimpot location.

B. Leakage Circuitry Calibration

1. LEAKAGE/GAIN meter (19) should be zero calibrated as per section "A" above.

2. Plug the Model 530 into power source and turn power on.

3. Set Test switch (4) to the top-most position. Set NPN/PNP switch (12) to "NPN/P-CH" position.

4. Connect a 5.1 KΩ resistor in series with a DC milliamp meter, to the blue an yellow test lead sockets (6) of the 530. (Blue socket should be connected to the positive lead of the external meter).

5. Press Model 530 PUSH-TO-TEST switch (13) and adjust front panel LEAKAGE VOLTS control (14) so that the external meter reads 0.9 milliamp DC.

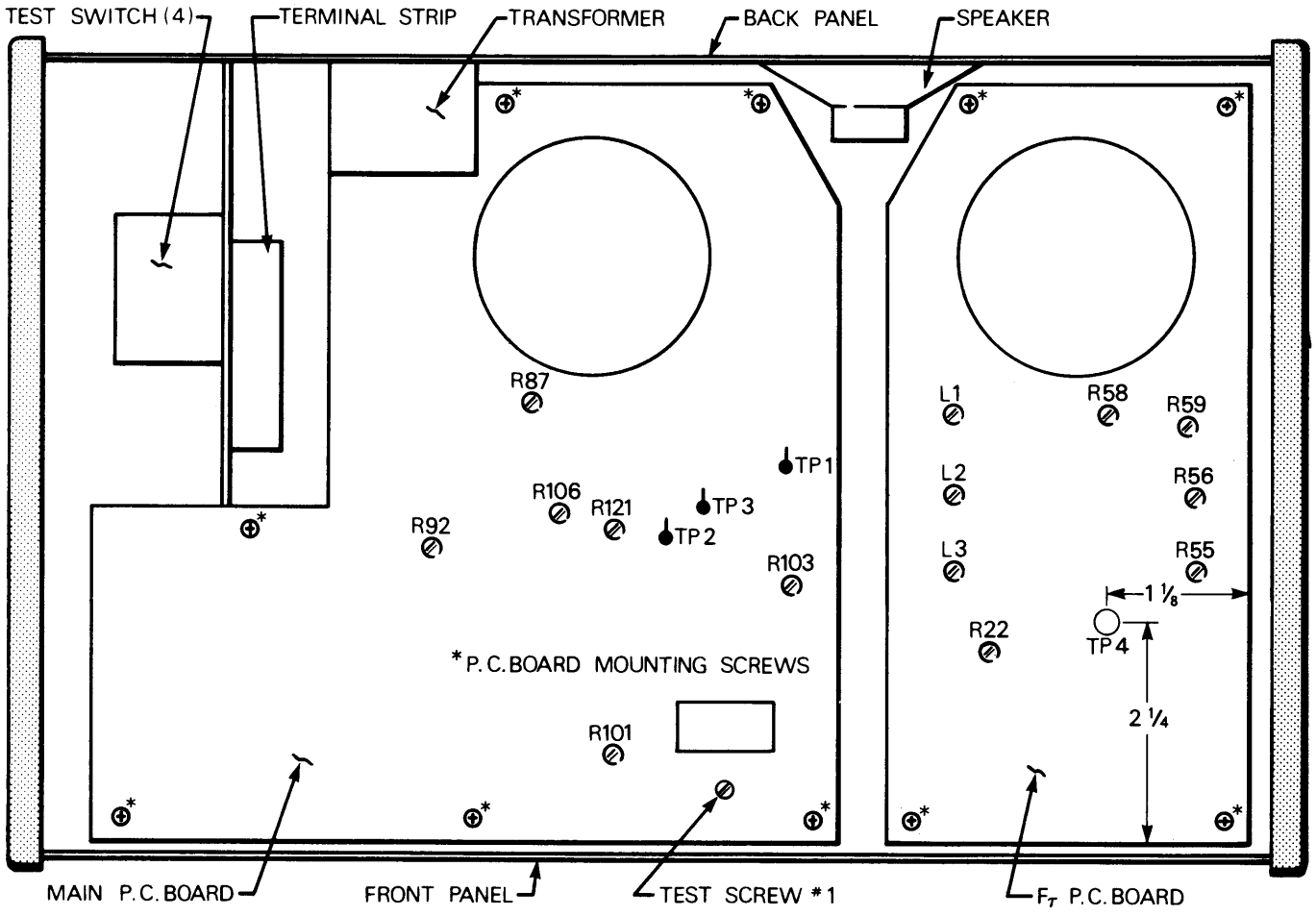


Fig. 8. Bottom view of Model 530, with bottom panel removed.

6. The Model 530 LEAKAGE/GAIN meter (19) should read 900 μA on top scale. If meter does not read 900 μA, unplug the 530 and remove the bottom panel.

7. Plug the 530 into the power source and repeat step #5. With suitable screwdriver, adjust trimpot R-103 so that LEAKAGE/GAIN meter (19) reads 900 μA on top scale. Refer to Fig. 8 for trimpot location.

C. Low Beta/g_m Calibration

1. Leakage/gain meter should be zero calibrated as per section "A".

2. Unplug the Model 530, and remove the bottom panel (by removing the five screws, three on bottom panel and two on pack panel).

3. Build yourself a simple resistive network as shown in Fig. 9 (either by fixed resistors or by adjusting trimpots).

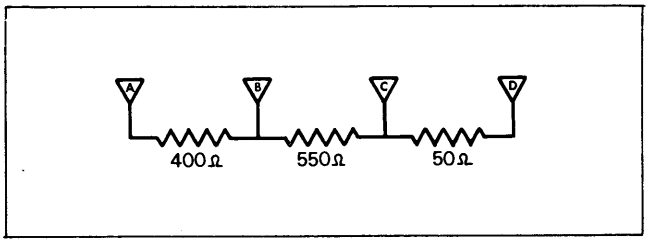


Fig. 9. Resistive network.

4. Remove the small grounding TEST screw #1 and washer from back of the main P.C. board (at the corner next to the pushbutton switch). Refer to Fig. 8. Connect a lead between point "A" of the resistive network (Fig. 9) and main P.C. board test point 2 (TP-2); also connect a lead between point "D" (Fig. 9) and main P.C. board test point 3 (TP-3). Refer to Fig. 8.

5. Set HI PWR/LO PWR switch (10), of the Model 530, to the "LO PWR" position. Set NPN/PNP switch (12) to the "NPN/N-CH" position. Lever Test switch (4) should be in the top-most position. Connect the blue test lead, which should be plugged into the blue test lead socket (6), to point "C" of resistive network (Fig. 9).

6. Plug the Model 530 into the power source and turn power switch (11) on. Turn TRANSISTOR BETA/FET g_m switch (9) to "TRANSISTOR BETA" position. LEAKAGE/GAIN meter (19) should read "50" on LO β scale. If not, adjust main P.C. board trimpot R-121 with suitable screwdriver (while holding the TRANSISTOR BETA/FET g_m switch (9) in "TRANSISTOR BETA" position), so that the meter reads "50" on LO β scale. Refer to Fig. 8.

7. Connect the blue test lead to point "B" of the resistive network (Fig. 9). Turn the TRANSISTOR BETA/FET g_m switch (9) to "TRANSISTOR BETA" position. The LEAKAGE/GAIN meter (19) should read full scale. If not, adjust main P.C. board trimpot R-101 with suitable screwdriver so that LEAKAGE/GAIN meter reads full scale. Refer to Fig. 8. Unplug the Model 530 from power and disconnect all leads. Replace test screw #1 and washer to its original position. Refer to Fig. 8.

D. High Beta/g_m Calibration

1. LEAKAGE/GAIN meter (19) should be zero calibration as per section "A".

2. Turn power switch (11) on and the DRIVE switch (10) to "LO" position. Connect the three test leads to a power transistor (any power transistor TO-3 package will do). Move Test Switch (4) through its positions until the unit indicates "GOOD" device (NPN/N-CH or PNP/P-CH lamp will light), and leave lever Test Switch (4) in that position.

3. Set NPN/PNP switch (12) to either "NPN/N-CH" or "PNP/P-CH" position, as indicated by the "GOOD" LED polarity. Set HI PWR/LO PWR switch (10) to its "HI PWR" position.

4. Identify the collector terminal of the transistor under test. Connect an oscilloscope probe to the collector lead of the power device under test. Connect oscilloscope ground lead to the back panel. (Oscilloscope should be set to DC with horizontal sweep of 10 mSEC/DIV. and vertical gain of 1 volt/div.).

5. Turn TRANSISTOR BETA/FET g_m switch (9) to the "TRANSISTOR BETA" position. Observe oscilloscope. Record pulse voltage height (V) (Fig. 10).

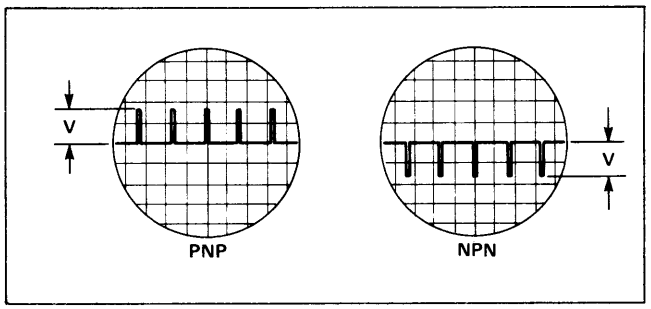


Fig. 10. Pulse voltage waveforms.

6. Using graph in Fig. 11, find the pulse height (V) (recorded in step 5), on the horizontal axis. Extend a vertical line from that point. The intersection of that line with the diagonal line when projected on the vertical axis should be the required "HI β" scale reading. Record this value "HI β CAL." If another value is on the "HI β" scale, unplug the Model 530 and remove the bottom panel to expose the printed circuit board. (Do not remove or upset test transistor connections and Model 530 control settings.

7. Plug the Model 530 into the power source. Turn TRANSISTOR BETA/FET g_m switch (9) to the

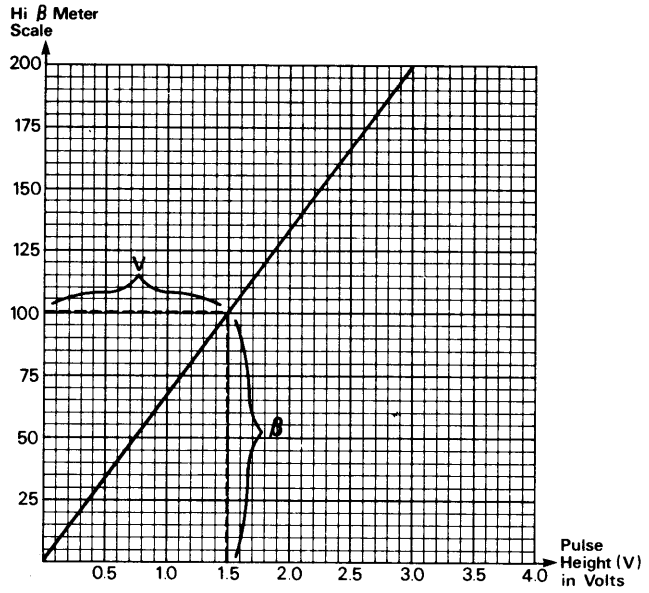


Fig. 11. Hi β calibration chart.

"TRANSISTOR BETA" position, and adjust trimpot R-92 with suitable screwdriver so that LEAKAGE/GAIN meter (19) reads the recorded "HI β CAL" value (found in step 6) on the "HI β" scale of the LEAKAGE/GAIN meter (19).

E. $f\tau$ Circuit Calibration

1. Turn Model 530 off. If $f\tau$ OUT-OF-CIRCUIT meter (18) does not indicate zero, insert a suitable screwdriver in the hole just below the meter and adjust it to indicate zero on the top scale.

2. Remove the Model 530 bottom panel by removing the five screws (three on the bottom panel and two on the back panel).

3. Turn Model 530 power on. Without any transistors plugged into $f\tau$ sockets (15) or (16), check for $f\tau$ meter (18) reading of zero for each range selected on the RANGE, MHz Switch (17). If the $f\tau$ meter (18) does not read zero, adjust R-55 to obtain a zero reading (Fig. 8).

4. Calibration of Automatic Bias Circuit.

   Equipment Required:

   - Any good quality digital Voltmeter (**B & K-Precision** Model 280).
   - Any known good NPN and PNP Transistors.

   (a) Turn Model 530 power on.

   (b) Insert NPN Transistor into front panel transistor socket labeled NPN (16).

   (c) Place current meter in series with the collector lead. (See Fig. 12.)

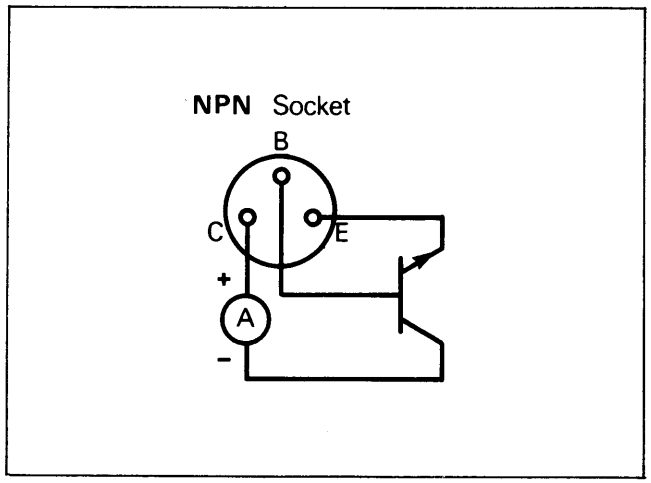


Fig. 12. Field calibration, $f\tau$ circuit.

(d) Adjust R-22 for a collector current of 10 milliamperes (See Fig. 8 for location of R-22).

(e) Remove NPN Transistor and insert PNP Transistor into front panel socket labeled PNP (15) with current meter in series with the collector lead (See Fig. 13). Current measured should be between 9 and 11 milliamperes for proper operation.

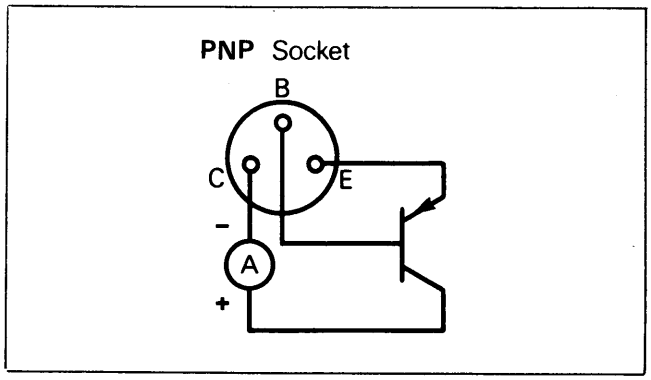


Fig. 13. Field calibration, $f\tau$ circuit.

5. Calibration of 1 MHz, 10 MHz, and 30 MHz oscillators.

   Equipment Required:

   - Frequency Counter – 100 mV sensitivity at frequency up to 30 MHz (**B & K-Precision** Model 1801).
   - Any NPN transistor with an $f\tau$ of greater than 500 MHz.
   - Non-metallic coil-adjusting tool.

   (a) Turn Model 530 power on.

   (b) Insert NPN transistor into front panel socket labeled NPN (16). All frequency measurements are taken at TP-4. See Fig. 8 for location of TP-4 and oscillator coils.

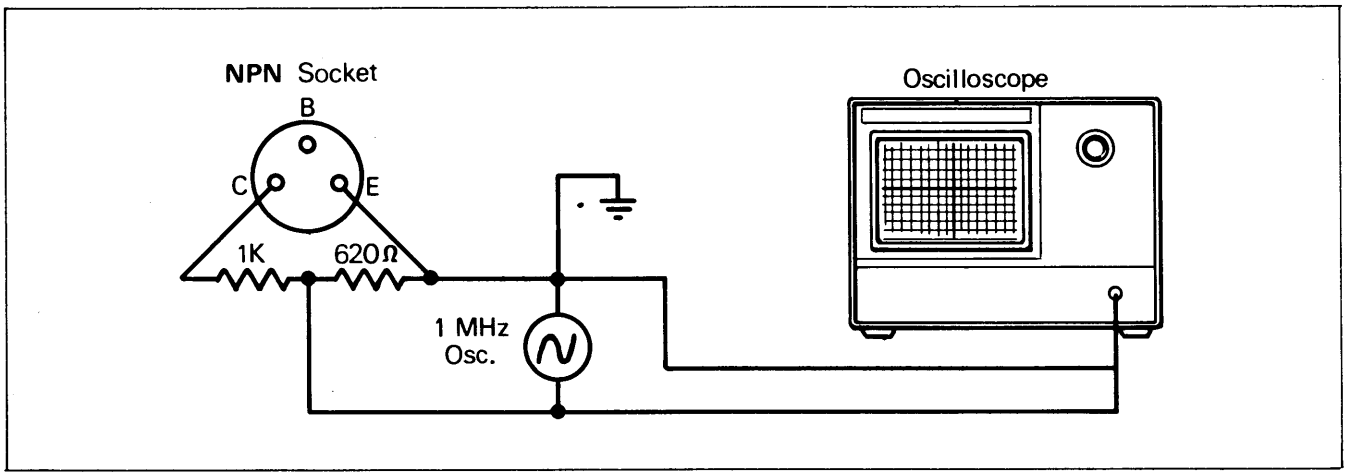


Fig. 14. Field calibration, $f\tau$ circuit.

(c) Set Range Switch (17) to 0-100. Adjust L_1 for a reading between .98 MHz and 1.02 MHz.

(d) Set Range Switch (17) to 0-500. Adjust L_2 for a reading between 9.8 MHz and 10.2 MHz.

(e) Set Range Switch (17) to 0-1500. Adjust L_3 for a reading between 29.5 MHz and 30.5 MHz.

6. Calibration of $f\tau$ Meter Scales.

Equipment Required:

- Oscilloscope with a minimum band width of 5 MHz (**B & K-Precision** Model 1472 or equivalent).
- Oscillator capable of producing a 1 MHz sine wave with an output of 1V peak-to-peak (**B & K-Precision** Model E310B or equivalent).
- One 1KΩ ±5% 1/4-watt resistor and one 620Ω ±5% 1/4-watt resistor.

(a) Connect two resistors in series and connect to Model 530 NPN Transistor Socket (16) as shown in Fig. 14. Turn power on. (See Fig. 8 for location of R-56, R-59 and R-58).

(b) Set Range Switch (17) to 0-100.

(c) Set output of external 1 MHz oscillator for output of 1V peak-to-peak.

(d) Adjust R-56 for a reading of 60 on the top scale of the $f\tau$ meter (18).

(e) Set Range Switch (17) to 0-500.

(f) Set output of external 1 MHz oscillator for output of .6V peak-to-peak.

(g) Adjust R-59 for a reading of 60 on the top scale of the $f\tau$ meter (18).

(h) Set Range Switch (17) to 0-1500.

(i) Set output of external 1 MHz oscillator for output of .6V peak-to-peak.

(j) Adjust R-58 for a reading of 54 on the top scale of the $f\tau$ meter (18).

F. P.C. Board Service Procedures

1. Removal of main P.C. board for service.

(a) On the control panel, remove the glamor caps (lift the caps perpendicular from the panel) from the following switches:

- DRIVE switch (5).
- LO PWR/HI PWR test selector switch (10).
- NPN/PNP test selector switch (12).

(b) Pull to remove knob from the LEAKAGE VOLTS control (14).

(c) Pull to remove knob and remove the mounting nut from the TRANSISTOR BETA/FET g_m test selector switch (9).

(d) Turn the Model 530 over so that it lies with the control panel face *down* and the bottom panel *up*.

(e) Remove the bottom panel by removing the three screws in the bottom panel and two screws in the back panel nearest the bottom panel.

(f) Remove the six P.C. board mounting screws (identified with an asterisk in Fig. 8) from the main P.C. board located as follows:

- Two screws near back panel.
- Three screws near front panel.
- One screw near terminal strip.

(g) Being careful not to break any wires, raise the front edge of the main P.C. board and slide it toward the front so that the back edge clears the transformer. Next, rotate the main P.C. board with the front edge up with the board in the vertical position for full access to all components.

(h) To replace the main P.C. board, reverse the previous steps for removal.

2. Removal of fτ P.C. board for service.

(a) On the control panel, pull to remove the knob and remove the mounting nut from the RANGE MHz switch (17).

(b) Turn the Model 530 over so that it lies with the control panel face *down* and the bottom panel *up*.

(c) Remove the bottom panel by removing the three screws in the bottom panel and two screws in the back panel nearest the bottom panel.

(d) Remove the four P.C. board mounting screws (identified with an asterick in Fig. 8) from the fτ P.C. board located as follows:

- Two screws near back panel.
- Two screws near front panel.

(e) Lift the fτ board out and rotate it to a suitable position for access to service components.

(f) To replace the fτ P.C. board, reverse the previous steps for removal.

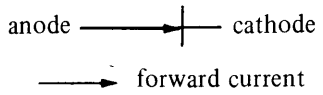
NOTES

APPENDIX

GLOSSARY OF TERMS

GENERAL:

anode. The electrode from which the forward current flows within the device.



bipolar transistor. A transistor that utilizes charge carriers of both polarities.

breakdown. A phenomenon occurring in a reverse-biased semiconductor junction, the initiation of which is observed as a transition from a region of high small-signal resistance to a region of substantially lower small-signal resistance for an increasing magnitude of reverse current.

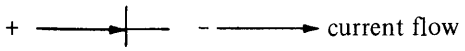
breakdown region. A region of the volt-ampere characteristic beyond the initiation of breakdown for an increasing magnitude of reverse current.

breakdown voltage. The voltage measured at a specified current in a breakdown region.

cathode. The electrode to which the forward current flows within the device. For diagram, see "anode."

electrode. An electrical and mechanical contact to a region of a semiconductor device.

forward bias. The bias which tends to produce current flow in the forward direction.



forward direction. The direction of current flow which results when the P-type semiconductor region is at a positive potential relative to the N-type region.

reverse bias. The bias which tends to produce current flow in the reverse direction.

reverse direction. The direction of current flow which results when the N-type semiconductor region is at a positive potential relative to the P-type region.

semiconductor device. A device whose essential characteristics are governed by the flow of charge carriers within a semiconductor.

semiconductor diode. A semiconductor device having two terminals and exhibiting a nonlinear voltage-current characteristic; in more restricted usage, a semiconductor device which has the asymmetrical voltage-current characteristic exemplified by a single P-N junction.

V_F – forward voltage, DC. The DC voltage across a semiconductor junction associated with the flow of forward current.

V_R – reverse voltage, DC. The DC voltage applied to a semiconductor junction which causes the current to flow in the reverse direction.

BIPOLAR TRANSISTORS:

β – common emitter current gain. For DC operation, $\beta = h_{FE}$. For small signal AC operation, $\beta = h_{fe}$.

base (B, b). A region which lies between an emitter and a collector of a transistor and into which minority carriers are injected.

collector (C, c). A region through which a primary flow of charge carriers leaves the base.

emitter (E, e). A region from which charge carriers that are minority carriers in the base are injected into the base.

f_c – small-signal, short-circuit, forward-current transfer ratio, cutoff frequency. The lowest frequency at which the modulus (magnitude) of the small-signal short-circuit forward-current transfer ratio is 0.707 of its value at a specified low frequency (usually 1 kHz or less).

f_T – transition frequency or frequency at which small-signal forward current transfer ratio (common-emitter) extrapolates to unity. The product of the modulus (magnitude) of the common-emitter small-signal short-circuit forward current transfer ratio (h_{fe}), and the frequency of measurement when this frequency is sufficiently high so that (h_{fe}) is decreasing with a slope of approximately 6 dB per octave.

f_τ – frequency of unity current transfer ratio. The lowest frequency at which the modulus (magnitude) of the common-emitter small-signal short-circuit forward current transfer ratio (h_{fe}), has decreased to unity.

h_{FE} – static forward current transfer ratio (common-emitter). The ratio of the DC output current to the DC input current.

h_{fe} – small-signal short-circuit forward current transfer ratio (common-emitter). The ratio of the AC output current to the small-signal AC input current with the output short-circuited to AC.

I_B, I_C, I_E – DC current for base-terminal, collector-terminal, emitter-terminal. The value of the DC current into the terminal indicated by the subscript.

FIELD-EFFECT TRANSISTORS

g_m – common source transfer conductance. Ratio of AC drain current to gate-to-source voltage in common source mode.

channel. A region of semiconductor material in which current flow is influenced by a transverse electrical field. A channel may physically be an inversion layer, a diffused layer, or bulk material. The type of channel is determined by the type of majority carriers during conduction; i.e., P-channel or N-channel.

depletion-mode operation. The operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value decreases the magnitude of the drain current.

depletion-type field-effect transistor. A field-effect transistor having appreciable channel conductivity for zero gate-source voltage; the channel conductivity may be increased or decreased according to the polarity of the applied gate-source voltage.

drain (D, d). A region into which majority carriers flow from the channel.

enhancement-mode operation. The operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value increases the magnitude of the drain current.

enhancement-type field-effect transistor. A field-effect transistor having substantially zero channel conductivity for zero gate-source voltage; the channel conductivity may be increased by the application of a gate-source voltage of appropriate polarity.

field-effect transistor. A transistor in which the conduction is due entirely to the flow of majority carriers through a conduction channel controlled by an electric field arising from a voltage applied between the gate and source terminals.

gate (G, g). The electrode associated with the region in which the electric field due to the control voltage is effective.

insulated-gate field-effect transistor. A field-effect transistor having one or more gate electrodes which are electrically insulated from the channel.

junction (junction-gate) field-effect transistor. A field-effect transistor that uses one or more gate regions that form P-N junction(s) with the channel.

metal-oxide-semiconductor (MOS) field-effect transistor. An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material.

N-channel field-effect transistor. A field-effect transistor that has an N-type conduction channel.

P-channel field-effect transistor. A field-effect transistor that has a P-type conduction channel.

source (S, s). A region from which majority carriers flow into the channel.

substrate (U, u) of a junction field-effect transistor or an insulated-gate field-effect transistor. A semiconductor material that contains a channel, a source, and a drain and which may be connected to a terminal.

substrate – of a thin-film field-effect transistor. An insulating material that supports the thin semiconductor layer, the insulating layer, and the source, gate, and drain electrodes.

tetrode field-effect transistor. A field-effect transistor having two independent gates, a source, and a drain. An active substrate terminated externally and independently of other elements is considered a gate for the purpose of this definition.

triode field-effect transistor. A field-effect transistor having a gate, a source, and a drain.

I_D – drain current, DC. The direct current into the drain terminal.

I_{DSS} – zero-gate-voltage drain current. The direct current into the drain terminal when the gate-source voltage is zero. This is an on-state current in a depletion-type device, an off-state current in an enhancement-type device.

I_G – gate current, DC. The direct current into the gate terminal.

I_{GSS} – reverse gate current, drain short-circuited to source. The direct current into the gate terminal of a junction-gate field-effect transistor when the gate terminal is reverse-biased with respect to the source terminal and the drain terminal is short-circuited to the source terminal.

I_S – source current, DC. The direct current into the source terminal.

VB_{GSS} – gate-source breakdown voltage. The breakdown voltage between the gate and source terminals with the drain terminal short-circuited to the source terminal. *Note:* The symbol VB_{GSS} is primarily used with junction-gate field-effect transistors. The symbols VB_{GSSR} or VB_{GSSF} should be used with insulated-gate transistors having shunting diodes or similar voltage-limiting devices.

VB_{GSSF} – forward gate-source breakdown voltage. The breakdown voltage between the gate and source terminals with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal. See V_{GSF}.

VB_{GSSR} – reverse gate-source breakdown voltage. The breakdown voltage between the gate and source terminals with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal. See V_{GSR}.

V_{DD}, V_{GG}, V_{SS} – DC supply voltage for drain, gate, source. The DC supply voltage applied to a circuit connected to the reference terminal.

V_{DG} – drain-gate voltage. The DC voltage between the drain and gate terminals.

V_{DS} – drain-source voltage. The DC voltage between the drain and source terminals.

I_Z – **zener current.** The value of DC reverse current that flows through the diode when it is biased to operate in its breakdown region and at a point on its voltage-current characteristic as follows:

I_Z: a specified operating point between I_{ZK} and I_{ZM}.
I_{ZK}: a specified point near the breakdown knee.
I_{ZM}: a specified point based on the maximum-rated power.

V_Z – **zener voltage.** The value of DC voltage across the diode when it is biased to operate in its breakdown region and at a specified point in its voltage-current characteristic as follows: V_Z: at I_Z.

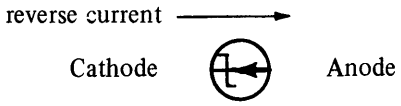
V_{GS} – **gate-source voltage.** The DC voltage between the gate and source terminals.

DIODES AND ZENER DIODES

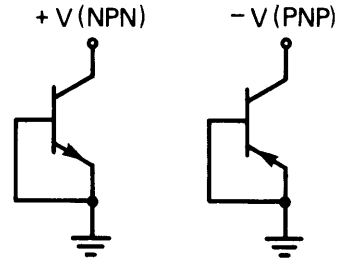
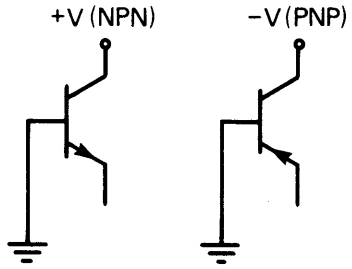
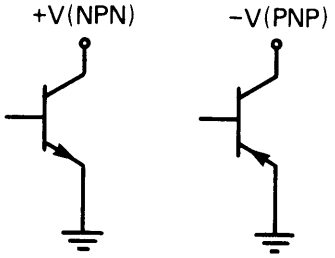
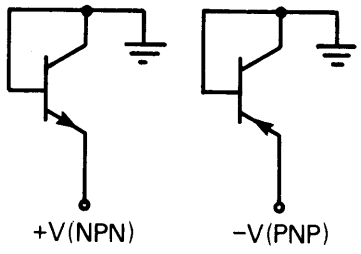
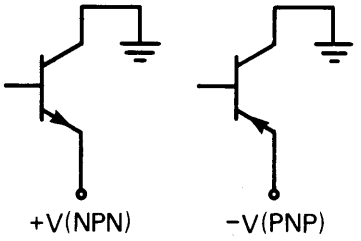
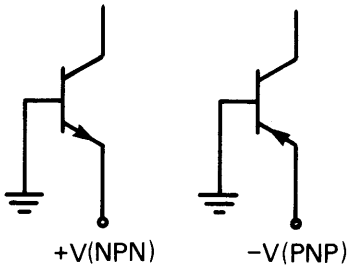
I_F – **forward current.** The respective value of current that flows through a semiconductor diode or rectifier diode in the forward direction.

I_R – **reverse current.** The respective value of current that flows through a semiconductor diode or rectifier diode in the reverse direction.

zener diode – voltage-reference diode. A diode which is normally biased to operate in the breakdown region of its voltage-current characteristic and which develops across its terminals a reference voltage of specified accuracy, when biased to operate throughout a specified current and temperature range. Graphic symbol for voltage-reference diode:



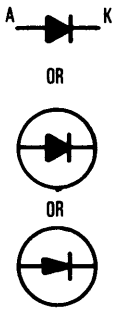
NOTES

TERM	DEFINITION	
BV_{CES}	Collector-emitter breakdown voltage at a specified current (I_{CES}) with the base shorted to emitter.	
I_{CES}	Collector-emitter current with the base shorted to emitter.	
BV_{CBO}	Collector-base breakdown voltage at a specified current (I_{CBO}) with the emitter open.	
I_{CBO}	Collector-base current with the emitter open.	
BV_{CEO}	Collector-emitter breakdown voltage at a specified current (I_{CEO}) with the base open.	
I_{CEO}	Collector-emitter current with the base open.	
BV_{ECS}	Reverse emitter-collector breakdown voltage at a specified current (I_{ECS}) with the base shorted to collector.	
I_{ECS}	Emitter-collector current with the base shorted to collector and reverse voltage.	
BV_{ECO}	Reverse emitter-collector breakdown voltage at a specified current (I_{ECO}) with the base open.	
I_{ECO}	Emitter-collector current with the base open and reverse voltage.	
BV_{EBO}	Reverse emitter-base breakdown voltage at a specified current (I_{EBO}) with the collector open.	
I_{EBO}	Emitter-base current with the collector open and reverse voltage.	

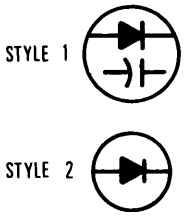
NOTES

Graphic Symbols for Semiconductor Devices

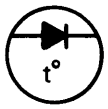
Semiconductor diode; semiconductor rectifier diode; metallic rectifier



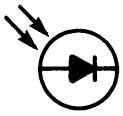
Capacitive diode (varactor)



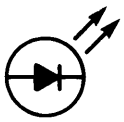
Temperature-dependent diode



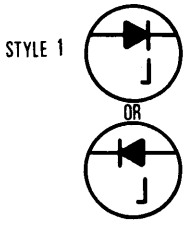
Photosensitive type



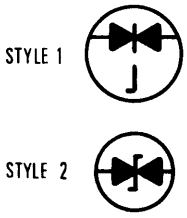
Photoemissive type



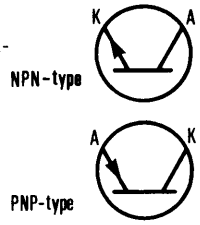
Unidirectional diode; voltage regulator



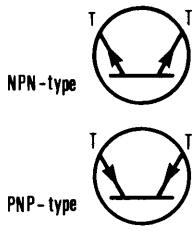
Bidirectional diode



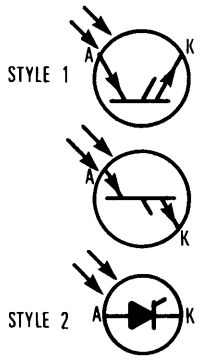
Unidirectional negative resistance breakdown diode; trigger diac



Bidirectional negative resistance breakdown diode; trigger diac

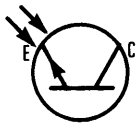


Light-activated type



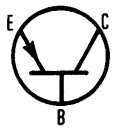
Thyristor, bidirectional diode type; bi-switch

Phototransistor (NPN-type) (without external base-region connection)

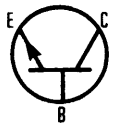


Current regulator

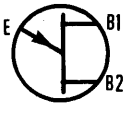
PNP transistor



NPN transistor

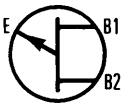


Unijunction transistor with N-type base



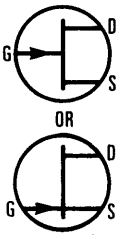
Graphic Symbols for Semiconductor Devices

Unijunction transistor with P-type base

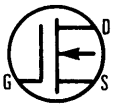


Field-effect transistor with N-channel

N-channel junction gate



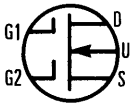
N-channel insulated-gate, depletion-type, single-gate, three-terminal device



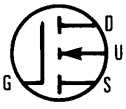
N-channel insulated-gate, depletion-type, single-gate, substrate internally terminated to source, three-terminal device

N-channel insulated-gate, depletion-type, single-gate, substrate externally terminated, four-terminal device

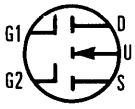
N-channel insulated-gate, depletion-type, two-gate, five-terminal device



N-channel insulated-gate, enhancement-type, single-gate, substrate externally terminated, four-terminal device

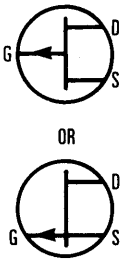


N-channel insulated-gate, enhancement-type, two-gate, five-terminal device

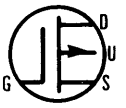


Field-effect transistor with P-channel

P-channel junction gate



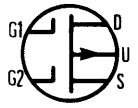
P-channel insulated-gate, depletion-type, single-gate, three-terminal device



P-channel insulated-gate, depletion-type, single-gate, substrate internally terminated to source, three-terminal device

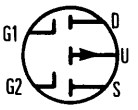
P-channel insulated-gate, depletion-type, single-gate, substrate externally terminated, four-terminal device

P-channel insulated-gate, depletion-type, two-gate, five-terminal device



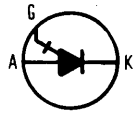
P-channel insulated-gate, enhancement type, single-gate, substrate externally terminated, four-terminal device

P-channel insulated-gate, enhancement-type, two-gate, five-terminal device



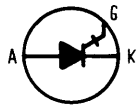
Thyristor, reverse-blocking triode-type, N-type gate; semiconductor controlled rectifier, N-type gate

Gate turn-off type

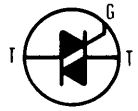


Thyristor, reverse-blocking triode-type, P-type gate; semiconductor controlled rectifier, P-type gate

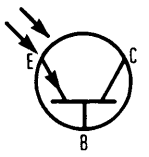
Gate turn-off type



Thyristor, bidirectional triode-type; triac; gated switch



Phototransistor (NPN-type)



f_T EXPLANATION

f_T is one method used to measure and define the high-frequency characteristics of a transistor. Each individual transistor has a low-frequency current gain. This current gain is constant from DC up to some frequency determined by the transistor characteristics. This is the transistor cut-off frequency (f_c) and is defined as the frequency at which the current gain is reduced 3 dB (.707 times the low-frequency current gain). At frequencies greater than the cut-off frequency, the current gain decreases at a rate of 6 dB per octave. (The current gain is divided by 2 each time the frequency is doubled). This is illustrated in Fig. 15 for transistor A at frequencies greater than 1 MHz where the slope is negative. The highest frequency at which the transistor can actually provide current gain is the frequency at which the current gain has decreased to a value of one. Therefore, let us call this frequency f_T, according to the following definition:

DEFINITION OF f_T

f_T is the frequency at which the current gain of the transistor is equal to one, with the transistor in the common emitter mode and the collector shorted (AC) to the emitter.

The above description of current gain versus frequency characteristics of a transistor can be represented by the following mathematical equation:

$$\beta = \frac{\beta o}{1 + j\frac{f}{fc}} = \frac{\beta o}{-\sqrt{1 + \frac{f^2}{f_c^2}}}$$

β = current gain
βo = low frequency current gain.
f = frequency
f_c = cut-off frequency

Therefore, at frequencies much less than cut-off frequency:

$$\beta = \frac{\beta o}{1} = \beta o$$

At frequencies much greater than the cut-off frequency:

$$\beta = \frac{\beta o}{\frac{f}{fc}} = \frac{\beta o \times fc}{f}$$

$$\beta \times f = \beta o \times fc$$

Let $\beta = 1$, where f_T is defined

$$1 \times f = \beta o \times fc = f_T$$

Thus, from definition, f_T is the frequency at which current gain is one, or unity, and the above equation shows that f_T is equal to the product of the low frequency current gain times the cut-off frequency.

Fig. 15 shows three examples of transistor current gain versus frequency characteristics. It is interesting to observe that the low frequency current gain of transistor B is less than that of transistor A, but transistor A has a lower cut-off frequency than transistor B; therefore, the f_T of both transistors can be the same although the cut-off frequencies of the transistors are different.

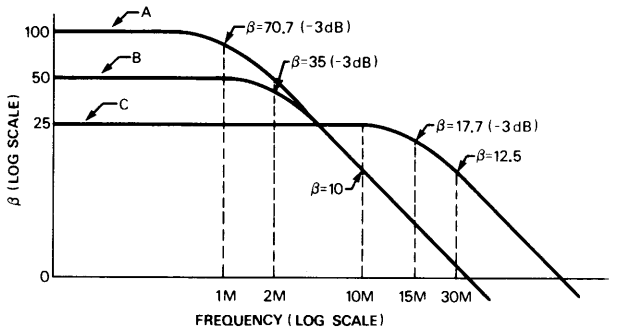


Fig. 15. β versus frequency for transistors A, B and C.

Transistor A $f_T = \beta o \times fc = 100 \times 1$ MHz $= 100$ MHz

Transistor B $f_T = \beta o \times fc = 50 \times 2$ MHz $= 100$ MHz

Another example is transistor C which has a low-frequency current gain that is less than the other two transistors, but, because of its high cut-off frequency, its f_T is greater than that of the other two transistors.

Transistor C $f_T = \beta o \times fc = 25 \times 15$ MHz $= 375$ MHz

Taken from a previous equation, when the frequency is much greater than the cut-off frequency:

$$f_T = \beta \times f = \beta o \times fc \text{ when } f \gg fc$$

Thus, a practical method for measuring f_T is to measure the current gain at a frequency greater than the cut-off frequency, and then multiply current gain times frequency. This method is used in the Model 530 for three different test frequencies as follows:

Scale = 0 - 100 MHz:

Test frequency = 1 MHz.

1 MHz is used for low-frequency transistors and the current gain is measured up to 100 which provides a maximum f_T of 100 MHz.

f_T max. = 100 x 1 MHz = 100 MHz

Scale = 0 - 500 MHz:

Test frequency = 10 MHz.

10 MHz is used for medium-frequency transistors and the current gain is measured up to 50 which provides a maximum f_T of 500 MHz.

f_T max. = 50 x 10 MHz = 500 MHz

Scale = 0 - 1500 MHz

Test frequency = 30 MHz.

30 MHz is used for higher-frequency transistors and the current gain is measured up to 50 which provides a maximum f_T of 1500 MHz.

f_T max. = 50 x 30 MHz = 1500 MHz

For practical reasons, there are minimum meter deflections that must be met for each scale in order to provide an accurate f_T measurement. These minimum meter deflections are as follows:

SCALE	MINIMUM
0 - 100 MHz	5 MHz
0 - 500 MHz	50 HMz
0 - 1500 MHz	300 MHz

If the minimum meter deflection cannot be obtained, change to the next lower scale.

As an example, the three transistors in Fig. 15 would display the following reading on each scale:

Transistor	0 - 100	0 - 500	0 - 1500	f_T
A	71	100	100 (no good)	100
B	50	100	100 (no good)	100
C	25	250	375	375

Thus, the most accurate value for f_T is the largest absolute value obtained from any scale provided that the minimum meter deflection values are exceeded on the scale giving the greatest f_T value.

Since the collector bias current is one of the most important variables for determining f_T, the Model 530 provides an automatic bias of 10 ma for collector current, because many signal transistors provide the highest f_T at this current. An example of f_T versus collector current and bias voltage is shown in Fig. 16. V_{CE} is usually between 5 volts and 10 volts for most f_T measurements. The Model 530 provides a nominal 8 volts V_{CE} for measuring f_T. Therefore, the measured value of f_T is valid at these parameter values within the accuracy stated in the specifications.

It should be remembered that there are many variables involved in measuring f_T and that changes in the test parameters can change the f_T reading. The fact that the f_T reading accuracy applies only at the specified test parameters does not mean that the test cannot be used to evaluate devices to be used under other operating conditions. Reference to Fig. 16 shows that by use of the curve family information shown, the performance at other operating conditions can be predicted. Even without this information, the relative high-frequency performance of transistors can be determined.

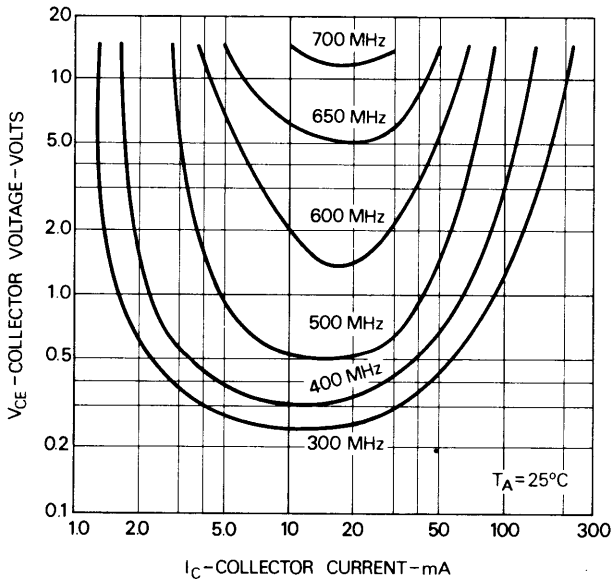


Fig. 16. Constant f_T curves for collector-emitter voltage vs. collector current (bipolar transistors).

WARRANTY SERVICE INSTRUCTIONS

1. Refer to the MAINTENANCE section of your B & K-Precision instruction manual for adjustments that may be applicable.

2. Defective parts removed from units which are within the One Year Limited Warranty period should be sent PREPAID to the Service Department listed below. Be sure to state the model and serial number of the unit from which the parts were removed and date the unit was purchased. These parts will be exchanged at no charge, under the terms of the Warranty.

3. If the above-mentioned procedures do not correct the problem you are experiencing with your unit, pack it securely (preferably in the original carton or double-packed). Enclose a letter describing the problem and include your name and address. Deliver to, or ship PREPAID (UPS preferred) to the nearest B & K-Precision authorized service agency (see list enclosed with unit).

If your list of authorized B & K-Precision service agencies has been misplaced, contact your local distributor for the name of your nearest service agency, or write to:

Service Department

B & K-Precision Product Group
DYNASCAN CORPORATION
2815 West Irving Park Road
Chicago, Illinois 60618

LIMITED ONE-YEAR WARRANTY

DYNASCAN CORPORATION warrants to the original purchaser that its B & K-PRECISION product, and the component parts thereof, will be free from defects in workmanship and materials for a period of one year from the date of purchase.

DYNASCAN will, without charge, repair or replace, at its option, defective product or component parts upon delivery to an authorized B & K-PRECISION service contractor or the factory service department, accompanied by proof of the date of purchase in the form of a sales receipt.

To obtain warranty coverage, this product must be registered by completing and mailing the enclosed warranty registration card to DYNASCAN, B & K-PRECISION, P.O. Box 35080, Chicago, Illinois 60635 within five (5 days) from the date of purchase.

Exclusions: This warranty does not apply in the event of misuse or abuse of the product or as a result of unauthorized alterations or repairs. It is void if the serial number is altered, defaced or removed.

DYNASCAN shall not be liable for any consequential damages, including without limitation damages resulting from loss of use. Some states do not allow limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

This warranty gives you specific rights and you may also have other rights which vary from state to state.

For your convenience we suggest you contact your B & K-PRECISION distributor, who may be authorized to make repairs or can refer you to the nearest service contractor. If warranty service cannot be obtained locally, please send the unit to B & K-PRECISION Service, 2815 West Irving Park Road, Chicago, Illinois 60618, properly packaged to avoid damage in shipment.

B+K PRECISION

DYNASCAN CORPORATION
6460 W. Cortland Street
Chicago, Illinois 60635

480-206-9-001

B & K-PRECISION MODEL 530 PARTS LIST

488-195-9-003

SCHEMATIC SYMBOL	DESCRIPTION	B & K PART NO.
	RESISTORS & CONTROLS	
R85	9.1KΩ, ±2%, ¼W, Deposited Carbon	002-039-9-001
R79	13KΩ, ±2%, ¼W, Deposited Carbon	002-040-9-001
R83, 81	18KΩ, ±2%, ¼W, Deposited Carbon	002-041-9-001
R121	100KΩ, ±20%, ¼W, Horizontal Mount Linear Trimpot	008-216-9-001
R101, 55	50KΩ, ±20%, ¼W, Horizontal Mount Linear Trimpot	008-224-9-001
R22, 87	10KΩ, ±20%, ¼W, Horizontal Mount Linear Trimpot	008-241-9-001
R72	30KΩ, ±10%, ½W, Linear Carbon Pot	008-301-9-001
R92, 106	500KΩ, ±20%, ¼W, Horizontal Mount Linear Trimpot	008-286-9-001
R56, 59	2KΩ, ±20%, ¼W, Horizontal Mount Linear Trimpot	008-287-9-001
R103, 58	1KΩ, ±20%, ¼W, Horizontal Mount Linear Trimpot	008-289-9-001
	CAPACITORS	
C44	10μf @ 250VDC Electrolytic	021-040-9-001
C42	100μf @ 10VDC Electrolytic	022-050-9-001
C38, 39, 40, 41	1000μf @ 25VDC Electrolytic	022-084-9-001
C20, 25	47μf @ 6.3VDC Tantalum	027-013-9-001
C56, 57, 47, 50, 49	.01μf @ 250VDC Polyester	025-027-9-001
C56, 46	.047μf @ 250V Polyester	025-096-9-001
C43	.1μf @ 100V Polyester	025-120-9-001
	COILS	
L1	Oscillator, 1 MHz	044-035-9-001
L2	Oscillator, 10 MHz	044-036-9-001
L3	Oscillator, 30 MHz	044-038-9-001

COMPOSITE
499-114-9-001

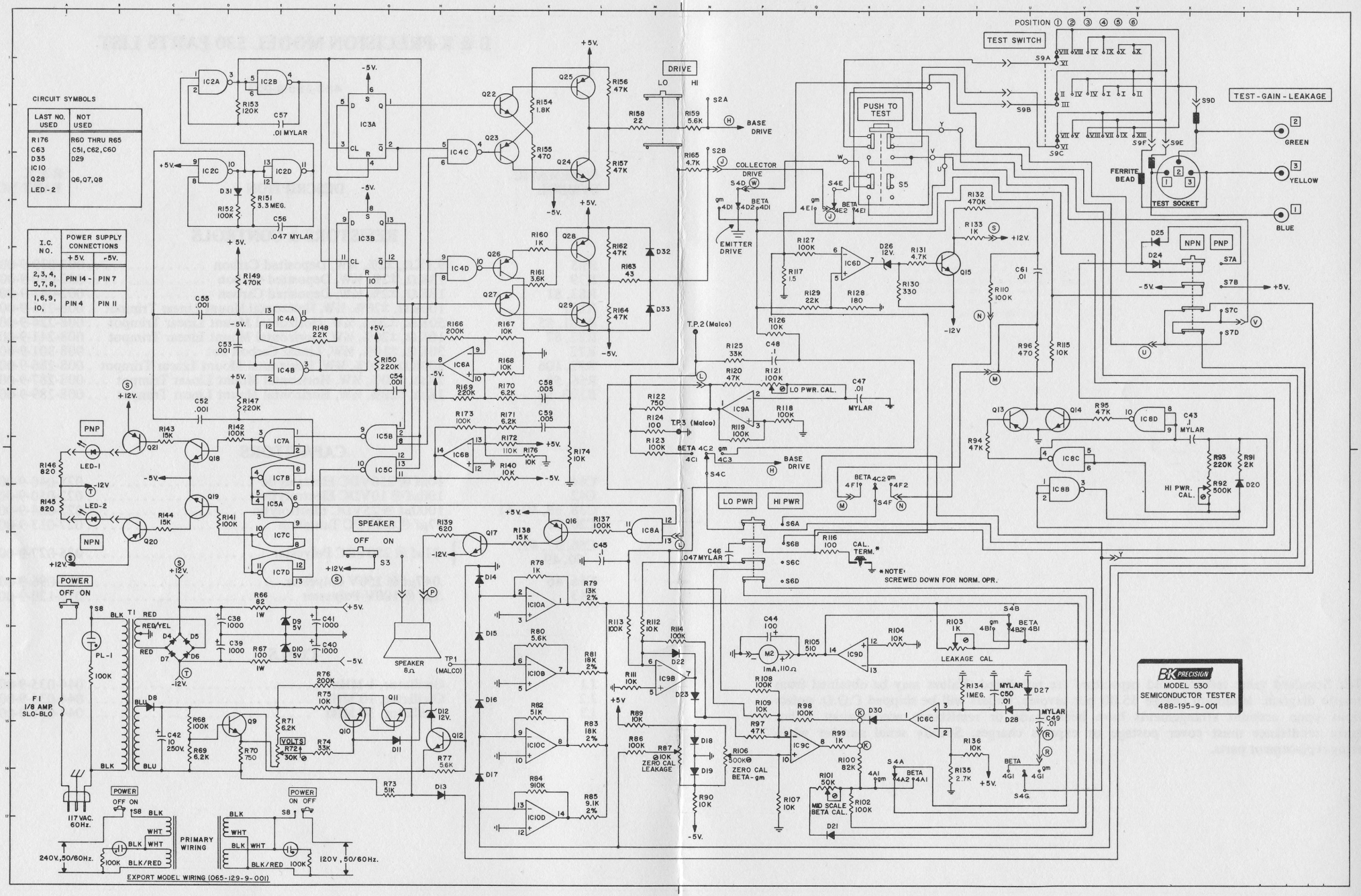
MODEL 530 PARTS LIST

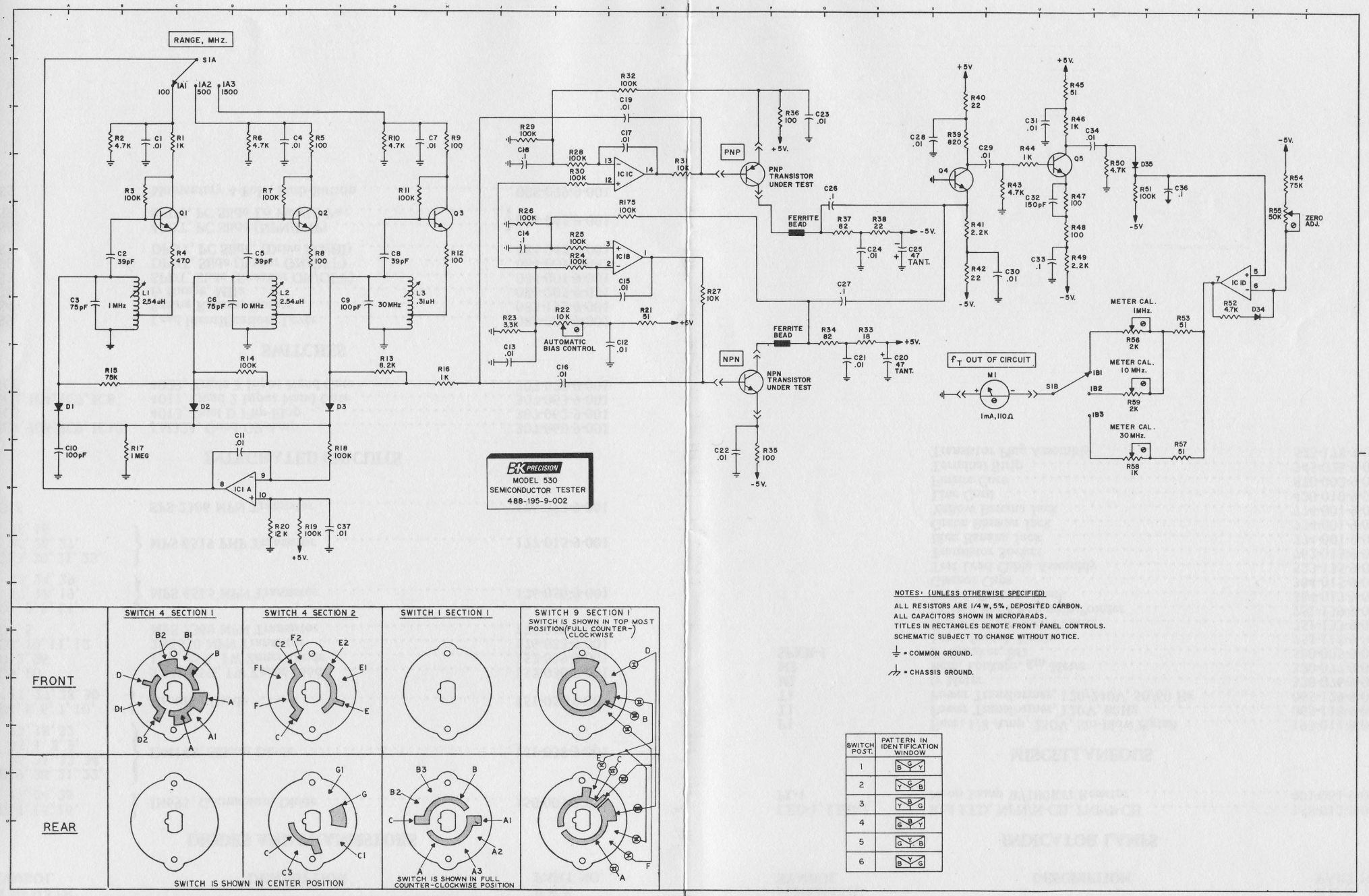
SCHEMATIC SYMBOL	DESCRIPTION	B & K PART NO.
	DIODES AND TRANSISTORS	
D14, 15, 16, 17, 24, 25	IN695, Germanium Diode	150-007-9-001
D19, 20, 21, 22, 23, 31, 33, 34, 35, 1, 2, 3, 13, 18, 32	IN4148, Silicon Diode	151-038-9-001
D4, 5, 6, 7, 10, 11, 27, 28, 30	Rectifier Diode	151-050-9-001
D9, 10	5.1V, ±5%, 1W Zener Diode	152-030-9-001
D12, 26	12V, ±5%, 1W Zener Diode	152-039-9-001
Q9, 10, 11, 12	2N5550 NPN Transistor	176-033-9-001
Q4, 5	MPS 2369 NPN Transistor	176-049-9-001
Q1, 2, 3, 14, 17, 18, 19, 22, 24, 29	MPS 6515 NPN Transistor	176-050-9-001
Q13, 20, 21, 23, 25, 26, 27, 28, 16	MPS 6519 PNP Transistor	177-015-9-001
Q15	SPS-2306 NPN Transistor	176-023-9-001
	INTEGRATED CIRCUITS	
IC1, IC6, IC9, IC10	LM324, Quad OP-Amp	307-060-9-001
IC3	4013, Dual D Flip-Flop	307-062-9-001
IC2, IC4, IC7, IC8	4011, Quad 2 Input Nand Gate	307-063-9-001
IC5	4023, Triple 3 Input Nand Gate	307-070-9-001
	SWITCHES	
S9	Lead Identification, Lever	080-002-9-001
S4	Spring Return, Rotary	083-195-9-001
S1	f_T Range, MHz	083-205-9-001
S3	SPDT, Slide (Speaker ON/OFF)	084-001-9-001
S8	DPDT, Slide (Power ON/OFF)	084-001-9-003
S2	DPDT, PC Slide, (Drive LO/HI)	084-043-9-001
S6	4PDT, PC Slide (NPN/PNP)	084-045-9-001
S7	4PDT, PC Slide Lo Pwr/Hi Pwr	
S5	Momentary 4-Pole, Push-Button	088-029-9-001

MODEL 530 PARTS LIST

SCHEMATIC SYMBOL	DESCRIPTION	B & K PART NO.
	INDICATOR LAMPS	
LED-1, LED-2	Red LED, NPN/N-CH, PNP/P-CH	158-012-9-001
PL-1	Neon Lamp W/100KΩ Resistor	401-061-9-002
	MISCELLANEOUS	
F1	Fuse, 1/8 Amp, 250V, Slo-Blow Pigtail	193-011-9-001
T1	Power Transformer, 120V, 60Hz	065-118-9-001
T1	Power Transformer, 120/240V, 50/60 Hz	065-129-9-001
M1	f_T Meter	320-076-9-001
M2	Beta, Leakage, g_m Meter	320-077-9-001
SPKR-1	2" Speaker, 8Ω	580-005-9-001
	Lever Switch Knob	751-118-9-001
	Skirted Knob with Pointer	751-133-9-001
	Skirted Bar Knob with Pointer	751-139-9-001
	Switch Button, Black	384-013-9-001
	Glamor Caps	384-015-9-001
	Test Lead Cable Assembly	523-135-9-001
	Transistor Socket	762-015-9-001
	Blue Banana Jack	774-001-9-003
	Green Banana Jack	774-001-9-004
	Yellow Banana Jack	774-001-9-006
	Line Cord	420-010-9-001
	Ferrite Core	870-002-9-001
	Terminal Strip	345-026-9-001
	Transistor Plug Assembly	523-178-9-001

NOTE: Standard value resistors and capacitors are not listed. Values may be obtained from schematic diagram. Minimum charge $5.00 per invoice. Orders will be shipped C.O.D. unless previous open account arrangements have been made or remittance accompanies order. Advance remittance must cover postage or express charges. Specify serial number when ordering replacement parts.


CIRCUIT SYMBOLS
LAST NO. USED
NOT USED
R176
R60 THRU R65
C63
C51, C62, C60
D35
D29
IC10
Q28
Q6, Q7, Q8
LED-2
I.C. NO.
POWER SUPPLY CONNECTIONS
+5V.
-5V.
2, 3, 4, 5, 7, 8,
PIN 14 -
PIN 7
1, 6, 9, 10,
PIN 4
PIN 11
DRIVE
LO
HI
BASE DRIVE
COLLECTOR DRIVE
EMITTER DRIVE
PUSH TO TEST
TEST SWITCH
POSITION
TEST - GAIN - LEAKAGE
GREEN
YELLOW
BLUE
FERRITE BEAD
TEST SOCKET
NPN
PNP
LO PWR
HI PWR
LO PWR. CAL.
HI PWR. CAL.
LEAKAGE CAL
MID SCALE BETA CAL.
ZERO CAL LEAKAGE
ZERO CAL BETA-gm
CAL. TERM.*
*NOTE: SCREWED DOWN FOR NORM. OPR.
SPEAKER
OFF ON
SPEAKER 8Ω
TP1 (MALCO)
T.P.2 (Malco)
T.P.3 (Malco)
LED-1
LED-2
PL-1
POWER
OFF ON
F1 1/8 AMP SLO-BLO
117 VAC. 60Hz.
PRIMARY WIRING
240V., 50/60Hz.
120V., 50/60Hz.
EXPORT MODEL WIRING (065-129-9-001)
BK PRECISION
MODEL 530
SEMICONDUCTOR TESTER
488-195-9-001



B&K PRECISION
MODEL 530
SEMICONDUCTOR TESTER
488-195-9-002

NOTES: (UNLESS OTHERWISE SPECIFIED)

ALL RESISTORS ARE 1/4 W, 5%, DEPOSITED CARBON.
ALL CAPACITORS SHOWN IN MICROFARADS.
TITLES IN RECTANGLES DENOTE FRONT PANEL CONTROLS.
SCHEMATIC SUBJECT TO CHANGE WITHOUT NOTICE.

⏚ = COMMON GROUND.

⏚ = CHASSIS GROUND.

SWITCH POST.	PATTERN IN IDENTIFICATION WINDOW
1	B G Y
2	Y G B
3	Y B G
4	G B Y
5	G Y B
6	B Y G