The LHC DS22 bit ADC

The LHC high precision current measurement chain

The main power converters in LHC require an unprecedented level of accuracy in the control of current to the superconducting magnets, in the order of ~10^{-6}.

The power converter output current accuracy is mainly determined by the **DCCT** (Direct Current Current Transducer) and **ADC** (Analogue-Digital Converter) employed.

There are three types of ADCs used in the LHC: a 16 bit Delta Sigma and a 16 bit SAR, both included in the power converters' digital controller electronics (FGC) and, in the case of the main and inner triplet power converters, a 22 bit delta sigma standalone unit.

Introduction to Delta sigma converters

The ADC employed in the digital regulation loops for the LHC requires high resolution and accurate digitization of low frequency waveforms. Since the ADC can be one of the major sources of error in the magnet current, along with the current transducer, its performance largely determines the overall accuracy which can be obtained. The potential of the Delta-Sigma method to deliver ppm performance determined the choice of this method for the LHC.
The simplified block diagram of a first order Delta sigma ADC is shown in Fig.1.

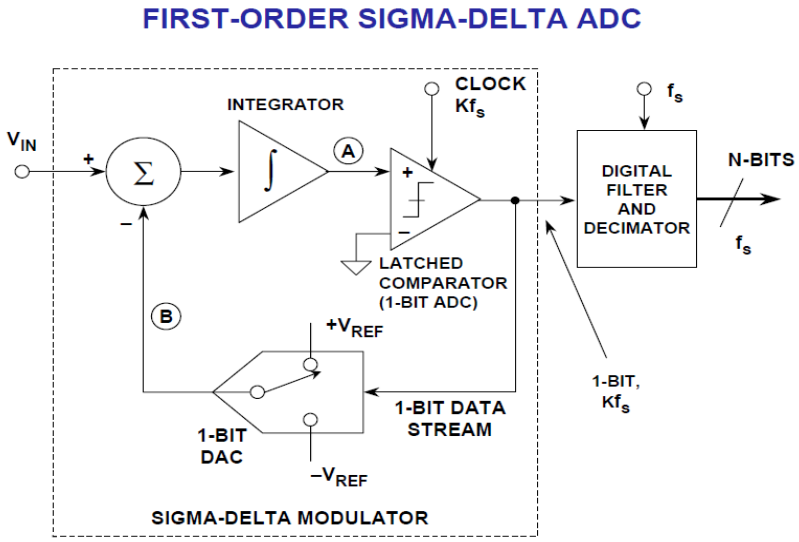

Fig. 1 – Block diagram of a first order Delta Sigma

If we assume a DC input at VIN, we can see that the integrator will ramp up or down depending on the input voltage. The output of a latched comparator is fed back through a 1-bit DAC to the summing input. The negative feedback loop will force the average DC voltage at node B to as equal as possible equal to VIN. This implies that the average DAC output voltage (density of “ones” in the one bit data stream from the comparator output) must equal to the input voltage VIN. As the input signal increases the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. This very simplistic analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator processes the serial bit stream to extract the average value and produce the final output data.

For a more complete explanation, understanding the concepts of oversampling, noise shaping and decimation becomes essential. However this isn’t within the scope of this document. Please look here for a better description of the Delta Sigma principle.

The CERN 22 bit Delta sigma converter

The CERN 22 bit Delta Sigma converter is composed of two main elements combined into 1 single module:

- The power supply card (DS PS)
- The modulator card (DS MOD)

Fig. 2 – DS22 module

Fig. 3 – DS22 modulator card

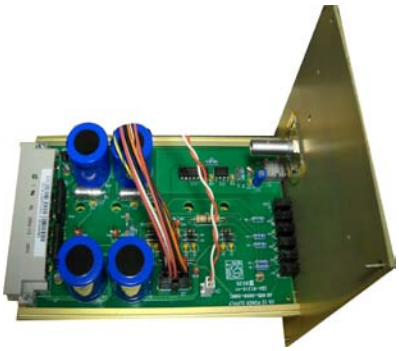

Fig. 4 – DS22 power supply card

The CERN 22 bit Delta Sigma are used in the main dipole, main quadrupole and inner triplet power converters. They are installed outside the power converter, in special temperature controlled EMC racks. Their use in the machine is described below.

Machine installation

LHC calibration clusters	80 DS22 ADCs installed in 16 calibration clusters
Radiation Safe Locations (68)	UA23 (10), UA27 (10), UA43 (6), UA47 (6), UA63 (6), UA67 (6), UA83 (10), UA87 (10), USC55 (4)
Radiation Exposed Locations (12)	UJ14 (4), UJ16 (4), UJ56 (4)

Architecture

The basic structure chosen for the CERN 22bit DS ADC is shown in Fig. 2. A third order integrator is used. The circuit is fully implemented using discrete components. One CPLD is used for clock division but apart from that only basic logic blocks and analog components are used. The output bit stream is transmitted by optical fibre to the power converter's digital controller where the digital filter is implemented.

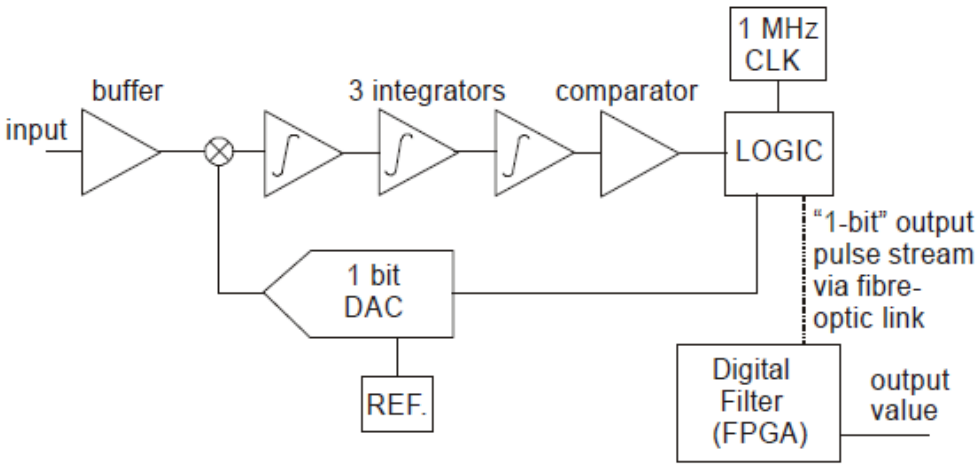

Fig. 5 - CERN DS22 bit architecture

The Hardware - the power supply (Fig. 4)

The power supplies to the SD card are very conventional and employ standard IC regulators, where the +5V is derived from the +15V supply. This ensures correct start-up [anti-latchup] for the CMOS ICs. Test points and LEDs are provided but the circuit merits no further description. The 'mains' transformer however is a special low field design, with twin electrostatic screens.

Since the output of the Delta Sigma is sent via fibre optics to the digital controller of the converter, a fibre-optic driver, which consumes ~50mA, is mounted on this card to avoid having this dissipation inside the modulator temperature-controlled guard box.

The Hardware - the modulator (Fig. 3)

The whole of the modulator circuit is floating with respect to ground and is contained within a temperature-controlled guard box. This method assures a common-mode rejection ratio of greater than 150dB at 50Hz. To provide adequate EMI suppression, a capacitive coupling network is placed between the input cable screen and ground, followed by two isolating hf chokes at the single-ended buffer input.

The schematic is shown in Fig. 6 and the different functional blocks are identified. A complete analysis of each block is not in the scope of this document but a short description is presented below.

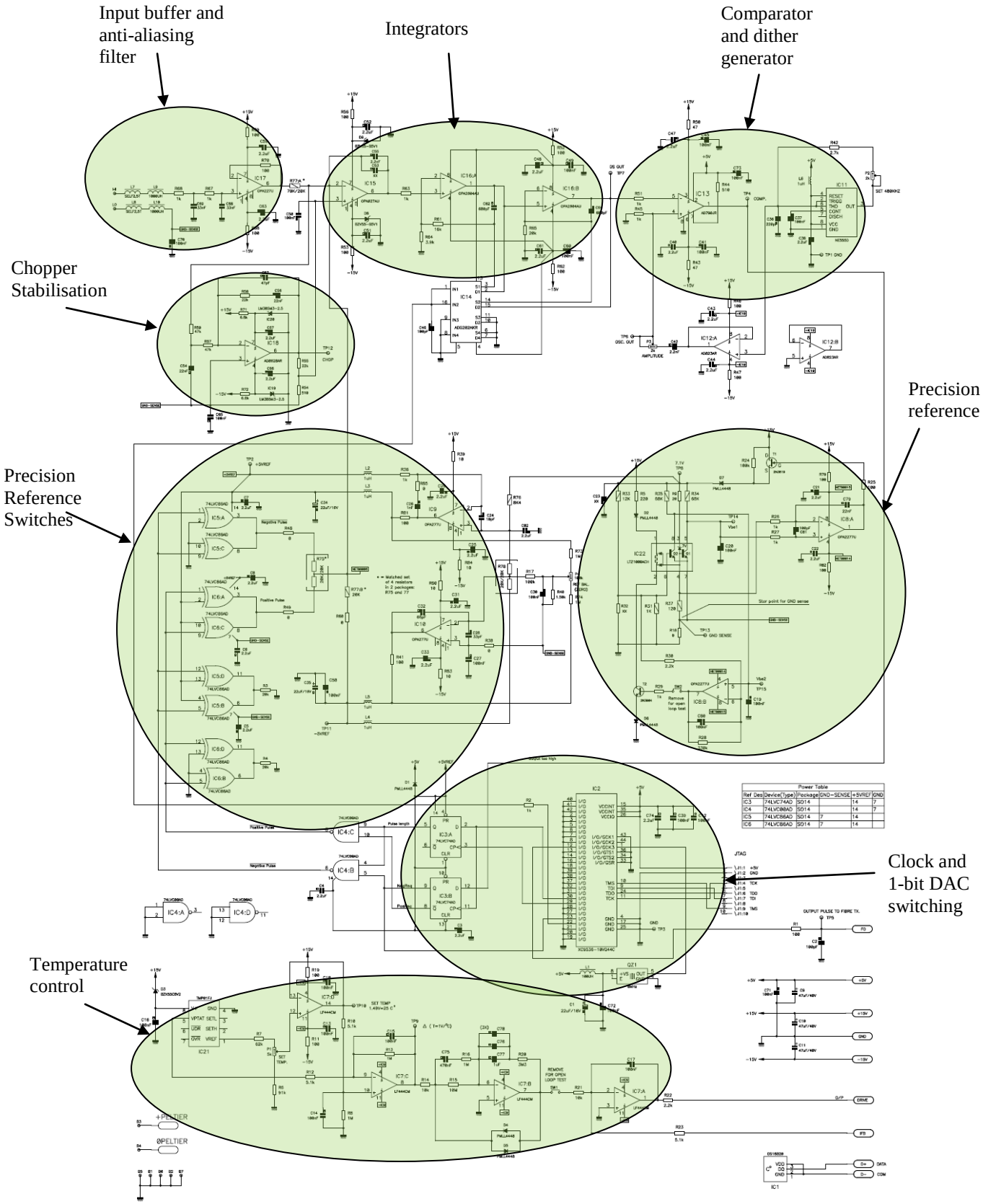

Fig. 6 Schematic of CERN DS22 bit ADC

Input Buffer and Anti-Alias Filter
High input impedance buffer amplifier preceded by a two-pole anti-alias filter.

Integrators
The 1st summing integrator combines the input signal with the output from the 1bit precision DAC.
The 2nd and 3rd integrator stages are configured as non-inverting integrators.

Comparator and Dither Generator
The output of the 3rd integrator drives the comparator, the output of which is clocked into the precision switches control circuit.
A triangular 960kHz "dither" signal is injected into the + ve input terminal of the comparator for "idle-tone" suppression. Note - An 'idle-tone' is a part of the modulator output noise occurring at a particular frequency, which falls within the required pass-band.

Precision References
The basic precision-voltage-reference design is a modified "Spreadbury" circuit with internal temperature stabilisation

Clock Source, Logic and 1bit DAC Switching
The basic clock source is derived from a 8MHz Xtal controlled oscillator and has heavy supply-line decoupling to minimise clock "pulling" and phase jitter. The 8MHz clock feeds a CPLD which is programmed to divide this input to provide the 500kHz clock for the switch control. At the same time a 125nsec 'guard pulse' is generated to clamp the 1bit DAC output to zero during basic clock transitions, and also ensuring precisely equal switching surfaces in the 1bit DAC output irrespective of pulse sequencing.

Precision Switches
The information from the latched comparator signal is combined with the 125nsec 'guard pulse' to drive the precision switches, connecting either the positive or the negative 5V reference to the 1st integrator.
Great care was taken to design a minimal overall delay for each switch circuit with very symmetrical and short rise and fall times.

Temperature Control
The temperature control circuit uses a Peltier element to stabilise the aluminium block containing the precision reference voltage and which is thermally connected to the critical switching components. The block also contains a temperature sensor which must be tightly coupled thermally to this block. The overall control of block temperature gives fast slewing to temperature and a final stability well within 1/100th of a degC.