CERN — Organisation Européenne pour la Recherche Nucléaire — European Organization for Nuclear Research

TE Technology Department

Design Office

FIQ51-1

TE/MPE/EM Electronic Modules

PCB Fabrication Specification

Designation

Number	**EDA-03803-V2**		
Title	**AD7177-2 Daughterboard**	*Date:*	13-Sep-2018
Customer	N. Beev		
Contact	electronics-design-office@cern.ch	*Etude/Design:*	C. Lesguillier

Mechanical Description

External Size (mm):	90.0mm x 50.0mm			Thickness [mm]:	1.6
PCB type :	Multilayers	4	Layers	Panel:	YES *

Finished Copper Thicknesses Requirements

External Layers [µm]:	35µ	Internal Layers - Planes [µm]:	35µ
Holes Walls [µm]:	25µ	Internal Layers - Signals [µm]:	35µ

Board Finish Requirements

Silkscreen On Top:	YES	Silkscreen On Bottom:	YES
Silkscreen Colour:	White		
Soldermask On Top:	YES	Soldermask On Bottom:	YES
Soldermask Colour:	Green		
Surface Finish:	ENIG - Electroless Nickel/Immersion Gold according to **IPC-4552**		
Thicknesses:	**Ni: 3µm min - 6µm max / Au: 0.05µm min - 0.125µm max**		

Additional Information

Minimun Track Width:	0.127mm	Minimum Track/Pad Clearance:	0.15mm
Minimum Hole Diameter:	0.3mm	Wedge Aluminium Wire Bonding:	NO
Buried Holes:	NO	Blind Holes:	NO
		Filled and Capped Vias:	NO
Press-Fit Through Holes:	NO	Card Edge Connector:	NO
Specified Stackup:	NO	Controlled Impedance:	NO
Electrical Test:	YES	Test Coupons Required:	YES

* = See http://edms.cern.ch/nav/EDA-03803-V2-0 -> Manufacturing -> EDA-03803-V2_mfg.pdf

Laminate And Copper Foils Requirements

Base material, when used, shall be flame retardant rated **UL 94V-0** laminate glass fiber epoxy and conform to L94 according to **IPC-4101/128** , halogen-free. Copper shall be **type H** with pits and dent, **class B**. When procuring base material the following are required: minimum **TG 150°C**, minimum **TD(5%) 350°C**, minimum **T-288 35min**, maximum Z-axis thermal expansion coefficient above **TG 280PPM/°C** (alternatively Z-axis thermal expansion coefficient between 50-260°C of **3.5%** maximum is acceptable).

Prepreg material shall conform to P94 according to **IPC-4101/128**, halogen-free and be subjected to the same requirement set forth for the laminate base material.

All internal layer copper foils shall conform to **IPC-4562/3 CU-E3, class 2**

Additional Plating Requirements

Finished external layers and plated through holes plating shall be **25µm**.
The copper plating shall be performed with plating chemistries/processes commensurate with the maximum aspect ratio plated hole in the board. The aspect ratio is defined as the ratio of the board thickness divided by the smallest drilled hole diameter on the board.

The quality of the copper plating shall be verified according to **IPC-TM-650**, **2.4.18.1** as to tensile strength and according to **IPC-TM-650**, **2.4.2.1** as to ductility.

Thieving may be added outside the circuit board border to compensate for high density areas on the board. For thieving within the borders of the circuit board approval is required.

Vias/Through Holes Requirements

Non functional lands shall not be removed on layers 1, 2, 3, N-2, N-1 and N. Other non functional lands may be removed as long as no removal on adjacent layers occurs.

Negative etchback is not allowed. Positive etchback is permissible to 0.2mils maximum.

All holes are located on the basic modular grid system. All holes shall be located within a 3-mils-diameter of true position. Drilling should be according to **IPC-DR-572**.

Via holes are specified as to drilled hole size ; for these holes the finished hole size is for reference only. Holes receiving component leads or pins are specified as to finished hole size; for these holes the drilled hole size is for reference only.

Additional Board Finish Requirements

Solder mask over bare copper according to **IPC-SM-840**, class H. All fiducials, lands and holes, except vias, shall be free of solder mask material.

Silkscreen shall be with permanent, organic, non-conductive and RoHS compliant ink. Silkscreen ink must be capable to withstand peak temperatures of 260-270°C for a duration of 60 seconds and at least 3-4 cycles without discoloration.

An identification marking shall be applied on the PCB. It shall contain the PCB manufacturer logo, UL marking, date-code and surface finish according to **J-STD-609**. Marking shall be applied on silkscreen and located in the indicated area near the TE/MPE logo.

Additional Quality Control Requirements

The printed wiring board, and test coupon when used in lieu of a production board, shall be according to **IPC-2221 and IPC-2222, type 3, class2**. Date code and PCB manufacturer logo shall be present on test coupons for traceability.

Acceptance of finished printed boards shall be in accordance with **IPC-A-600, class 3**.

Fabrication and inspection shall be according to **IPC-6011 and IPC-6012, class 3**.

The maximum allowable bow and twist shall be **0.75%**.

All quality controls shall be performed per **IPC-TM-650** procedures and per **IPC-4552**.

Packing Requirements

Boards shall be wrapped in sulfur-free neutral PH wrapping paper and shipped in vacuum-sealed anti-static bags.

A humidity indicator and desiccant may be inserted in the bags.

Quality Documentation To Be Delivered

A certificate of conformity shall be delivered with the PCB's. It shall declare all material used (laminate exact type, soldermask, silkscreen, etc) and their respective lot numbers.