Analog-to-digital conversion beyond 20 bits

Architectures, applications, state of the art, technical limits, and future prospects

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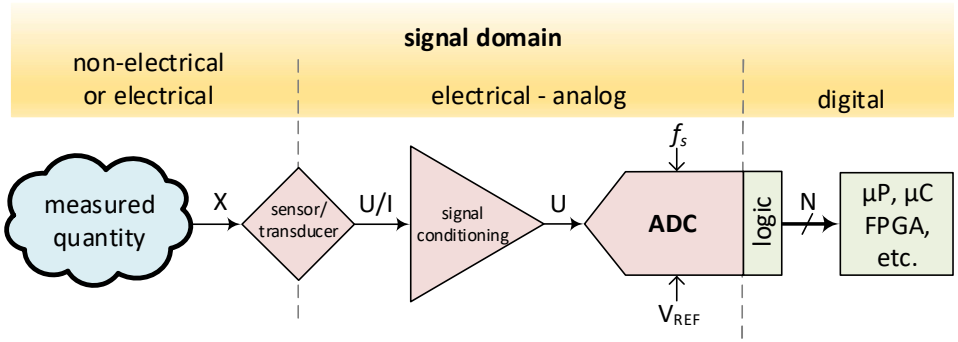
Presentation Outline

1. The need for high resolution
2. Applications overview
3. SNR and equivalent resolution metrics
4. High-resolution ADC architectures
5. State of the art
6. Technical limitations
7. Future prospects

The Need for High Resolution



- Some natural or artificial signals have very high **intrinsic dynamic range**
  Examples: magnetic fields, light intensity, seismic signals
- Measurement systems often use workarounds: sub-ranging, compensation, non-linear conversion, etc. **Sometimes these are not practical or possible.**
- Analog signal processing stages are limited by noise, voltage rails, and bandwidth. In terms of system resources, they are “expensive”.
- DSP is “cheap” and much more flexible, but needs an interface to the outside world.
- In this work, “high resolution” means ≥20 bits. The focus is on integrated ADCs.

High-Resolution ADC Applications

Application field	Signal bandwidth	Main requirements	Notes
Audio	20 Hz – 20 kHz	low distortion low noise	Sigma-Delta ADCs, integrated codecs (ADC/DAC) with poor or missing DC specifications
Industrial instrumentation	near-DC	EMI robustness resolution provisions for signal conditioning stability	Highly integrated devices with flexible analog and digital capabilities
Seismology / geophysical surveying	near-DC to 10^2-10^3 Hz	high dynamic range low distortion	A few commercial ADCs (ADS1281, MAX11214), many hybrid and research systems
Voltage metrology	DC	voltage range >±10V linearity stability	DVMs like 3458A Calibration/comparison against primary JJ voltage standards is ultimate
Electrical power metrology	DC to 10^3 - 10^4 Hz	linearity stability	AC voltage/current measurements, different from pure DC
Scientific instrumentation	diverse	diverse	Many applications; very specific requirements
High-precision magnet current control	near-DC	voltage range ≥±10V resolution linearity stability deterministic latency	Outstanding performance required for the highest accuracy class in LHC; even higher performance needed for HL-LHC.

Quantization, Excess Noise and Distortion

- An ideal ADC has **no intrinsic noise**

- **"Quantization noise"** - the residue of a sampled **dynamic** input signal
  - Has bounded value of [-½ LSB; +½ LSB] → 1 LSB_{p-p}
  - Under certain simplifying conditions has **uniform probability distribution** and flat frequency distribution
    → *white noise* with RMS value of 1 LSB/$\sqrt{12}$, spread in frequency over (0 - f_s/2)

- Any practical ADC has **excess noise** of electronic origins
  - Has nothing to do with quantization
  - Has **normal** (**Gaussian) probability distribution**
  - Fixed relation between the RMS and p-p values for a given number of samples, derived from basic statistics
    (e.g. k = 3σ (p=0.998) -> factor of 6.6)
  - Can be specified differently: RTI (in V_{RMS}, V_{p-p}, or as a spectral density in V^2/Hz or V/$\sqrt{Hz}$) or RTO (relative to 1 LSB or to FS)

- Any practical ADC has **nonlinearity** that causes **signal distortion**
  - Usually estimated from the harmonics of a pure sine-wave test signal
  - Unlike excess noise, distortion products are **narrowband signals** (quasi-deterministic)

Metrics - SNR and Equivalent Resolution

- **Nominal resolution** – number of bits at the ADC output for a single conversion
- **Digital code resolution** – log_2(*number of digital codes*) ⟶ Arbitrarily high

Signal-to-Quantization Noise Ratio (SQNR) *

$$SQNR\ [dB] = 10log_{10}\frac{P_{signal}}{P_{quant.\ noise}} = 6.02N \quad .76$$

Signal-to-Noise Ratio (SNR) *

$$SNR\ [dB] = 10lo\ _{10}\frac{P_{signal}}{P_{quant.\ noise} + P_{excess\ noise}} \approx 10lo\ _{10}\frac{P_{signal}}{P_{excess\ noise}}$$

Signal-to-Noise and Distortion ratio (SINAD) *

$$SINAD\ [dB] = 10lo\ _{10}\frac{P_{signal}}{P_{noise}+P_{distortion}}$$

hard, or even impossible to measure

To equivalent ideal ADC

Nominal resolution

$$N[bits] = \frac{SQNR\ [dB]-1.76}{6.02}$$

SNR bits

$$SNR\ bits\ [bits] = \frac{SNR\ [dB]-\ .76}{6.02}$$

Effective Number of Bits (ENOB)

$$ENOB\ [bits]\quad \frac{SINAD[dB]-\ .76}{6.02}$$

Ideal or low-resolution ADC

Practical high-resolution ADC

Effective Resolution (ER)

$$ER\ [bits] = lo\ _2\left(\frac{V_{FS(p-p}}{V_{excess\ noise(RMS)}}\right)$$

0V input

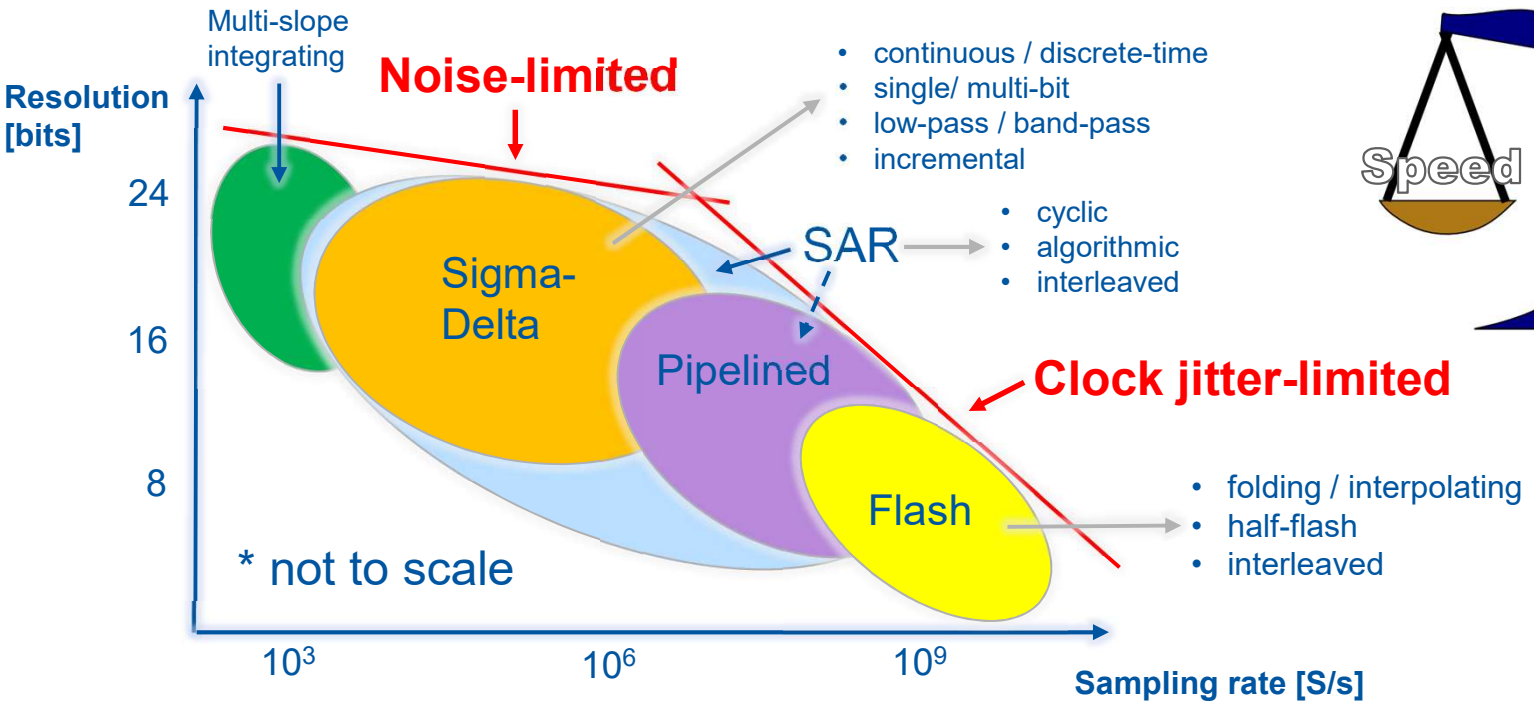
Noise-Free Code Resolution (NFCR)

$$NFCR\ [bits] = log_2\left(\frac{V_{FS(p-p)}}{V_{excess\ noise(p-p)}}\right) = ER - 2.7\ bits\ ^*$$

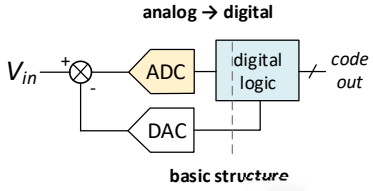
*1000 samples of noise with Gaussian PDF

* for a full-scale pure sine wave

ADC Architectures



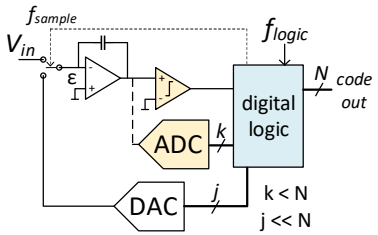
High-Resolution ADC Architectures



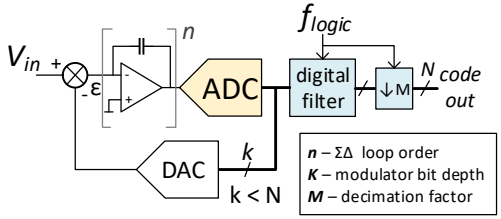
Common features

- closed-loop topology
- low-resolution ADC (or comparator) in the loop
- DAC in the feedback path
- requires $f_{logic} >> f_{sample}$

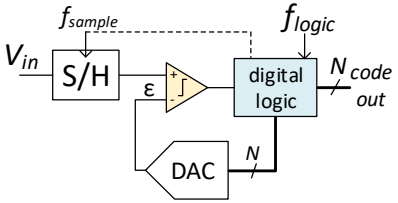
Multislope integrating ADC



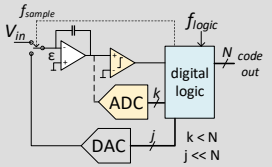
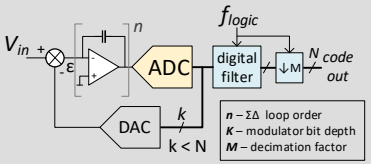
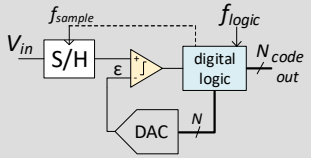
Sigma-Delta ADC



SAR ADC

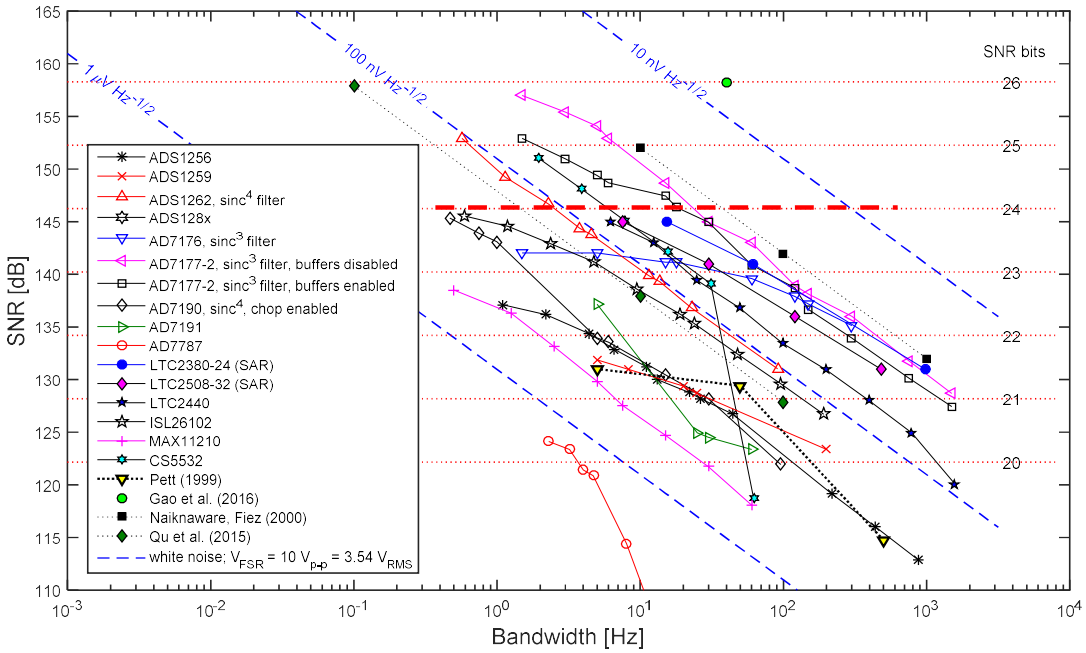


Comparison of the 3 Architectures

	Multislope integrating	Sigma-Delta	SAR
			
In-loop DAC resolution	> 1 bit	≥ 1 bit	N bits (nominal resolution)
Error signal	ε → 0 at EOC *	$\int_t \varepsilon(t)\,dt \to 0$	ε < ±½ LSB at EOC
Speed	slowest	mid-range to fast	fastest
Latency	single cycle	determined by digital filter	single cycle
Unique features	synchronization to power line frequency	quantization noise shaping	easy to multiplex and interleave
IC realizations	no	yes	yes
Typical representatives	Keysight 3458A Fluke 8508A Keithley 2182A	AD7177-2 ADS1281 MAX11210	AD7767 LTC2380-24 MAX11905

* EOC – End of Conversion

State of the art – SNR / Resolution



- Many ADCs have nominal resolution of ≥24 bits, but few achieve 24 *SNR bits* even at very narrow bandwidths (<30 Hz).
- ENOB would be even worse.
- There is considerable spread.

State of the art – Accuracy

ADC	Type	Nominal resolution [bits]	Noise floor [$nV/\sqrt{Hz}$]	Offset drift [ppb/°C]	Gain drift [ppm/°C]	INL (typ) [ppm]
AD7177-2	SD	32	**30** [a]	±8	±0.4	±1
ADS1256	SD	24	120	±20	±0.8	±3
ADS1262	SD	32	110	**±0.1**	0.5	3
ADS1281	SD	32	110	6	0.4	**0.6**
AD7190	SD	24	280 [a]	**±0.5**	±1	±5
LTC2440	SD	24	70	±2	0.2	5
CS5532	SD	24	70	±1	±2	±15
ISL26104	SD	24	120	±30	±0.1	±2
MAX11210	SD	24	250 [b]	5	**0.05**	±10
LTC2508-32	SAR	32	50	±14	**±0.05**	**±0.5**
LTC2380-24	SAR	24	**30** [b]	9	**0.05**	**0.5**
AD7767	SAR	24	60	1.5	0.4	3

Estimated, assuming [a] BW = ODR/3; [b] BW = ODR/2

ODR = output data rate

↓ ppb (!) ↓ <ppm ↓ ≈1 ppm

Technical Limitations

- **ADC input signal range (excluding PGA)**
  - fully differential inputs => 2 x V_{REF}
  - usually **10 V_{p-p}** (±5 V); 5 V_{p-p} is less common

- **Reference voltage**
  - 5 V is standard for **external** reference
  - ≈7 V buried-zener references (LTZ1000, LM399) must be scaled down
  - drift <1 ppm/°C possible only with external zener V_{ref} and good thermal management

- **Broadband voltage noise (ADC input-referred)**
  - V_{REF} noise can be low-pass filtered; ADC core noise – not
  - Typically 50-200 nV/$\sqrt{Hz}$ for high-resolution devices
  - Lower absolute noise floor possible, but with degraded system dynamic range (low-noise PGA at high gain setting)

Input-referred Voltage Noise [nV/$\sqrt{Hz}$]	
100	**good commercial ADCs (core)**
10	best ADCs in scientific literature
1	best bipolar-input op amps
<1	discrete transistors or cryogenic parts

Technical Limitations 2

- **Low-frequency noise**
  - 1/f noise – limiting the mid-term stability (minutes to hours). Not reducible by time-averaging.
  - Usually not specified, but can be deduced from datasheets
  - Best devices: f_{corner} < 1 Hz
  - Auto-zeroing op-amps and stages can have practically no 1/f noise

- **Linearity**
  - Differential (DNL) – typically < 0.1ppm (monotonicity of >24 bits)
  - INL in the best devices is ≈1 ppm (typical) to a few ppm (max)

- **Temperature drifts, etc.**
  - Offset drift is comparable to auto-zero operational amplifiers
  - Gain drift is comparable to the best V_{ref} sources
  - Linearity drift should be considered (may be significant in some devices)
  - Analog signal conditioning stages (input, V_{ref}) should be designed carefully.

The future of High-Resolution ADCs

- Process and ATE improvement → gradual improvement of noise floor, SNR, linearity; better built-in bandgap references
- More **flexibility** in the analog path (PGAs, multiplexers, etc.) – market pressure for industrial applications
- Improvements due to **higher integration** - CDS, built-in calibration, digital processing
- Technologies that could offer a **massive boost** are still very expensive and difficult to use in practice (cryogenics – Josephson junctions, RSFQ; photonics - interferometric ADCs, optical clock distribution)
- **Different approaches** - *if possible*, avoid voltage-input ADCs

- frequency references are much better than voltage references in almost any aspect
- *V-f*, *I-f* – conversion becomes the bottleneck.

Thank you!