

CALIBRATION AND SERVICING HANDBOOK

for

THE DATRON AUTOCAL 1082 and 1081 DIGITAL MULTIMETERS

(The calibration and servicing information in this Handbook applies equally to the Autocal instruments 1081 and 1082.
For operating procedures refer to the User's Handbook.)

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For any assistance contact your nearest Datron Sales and Service center.
Addresses can be found at the back of this handbook.

Due to our policy of continuously updating our products, this handbook may contain minor differences in specification, components and circuit design to the instrument actually supplied. Amendment sheets precisely matched to your instrument serial number are available on request.

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SECTION 1

CALIBRATION

1.1 INTRODUCTION

1.1.1 General

The purpose of calibration is to take account of any long-term drifts in the components of the instrument and to restore the accuracy, traceable to a known standard.

The period between calibrations depends upon the accuracy performance required from the instrument and for guidance, guaranteed accuracies for 24 hours, 90 days and 1 year are quoted.

The calibration procedures presented in the following pages should cater for most calibration situations. If, however, a special problem arises, please contact your Datron Service Center.

1.1.2 The Essentials for Good Calibration

Temperature - So that the instrument can meet its specification over the quoted temperature range, the temperature environment should be stabilized at $23^{\circ}\text{C} \pm 1^{\circ}\text{C}$. In addition, temperature gradients around the instrument should be considered, therefore calibrate the instrument in its normal operating position and allow plenty of room for ventilation.

Warm up - It is essential that the instrument has fully temperature stabilized if the best results from calibration are to be achieved. Therefore, at least a 2 hour warm-up period is recommended during which time the line supply or the covers should not be removed even for a short period. In addition, if the covers have been removed, make certain that they are correctly fitted and that the leaf contacts to the Ground and Guard Shields are in good shape.

Calibration Source - To perform a useful calibration the accuracy of the source should always be at least four times that of the instrument being calibrated. In most cases, examples of likely sources are given for each calibration function.

With some calibration sources, the output may take several seconds to settle to a final value, therefore unless a shorter settling time is assured, a period of 10 seconds is recommended before each calibration operation.

Guarding - It is preferable to arrange for the DMM to be calibrated with 'Local Guard' selected. Furthermore to arrange for the 'Lo' terminal of the DMM to remain at ground throughout and let the the calibration source float. If a 'Remote Guard' connection is necessary then examples are shown in the User's Handbook.

1.1.3 The 'AUTOCAL' Process

1.1.3.1 General

The Datron 'AUTOCAL' process means that complete calibration of AC, DC and Ohms on every range can be carried out from the instrument's own front panel. In the process, an internal non-volatile memory stores calibration constants for each function and range as determined when the instrument takes a series of 16 readings of the applied calibration source. Internally, each of the readings is deviated by one sixteenth of a digit and when an average is taken, the instrument is able to resolve to better than one least significant digit displayed.

Access to the non-volatile memory is gained using a key inserted into the rear panel. When calibration is complete, the key is removed, therefore preventing accidental or unauthorized use of the calibration routine.

1.1.3.2 Procedure Outline

- Select the 'FUNCTION' and 'RANGE' to be calibrated and cancel any 'MODE' or 'COMPUTE' keys.

- Insert the key into the 'CALIBRATE ENABLE' keyswitch on the rear panel and turn to the 'CAL' position. (The 'cal' legend will be displayed on the front panel.)

- Set the rear panel IEEE Bus address switch to 31 i.e. all 1's.

- Connect the calibration source to the input terminals and operate the keys shown in the tables in the following pages. When a 'CALIBRATE' key is operated, its associated L.E.D. indicator will light and extinguish when the calibration operation is executed.

- When all calibration is complete turn the key-switch to 'RUN' and remove the key.

1.1.3.3 The Five 'AUTOCAL' keys

'Zero' - This takes account of offsets in the instrument and in the calibration source.

'Gain' - This sets a scaling factor for each range and function.

'STD' - This very important calibration operation trims the internal master reference voltage. It must be preceded by a 'Zero' operation and is essential prior to a voltage calibration. See section 1.5.

AcHf - This flattens the response of the AC amplifier used for AC voltage measurement. It should only be used when a full calibration i.e. 'Zero', 'Gain' and 'AcHf' is carried out. The calibration action is iterative and requires several operations of the key to complete.

'Lin' - This is an important calibration operation as it optimizes the basic linearity of the internal measurement circuitry used for all ranges and functions. It must be used before any DC voltage or Ohms calibration is carried out.

1.1.3.4 'AUTOCAL' using 'KEYBOARD'

This is an extension of the 'AUTOCAL' process which is useful when using a calibration source set to a nominal value but with known errors. This means for example that calibration directly to a standard cell is possible. A full explanation of the procedure is covered in section 1.6.

1.1.3.5 'AUTOCAL' over the Bus

Each of the five calibration operations can be controlled using Option 50, the IEEE bus. This means that the instrument can be entirely calibrated remotely or under program control. As mentioned in the 'Procedure Outline' for a manual calibration, the rear panel address switch should be set to 31, i.e. all 1's. When a bus calibration is required the address switch must be set to the address number assigned to the DMM in the system. More details of calibration with the bus are included in section 1.7.

1.2 DC VOLTAGE CALIBRATION

1.2.1 General

The procedure in the table opposite is all that is necessary to completely 'AUTOCAL' the DC voltage function. Steps 1 and 2 affect the accuracy on all ranges and should therefore be carried out even if just one range is being calibrated.

On each range a 'Zero' and 'Gain' calibration is required for each polarity of input. The two 'Zero' calibrations are included to overcome a possible zero difference with the polarity setting of the DC calibration source.

If the 'DMM Reading After Calibration' is not in accordance with the table, repeat operation of the same 'CALIBRATE' key is permissible to improve the reading.

1.1.3.6 'Error 4'

If during calibration 'Error 4' is displayed, this indicates that the Calibration Source deviates too far from the calibration span of the instrument. Under these circumstances, the calibration memory is not updated and the calibration LED remains on.

In the case of 'Zero', 'Gain' or 'AcHf' the Calibration Source should be checked and the same 'CALIBRATE' key depressed. The 'Hold' mode may be released any time and the instrument will free-run again. If 'Error 4' follows 'STD' or 'Lin' or persistently appears following 'Zero', 'Gain' or 'AcHf' then an instrument failure may have occurred. Therefore either consult our Customer Service Section or the Servicing Section of this Handbook.

1.1.3.7 'Memory' Key

An 8-character memory is available to record a message, such as the last date of calibration or PRT probe serial number.

The stored message can be changed using the keyboard in 'Cal' mode. Proceed as follows:

- On rear panel, insert key into CALIBRATION ENABLE switch and turn to 'CAL'.
- Select 'KEYBOARD', press 'Memory' key, and use keyboard keys to enter the new message on the display (up to eight numerals).
- Press 'Memory' key.
- On rear panel, turn CALIBRATION ENABLE switch to 'RUN' and withdraw key.

The stored message can be displayed when not in 'Cal' mode, by pressing 'KEYBOARD' followed by 'Memory'.



1.2.2 Equipment Required

- A DC Calibration Source. e.g.:-
Datron 4000 or 4000A

1.2.3 Checking Accuracy after 'AUTOCAL'

To check the accuracy after 'AUTOCAL', use 'Spec' mode in conjunction with the 'CALIBRATION INTERVAL' switch on the rear panel, to display the specification tolerance. Refer to 1081 User's Handbook, Section 7.

DC VOLTAGE CALIBRATION

Step	Calibration Operation	Calibration Source Output	DMM Setting	'CALIBRATE' Key	DMM Reading After Calibration	Remarks
1	Linearity	Short Circuit	DC,1000 Filter	'Lin'	<10 digits	This calibration step may take around 30 seconds to complete
2	10V Range Zero	0.00000V	DC,10	ZERO	$\pm 0.000,00V$ ± 1 digit	
3	10V Range STD CAL	+10.00000V	DC,10	STD	10.000,00V ± 1 digit	Must be done for full calibration
4	10V Positive Full Range	+10.00000V	DC,10	'Gain'	+10.000,00V ± 1 digit	If STD carried out on 10V range omit this step
5	10V Range Zero	-0.00000V	DC,10	'Zero'	$\pm 0.000,00V$ ± 1 digit	
6	10V Negative Full Range	-10.00000V	DC,10	'Gain'	-10.000,00V ± 1 digit	
7	1V Range Zero	+0.000000V	DC,1	'Zero'	$\pm 000,000V$ ± 1 digit	
8	1V Positive Full Range	+1.000000V	DC,1	'Gain'	+1.000,000V ± 1 digit	
9	1V Range Zero	-0.000000V	DC,1	'Zero'	$\pm 000,000V$ ± 1 digit	
10	1V Negative Full Range	-1.000000V	DC,1	'Gain'	-1.000,000V ± 1 digit	
11	.1V Range Zero	+0.0000mV	DC,.1 Filter	'Zero'	$\pm 0.000,0mV$ ± 3 digits	Wait for the reading to stabilize before operating 'Zero'
12	.1V Positive Full Range	+100.0000mV	DC,.1 Filter	'Gain'	+100.000,0mV ± 3 digits	
13	.1V Range Zero	-0.0000mV	DC,.1	'Zero'	$\pm 0.000,0mV$ ± 3 digits	Wait for the reading to stabilize before operating 'Zero'
14	.1V Negative Full Range	-100.0000mV	DC,.1	'Gain'	-100.000,0mV ± 3 digits	
15	100V Range Zero	+0.0000V	DC,100	'Zero'	$\pm 0.000,0V$ ± 1 digit	
16	100V Positive Full Range	+100.0000V	DC,100	'Gain'	+100.000,0V ± 1 digit	
17	100V Range Zero	-0.0000V	DC,100	'Zero'	$\pm 0.000,0V$ ± 1 digit	
18	100V Negative Full Range	-100.0000V	DC,100	'Gain'	-100.000,0V ± 1 digit	
19	1000V Range Zero	+0.000V	DC,1000	'Zero'	$\pm 0.000V$ ± 1 digit	
20	1000V Positive Full Range	+1000.000V	DC,1000	'Gain'	+1,000.000V ± 1 digit	 Lethal voltages present - increase calibration source in 100V steps if possible
21	1000V Range Zero	-0.000V	DC,1000	'Zero'	$\pm 0.000V$ ± 1 digit	
22	1000V Negative Full Range	-1000.000V	DC,1000	'Gain'	-1,000.000V ± 1 digit	 Lethal voltages present - increase calibration source in 100V steps if possible

1.3 OHMS AND PRT CALIBRATION

1.3.1 General

The Ohms Calibration Table opposite contains the complete sequence of operations necessary to 'AUTOCAL' the seven Ohms ranges and the kOhms-PRT function. If just the ' Ω ' range or 'k Ω -PRT' is to be calibrated, steps 1 and 2 of the DC Voltage Calibration Table should be carried out first. Then on each range just a 'zero' and 'gain' calibration is required.

If the 'DMM Reading After Calibration' is not in accordance with the table, repeat-operations of the same 'CALIBRATE' key are permissible to improve the readings.

1.3.2 'Zero' Resistance Source

For accurate 'Zero' calibration on Ohms or kOhms-PRT it is essential that a correctly connected zero source is used. The necessary arrangement is shown in Fig. 1.1; it can be seen that a copper shorting link is required on 1M Ω and 10M Ω ranges, and that '4 wire Ω ' selection is recommended on all ranges.

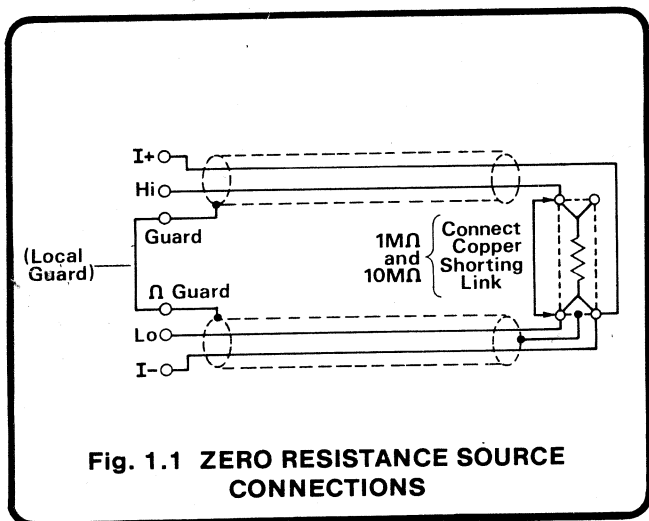


Fig. 1.1 ZERO RESISTANCE SOURCE CONNECTIONS

1.3.3 Equipment Required

Datron 4000, 4000A or a set of resistance standards in decades from 10 Ω to 10M Ω .

It is essential that 10 Ω to 100k Ω standards are 4-terminal devices.

1.3.4 Calibration of the k Ω -PRT Function

Calibrate the k Ω -PRT function under the same conditions as the normal 100 Ω range and immediately following in sequence to avoid disconnecting the standard 100 Ω resistor. On selection of 'k Ω -PRT', the .1 k Ω range is forced, but '4 wire' must be switched manually.

1.3.5 Calibration to a PRT-100 probe

PRTs are originally calibrated by the manufacturer at the fixed temperature points of 0.000 and 100.00 deg.C. The resistance values at these points are given on the calibration certificate provided by the manufacturer.

To calibrate the 1081 to a probe, it is only necessary to enter these two values (or the latest recalibrated values) in the 1081 calibration memory. The procedure is as follows:

1. Switch on the 1081.
2. Ensure that the 1081 'kOhms-PRT' function is correctly calibrated. (Refer to Sect. 1.3.4).
3. a. Select 'PRT'.
b. On rear panel, insert key into the CALIBRATION ENABLE switch and turn to 'CAL'.
- c. Select 'KEYBOARD', and use keyboard keys to enter the PRT resistance value at 0.000 deg. C.
- d. Press COMPUTE 'Zero' key (Cal. zero): 1081 responds by momentarily displaying '0°C' and cancelling 'Keyboard' mode.
- e. Reselect 'KEYBOARD', and use keyboard keys to enter the PRT resistance value at 100.00 deg.C.
- f. Press COMPUTE 'Gain' key (Cal. gain): 1081 responds by momentarily displaying '100°C' and cancelling 'Keyboard' mode.
- g. On rear panel, turn CALIBRATION ENABLE switch to 'RUN' and withdraw key.

The 1081 is now calibrated to the PRT, but not optimized for other PRTs.

It may be convenient to record the Serial Number of the PRT probe as a CAL message in the 1081 memory. The procedure is given in para. 1.1.3.7.

1.3.6 Checking Accuracy after 'AUTOCAL'

To check the accuracy after 'AUTOCAL', use 'Spec' mode in conjunction with the 'CALIBRATION INTERVAL' switch on the rear panel, to display the specification tolerance.

OHMS CALIBRATION TABLE

Step	Calibration Operation	Calibration Source	DMM Setting	'CALIBRATE' Key	DMM Reading After Calibration	Remarks
1	10 Ω Range Zero	4 wire zero	k Ω , 4 wire, 10 Ω filter	'Zero'	$\pm 0.000,00\Omega$ ± 5 digits	Wait for the reading to stabilize before operating 'Zero'
2	10 Ω Full Range	10 Ω [1] Standard Resistor	k Ω , 4 wire, 10 Ω filter	'Gain'	10.000,00 Ω ± 5 digits	Wait for the reading to stabilize before operating 'Gain'
3	.1k Ω Range Zero	4 wire zero	k Ω , 4 wire, .1	'Zero'	$\pm 0.000,0\Omega$ ± 1 digit	
4	.1k Ω Full Range	100 Ω [1] Standard Resistor	k Ω , 4 wire, .1	'Gain'	100.000,0 Ω ± 1 digit	
5	PRT-100 Ω Range Zero	4 wire zero	k Ω -PRT, 4 wire filter	'Zero'	$\pm 0.000,0\Omega$ ± 1 digit	
6	PRT-100 Ω Full Range	100 Ω [1] Standard Resistor	k Ω -PRT, 4 wire filter	'Gain'	100.000,0 Ω ± 1 digit	
7	1k Ω Range Zero	4 wire zero	k Ω , 4 wire, 1	'Zero'	$\pm 0.000,000k\Omega$ ± 1 digit	
8	1k Ω Full Range	1k Ω [1] Standard Resistor	k Ω , 4 wire, 1	'Gain'	1.000,000k Ω ± 1 digit	
9	10k Ω Range Zero	4 wire zero	k Ω , 4 wire, 10	'Zero'	$\pm 0.000,00k\Omega$ ± 1 digit	
10	10k Ω Full Range	10k Ω [1] Standard Resistor	k Ω , 4 wire, 10,	'Gain'	10.000,00k Ω ± 1 digit	
11	100k Ω Range Zero	4 wire zero	k Ω , 4 wire, 100	'Zero'	$\pm 0.000,0k\Omega$ ± 1 digit	
12	100k Ω Full Range	100k Ω [1] Standard Resistor	k Ω , 4 wire, 100	'Gain'	100.000,0k Ω ± 1 digit	
13	1000k Ω Range Zero	4 wire zero	k Ω , 4 wire, 1000, Filter	'Zero'	$\pm 0.000k\Omega$ ± 1 digit	
14	1000k Ω Full Range	1000k Ω [1] Standard Resistor	k Ω , 4 wire, 1000, Filter	'Gain'	1,000.000k Ω ± 5 digits	
15	10M Ω Range Zero	4 wire zero	k Ω , 4 wire, 10M Ω , Filter	'Zero'	$\pm 0.000,00M\Omega$ ± 1 digit	
16	10M Ω Full Range	10M Ω [1] Standard Resistor	k Ω , 4 wire, 10M Ω , Filter	'Gain'	10.000,00M Ω ± 25 digits	

[1] With Standard Resistor sources it may be useful to use the 'KEYBOARD' method of calibration - see section 1.6

1.4 AC VOLTAGE CALIBRATION

1.4.1 General

The procedure in the table opposite is all that is necessary to completely 'AUTOCAL' the AC voltage function. On each range just a 'Zero', 'Gain' and 'AChf' calibration is required.

If the 'DMM Reading After Calibration' is not in accordance with the table, repeat operation of the same 'CALIBRATE' key is permissible to improve the readings. This will be necessary with the AChf key.

Note: To reduce the effects of noise at low input levels, AC zero calibration is carried out at 0.1% Range; and for 100mV Range zero (steps 1 & 2 of the table), Guard is connected to Lo using a copper shorting link.



1.4.2 Equipment Required

A copper shorting link and an AC calibration source e.g. Fluke 5200A and 5215A.

1.4.3 Checking Accuracy after 'AUTOCAL'

To check the accuracy after 'AUTOCAL' the 'Specification Verification' section of the User's Handbook can be employed. It describes the use of 'Spec' mode to verify the accuracy of the instrument, also providing a report sheet 'master copy' for compilation of permanent records.

AC VOLTAGE CALIBRATION TABLE

Step	Calibration Operation	Calibration Source Output	DMM Setting	'CALIBRATE' Key	DMM Reading After Calibration	Remarks
1	DC coupled AC Zero	0.100mV 500Hz (short Guard to Lo)	AC,DC,,1	'Zero'	0.100mV ±10 digits	Set 'Local Guard'. Do not set any filter. Wait for reading to stabilize before operating 'Zero'
2	.1V Range Zero	Short Hi to Lo to Guard	AC,,1	Check only	<100 digits	
3	1V Range Zero	0.00100V 500Hz	AC,1	'Zero'	0.00100V ±1 digit	
4	10V Range Zero	0.0100V 500Hz	AC,10	'Zero'	0.010,0V ±1 digit	
5	100V Range Zero	0.100V 500Hz	AC,100	'Zero'	0.100V ±1 digit	
6	1000V Range Zero	1.00V 500Hz	AC,1000	'Zero'	1.00V +1 digit	
7	10V Full Range LF	10V rms 500Hz	AC,10	'Gain'	10.000,0V ±1 digit	
8	10V Full Range HF	10V rms 30kHz	AC,10	'AcHf'	10.000,0V ±10 digits	
9	1V Full Range LF	1V rms 500Hz	AC,1	'Gain'	1.000,00V ±1 digit	
10	1V Full Range HF	1V rms 30kHz	AC,1	'AcHf'	1.000,00V ±10 digits	
11	.1V Full Range LF	.1V rms 500Hz	AC,,1	'Gain'	100.000mV ±2 digits	
12	.1V Full Range HF	.1V rms 30kHz	AC,,1	'AcHf'	100.000mV ±10 digits	
13	100V Full Range LF	100V rms 500Hz	AC,100	'Gain'	100.000V ±1 digit	
14	100V Full Range HF	100V rms 30kHz	AC,100	'AcHf'	100.000V ±10 digits	
15	1000V LF Range Gain	500V rms 500Hz	AC,1000	'KEYBOARD 500V' 'Gain'	500.00V ±1 digit	 Lethal voltage present - increase calibration source in 100V steps if possible
16	1000V HF Range Gain	500V rms 20kHz	AC,1000	'KEYBOARD 500V' 'AcHf'	500.00V ±15 digits	 Lethal voltage present - increase calibration source in 100V steps if possible. DO NOT EXCEED 25kHz

1.5 STANDARDIZE USING 'KEYBOARD'

The STD key allows the user to trim or standardize the value of the internal Master Reference voltage. The facility can be used to correct for any long term drift, or to avoid a full recalibration of the 1081 when standardizing to local laboratory references.

STD calibration effectively changes the gain of all the voltage ranges in the same ratio, by a simple procedure available either on the 1V or 10V DC ranges. The process functions with a source of magnitude between 20% and 200% of the range selected but it should be noted that for equal magnitude source errors, standardizing at the lower percentage end of the range produces a higher percentage calibration error. An example using 'Keyboard' to standardize directly to a standard cell is shown in the table below.

STANDARDIZE EXAMPLE USING 'KEYBOARD'

Step	Calibration Operation	Calibration Source Setting	DMM Setting	'CALIBRATE' Key	DMM Reading After Calibration	Remarks
1	1V Range Zero	Short-circuit	DC,1	'Zero'	$\pm 0.000,000V$	Short connecting leads at Standard Cell end
2	Connect Standard Cell	Standard Cell	KEYBOARD	—	0	
3	Enter Standard Cell Voltage	Standard Cell	1,.,0,1,8,1,6,9,1	—	+1.018,169,1	
4	Standardize Calibration	Standard Cell	—	'STD'	+1.018,169	

1.6 AUTOCAL USING 'KEYBOARD'

1.6.1 General

The 'KEYBOARD' method of calibration is useful when a calibration source, although set to a nominal value, has known errors. In this situation the known value of the calibration source can be entered into the DVM before the 'AUTOCAL' process is executed.

'KEYBOARD' operates for sources of magnitude between 20% and 200% of the range selected but it should be noted that for equal-magnitude source errors, calibrating at the lower-percentage end of range produces a higher-percentage calibration error.

The process is available for the 'STD', 'Gain', and 'Achf' calibration operations. An example using 'STD' is given in Sect. 1.5.


1.6.2 'KEYBOARD' with Negative Inputs

If the 'KEYBOARD' method is used on DC Voltage calibration with Negative polarity sources, it is important NOT to enter a negative sign with the keyed-in source value. The instrument itself can determine the polarity of the source and update the appropriate calibration memory location.

1.6.3 'KEYBOARD' Calibration Example

The example shown in the table below uses 'KEYBOARD' to calibrate the 1000V AC LF Range Gain at 500V (step 15 of the AC Voltage Calibration table).

CALIBRATION EXAMPLE USING 'KEYBOARD'

Step	Calibration Operation	Calibration Source	DMM Setting	'CALIBRATE' Key	DMM Reading After Calibration	Remarks
1	1000V Range Zero	1.00V rms 500Hz	AC,1000	'Zero'	1.00V ±1 digit	
2	Set and Enter Source Value	500.00V rms 500Hz	'KEYBOARD' then 5,0,0,-,0,0	—	0 then +500.00	 Lethal voltage present. Increase Calibration Source in 100V steps if possible
3	1000VAC LF Range Gain Calibration	As above	—	'Gain'	500.00V ±1 digit	

1.7 'AUTO CAL' OVER THE BUS

All the calibration procedures covered in this manual can be carried out remotely using the IEEE Bus.

Effectively, the five calibration keys are replaced by five Bus instructions and these are used instead of the 'CALIBRATE' keys listed in the Calibration tables on previous pages.

An example of calibration with the Bus is given in the table below. A complete program listing for the same calibration operation assuming an HP9825 controller is as follows:-

```

0: dim D$[15]           define 15 character string
                        variable
1: clr 728              send 'device clear' to DMM
                        (interface 7, address 28)
2: wrt 728,"F3R3Q1W1=" program to DC 1V, SRQ
                        Mode 1, Enable Cal.
3: 0t-S                program zero cal. trigger
4: wrt 728,"G0="

```

```

5: oni 7,"srq"         jump to SRQ service routine
                        on interrupt
6: eir 7,128           enable SRQ interrupts from
                        interface 7
7: if bit ("01XXXXXX",S) check status byte S
                        obtained by service routine.
                        =0: jmp-1 prompt operator to apply
                        calibration source on com-
                        pleting zero cal
8: dsp "Apply 1V &
   CONTINUE"
9: 0-S;stp            program gain cal. trigger
10: wrt 728,"G1="
11: oni 7,"srq"
12: eir 7,128
13: if bit ("01XXXXXX",S)
   =0: jmp-1
14: wrt 728,"T0W0="  program to Internal Trigger,
                        Disable Cal. on completion
                        of gain cal.
                        program DMM to local state
15: lcl 728           SRQ service routine to read
16: stp              status byte
17: "srq";rds(728)-S
18: red 728,D$
19: iret
*7717

```

CALIBRATION EXAMPLE USING THE BUS

Step	Calibration Operation	Calibration Source	DMM Setting	Bus Controller Instruction	DMM Reading After Calibration	Remarks
1	Set DMM to known state	—	In Remote State	'Device Clear'	—	Program DMM to predetermined state A0C0DXE0F3M0N0 00P0Q0R6S0T5
2	Set DMM to DCV, 1V Range, and prepare for calibration	+0.000000V	Calibration key to 'CAL'	'F3R3Q1W1='	—	Program DMM to Function: DC V (F3) Range: 1V (R3) SRQ Mode 1 (Q1) Enable Cal. (W1)
3	1V Range Zero	+0.000000V	In Remote State	'G0='	±.000,000V	Program 'Zero' cal., SRQ indicates when calibration operation completed
4	1V Positive Full Range	+1.000000V	In Remote State	'G1='	+1.000,000V	Program 'Gain' cal., SRQ indicates when calibration operation completed
5	Set DMM to Internal Trigger, Disable Cal.	—	In Remote State	'T0W0='	—	Program DMM to Internal Trigger (T0), Disable Cal. (W0)
6	—	—	In Local State, Calibration key to 'RUN'	'Local'	—	DMM in normal mode, free-running

SECTION 2**MECHANICAL DESCRIPTION****2.1 GENERAL**

The 1081 has been designed to be either rack mounted in a standard 19" rack (3½" [2U] height required) or bench top/portable with integral tilt stand. An exploded view of the instrument is shown in Fig 2.1.

2.2 FRONT PANEL

The front panel incorporates the signal input terminals, range, function, mode, keyboard, compute and power switches and a numeric/legend gas discharge display.

2.3 REAR PANEL

The rear panel incorporates the line supply, power input socket and fuses, analog output socket, rear and ratio signal input sockets, run/calibrate keyswitch and calibration interval (spec) select switch.

2.4 EXTERNAL CONSTRUCTION

A printed key designation overlay adheres to the front panel trapping the polarising filter in front of the display. Both the front and rear panels are held together by two side extrusions running from front to rear. These side extrusions provide both slots for the handles or rack mounting 'ears' and locating points for the structural foam covers. The bottom cover is fitted with the tilt-stand, rubber feet and instruction card. Ground screening for the

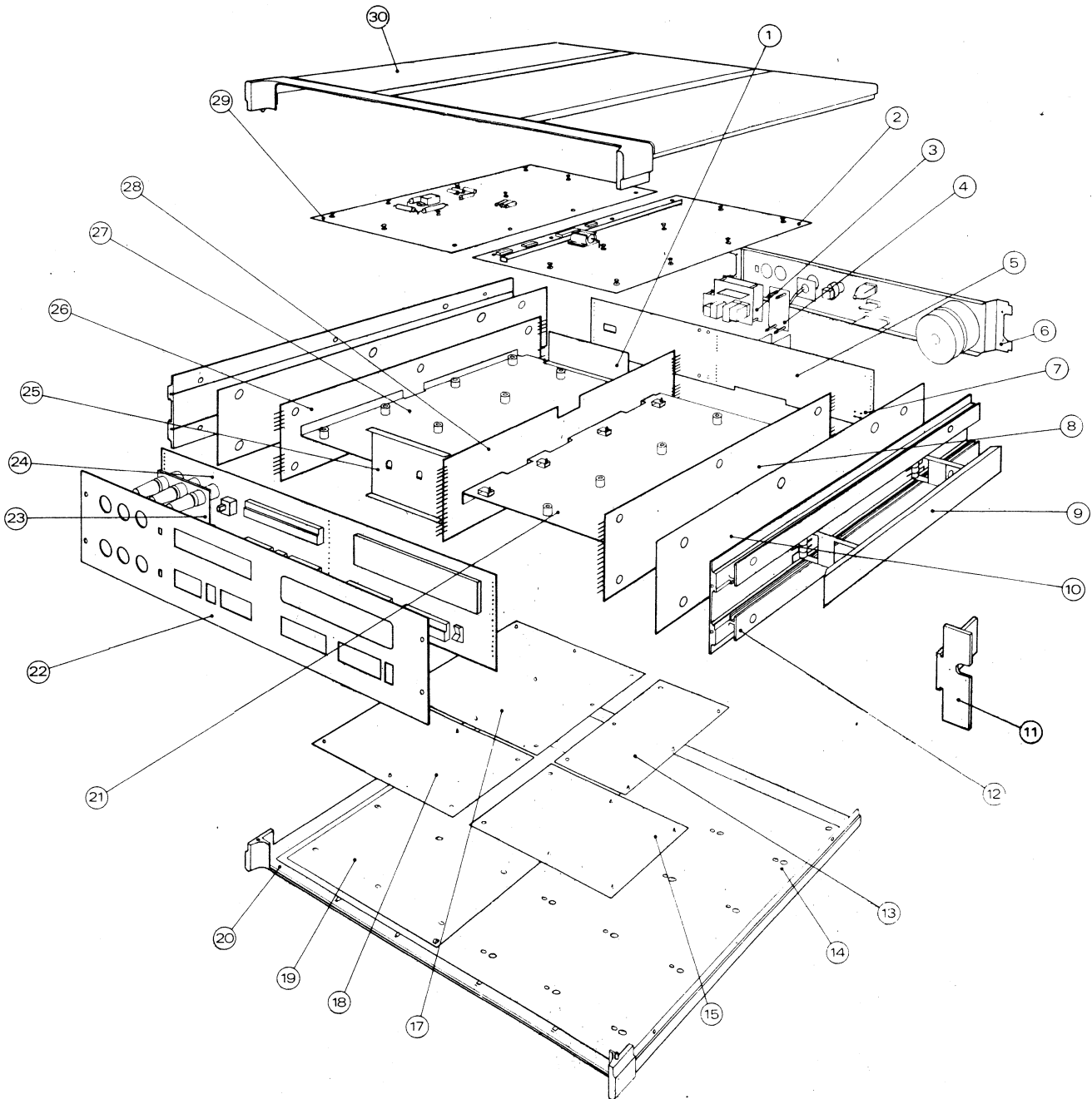
covers and guarding is provided by aluminium plates, heat-staked to the inside of the covers with electrical connections made by spring contacts.

2.5 INTERNAL CONSTRUCTION

An internal chassis is constructed from five printed circuit boards, held together by connectors at each corner and held rigid by two inner aluminium shields fixed horizontally on the instrument's centre line running from front to rear. Input terminals, switches and display are mounted on the front printed circuit board (pcb) and the power supply on the rear pcb. The two side and centre pcb's are used for interconnections between the main circuit boards.

All the main circuit boards are mounted on the inner shields with hinges and quick release fasteners with flexible connections to allow operation in the 'hinged-up' position. The Analog output circuitry is fixed on to the rear pcb of the chassis and the Ratio/Rear Input circuitry on to the rear panel. The options are mechanically fitted and require no soldering.

The chassis is mounted on to the side extrusions with nylon screws, spacers and an insulation sheet to ensure that the 'electrical spacings' of the UL, BSI and VDE specifications are achieved.



- | | |
|---|------------------------------|
| 1. REAR GUARD SCREEN | 17. AC ASSEMBLY |
| 2. DIGITAL ASSEMBLY | 18. OHMS ASSEMBLY |
| 3. RATIO/REAR INPUT ASSEMBLY | 19. OUTER GUARD SCREEN |
| 4. ANALOG OUTPUT ASSEMBLY | 20. BOTTOM COVER ASSEMBLY |
| 5. REAR (POWER SUPPLY) PCB ASSEMBLY | 21. R.H. CENTRE GUARD SCREEN |
| 6. REAR PANEL ASSEMBLY | 22. FRONT PANEL AND OVERLAY |
| 7. POWER SUPPLY VOLTAGE SELECTION LINKS | 23. TERMINAL SUPPORT PLATE |
| 8. R.H. PCB ASSEMBLY | 24. FRONT PCB ASSEMBLY |
| 9. HANDLE ASSEMBLY | 25. FRONT GUARD SCREEN |
| 10. INSULATION SHEET | 26. L.H. PCB ASSEMBLY |
| 11. RACK MOUNTING BRACKET | 27. L.H. CENTRE GUARD SCREEN |
| 12. SIDE EXTRUSION | 28. CENTRE PCB ASSEMBLY |
| 13. DIGITAL INTERFACE ASSEMBLY | 29. ANALOG ASSEMBLY |
| 14. GROUND SCREEN | 30. TOP COVER ASSEMBLY |
| 15. DISPLAY DRIVER ASSEMBLY | |

FIG. 2.1 EXPLODED VIEW OF INSTRUMENT

SECTION 3

TECHNICAL DESCRIPTION

3.1 INTRODUCTION

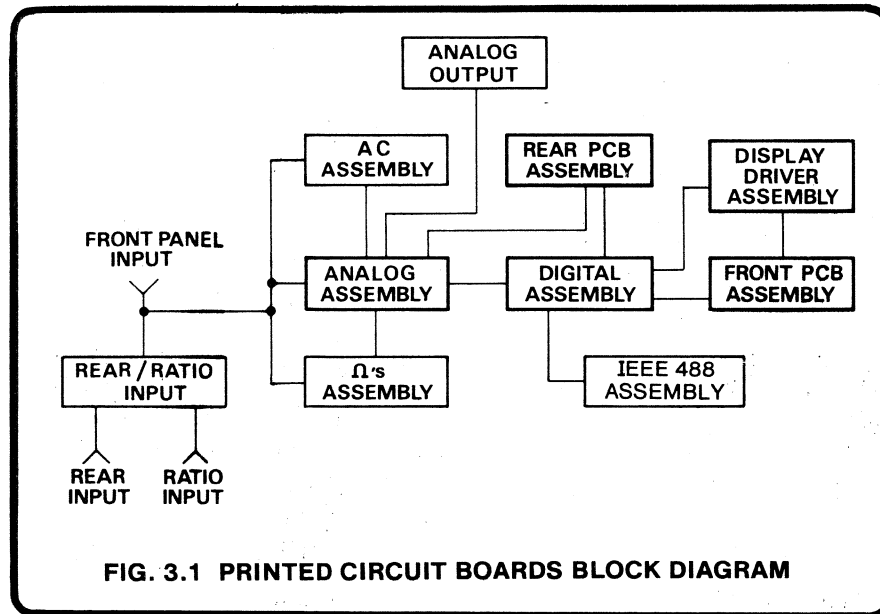


FIG. 3.1 PRINTED CIRCUIT BOARDS BLOCK DIAGRAM

The internal circuits of the basic DC only instrument are divided between five printed board assemblies (shown in bold outline in Fig. 3.1).

For the purposes of explanation each assembly will be described separately and each assembly further subdivided according to the various functions involved.

3.2 ANALOG ASSEMBLY (Circuit Drawing No. 430503).

The Analog assembly is split into three distinct sections: (i) the Analog Interface, (ii) the DC Isolator and (iii) the Analog to Digital (A - D) Converter.

The Analog Interface receives data from the Digital assembly to control the selection of range, scaling and other features of the analog circuitry. Messages between the Analog and Digital assemblies are passed via opto-isolators, electrically isolating one from the other.

The DC Isolator includes the preamplifier, range scaling circuits and bootstrapped supplies. The A - D section converts the scaled input signal to a time period proportional to the signal using a modified triple slope technique.

3.2.1 Analog Interface (430503 sheet 5)

3.2.1.1 Introduction

The Analog Interface provides electrical isolation between the Digital and Analog circuitry. Latched data from the microprocessor is passed through opto-isolators, decoded and latched again on an analog assembly to select function, range, test, average and the D - A converter set up conditions. A line is also provided to instruct the micro-processor which options are present; for AC measurements, this line also indicates the frequency band of measured signals (up to 200Hz, 200Hz to 20kHz, or above 20kHz).

3.2.1.2 Power-On

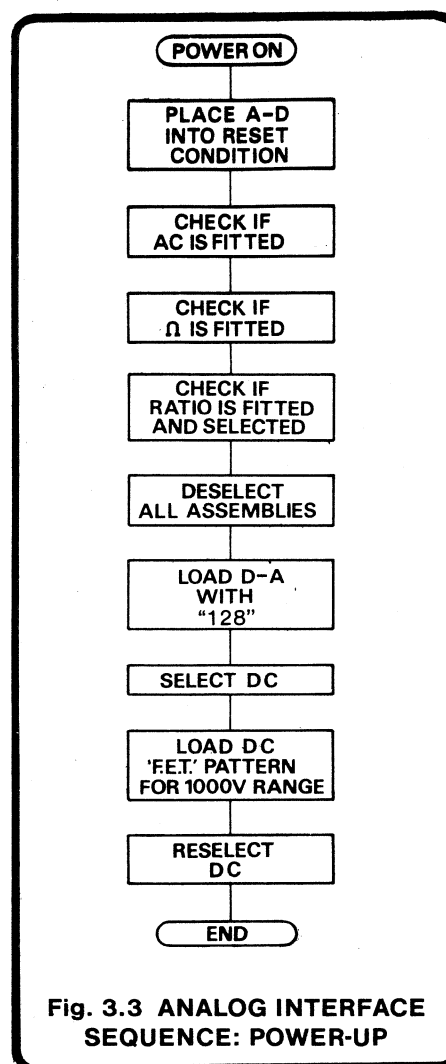
At power-on the A - D converter is placed into the RESET condition (See Section 3.2.3.8). The analog circuitry is then interrogated to discern which options (if any) are fitted. Finally the analog circuitry is placed into the DC, 1000V range until a different range or function is selected (See Fig. 3.3).

To determine which options are fitted, the Digital assembly sends a series of messages across the isolation barrier, decodes them on the analog side and gates them with lines from the option assemblies to feed a signal back across the isolation barrier to the micro-processor.

Option checked	ID line low	Pin No. of M19 held low if Option incorporated
AC	ID 1	M19-3
Ω	ID 2	M19-11
RATIO	ID 4	M19-10

Fig. 3.2 POWER-ON OPTIONS FITTED TEST

Looking at the procedure in more detail, the Analog Interface Data (ID) lines are all set to a logic '1' except one, which is set to a logic '0', depending on the option being interrogated (See Fig. 3.2). As an example we will check to see if the AC option is fitted. ID1 is set low, the rest of the ID lines set high and the Analog Interface Address lines, IA0 and IA1 set low. The opto-isolators *invert* all signals, thus M17-3 is low and M19 pins 10, 4 and 11 are high. If the AC option is *not* fitted M19-2 is driven low via R55 from M17-3, causing M19-3 to be high, producing a logic '0' (-15 volts) on M18-4. If the AC option *is* fitted a 33k Ω resistor on the AC assembly (R15) overrides R55 and a high is placed on M19-2. The effect is to produce a high on M18-4, turning the opto-isolator M2-B on and thus COND. VAL (M2-8) is high, signalling to the Digital assembly that the



AC option is fitted. Similarly, when the Ω or RATIO options are interrogated, the appropriate output of M19 is set low if the option is fitted causing the COND. VAL to be set high.

*Note: ID and IA lines

logic '1' \equiv +5 volts logic '0' \equiv 0 volts

AD lines

logic '1' \equiv 0 volts logic '0' \equiv -15 volts

The next step in the power-up sequence as far as the analog circuits are concerned, is to be placed into the DC, 1000V range (See Fig. 3.3 Flowchart). Firstly, all assemblies are deselected by placing logic '1's on all the ID lines, then setting the IA0 and IA1 lines low (see Fig. 3.4), clocking the option select latches (M20 Analog assembly, M5 AC assembly, M9 Ohms assembly, M1 Ratio assembly) from M17-3. Both IA lines then return high. Secondly, the latches of the D - A converter (M13, M14) are set up to '128', the D - A mid-point value. The ID lines are set to the appropriate pattern and the information is clocked on to M13 and M14 by a delayed low to high edge from M17-4, originating from IA0 going low. The delay makes sure that the signal from M17-10 has disabled the "F.E.T." latch M21. Once again, the IA0 line returns to the resting state of logic '1'. Thirdly, the DC analog circuits are enabled by setting all the ID lines high except ID0, then

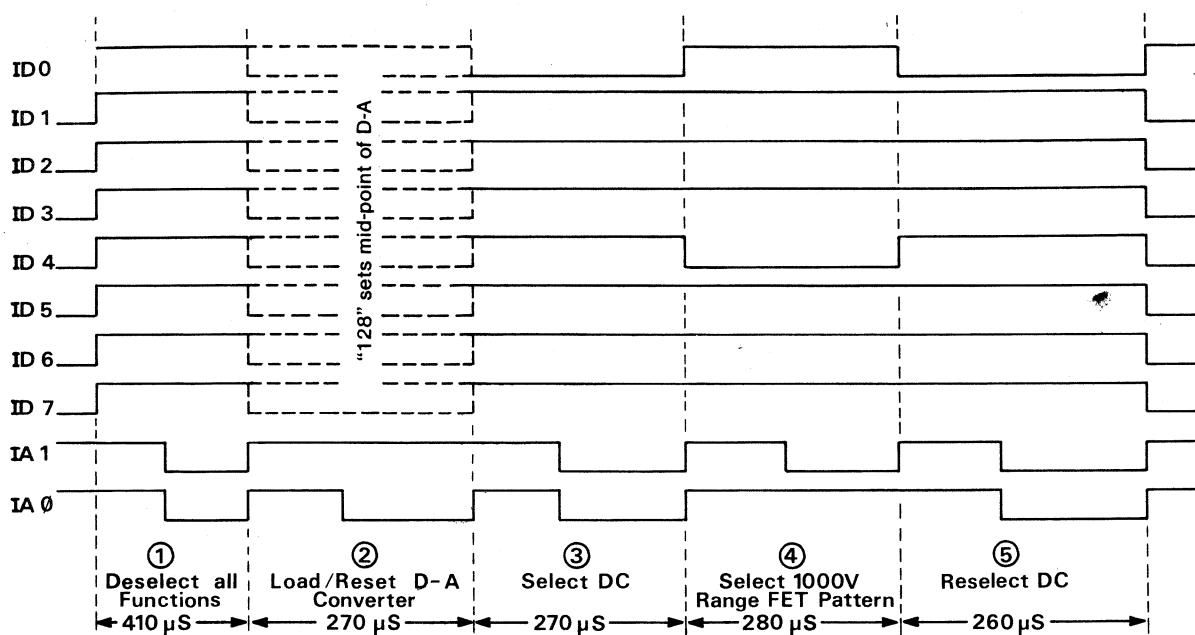


Fig. 3.4 ANALOG INTERFACE DATA LINE TIMING DIAGRAM (Power-Up)

clocking M20 by a low to high edge from M16-6 caused by both IA lines going low. Once DC has been selected, the F.E.T. pattern latch is enabled from M12-1, and the penultimate step is to load the latch with 1000V range data from the ID lines (ID4 low, the rest high). This is executed by clocking the 'F.E.T.' latch from M17-4 once again, but this time being due to IA1 going low. The final step is to reselect DC as described above.

3.2.1.3 General Interface Update Sequence

Before the start of each reading, the analog interface undergoes a complete update. The series of events is the same as the power-up sequence for selection of function and range, as can be seen by comparing the two flowcharts (Figs. 3.3 and 3.5). When Ohms is selected, the DC isolator is also used in the measurement procedure as seen in the following table.

Type of Measurement	Circuits Selected	Use of D - A
DC Volts	Analog Assembly	Linearity Calibration
AC Volts	AC Assembly	Frequency Compensation
AC + DC Volts	AC Assembly	Frequency Compensation
Resistance	Ohms Assembly and Analog Assembly	—

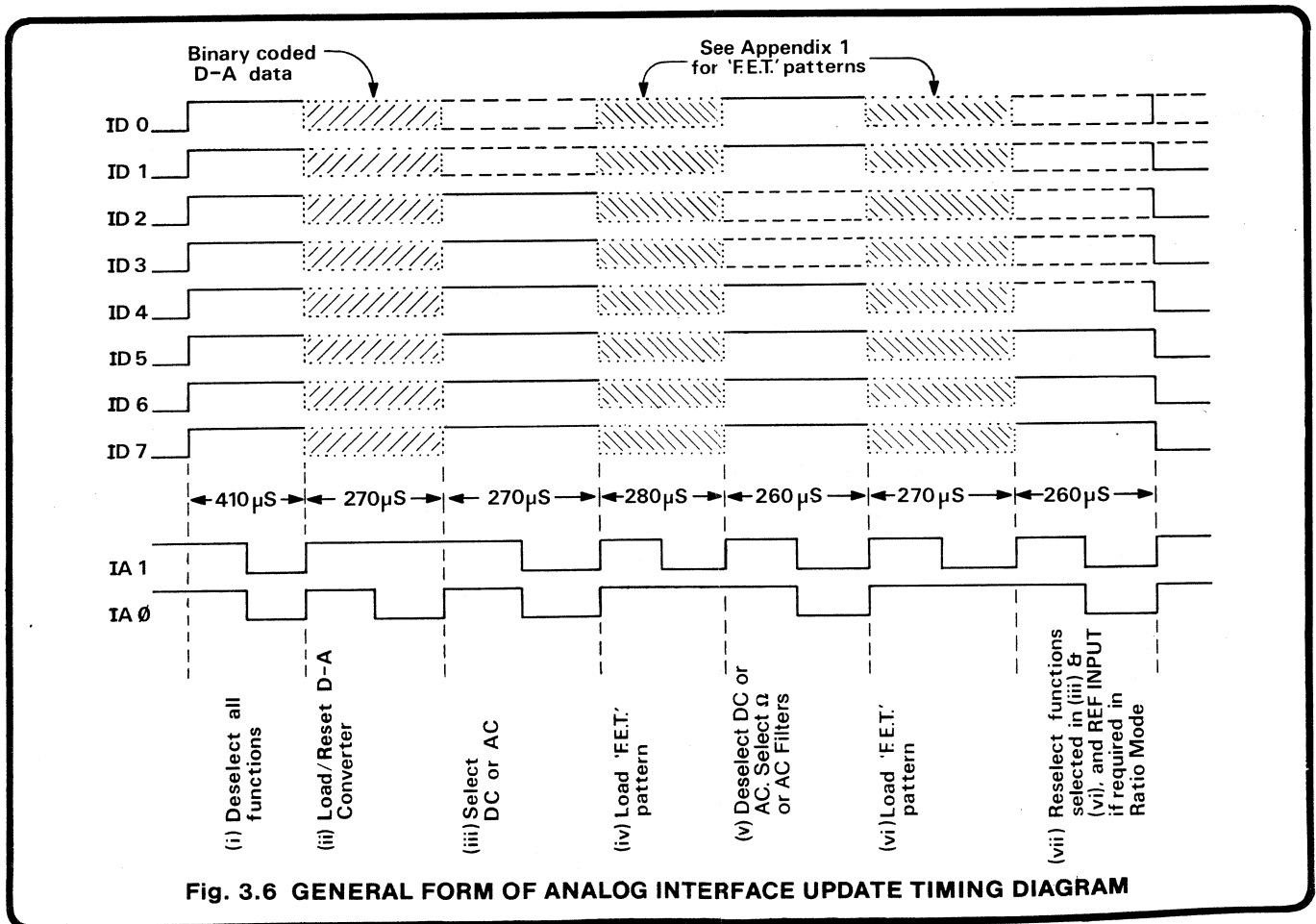
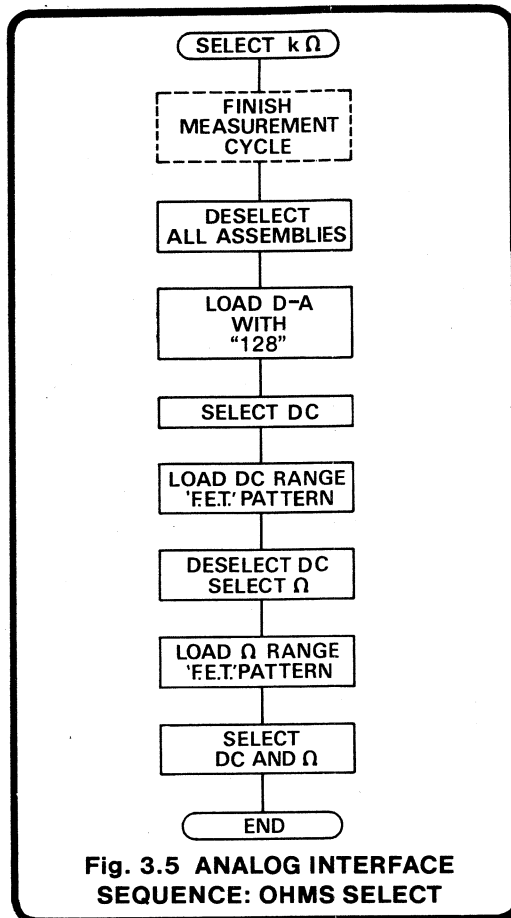
The update sequence order is (i) Deselect all assemblies, (ii) Load D - A latches, (iii) Select AC assembly or DC Isolator, (iv) Load range pattern into DC or AC range latches, (v) Deselect DC or AC and select the Ohms assembly (vi) Load range pattern into Ω 's range latches, (vii) Reselect circuits selected in (iii) and (iv).

Note: Steps (v) and (vi) are used only when Ω is selected.

Flowchart 3.5 gives the above sequence for an ohms update. The general form of the timing diagram for the above sequence is given in Fig. 3.6, the analog 'F.E.T.' pattern for each range of each function being given in Appendix 1.

3.2.1.4 Test

When TEST is selected, a logic '0' is placed on ID7 at stages (iii), (v) and (vii) in Fig. 3.6, i.e. each time a function measurement circuit is selected. Appendix 1 lists the 'F.E.T.' pattern of each assembly for each test measurement cycle.



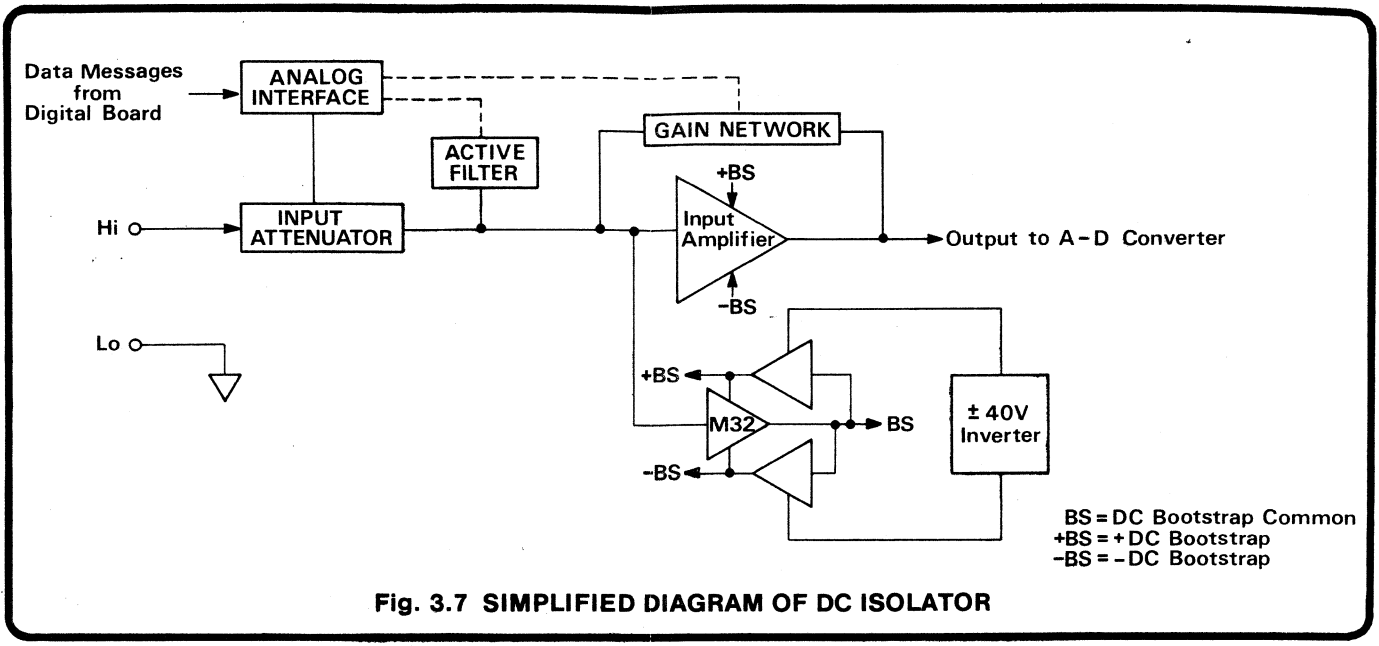


Fig. 3.7 SIMPLIFIED DIAGRAM OF DC ISOLATOR

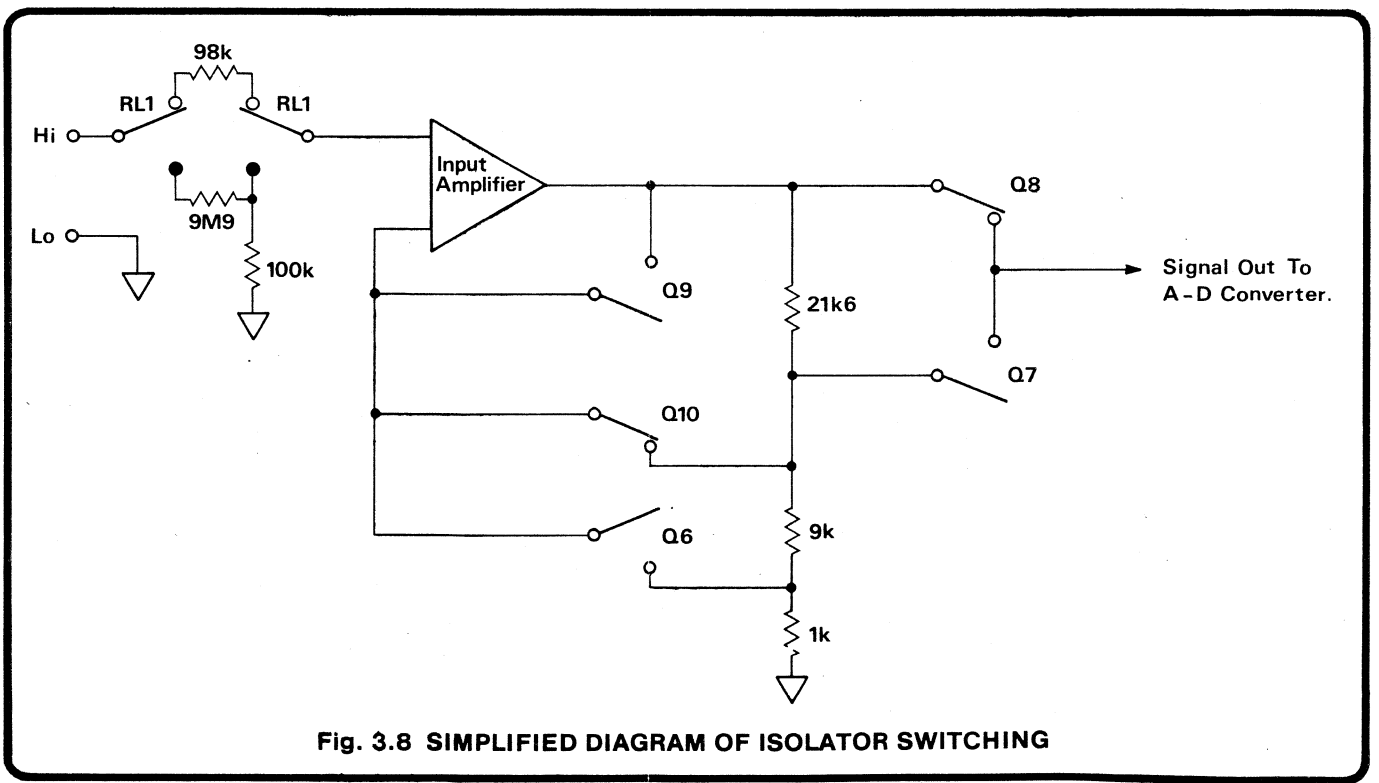


Fig. 3.8 SIMPLIFIED DIAGRAM OF ISOLATOR SWITCHING

3.3.2 DC Isolator Section

3.2.2.1 Preamplifier Scaling (430503 sheet 1)

Figure 3.8 shows the essential features of the isolator scaling circuit. For the purpose of explanation the same symbols are used regardless of whether the switching is accomplished electronically (F.E.T.) or by means of relay contacts. In Fig. 3.8 all switches are shown in the 1V RANGE position.

The various switching combinations for the different ranges are as follows:-

Range	Gain	Q6	Q7	Q8	Q9	Q10	RL1
100mV	x31.6	ON	OFF	ON	OFF	OFF	ON
1V	x3.16	OFF	OFF	ON	OFF	ON	ON
10V	÷3.16	OFF	ON	OFF	ON	OFF	ON
100V	÷31.6	OFF	OFF	ON	OFF	ON	OFF
1000V	÷316	OFF	ON	OFF	ON	OFF	OFF
DC		OFF	OFF	OFF	ON	OFF	OFF

The configuration of the circuit for each range is shown in Fig. 3.9.

Reference should be made to circuit diagram number 430503, sheet 1, for the complete circuit. Sheet 2 gives tables of the coding on the input control lines (from the Analog Interface).

When the 100V or 1kV range is selected, a ÷100, 10MΩ input attenuator (R143, R156, R149, R148) is incorporated into the circuit. This is a matched set of resistors for low temperature coefficient. The selection of a lower range energizes relay RL1 (via Q33), causing resistor chain R119-R122 to be in series with the Hi input. Should an overload signal then be applied, the resistor chain limits the current and the power dissipation is such that 1000V can be applied continuously.

The amplifier end of the resistors is clamped by zener diodes D22, D23 and Q18, Q19 to low, thus the amplifier input can never exceed approximately ±24 volts.

The output from the DC Isolator (test link TL B) is approximately 3.16 volts ($\approx \sqrt{10}$) for a full range (1000000) input. The Preamplifier gain circuits (see Fig. 3.9) operate as follows:

100mV Range Q6 and Q8 are turned on; all other F.E.T.s are turned off and RL1 energized. Thus the output of the amplifier is connected to its inverting input via R108, R109, R110, R111 and Q6, an attenuator chain of ÷31.6, giving the amplifier an overall gain of x31.6. Q8 connects the preamplifier directly to the output.

1V Range Q10 and Q8 are turned on, all other F.E.T.s are turned off and RL1 energized. The output of the amplifier is connected to its inverting input via R108, R109, R110, R111 and Q10, an attenuator

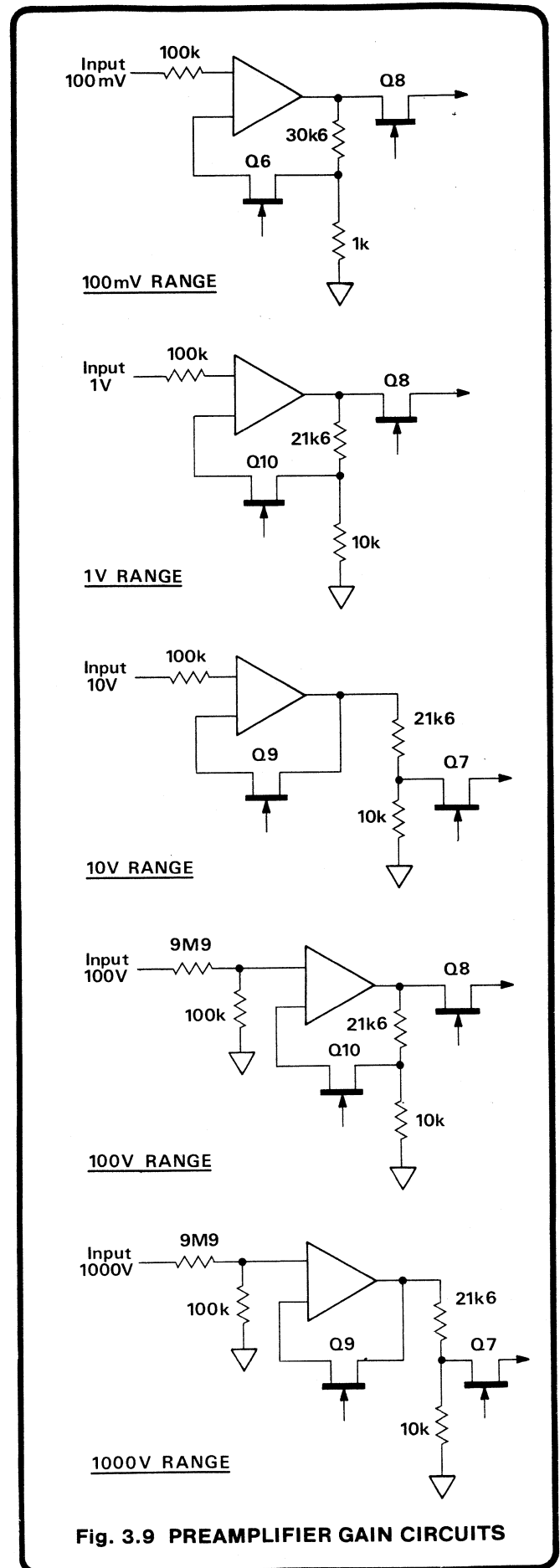


Fig. 3.9 PREAMPLIFIER GAIN CIRCUITS

chain of $\times 3.16$, giving the amplifier an overall gain of $\times 3.16$. Q8, once again, connects the preamplifier directly to the output.

10V Range Q9 and Q7 are turned on; all other F.E.T.s are turned off and RL1 energized. Q9 causes the amplifier output to be directly connected to its inverting input, giving a gain of unity. The output of the amplifier is attenuated by 3.16 (R114, R115) before being passed to the output via Q7 instead of Q8.

100V and 1000V Ranges These two ranges select the 1V and 10V ranges respectively but a $\div 100$ attenuator (R149, R156, R143, R148) is inserted between Hi and the preamplifier input when RL1 is de-energized.

3.2.2.2 Preamplifier (430503 Sheet 1)

The preamplifier is designed to present an input impedance of greater than $10,000M\Omega$ for signals up to ± 20 Volts. It is also bootstrapped (tracking of both ground lines and supply lines with input signal), which is essential for correct operation of common mode rejection.

Q12 is a well-matched monolithic JFET pair exhibiting minimal voltage drift and low noise characteristics, the output being buffered by M31. A chopper-stabilized amplifier (M30) nulls the offset of Q12. Filter components R123 - R126, C30 and C42 eliminate the effects of current 'kickback' from M30 to the main signal path.

3.2.2.3 DC Bootstrap (430503 sheet 2)

Bootstrapping supplies are generated which track the input signal directly (BS), track the input signal with a positive offset of $+12V$ (+BS) and track the input signal with a negative offset of $-12V$ (-BS).

M32 is the high impedance buffer which tracks the inverting input of the preamplifier. The offset of M32 is adjusted so that its input is within $100\mu V$ of the input of the preamplifier. M32 thus functions as the low impedance rail (BS) following the input signal.

Selection of DC (M20-3) enables the capacitive inverter driven from M33 to provide the unregulated $+42V$ (TLC) and $-42V$ (TLD) supply from the $\pm 15V$ supply.

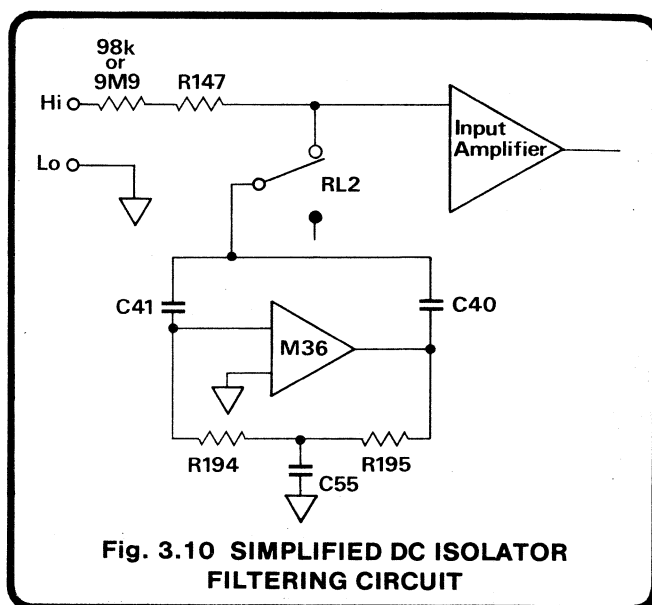
The positive Bootstrap supply (+BS) is generated as a current source comprising Q26 and the shunt regulator, Q27, referenced to D50. When the output voltage of the regulator is approximately 1.2 volts above D50 cathode, Q27 conducts current into R175. Since the current in R175 is controlled to be constant by Q30, referenced to D50, the current flowing through R174 is reduced. Hence

the supply current, "mirrored" in R173, is reduced and the output voltage controlled.

The negative bootstrap supply (-BS) is generated in a similar manner. Thus bootstrapped supplies of approximately ± 12 volts are produced, tracking the input signal exactly.

3.2.2.4 Filtering (430503) sheet 1)

Selection of 'filter' causes an active filter to be switched in by relay RL2 (via Q32). The filter gives an attenuation of $-54dB$ at 50Hz. The essential components of the filter are shown in Fig. 3.10.



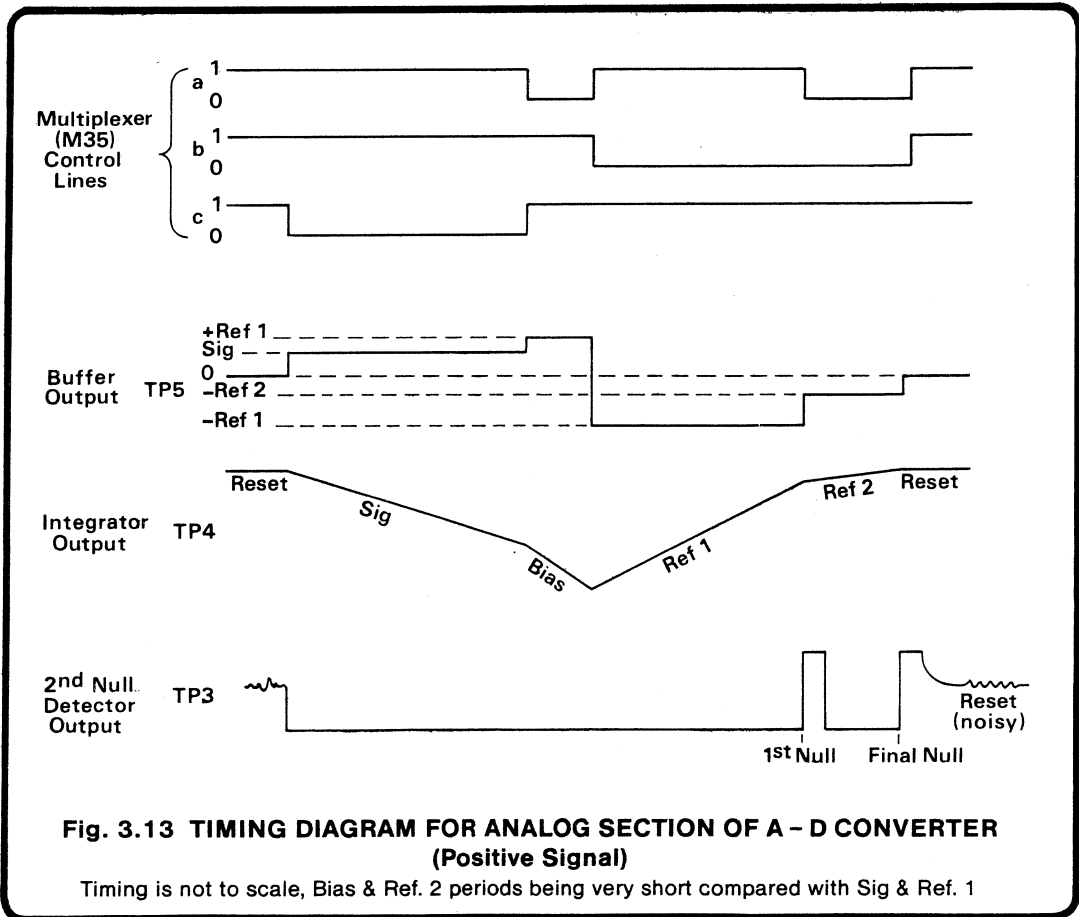
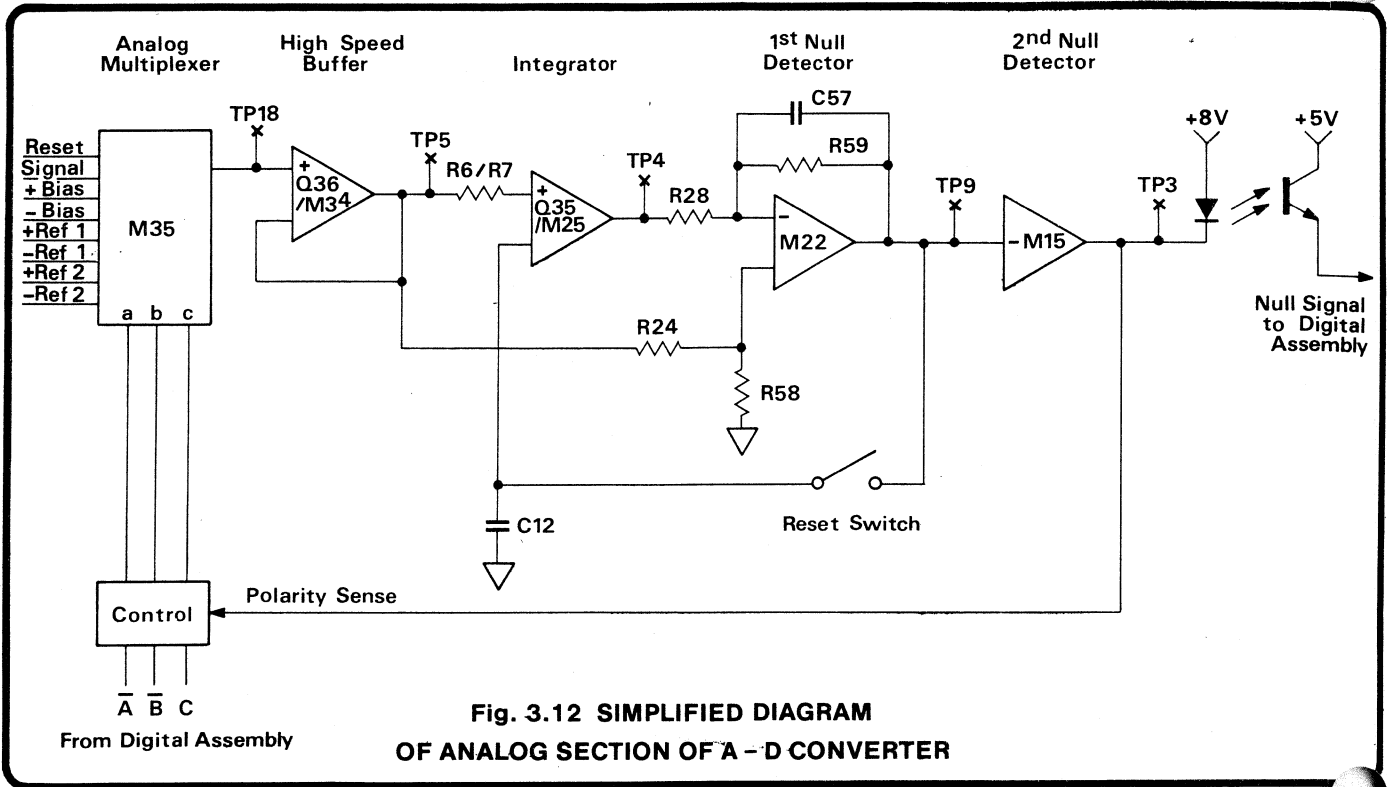
3.2.2.5 Test (430503 sheets 1 and 5)

During the self-test routine, (actuated from the front panel or remotely programmed) the DC isolator is checked for correct operation. The circuitry is placed into the 0.1V range, as described in 3.2.1.3, except that relay RL1 is not energized, (i.e. the $\div 100$ attenuator is across the input amplifier). Filter is selected and F.E.T. Q5 'closed' via M20-5 causing a small signal to be injected into the feedback path of the input amplifier. Thus a signal of -3.125 volts is output from the DC Isolator (TLB). This signal is then measured and compared with a stored value. If the measured signal is within $\pm 6\%$ of the stored value, the test continues with a 1V range check and a 10V range check.

Range	Output signal from DC Isolator (TLB)
0.1V	-3.125 volts
1V	-0.2193 volts
10V	$+0.06932$ volts

DC Isolator Output Test Voltages

3.2.3 Analog to Digital Conversion (Analog Section)
 (430503 Sheets 3 and 4)



3.2.3.1 General Principles

Section 1 and Fig. 1.1 of the User's Handbook give a very basic description of the principles of the integration involved. The technique used in the Autocal Multimeter is a quadruple slope, the two extra slopes being towards the end of the signal and reference integration periods respectively.

Fig. 3.12 is a simplified diagram showing the essentials of the analog section of the A - D conversion and should be used with timing diagram Fig. 3.13 for full appreciation of the circuit operation.

3.2.3.2 A - D Input Control

The analog signal from the DC Isolator is applied to the analog multiplexer (M35) and fed to the input of the buffer (Q36/M34). This in turn feeds the signal to the integrator comprising Q35, M25 and C9.

Control of the multiplexer is derived from the Digital assembly via opto-isolators M4, M5 and M6. These signals control the sequence of events, allowing first the signal, then a bias voltage of the same polarity as the signal, followed by opposite polarity reference and reference +16 signals to the buffer and integrator. The multiplexer is then placed in a reset condition ready for the next measurement cycle. Fig. 3.14 gives the multiplexer control line sequence for both positive and negative signals.

STATE	a	b	c	STATE	a	b	c
RESET	1	1	1	RESET	1	1	1
SIG	1	1	0	SIG	1	1	0
+BIAS	0	1	1	-BIAS	0	1	0
-REF 1	1	0	1	+REF 1	1	0	0
-REF 2	0	0	1	+REF 2	0	0	0
RESET	1	1	1	RESET	1	1	1

Positive signal Negative signal

Logic levels : (0 ≡ -8V, 1 ≡ +8V)

Fig 3.14 MULTIPLEXER CONTROL LINE SIGNALS

3.2.3.3 Reference Voltages Supply (430503 sheet 4)

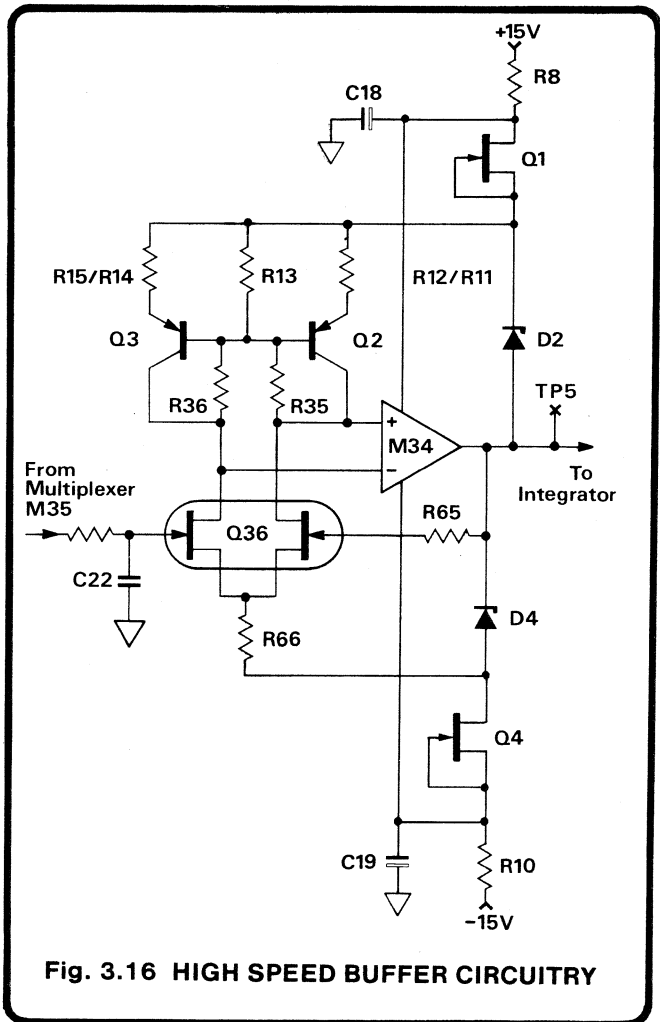
M39 senses the voltages from the two zener chains, setting the reference span across R44 and R45. This resistor pair is very tightly matched so that the positive

and negative references track very closely. M40 is then used to balance the mid-point of R44, R45 to give the correct zero level.

3.2.3.4 High Speed Buffer

C22 slows the switching edges from the multiplexer M35 so that the buffer cannot slew-limit and thus lose the charge. The signals are fed to Q36, M34 which comprise a high speed buffer with high common mode rejection ratio (see Fig. 3.16). The common mode rejection is dependent on the power supplies of Q36 (from R66 and R11-R15) being bootstrapped to the output of the buffer, via D2 and D4. Thus the difference between input signal and power supply around the input stage is maintained constant whatever the input signal.

Q2 and Q3 boost the gain of Q36 by allowing the drains to see a high load resistance.



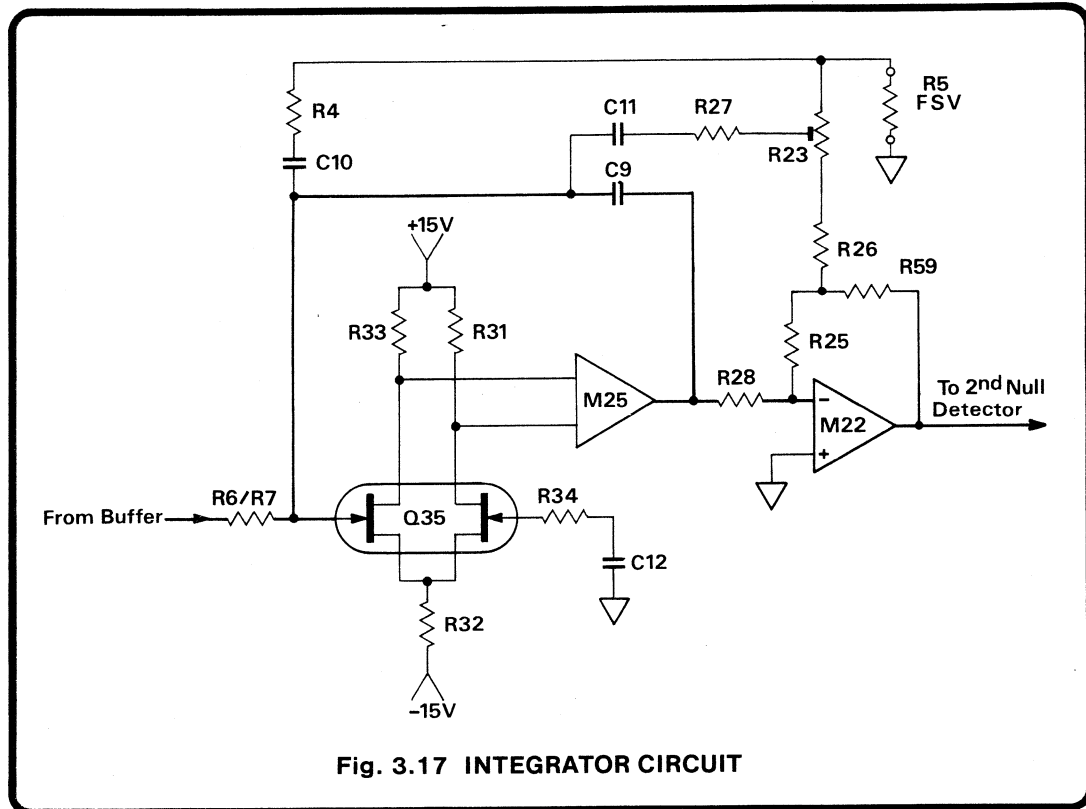
3.2.3.5 Integrator

The basic Integrator comprises R6, R7 and C9, with hybrid amplifier Q35 and M25. (See Fig. 3.17). Low-noise FET-pair Q35 also has low gate leakage, which maintains the effectiveness of 'sample-and-hold' components R34 and C12.

An inverted and attenuated version of the integrator output voltage is developed across R5. This is applied via

R4 and C10 to compensate for the small amount of dielectric absorption in C9. The value of R5 is factory-selected to equalize readings of the same input, taken at differing read-rates (including 'one-shot' measurements).

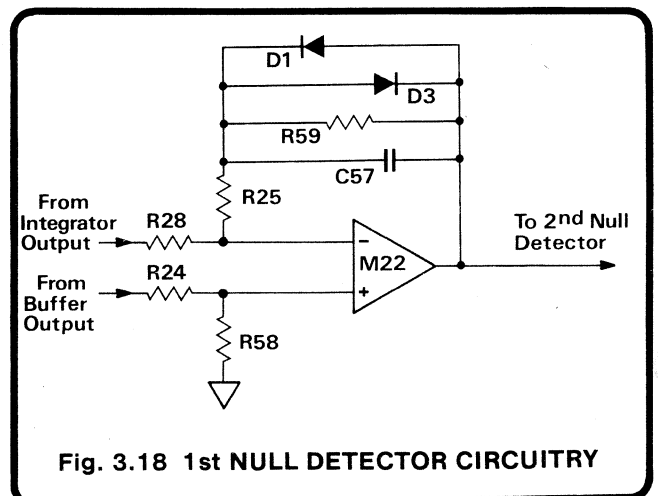
C11 and R27 provide shorter term compensation, R23 being set to correct linearity at 10% of full range.



3.2.3.6 1st Null Detector

The 1st null detector comprises a low noise amplifier, M22, in an inverting configuration, where the DC gain is controlled by the ratio of R59 to R28 for small inputs. For larger inputs from the integrator the clamp diodes, D1 and D3, prevent the amplifier from saturating (Fig. 3.18).

During REF 1 the non-inverting input is offset by approximately 10mV to determine the point at which REF 2 is applied (after counting is synchronised). In REF 2 the offset reduces by a factor of 16 giving the null reference point.



3.2.3.7 2nd Null Detector

The signal from the 1st null detector is voltage-amplified by M15, providing a logic drive signal (NULL DET) via opto-isolator M1. The NULL DET signal is passed to the digital circuitry whenever a null condition changes (Fig. 3.19).

When in "High Resolution" (Hi Res mode, Zero or CAL selected), the input to the 2nd null detector is jittered by small increments of offset in a 16-measurement cycle (see Fig. 3.20). The offsets are generated by D-A converter M28, which is enabled by the level-shifted HI RES signal, and clocked from the 'C' control opto-isolator M6.

For each measurement in Hi Res mode, the displayed reading is the software average of the latest 16 offset measurements. Continuous cycling of the jitter ensures that a valid average is obtained at each measurement, allowing an extra digit of resolution to be displayed.

With Zero or CAL selected, one 16-measurement cycle only is averaged.

The 16-step jitter is not activated in 'Continuous' or 'Block' averaging modes.

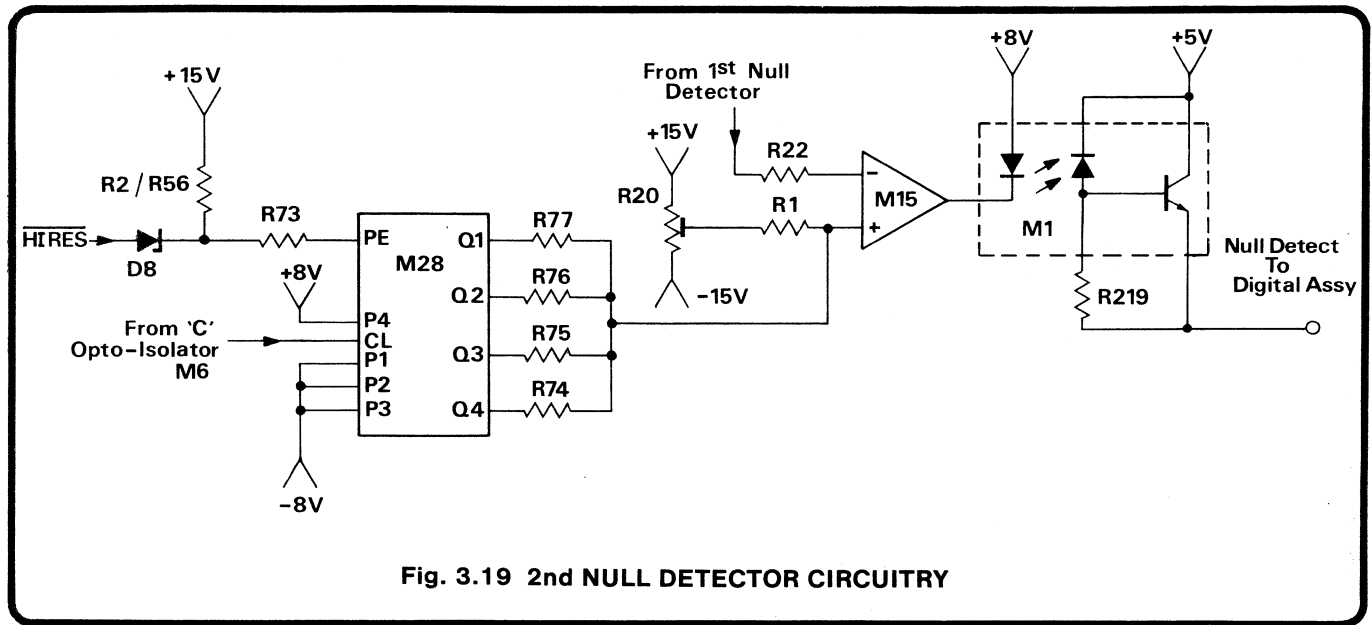


Fig. 3.19 2nd NULL DETECTOR CIRCUITRY

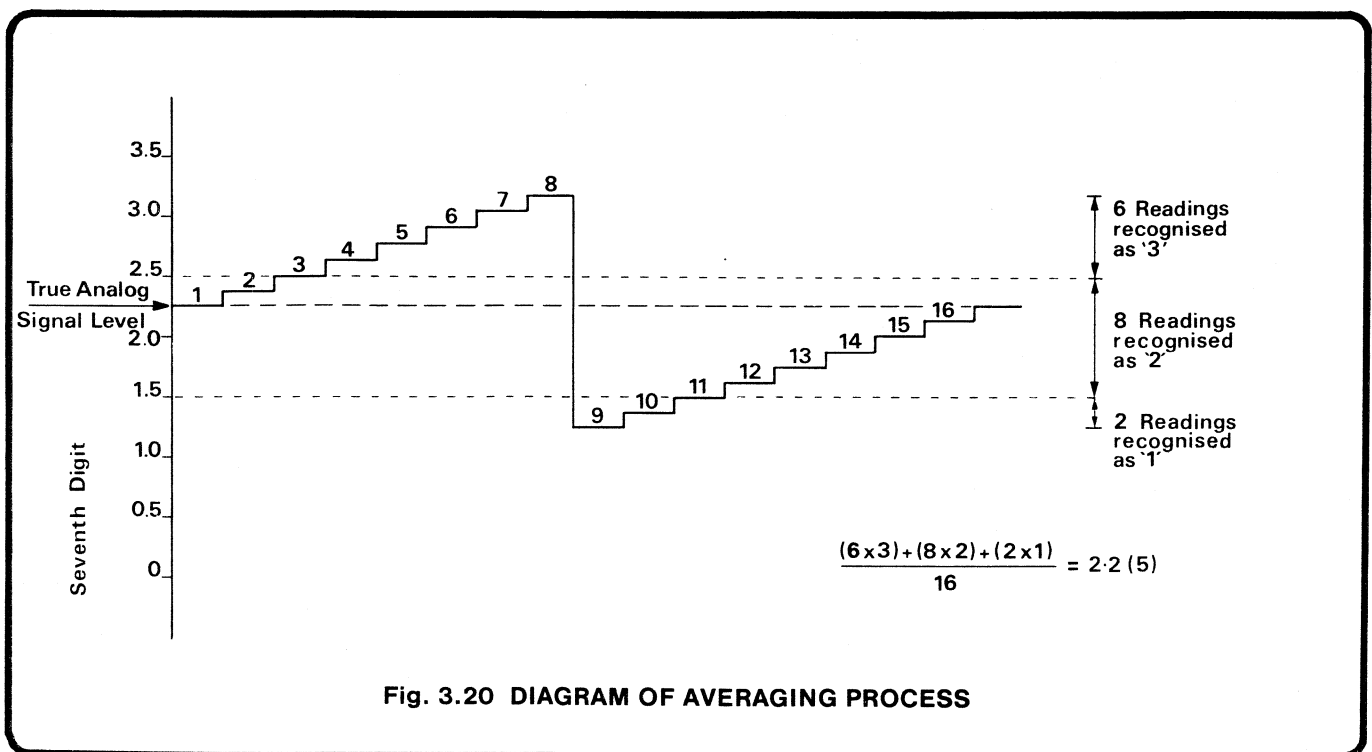


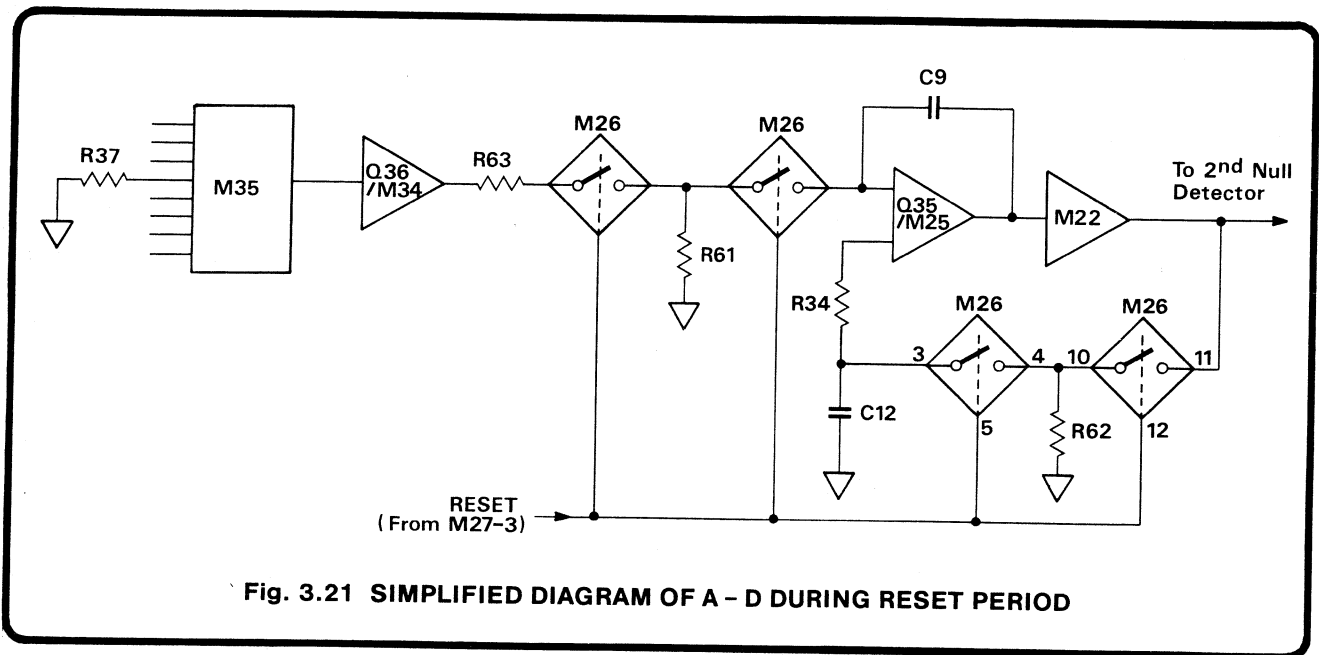
Fig. 3.20 DIAGRAM OF AVERAGING PROCESS

3.2.3.8 Reset Period

At the end of a measurement cycle or in hold, the circuitry is placed into a reset condition. The control lines of the multiplexer M35 allows the 0 volts reference input, at pin 4, to be connected to its output. (See Fig. 3.2.1). At the same time the reset line (M27-3) is taken high turning on M26. This reset signal, applied to pins 5 and 12 of M26 allows the output of the 1st null detector to be fed back via R60 to a sample and hold capacitor C12 on the integrator.

Thus, with the input to the A - D converter at zero volts, the charge stored on C12 is the sum of all the offsets from the multiplexer, buffer, integrator and 1st null detector, allowing the 1st null detector to indicate the true zero crossing (null) point.

The reset signal applied to M26 pins 6 and 13 merely allows a lower impedance path between the buffer and the integrator to speed up the settling time as C9 is discharged to zero.



3.3 AC ASSEMBLY (Circuit Diagram No. 430504)

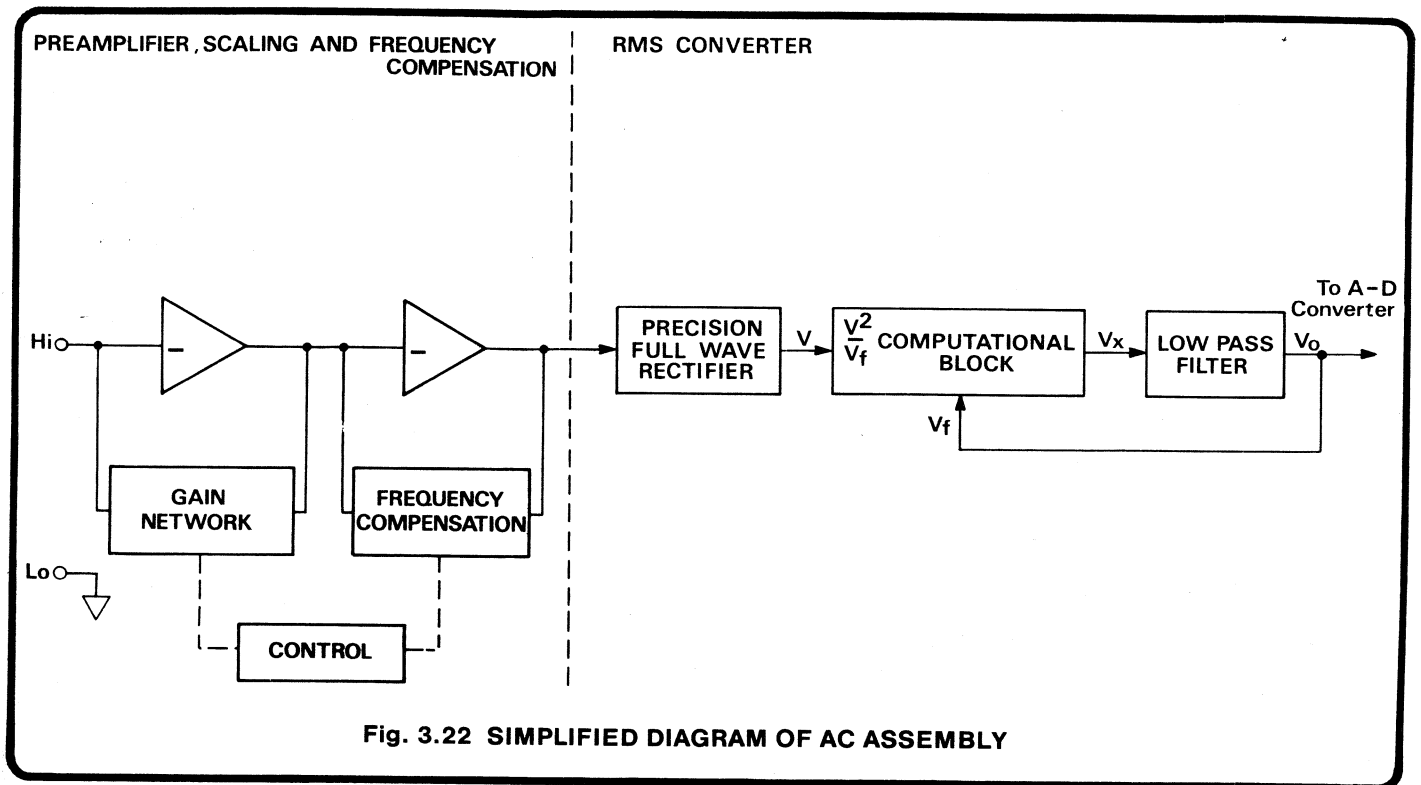


Fig. 3.22 SIMPLIFIED DIAGRAM OF AC ASSEMBLY

3.3.1 General Principles

The preamplifier buffers and ranges the signal in order to present 0.9 volts full range to the AC to DC converter section.

Once converted to an equivalent DC signal, it is applied to the analog to digital converter on the main analog assembly.

The conversion technique is electronic true RMS sensing as shown in the simplified block diagram Fig. 3.22. The Datron RMS module can be best considered as a functional block consisting of circuitry which accepts two inputs, V and V_f , computes V^2/V_f and has an output of V_o which is then filtered so that all the AC components are

removed. The output of the block is fed back to V_f , thus closing the loop around the whole circuitry.

Mathematically: $\overline{V_x} = V_o$

but $V_x = V^2/V_f$

$$\overline{V^2}/V_f = V_o, \text{ but } V_o = V_f$$

$$\overline{V^2} = V_o^2$$

i.e. $V_o = \sqrt{\overline{V^2}}$

3.3.2 Preamplifier and Scaling (430504 Sheet 1)

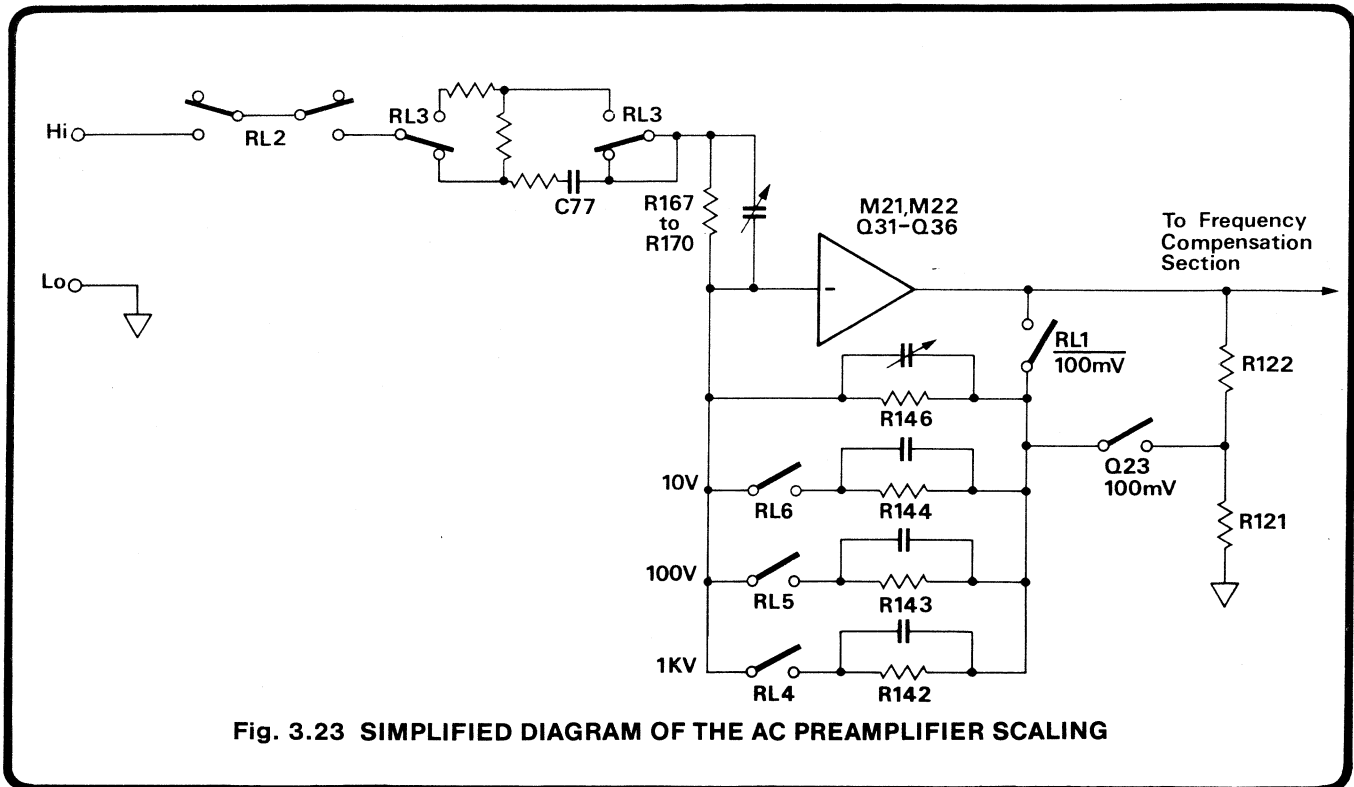


Fig. 3.23 SIMPLIFIED DIAGRAM OF THE AC PREAMPLIFIER SCALING

When the AC option is selected, the AC preamplifier is connected in parallel with the 1000 Volt range of the DC isolator. The resultant impedance presented at the input terminals is a resistance of $1\text{M}\Omega$, shunted by 150pF .

Relay RL2 is energized on selection of AC, directly connecting the Hi terminal to the input of the AC assembly. If DC and AC are selected together, the AC assembly becomes DC coupled by energizing RL3, causing C77, the AC coupling capacitor, to be by-passed.

The signal is then fed to the switched gain inverting preamplifier whose full range output is 0.9 volts r.m.s. A simplified diagram of this arrangement is shown in Fig. 3.23. The frequency response is held flat, to within $\pm 1\%$, by controlling the gain defining component time constants, to a similar order of accuracy. Residual errors are removed by the frequency compensation stage. (See section 3.3.4).

The main amplifier M22 responds to signals from DC to above 1MHz. Its input buffer Q36 reduces bias current errors. A chopper-stabilized amplifier M21 nulls the offset of Q36. Filter components R123 and C90 eliminate the effects of current 'kickback' from M21 to the main signal path. M22 output (Test link TLK) is fed directly to the unity gain frequency compensation stage.

C88 and C89 decouple R160 and R162 except on the 100mV range, when Q33 and Q34 are switched off to provide greater open loop gain. To ensure stability at the higher feedback levels required for the 10V, 100V, and 1000V ranges; C73 is switched in by Q32 to decouple M22 non-inverting input, further reducing the open loop gain.

The unity gain frequency-compensation amplifier includes a stable DC path M20, and a fast AC path Q28 and Q29. The capacitance of varicap diode D14 is determined by the bias voltage at J1-11. The bootstrap circuit of Q17/Q21 ensures that both halves of the varicap are subjected to the same AC signal, removing the non-linearity of the voltage-capacitance characteristic.

3.3.3 RMS Converter (430504 Sheets 2 & 3)

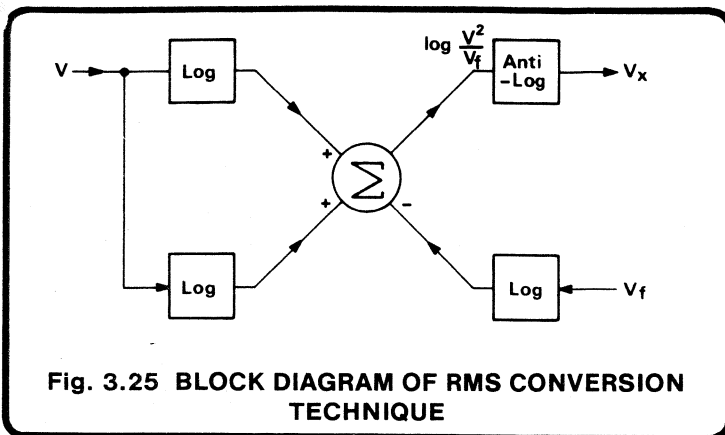


Fig. 3.25 BLOCK DIAGRAM OF RMS CONVERSION TECHNIQUE

The RMS converter takes the scaled AC signal and converts it to an equivalent DC signal suitable for Analog-to-Digital conversion. The technique used is Electronic True RMS Sensing as shown in the simplified block diagram Fig. 3.25.

M13 and M14 form a summing full-wave rectifier. The output of precision half-wave rectifier M13 is summed with the non-inverted signal at the input of M14, with a weighting of 2:1. This forces an accurately rectified full-wave current to flow in RMS module M11. Potentiometer R62 adjusts the rectifier symmetry to provide the same output for signals of either polarity.

The output current from the RMS module drives the low pass current-to-voltage converter M10/M3, which generates a nominal 0.5 Volts for a full range signal. (Note that M10, M9 and M4 are chopper-stabilized amplifiers to handle the low signal voltages).

M16 is the active element of a switched 3-pole Bessel filter. M15 and M17 switch the time constants, extending the overall low-frequency response down to 10Hz, 1Hz or 0.1Hz. (See Fig. 3.24).

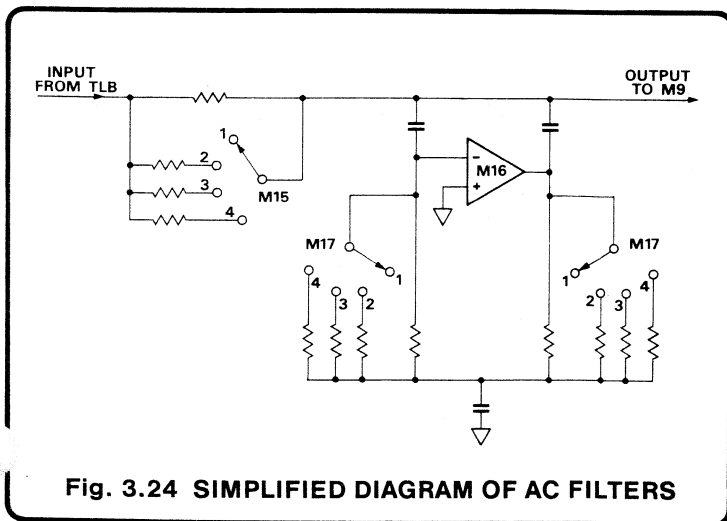


Fig. 3.24 SIMPLIFIED DIAGRAM OF AC FILTERS

The high impedance output from the 3-pole filter is buffered by M9/M2, and the other half of M2 provides a bootstrap for M9 input. R50 is set to null-out the bias current in M9 so that when R44 is dominant (0.1Hz filter selected), the bias current is negligible. D26 and D16 prevent the voltage on TL A from exceeding the +5V power rail, providing overload protection.

The buffer output voltage (3.12V full range) is developed across R52-R56 and R70, referred to Output Common at M4 input. Log-feedback stage M4/M3 closes the 'Square-Root' loop, providing feedback current for the RMS computation in M11.

When the AC, or DC-coupled AC option is selected, Q3 connects the buffer output to the Analog-to-Digital converter. Test links TLC, D, E and F are selectively removed at manufacture to set the correct output level.

3.3.4 High Frequency Compensation

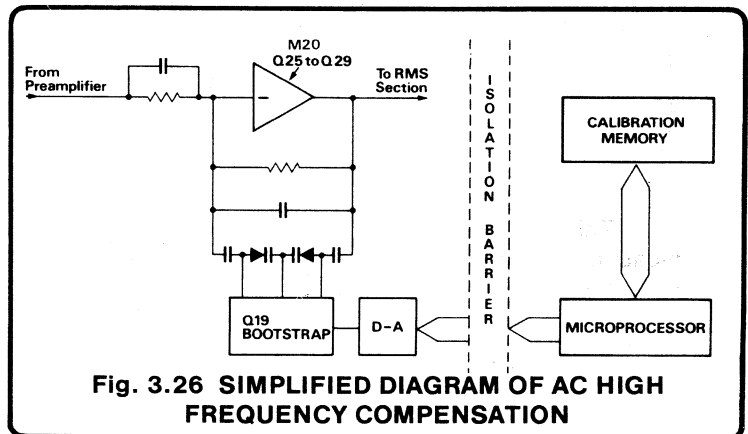


Fig. 3.26 SIMPLIFIED DIAGRAM OF AC HIGH FREQUENCY COMPENSATION

During the calibration cycle, the microprocessor notes and stores the high frequency (HF) error of each range. When AC volts is selected the compensation information for a particular range is recalled by the microprocessor, transferred across the isolation barrier and latched on to M13, M14 (Drawing No. 430503 sheet 5), see Fig. 3.26.

The output from the latches is applied to a digital-to-analog converter, AN2. The voltage produced is fed to the AC converter via connector J1 pin 11 and applied to varicap D11. The varicap is thus adjusted to give the amplifier chain a flat frequency response.

The calibration is carried out at one H.F. frequency but since it flattens the AC amplifier response, the correction is valid for all specified frequencies. It should be noted that the calibration routine is iterative since the varicap is non-linear.

3.3.5 Frequency Detection (430504 sheet 2)

The signal frequency is monitored by M18 and M19. Signals below 2kHz cause a logic-0 (-15V nominal) at pin 4 of both detectors. If the frequency is 2kHz or above, M18-4 rises to logic-1 (0V nominal), and if 20kHz or above, M19-4 also rises to logic-1. M18 and M19 outputs are open-drain FETs (logic-1 active).

For each AC measurement, the digital system sets F3 = logic-0, recording the logic state of J1-1 (HF FLAG). Then F3 is set to logic-1, and HF FLAG is recorded again. The result of this two-part test is interpreted by the digital system as shown in the table below:

HF FLAG states		Frequency Band
F3 = 0	F3 = 1	
0	0	$f < 2\text{kHz}$
1	0	$2\text{kHz} \leq f < 20\text{kHz}$
1	1	$f \geq 20\text{kHz}$
0	1	Excluded combination

This frequency information is retained until the next measurement and used to select the appropriate measurement uncertainty for display if 'Spec' is selected.

3.3.6 Test

During the self-test routine (actuated from the front panel or remotely programmed) the AC assembly is checked for correct operation. The circuitry is placed into the .1V range as described in Section 3.2.1.3. F.E.T. Q31 is 'closed' from M7-13 causing a signal of 0.08 volts DC to be injected into the preamplifier. Thus a signal of approximately 3.14 volts is output from the RMS section and applied to the A - D converter situated on the Analog assembly. This signal is then measured and compared with a stored value. If the measured signal is within $\pm 6\%$ of the stored value, the test continues with a 1V range check.

Range	Output from RMS section
.1	+3.14 volts
1	+0.314 volts

3.4 OHMS ASSEMBLY (Circuit Diagram No. 430505)

The instrument functions by measuring the voltage across an unknown resistance with a known constant current flowing in it. The converter can be split into two parts: a low-drift voltage follower, and a constant current sink covering 6 decades from 500nA to 10mA (see Fig. 3.27).

It should be noted that when the Ohms assembly is fitted, the DC Isolator Lo is no longer connected directly to the front/rear panel Lo terminal, but goes via RL1 on the Ohms assembly (connector link removed on side panel). Lo becomes an active terminal in resistance measurements.

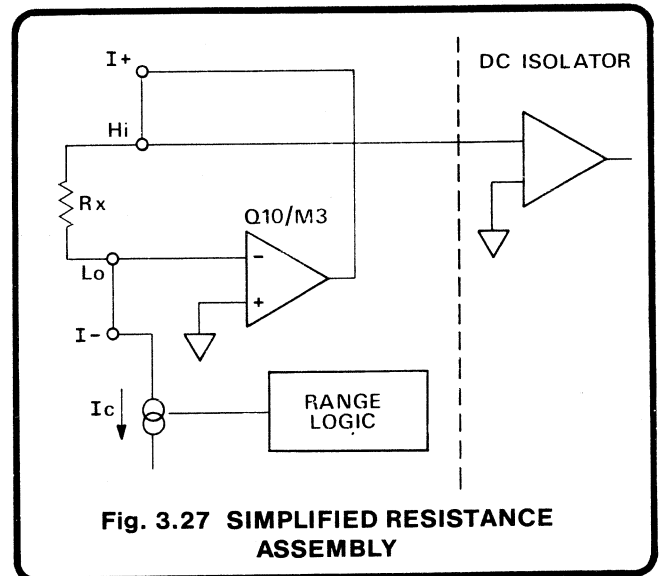


Fig. 3.27 SIMPLIFIED RESISTANCE ASSEMBLY

For 2-wire measurement, I+ is linked to Hi, I- to Lo, and the unknown resistance (R_x) is connected between Hi and Lo. The constant current I_c flows from its source at Q10/M3, along the path:

$$I^+ \rightarrow \text{Hi} \rightarrow R_x \rightarrow \text{Lo} \rightarrow \text{I}^-$$

into its precision current sink.

The Lo terminal is maintained at Reference Common (0V). Therefore the Hi terminal (DC Isolator input) is held at $[I_c \times (R_x + \text{lead resistance})]$ volts above Lo. The voltage measured by the DC Isolator is thus an accurate analog of the resistance of R_x and its connecting leads.

For 4-wire measurement, the resistance of the leads is eliminated by connecting I+ and Hi separately to one R_x terminal, with I- and Lo each connected separately to the other. In this case the voltage measured by the DC Isolator is an accurate analog of the resistance of R_x alone; as the voltage drop is sensed directly across R_x , and no current flows in the sensing leads.

The DC Isolator voltage measurement is scaled in software (effectively divided by the constant current value) to provide a direct reading in Ohms.

3.4.1 Low Drift Voltage Follower (430505 sheet 1)

When OHMS is selected, the front panel Lo terminal is connected to the inverting input of amplifier Q10/M3, with the non-inverting input referred to DC Isolator Lo (this remains Reference Common). Q10/M3, together with output follower Q13, apply a voltage to the I+ terminal such that the voltage at the Lo terminal is kept at 0V (Reference Common). The offset voltage of Q10 is removed by the use of the chopper-stabilized amplifier M10. Compensation network R26, R35, R68, R18 nulls out the small bias current of Q10 and M10.

Input protection is provided as follows:

Voltage/Current applied to input terminals

I+: R9, D10, D11, D15

I-: R2, D1, D2, Q20, Q21, R23.

Lo: R12, R13, Q8, Q9.

Open circuit voltage limit protection

I+: R15, R16, Q6, Q7.

I-: R6, D7, D8, Q2, Q22.

3.4.2 Constant Current Source (430505 sheet 1)

Seven decades of Ohms ranges are provided by 6 ranges of current (see Fig. 3.29), and 3 DC Isolator voltage ranges:

10 Ω range and PRT	-	100mV
100 Ω , 1k Ω , 10k Ω , 100k Ω ranges	-	1V
1M Ω , 10M Ω ranges	-	10V (5V full range)

Range	Current	F.E.T.s/Switches turned on	
		Current Selector	Leakage path
10 Ω	10mA	Q11	M2(A)
100 Ω	10mA	Q11	M2(A)
PRT	1mA	M1(A)	
1k Ω	1mA	M1(A)	
10k Ω	100 μ A	M1(B)	
100k Ω	10 μ A	Q4	M2(B)
1M Ω	5 μ A	M1(D)	Q3, M2(C)
10M Ω	500nA	M1(C)	Q3, M2(C)

FIG. 3.29 OHMS CURRENT RANGE SWITCHING

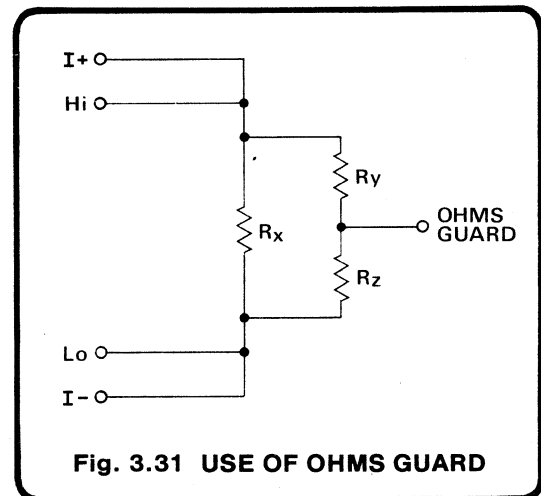
When k Ω is not selected, M2D is turned on, holding C8 charged up to approx 6V. When k Ω is selected, M2D switches off and Q17 (Sheet 2) is turned on, enabling astable M6 to produce a 200Hz signal to switch M5.

Thus when gates B and C of M5 are open, C9 is charged up from the negative reference (originating from the analog section of the A - D converter). These gates close, then A and B open, sharing the charge with C8 (sheet 1); the voltage across C8 soon equals the reference voltage.

The voltage developed across C8 causes M4 to sink current through resistor chain R24, R25, R29, R30, R31 until the voltage developed across the chain balances that across C8. Thus the current required for a particular range is selected by the value of the resistor chain switched by M1, M2, Q4 and Q11. Simplified diagram Fig. 3.30 shows the resistor chain and switching for each range. On the high resistance ranges leakage paths are provided by Q3, M2(B) and M2(C).

To produce good common mode rejection, M4 supplies are bootstrapped, the supply span being defined by a 13 volt zener, D17. The filtering bootstrap supplies (+ Ω BS and - Ω BS) power the astable (M6) and bilateral switch M5.

The use of ohms guard permits in-circuit measurement of resistors, provided shunt paths are greater than 250 Ω and a suitable tapping point is available. Consider Fig. 3.31. Guard is reference 0, Lo is actively maintained within microvolts of reference 0 (as previously explained). Thus there is no voltage across Rz and consequently no current in Rz. Voltage follower Q10/M3 will simply pass more current into Ry from the I+ terminal until the selected current for the particular range flows through Rx.



3.4.3 Test

During the self-test routine (actuated from the front panel or remotely programmed), the Ohms Converter is checked for correct operation. The circuitry is placed into the 10M Ω range as described in Section 3.2.1.3. Filter is selected and FET Q5 'closed' from M9-1 causing R8 (9.76k Ω) to be placed between I+ and Lo. 2-wire must be selected on the front panel (Error 6 occurs during self-test if this is not done).

M1C is on so 100 μ A flows through it. Since Lo is maintained at 0V there is no potential difference across either R1 or R3. Therefore all the current flows in R8 generating approximately 1V on I+ and Hi. The resulting voltage output from the DC Isolator is applied to the A - D converter, measured and compared with the stored value. If the measured value is within $\pm 6\%$ of the stored value, the test is complete.

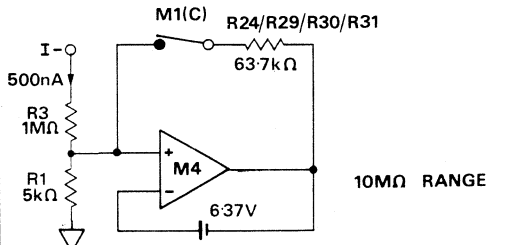
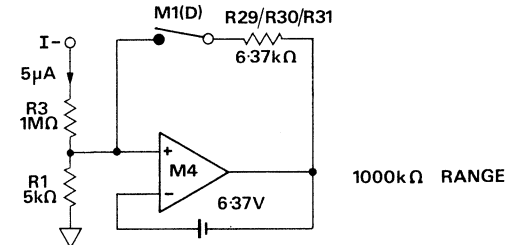
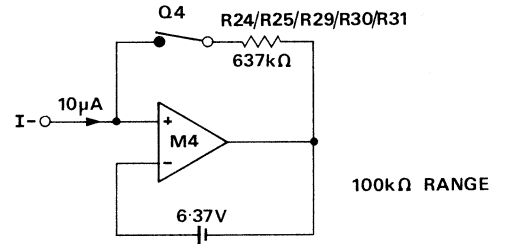
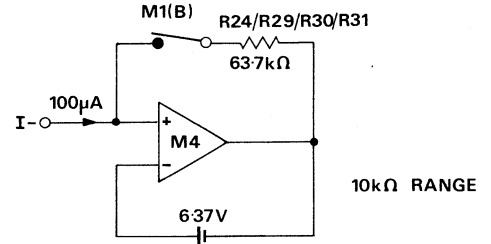
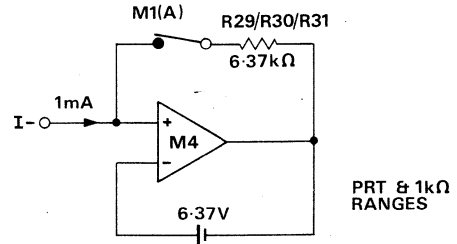
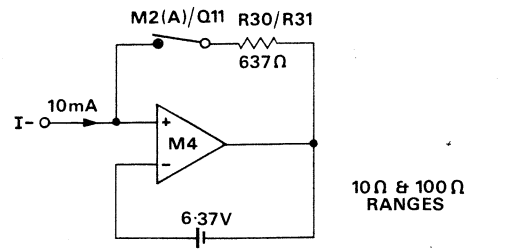


Fig. 3.30 SIMPLIFIED Ω CURRENT SWITCHING

3.5 REAR INPUT/RATIO ASSEMBLY (Circuit Diagram No. 430506)

3.5.1 General

The Rear Input/Ratio assembly contains switching circuitry which selects the input to be measured — from one of 3 channels:

Front panel terminals - J6 on Rear Input/Ratio pcb
 SIG socket - J11 on rear panel
 REF socket - J10 on rear panel

A user makes the selection either remotely, using IEEE codes I or P (see User's Handbook Table 4.4); or from the front panel, using the MODE keys:

- 'Sig' selects inputs from J11 (SIG) only.
- 'Ref' selects inputs from J10 (REF) only.
- ' Δ ' or 'Ratio %' (or both) provides a continuous series of readings, each processed digitally from two measurements: the first from J10 (REF) and the second from J11 (SIG). The Rear Input/Ratio assembly therefore alternates between J10 and J11 under software control.

Switching information enters the Rear Input/Ratio assembly via J2, to be latched by M1, which sets the input conditions for relay driver transistors Q1, Q2, Q5, and Q6. Relays RL1 and RL4 switch the Hi and I+ input lines, RL2 and RL3 switch Lo, I-, Guard and Ohms Guard.

3.5.2 Front Panel/Rear Panel Switching

To select the front terminals, AD6 is set to logic-1 (M1-9 at 0V) and the positive-going edge of 'OP SEL CLK' clocks M1-11. M1-13 is latched at logic-1, turning on Q1 and Q6, energizing relays RL1 and RL2. Thus the front input terminals are connected to the internal measurement circuits. Should 'Rear' input, 'Ratio %' or ' Δ ' be selected, AD6 is clocked into M1 as logic-0 (M1-9 at -15V). M1-13 is latched at logic-0, Q1 and Q6 are turned off, so the contacts of relays RL1 and RL2 permit RL3 and RL4 to select between the two rear inputs.

3.5.3 SIG/REF Switching

To select REF (J10), AD6 is at logic-0 (see para 3.5.2), AD4 is set to logic-1 (M1-5 at 0V) and the positive-going edge of 'OP SEL CLK' clocks M1-3. M1-1 is latched at logic-1, turning on Q2 and Q5, energizing relays RL3 and RL4. Thus J10 is connected to the internal measurement circuits. Should SIG (J10) be selected, AD4 is clocked into M1 as logic-0 (M1-5 at -15V). M1-1 is latched at logic-0, Q2 and Q5 are turned off, so relays RL3 and RL4 connect J11 to the measurement circuits.

3.5.4 Ratio %, Δ , or Δ % Selection

For these mode selections, M1-13 remains at logic and the logic state of M1-1 is reversed during the last part of each analog interface update sequence (see Fig. 3.6). As a result, relays RL3 and RL4 alternately select J10 (REF) and J11 (SIG) inputs.

3.5.5 Hi and I+ Delays

To avoid excessive slew-rates in the measurement circuits, the Hi and I+ line switching is delayed by components in the base circuits of Q5 and Q6. This allows the input commons and guards (RL2 and RL3 contacts) to assume their correct potentials slightly before Hi and I+ are applied.

3.5.6 Test

When TEST is selected, a check is carried out to see if the Rear Input/Ratio option is fitted. R9 holds the AD4 line at logic-1 (0V) for the 'Option fitted' test (refer to sect 3.12).

3.6 ANALOG OUTPUT ASSEMBLY (Circuit Diagram No. 430308)

3.6.1 General

The Analog Output Assembly accepts the DC Isolator or AC Converter output and converts it to a ± 1 volt DC full range output. This signal can then be used, for example, to drive X-Y plotters or strip chart recorders.

3.6.2 Description

The 3.16 full range signal from the DC Isolator to AC Converter is buffered by unity gain amplifier M2. The output is potentially divided by R7 and R8 so that 1 volt full range is presented to M1, another unity gain amplifier. Potentiometer R5 is adjusted to remove any offset caused by M1 and M2. Positive temperature coefficient thermistors R3, R4 and diodes D1, D2 protect the analog output circuitry from accidental input applied to the Analog Output external connector.

3.7 DIGITAL ASSEMBLY (Circuit Diagram No. 430526)

The Digital assembly contains the digital section of the A - D converter, and the circuitry which provides the general management of the instrument. Fig. 3.33 outlines the main elements and signal highways of the digital system.

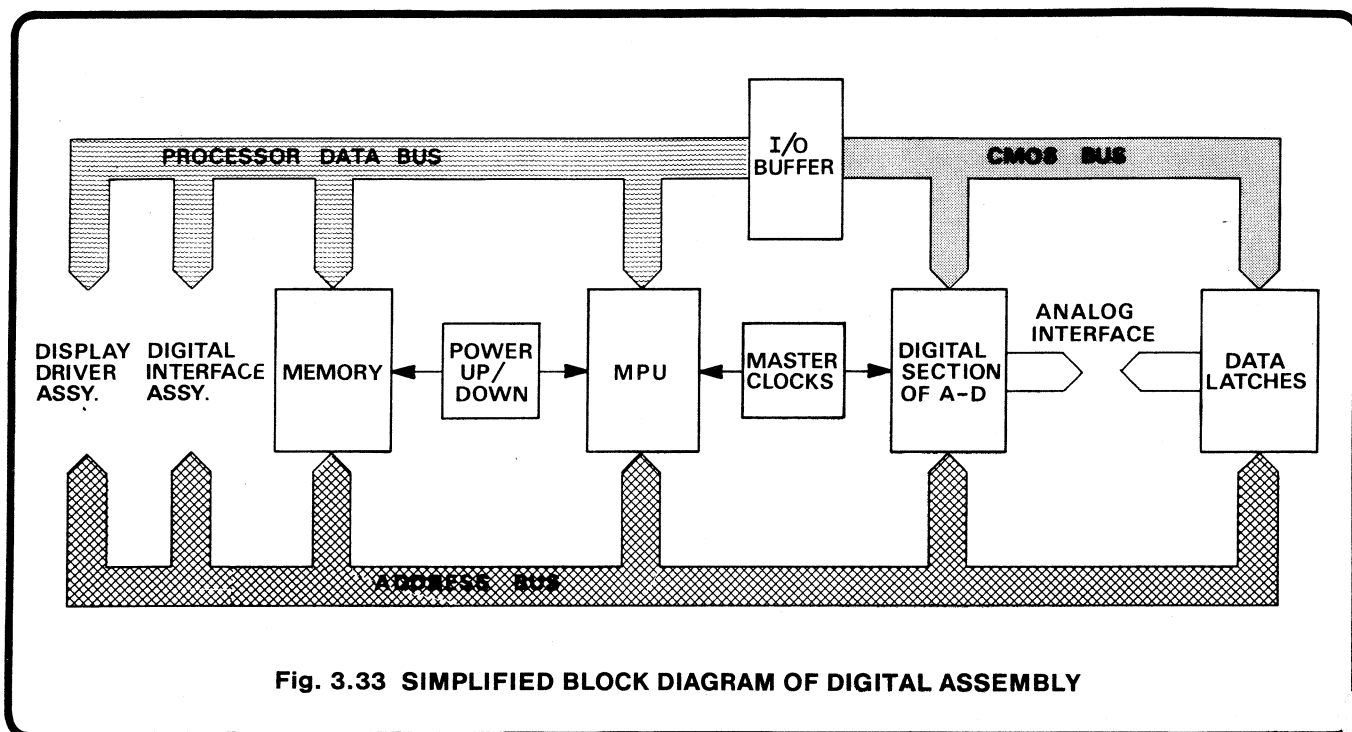


Fig. 3.33 SIMPLIFIED BLOCK DIAGRAM OF DIGITAL ASSEMBLY

3.7.1 Processor and Memory (430526 sheet 1)

A 6800 general-purpose microprocessor (MPU) together with 16k-bytes of memory controls the communication between the digital and analog assemblies, front panel, digital interface and display drivers. The memory can be split into three main areas:

- Program Memory:** Stored in 12k-bytes of ROM, this defines the 6800 MPU processes for control of the 1081 DMM. The ROM also contains constant data such as self-test limits, 'Spec' readout specifications and other fixed factors.
- Non-volatile Calibration Memory:** 256 bytes of RAM backed up by an internal battery, this stores the calibration errors used for each reading (updated during any 'AUTOCAL' or 'ZERO' operation).
- Operating Memory:** 1k-bytes of RAM store any intermediate calculation results, the DMM status, Max/Min

and limit values, etc. A separate RAM on the Front Assembly holds volatile display data. No battery back-up is provided, so all this data is lost when the instrument is powered down.

3.7.1.1 Software Overview

The system uses the technique of a looping prioritized job scheduler (see Fig. 3.34). Each job driven from the scheduler is controlled by a flag in the system workspace which is set when the job is required to be run and cleared when completed. Priority of activation is ensured by making each job exit on completion, to the top of the schedule.

Program Modules: The program memory is split into a series of functional modules, each module corresponding fairly closely to a major functional area and hence to one of the jobs activated by the job scheduler, the larger ones being sub-divided, see Drawing No. 890043.

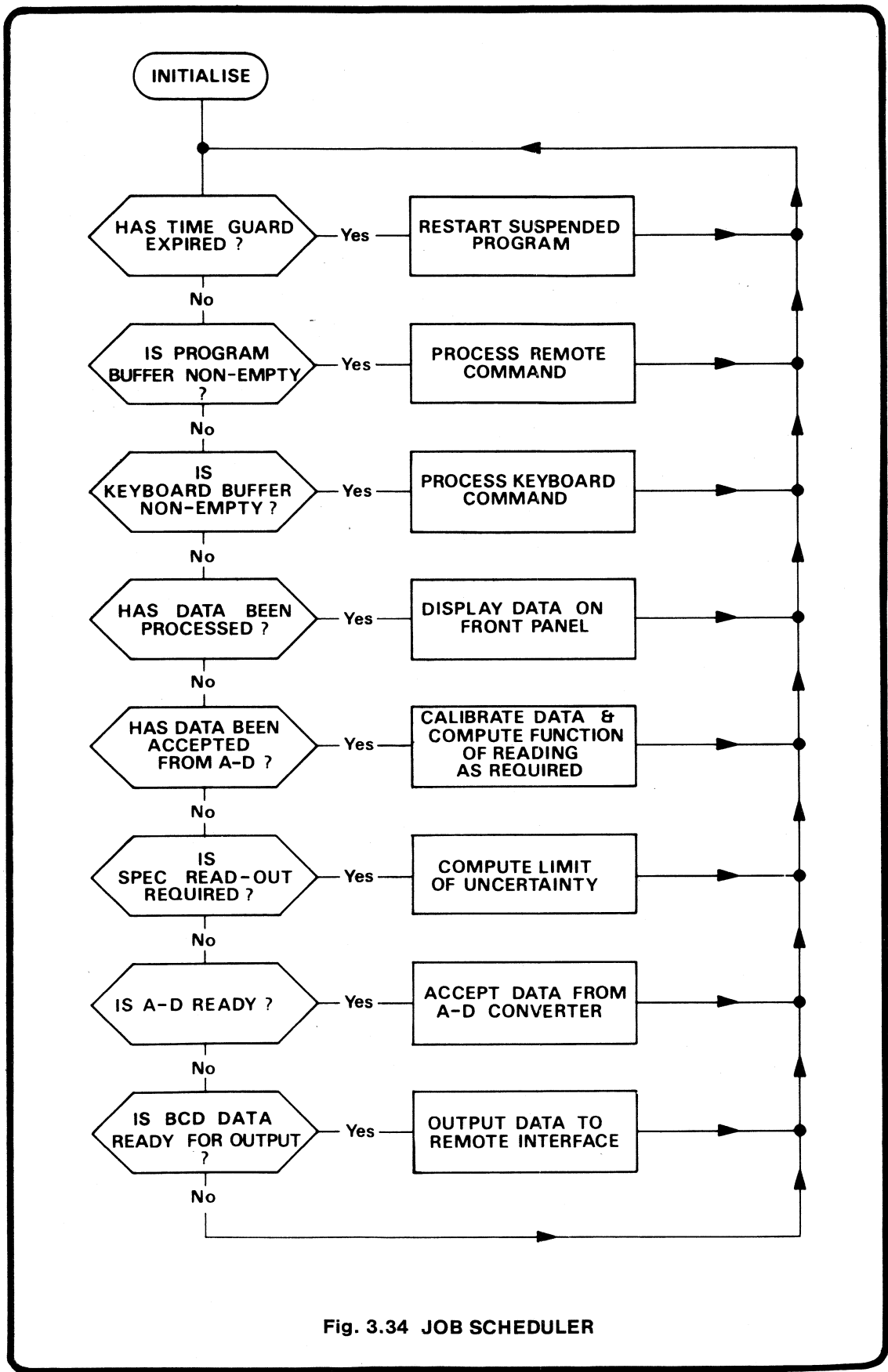


Fig. 3.34 JOB SCHEDULER

Data Control: Data handled by the system consists of a stream of measurement information on which a number of operations are carried out. A second stream, asynchronous with the first, consists of commands derived from the front panel or digital interface, controlling both the measurement circuits and computation programs. Operations on the measurement stream basically consist of acquiring the raw data from the A-D converter, calibrating this data and carrying out any other computations, and converting and formatting the data for output. Note that a job consuming data is given higher priority than the one producing data for it, allowing a producer to place data into an empty buffer. The consumer is activated by a flag, set by the producer to indicate data ready in the buffer.

Process Control: Control of the instrument by the processor, initiated from the front panel or digital interface, is arranged by using a 'pipeline control' of the major system state and a 'first in/first out' buffer between the interrupt level routine receiving the control command and the main program implementing it. The major system state consists of the range, function, resolution, filter, ratio, autorange, etc., flags and the computation mode (reading, A-B, ÷C, etc.). The pipeline comprises three levels. The top, level 1, reflects the state being programmed, the second, level 2, the state of the measurement circuits and the third, level 3, the measurement being processed. When a command is input, level 1 is updated (e.g. a new range is selected) and as soon as the measuring circuits are not converting an input signal, the state in level 1 is moved to level 2 causing the measurement circuits to update to the

new state. When an A-D conversion is complete, data is read from the A-D and the state transferred from level 2 to 3, providing information for the processing routines. Additionally, at this time, the level 1 to level 2 transfer is repeated and the measurement circuits again updated to allow for commands received while the conversion is in progress.

A second control mechanism used is to input all the commands via a 'first in/first out' buffer between the interrupt level routine receiving the command and the main program implementing it. Thus the processor under remote control is able to 'simultaneously' set up the requirements for the next reading, convert the current reading and process the last one.

3.7.1.2 The Two-Phase Clock

The 6800 requires a non-overlapping positive two-phase ($\phi 1, \phi 2$) clock and is derived from the crystal master clock (sheet 4) producing a 1.6MHz (50Hz supply) or 1.9MHz (60Hz supply) signal. M57 acts as a ÷2 thus antiphase 800kHz square-waves appear on pins 14 and 15. If data is not being transferred to the CMOS Bus, M57-11 is high, thus M56-8 follows M57-15. The non-overlapping of $\phi 1$ and $\phi 2$ is produced by the utilization of the inherent propagation delay (approx. 10nS) through each gate of M54 and M55. This is best seen by referring to Fig.3.35, the circuitry around the output stage increasing the voltage levels demanded by the processor (0V and +5V).

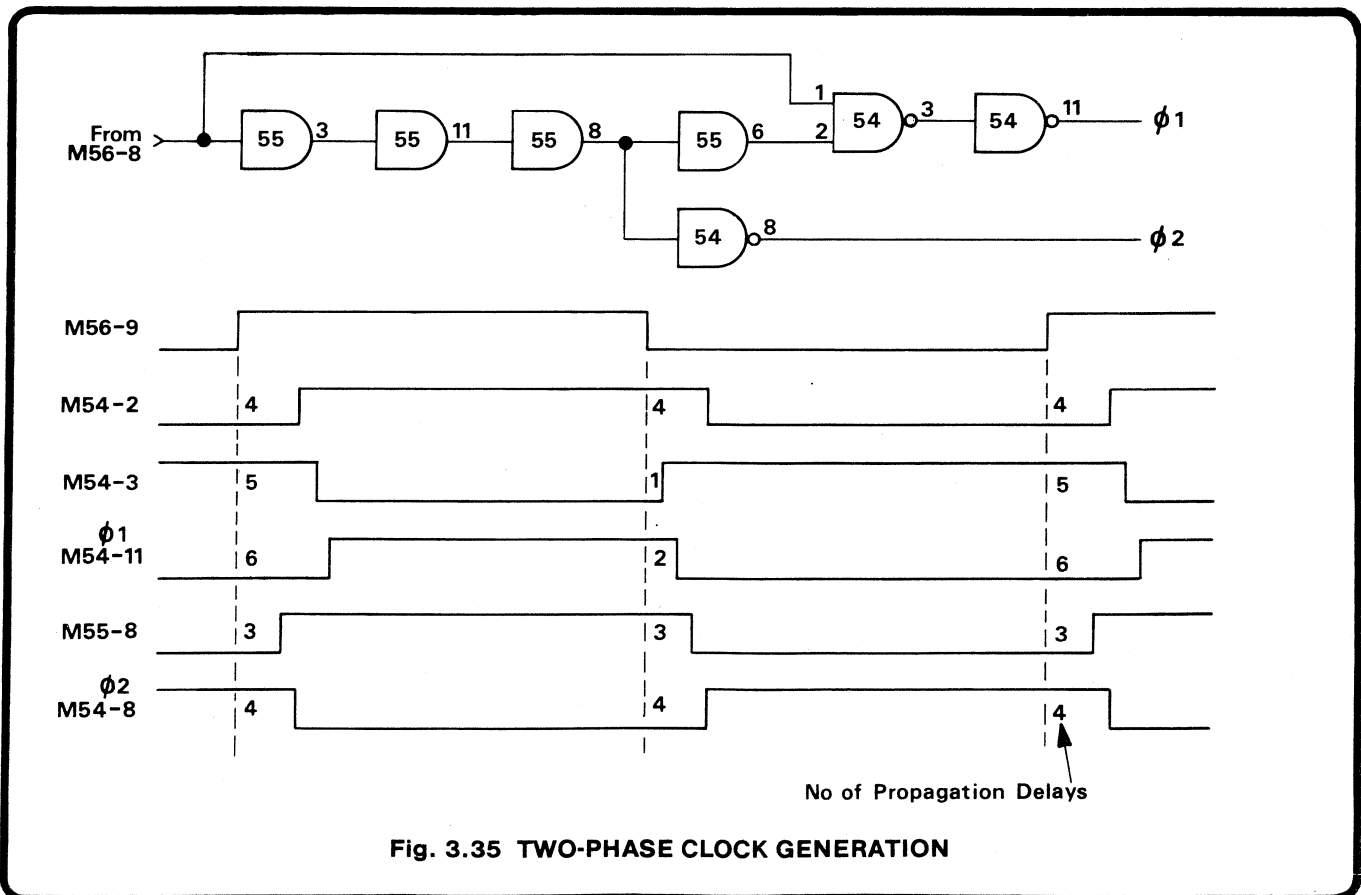


Fig. 3.35 TWO-PHASE CLOCK GENERATION

During a period when data is being transferred across the CMOS Data Bus, $\phi 1$ and $\phi 2$ are reduced to 400kHz by utilizing the other half of M57. The signal CMOS I/O is high thus a 400kHz square-wave is output on M57-11, the

wave-forms of $\phi 1$ and $\phi 2$ are altered such that one half of the period is stretched, covering $1\frac{1}{2}$ cycles of the normal 800kHz operation. (See Fig. 3.36).

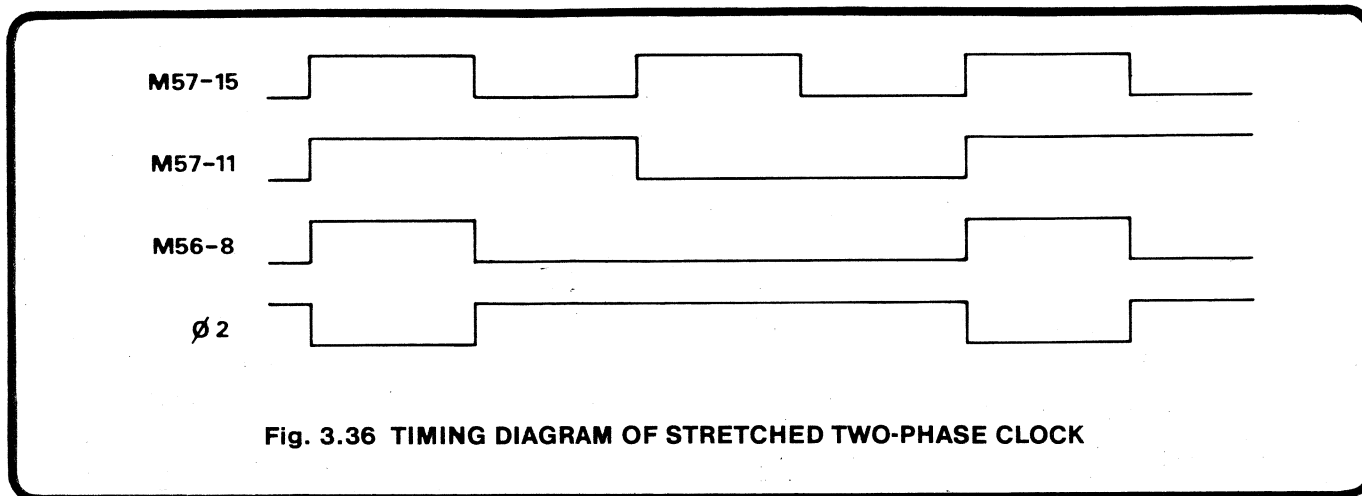


Fig. 3.36 TIMING DIAGRAM OF STRETCHED TWO-PHASE CLOCK

3.7.1.3 RAM/ROM Circuit

The 6800 uses 3 Read-Only Memory chips (ROMs) which contain the program necessary to run the instrument. Each ROM is able to store up to 4096, 8-bit 'bytes' of program information; grouped in program modules. The MPU accesses a byte by placing its address on the 16-bit Address Bus and driving the Valid Memory Address (VMA) line true (logic-1). The information held in that particular location is then sent back to the MPU via the Processor Data Bus.

The chip-select inputs for the RAM and ROM are decoded from a selection of high-order address bits. This selection determines the positions of the RAM and ROM in the memory map. For example: M30 is fed from A15.A13.A12 so that it covers the memory locations from #F000 to #FFFF (Note that since A14 is not decoded M30 also appears at #B000 to #BFFF).

The processor employs 1024 bytes of 8-bit wide Random Access Memory (RAM) made up from two 1024 x 4-bit RAMs (M31/M36). M31 and M36 are employed as operating memory for scratch pad operations and storing volatile data (e.g. Max, Min). The principal location of the RAM is from #0000 to #00FF. Since A8 and A9 are not decoded there are images starting at #0100, #0200, #0300.

A further 256 bytes of 8-bit wide RAM are made up from two 256 x 4-bit RAMs (M19/M20). M19 and M20 are backed up by a battery to provide the non-volatile 'Calibration' and 'Zero' memory. Three address bits A12, A14 and A15 are decoded by M33 (pin 8) to enable M19/M20; but M29 (pin 6) permits the memory contents to be changed only if CAL is selected, or if the ZERO section of the memory is addressed (A7 and A6 both at logic-1).

The read/write control line R/\overline{W} from the 6800 is gated with a 'Master Clock $\div 2$ ' signal to provide correct timing, and the address decodes include gating with VMA $\phi 2$.

An instrument power up is detected by M60/M62 causing an initialization RESET signal to be fed to the MPU via Q16. (See Fig. 3.38).

During a power-up or power-down (+5V supply line <+4.75V) a signal from the supply-level detectors prevents RAMs M19 and M20 from being overwritten by holding the CS (chip select) lines low (<0.2 volts) via Q14 for a period of approx. 25mS determined by R55/C32.

3.7.2 CMOS Address Decode and Input/Output Circuits (430526 sheet 2)

Information is transferred to and from CMOS devices via the CMOS Data Bus during periods when the signal CMOS I/O is at logic-1 (M33-6). CMOS I/O is addressed when A15.A14.A11 is true. This occurs when memory locations starting at #4100 (and its images) are selected. The transfer of data between the Processor Data Bus and the CMOS Data Bus takes place at 400kHz, the Read/Write lines selecting the direction of the information through the tri-state buffers M4, M5 and M6.

In order to address the various CMOS input/output devices, the address lines must be further decoded. M32 is a 1-of-10 decoder, providing 5 addressable drives; M16 is a dual 1-of-4 decoder addressing the front panel circuitry and the digital elements of the A-D converter. A summary of the decoded CMOS address signals is given in Fig. 3.39.

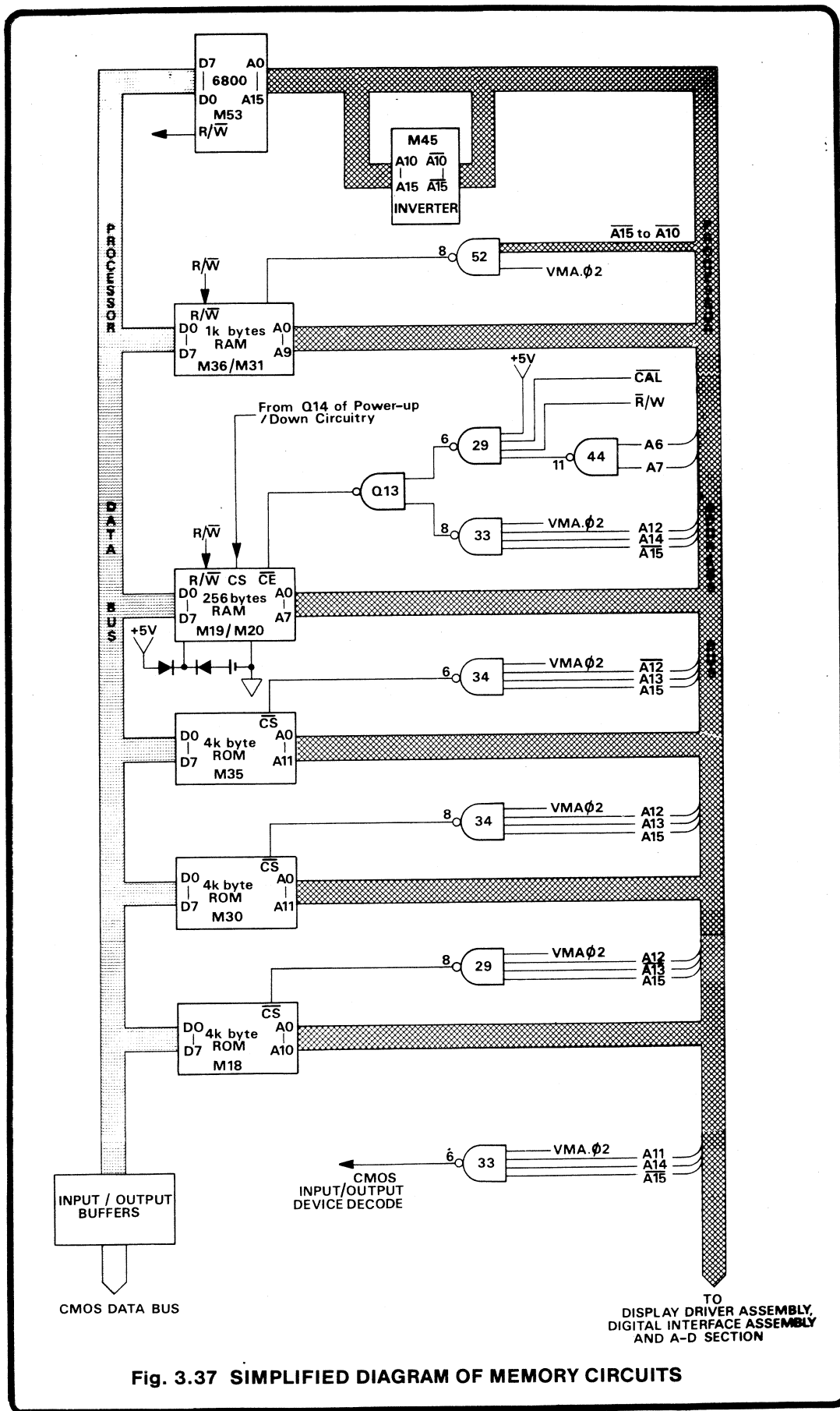


Fig. 3.37 SIMPLIFIED DIAGRAM OF MEMORY CIRCUITS

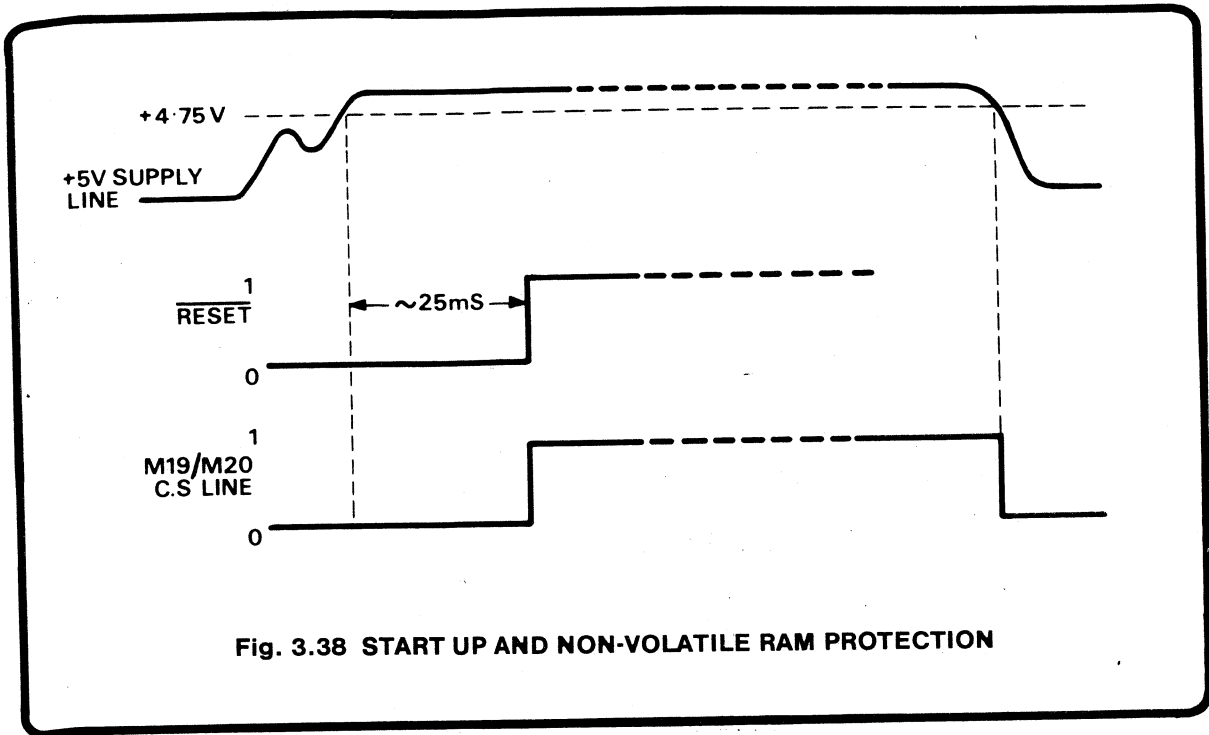


Fig. 3.38 START UP AND NON-VOLATILE RAM PROTECTION

A6	A5	A4	A2	A1	A0	SIGNAL	M32/M16 Pin No.	Operation
0	0	0	1	X	X	$\overline{\text{XKYBRD}}$	M32-2	Keyboard read/write
0	0	1	X	X	X		(M32-4)	Forces a MPU 'power up' sequence
1	0	0	X	X	X		(M32-11)	Triggers processor time guard (M43)
0	1	0	1	X	X	$\overline{\text{XADDT}}$	M32-6	A-D main counter output enable
0	1	1	X	X	X		(M32-9)	Analog interface address latch input enable
0	0	0	X	0	0	$\overline{\text{XKDSP0}}$	M16-7	} Addresses keyboard i.e.d. latches
0	0	0	X	0	1	$\overline{\text{XKDSP1}}$	M16-6	
0	0	0	X	1	0	$\overline{\text{XKDSP2}}$	M16-5	
0	0	0	X	1	1	$\overline{\text{XKDSP3}}$	M16-4	
0	1	0	X	0	0	$\overline{\text{XADSTA}}$	M16-9	A-D, and interrupt status output enable
0	1	0	X	0	1		M16-10	Error switch output enable
0	1	0	X	1	0	$\overline{\text{XADCTL}}$	M16-11	A-D control latches, input enable
0	1	0	X	1	1	$\overline{\text{XADDLY}}$	M16-12	A-D delay counter input enable

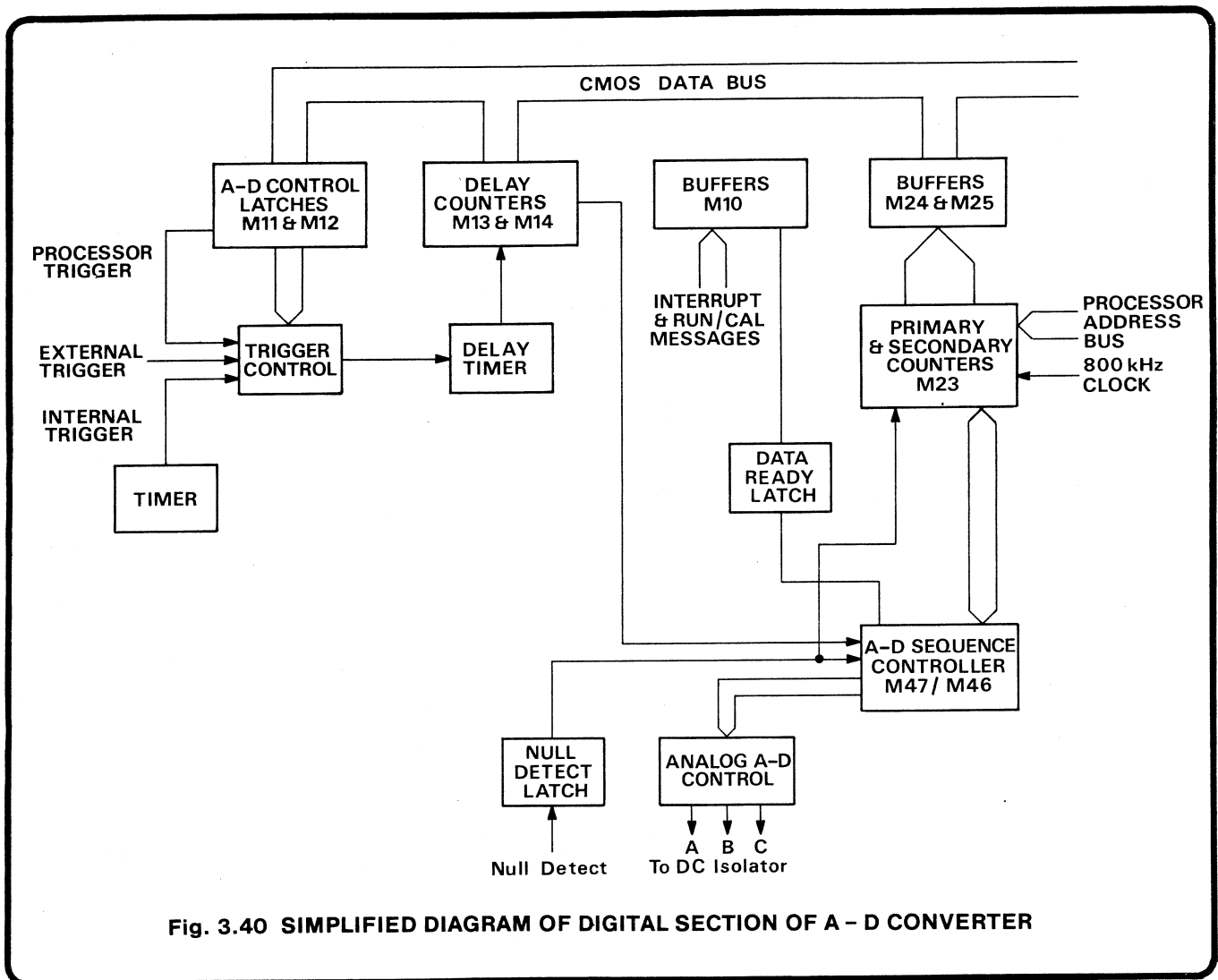
FIG. 3.39 CMOS ADDRESS DECODING

3.7.3 Analog to Digital Conversion (Digital Section)

3.7.3.1 General Principle

Block diagram Fig. 3.40 outlines the essentials of the digital section and should be used with flowchart Fig. 3.41 in order to follow the operation of this section.

The function of this section of the circuitry is to generate the sequence that when transferred to the analog section, controls the sequence from RESET through the integration cycle and back to RESET. The circuitry controls the length of SIG and BIAS and counts during REF 1 and REF 2, the accumulated count being proportional to the length of the reference periods, which in turn is proportional to the measured input signal. At the end of each reading cycle the count is read by the MPU, processed and displayed.



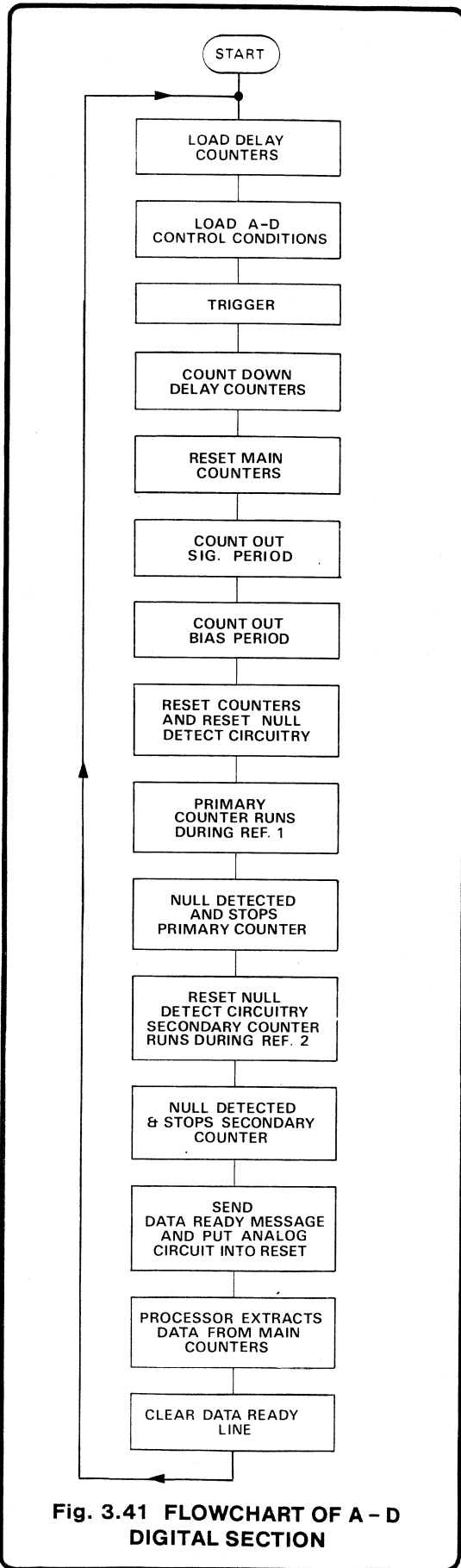


Fig. 3.41 FLOWCHART OF A - D DIGITAL SECTION

SIGNAL	\bar{A}	\bar{B}	C
RESET	1	1	0
SYNCH	1	1	0
SIG	1	1	1
BIAS	0	1	1
WAIT	0	1	1
REF 1	1	0	1
REF 2	0	0	1
END	1	1	1

FIG. 3.42 A-D ANALOG SEQUENCE CONTROL SIGNALS

3.7.3.2 Preset Procedure

As part of the initialization routine (at switch on), M47 (used as the sequence controller), is reset from M37-11, causing M47-2 to be logic '1'. Thus the control lines \bar{A} , \bar{B} and C put the analog section of the A-D into RESET (See Fig. 3.42). The Address Bus decoded signal \bar{XADDLY} is taken low, enabling the presetting of the delay counters M13 and M14 from the CMOS Data Bus, the amount of delay being determined by the selected range, function and filter state, see Fig. 3.43. The A-D control latches, M11 and M12 are then enabled by \bar{XADCTL} to (i) reset the command latch M1 (from M11-4), (ii) set the resolution of the main counter (M11-5 and 6), (iii) select trigger gate (M12-3, 4 or 5) and (iv) reset the data ready latch (M12-6).

FUNCTION	1081 COUNT	
	FILTER	FILTER
DC Volts	6	101
AC Volts	101	22
DC + AC Volts	101	22
PRT	6	101
10 Ω - 100k Ω	6	101
1M Ω	6	121
10M Ω	32	251

NOTE: With AC LF Filter in, a number (n) of delayed measurements follow EXT TRIG. The nth measurement is accepted as a valid reading for display. Value of n:

FILTER selection	10Hz	1Hz	0.1Hz
Measurements/Reading	8	50	550

FIG. 3.43 COMMAND DELAYS

3.7.3.3 A-D Measurement Sequence

Trigger. The trigger, required to initiate the measurement sequence, is generated from one of three possible sources:

1. Internally generated 2/second trigger, from timer M61-7.
2. Externally generated trigger, from EXT TRIG on rear panel via M24-13.
3. An MPU-derived trigger from M11-3 generated when auto-ranging, during calibration or a ZERO sequence, or via the digital interface.

The trigger source is selected by the latched data on M12, enabling one of the three gates of M2.

Delay. The trigger pulse clocks the 'command latch' M1 causing the timer, M15, to output clock pulses (100Hz) to the delay counters (M13 and M14) after a delay of approx. 1.5mS set by C5, R8, R9, R11. The delay counters proceed to count down to zero, at which time the delay latch (M26) is clocked. Thus M26-14 becomes a logic-0, enabling the sequencer M47 (an octal counter) to proceed on to the next step via M46-2.

SYNCH. The SYNCH phase from the sequencer resets the counters of M23 and places the analog section of the A-D into SIG. The pulse is fed back to M47 via M46-3 to step on the sequencer.

SIG. During the time the SIG line is at logic-1 (M47-3), the primary counter in M23 is enabled and counts out the signal period (160ms). At the end of this period M23-23 goes to logic-0, enabling M47-13 via M46-11, and stepping the sequence on to BIAS (FFWD/M47-7 to logic-1).

BIAS. The BIAS signal (M47-7) is transferred to the analog section of the A-D by changing the state of the \bar{A} line (M38-9 to a logic '0'). BIAS also enables the secondary counter of M23 to count out the BIAS period (160 μ s). The signal indicating the end of this period is passed via M46-9 causing the sequencer to carry on to the next step. The BIAS signal also resets the 'delay latch' (M26) ready for the next measurement cycle, and the 'null detector' latch (M22A).

WAIT. The WAIT pulse resets the counter of M23 via M39-10, keeps the \bar{A} line to the analog section low, clocks the polarity null detect latch M22(B) causing a logic '1' on pin 1 if the signal applied to the analog section of the A-D converter was positive (logic '0' if negative) and is fed back to enable the sequencer via M46-3.

REF 1. The high to low edge of WAIT causes the \bar{A} to change state and going into REF 1 makes \bar{B} a logic '0'. The analog side is then in the condition to start 'ramping down'. While REF 1 is high the primary counter of M23 is enabled (pin 3) and counts the period of REF 1.

REF 1 is ended when a null detector pulse is detected and latched on to M22. This causes the sequencer to step on once more from M46-3, the low to high edge from pin 4 disabling the primary counter.

REF 2. The REF 2 signal changes the state of the \bar{A} line (causing the analog section to ramp down at a slower rate), resets the 'null detect' latch and enables the secondary counter of M23 (Pin 13) to count the period of REF 2. If the secondary counter overflows the primary counter is incremented from M23-16.

As in REF 1, a null detector pulse causes the counting period to end (M22-12) and increment the sequencer via M46-3 causing the \bar{A} and \bar{B} lines to change state.

END. The low to high edge from M47-10 is fed back to M47, via M48-6 giving a master reset. Thus the sequencer is placed into RESET.

RESET. The sequence pulse from M47-2 clocks the 'data ready' latch M1-3 placing a signal on to the CMOS Data Bus via tri-state buffer M10 indicating to the MPU that a reading is ready to be taken from the main counter M23. Data is extracted from the counters in three bytes (controlled by the A1 and A0 lines of the processor address bus) with the counter output buffers, M24 and M25 being enabled by \bar{XADDT} , a decoded processor address.

The RESET signal is also passed to the analog section of the A-D by changing the state of the C line.

Once the data has been extracted from the main counter the set-up procedure is then repeated to await a further trigger.

3.7.3.4 Master Clock (430526 sheet 4)

The master timing element of the instrument is a crystal controlled Colpitts oscillator. The crystal is chosen to be a binary multiple of the supply frequency to provide an oscillator output of 1.6384MHz (50 or 400Hz supply) or 1.96608MHz (60Hz supply).

3.8 FRONT PCB ASSEMBLY (Circuit Drawing No. 430294)

The Front pcb assembly accepts the input signals, digitally displays the value, provides manual control of the measurement circuits and data conditioning; and gives a visual status indication of the selectable Instrument states.

3.8.1 Analog Input Signals (430294 sheet 2)

Signals applied to the front panel input terminals are routed directly to the rear panel pcb along two cables. The first takes the Hi and I+ lines and the second takes the lines: Lo, I- and Ω 's Guard. Both cables are screened by front panel Guard.

KEY	M7				KEY	M10			
	14	15	16	17		14	15	16	17
	CD7	CD6	CD5	CD4		CD3	CD2	CD1	CD0
100	0	0	0	0	SIG	0	0	0	0
10	0	0	0	1	REF	0	0	0	1
1000	0	0	1	0	Δ	0	0	1	0
10M Ω	0	0	1	1	RATIO %	0	0	1	1
1	0	1	0	0	(A-B)	0	1	0	0
.1	0	1	0	1	HI RES	0	1	0	1
10 Ω	0	1	1	0	\div C	0	1	1	0
AUTO	0	1	1	1	MAX	0	1	1	1
DC	1	0	0	0	MIN	1	0	0	0
k Ω	1	0	0	1	RESET	1	0	0	1
KEYBOARD	1	1	0	1	HOLD	1	0	1	0
PRT	1	1	1	0	FILTER	1	1	0	1
ZERO	1	1	1	1	AC	1	1	1	1

FIG. 3.44 CMOS DATA BUS : KEY SELECT CODING

The front panel pcb connects the front panel input terminals to the 2-4 wire and Local-Remote switches. Thus I+ and I- are wired to the 2-4 wire switch through thermistors R1 and R2 for connection to Hi and Lo if required. Similarly, Ω 's Guard and Guard may be shorted via the Local-Remote switch.

3.8.2 Display Signals (430294 sheet 1)

The front panel pcb routes the display signals from the Display Driver assembly to the plasma display.

3.8.3 Keyboard Data Encode (430294 sheet 1)

Selection of a front panel keyswitch causes one of the two 16-key encoders (M7 or M10) to send a data available message to M2 (a data latch) and to remember which key was pressed. The output of M2, (pin 1 or 13) signals the interrupt circuitry of the Digital Board (IRQK1 or IRQK2).

When the microprocessor accepts the interrupt and has located the source, the XKY BRD line to pin 13 of M7 and M10 is taken low, enabling the data outputs of the encoders to be placed on to the CMOS data bus (See Fig. 3.44 for the key select coding). This signal also resets M2 ready for the next key selection.

CMOS DATA LINE	M12/M11	M8/M5	M6/M4	M9
CD0	\div C	DC	AUTO	
CD1	HI RES	k Ω	10 Ω	
CD2	RATIO %	ZERO	.1	
CD3	Δ	FILTER	1	
CD4	A-B	KEYBOARD	10	
CD5	MIN		100	HOLD
CD6	MAX	PRT	1000	REF
CD7	RESET	AC	10M Ω	SIG

FIG. 3.45 CMOS DATA BUS : LED-SELECT CODING

3.8.4 Keyboard LED Data Decode (430294 sheet 1)

The $\overline{\text{XKYBRD}}$ signal is inverted by R6, R7 and Q1 to enable the LED data latches. These are divided into the four sets: M4/M6, M5/M8, M11/M12, M9; each set being addressed by one of the $\overline{\text{XKDSP}}$ lines.

On initialization or after a change of the instrument's selectable states, the LED data latches are updated by placing data on the CMOS Data Bus (see Fig. 3.45) while addressing the appropriate set of data latches (eg. XKDSP1 addresses M5/M8); then clocking from the CMOS CLK line (J2-6).

The outputs of the LED latches provide the signals to the bases of the LED drive transistors, switching them on or off as required.

3.9 DISPLAY DRIVER ASSEMBLY (Circuit Diagram No. 430301)

Basically, the Display Driver assembly receives the display information from the microprocessor (running at 800kHz) and stores it in a Random Access Memory (RAM) digit by digit. This data is then read out at a slower

frequency (2kHz), level shifted and output to the gas discharge display.

NOTE: In the following description, each bar, decimal point or legend is referred to as a display segment and each set of segments i.e. \pm , \square or a legend block, is referred to as a display block.

3.9.1 Write Mode

On completion of a reading or when certain modes are selected, (e.g. SPEC, keyboard entry), the processor indicates to the Display Driver Board that data is ready to be transferred by the signal XDDSP (TP6). This causes the RAM (M1) to be placed into its write mode and the quadruple 1-to-2 data selector, M9, to select the 'B' inputs which are connected to the processor Address Bus.

The signal XDDSP also causes the tri-state buffers M6 and M7 to become enabled, causing the data input lines of the RAM to be connected to the processor data bus. Thus under MPU control, the display data (\pm , \square 's, decimal points, legends and commas) are written into the RAM.

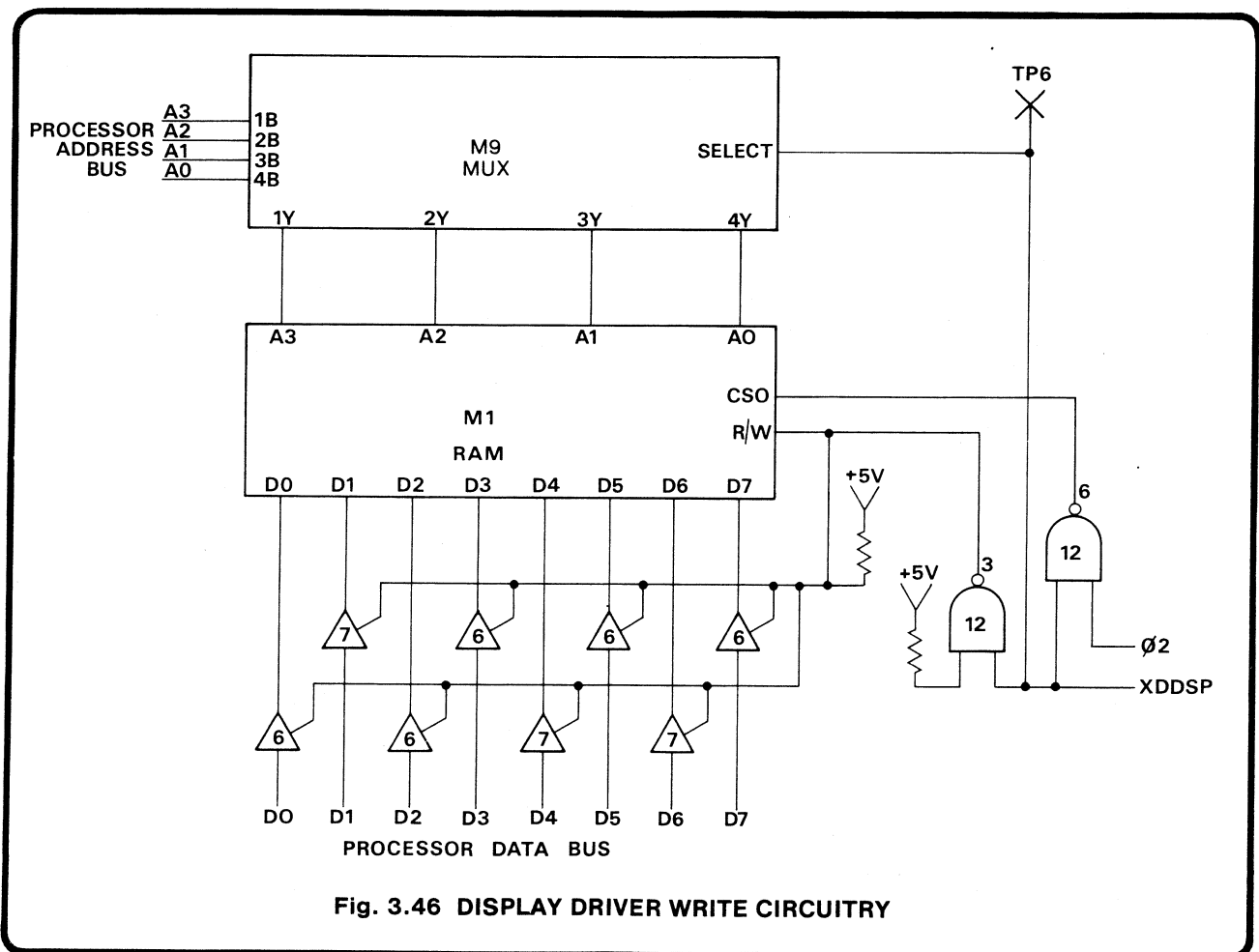


Fig. 3.46 DISPLAY DRIVER WRITE CIRCUITRY

COUNTER (M8)				RAM (M1)				COMMA MULTIPLEXER (M10)				Display block energized or operation implemented from M11
Q ₃	Q ₂	Q ₁	Q ₀	A ₃	A ₂	A ₁	A ₀	INHIBIT	C	B	A	
0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1	0	0	0	1	3
0	0	1	0	0	0	1	0	0	1	0	0	5
0	0	1	1	0	0	1	1	0	0	1	0	7
0	1	0	0	1	1	0	0	0	1	0	0	9
0	1	0	1	1	1	0	1	0	1	0	0	11
0	1	1	0	1	1	1	0	0	1	1	0	} Load comma data
0	1	1	1	1	1	1	0	0	1	1	0	
1	0	0	0	0	0	0	1	0	0	0	1	2
1	0	0	1	0	0	0	1	1	0	0	1	4
1	0	1	0	0	1	0	1	0	1	0	1	6
1	0	1	1	0	1	1	1	0	1	1	1	8
1	1	0	0	1	1	0	0	1	0	0	1	10
1	1	0	1	1	1	0	1	1	0	1	1	Reset Counter

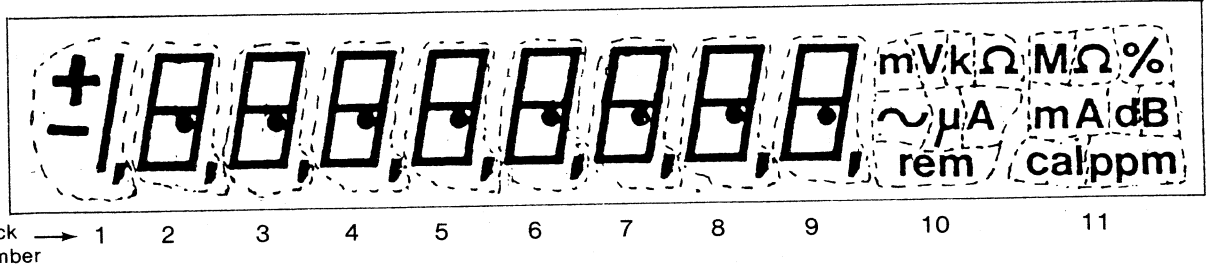


FIG. 3.47 DISPLAY DRIVER READ MODE ADDRESS STATES

Once this transfer of data is complete, signal XDDSP reverts to logic-0 selecting the read mode of the RAM. The buffers return to their open-circuit state, isolating the RAM Data Bus from the main Processor Data Bus.

3.9.2 Read Mode

A multiplexed display is normally scanned from left to right, driving each anode in turn and providing the appropriate segment information to the cathodes. For this type of display, however, adjacent anodes should not be activated consecutively, as this can cause inter-block 'streaming'. Thus the 1081 employs two scans per cycle: the first for odd numbered blocks, the second for even.

The free running clock M13, R3, R5, C16, produces a 2kHz signal (M13-9) to drive a 4-bit binary counter, M8, which provides the control of the address lines in the read mode (See Fig. 3.48). The display block selection is achieved by decoding these 4 lines into 16 bits using M11. The output lines of M11 are connected to the bases of transistors Q1-Q3, Q13-Q20 which act as anode switches. Note that when the address lines are in the state 0000 the output of M11 (pin 11) selects the anode to block 1; 0001

selects the anode to block 3 (M11-9); 0010 ... block 5, etc., thus the display blocks are selected alternately.

To select the appropriate segment data from the RAM to match the display block selection the address lines are given a left hand bit rotation i.e. if the output of M8 is labelled DCBA, (2³, 2², 2¹, 2⁰), the address input of M1 would be CBAD. (Fig. 3.47 gives the state of the address lines for each display block). The particular display block segment data is recalled by the RAM, buffered by M4 and M5, level shifted -180 volts by R8-R15, C4-C11 causing Q5-Q12 to drive the cathodes, D4-D11 acting as restoration diodes. Between the transfer of each set of segment data, M13-3 is taken high, causing the outputs of M4 and M5 to be a logic '0'. This produces a refresh period for capacitors C4-C11 to discharge from the -180V supply through the restoration diodes. Each 'E' display block consists of 7 'digit bars', a decimal point and a comma, thus a total of 9 bits is needed to drive the block. As the 680C series only has an 8 bit wide data bus, the comma information is treated as extra word. When the RAM is in its write mode, the last byte transferred from the processor is the comma information (8 bits for segments 1 to 8, See Fig 3.48).

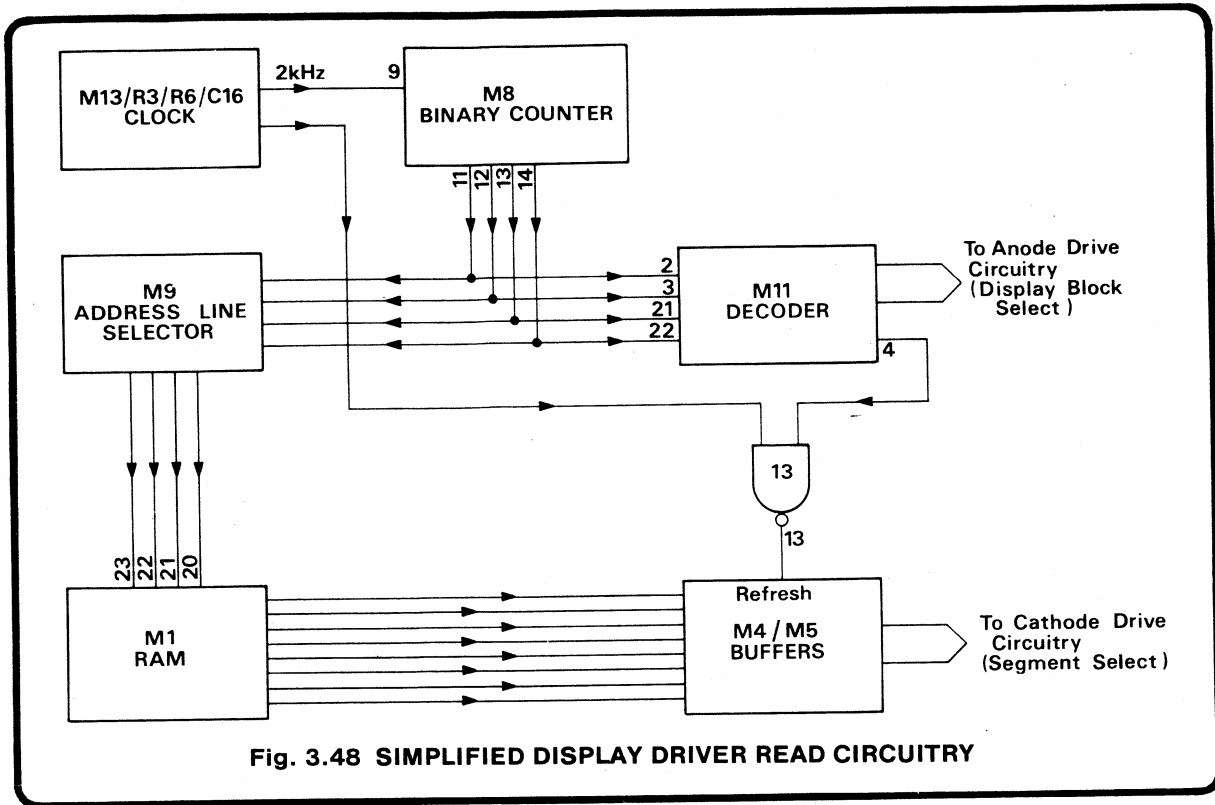


Fig. 3.48 SIMPLIFIED DISPLAY DRIVER READ CIRCUITRY

In the read mode the comma information is transferred from the RAM to latches M2 and M3 (Fig. 3.49) when the RAM address is 1110. So that this information is not sent to the cathodes of the display (it would constitute a display segment combination under the normal cycle), it is inhibited from passing through M4 and M5 by the decoder (M11-4). The previous signal from M11 (pin 5) is delayed by R6, D2, C2 such that when it reaches pin 7 of M2 and M3 it is coincident with that from M11-4, clocking the

comma data on to the latches. M2/M3 outputs are permanently enabled, so the comma data is transferred to the 'X' inputs of 8-channel selector M10. As M10 is under the control of block counter M8, it multiplexes the comma data to coincide with activation of the corresponding block anode. M10 'Z' output is passed via M13 and Q4 to the comma segment (i) line, subject to inter-block refresh by M13-13 as for M4/M5.

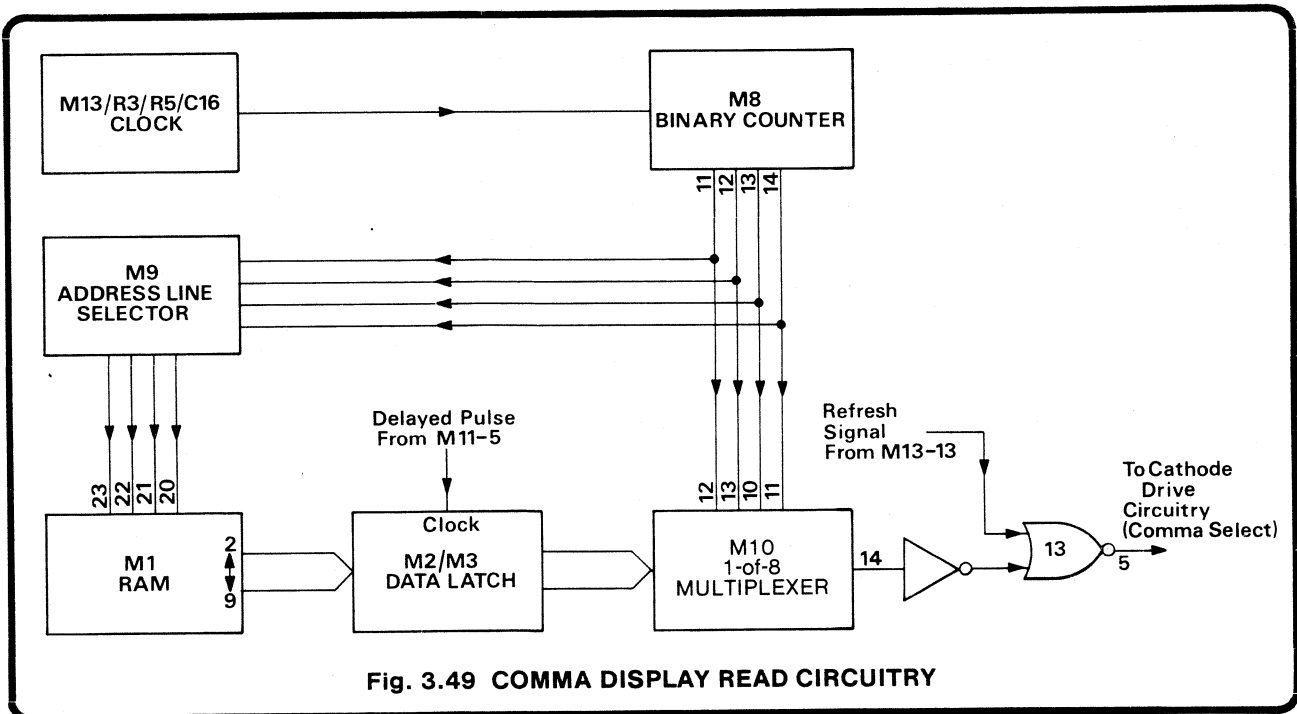


Fig. 3.49 COMMA DISPLAY READ CIRCUITRY

3.10 IEEE 488 STANDARD DIGITAL INTERFACE (Circuit Diagram No. 430427)

The IEEE Digital Interface assembly contains the extra memory circuitry required for the execution and decoding of interface functions, and for data input and output transfers. Simplified diagram Fig. 3.50 shows its essential features.

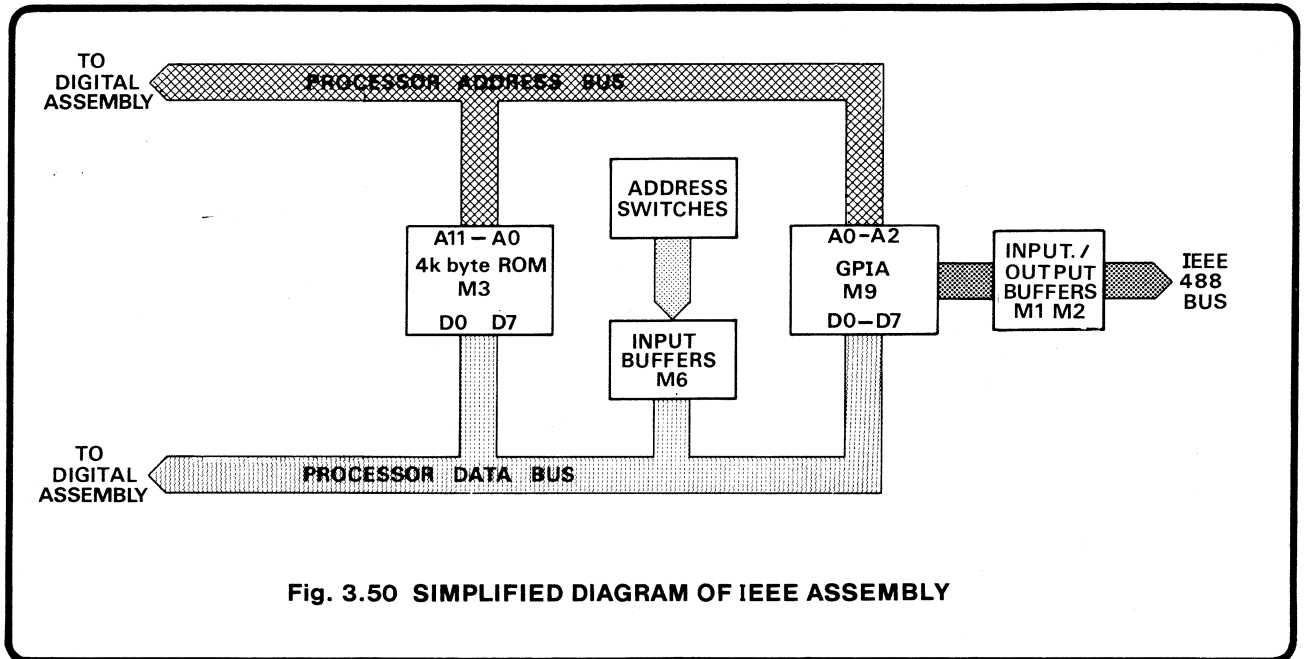


Fig. 3.50 SIMPLIFIED DIAGRAM OF IEEE ASSEMBLY

3.10.1 ROM Circuit

The IEEE Digital Interface assembly acts as an extension to the Digital assembly with connections to both the Processor Address and Data Buses. The board houses 4k bytes of program memory (M3) containing the sub-routines to control the instrument from the IEEE 488 Bus. The ROM receives the address information, with chip selection being made by decoding address lines A3-A11 with XIOBD and master clock $\phi 2$.

Service Request
Parallel Poll
Device Clear
Device Trigger

With the MPU it is also capable of:-
Programmable Interrupts
Storing the instrument's address
Control of the interface input/output buffers.

3.10.2 Interface Circuit

The General Purpose Interface Adaptor (GPIA), M9, provides the interface between the IEEE 488 Standard Instrument Bus and the 6800 microprocessor. The MPU can receive, process and send messages to the interface through the GPIA.

The GPIA is selected by decoding address lines A3-A11 with XIOBD. Address lines A0-A2 with the state of the MPU R/W line select one of the 8 read only or 7 write-only registers in the GPIA, enabling the MPU to send or receive data over the interface.

The GPIA is able to automatically handle the following interface protocol^[1]:-

Single address capability
Source and acceptor handshake
Talker and Listener states

The two signals $T/\bar{R}1$ and $T/\bar{R}2$ are used to control low power transceivers (formed from M1, 2) which drive the interface bus.

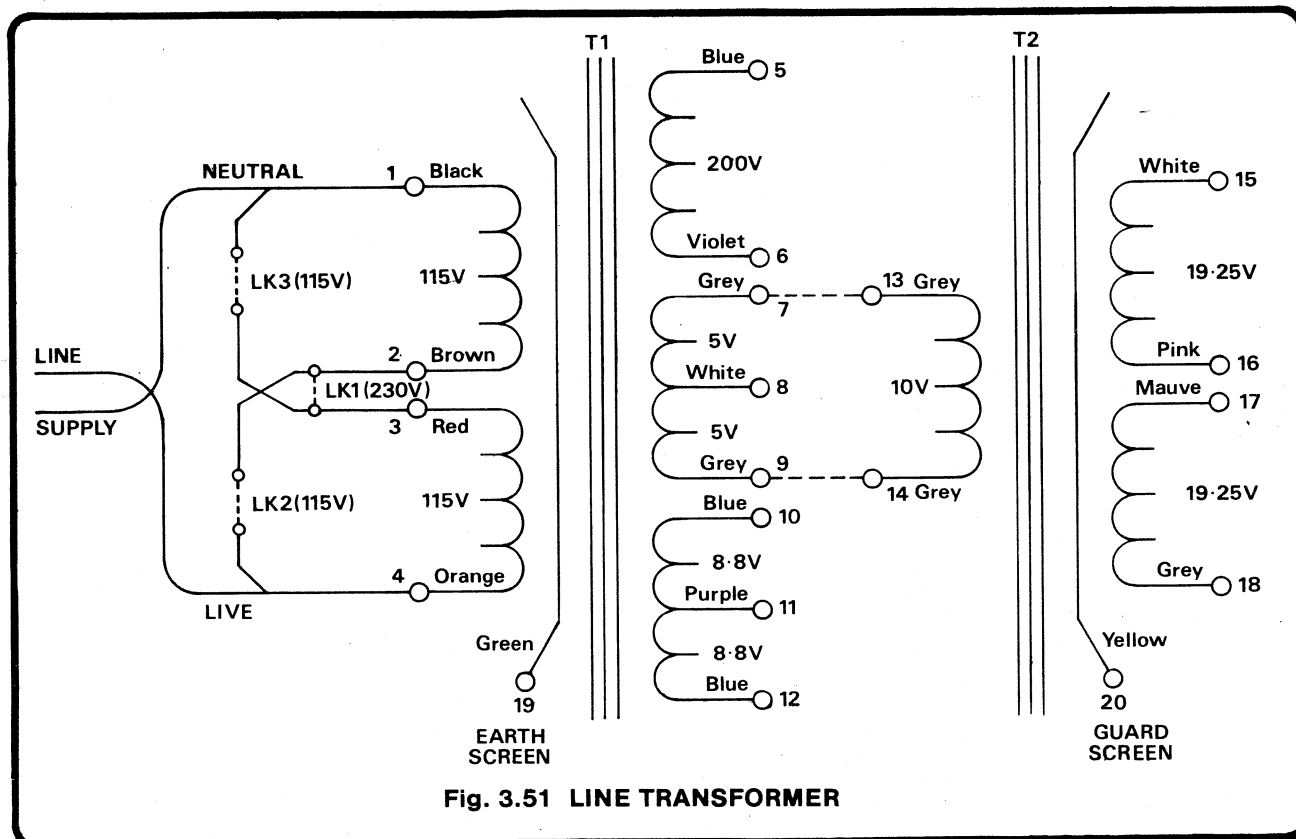
[1] For further information refer to 'Getting aboard the 488 Bus' published by Motorola.

3.11 REAR (POWER SUPPLY) ASSEMBLY (Circuit Diagram No. 430295)

3.11.1 General

The line transformer and power supply components are situated at the rear right hand side of the instrument, when viewed from the front. Transformers T1 and T2 are of toroidal construction mounted one on top of the other and bolted to the rear panel. T1 has a split primary comprising two 115V windings, intended for either series or parallel

connection depending on the line voltage. An earth screen is interposed between primary and secondary windings to minimise electrostatic coupling, and is grounded to line ground. The second transformer T2 is driven from T1. It also possesses an electrostatic screen, this time being connected to Guard.



3.11.2 180V supply

The 180V supply is required for the plasma display. The 200V AC output from the secondary of T1 is full-wave rectified by W1 and smoothed by C6. R6/D3 form a 6.8V reference so that Q2/R4 becomes a constant current sink of approx. 14mA. Shunt regulator D4/Q1 maintains 180V between J1-5 and J1-2. J1-5 is referenced by direct connection to the digital +5V line in the Display driver assembly.

3.11.3 5V supply

All the logic circuitry to the right of the instrument's central pcb is powered from the supply generated by the two 8.8V, 750mA secondary windings on transformer T1. The center-tap (digital common) is connected to line ground. D1 and D2 form a bi-phase bridge applying a full-wave rectified supply to reservoir capacitor C7. The 5V regulator is referred to R2 rather than ground so that the 5V rail can be accurately set. Feedforward capacitor C8 improves the effective ripple rejection of M1.

3.11.4 $\pm 15V$ Supply

The output of the third secondary winding of transformer T1 (10V AC) is input to the primary of T2. The two 19.25V outputs are connected in series, with the centre tap connected to analog common. The output of bridge rectifier W2 is fed to voltage regulators M2 and M3, to produce positive and negative 15 volt supplies to power the analog circuitry. These regulators also include foldback current limiting and thermal shut-down, to provide short-circuit protection.

3.12 SELF TEST SEQUENCE

Selection of the \rightarrow key then the TEST key places the instrument into a test routine, checking the display and basic measurement circuits. A flowchart for the routine is given in Fig. 3.52. The analog circuitry conditions for each test are given in the last subsection of the circuit description for the particular assembly. The Range FET patterns are listed in Appendix 1.

SECTION 4

INTERNAL ADJUSTMENT PROCEDURES

4.1 CHANGING LINE VOLTAGE AND LINE FREQUENCY

The instrument is set to 50Hz, 205V to 255V supplies unless Option 80, 81 or 82 is specified. This information is carried on the instrument identification label located on the rear panel. Alteration to a different line voltage/line frequency may necessitate an instrument recalibration.

4.1.1 Changing Line Voltage

1. Disconnect power and all signal input/output leads.
2. Remove the lower cover.
3. Locate the link(s) connecting the split primary on the printed circuit board in front of the toroidal mains transformer, Fig. 2.1 and Drawing No 400295.
4. 115V Operation:- Remove LK1 (link 1) and fit LK2 and LK3^[1].
230V Operation:- Remove links LK2 and LK3, and fit LK1^[1].
5. Amend instrument identification label.
6. Replace lower cover.
7. Replace power fuses with 160mA anti-surge (230V) or 500mA anti-surge (115V).
8. Carry out the Specification Verification tests (Section 8, User's Handbook) and recalibrate if necessary.

4.1.2 Changing Line Frequency

1. Disconnect power and all signal input/output leads.
2. Remove the top cover.
3. Change X1, C23, C24 on the Digital assembly (Drawing No. 400526) to the values shown below.

50/400Hz	Datron Part Number	Description
X1	800020	1.6384MHz crystal
C23	130059	470pF 500V Ceramic Disc
C24	130015	120pF 160V Polystyrene

60Hz	Datron Part Number	Description
X1	800021	1.96608MHz crystal
C23	102331	330pF 500V Ceramic Disc
C24	130006	82pF 160V Polystyrene

^[1] Links should be 22 SWG TIN.Cu wire with silicone rubber sleeving.

4. Amend Instrument identification label.
5. Replace top cover.
6. Carry out the Specification Verification tests (Section 8, User's Handbook) and recalibrate if necessary.

4.2 BATTERY REPLACEMENT

The battery should be replaced on or before the date indicated on the rear panel instrument identification label. To retain the calibration memory; the instrument must be powered-up during replacement. Therefore great care must be taken due to voltages up to 260 volts being present inside the instrument.

1. Remove top cover and locate battery on the Digital assembly (see Fig. 2.1).
2. Power-up instrument.
3. Desolder battery at end of tags and remove from clip.
4. Replace with new battery, (Datron Part No. 930049) positive terminal to resistor.
5. Replace top cover.
6. Amend instrument identification label (Current date +5 years).
7. Carry out the Specification Verification tests (Section 8, User's Handbook) and recalibrate if necessary.

4.3 POST-REPAIR PROCEDURES

Most integrated circuits and semiconductor devices used in the 1081 are manufacturers' standard products. Two exceptions, available only from Datron, are:

RMS Module (M11 on AC assembly)
Programmed ULA (M23 on Digital assembly)

During manufacture certain resistors are selected in value (FSV = Factory Selected Value) to accommodate circuit component tolerances, or to bring the desired setting of the preset control to the center of its adjustment range.

To achieve the high performance of the 1081, some critical devices have been selected for low leakage, high speed or low noise etc., and are marked with a paint spot. Therefore any replacements for these parts should be ordered from Datron stock.

NOTE:

A routine calibration as detailed in Section 1 should be carried out after completion of the following procedures.

WARNING:

Up to 260 volts is present inside the instrument. Personal contact with this voltage may result in injury.

4.3.1 Basic DC Instrument

Equipment Requirements:

5½ digit Digital Voltmeter e.g. Datron 1065, 1061
 Variable 5V, 1 amp DC supply
 5mV/division Oscilloscope e.g. Telequipment D83
 DC Voltage Calibrator, e.g. Datron 4000 or 4000A
 Shielded 10M Ω resistor in parallel with 10nF capacitor,
 e.g. Datron part No. 400392.

Procedure:

Power Supplies

1. Turn instrument on and allow 30 minutes warm-up period.
2. Connect DVM Hi to TP8 and Lo to TP28 on the Digital Board. Adjust R2 on the Rear (Power Supply) pcb assembly to give +5.100V \pm 25mV.
3. Connect DVM Hi to TP1 and Lo to TP23 on the Analog assembly. Adjust R7 on the Rear (Power Supply) pcb assembly to give +15.000V \pm 15mV.
4. Connect DVM Hi to TP2 and Lo to TP23 on the Analog assembly. Adjust R12 on the Rear (Power Supply) pcb assembly to give -15.000V \pm 15mV.

Digital Assembly

5. Switch the instrument off and disconnect the power lead.
6. Isolate the Digital assembly by removing the connectors along the centre panel (J1-J5).
7. Connect variable 5V supply and DVM Hi's to TP8, Lo's to TP28. Reduce supply to 4.750 \pm 10mV.
8. Set R83 fully clockwise. Connect oscilloscope Lo to TP28 and monitor M53 pin 40. Turn R83 anti-clockwise until TP30 undergoes a high to low transition (or begins to pulse low).
9. Remove variable supply and reconnect items disconnected in steps 5 and 6. Disconnect the oscilloscope. Switch on the instrument.
10. Connect DVM Hi to battery positive terminal, Lo to TP28. Check battery voltage is >2.5 volts.
11. Disconnect DVM and connect oscilloscope Hi to TP25, Lo to TP28. Adjust R11 to give a 10mS \pm 1mS period, mark-space ratio 3.5 : 1.5. (NOTE. This signal appears in short 'bursts' every reading.) Disconnect oscilloscope.

CAUTION:

The next sequence of operations (12, 13 and 14) clears the whole calibration memory, so all previous calibration information is lost. DO NOT carry out these operations unless one or more Cal. Stores is at one end of its span. (e.g. IP-0 or FAIL has been displayed.)

12. Insert calibration key into keyswitch on the back panel and turn, placing the instrument into CAL mode.
NOTE: The display CAL legend will be lit.
13. Short together pins 'D' and 'E' on Digital assembly.
NOTE: All the calibration store correction factors are now reset to zero.
14. Turn the calibration key back to RUN mode.

Analog Assembly

NOTE.

- Before carrying out operations (15) to (19), ensure that the instrument has warmed up with covers on for at least 2 hours.
15. Select DC, 1V and FILTER; apply short copper link across input terminals, and connect DVM Lo to TP23, Hi to TP34. Adjust bootstrap offset R160 to reduce the voltage at TP34 to <20 μ V. Disconnect the DVM.
 16. Apply short-circuit input and press 1081 ZERO key. Repeat until display reading is .000,000 \pm 1 digit.
 17. Connect shielded 10M Ω resistor across the Hi and Lo input terminals. The display reading is the input bias current to a resolution of tenths of a picaAmp (e.g. .000,125 represents a bias current of 12.5pA). Adjust R159 to null this reading.
 18. Repeat (16) and (17) until the bias current is <10pA.
 19. Repeat (15), (16) and (17) until the bootstrap and bias current are both within the specified limits without further adjustment.
 20. Replace covers but do not replace screws. Apply short-circuit input. Select 1000V DC range and deselect FILTER. Turn rear panel keyswitch to CAL mode and select LIN.
 21. Select 10V DC range and FILTER. Press ZERO.
 22. Remove input short. Apply +10V DC to the input terminals. Press STD, repeating until display reading is +10.00000 \pm 1 digit.

Important Note

[Operations (23) to (35)]

The basic linearity of the 1081 DC analog circuitry is of such a high order, that it is dependent on the nature and degree of compensation applied to adjust the dielectric absorption of the main A-D integrator capacitor C9. This is done on the 10V range using FSV resistor R85 at +19V, and trimmer R23 at +2V.

The calibration source used by the manufacturer to provide the test voltages, is itself of very low noise and excellent linearity. If a Datron 4000 or 4000A is not available, any calibration source used to provide test voltages must have less than 0.5ppm of noise, and be linear to better than 0.5ppm of range. Otherwise there is little point in testing or adjusting the 1081 linearity.

Before any linearity tests, or adjustment of R23 or R85, the instrument must be warmed up with covers on for at least 2 hours. For adjustment, the top cover should be lifted for as little time as possible.

IF THE LINEARITY IS SUSPECT, AND THE ABOVE CONDITIONS CANNOT BE MET, DO NOT CARRY OUT OPERATIONS (23) TO (35). IT IS RECOMMENDED THAT THE 1081 BE RETURNED TO YOUR DATRON INSTRUMENTS SERVICE CENTER FOR TEST AND ADJUSTMENT.

23. Apply +19.000,000 volts to the input terminals and select HI RES. If the displayed reading is within the limits +18.999,980V and +19.000,020V, omit operations (24) to (34).
24. Read the Important Note above. Unsolder R85 and clean out its terminal posts. When the instrument is fully warmed up again, proceed to operation (25).
25. Reapply +19.000,000V (HI RES selected). Select values of R85 until the displayed reading is +19.000,000V \pm 20 digits.
26. Apply 0.000,000V and press ZERO. Repeat until the reading is 0.000,000V \pm 5 digits.
27. Apply +10.000,000V and press GAIN. Repeat until the reading is +10.000,000V \pm 5 digits.
28. Repeat operations (25) to (27) until no further reselection of R85 is necessary.
29. Apply +2.000,000V (HI RES selected). Adjust R23 until the displayed reading is +2.000,000V \pm 20 digits.
30. Apply 0.000,000V and press ZERO. Repeat until the reading is 0.000,000V \pm 5 digits.
31. Apply +10.000,000V and press GAIN. Repeat until the reading is +10.000,000V \pm 5 digits.
32. Repeat operations (29) to (31) until no further adjustment of R23 is necessary.
33. Repeat operations (25) to (32) until no further reselection of R85, nor adjustment of R23 is necessary.
34. Solder the selected R85 into its terminal posts. When the 1081 is warmed up, repeat operation (23).
35. Turn rear panel keyswitch to RUN mode. The basic DC-only instrument set-up procedure is complete.

4.3.2 Ohms Assembly

Equipment Required:

5½ digit DVM e.g. Datron 1065, 1061
 10M Ω 5% Resistor in parallel with 10nF capacitor. e.g. Datron part No. 400392
 Copper shorting links.

Procedure.

1. Select 10k Ω range, 4-wire. Connect I- to Ω Guard, I+ to Hi, and 10M Ω between Hi and Lo.
2. Connect DVM Hi to TP7, Lo to TP12, and adjust bias current R26 until TP7 voltage is zero \pm 100 μ V.
3. Connect Lo to Ω G. Connect shorting link between TP12 and TP8.
4. Connect DVM Hi to TP5 and check reading is zero \pm 50 μ V. Adjust FSV R40 if >+50 μ V, or FSV R39 if <-50 μ V.
 Note R39, R40 must be \geq 100k Ω .
5. Remove link between TP12 and TP8 and connections on front panel.

The basic Ohms set up procedure is complete.

4.3.3 AC Assembly

Equipment Required:

5mV/Div oscilloscope. e.g. Telequipment D83.
 5½ digit DVM with Ohms. e.g. Datron 1065, 1061.
 DC calibrator. e.g. Datron 4000 or 4000A.
 AC calibrator. e.g. Fluke 5200A.
 Asymmetric signal, 1V RMS, Crest Factor 5:1 ±0.02%, reversible polarity.

CAUTION

The following procedures should commence with the HF Autocal voltage close to the center of its span. To check this, select the 100V AC range and measure the DC voltage at J1-11 with respect to TP8. If it is between +4V and +6V it is NOT necessary to clear the calibration stores. If outside these limits, the cal stores should be cleared as described in para 4.3.1 operations (12), (13) and (14).

CLEARING THE CAL STORES ENTAILS A FULL 'AUTOCAL' OF THE INSTRUMENT!

Before proceeding; ensure that at least the Analog Assembly LIN, ZERO, and STD Autocalibrations have been carried out. (See para 4.3.1 operations 17 - 22.)

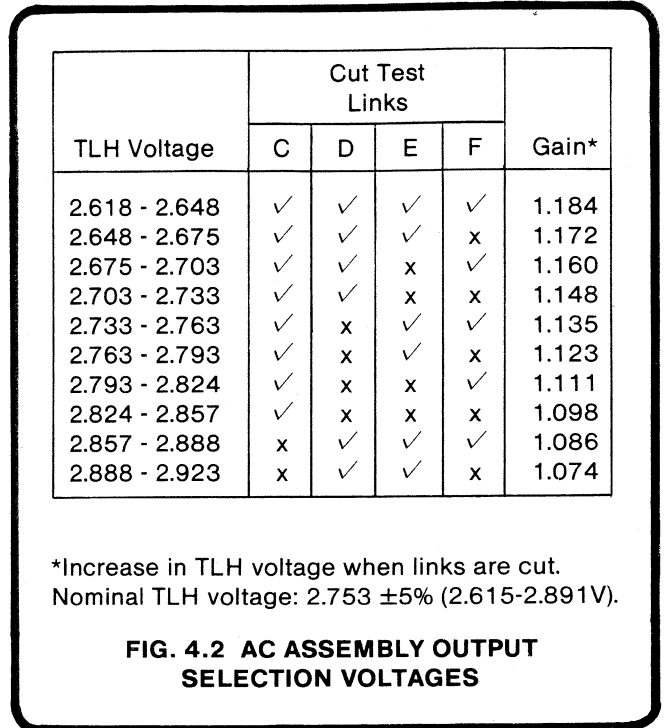
AC Preamplifier Zero

1. Read and comply with the CAUTION above.
1. Apply short circuit input. Select AC + DC, 100mV range and HOLD.
3. Connect DVM Lo to TP8, Hi to Test link K (TLK). Adjust R148 (bias current) for a reading of zero, ±140µV.
4. Select 100mV range AC, and check that the reading is zero, ±140µV. It may be necessary to re-adjust R148 to obtain this value. If so, recheck operation 3.
5. Select each range in turn, and check that the DVM reading is within ±70µV of zero (except 100mV range: ±140µV).

Set up RMS Converter

6. Select 10V range. Adjust R119 (Rectifier zero) for the most negative (or least positive) reading on the display.
7. Connect DVM to TLH. Adjust R101 (linearity) for a reading of +1.1mv±10%.
8. Select 100mV range. Check that the DVM reading is between 0.8mV and 1.8mV.

9. Select 1V range and apply 1V, 500Hz; with the DVM still connected to TLH. Refer to Fig. 4.2 and make or cut links TLC - TLF as appropriate to give a DVM reading of 3.120V ±0.025V.



Check Spec Readout Frequency Flags

10. Select HOLD. Connect DVM to TP6. Adjust the applied frequency and note that TP6 changes logic state at a frequency between 1.8kHz and 2.2kHz. Note also that the TP6 voltage increases by approx. 0.3V between 18kHz and 22kHz. Disconnect the DVM.

Set Range 'Zeros'

11. Deselect HOLD, and apply 500Hz at 0.1%FR input to each range in turn. Perform ZERO autocal on each range, using the instrument display to check that each range calibrates to 100 digits ±3 digits. Disconnect the input.
12. Apply a short circuit to the input, short Guard to Lo and select each range in turn. Check that the reading on each range is zero ±10 digits on the display (except 100mV range: ±30 digits). Remove the shorts.

Set up DC-DC Turnover

13. Select 1V range, AC + DC. Apply 1V 500Hz and perform GAIN autocal.
14. Apply +1V DC and note the displayed reading.
15. Apply -1V DC and adjust R62 (DC turnover) for the same reading as in operation (14). (±3 digits).

* VOL-145C ?


16. Repeat (13) to (15) until all readings are the same to within ± 20 digits.

Set up Coarse Frequency Response

17. Select 100V range, AC; apply 100V, 500Hz and perform GAIN autocal. Apply 100V, 50kHz and adjust C82 for a display reading of $100.000V \pm 20$ digits. (If necessary change C81 to a value which permits this adjustment).
18. Apply 100V, 100kHz and note the reading error. Adjust C79 to give 5 times the error in the same direction.
19. Repeat (17) and (18) until the 50kHz and 100kHz readings are separated by less than 20 digits.
20. Select 1V range, AC; apply 1V, 500Hz and perform GAIN autocal. Apply 1V, 50kHz and adjust C84 for a display reading of $1.00000V \pm 20$ digits. (If necessary change C85 to a value which permits this adjustment).

Set up Crest Factor

21. Apply 1VRMS, +ve 5:1 Crest Factor signal. Adjust R61 (crest factor) for a display reading of $1.00000V \pm 30$ digits.
22. Apply 1VRMS, -ve 5:1 Crest Factor signal. Check that display reading is $1.00000V \pm 0$ digits.
23. Apply 1V, 500Hz, and perform GAIN Autocal. Repeat (21), (22) and (23) until crest factor readings are within limits.

Linearity Checks

24. Select 1V range, AC + DC. Apply 1V DC and perform GAIN Autocal.
25. Apply 1.9VDC and adjust R27 value (Factory Selected Value - FSV) for a display reading of $1.90000V \pm 6$ digits (reducing R27 increases reading).
26. Repeat (24) and (25) until both correct.
27. Select 1V range AC. Apply in turn 1V, 100mV, 10mV, at 500Hz and check that display reading is correct to within ± 10 digits of the input voltage.
28. Apply open circuit input, set CAL/RUN switch to RUN; press '→', 'Test' and check for a display of 'PASS'.

Set up Output Buffer Input Current

29. Select 1V range, AC + DC, no filter. Apply 1V DC and set CAL switch to RUN. Use the 'A-B' computation mode to null out the reading: press STORE, B, then (A-B).

30. Select 0.1Hz filter, and leave to settle for two minutes. Check that the displayed reading is within ± 50 digits of zero.
31. Adjust R50, in small steps, to null out the reading error. Allow time for the reading to settle after one step before passing on to the next. Turn clockwise to make the reading more positive.
32. Repeat (29) to (31) until the difference is reduced to less than 10 digits.
33. Repeat (28).

The AC set-up procedure is now complete.

APPENDIX 1

ANALOG DATA LINE 'F.E.T.' PATTERNS

DC Voltage (IEEE 488 code F3)

Range		DC Isolator							
		AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7
R									
1	100mV	0	0	0	0	0	1	1	X
2	100mV	0	0	0	0	0	1	1	X
3	1V	0	0	0	0	1	1	1	X
4	10V	0	0	0	0	1	0	1	X
5	100V	0	0	0	0	1	1	0	X
6	1000V	0	0	0	0	1	0	0	X
7	1000V	0	0	0	0	1	0	0	X

AC Voltage (IEEE 488 code F2)

Range		AC assembly							
		AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7
R									
1	100mV	0	0	X	0	0	0	1	0
2	100mV	0	0	X	0	0	0	1	0
3	1V	0	0	X	0	0	0	0	0
4	10V	0	0	X	1	0	0	0	1
5	100V	0	0	X	0	1	0	0	1
6	1000V	0	0	X	0	0	1	0	1
7	1000V	0	0	X	0	0	1	0	1

DC Coupled AC Voltage (IEEE 488 code F6)

Range		AC assembly							
		AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7
R									
1	100mV	0	1	X	0	0	0	1	0
2	100mV	0	1	X	0	0	0	1	0
3	1V	0	1	X	0	0	0	0	0
4	10V	0	1	X	1	0	0	0	1
5	100V	0	1	X	0	1	0	0	1
6	1000V	0	1	X	0	0	1	0	1
7	1000V	0	1	X	0	0	1	0	1

AC Filter Selection (IEEE 488 codes F2 C0-C3)

Filter	AD1/F1	AD0/F0	A1	A0	S1	S2	S3	S4
.1 Hz	1	1	0	0	1	0	0	0
1 Hz	1	0	0	1	0	1	0	0
10 Hz	0	1	1	0	0	0	1	0
100 Hz	0	0	1	1	0	0	0	1

Ohms (IEEE 488 code F1)

Range R	DC Isolator									Ohms assembly							
	AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7		AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7
1 10Ω	0	0	0	0	0	1	1	X		0	0	0	0	0	0	1	X
2 100Ω	0	0	0	0	1	1	1	X		0	0	0	0	0	0	1	X
3 1kΩ	0	0	0	0	1	1	1	X		0	0	0	0	0	1	0	X
4 10kΩ	0	0	0	0	1	1	1	X		1	0	0	0	0	0	0	X
5 100kΩ	0	0	0	0	1	1	1	X		0	0	0	0	1	0	0	X
6 1MΩ	0	0	0	0	1	1	1	X		0	0	1	1	0	0	0	X
7 10MΩ	0	0	0	0	1	1	1	X		0	1	0	1	0	0	0	X
PRT and kΩPRT (IEEE 488 codes F4 and F5)																	
PRT } kΩPRT }	0	0	0	0	0	1	1	X		0	0	0	0	0	1	0	X

TEST (IEEE 488 code Y)

Function Tested	Range Checked	Voltage Measurement										Option assembly							
		AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7		AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7	
DC	.1 1 10	DC Isolator										No Option Required							
		0	0	0	0	0	1	0	1										
		0	0	0	0	1	1	0	1										
kΩ	10M	DC Isolator										Ohms assembly							
		0	0	0	0	1	1	1	1			0	1	0	1	0	0	0	1
AC	.1 1	AC assembly - J1 (Ranging)										AC assembly - J2 (Filters)							
		0	0	X	0	0	0	1	0			0	0	X	X	X	X	X	X
		0	0	X	0	0	0	0	0			0	0	X	X	X	X	X	X

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	090001	P.T.C. THERMISTOR	MULLARD	VA8650	2
R2	090001	P.T.C. THERMISTOR	MULLARD	VA8650	-
R3	000151	150Ω 1/4 W CARBON	MULLARD	CR25	8
R4	000151	150Ω " " "	"	"	-
R5	000151	150Ω " " "	"	"	-
R6	000102	1K 1/4 W. CARBON	"	CR25	1
R7	000104	100K 1/4 W. CARBON	MULLARD	CR25	1
R8	000151	150Ω 1/4 W. CARBON	MULLARD	CR25	-
R9	000151	150Ω " " "	"	"	-
R10	000151	150Ω " " "	"	"	-
R11	000151	150Ω " " "	"	"	-
R12	000151	150Ω " " "	"	"	-
AN1	090032	150R x7 2% NETWORK	BECKMAN	764 - 1 - R150	2
AN2	090032	" " " " " " " "	"	"	-
C1	102101	100PF CER DISC	ERIE	801	1
C2	150002	10MF 20% 16V DIP TANT	UNION CARBIDE	K10E16	2
C3	150016	1.0 MF 20% 35V " "	UNION CARBIDE	K10E35	2
C4	101103	0.01MF 250V CER DISC	ERIE	801	3

NOTES: CIRCUIT DIAG 430294
CHECK PROC. 460294
CHECK LIST 470294

DATE: 28-4-78
DRAWN: B.J.
TITLE: 1061/1071/1081 FRONT P.G.B. ASSY
DRAWING NUMBER: 400294
SHEET: 2 OF 6

C	D	1	2	3	4	5	6	7	8	9	
		17-8-78	29-9-78	6-12-78	25-JAN 79	11-JUN 79	26-OCT 79	21-4-80	11-6-80	11-7-82	2-6-83
		MD	EA	A	N	MD	MD	MD	MD	D	

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C5	101103	0.01MF. 250V CER DISC	ERIE	801	-
C6	150016	1.0 MF 20% 35V DIP TANT	UNION CARBIDE	K10E35	-
C7	101103	0.01MF 250V CER DISC	ERIE	801	-
C8	150002	10MF 20% 16V. DIP. TANT	UNION CARBIDE	K10E16	-
C9	104023	2n2F 20% 1KV CER DISC	ITT	HD16K102N2M5-SSIKODSC	1
C10	102472	4n7F 25% 500V CER DISC	ITT	CD10	1
Q1	240001	Si NPN	NATIONAL	BC184K	6
Q2	240001	Si NPN	NATIONAL	BC184K	-
Q3	240001	" "	"	"	-
Q4	240001	" "	"	"	-
Q5	240001	" "	"	"	-
Q6	240001	" "	"	"	-
M1	290042	GP. HIGH CURRENT TRANS ARRAY	R.C.A.	CA3081P	3
M2	280011	DUAL D FLIP-FLOP	MOTOROLA	MC14013 BCP	1
M3	290042	GP. HIGH CURRENT TRANS ARRAY	R.C.A.	CA3081P	-
M4	280015	QUAD LATCH	MOTOROLA	MC14076	7

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

DATE	DATE	DATE	DATE	DATE	DATE	DATE	DATE	DATE	DATE	DATE

DATE: 1061/71/81
DRAWN: B.J.
CHECKED: [Signature]
APPROVED: [Signature]
TITLE: FRONT. P.C.B. ASSY.
DRAWING NUMBER: 400294
SHEET: 3 OF 6

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1		NOT USED			-
R2	066200	20R POT 3/8 SQ VERT. CERMET	BECKMAN	72XW	1
R3	000221	220R 5% 1/4W CARBON	MULLARD	CR25	1
R4	014320	432R 1% M.F.	HOLCO	H.8	1
R5	000102	1K 5% 1/4W CARBON	MULLARD	CR25	2
R6	001184	180K 5% 1/2W CARBON	MULLARD	CR37	1
R7	066102	1K 3/8" RIGHT ANGLED CER. POT.	BECKMAN	72XW	1
R8	014021	4K02 1% 1/8W M.F.	HOLCO	H.8.	1
R9	019091	9K09 1% 1/8W M.F.	HOLCO	H.8.	1
R10	012001	2K 1% 1/8W M.F.	HOLCO	H.8.	1
R11	011302	13K 1% 1/8W M.F.	HOLCO	H.8.	1
R12	066501	500R 3/8" RIGHT ANGLED CER. POT.	BECKMAN	72XW	1
R13	000102	1K 5% 1/4W CARBON.	MULLARD	CR25	-
L1	370001	10uH 0.852 R.F. CHOKE.	PLESSEY	58/10/0011/10	3
L2	370001	10uH " "	"	"	-
L3	370001	10uH " "	"	"	-
C1	NOT USED				-
C2	NOT USED.				-
C3	NOT USED.				-

NOTES: CIRCUIT DIAG. 430295.
CHECK PROC. 460295.
CHECK LIST 470295.

SEE SHEET 2 FOR LATEST ISSUE

ISS	C	D	1	2	3	4	5	6	7	8	9	10	
DATE	-	-	22-8-78	29-9-78	8-12-78	25 JAN 79	6 JUN 79	31-10-79	21.4.80	11-2-85	16-2-85	1.6.85	16-8-83
CHKD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	

DATE: 2-5-78
DRAWN: B.J.
CHECKED: P.H.K.
APPROVED: [Signature]
DATE: [Blank]

TITLE: 1061/1071/1081
REAR P.C.B. ASSY.
DRAWING NUMBER: 400295
SHEET OF 6

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C4		NOT USED			-
C5	101103	0.01uF 250V CER DISC ERIE		801	3
C6	180026	10uF 350V ELECT. ITT		EN12/12 10/350	1
C7	180004	4700uF 16V AL ELECT. WIMA		PRINTILYT	1
C8	104026	47nF +50% 50V CER DISC SIEMENS		B37449	1
C9	150003	47uF 20% 6V3 DIP TANT UNION CARBIDE		K47E6V3	1
C10	150021	22uF 20% 25V DIP TANT UNION CARBIDE		K22E25	2
C11	150021	" " " " " "		"	-
C12	101103	0.01uF 250V CER DISC ERIE		801	-
C13	180025	1000uF 35V ELECT. WIMA		PRINTILYT	2
C14	101103	0.01uF 250V CER DISC ERIE		801	-
C15	180025	1000uF 35V ELECT. WIMA		PRINTILYT	-
C16	102102	1nF 10% 500V CER DISC ITT		CD10	1
D1	200022	Si RECTIFIER 3A 400V	MOTOROLA	BY252	2
D2	200022	" " " " " "	"	"	-
D3	210068	6V8 400mW ZENER	MULLARD	BZY88C6V8	1
D4	213004	180V 500mW ZENER	MOTOROLA	1N5279B	1

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

ISS												
E.C.O.												
DATE												
CHKD												

DATE: 2-5-78
DRAWN: B.J.
CHECKED: P.H.K.
APPROVED: [Signature]
DATE: [Blank]

TITLE: 1061/171/81
REAR P.C.B. ASSY.
DRAWING NUMBER: 400295
SHEET OF 6

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
J2	572115 /C	16WAY RIBBON CABLE ASSY	DATRON.		1
J3	604035	ACCT. RIGHT ANGLED WAFER, GOLD	MOLEX.	22-12-2041.	5
J4	604035	" " " " " "	"	"	-
J6	604035.	" " " " " "	"	"	-
	410092-5A	P.C.B.			1
J1 & J5	604036	STRIP OF 10 AMP PINS	AMP	163740-8	4
	630023	SCOTCHFLEX ADHESIVE CLIP	3M	CLIP 706	1
	630099	25mm MASKING TAPE	3M	SCOTCH N.230	A/R.
	620007	TEST POINT TERMINAL	MICROVAR	C 30	2
R1	000473	47K 5% 1/4W CARBON	MULLARD	CR25	2
R2	000473	47K " " " "	"	"	-
D1	200002	SI RECTIFIER 1A 50V	FAIRCHILD	1N4001	2
D2	200002	" " " " " "	"	"	-

NOTES CIRCUIT DIAGRAM . 430296
CHECK PROC. . 460296.
CHECK LIST . 470296.

SEE SHEET 2 FOR LATEST ISSUE

ISS	C	D	1	2	3	4	5	6	7	8
E.C.O.	-	-	RELEASED	ECO784	EC0849	867/904	992	1000	1102	1217
DATE	-	25-8-78	29-9-78	6-12-78	4-5-79	11-6-79	25-10-79	18.1.80	14.4.80	18.8.81
CHKD.	-	MD	MD	MD	MD	MD	MD	MD	MD	MD

DATE	2-5-78	datron ELECTRONICS LTD	
DRAWN	B.J.	TITLE	1061/71/81
CHECKED	<i>[Signature]</i>	CENTRE P.C.B. ASSY	
APPROVED		DRAWING NUMBER	400296
DATE		SHEET	2 OF 2

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
J2	604035	RIGHT ANGLED WAFER PIN, GOLD	MOLEX	22-12-2041	12
J3	604035	" " " " " "	"	"	-
J4	604035	" " " " " "	"	"	-
J5	604035	" " " " " "	"	"	-
J6	604035	" " " " " "	"	"	-
	410093-4	PRINTED CIRCUIT BOARD			1
	510111	7/0.2 BROWN WIRE			120mm
J1 & J7	604036	STRIP OF 10 AMP PINS	AMP	163740-8	2
	605053	12 WAY POLARISED SOCKET	MOLEX	22-01-2125	2
	605057	GOLD CRIMP PINS	MOLEX	4809-GL	7
	606004	PLASTIC POLARISING PEG	MOLEX	4161-1	4
	540002	22 SW.G. TIN CU WIRE			A/R
	590001	SLEEVE MAX CABLE Ø3.0	HELLERMANN ELECTRIC	H15 x 20mm BLK HELSYN	1

NOTES CIRCUIT DIAGRAM . 430297.
CHECK PROC. . 460297.
CHECK LIST . 470297.

SEE SHEET 2 FOR LATEST ISSUE

ISS	C	D	1	2
E.C.O.	-	-	RELEASED	867
DATE	-	24-8-78	29-9-78	11-6-79
CHKD.	-	MD	MD	

DATE	28-4-78	datron ELECTRONICS LTD	
DRAWN	B.J.	TITLE	1061/71/81
CHECKED	<i>[Signature]</i>	L.H. PCB ASSEMBLY	
APPROVED		DRAWING NUMBER	400297
DATE		SHEET	2 OF 2

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000334	330K 5% 1/4W CARBON	MULLARD	CR25	2
R2	000334	" " " "	"	"	-
	410094-4A	P.C.B.			1
	540002	22SWG TIN. CU. WIRE			A/R
J2	574270/C	24WAY RIBBON CABLE ASSY	DATRON		1
J1 & J3	604036	STRIP OF 10AMP PINS	AMP	163740-8	4
	590001	SLEEVE MAX CABLE Ø 3.0	HELLERMANN ELECTRIC	H15x20mm BLK. HELSYN	2
	630099	25mm MASKING TAPE	3M	SCOTCH N.230	A/R

NOTES CIRCUIT DIAGRAM - 430298
CHECK PROC. - 460298
CHECK LIST - 470298
SEE SHEET 2 FOR LATEST ISSUE

ISS	C	D	1	2	3	4	5	6
E.C.G.	-	-	RELEASED	EC0850	867/504	943	1217	1474
DATE	-	24-8-78	29-9-78	4-5-79	11-6-79	10-9-79	18-8-81	3-6-83
CHKD	-	MD	MD	MD	MD	MD	MD	MD

DATE	28-4-78	datron ELECTRONICS LTD	
DRAWN	B.J.	DATE	1061/71/81
CHECKED	<i>[Signature]</i>	R.H. PCB ASSEMBLY	
APPROVED		DRAWING NUMBER	400298
DATE		SHEET OF	2 2

DESIGNATOR	DATRON PART No	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No	No. USED Per Assy
R1	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	4
R2	000103	10k " " "	"	"	3
R3	000183	18k " " "	"	"	1
R4	000103	10k " " "	"	"	-
R5	000104	100k " " "	"	"	1
R6	000103	10k " " "	"	"	-
R7	000102	1k " " "	"	"	20
R8	000102	1k " " "	"	"	-
R9	000102	1k " " "	"	"	-
R10	000102	1k " " "	"	"	-
R11	000102	1k " " "	"	"	-
R12	000102	1k " " "	"	"	-
R13	000102	1k " " "	"	"	-
R14	000102	1k " " "	"	"	-
R15	000102	1k " " "	"	"	-
R16		NOT USED			-
R17		NOT USED			-
R18	000102	1k " " "	"	"	-
R19	000102	1k " " "	"	"	-
R20	000102	1k " " "	"	"	-
R21	000472	4k7 " " "	"	"	-
R22	000272	2k7 " " "	"	"	5
R23	000472	4k7 " " "	"	"	-

NOTES. CIRCUIT DIAGRAM = 430301
CHECK PROCEDURE = 460301
CHECK LIST = 470301

SEE SHEET 2 FOR LATEST ISSUE

REV	C	1	2	3	4	5	6	7	8
E.C.O	-	-	789	822	854	904	904	12.17	12.53
DATE	28.4.78	29.9.78	17 NOV 78	19 FEB 79	8 MAY 79	21.6.79	8-1-80	17.8.81	2.12.81
CHKD.	-	BRV	MSD	MSD	MD	MD	MD	MD	MD

DATE	28.4.78	datron ELECTRONICS LTD
DRAWN	JL	
CHECKED	MM	TITLE
APPROVED		1071 DISPLAY DRIVER 1081 PCB. ASSY.
DATE		DRAWING NUMBER
		400301
		SHEET
		2 OF 7

LW. 1164

DESIGNATOR	DATRON PART No	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No	No. USED Per Assy
R24	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	-
R25	000272	2k7 " " "	"	"	-
R26	000272	2k7 " " "	"	"	-
R27	000182	1k8 " " "	"	"	1
R28	000222	2k2 " " "	"	"	1
R29	000272	2k7 " " "	"	"	-
R30	000102	1k " " "	"	"	-
R31	000102	1k " " "	"	"	-
R32	000102	1k " " "	"	"	-
R33	000102	1k " " "	"	"	-
R34	000102	1k " " "	"	"	-
R35	000102	1k " " "	"	"	-
R36	000102	1k " " "	"	"	-
R37	000102	1k " " "	"	"	-
R38	000472	4k7 " " "	"	"	-
R39	000393	39k " " "	"	"	1
R40		NOT USED			-
R41	000665	56k 3% 1/4W CARBON	MULLARD	CR25	1

NOTES.
SEE SHEET 2 FOR LATEST ISSUE

REV	C	1	2	3	4	5	6	7	8
E.C.O									
DATE									
CHKD.									

DATE		datron ELECTRONICS LTD
DRAWN		
CHECKED		TITLE
APPROVED		1071 DISPLAY DRIVER 1081 PCB. ASSY.
DATE		DRAWING NUMBER
		400301
		SHEET
		3 OF 7

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M1	280062	128 x 8 BIT STATIC RAM	MOTOROLA	MC 6810A	1
M2	280015	QUAD LATCH	NATIONAL	MM 74C173N	2
M3	280015	" " " "	"	"	-
M4	280023	QUAD 2 1/P NOR GATE	MOTOROLA	MC 14001 BCP	2
M5	280023	" " " "	"	"	-
M6	280024	TRI-STATE HEX NON-INV. BUFFER	"	MC 14503 BCP	2
M7	280024	" " " " " "	"	"	-
M8	280059	DUAL BINARY UP COUNTER	"	MC 14520 BCP	1
M9	270045	QUAD 2-1 DATA SELECT LS TTL	NATIONAL	SN74 LS 157	1
M10	280033	8 CHANNEL DATA SELECT	MOTOROLA	MC 14512 BCP	1
M11	280043	4 BIT LATCH/4-TO-16 LINE DECODER	"	MC 14515 BCP	1
M12	270048	QUAD 2/P NAND LS TTL	NATIONAL	SN74 LS 00	1
M13	280077	HEX GATE	MOTOROLA	MC 14572	1
J1	571095/C	16 WAY AP/3M RIBBON CABLE	DATRON	-	1
J2	605102	24 WAY DIL SKT. GOLD	CA	CA 245 106D	1
	605060	14 WAY DIL SOCKET	ASTRALUX or JERMYN	ICL 143 - S3T	3
	605061	16 WAY DIL SOCKET	"	ICL 163 - S6T	8
	605064	24 WAY DIL SKT. TIN PLATE	AUGAT	324 - AG 39D	2
AN2 - AN4	090065	330K x 7 2% RESISTOR NETWORK	BECKMAN	764-1-R330K	3

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS																				
E.C.O.																				
DATE																				
CHKD																				

DATE		datron ELECTRONICS LTD TITLE 1071 DISPLAY DRIVER 1081 PCB ASSY. DRAWING NUMBER 400301	SHEET 6 OF 7
DRAWN			
CHECKED			
APPROVED			
DATE			

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	410097-5A	PCB			1
	617010	NYLATCH - PLUNGER	ORDER FROM C.J. FOX & SONS	HN3P-32-4-1	4
	617011	NYLATCH - GROMMET	" " " "	HN3G-32-1	4
TPI-TPG	540001	22 SWG. BTC WIRE			A/R
	590004	SLEEVE - PTFE	HELLERMANN ELECTRIC	FE10	A/R
	620007	TEST POINT TERMINAL	MICROVAR	C 30	S

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS																				
E.C.O.																				
DATE																				
CHKD																				

DATE		datron ELECTRONICS LTD TITLE 1071 DISPLAY DRIVER 1081 PCB ASSY. DRAWING NUMBER 400301	SHEET 7 OF 7
DRAWN			
CHECKED			
APPROVED			
DATE			

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No USED Per Assy
M3		FITTED AT FINAL ASSY.			-
M4		NOT USED			-
M5		NOT USED			-
M6	280024	TRI-STATE HEX. BUFFER	MOTOROLA	MC14503 BCP	1
M7		NOT USED			-
M8	270050	HEX. INVERTER LS	NATIONAL	DM74 LS04N	1
M9	280064	GPIA	MOTOROLA	MC68488P	1
M10	280068	DUAL PREC. M'STABLE M'VIBR.	MOTOROLA	MC14538 BCP	1
M11	270055	DUAL 4 I/P NAND LS	NATIONAL	DM74 LS20N	2
M12	270055	DUAL 4 I/P NAND LS	NATIONAL	DM74 LS20N	-
M13	270051	DUAL 4 I/P AND LS	NATIONAL	DM74 LS21N	1
J1	605102	24 WAY DIL. SOCKET GOLD	CA	CA-24-S 10SD	1
J2	605002	16 WAY DIL. LOW PROFILE SKT.	JERMYN OR ANTIFERRENCE	A23-2001/Y OR ICN-63-S3	1
J3	573120/C	24 WAY AP/3M CABLE ASSY	DATRON		1
J4	605051	4 WAY POLARISED SOCKET	MOLEX	(22-01-2045) 6471-4-1	1
	400379/1	WIRE/TERMINAL ASSY			2
	410165-4A	PCB			1
	540002	22 SWG BTC WIRE			A/R
	590004	SLEEVE - PTFE	HELLERMANN ELECTRIC	FE10	A/R
	605060	14 WAY DIL. SOCKET	ASTRALUX OR JERMYN	ICL-143-S3T	4

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS																			
E.C.O.																			
DATE																			
CHKD																			

DATE		datron ELECTRONICS LTD TITLE 1061/1065/1071/1081 IEEE PCB. ASSY. DRAWING NUMBER 400427 4 SHEET OF 5
DRAWN		
CHECKED		
APPROVED		
DATE		

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No USED Per Assy
	605061	16 WAY DIL. SOCKET	ASTRALUX OR JERMYN	ICL-163-S6T	2
	605050	40 PIN DIL. LOW PROF. SKT	AUGAT	340-AG39D	1
	605064	24 PIN DIL. SOCKET	AUGAT	324-AG39D	3
	605056	CRIMP TERMINAL	MOLEX	4809-TL	2
	606005	CLIP FOR 605002	ANTIFERRENCE	RC-74	1
	620007	TEST POINT TERMINAL	MICROVAR	C30	5
	900004	SILICONE RUBBER COMPOUND	RS	555-588	A/R

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS																			
E.C.O.																			
DATE																			
CHKD																			

DATE		datron ELECTRONICS LTD TITLE 1061/1065/1071/1081 IEEE PCB. ASSY. DRAWING NUMBER 400427 5 SHEET OF 5
DRAWN		
CHECKED		
APPROVED		
DATE		

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000104	100k 5% 1/4W CARBON	MULLARD	CR25	10
R2	000101	100R " " "	"	"	8
R3	000101	100R " " "	"	"	-
R4	000156	15M 10% " "	ALLEN BRADLEY	CB	1
R5		FSV (18k NOM)		CR25	-
R6	050057	27k4 1% 15ppm MF	HOLCO	H8	2
R7	050057	27k4 " " "	HOLCO	H8	-
R8	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R9		NOT USED			-
R10	000101	100R 5% 1/4W CARBON	"	"	-
R11		FSV		CR25	-
R12	014751	4k75 1% 1/8W 50ppm MF	HOLCO	H8C	2
R13	011003	100k 1% 1/8W 50ppm MF	HOLCO	H8C	3
R14	014751	4k75 1% 1/8W 50ppm MF	HOLCO	H8C	-
R15		FSV			-
R16	019091	9k09 1% 1/8W 50ppm MF	HOLCO	H8C	1
R17	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	3
R18	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R19	000331	330R 5% 1/4W CARBON	MULLARD	CR25	1
R20	063203	20K POT CERMET	BECKMAN	72P	1
R21	000105	1M 5% 1/4W CARBON	MULLARD	CR25	11
R22	000101	100R " " "	"	"	-
R23	063504	500K POT CERMET	BECKMAN	72P	1

NOTES: CIRCUIT DIAG. = 430503
CHECK PROCEDURE = 460503
CHECK LIST = 470503
SEE SHEET 2 FOR LATEST ISSUE

ISS	A	I
E.C.O.	-	-
DATE	-	31.3.83
CHKD		

DATE	6.12.82	datron ELECTRONICS LTD TITLE 1081 ANALOGUE PCB ASSEMBLY. DRAWING NUMBER 400503	2 SHEET OF 24
DRAWN			
CHECKED	LOG/MD		
APPROVED	RWF		
DATE	31-3-83		

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	000184	180k 10% 1/4W CARBON	MULLARD	CR25	1
R25	000122	1K2 5% 1/4W CARBON	MULLARD	CR25	2
R26	000185	1M8 10% 1/4W CARBON	"	"	1
R27	000475	4M7 " " "	"	"	1
R28	000222	2k2 5% 1/4W CARBON	"	"	4
R29	000100	10R " " "	"	"	7
R30	000100	10R " " "	"	"	-
R31	014752	47k5 1% 1/8W 50ppm MF	HOLCO	H8C	2
R32	013922	39k2 1% 1/8W 50ppm MF	HOLCO	H8C	1
R33	014752	47k2 1% 1/8W 50ppm MF	HOLCO	H8C	-
R34	000102	1K 5% 1/8W 50ppm MF	MULLARD	CR25	-
R35	011003	100k 1% 1/8W 50ppm MF	HOLCO	H8C	-
R36	011003	100k 1% 1/8W 50ppm MF	HOLCO	H8C	-
R37	000682	6k8 5% 1/4W CARBON	MULLARD	CR25	6
R38		NOT USED			-
R39	090012-2	9k10 .02% R 2ppmR WW	MANN	AX175 BT	1
R40	090012-2	9k10 .02% R 2ppmR WW	MANN	AX175 BT	-
R41	000332	3k3 5% 1/4W CARBON	MULLARD	CR25	2
R42	000473	47k 5% 1/4W CARBON	MULLARD	CR25	5
R43	070164	5k .1% 3ppm WW	MANN	AX175C	1
R44	090110-1	5k ATTN SET	VISHAY	SEE DRG	1 SET
R45	090110-1	5k ATTN SET	VISHAY	SEE DRG	-
R46	000182	1K8 5% 1/4W CARBON	MULLARD	CR25	1

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

ISS	A	I
E.C.O.		
DATE		
CHKD		

DATE	6.12.82	datron ELECTRONICS LTD TITLE 1081 ANALOGUE PCB ASSEMBLY. DRAWING NUMBER 400503	3 SHEET OF 24
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DESIGNATOR	DATRON PART No	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
53	20000B	Si LOW LEAKAGE	FAIRCHILD	IN458A	-
D54	20000B	" " "	"	"	-
D55	200001	Si GEN PURPOSE	"	IN414B	-
D56	200001	" " "	"	"	-
D57		NOT USED			-
D58		NOT USED			-
D59	219020-1	ZENER REFERENCE SET			-
D60	219020-1	" " "			-
D61	219020-1	" " "			-
D62	219020-1	" " "			-
D63	200001	Si GEN PURPOSE	FAIRCHILD	IN414B	-
D64		NOT USED			-
D65		NOT USED			-
D66	20000B	Si LOW LEAKAGE	FAIRCHILD	IN458A	-
D67	20000B	" " "	"	"	-
D68	200001	Si GEN PURPOSE	"	IN414B	-
D69	200001	Si GEN PURPOSE	"	IN414B	-
D70	200001	Si GEN PURPOSE	"	IN414B	-
D71	210047	4V7 400mw ZENER	MULLARD	BZY83C4V7	-
D72	200001	Si GEN PURPOSE	FAIRCHILD	IN414B	-

NOTES

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DESIGNATOR	DATRON PART No	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q1	230001	N-CHAN CURRENT LIM	SILICONIX	E506	2
Q2	250008	Si P.N.P	FAIRCHILD	BC214C	2
Q3	250008	Si P.N.P	FAIRCHILD	BC214C	-
Q4	230001	N-CHAN CURRENT LIM	SILICONIX	E506	-
Q5	230027-1	LOW LEAKAGE N-FET	TELEDYNE	U3114	7
Q6	230027-1	"	"	"	-
Q7	230027-1	"	"	"	-
Q8	230027-1	"	"	"	-
Q9	230027-1	"	"	"	-
Q10	230027-1	"	"	"	-
Q11	230027-1	"	"	"	-
Q12	230031	N-CHAN DUAL JFET	"	SU2656M	4
Q13	230002	N-CHAN J-FET	TELEDYNE	U1934E	6
Q14	230002	"	"	"	-
Q15	230002	"	"	"	-
Q16	230002	"	"	"	-
Q17		NOT USED			-
Q18	230002	N-CHAN J-FET	TELEDYNE	U1934E	-
Q19	230002	"	"	"	-
Q20	240006	Si NPN	FAIRCHILD	2N3904	5
	240006	"	"	"	-
	240006	"	"	"	-
Q23	240006	"	"	"	-

NOTES

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R47	012743	274k 1% 1/8W 50ppm MF	HOLCO	H8C	-
R48	041004	1M 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	2
R49	011002	10k 1% 1/8W 50ppm M/F	HOLCO	H8C	2
R50	063104	100k POT 3/8 SQ. CERMET	BECKMAN	72P	2
R51	090111	100M 5% THICK FILM	HOLSWORTHY	SEE DRG	-
R52	080049-1	25k .1% 3ppm M. FOIL	VISHAY	SEE DRG	1
R53	080039	3k .1% 10ppm M. FOIL	VISHAY	VSRC1	1
R54	080040	1k5 .1% 10ppm M. FOIL	VISHAY	VSRC1	1
R55	080041	750R .1% 50ppm M. FOIL	VISHAY	VSRC1	1
R56	080042	375R .1% 50ppm M. FOIL	VISHAY	VSRC1	1
R57	000182	1k8 5% 1/4W CARBON	MULLARD	CR25	4
R58	000151	150R 5% 1/4W CARBON	MULLARD	CR25	1
R59	000752	7k5 5% 1/4W CARBON	MULLARD	CR25	3
R60	000478	4R7 5% 1/4W CARBON	MULLARD	CR25	1
R61	063200	20R POT 3/8 SQ. CERMET	BECKMAN	72P	1
R62	063100	10R POT 3/8 SQ. CERMET	BECKMAN	72P	1
R63	000100	10R 5% 1/4W CARBON	MULLARD	CR25	3
R64	012003	200k 1% 1/8W 50ppm MF	HOLCO	H8C	1
R65	000124	120k 5% 1/4W CARBON	MULLARD	CR25	1
R66	000332	3k3 5% 1/4W CARBON	MULLARD	CR25	4
R67	000332	3k3 5% 1/4W CARBON	MULLARD	CR25	-
R68	000332	3k3 5% 1/4W CARBON	MULLARD	CR25	-
R69	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-

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1081 AC PCB ASSY

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R70	080045-1	5k5 .01% 3ppm M. FOIL	VISHAY	SEE DRG	-
R71	000331	330R 5% 1/4W CARBON	MULLARD	CR25	-
R72	000680	68R 5% 1/4W CARBON	MULLARD	CR25	-
R73	000562	5k6 5% 1/4W CARBON	MULLARD	CR25	-
R74	080045-1	5k5 .01% 3ppm M. FOIL	VISHAY	SEE DRG	-
R75	080044-1	4k9925 .01% 3ppm M. FOIL	VISHAY	SEE DRG	1
R76	014991	4k99 1% 1/8W 50ppm MF	HOLCO	H8C	1
R77	090111	100M 5% THICK FILM	HOLSWORTHY	SEE DRG	-
R78	000182	1k8 5% 1/4W CARBON	MULLARD	CR25	-
R79	000752	7k5 5% 1/4W CARBON	MULLARD	CR25	-
R80	000471	470R 5% 1/4W CARBON	MULLARD	CR25	1
R81	000105	1M 5% 1/4W CARBON	MULLARD	CR25	-
R82	000475	4M7 5% 1/4W CARBON	MULLARD	CR25	1
R83	000332	3k3 5% 1/4W CARBON	MULLARD	CR25	-
R84	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-
R85	000105	1M 5% 1/4W CARBON	MULLARD	CR25	-
R86	013323	332k 1% 1/8W 50ppm MF	HOLCO	H8C	1
R87	011503	150k 1% 1/8W 50ppm MF	HOLCO	H8C	1
R88	000105	1M 5% 1/4W CARBON	MULLARD	CR25	-
R89	000104	100k 5% 1/4W CARBON	MULLARD	CR25	-
R90	000182	1k8 5% 1/4W CARBON	MULLARD	CR25	-
R91	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R92	000221	220R 5% 1/4W CARBON	MULLARD	CR25	-

NOTES.

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M24	220017-2	DUAL OPTO ISOLATOR	FAIRCHILD	FCDB80	-
M25	260022	LINEAR IC OP AMP	NATIONAL	LF 355	2
M26	290078	4016 SWITCH SELECTED	DATRON	MC14016BCL (WHITE)	1
M27	280008	QUAD 2 I/P NAND GATE	"	MC14011 BCP	-
M28	280044	BINARY UP/DOWN COUNTER	"	MC14516 BCP	1
M29	280011	DUAL D FLIP-FLOP	"	MC14013 BCP	1
M30	260053	7650 OP AMP	INTERSIL	ICL7650 CPD	1
M31	260067	11 OP AMP	NATIONAL	LM111CLH	1
M32	260066	11 OP AMP	NATIONAL	LM111CN	1
M33	260002	" " " "	FAIRCHILD	μA 741 HC	2
M34	260013	" " " "	NATIONAL	LF 356	1
M35	290081	4051 MUX SELECTED	DATRON	M14051 BCL (WHITE)	1
M36	260002	741 OP AMP	FAIRCHILD	μA 741 HC	-
M37	NOT USED				-
M38	NOT USED				-
M39	260027	714 OP AMP	FAIRCHILD	μA 714 HC	2
M40	260027	714 OP AMP	FAIRCHILD	μA 714 HC	-

NOTES

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
RL1	330018-1	RELAY 2P2W 7V HOLD-IN	AMF	SEE DRAWING	1
RL2	330027-A	RELAY 1P2W MINIATURE	TAKAMISAWA	MZ12HSC	1
	400379/1	WIRE/TERMINAL ASSY			7
	400379/2	"			4
	410216-1	P.C.B.			1
	459112-2	RELAY BRACKET	KDP		1
	540002	22 SWG. TINNED COPPER WIRE			A/R
	540008	7/2 PTFE INSULATED WHITE WIRE			165
	590001	SLEEVE MAX CABLE Ø 3.0	HELLERMANN ELECTRIC	H15 X 20 - BLK HELSYN	5
J3	571075/C	16 WAY AP/3M RIBBON CABLE	DATRON		1
	602001	F.S.V. TERMINAL	MOLEX	02-04-1875	8
J2, 4, 5	605002	16 WAY DIL SOCKET	JERMYN	A23-2001/Y	3
	605060	14 WAY DIL SOCKET	ASTRALUX	ICL 143-53T	8
	605061	16 WAY DIL SOCKET	ASTRALUX	ICL 143-56T	11
V1 & J6	605052	8 WAY POLARISED SOCKET	MOLEX	22-01-2085	2
	605059	8 WAY DIL SOCKET	ASTRALUX	ICL-083-56T	6
	606005	CLIP FOR 605002	ANTI-FERRENCE	RC-74	3

NOTES

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R139	011822	18k2 1% 1/8w 50ppm MF	HOLCO	H8C	2
R140	014321	4k32 1% 1/8w 50ppm MF	HOLCO	H8C	1
R141	041824	1M82 1% 1/2w 100ppm MF	HOLCO	H8C	1
R142	080043-	1k -1% 3 ppm M. FOIL	VISHAY	SEE DRG	-
R143	080048-	10k1 -1% 3 ppm M. FOIL	VISHAY	SEE DRG	1
R144	080051-	111k -1% 3 ppm M. FOIL	VISHAY	SEE DRG	1
R145		NOT USED			-
R146	080062	1M -1% 5 ppm M. FILM	VTM	MAR7-T16-1M-0.1%	1
R147	000101	100R 5% 1/4w CARBON	MULLARD	CR25	-
R148	063104	100k POT 3/8 SQ. CERMET	BECKMAN	72P	-
R149	011822	18k2 1% 1/8w 50ppm MF	HOLCO	H8C	-
R150	000100	10R 5% 1/4w CARBON	MULLARD	CR25	-
R151	000100	10R 5% 1/4w CARBON	MULLARD	CR25	-
R152	000104	100k 5% 1/4w CARBON	MULLARD	CR25	-
R153	000104	100k 5% 1/4w CARBON	MULLARD	CR25	-
R154	013320	332R 1% 1/8w 50ppm MF	HOLCO	H8C	1
R155	041004	1M 1% 1/2w 100ppm CF	ALLEN BRADLEY	CC	-
R156	019768	37R6 1% 1/8w 50ppm MF	HOLCO	H8C	1
R157	000105	1M 5% 1/4w CARBON	MULLARD	CR25	-
R158	090111-	100M 5% THICK FILM	HOLSWORTHY	SEE DRG	-
R159	000241	240R 5% 1/4w CARBON	MULLARD	CR25	1
R160	012001	2K00 1% 1/8w 50ppm MF	HOLCO	H8C	-
R161	000101	100R 5% 1/4w CARBON	MULLARD	CR25	-

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R162	012151	2k15 1% 1/8w 50ppm MF	HOLCO	H8C	1
R163	000912	9k1 5% 1/4w CARBON	MULLARD	CR25	1
R164	014750	475R 1% 1/8w 50ppm MF	HOLCO	H8C	1
R165	000104	100k 5% 1/4w CARBON	MULLARD	CR25	-
R166	015620	562R 1% 1/8w 50ppm MF	HOLCO	H8C	1
R167	080052-	277k -1% 3 ppm M. FOIL	VISHAY	SEE DRG	4
R168	080052-	277k -1% 3 ppm M. FOIL	VISHAY	SEE DRG	-
R169	080052-	277k -1% 3 ppm M. FOIL	VISHAY	SEE DRG	-
R170	080052-	277k -1% 3 ppm M. FOIL	VISHAY	SEE DRG	-

NOTES

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000824	820k 5% 1/4W CARBON	MULLARD	CR25	1
R2	000103	10k 5% 1/4W CARBON	MULLARD	CR25	10
R3	000473	47k 5% 1/4W CARBON	MULLARD	CR25	3
R4	000223	22k 5% 1/4W CARBON	MULLARD	CR25	4
R5	080045-1	5k5 -01% 3ppm M. FOIL	VISHAY	SEE DRG	4
R6	000223	22k 5% 1/4W CARBON	MULLARD	CR25	-
R7	000473	47k 5% 1/4W CARBON	MULLARD	CR25	-
R8	000154	150k 5% 1/4W CARBON	MULLARD	CR25	1
R9	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-
R10	000333	33k 5% 1/4W CARBON	MULLARD	CR25	3
R11	000105	1M 5% 1/4W CARBON	MULLARD	CR25	6
R12	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-
R13	000155	1M5 5% 1/4W CARBON	MULLARD	CR25	1
R14	000105	1M 5% 1/4W CARBON	MULLARD	CR25	-
R15	000333	33k 5% 1/4W CARBON	MULLARD	CR25	-
R16	000333	33k 5% 1/4W CARBON	MULLARD	CR25	-
R17	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-
R18	011001	1k00 1% 1/8W 50ppm MF	HOLCO	H8C	2
R19	011001	1k00 1% 1/8W 50ppm MF	HOLCO	H8C	-
R20	000223	22k 5% 1/4W CARBON	MULLARD	CR25	-
R21	000102	1k 5% 1/4W CARBON	MULLARD	CR25	3
R22	000473	47k 5% 1/4W CARBON	MULLARD	CR25	-
R23	000101	100R 5% 1/4W CARBON	MULLARD	CR25	6

NOTES CIRCUIT DIAGRAM = 430504
CHECK PROCEDURE = 460504
CHECK LIST = 470504
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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	000562	5k6 5% 1/4W CARBON	MULLARD	CR25	2
R25	000122	1k2 5% 1/4W CARBON	MULLARD	CR25	1
R26	000102	1k 5% 1/4W CARBON	MULLARD	CR25	-
R27		FSV			1
R28	290026	RMS KIT	DATRON	SEE DRG	1 KIT
R29	000120	12R 5% 1/4W CARBON	MULLARD	CR25	1
R30	090111-1	100M 5% THICK FILM	HOLSWORTHY	SEE DRG	4
R31	000331	330R 5% 1/4W CARBON	MULLARD	CR25	3
R32	012743	274k 1% 1/8W 50ppm MF	HOLCO	H8C	2
R33	011003	100k 1% 1/8W 50ppm MF	HOLCO	H8C	1
R34	290026	RMS KIT	DATRON	SEE DRG	-
R35	000221	220R 5% 1/4W CARBON	MULLARD	CR25	5
R36	000680	68R 5% 1/4W CARBON	MULLARD	CR25	3
R37	000271	270R 5% 1/4W CARBON	MULLARD	CR25	2
R38	000271	270R 5% 1/4W CARBON	MULLARD	CR25	-
R39	000224	220k 5% 1/4W CARBON	MULLARD	CR25	1
R40	000104	100k 5% 1/4W CARBON	MULLARD	CR25	10
R41	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-
R42	000104	100k 5% 1/4W CARBON	MULLARD	CR25	-
R43	000104	100k 5% 1/4W CARBON	MULLARD	CR25	-
R44	042674	2M67 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	1
R45	016811	6k81 1/8W 50ppm MF	HOLCO	H8C	1
R46	012742	27k4 1% 1/8W 50ppm MF	HOLCO	H8C	1

NOTES.

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R93	000221	220R 5% 1/4W CARBON	MULLARD	CR25	-
R94	011002	10k0 1% 1/8W 50ppm MF	HOLCO	H8C	-
R95	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	2
R96	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	-
R97	080047-1	10k .01% 3ppm M. FOIL	VISHAY	SEE DRG	1
R98	080045-1	5k5 .01% 3ppm M. FOIL	VISHAY	SEE DRG	-
R99	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R100	000335	3M3 5% 1/4W CARBON	MULLARD	CR25	1
R101	063105	1M POT 3/8 SQ CERMET	BECKMAN	72P	1
R102	000225	2M2 5% 1/4W CARBON	MULLARD	CR25	1
R103	012001	2k00 1% 1/8W 50ppm MF	HOLCO	H8C	4
R104	012001	2k00 1% 1/8W 50ppm	HOLCO	H8C	-
R105	000221	220R 5% 1/4W CARBON	MULLARD	CR25	-
R106	000104	100k 5% 1/4W CARBON	MULLARD	CR25	-
R107	013923	392k 1% 1/8W 50ppm MF	HOLCO	H8C	2
R108	013923	392k 1% 1/8W 50ppm MF	HOLCO	H8C	-
R109	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	1
R110	000104	100k 5% 1/4W CARBON	MULLARD	CR25	-
R111	000223	22k 5% 1/4W CARBON	MULLARD	CR25	-
R112	011053	105k 1% 1/8W 50ppm MF	HOLCO	H8C	2
R113	011053	105k 1% 1/8W 50ppm MF	HOLCO	H8C	-
R114	000104	100k 5% 1/4W CARBON	MULLARD	CR25	-
R115	000222	2k2 5% 1/4W CARBON	MULLARD	CR25	1

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R116	000752	7k5 5% 1/4W CARBON	MULLARD	CR25	-
R117	000680	68R 5% 1/4W CARBON	MULLARD	CR25	-
R118	000221	220R 5% 1/4W CARBON	MULLARD	CR25	-
R119	063204	200k POT 3/8 SQ. CERMET	BECKMAN	72P.	1
R120	000274	270k 5% 1/4W CARBON	MULLARD	CR25	1
R121	080043-1	1k .1% 3ppm M. FOIL	VISHAY	SEE DRG	2
R122	080046-1	9k .1% 3ppm M. FOIL	VISHAY	SEE DRG	1
R123	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-
R124	048253	825k 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	1
R125	012001	2k00 1% 1/8W 50ppm MF	HOLCO	H8C	1
R126	000102	1k 5% 1/4W CARBON	MULLARD	CR25	-
R127	000682	6k8 5% 1/4W CARBON	MULLARD	CR25	1
R128	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R129	000331	330R 5% 1/4W CARBON	MULLARD	CR25	-
R130	000182	1k8 5% 1/4W CARBON	MULLARD	CR25	-
R131	080050-1	62k6 .1% 3ppm M. FOIL	VISHAY	SEE DRG	2
R132	080050-1	62k6 .1% 3ppm M. FOIL	VISHAY	SEE DRG	-
R133	000330	33R 5% 1/4W CARBON	MULLARD	CR25	1
R134	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-
R135	000103	10k 5% 1/4W CARBON	MULLARD	CR25	-
R136	018251	8k25 1% 1/8W 50ppm MF	HOLCO	H8C	1
R137	018252	82k5 1% 1/8W 50ppm MF	HOLCO	H8C	1
R138	011823	182k 1% 1/8W 50ppm MF	HOLCO	H8C	1

NOTES

SEE SHEET 2 FOR LATEST ISSUE

ISS		DATE	
E.C.O.		DATE	
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DATE	22.12.82	datron ELECTRONICS LTD	
DRAWN	11	TITLE	
CHECKED		1081 AC PCB ASSY	
APPROVED		DRAWING NUMBER	400504
DATE		SHEET	7 OF 19

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1	150020	10 μ F 20% 25V DIP TANT	UNION CARBIDE	K10E25	9
C2	150020	10 μ F 20% 25V DIP TANT	UNION CARBIDE	K10E25	—
C3	102101	100 μ F 10% 500V CER DISC	ITT	CD10	3
C4	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	25
C5	120018	1 μ SF 10% 63V POLYCARB	ASHCROFT	A2B1521B	2
C6	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C7	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C8	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C9	102101	100 μ F 10% 500V CER DISC	ITT	CD10	—
C10	150020	10 μ F 20% 25V DIP TANT	UNION CARBIDE	K10E25	—
C11	150020	10 μ F 20% 25V DIP TANT	UNION CARBIDE	K10E25	—
C12	150020	10 μ F 20% 25V DIP TANT	UNION CARBIDE	K10E25	—
C13	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C14	101103	10nF 25% 250V CER DISC	ITT	CD10	5
C15	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C16	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C17	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C18	102121	120 μ F 10% 500V CER DISC	ITT	CD10	1
C19	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C20	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C21	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C22	120018	1 μ SF 10% 63V POLYCARB	ASHCROFT	A2B1521B	—
C23	102102	1nF 10% 500V CER DISC	ITT	CD10	2

NOTES

SEE SHEET 2 FOR LATEST ISSUE

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DATE	22.12.82	datron ELECTRONICS LTD	
DRAWN	IL	TITLE	
CHECKED		1081 AC PCB ASSY	
APPROVED		DRAWING NUMBER	400504
DATE		SHEET	10 OF 19

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C24	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C25	101103	10nF 25% 250V CER DISC	ITT	CD10	—
C26	102101	100 μ F 10% 500V CER DISC	ITT	CD10	—
C27	102680	68 μ F 5% 500V CER DISC	ITT	CD10	1
C28	150004	100 μ F 20% 6V3 DIP TANT	UNION CARBIDE	K100E6V3	1
C29	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C30	110013	100nF 20% 250V POLYESTER	MULLARD	C280AE P100K	1
C31	102150	15 μ F 5% 500V CER DISC	ITT	CD10	2
C32	102150	15 μ F 5% 500V CER DISC	ITT	CD10	—
C33	102478	4 μ 7F \pm .5 μ F 500V CER DISC	ITT	CDO8	2
C34	102478	4 μ 7F \pm .5 μ F 500V CER DISC	ITT	CDO8	—
C35	102228	2 μ 2F \pm .5 μ F 500V CER DISC	ITT	CDO8	1
C36	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C37	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C38	150023	33 μ F 20% 25V DIP TANT	UNION CARBIDE	K33E25	1
C39	130065	1n8F 1% 63V POLYSTYRENE	SUFLEX	HS1800/1-10/63	2
C40	130065	1n8F 1% 63V POLYSTYRENE	SUFLEX	HS1800/1-10/63	—
C41	130082	680 μ F 1% 30V POLYSTYRENE	SUFLEX	HS	2
C42	102108	1 μ F \pm .5 μ F 500V CER DISC	ITT	CDO6	1
C43	130070	13 μ F \pm .5 μ F 160V POLYSTYRENE	SUFLEX	HS	2
C44	140058-1	150 μ F x2 MATCHED SET	DATRON	SEE DRG	1
C45	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C46	130070	13 μ F \pm 1 μ F 160V POLYSTYRENE	SUFLEX	HS13/1-7/160	—

NOTES

SEE SHEET 2 FOR LATEST ISSUE

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DATE	22.12.82	datron ELECTRONICS LTD	
DRAWN	IL	TITLE	
CHECKED		1081 AC PCB ASSY	
APPROVED		DRAWING NUMBER	400504
DATE		SHEET	10 OF 19

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	090107-1	5K0 0.1% WIRE WOUND	MANN	MATCHED SET (R1-R3)	(1 SET)
R2	090001	P.T.C. THERMISTOR	MULLARD	VA0650	2
R3	090107-1	1M0 0.1% WIRE WOUND	MANN		-
R4		NOT USED			-
R5		NOT USED			-
R6	000392	3K9 5% 1/4W CARBON	MULLARD	CR25	2
R7	000106	10M " " "	"	"	3
R8	019761	9K76 1% 50ppm M.F.	HOLCO	H8	1
R9	090001	P.T.C. THERMISTOR	MULLARD	VA0650	-
R10	000223	22k 5% 1/4W CARBON	MULLARD	CR25	2
R11	000106	10M 5% 1/4W CARBON	MULLARD	CR25	-
R12	000563	56K " " "	"	"	3
R13	000563	56K " " "	"	"	-
R14	000121	120R " " "	"	"	1
R15	011502	15k0 1% 1/8W 50ppm MF	HOLCO	H8C	1
R16	011212	12k1 " " "	"	"	1
R17	000273	27k 5% 1/4W CARBON	MULLARD	CR25	3
R18	090111-	100M " THICK FILM	HOLSWORTHY	SEE DRG	1
R19	000104	100K " 1/4W CARBON	MULLARD	CR25	7
R20	000104	100k " " "	"	"	-
R21	000104	100k " " "	"	"	-
R22	000222	2K2 5% 1/4W CARBON	"	"	2
R23	000391	390R " " "	"	"	1

NOTES: CIRCUIT DIAGRAM = 430505
CHECK PROCEDURE = 460505
CHECK LIST = 470505
SEE SHEET 2 FOR LATEST ISSUE

REV	A	1	2
E.C.O.			1484.1500
DATE		31.3.83	18.5.83
CHKD			MD

DATE	8.12.82	datron ELECTRONICS LTD	
DRAWN	LL	TITLE	1081 OHMS PCB ASSY.
CHECKED	LOG/MD	DRAWING NUMBER	400505
APPROVED	RWF	SHEET	2 OF 12
DATE	31-3-83		

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	070160-2	57k33 0.1% 1ppm WW	MANN	SEE DRG	1
R25	070161-2	573k3 0.1% 1ppm WW	MANN	SEE DRG	1
R26	063104	100K POT CERMET	BECKMANN	72 P	1
R27		NOT USED			-
R28	000105	1M 5% 1/4W CARBON	MULLARD	CR25	3
R29	070159-2	5k733 0.1% 1ppm WW	MANN	SEE DRG	1
R30	070158-2	1k274 0.1% 1ppm WW	MANN	SEE DRG	2
R31	070158-2	1k274 0.1% 1ppm WW	"	SEE DRG	-
R32	000473	47k 5% 1/4W CARBON	MULLARD	CR25	6
R33	000473	47k 5% 1/4W CARBON	MULLARD	CR25	-
R34	001271	270R 5% 1/2W CARBON	"	CR37	1
R35	041004	1M00 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	1
R36	015621	5k62 1% 1/8W 50ppm MF	HOLCO	H8C	1
R37	012742	27k4 1% 1/8W 50ppm MF	HOLCO	H8C	2
R38	012742	27k4 1% 1/8W 50ppm MF	HOLCO	H8C	-
R39		F.S.V			-
R40		F.S.V			-
R41	000473	47K 5% 1/4W CARBON	MULLARD	C	-
R42	000624	620K " " "	"	"	1
R43	000473	47K " " "	"	"	-
R44	000102	1K " " "	"	"	3
R45	000102	1K " " "	"	"	-
R46	000562	5K6 " " "	"	"	1

NOTES:
SEE SHEET 2 FOR LATEST ISSUE

REV	A	1	2
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DATE	8.12.82	datron ELECTRONICS LTD	
DRAWN	LL	TITLE	1081 OHMS PCB ASSY.
CHECKED		DRAWING NUMBER	400505
APPROVED		SHEET	3 OF 12
DATE			

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	Nc. USED Per Assy.
RL1	330012-1	REED RELAY 1A GUARDED	HAMLIN	HE721A5134	4
RL2	330018-1	RELAY 2P2W 7V HOLD-IN	AMF	SEE DRG	2
RL3	330018-1	RELAY 2P2W 7V HOLD-IN	AMF	SEE DRG	-
RL4	330012-1	REED RELAY 1A GUARDED	HAMLIN	HE721A5134	-
RL5	330012-1	REED RELAY 1A GUARDED	HAMLIN	HE721A5134	-
RL6	330012-1	REED RELAY 1A GUARDED	HAMLIN	HE721A5134	-
	450388-1	GUARD SHIELD			1
	400379/5	WIRE/TERMINAL ASSY			1
	410217-2	PCB			1
	459112-2	RELAY BRACKET			2
	540002	22SWG BTC WIRE			A/R
	540008	7/02 PTFE INSUL.(WHITE)WIRE			490mm
J1, J2	571095/c	16 WAY AP/3M RIBBON CABLE			2
	590001	SLEEVE MAX CABLE ϕ 3.0	HELLERMANN ELECTRIC	H15 x 20mm BLACK HELSYN	7
	590004	SLEEVE - PTFE	HELLERMANN ELECTRIC	FE10	A/R
	605059	8WAY D.I.L. SOCKET			4
	602001	FSV TERMINAL	MOLEX	02-04-1675	2
	602004	BREAKAWAY TERM. STRIP	MOLEX	05-30-0001	16
J3	605052	8WAY POLARISED SOCKET	MOLEX	(22-01-2085)6471-8-1	1
	605060	14 PIN DIL SOCKET	ASTRALUX	1CL143-S3T	2
	605061	16 PIN DIL SOCKET	ASTRALUX	1CL163-S6T	6
	605057	CRIMP TERMINAL	MOLEX	4809-CL	2

NOTES

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datron ELECTRONICS LTD

1081 AC PCB ASSY

DRAWING NUMBER 400504

SHEET 19 OF 19

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	Nc. USED Per Assy.
	611007	M3x6mm POZICK STEEL	ZN.PL.		3
	611016	M3x8mm POZIPAN STEEL	ZN.PL.		5
	612021	M3x16mm SPACER	HARWIN	R6377-02	3
	613005	M3 INT. SHAKEPROOF			2
	613014	M2.5 INT. SHAKEPROOF			2
	615002	M3 FULL NUT STEEL ZN.PL.			2
	615005	3-48UNC FULL NUT STEEL	ZN.PL.		2
	617010	NYLATCH PLUNGER 3/16"	HARTWELL CORP	HN3P-32-4-1	5
	617011	NYLATCH GROMMET 3/16"	HARTWELL CORP	HN3G-32-1	5
	620003	SOLDER PIN	HARWIN	H2105 A01	4
	620005	CLOVERLEAF PTFE INSUL.	SEAELECTRO	FTE15P59	18
	620007	TEST POINT TERMINAL	MICROVAR	TYPE C30	10
	630107	BRASS STRIP 15.5 x .38mm	RIGHTON	CZ108 1/2H	220mm
	613029	M3 CRINKLE WASHER S.S.			3

NOTES

SEE SHEET 2 FOR LATEST ISSUE

NO.

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DATE 22.12.82

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DATE

datron ELECTRONICS LTD

TITLE 1081 AC PCB ASSY

DRAWING NUMBER 400504

SHEET 19 OF 19

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M1	280022	QUAD BILATERAL SWITCH	MOTOROLA	MC 1401G BCP	2
M2	280022	" " "	"	"	-
M3	260027	OP AMP 714	FAIRCHILD	UA714 HC	1
M4	260026	OP AMP	NATIONAL	LM212	1
M5	280025	QUAD ANALOGUE SWITCH	MOTOROLA	MC 14066 BCP	1
M6	280072	MSTABLE /ASTABLE M/VIBR	R.C.A.	CD 4047 AE	1
M7	280015	QUAD LATCH	MOTOROLA	MC 14076 BCP	2
M8	280015	" "	"	"	-
M9	280011	DUAL D FLIP FLOP	MOTOROLA	MC 14013 BCP	1
M10	260053	7650 OP AMP	INTERSIL	ICL7650 CPD	1

NOTES

SEE SHEET 2 FOR LATEST ISSUE

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DATE	8.12.82	datron ELECTRONICS LTD
TITLE	1081 OHMS PCB ASSY	
DRAWN	<input type="checkbox"/>	DRAWING NUMBER 400505
CHECKED	<input type="checkbox"/>	
APPROVED	<input type="checkbox"/>	SHEET 10 OF 12
DATE		

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
RL1	330019-	RELAY 4P2W 7 $\frac{1}{2}$ HOLD-IN AMF		SEE DRAWING	1
	400379/2	WIRE / TERMINAL ASSY			6
	410218-	OHMS PCB.			1
	459112-2	RELAY BRACKET.	KDP		1
	540008	7/0-2 PTFE INSULATED WHITE		TYPE C	280mm.
	540002	22 SWG TINNED COPPER WIRE			A/R
	590001	SLEEVE MAX CABLE ϕ 3.0	HELLERMANN ELECTRIC	H15 X 20mm BLK HELSYN	9
	590004	SLEEVE P.T.F.E	"	FE10	A/R
	590055	SLEEVE ϕ 1.0 SIL. RUBBER	HELLERMANN ELECTRIC	H15 CONT. BLACK	30mm
	602001	F.S.V. TERMINAL	MOLEX	02-04-1875	4
J2	571095/C	16 WAY AP 3M RIBBON CABLE	DATRON		1
	605060	14 WAY DIL SOCKET	ASTRALUX	ICL-143-S3T.	5
	605061	16 WAY DIL SOCKET	ASTRALUX	ICL-163-S6T.	2
J1	605053	2 WAY POLARISED SOCKET	MOLEX	22-01-2125	1

NOTES

SEE SHEET 2 FOR LATEST ISSUE

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DATE	
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DATE	8.12.82	datron ELECTRONICS LTD
TITLE	1081 OHMS PCB ASSY.	
DRAWN	<input type="checkbox"/>	DRAWING NUMBER 400505
CHECKED	<input type="checkbox"/>	
APPROVED	<input type="checkbox"/>	SHEET 11 OF 12
DATE		

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	590001	SLEEVE MAX CABLE ϕ 3-D _{min}	HELLERMANN ELECTRIC	H15 x 20 _{min} BLK HELSYN	25
	590004	SLEEVE - PTFE	" "	FE 10	A/R
	602007	RELAY SOCKET 2 POLE PCB MOUNT	POTTER & BRUMFIELD	27E 212	1
	602008	RELAY SOCKET 4 POLE PCB MOUNT	" "	27E 213	1
J10, J11	604008	7 WAY PLUG PANEL MOUNT	PYE CONNECTORS	M7P	2
	605009	7 WAY SOCKET	PYE CONNECTOR	M7S	2
	605060	14 WAY DIL SOCKET	ASTRALUX OR JERMYN	ICU-246-54T or A23-2023Y	1
	605057	CRIMP TERMINAL	MOLEX	4200-GL	2
	606001	LOCKING HOOD	PYE CONNECTORS	MHN	2
	606002	NUT	PYE CONNECTORS	MN	2
	606003	WASHER	" "	MLW	2
	611004	SCREW M3x6 _{min} STEEL POZI-PAN ZINC PLATED	GKN		7
	611007	SCREW M3x6 _{min} STEEL POZI-CSK ZINC PLATED	GKN		7
	611016	" M3x8 _{min} " " PAN " " "			4
	612020	STANDOFF NYLON M3x19 TRANSPIILLAR	W.K. ELECTRONICS	TP1/G-5/19/M3/I/I	5

NOTES

SEE SHEET 3 FOR LATEST ISSUE

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DATE	10.2.83	datron ELECTRONICS LTD
DRAWN	IL	
CHECKED		TITLE
APPROVED		REAR INPUT / RATIO
DATE		ASSY 1081
		DRAWING NUMBER
		400506
		SHEET
		7 OF 8

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	613005	WASHER M3 INT/SHAKE PROOF ST	GKN DISTRIBUTORS	ZINC PLATED	13
	615001	NUT BBA FULL HEX STEEL		ZINC PLATED	2
	615002	" M3 " " "		" "	2
	630005	CLIP FOR P#B RIO 2 POLE RELAY	POTTER & BRUMFIELD	20C249	1
	630028	CLIP FOR P#B RIO 4 POLE RELAY	" "	20C250	1

NOTES

SEE SHEET 3 FOR LATEST ISSUE

REV																				
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DATE	10.2.83	datron ELECTRONICS LTD
DRAWN	IL	
CHECKED		TITLE
APPROVED		REAR INPUT / RATIO
DATE		ASSY 1081
		DRAWING NUMBER
		400506
		SHEET
		8 OF 8

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M1	280011	DUAL D FLIP-FLOP	MOTOROLA	MC14013 BCP	2
M2	280022	QUAD BILATERAL SWITCH	"	MC14016BCP	1
M3	280024	TRI-STATE HEX NON-INV. BUFFER	"	MC14503BCP	7
M4	280024	" " " " " "	"	"	-
M5	280024	" " " " " "	"	"	-
M6	280024	" " " " " "	"	MC14076 BCP	5
M7	280015	QUAD LATCH	"	"	-
M8	280015	" " " " " "	"	"	-
M9	280015	" " " " " "	"	MC14503BCP	-
M10	280024	TRI-STATE HEX NON-INV. BUFFER	"	MC14076 BCP	-
M11	280015	QUAD LATCH	"	"	-
M12	280015	" " " " " "	"	MC14516BCP	2
M13	280044	BINARY UP/DOWN COUNTER	"	"	-
M14	280044	" " " " " "	"	"	-
M15	290003	TIMER - ASTABLE	SIGNETICS	NE 555V	3
M16	270058	DUAL 1-of-4 DECODER	NATIONAL	74LS155	1
M17	270048	QUAD 2 1/P NAND GATE	NATIONAL	74LS00	2
M18	290120-19C	2532 EPROM PROGRAMMED	DATRON	TMS2532JL(290120-1SS)	1
M19	280066-1	256x4 BIT STATIC CMOS RAM	SEE DRAWING		2

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

REV									
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DATE	13.12.82	datron ELECTRONICS LTD TITLE 1081 DIGITAL PCB. ASSY.
DRAWN	11	
CHECKED		DRAWING NUMBER 400526
APPROVED		12 SHEET
DATE		

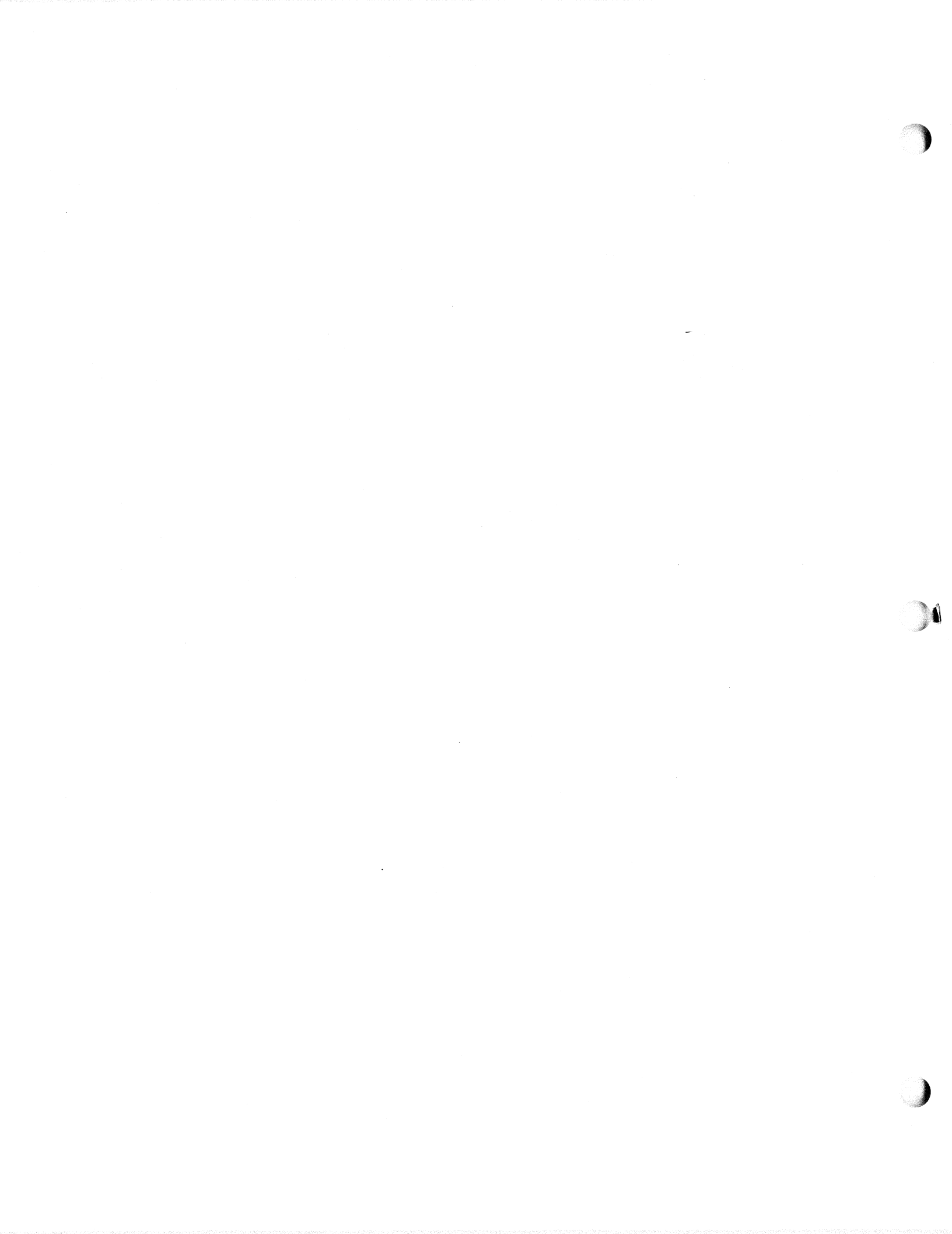
DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M20	280066-1	256x4 BIT STATIC CMOS RAM	SEE DRAWING	DM 74LS125N	1
M21	270064	QUAD TRISTATE BUFFER	NATIONAL	MC14013BCP	-
M22	280011	DUAL D FLIP-FLOP	"	ZNA 2035	1
M23	270053	A-D CHIP	FERRANTI	MC14503BCP	-
M24	280024	TRI-STATE HEX NON-INV. BUFFER	MOTOROLA	"	-
M25	280024	" " " " " "	"	MC14027BCP	1
M26	280006	DUAL J-K FLIP-FLOP	"	"	-
M27		NOT USED			-
M28	270051	DUAL 4 1/P AND GATE	NATIONAL	74LS21	2
M29	270055	DUAL 4 1/P NAND GATE	"	74LS20	2
M30	290119-19C	2532 EPROM PROGRAMMED	DATRON	TMS 2532 JL (290119-1SS)	1
M31	280096	1K x 4BIT STATIC CMOS RAM	SEE DRAWING		2
M32	270069	BCD/ DECIMAL DECODER LS	NATIONAL	74LS42N	1
M33	270051	DUAL 4 1/P AND GATE	"	74LS21	-
M34	270055	DUAL 4 1/P NAND GATE	"	74LS20	-
M35	290118-19C	2532 EPROM PROGRAMMED	DATRON	TMS 2532 JL (290118-1SS)	1
M36	280096	1K x 4BIT STATIC CMOS RAM	SEE DRAWING		-
M37	280025	QUAD BILATERAL SWITCH	MOTOROLA	MC14066BCP	2
M38	280071	TRIPLE 3 1/P NOR GATE	MULLARD	HEF 4025 P	2
M39	280017	HEX INVERTER	MOTOROLA	MC14069 BCP	1
M40	280083	QUAD 2 1/P NOR GATE	MULLARD	HEF 4001 BP	1
M41		NOT USED			-
M42		NOT USED			-

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

REV									
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DATE	13.12.82	datron ELECTRONICS LTD TITLE 1081 DIGITAL PCB. ASSY.
DRAWN	11	
CHECKED		DRAWING NUMBER 400526
APPROVED		13 SHEET
DATE		



DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M43	290003	TIMER - ASTABLE	SIGNETICS	NE 555V	-
M44	270048	QUAD 2 I/P NAND GATE	NATIONAL	74 LS 00	-
M45	270050	HEX INVERTER	"	74 LS 04	1
M46	280025	QUAD BILATERAL SWITCH	MOTOROLA	MC14066BCP	-
M47	280070	DIVIDE-BY-8 COUNTER/DIVIDER	MULLARD	HEF 4022P	1
M48	280071	TRIPLE 3 I/P NOR GATE	"	HEF 4025P	-
M49	280023	QUAD 2 I/P NOR GATE	MOTOROLA	MC14001BCP	1
M50		NOT USED			-
M51		NOT USED			-
M52	270056	8 I/P NAND GATE	NATIONAL	74 LS 30	1
M53	280061	MICRO PROCESSOR CHIP	MOTOROLA	MC 6800L	1
M54	270023	QUAD 2 I/P NAND GATE	NATIONAL	7437	1
M55	270054	QUAD 2 I/P AND GATE	"	74 LS 08	2
M56	270054	" " " "	"	"	-
M57	270057	DUAL JK FLIP-FLOP	"	74 LS 76	1
M58	280009	HEX INVERTER/BUFFER	MOTOROLA	MC14049	2
M59	280009	HEX INVERTER/BUFFER	MOTOROLA	MC14049	-
M60, M62	260031	VOLTAGE DETECTOR	INTERSIL	ICL 8211	2
M61	290003	TIMER - ASTABLE	SIGNETICS	NE 555V	-
S1		NOT USED			-
S2		NOT USED			-
S3		NOT USED			-

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

REV.																				
E.C.O.																				
DATE																				
CHGD																				

DATE	13.12.82	datron ELECTRONICS LTD	
DRAWN	11	TITLE	1081 DIGITAL PCB ASSY.
CHECKED		DRAWING NUMBER	400526
APPROVED		SHEET	14 OF 16
DATE			

J.P. 1304

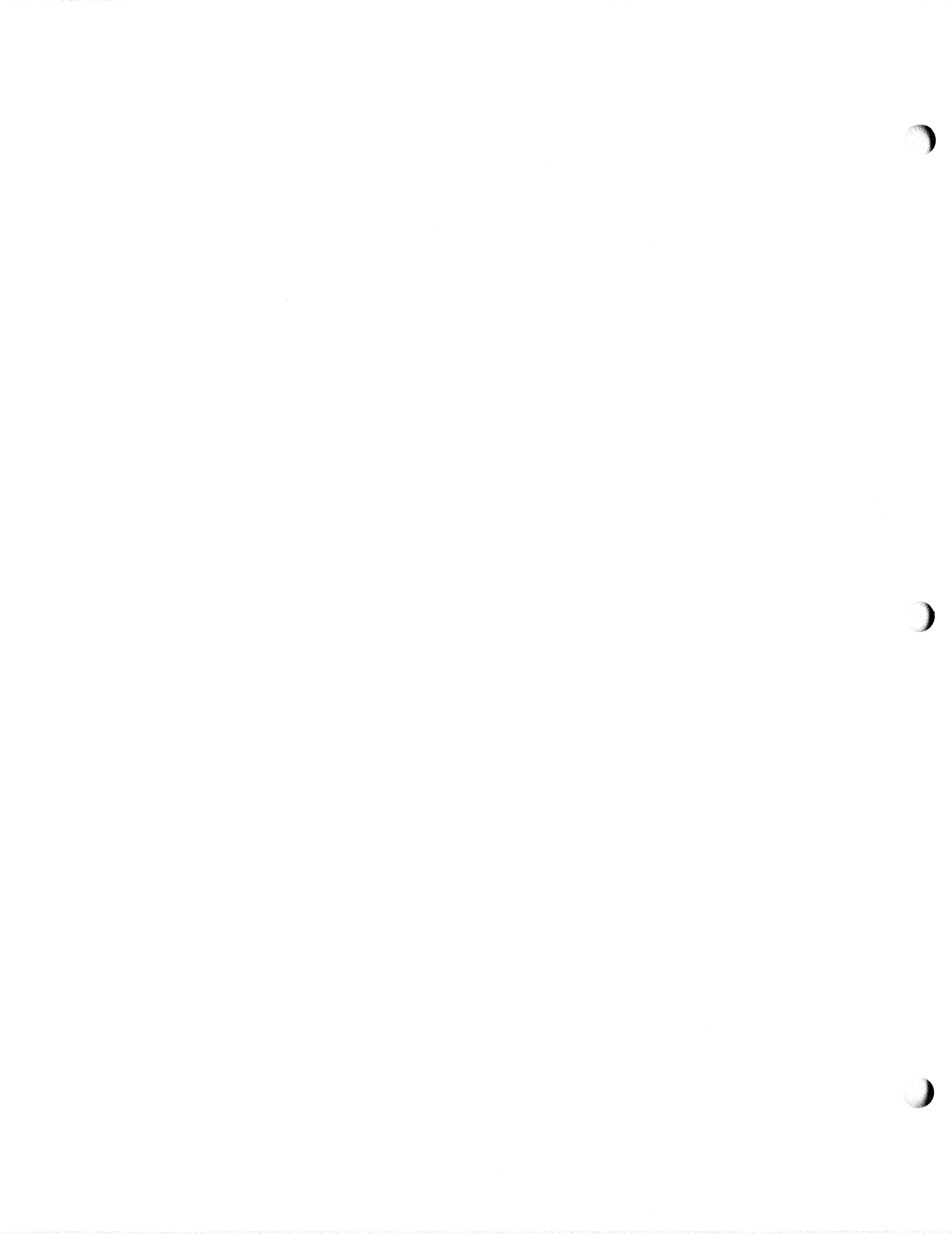
DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
L1	370004	100 μ H R.F. CHOKE	SIGMA	SC10/100	1
	590004	SLEEVE - PTFE	HELLERMANN ELECTRIC	FE10	A/R
	590055	SLEEVE ϕ 1.0 SIL. RUBBER	" "	HIS CONT. BLACK	10mm
	540002	22 SWG. BTC WIRE			A/R
	920048-1	BUS STRIP	MEKTRON	M823 14 7.3F	1
	613018	4BA NYLON WASHER			2
	630098	COMPONENT CLIP	RICHCO	KKU-8	1
	606005	CLIP FOR 605002	ANTIFERRENCE	RC 74	3
J1, J2, J4	605002	16 WAY D.I.L. LOW PROFILE SKT.	JERMYN OR ANTIFERRENCE	A23-2001/Y or ICN-163-S3	3
	605065	28 WAY D.I.L. " " "	AUGAT	328-AG39D	1
	605060	14 WAY D.I.L. SOCKET	ASTRALUX OR JERMYN	ICL 143-S3T	22
	605061	16 WAY D.I.L. SOCKET	" "	ICL 163-S6T	24
	605050	40 WAY D.I.L. SOCKET	AUGAT	340-AG39D	1
	605063	22 WAY D.I.L. SOCKET	AUGAT	322-AG39D	2
	605064	24 WAY D.I.L. SOCKET	"	324-AG39D	3
	605062	18 WAY D.I.L. SOCKET	"	318-AG39D	2
JL3	604037	PROGRAMMING CLASS160 PLUG	"	8136-475G8	1
	605059	8 WAY D.I.L. SOCKET	ASTRALUX	ICL-083-S6T	1
J5	605052	8 WAY POLARISED SOCKET	"	22-01-2085	1
	617010	NYLATCH PLUNGER	ORDER FROM GJ FOX & SONS	HN3P-32-4-1	8
	617011	NYLATCH GROMMET	" " " "	HN3G-32-1	8
J3	605102	24 WAY D.I.L. SOCKET. GOLD	CA	CA-245-10SD	1
	410096-10	PCB			1

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

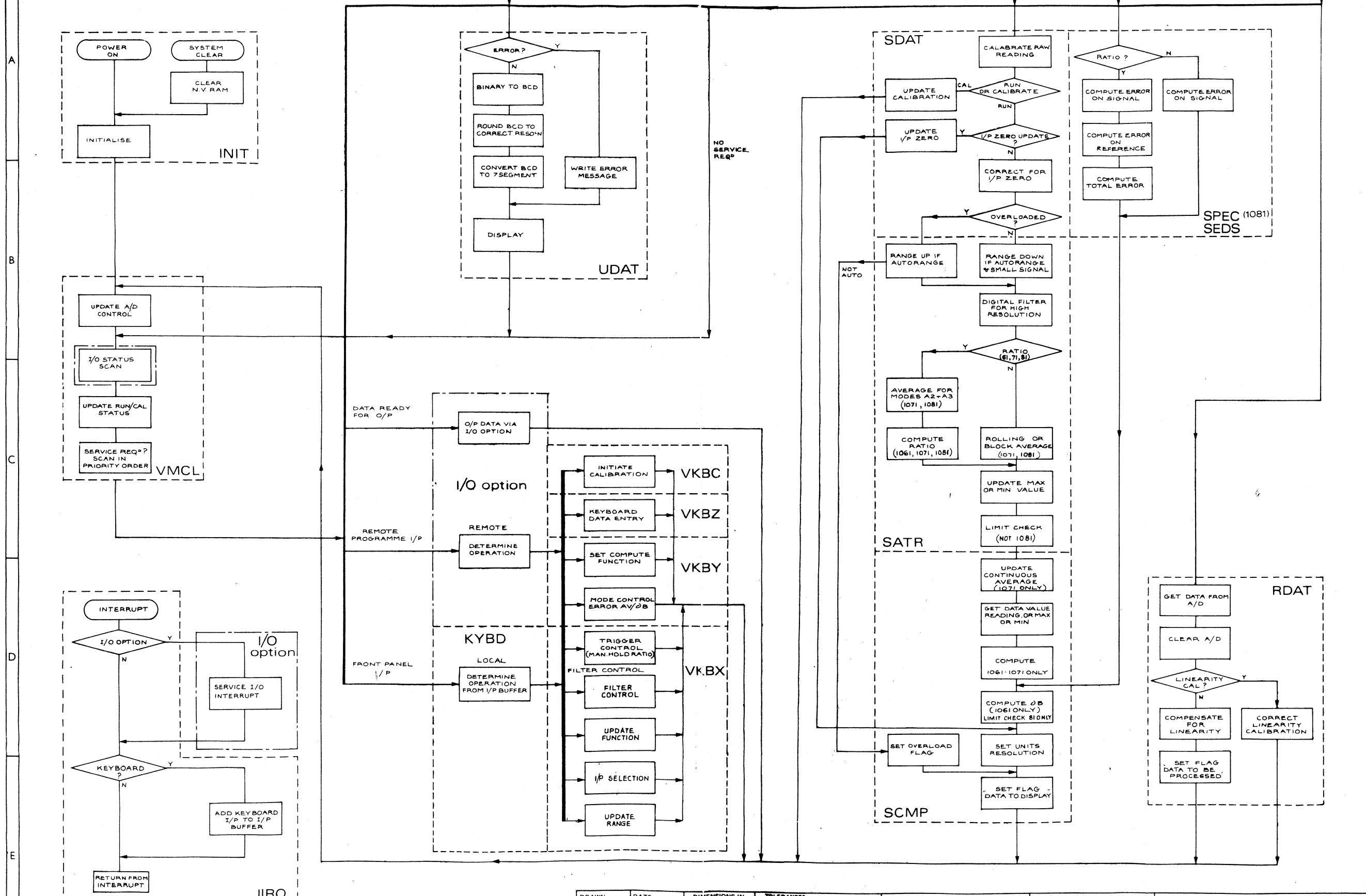
REV.																				
E.C.O.																				
DATE																				
CHGD																				

DATE	13.12.82	datron ELECTRONICS LTD	
DRAWN	11	TITLE	1081 DIGITAL PCB ASSY.
CHECKED		DRAWING NUMBER	400526
APPROVED		SHEET	15 OF 16
DATE			



DRAWING No.
890043

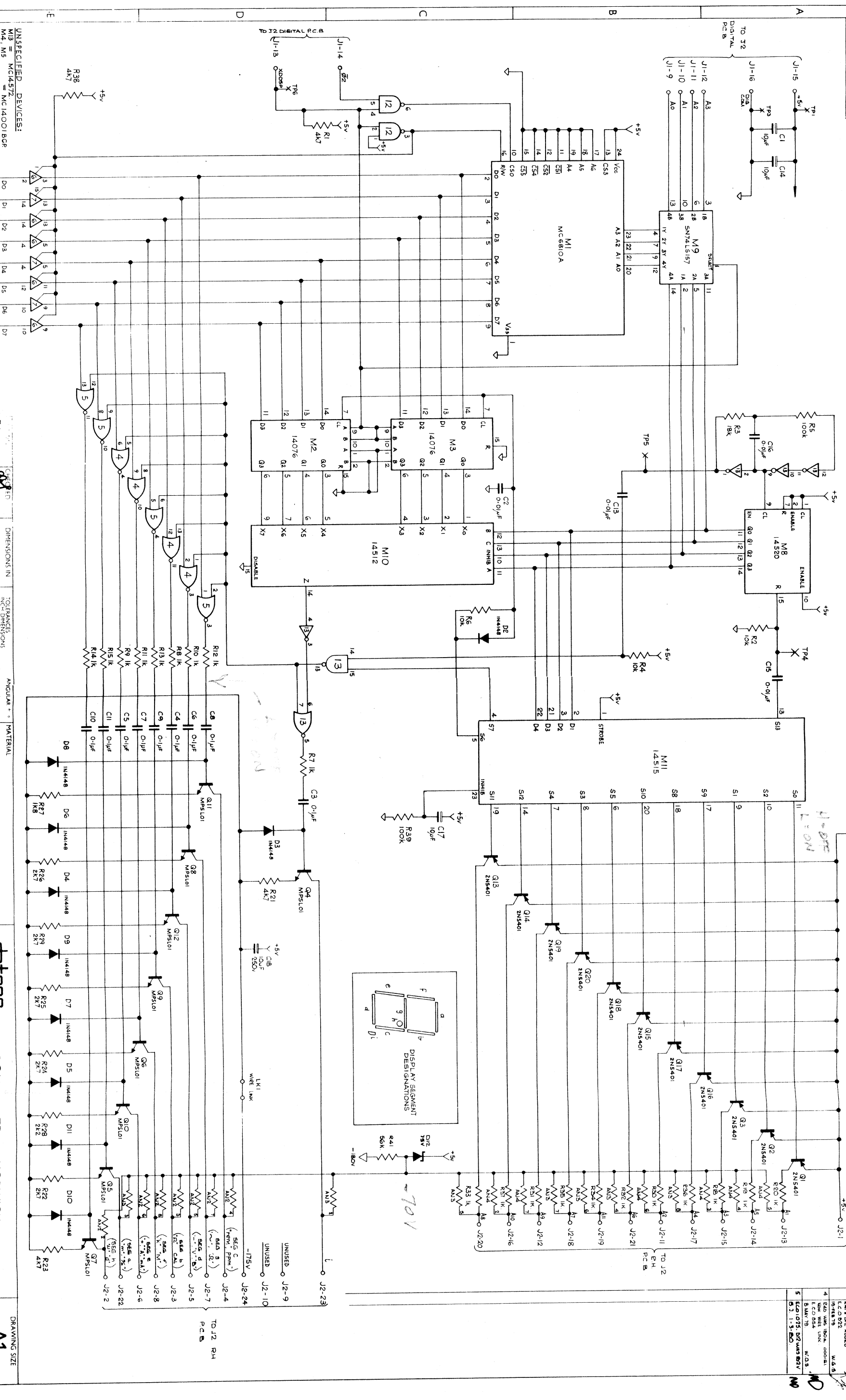
ISS CHANGES
12 ECO 1267
6 1/2 DIGIT MOD
AND GENERAL
UPDATE
J.R. 9.2.82



MASTER PROGRAM SOURCE

DRAWN JR	DATE 12-1-82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± 0.1mm DECIMAL TO 1 PLACE ± 0.2mm WHOLE DIMENSIONS ± 0.4mm ANGULAR ± 30'	MATERIAL	ASSY DRG & PARTS LIST	TITLE MASTER PROGRAM SOURCE	DRAWING No. 890043
CHECKED G.B.	DATE 9-2-82	SCALE	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION	FINISH	CIRCUIT DIAGRAM CHECK PROCEDURE CHECK LIST		SHEET 1 OF 27
APPR.	DATE	NOT TO BE SCALED					

datron
ELECTRONICS
LIMITED
NORWICH



UNSPECIFIED DEVICES:
 M1 = MC8810A
 M2 = M4076
 M3 = M4076
 M4 = M4512
 M5 = M4515
 R1-R57 = 5% 1/4W CARBON FILM
 C1-C17 = 20% 250V POLYESTER
 D1-D11 = 10% 250V POLYESTER
 TP1-TP6 = TEST POINTS
 J1-J16 = DIGITAL P.C.B.
 J2-J23 = DIGITAL P.C.B.

TOLERANCES UNLESS OTHERWISE STATED:
 DIMENSIONS IN MILLIMETERS
 ANGULAR DIMENSIONS IN DEGREES
 DECIMAL DIMENSIONS TO 3 PLACES
 DECIMAL DIMENSIONS TO 2 PLACES
 DECIMAL DIMENSIONS TO 1 PLACE
 UNLESS OTHERWISE STATED

FINISH: _____
MATERIAL: _____
DATE: 30.10.78
NOT TO BE SCALED

datron ELECTRONICS LTD. NORWICH.
 DISPLAY DRIVER PCB 1071/1081
 DRAWING NO. 430301
 SHEET 1 OF 1
 DRAWING SIZE A1

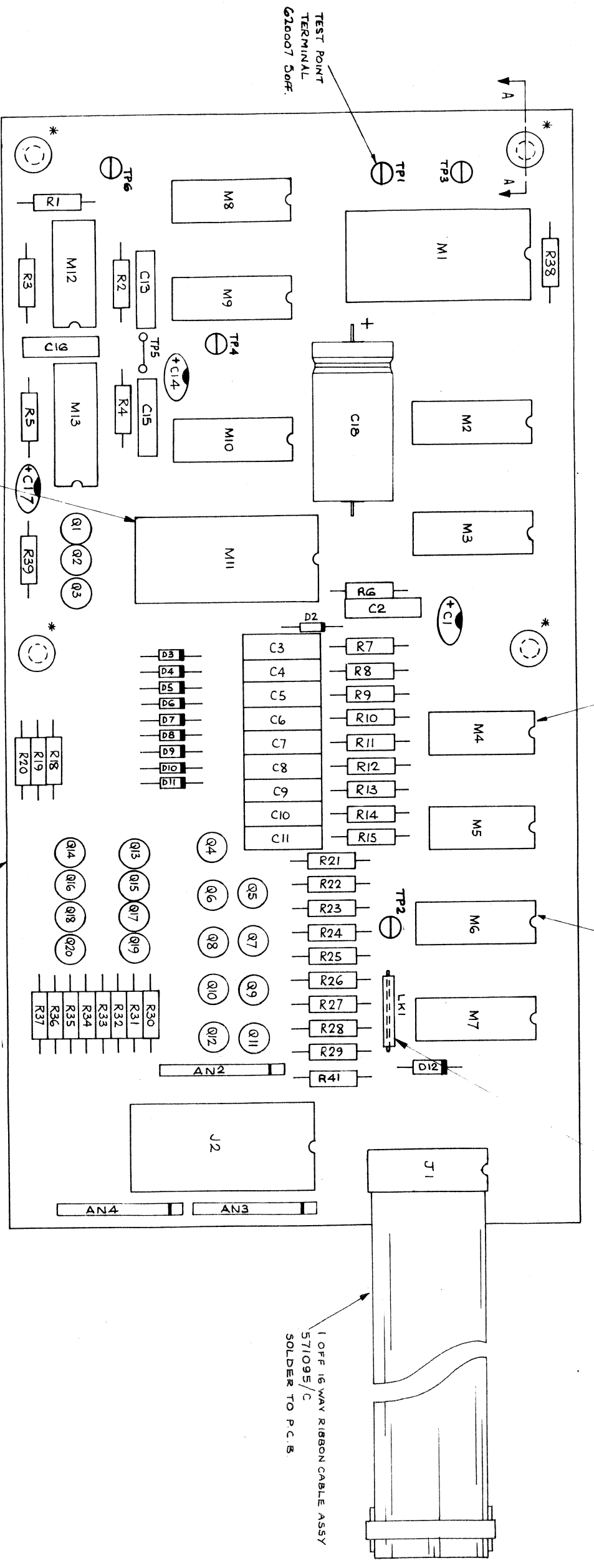
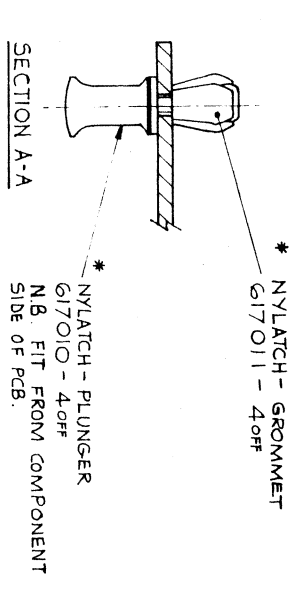
DISPLAY DRIVER

DRAWING No. 400301
 FIRST USED ON
THIRD ANGLE PROJECTION
 DRAWN IN ACCORDANCE WITH BS 308

ALL BURS TO BE REMOVED

NOTES

1. MAKE TP1-TP6 FROM 22 SWG BTC WIRE - PART N° 540002.



ISS.	CHANGES
C	RELEASED TO PRODUCTION
1	29.3.78
2	C18 ADDED # 240 ECO 1252 17 NOV 78 W.G.S
3	R41 ADDED ALL 2-NM4 & DIV ADDED ECO 8972 19 FEB 79 W.G.S
4	R40 WAS 180G ECO 954 R40 WAS 180W WIRE LINK ECO 954 R40 WAS 180W WIRE LINK ECO 954 R40 WAS 180W WIRE LINK ECO 954
5	CLIP FOR J1 WAS G06005 ECO 904 21.6.79
6	ECO 1000 & 1025 RIBBON CABLE CLIP W/5 G06007, 8, 9 DIE WAS 82V. 1988
7	ECO 1217 J1 WAS 16 WAY SOCKET OK 17.8.81
8	ECO 1253 PARTS LIST CHANGED TO 32 DR 2.12.81

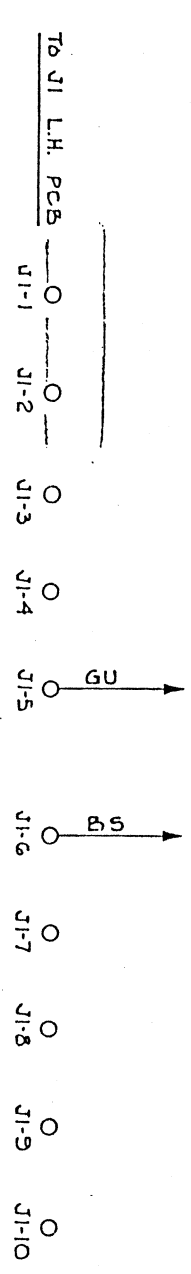
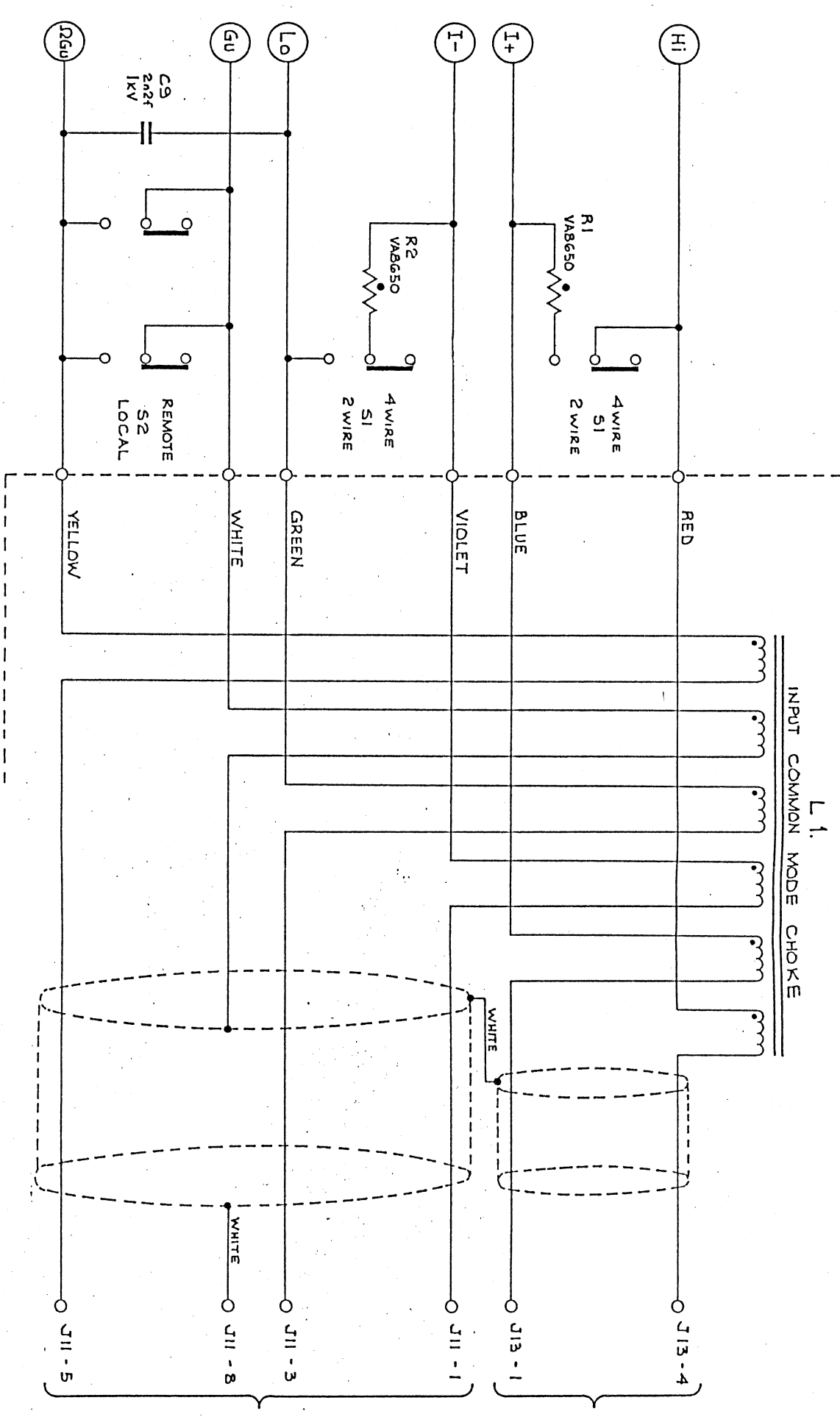
DRAWN I.L.	CHECKED <i>[Signature]</i>	DIMENSIONS IN MILLIMETRES	TOLERANCES INCH DIMENSIONS DECIMAL TO 2 PLACES + .015 DECIMAL TO 1 PLACE + .010 FRACTIONAL ANGULAR + .3°	MATERIAL SEE PARTS LIST	TITLE datron ELECTRONICS LTD. NORWICH. DISPLAY DRIVER PCB ASSY 1071/1081	DRAWING No. 400301	DRAWING SIZE A2
TRACED	APPROVED	SCALE 2:1	HERC DIMENSIONS DECIMAL TO 2 PLACES + .1mm DECIMAL TO 1 PLACE + .2mm WHOLE DIMENSIONS + .4mm UNLESS OTHERWISE STATED	FINISH			SHEET 1 OF 7
DATE 3.5.78	DATE	NOT TO BE SCALED					

DISPLAY DRIVER PCB

DRAWING No.
430294

FRONT PCB
400294

SIGNAL CABLE ASSY
400573

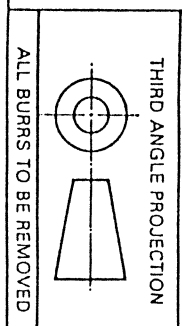


To J1 L.H. PCB
J1-1 J1-2 J1-3 J1-4 J1-5 J1-6 J1-7 J1-8 J1-9 J1-10

- NOTES:
1. GU (J1-5) SCREENS ALL CIRCUITRY ON THIS SHEET.
 2. B.S. SCREENS HI & I+.
 3. DG. SCREENS LO & I-.

TO J13 REAR PCB.
(VIA SIGNAL CABLE 400573)
(WHEN REAR INPUT/RATIO IS
FITTED, CONNECT TO J4 OF
RATIO PCB.)

TO J11 REAR PCB.
(VIA SIGNAL CABLE 400573)
(WHEN REAR INPUT/RATIO IS
FITTED, CONNECT TO J6
OF RATIO PCB.)



THIRD ANGLE PROJECTION
DRAWN B.S. JACKSON DATE 24th JAN 85
CHECKED HSD DATE 29.1.85
APPR B. Jones DATE 29.1.85
DIMENSIONS IN MILLIMETRES
SCALE NOT TO BE SCALED

TOLERANCES
DECIMAL TO 2 PLACES ± 0.1mm
DECIMAL TO 1 PLACE ± 0.2mm
ANGULAR ± 1/2°
UNLESS OTHERWISE STATED

MATERIAL FINISH

ASSY DRG & PARTS LIST } 400294
CIRCUIT DIAGRAM } 430294
CHECK PROCEDURE } 460294
CHECK LIST } 470294

TITLE
FRONT PCB CIRCUIT DIAGRAM

DRAWING No.
430294.
SHEET 2 OF 2

datron
INSTRUMENTS
NORWICH
ENGLAND

ISS CHANGES

2	REDRAWN B.J. 21.3.79.
3	SCREEN FOR HI & I+ NOW CONNECTED TO GU. VIA WHITE WIRE B.J. 11.6.79
4	ECO 1111 C9 ADDED. 11.21.4.80
5	ECO 1472 C10 ADDED (4.7F) 11.21.4.80
6	ECO 1662 SEE SHEET. 1.
7	ECO 1661 C10 DELETED AP. 10.9.84.
8	ECO 1825 B.J. REDRAWN. 25.1.85 CABLE ASSY ADDED TO FRONT PCB ASSY. CHOKE ADDED TO SIGNAL CABLE.

FRONT PCB CRTS 1

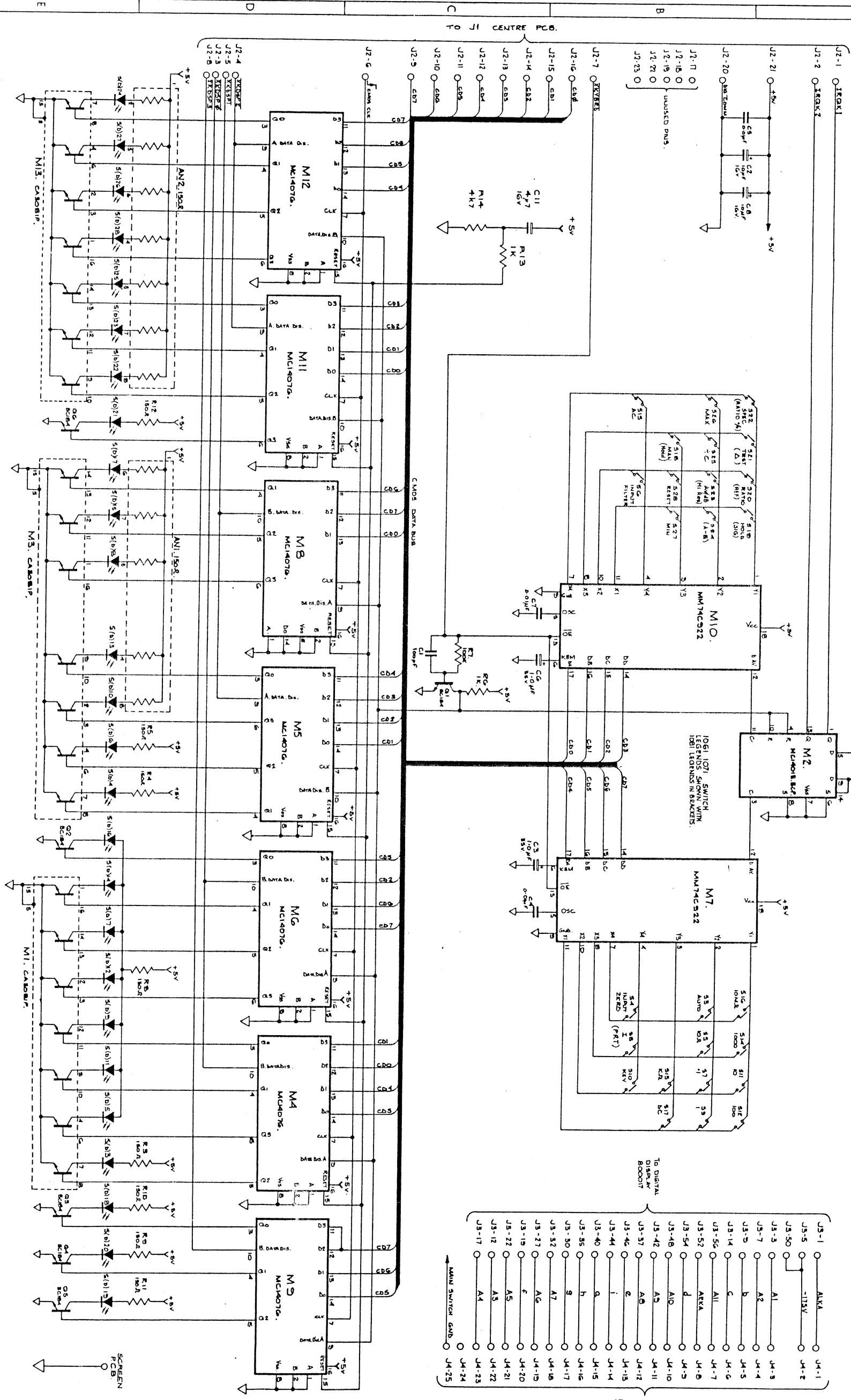
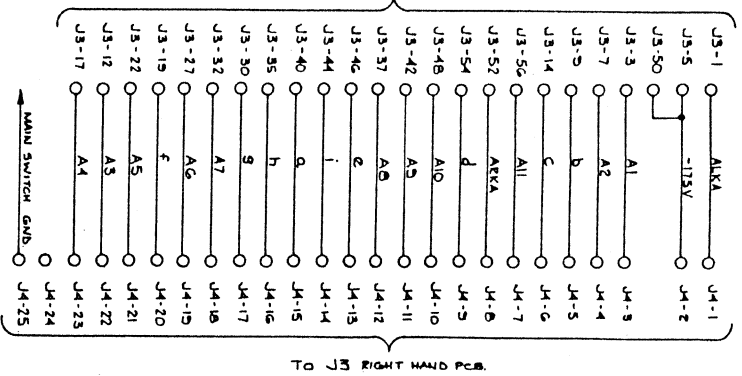
THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES
1. SIGNAL CDR ON J2-16, THERE IS A LINK LIKE IN THIS SIGNAL LINE.

NO.	CHANGES
1	REVISION, B.J.
2	ECO 1661
3	ECO 1672
4	ECO 1673
5	ECO 1674
6	ECO 1675
7	ECO 1676
8	ECO 1677
9	ECO 1678
10	ECO 1679
11	ECO 1680
12	ECO 1681
13	ECO 1682
14	ECO 1683
15	ECO 1684
16	ECO 1685
17	ECO 1686
18	ECO 1687
19	ECO 1688
20	ECO 1689
21	ECO 1690
22	ECO 1691
23	ECO 1692
24	ECO 1693
25	ECO 1694
26	ECO 1695
27	ECO 1696
28	ECO 1697
29	ECO 1698
30	ECO 1699
31	ECO 1700
32	ECO 1701
33	ECO 1702
34	ECO 1703
35	ECO 1704
36	ECO 1705
37	ECO 1706
38	ECO 1707
39	ECO 1708
40	ECO 1709
41	ECO 1710
42	ECO 1711
43	ECO 1712
44	ECO 1713
45	ECO 1714
46	ECO 1715
47	ECO 1716
48	ECO 1717
49	ECO 1718
50	ECO 1719
51	ECO 1720
52	ECO 1721
53	ECO 1722
54	ECO 1723
55	ECO 1724
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90	ECO 1759
91	ECO 1760
92	ECO 1761
93	ECO 1762
94	ECO 1763
95	ECO 1764
96	ECO 1765
97	ECO 1766
98	ECO 1767
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101	ECO 1770
102	ECO 1771
103	ECO 1772
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123	ECO 1792
124	ECO 1793
125	ECO 1794
126	ECO 1795
127	ECO 1796
128	ECO 1797
129	ECO 1798
130	ECO 1799
131	ECO 1800
132	ECO 1801
133	ECO 1802
134	ECO 1803
135	ECO 1804
136	ECO 1805
137	ECO 1806
138	ECO 1807
139	ECO 1808
140	ECO 1809
141	ECO 1810
142	ECO 1811
143	ECO 1812
144	ECO 1813
145	ECO 1814
146	ECO 1815
147	ECO 1816
148	ECO 1817
149	ECO 1818
150	ECO 1819
151	ECO 1820
152	ECO 1821
153	ECO 1822
154	ECO 1823
155	ECO 1824
156	ECO 1825
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172	ECO 1841
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174	ECO 1843
175	ECO 1844
176	ECO 1845
177	ECO 1846
178	ECO 1847
179	ECO 1848
180	ECO 1849
181	ECO 1850
182	ECO 1851
183	ECO 1852
184	ECO 1853
185	ECO 1854
186	ECO 1855
187	ECO 1856
188	ECO 1857
189	ECO 1858
190	ECO 1859
191	ECO 1860
192	ECO 1861
193	ECO 1862
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195	ECO 1864
196	ECO 1865
197	ECO 1866
198	ECO 1867
199	ECO 1868
200	ECO 1869
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207	ECO 1876
208	ECO 1877
209	ECO 1878
210	ECO 1879
211	ECO 1880
212	ECO 1881
213	ECO 1882
214	ECO 1883
215	ECO 1884
216	ECO 1885
217	ECO 1886
218	ECO 1887
219	ECO 1888
220	ECO 1889
221	ECO 1890
222	ECO 1891
223	ECO 1892
224	ECO 1893
225	ECO 1894
226	ECO 1895
227	ECO 1896
228	ECO 1897
229	ECO 1898
230	ECO 1899
231	ECO 1900
232	ECO 1901
233	ECO 1902
234	ECO 1903
235	ECO 1904
236	ECO 1905
237	ECO 1906
238	ECO 1907
239	ECO 1908
240	ECO 1909
241	ECO 1910
242	ECO 1911
243	ECO 1912
244	ECO 1913
245	ECO 1914
246	ECO 1915
247	ECO 1916
248	ECO 1917
249	ECO 1918
250	ECO 1919
251	ECO 1920
252	ECO 1921
253	ECO 1922
254	ECO 1923
255	ECO 1924
256	ECO 1925
257	ECO 1926
258	ECO 1927
259	ECO 1928
260	ECO 1929
261	ECO 1930
262	ECO 1931
263	ECO 1932
264	ECO 1933
265	ECO 1934
266	ECO 1935
267	ECO 1936
268	ECO 1937
269	ECO 1938
270	ECO 1939
271	ECO 1940
272	ECO 1941
273	ECO 1942
274	ECO 1943
275	ECO 1944
276	ECO 1945
277	ECO 1946
278	ECO 1947
279	ECO 1948
280	ECO 1949
281	ECO 1950
282	ECO 1951
283	ECO 1952
284	ECO 1953
285	ECO 1954
286	ECO 1955
287	ECO 1956
288	ECO 1957
289	ECO 1958
290	ECO 1959
291	ECO 1960
292	ECO 1961
293	ECO 1962
294	ECO 1963
295	ECO 1964
296	ECO 1965
297	ECO 1966
298	ECO 1967
299	ECO 1968
300	ECO 1969
301	ECO 1970
302	ECO 1971
303	ECO 1972
304	ECO 1973
305	ECO 1974
306	ECO 1975
307	ECO 1976
308	ECO 1977
309	ECO 1978
310	ECO 1979
311	ECO 1980
312	ECO 1981
313	ECO 1982
314	ECO 1983
315	ECO 1984
316	ECO 1985
317	ECO 1986
318	ECO 1987
319	ECO 1988
320	ECO 1989
321	ECO 1990
322	ECO 1991
323	ECO 1992
324	ECO 1993
325	ECO 1994
326	ECO 1995
327	ECO 1996
328	ECO 1997
329	ECO 1998
330	ECO 1999
331	ECO 2000

FRONT PCB CRT



DRAWN BY	CHECKED BY	DIMENSIONS IN	TOLERANCES	ANGULARS	MATERIAL
B.L.	P.F.	MILLIMETRES	UNLESS OTHERWISE SPECIFIED	UNLESS OTHERWISE SPECIFIED	
TRACED	APPROVED				
DATE	DATE	SCALE	NOT TO BE SCALED		

datron ELECTRONICS LTD. NORWICH.
FRONT PCB. CIRCUIT DIAGRAM 1061/1071/1081

DRAWING No. 430294
SHEET 1 OF 2

FRONT PCB CRTS 2

FRONT PCB

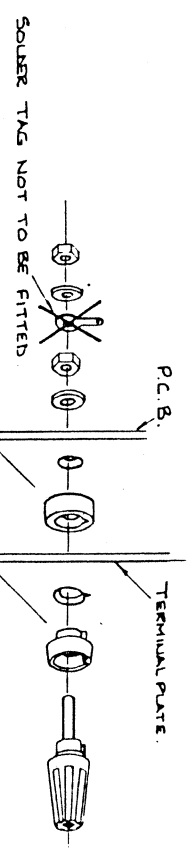
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURS TO BE REMOVED

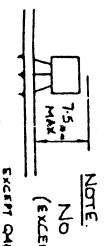
NOTES

- IMPORTANT**
- 1. FIT M1 3.45C B 21112 F13 INTO 16 WAY AUGAT SOCKET PART NO 605061.
 - 2. FIT M7 & M10 INTO AUGAT SOCKET PART NO 605062. 18WAY.
 - 3. FIT M2 INTO AUGAT SOCKET PART NO. 605060. 14 WAY.
2. TO REMOVE DISPLAY:-
CUT PINS HERE
- THIN
RUE
SIDE THIN STEEL RING
BETWEEN DISPLAY PCB TO SPLIT
FOAM TAPE.



ASSEMBLE 6 TERMINALS TO TERMINAL PLATE
No. 450179 & PCB AS SHOWN ABOVE. TERMINAL
COLOURS MUST BE AS INDICATED BELOW.

RESISTORS R1 & R2
2 OFF INSULATING BEAMS G30024
ASSEMBLED ON EACH LEG A SHOWN
RESISTORS TO BE MOUNTED ON
THE UNDER SIDE OF BOARD.



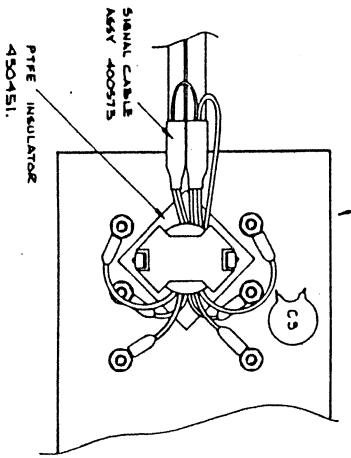
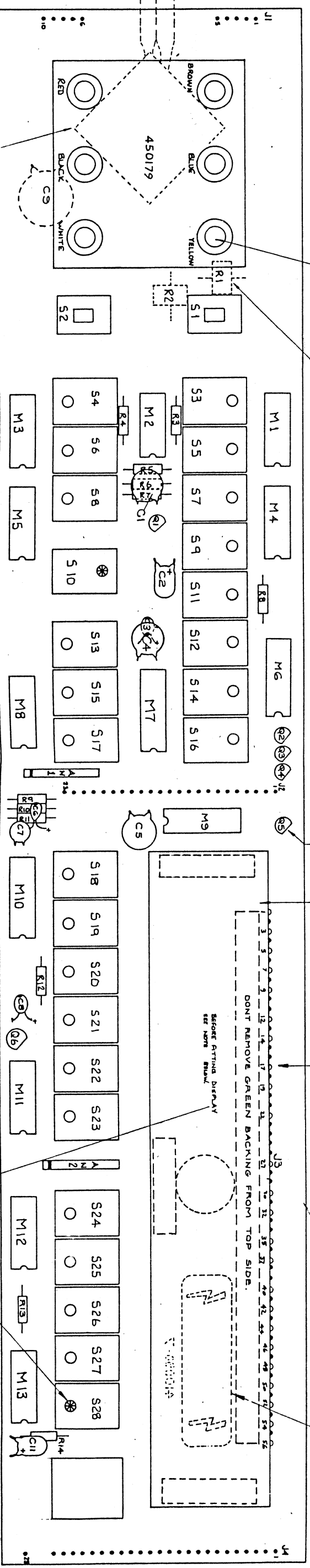
NOTE
NO COMPONENTS TO STAND HIGHER THAN 7.5 mm
(EXCEPT SWITCHES & TERMINALS)
EXCEPT DIMS WHICH MUST BE LESS THAN 6.5---

THE DISPLAY IS TO HAVE 7 PIECES OF PRESSURE SENSITIVE
TAPE (30029) PIECE (140mm) STUCK TO THE REVERSE
BELOW THE LINE OF HOLES AND 6 PIECES (25mm LONG)
STUCK TOGETHER IN PAIRS AND STUCK TO THE REVERSE OF
DISPLAY INTO POSITION AS SHOWN IN FIG 4. AND PINS OF DISPLAY
SHOWN BELOW (THERE ARE ONLY SOLDER PADS FOR THESE
PINS).

0.2 DIGIT DISPLAY
BOO017

FRONT P.C.B. 410090-7

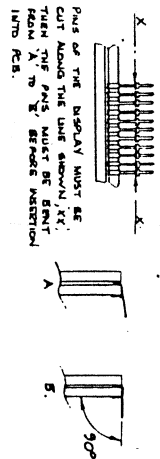
FIT WARNING LABEL 40000-1
M APPROX POSITION SHOWN
ON TERAAL SLIDE OF PCB. LEADS
MAKES AND DISPLAY CONNECTIONS.



SOLDER SIGNAL CABLE ASSY 400573 TO
REVERSE SIDE OF PCB WITH PTFE
INSULATOR 450451 BETWEEN PCB & CHOKO.
CONNECT WIRES TO TERMINALS THUS :-
WHITE WIRE TO WHITE TERMINAL
YELLOW " " YELLOW " "
GREEN " " BLACK " "
RED " " RED " "
VIOLET " " BLUE " "
BLUE " " BROWN " "

WHEN ASSEMBLY IS FINISHED TAPE CABLES
TO PCB USING MASKING TAPE G30025.
DO NOT STICK MASKING TAPE OVER DISPLAY!

ALL CAPACITORS TO BE LAID DOWN WHERE POSSIBLE,
AS SHOWN. LEADS TO BE BENT AT RIGHT ANGLES
THEN INSERTED INTO BOARD. THIS IS TO KEEP
CAPACITORS AS LOW AS POSSIBLE.



GREEN LED'S 2OFF
M1 OTHERWISE RED.

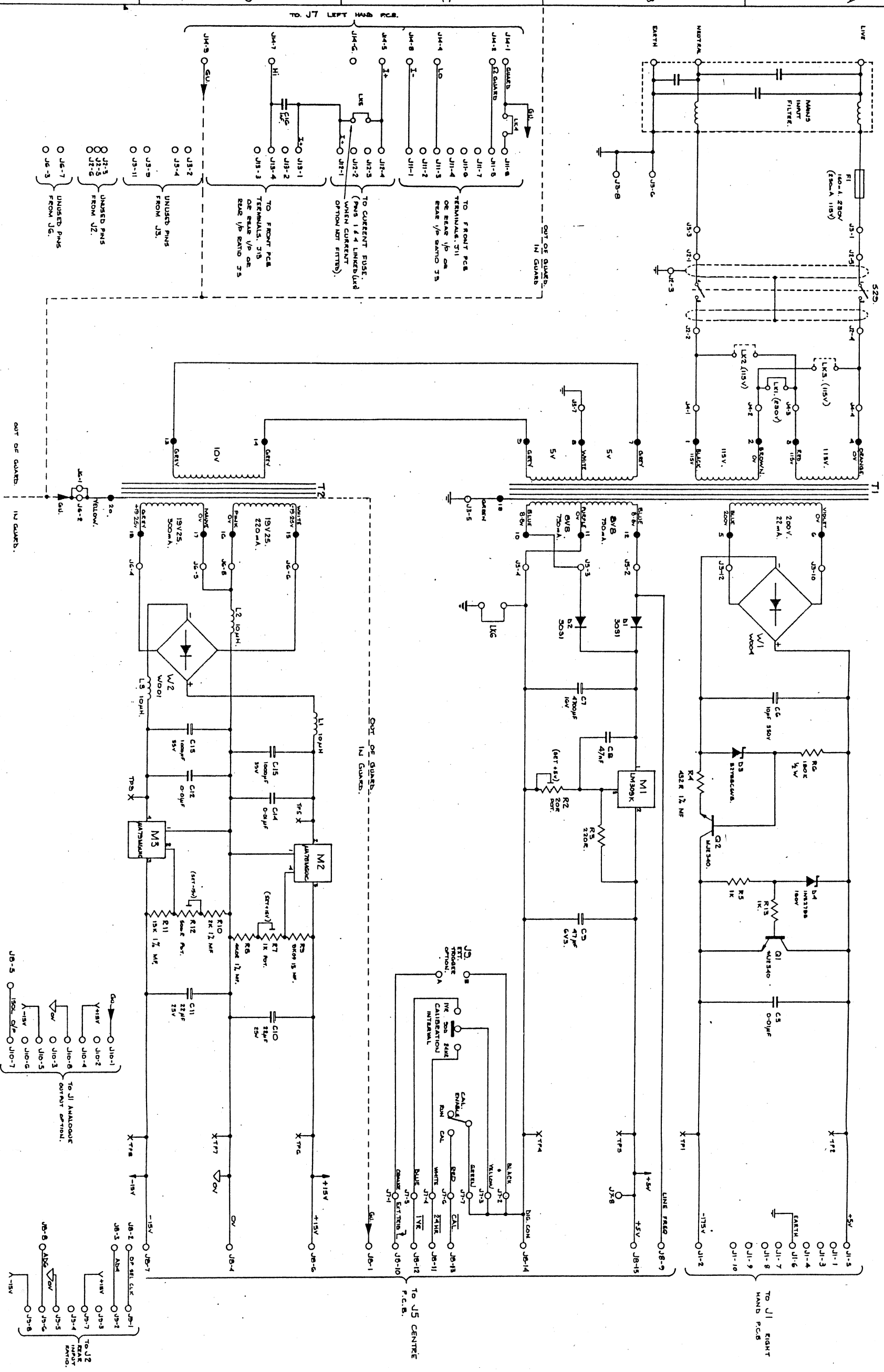
DRAWN B. J.	CHECKED [Signature]	DIMENSIONS IN MILLIMETRES		TOLERANCES UNLESS OTHERWISE STATED	ANGULAR	TITLE		DRAWING NO.	SHEET
DATE 19-4-78	APPROVED	SCALE 2:1	NOT TO BE SCALED	±0.05 ±0.10 ±0.15 ±0.20 ±0.30 ±0.40 ±0.50	±0.5° ±1.0° ±1.5° ±2.0° ±3.0° ±4.0° ±5.0°	datron ELECTRONICS LTD. NORWICH.		400294	1 OF 6
FRONT P.C.B. ASSY.		1061 / 1071 / 1081.							

FRONT PCB 1

DRAWING No. 430295
 FIRST USED ON 106/71
THIRD ANGLE PROJECTION
 DRAWN IN ACCORDANCE WITH BS 308

ALL BURS TO BE REMOVED

NOTES
 1. T1, T2 MAINS WINDY FILTER, F1, EXT TRIG. OPTION, 'RECORD SELECT' & CAL ENABLES ARE ALL FITTED ON THE REAR PANEL ASSY 430308, BUT INCLUDED ON THIS CIRCUIT DIAGRAM.



NO.	CHANGES
1	RESUBMITTED 30-3-78
2	REWORKED 30-3-78
3	REWORKED 30-3-78
4	REWORKED 30-3-78
5	REWORKED 30-3-78
6	REWORKED 30-3-78
7	REWORKED 30-3-78
8	REWORKED 30-3-78

DRAWN: B.J. CHECKED: [Signature] TRACED: [Signature] DATE: 30-3-78	DIMENSIONS IN MILLIMETRES SCALE: NOT TO BE SCALED FINISH:	TOLERANCES IN DIMENSIONS DECIMAL TO 2 PLACES ± 0.05 FRACTIONAL DIMENSIONS ± 0.10 ANGULAR ± 1mm UNLESS OTHERWISE STATED	TITLE: REAR PCB (Including rear panel) circuit diagram 106/1071/1081 DRAWING No. 430295 SHEET 1 OF 1
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REAR PCB CIRCUITS

DRAWING No. 400295
FIRST USED ON

THIRD ANGLE PROJECTION

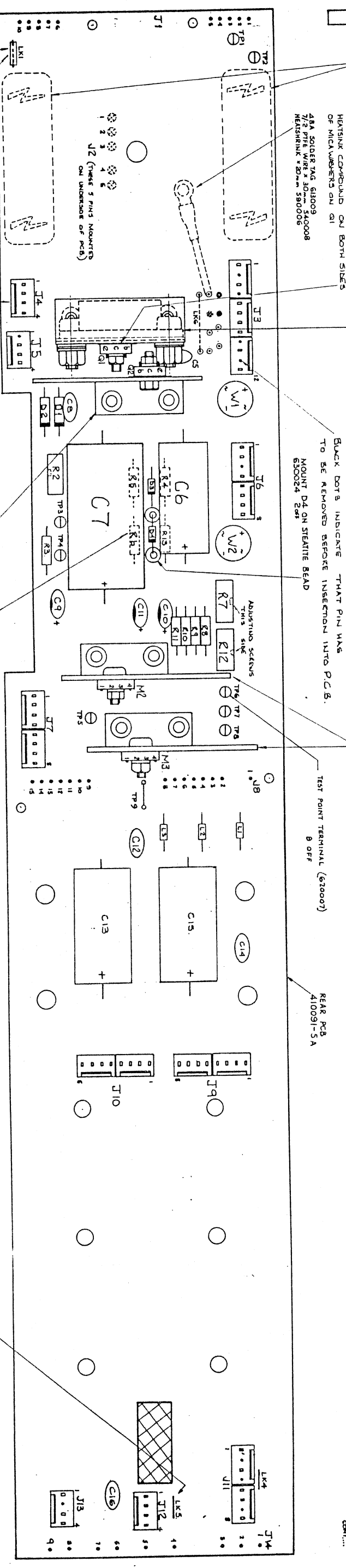
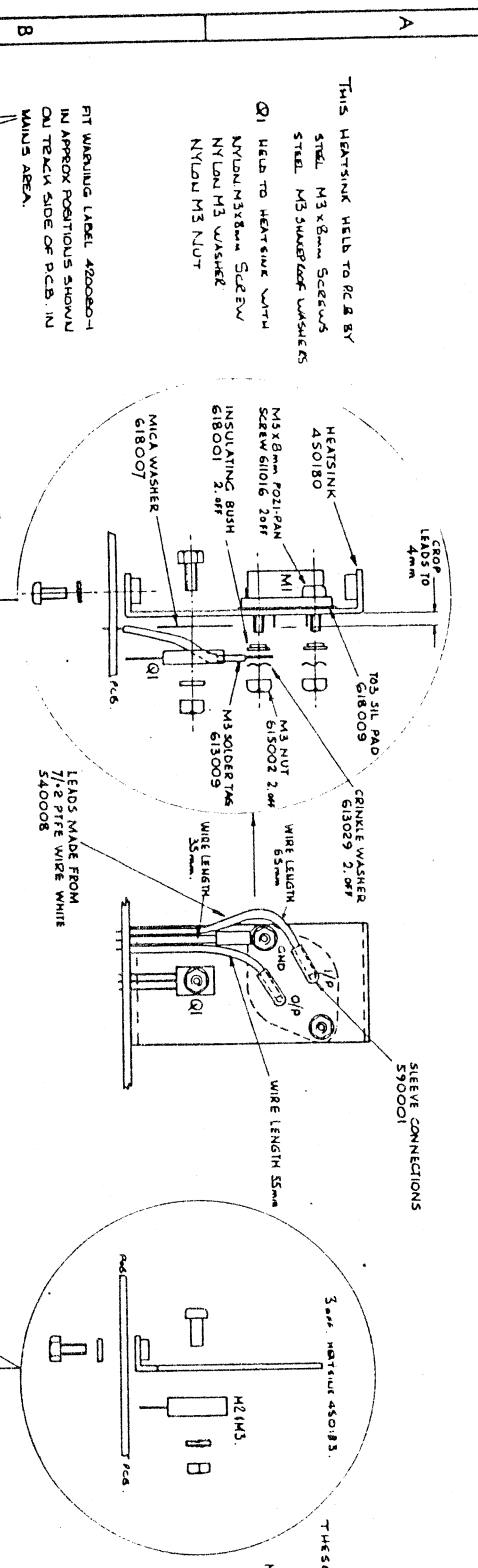
DRAWN IN ACCORDANCE WITH BS 308

- 4 off. Steel M3x8mm Secw. 6101b.
- 9 off. Nylon M3x8mm Secw. 61037.
- 4 off. Steel Shakerproof Washer. 61037.
- 9 off. Nylon M3 Washer. 61307.
- 2 off. Steel M3 Nut. 61500.
- 3 off. Nylon M3 Nut. 61505.

ALL BURRS TO BE REMOVED

NOTES

NO	CHANGES
1	Issued Per 22.5.70
2	Released to Prod 21.7.70
3	ECO 1085 1087
4	ECO 1085 1087
5	ECO 1085 1087
6	ECO 1085 1087
7	ECO 1085 1087
8	ECO 1085 1087
9	ECO 1085 1087



THIRD ANGLE PROJECTION

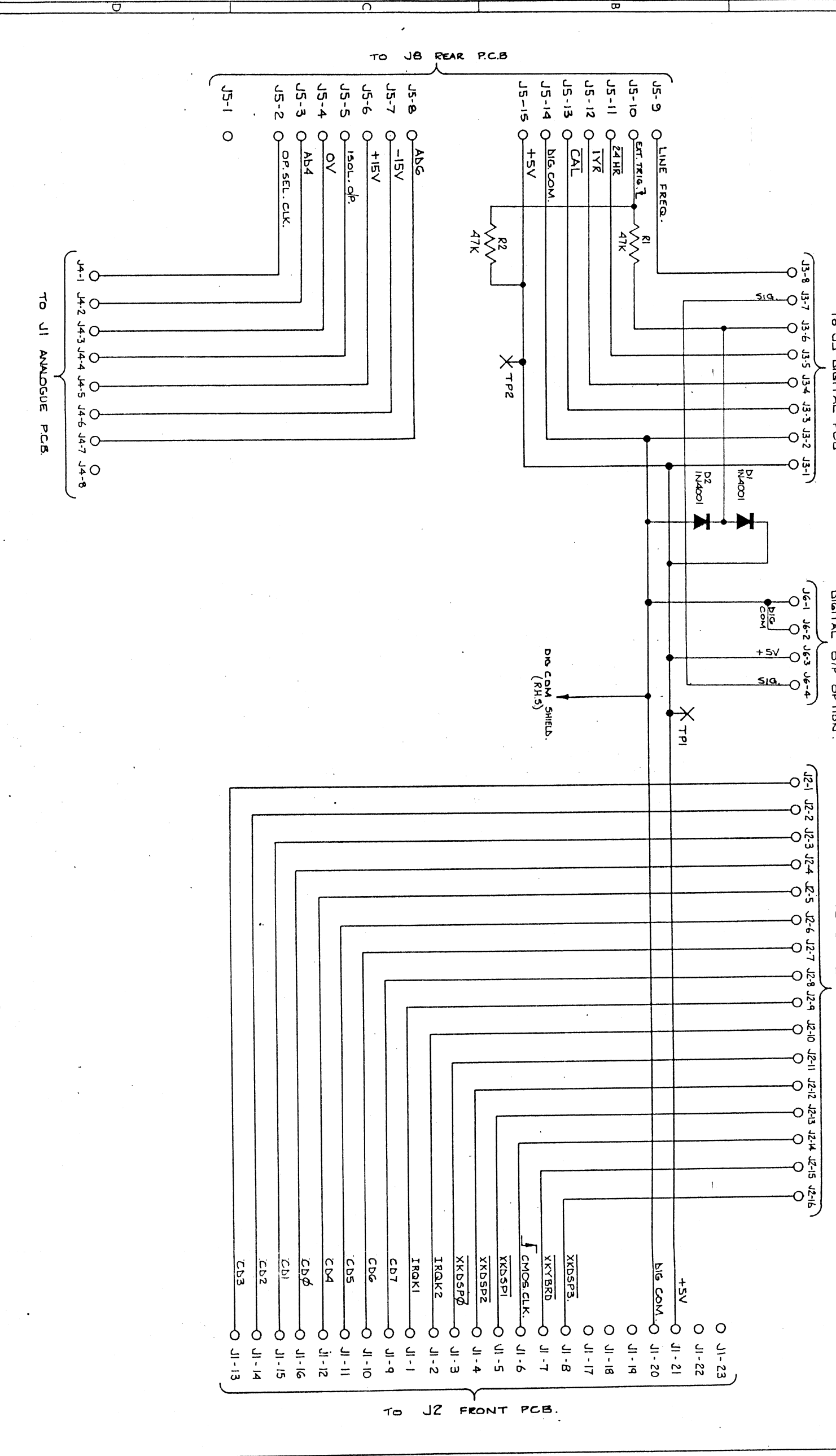
DRAWN IN ACCORDANCE WITH BS 308

DRAWING No. 430296
FIRST USED ON 1061/1071

ALL BURRS TO BE REMOVED

NOTES
1. IN GUARD TRACKS TO BE ON COT. SIDE (SHT. 2) *
2. OUT OF GUARD TRACKS TO BE ON THE COMP. SIDE (SHT. 3) OF P.C.B. WHERE POSSIBLE.

ISS.	CHANGES
1	RELEASED TO PRODUCE 29-9-78.
2	ECO B49. J6-4 sig. bonded to J5-7. B.J. 4-5-79
3	ECO 592. J5-8 moved to J5-1 GU. DIST. 29-10-79



DRAWN BY B.I.	CHECKED BY [Signature]	DIMENSIONS IN MILLIMETRES	TOLERANCES UNLESS OTHERWISE STATED
TRACED	APPROVED	SCALE NOT TO BE SCALED	ANGULAR ± 0.5°
DATE 30-5-78	DATE		DECIMAL TO 3 PLACES ± 0.05
			DECIMAL TO 2 PLACES ± 0.10
			FRACTIONAL ± 1/64
			METRIC DIMENSIONS: DECIMAL TO 2 PLACES ± 0.10mm
			WHOLE DIMENSIONS ± 2mm
			UNLESS OTHERWISE STATED

MATERIAL	FINISH

datron ELECTRONICS LTD. NORWICH.
CENTRE PCB SCHEMATIC 1061/1071/1081

DRAWING No. 430296
DRAWING SIZE A2
SHEET 1 OF 1

CENTRE PCB CRTS

DRAWING No. 400296
FIRST USED ON 10/61/1071

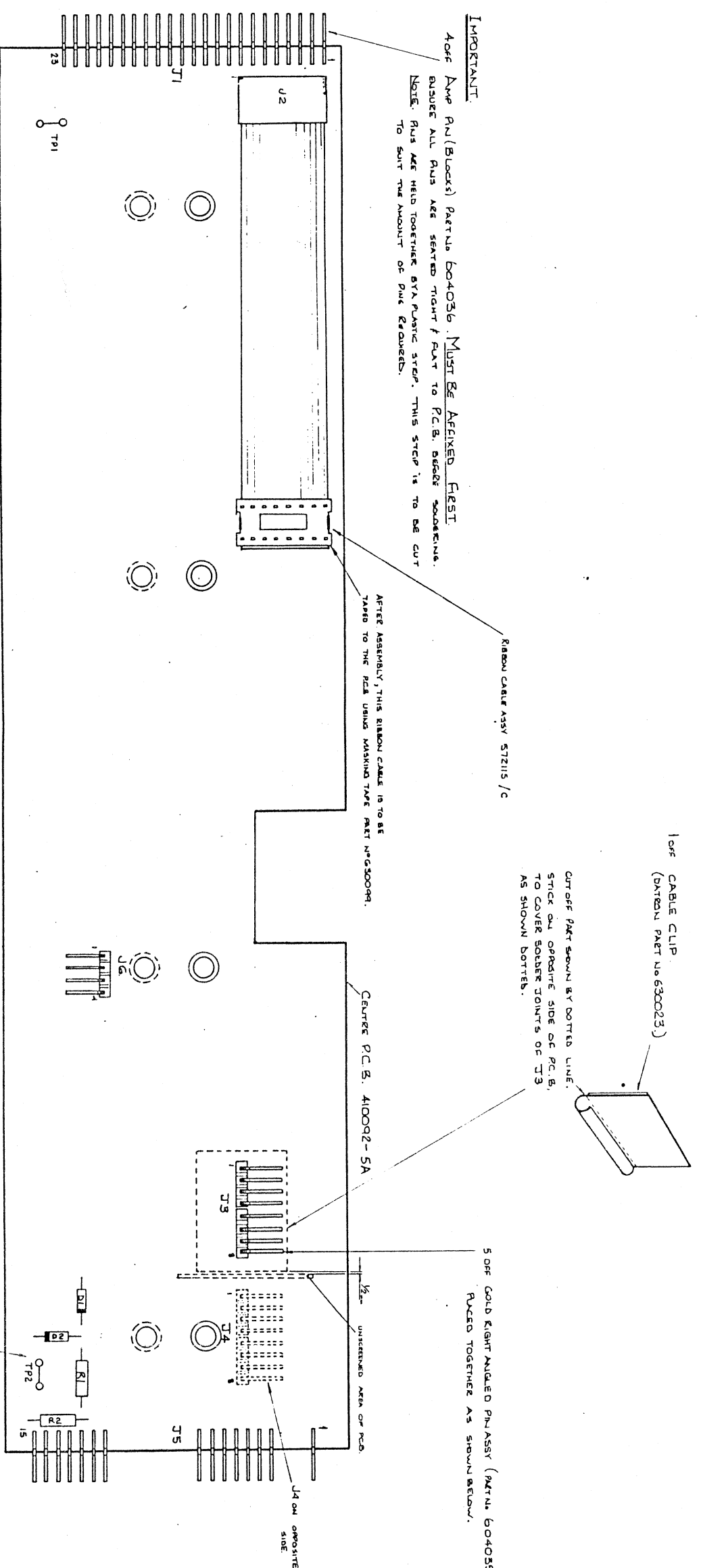
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURS TO BE REMOVED

NOTES

NO	CHANGES
C	DRAWN BY B.J.
D	APPROVED BY B.J.
1	REVISION TO DRAWING
2	REVISION TO DRAWING
3	REVISION TO DRAWING
4	REVISION TO DRAWING
5	REVISION TO DRAWING
6	REVISION TO DRAWING
7	REVISION TO DRAWING
8	REVISION TO DRAWING



DRAWN	CHECKED	DIMENSIONS IN	TOLERANCES	ANGULAR	PATTERN	TITLE	DRAWING No.	SHEET
B.J.	[Signature]	MILLIMETRES	NON-DECIMAL TO 1 PLACE DECIMAL TO 2 PLACES HEMIC DIMENSIONS DECIMAL TO 1 PLACE WHOLE DIMENSIONS UNLESS OTHERWISE STATED	90° 10° 45° 30° 15° 6°	[Crossed out]	datron ELECTRONICS LTD. NORWICH. CENTRE PCB ASSEMBLY. 10/61/1071/1081	400296	1 of 2
TRACED	APPROVED	SCALE			FINISH			
DATE 25-4-78	DATE	2:1 NOT TO BE SCALED						

CENTER PCB

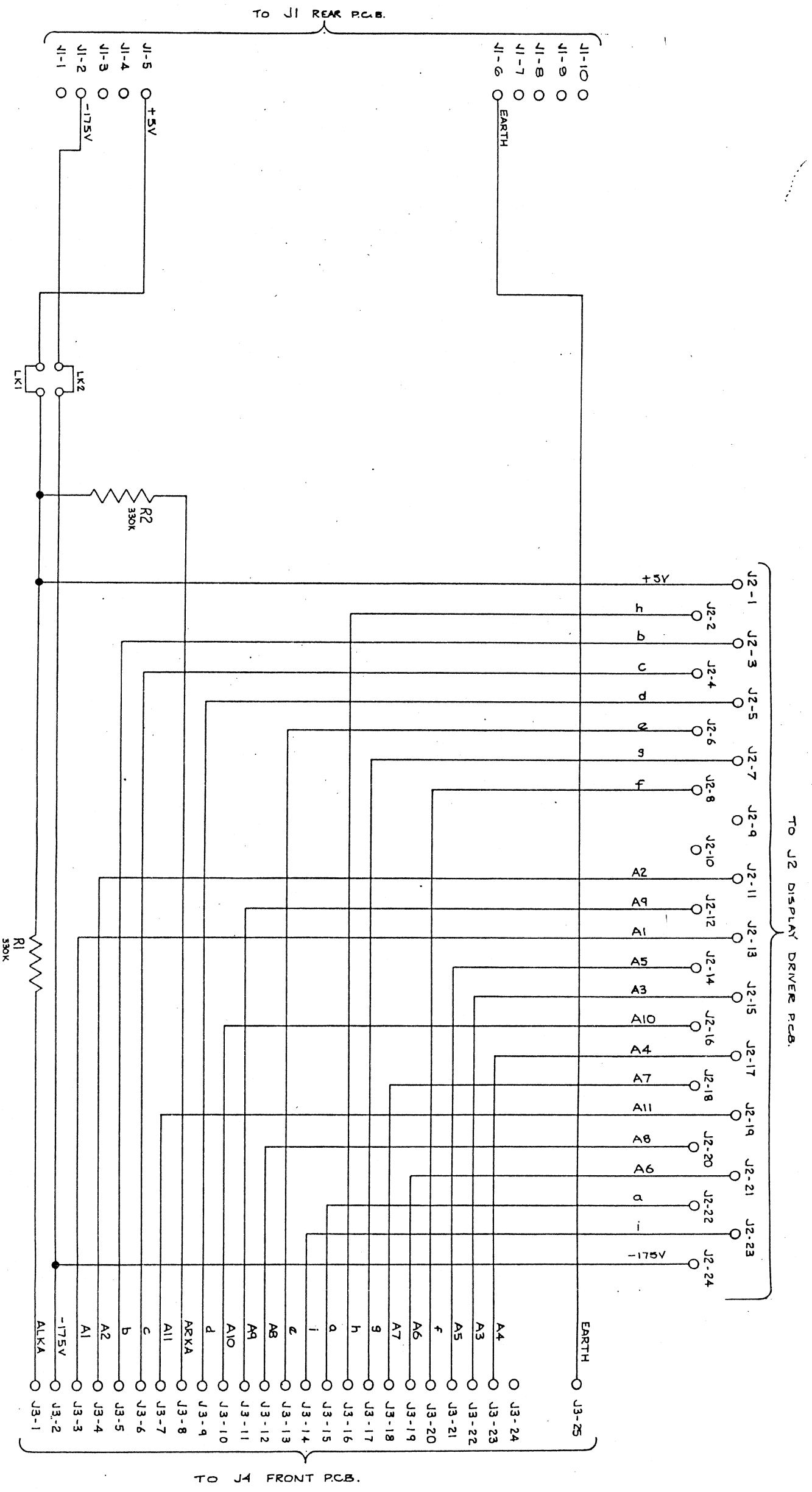
DRAWING No.
430298
FIRST USED ON
1061/1071

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

ISS.	CHANGES
1	RELEASED TO PROD 20-9-78
2	DIG CON SCREEN REMOVED. B.J. 20-9-78



DRAWN B.J.	CHECKED <i>[Signature]</i>	DIMENSIONS IN MILLIMETRES	TOLERANCES: INCH DIMENSIONS DECIMAL TO 3 PLACES ± 0.05 FRACTIONAL METRIC DIMENSIONS DECIMAL TO 1 PLACE ± 0.1mm WHOLE DIMENSIONS ± 0.4mm ANGULAR ± 1/2°
TRACED	APPROVED	SCALE NOT TO BE SCALED	FINISH
DATE 26-5-78	DATE		

datron ELECTRONICS LTD. NORWICH.
TITLE
RH. SIDE PCB. SCHEMATIC. 1061/1071/1081

DRAWING No. 430298	DRAWING SIZE A2
SHEET 1 OF 1	

RIGHT HAND PCB CKTS

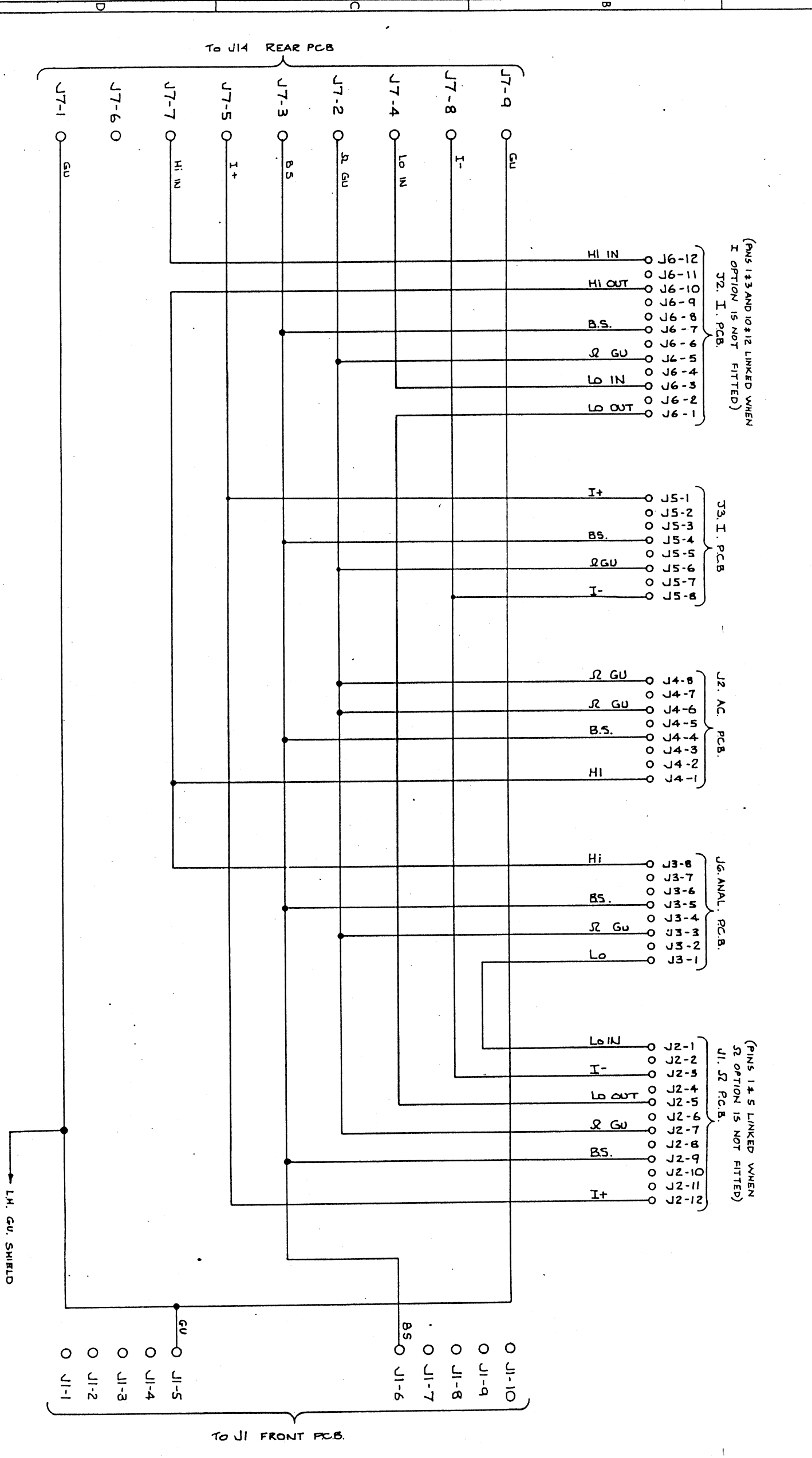
DRAWING No.
430297
FIRST USED ON
1061/1071

THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

- NOTES
- 1/ ALL CIRCUIT TO BE ON THE COMPONENT (SHEET 3) SIDE OF PCB WHERE POSSIBLE.
 - 2/ INPUT GUARD VIA JT7-1 TO PROVIDE ELECTROSTATIC SHIELD ON CIRCUIT (SHEET 2) SIDE OF PCB. WHERE POSSIBLE.
 - 3/ B.S. VIA JT3-5 TO ENCLOSE HI AND I+ CIRCUITS ON PCB WHERE POSSIBLE.
 - 4/ Ω GUARD VIA JT3-3 TO ENCLOSE LO & I- CIRCUITS ON PCB WHERE POSSIBLE.



DRAWN BT	CHECKED <i>[Signature]</i>	DIMENSIONS IN MILLIMETRES	TOLERANCES RICH DIMENSIONS DECIMAL TO 3 PLACES ± 0.05 DECIMAL TO 2 PLACES ± 0.10 FRACTIONAL METRIC DIMENSIONS DECIMAL TO 2 PLACES ± 1mm DECIMAL TO 1 PLACE ± 2mm WHOLE DIMENSIONS ± 4mm UNLESS OTHERWISE STATED
DATE 30.5.78	DATE	SCALE NOT TO BE SCALED	ANGULAR ± 0.5°

MATERIAL	FINISH
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datron ELECTRONICS LTD. NORWICH.
L.H. PCB SCHEMATIC 1061/1071/1081

DRAWING No. 430297
DRAWING SIZE **A2**
SHEET 1 OF 1

LEFT HANDS PCB CIRCS

DRAWING No.
400297
FIRST USED ON
1061/71

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

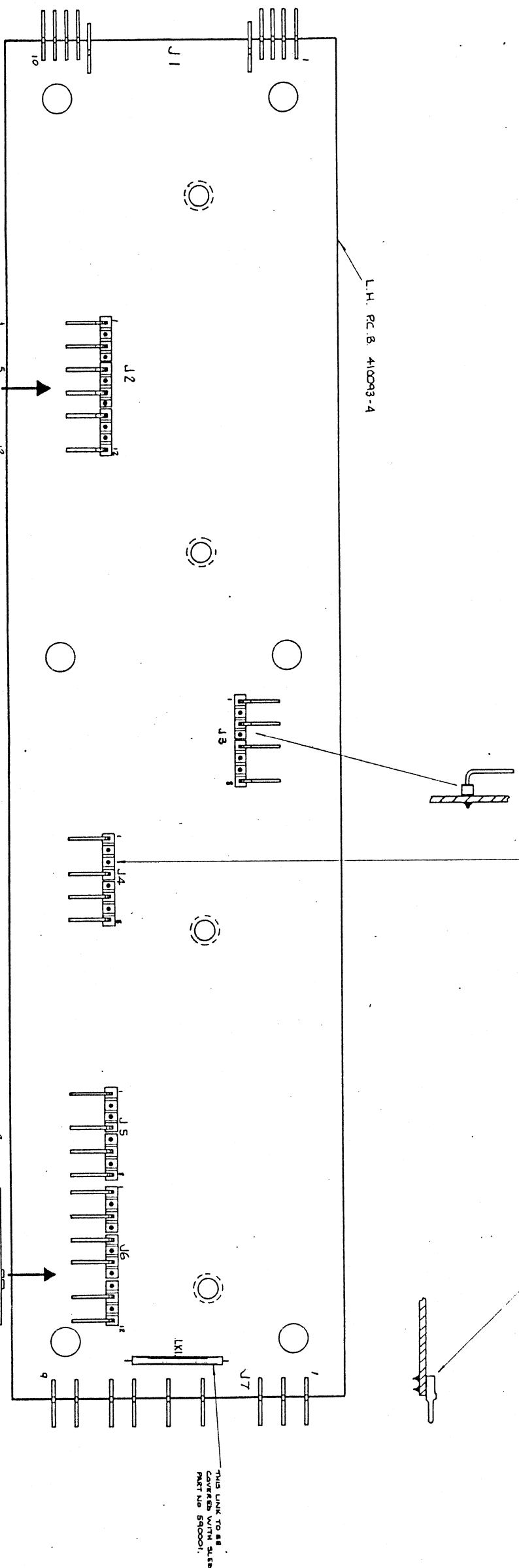
ALL BURRS TO BE REMOVED

NOTES

REV	DESCRIPTION	DATE
0	ISSUED FOR PRODUCTION	21.4.78
1	REWORKED TO PRODUCE 200007 PCB UPON	01.11.78

USE THE GOLD 4 RIGHT ANGLE PLUGS (PART NO 604035), 12 OFF.
PLACED TOGETHER TO MAKE UP THE REQUIRED AMOUNT OF CONTACTS (SHOW BELOW).
REMOVE PINS IN PLACES SHOWN BY BLACK DOTS.

IMPORTANT
2 OFF AMP PINS (PART NO 604036)
MUST BE AFFIXED FIRST.
ENSURE ALL PINS ARE SEATED TIGHT & FLAT TO P.C.B. BEFORE SOLDERING.
NOTE: PINS ARE HELD TOGETHER BY A PLASTIC STRIP. THIS STRIP IS TO BE CUT TO SUIT THE AMOUNT OF PINS REQUIRED.



BEND WIRE AND INSERT IT INTO 12 WAY SOCKET. ONE END IN HOLE 1 THE OPPOSITE END INTO HOLE 5.

RUSH SOCKET ONTO SET OF PINS AS SHOWN BY ARROW.
INSERT 1 GOLD CLAMP PIN IN POSITION 12 AS SHOWN BY SHADDED AREA.

2 OFF 12 WAY SOCKET. (PART NO 605055).

4 OFF PLASTIC PEGS (PART NO 606004) INSERTED INTO HOLES.

PLASTIC PEGS IN HOLES 10/12 OF SOCKET. AND 1/3 AS SHOWN ABOVE.

AFFIX 7 OFF GOLD CLAMP PINS (PART NO 606057) ONE ON EACH END OF WIRES. THE 7th INTO PIN 12 OF SOCKET.

3 OFF 40mm OF BROWN WIRE, (PART NO 51011) AND STRIP 3mm FROM EACH END (AS SHOWN).

DRAWN	CHECKED	DIMENSIONS IN	TOLERANCES	ANGULAR
B. T.	A.P.	MILLIMETRES	NO DIMENSIONS DECIMAL TO 1 PLACE UNLESS OTHERWISE STATED	± 0.05
TRACED	APPROVED	SCALE	HEMIC DIMENSIONS DECIMAL TO 1 PLACE UNLESS OTHERWISE STATED	± 0.05
DATE 21.4.78	DATE	2:1	WHOLE DIMENSIONS UNLESS OTHERWISE STATED	± 0.05
		NOT TO BE SCALED		

datron ELECTRONICS LTD. NORWICH.
TITLE 1061/71/81 L.H. P.C.B. ASSEMBLY

DRAWING No. 400297
DRAWING SIZE A1
SHEET 1 OF 1

LEFT HAND PCB

DRAWING No.
400298
FIRST USED ON
1061/71

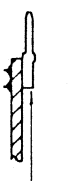
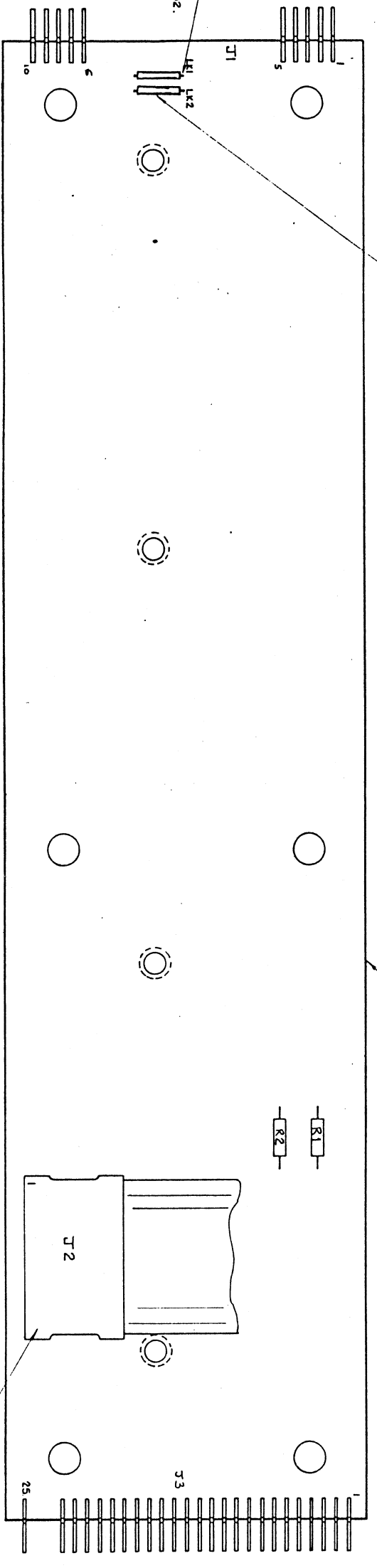
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

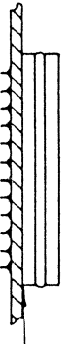
NOTES

NO.	CHANGES
1	NEW ISSUE PCB B. J.T. 24.8.78
2	REPLACED TO PCB N. 25.2.78.
3	ECO 050. 4.5.78. UPON PCB. B.J. J.I.C. WAS STUDIED.
4	ECO 067. 4.5.78. UPON PCB. B.J. J.I.C. WAS STUDIED.
5	ECO 943. 10.9.78. RIBBON CABLE/PCB. B.J. J.I.C. WAS STUDIED.
6	ECO 1474. 1.8.81. PCB ISSUE N° WAS 4. I.L. 3.6.81



IMPORTANT
AMP PINS (DATRON PART NO. 604036) 40PP MUST BE AFFIXED TO PCB FIRST. ENSURE ALL PINS ARE SEATING TIGHTLY AND FLAT TO PCB BEFORE SOLDERING.

NOTE: PINS ARE HELD TOGETHER BY PLASTIC STRIP. THIS STRIP IS TO BE CUT TO SUIT THE AMOUNT OF PINS REQUIRED. FOR EXAMPLE ABOVE 2 BLOCKS OF 5 PINS ARE REQUIRED, THEREFORE STRIP OF 10 PINS TO BE CUT IN HALF.



NOTE: RIBBON CABLE ASSY Part No. 574270/c
WHEN SOLDERING CABLE PLUG INTO BOARD ENSURE THAT THE PLUG BODY SITS FLAT AGAINST PCB.
AFTER ASSEMBLING PCB WRAP THE RIBBON CABLE AROUND THE PCB AND TAPE DOWN USING MASKING TAPE PART NO. 530094.

DRAWN B.J.	CHECKED <i>[Signature]</i>	DIMENSIONS IN MILLIMETRES	TOLERANCES UNLESS OTHERWISE STATED	FINISH	TITLE	DRAWING No.	DRAWING SIZE
20.4.78	DATE	2:1 NOT TO BE SCALED	ANGULAR 1°		datron ELECTRONICS LTD. NORWICH.	400298	A1
					1061/71/81 R.H. PCB ASSEMBLY		1 of 2

RIGHT HAND PCB

DRAWING No.
430308
FIRST USED ON
1061-1071

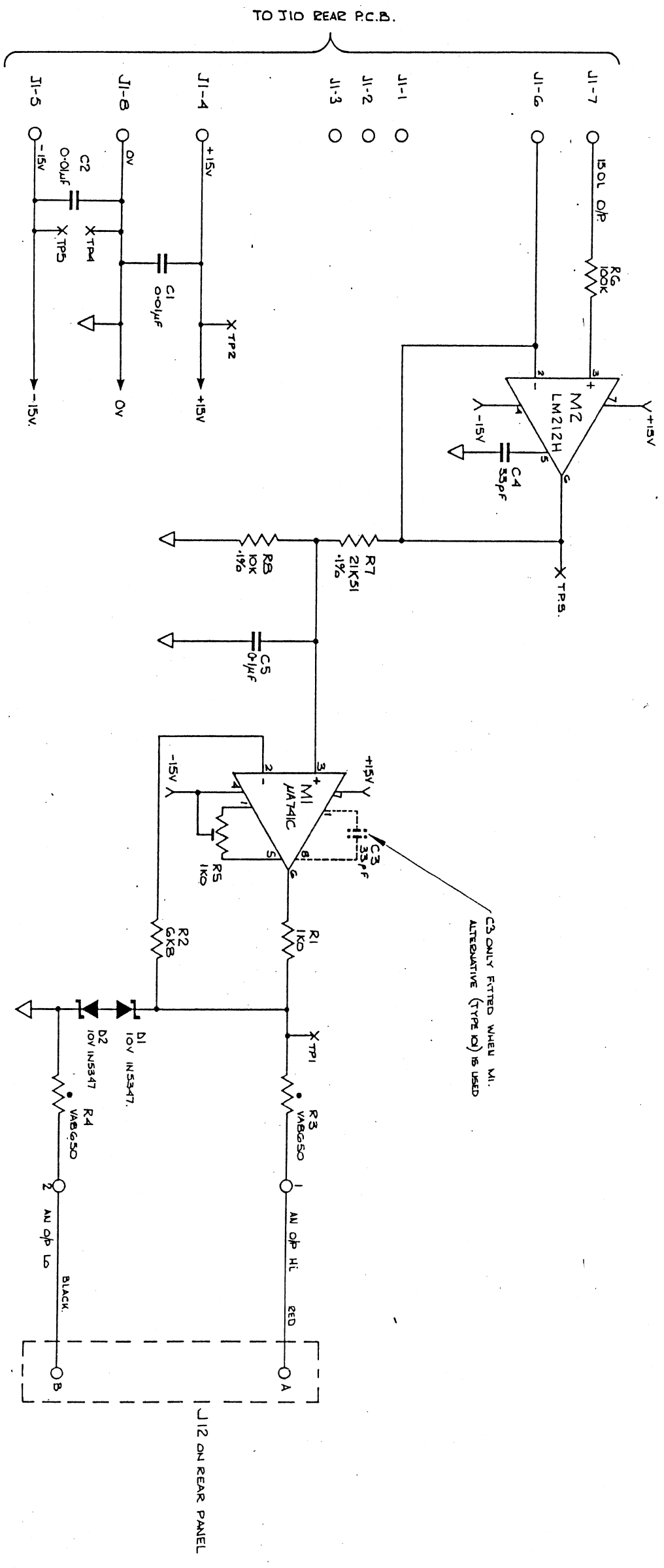
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

ISS.	CHANGES
1	RELEASED. 27 DEC 78. W.G.S.
2	R7 WAS 21K73 ECO. 945 1L 10979 1L



DRAWN B.J.	CHECKED M.S.	DIMENSIONS IN MILLIMETRES	TOLERANCES INCH DIMENSIONS DECIMAL TO 3 PLACES ± 0.05 FRACTIONAL DECIMAL TO 2 PLACES ± 1/16 FRACTIONAL ANGULAR ± 1/2°
TRACED	APPROVED	SCALE	PERIODIC DIMENSIONS DECIMAL TO 1 PLACE ± 1mm WHOLE DIMENSIONS ± 1mm UNLESS OTHERWISE STATED
DATE 23-11-78	DATE	NOT TO BE SCALED	

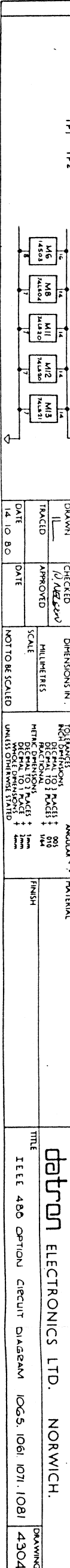
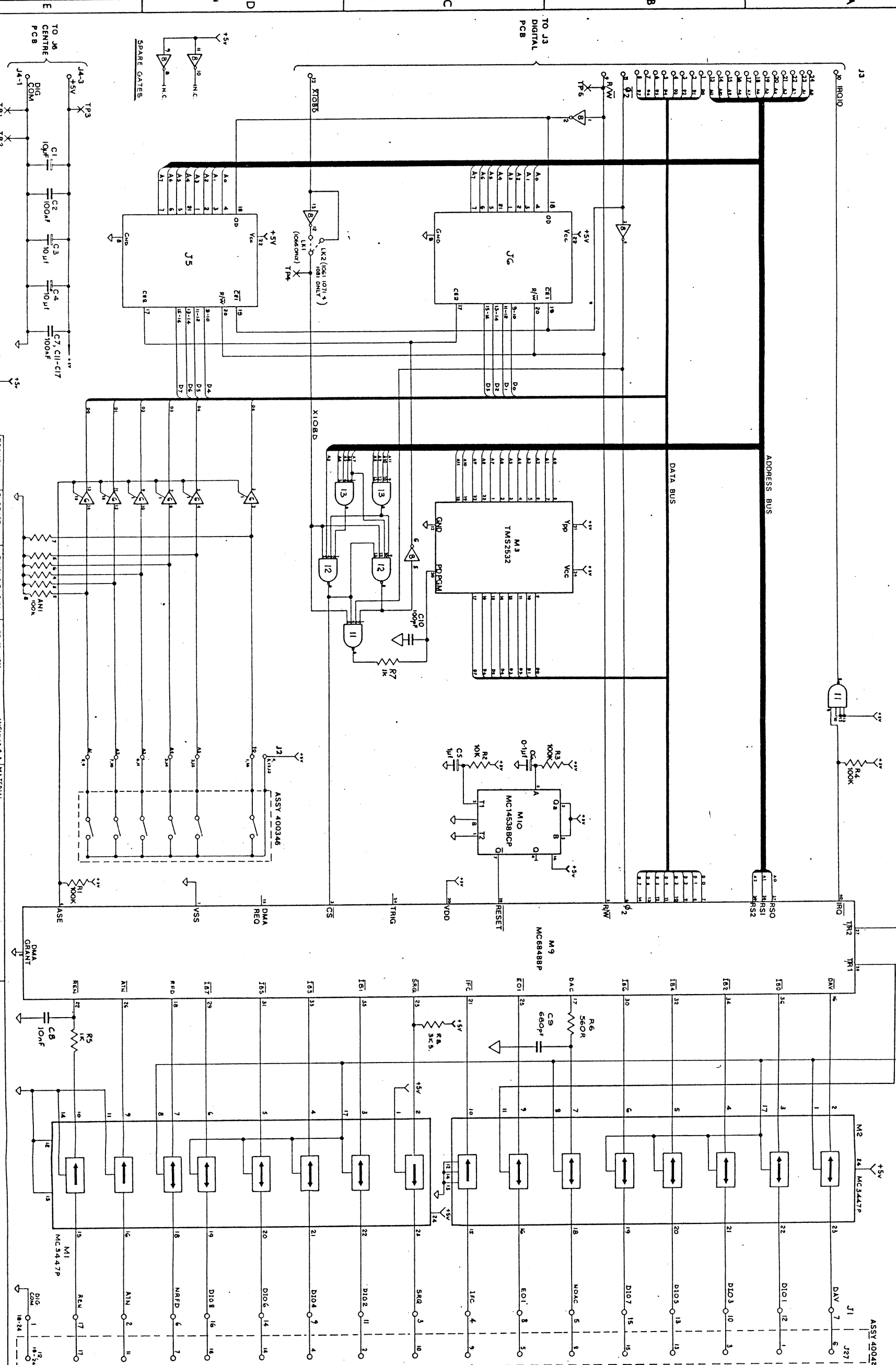
MATERIAL	FINISH

datron ELECTRONICS LTD. NORWICH.

TITLE
ANALOGUE OUTPUT CIRCUIT. 1061/1071/1081

DRAWING No. 430308	DRAWING SIZE A2
SHEET 1 OF 1	

ANALOGUE OUT



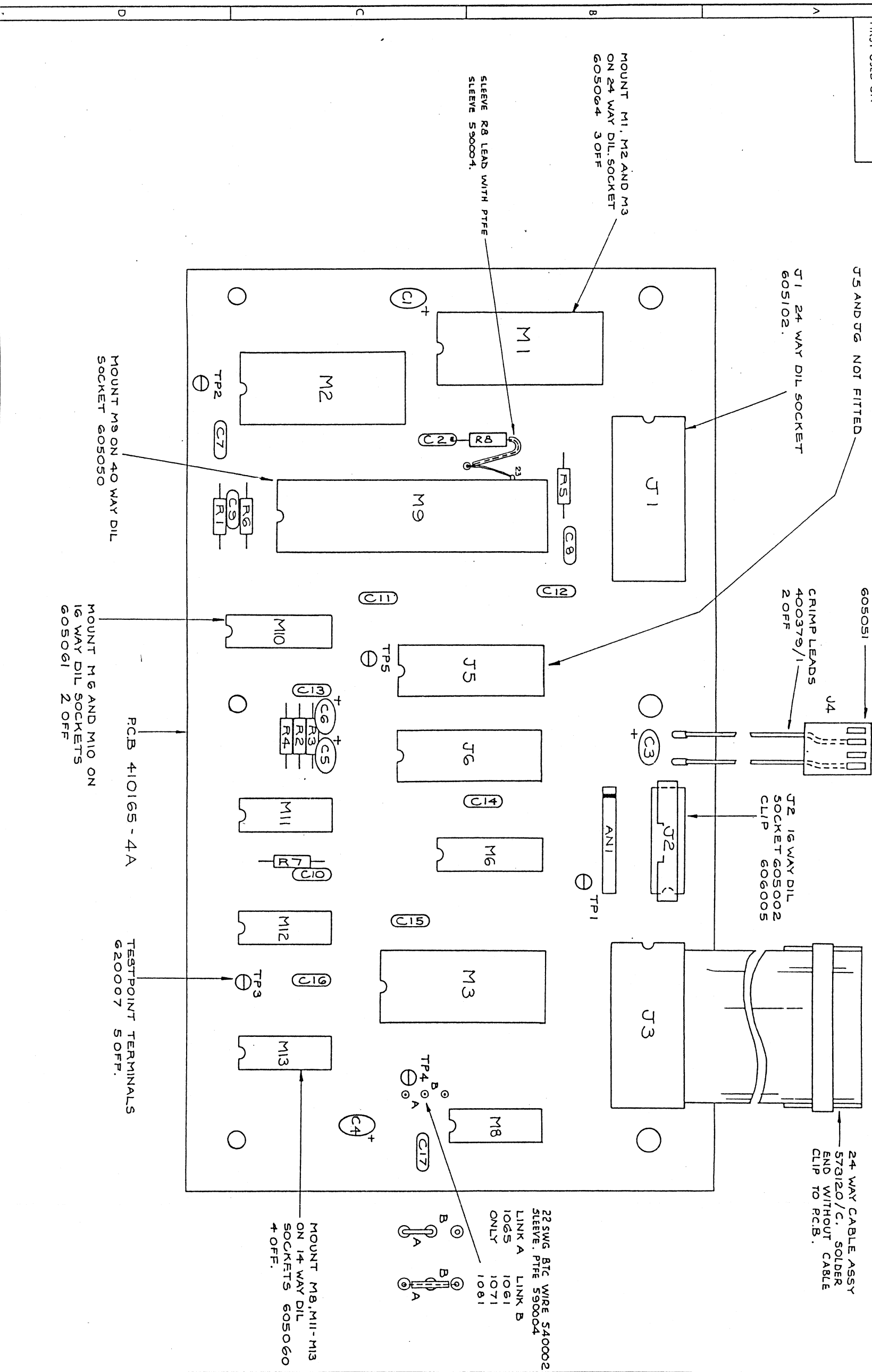
NO.	DESCRIPTION	DATE	BY	CHECKED	SCALE	APPROVED	DATE	DATE	SCALE	APPROVED	DATE
1	INITIALS DELETED										
2	RELEASED										
3	ECO1/29										
4	ECO1/29 ADDED										
5	ECO1/29 ADDED										
6	ECO1/29 ADDED										
7	ECO1/29 ADDED										

datron ELECTRONICS LTD. NORWICH.
 TITLE: IEEE 480 OPTION CIRCUIT DIAGRAM 1065, 1061, 1071, 1081
 DRAWING No. 430427
 SHEET 1 OF 1

1577 488 / 6P13

DRAWING NO.
400427
FIRST USED ON

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308



ALL BURRS TO BE REMOVED
FIT CRIMP TERMINALS
TO J4-2 & J4-4
605056

NOTES

ISS	CHANGES
9	ECO 1538/1588 3 ANTLATCHES REMOVED. P.C.B. WAS 1552 C2 WAS IOUF TANT C11-C17 ADDED. 28.2.84
10	ECO 1601 R8 ABDED. 85.26.7.84

DRAWN
CHKD.
APPD.

DATE
5.10.83

DIMENSIONS IN
MILLIMETRES
SCALE
2:1
NOT TO BE SCALED

MATERIAL
FINISH

TITLE
datron ELECTRONICS LTD. NORWICH.
IEEE PCB ASSY 1065 1061 1071 1081

DRAWING No.
400427
SHEET
1 OF 5

IEEE 488 / GPIB PCB

DRAWING No.
430503
PART USED ON

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

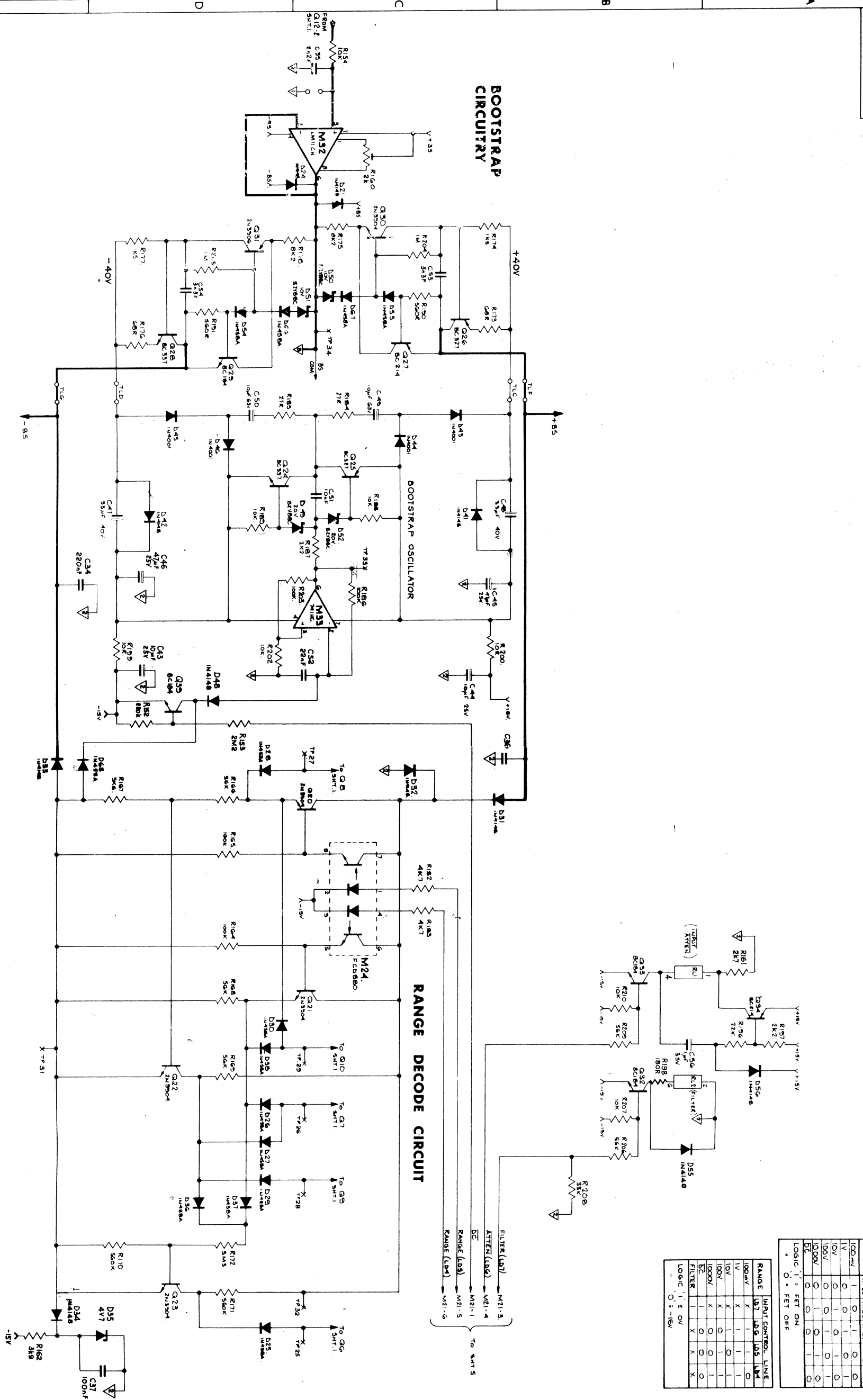
NOTES

RANGE	FET CONTROL LINE	LINE
100mV	1	0
1V	0	1
10V	0	1
100V	0	1
DC	0	1

LOGIC '1' = FET ON
LOGIC '0' = FET OFF

RANGE	INPUT CONTROL LINE	LINE
100mV	X	1
1V	X	1
10V	X	1
100V	X	1
DC	X	1

FILTER 1 = 50V
LOGIC '1' = 50V
LOGIC '0' = 15V



DRAWN	CHECKED	DIMENSIONS IN	TOLERANCES	ANGULAR	PARTIAL
TRACED	LOG	MILLIMETRES	DECIMAL TO 1 PLACE	0°	
	APPROVED	SCALE	FRACTIONAL	1/16	
	RWF	NOT TO BE SCALED	DECIMAL TO 2 PLACES	1/32	
DATE	DATE		DECIMAL TO 3 PLACES	1/64	
25.1.83	31.3.83		DECIMAL TO 4 PLACES	1/128	

datron ELECTRONICS LTD. NORWICH.

Boot strapped supplies & range logic 1081

DRAWING No.
430503
SHEET
2 OF 5

ISS. CHANGES
1 RELEASED 31.3.83

BOOTSTRAPPED SUPPLIES & RANGE LOGIC

DRAWING No
430503
FIRST USED ON

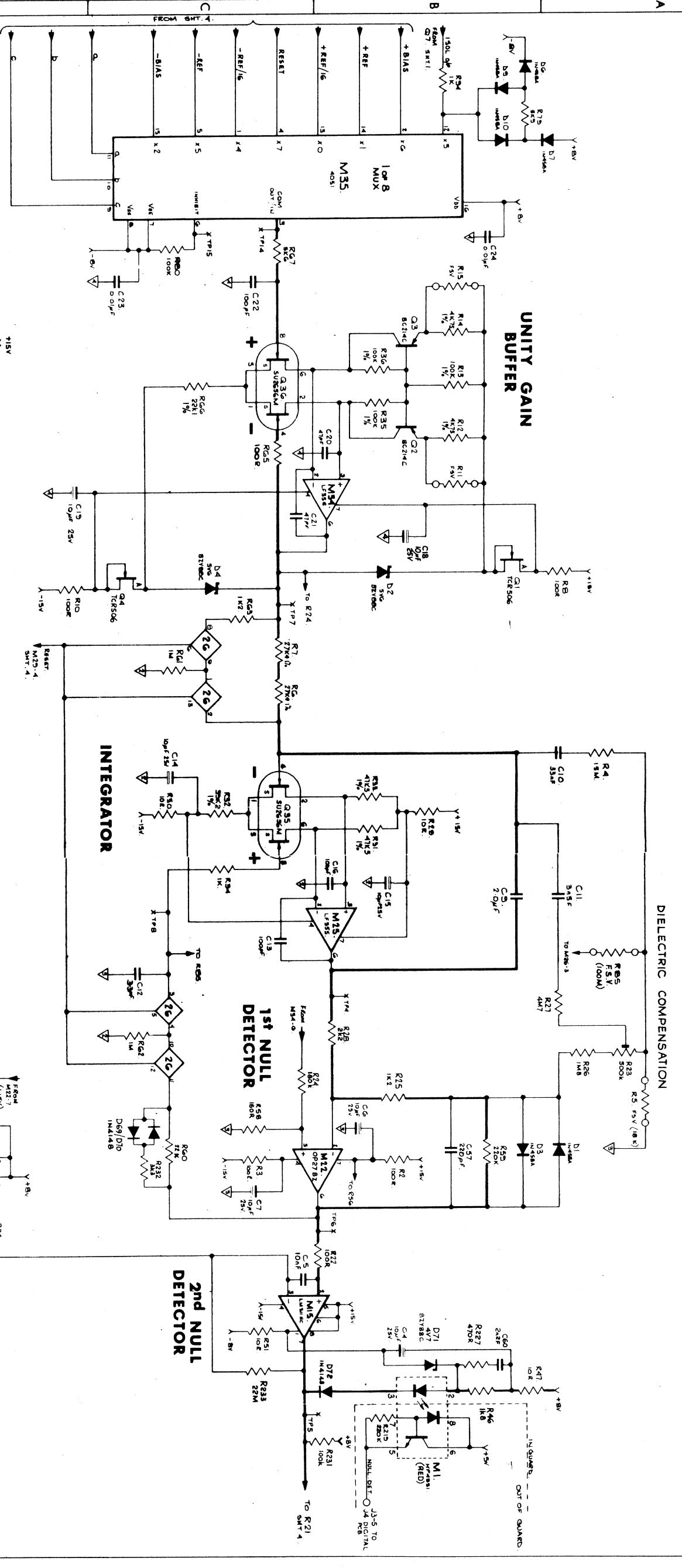
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

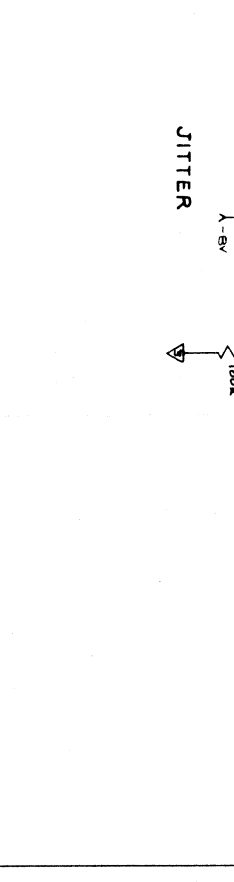
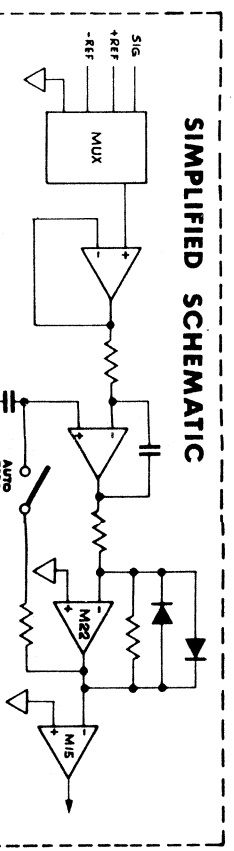
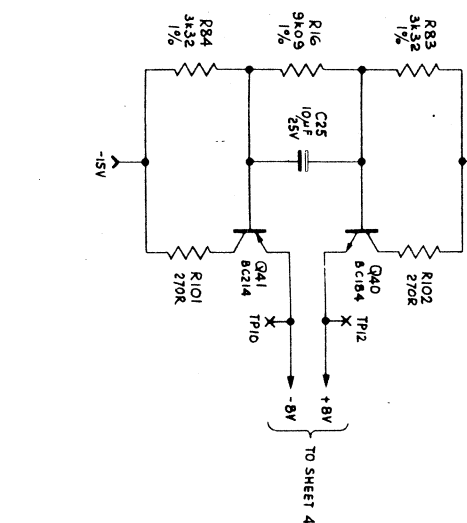
ALL BURS TO BE REMOVED

NOTES

ISS. CHANGES
1 RELEASED 31.3.83



CONDITION	MULTIPLIER	RESET
RESET	A	1
RESET	B	1
RESET	C	1
RESET	D	1
RESET	E	1
RESET	F	1
RESET	G	1
RESET	H	1
RESET	I	1
RESET	J	1
RESET	K	1
RESET	L	1
RESET	M	1
RESET	N	1
RESET	O	1
RESET	P	1
RESET	Q	1
RESET	R	1
RESET	S	1
RESET	T	1
RESET	U	1
RESET	V	1
RESET	W	1
RESET	X	1
RESET	Y	1
RESET	Z	1



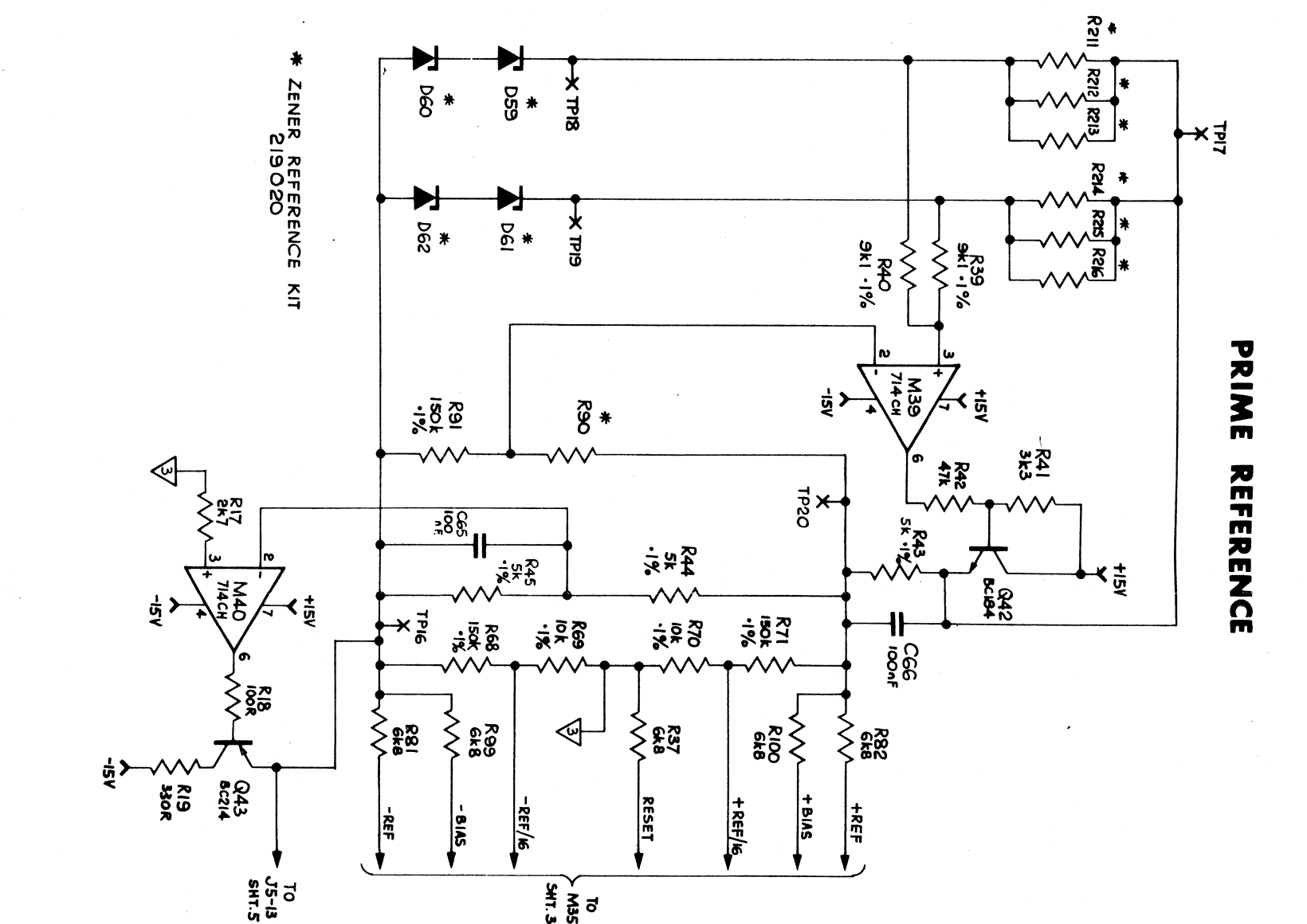
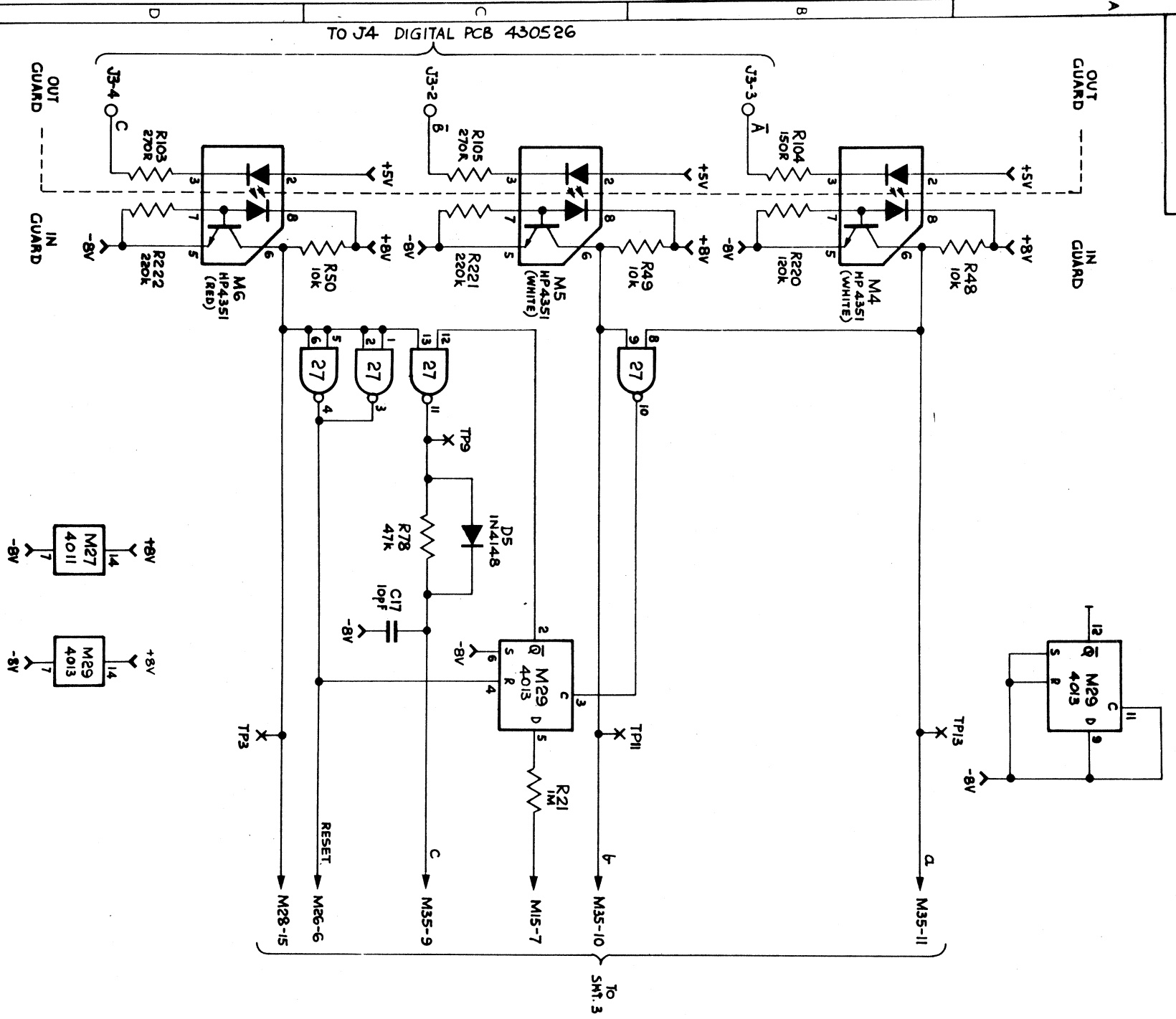
DRAWING No. 430503
SHEET 3 OF 5
DATE 25.1.83
DRAWN BY LOG
CHECKED BY K.W.P.
APPROVED BY K.W.P.
SCALE MILLIMETRES
DIMENSIONS IN MILLIMETRES
TOLERANCES: ANGULAR ± 0.1°
NON DIMENSIONS: DECIMAL TO 3 PLACES
FRACTIONAL: DECIMAL TO 1 PLACE
WHOLE DIMENSIONS: UNLESS OTHERWISE STATED
FINISH MATERIAL
TITLE A-D CONVERTOR 1081
datron ELECTRONICS LTD. NORWICH.
DRAWING SIZE A1

DRAWING No.
430503

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

ALL BURNS TO BE REMOVED

NOTES



* ZENER REFERENCE KIT
219020

DRAWN	DATE	DIMENSIONS IN	METRIC DIMENSIONS	MATERIAL
L.O.G.	26.1.83	MILLIMETRES	ANGULAR $\pm \frac{1}{2}^\circ$ DECIMAL TO 2 PLACES $\pm 1mm$ WHOLE DIMENSIONS $\pm 4mm$ UNLESS OTHERWISE STATED	
APPRO. RWE	DATE	SCALE		FINISH
	31-3-83	NOT TO BE SCALED		

datron ELECTRONICS LTD. NORWICH.
TITLE
A-D CONTROL + REFERENCES 1081

DRAWING No.
430503
DRAWING SIZE
A2
SHEET
4 OF 5

A-D CONTROL + REFERENCE SUPPLY

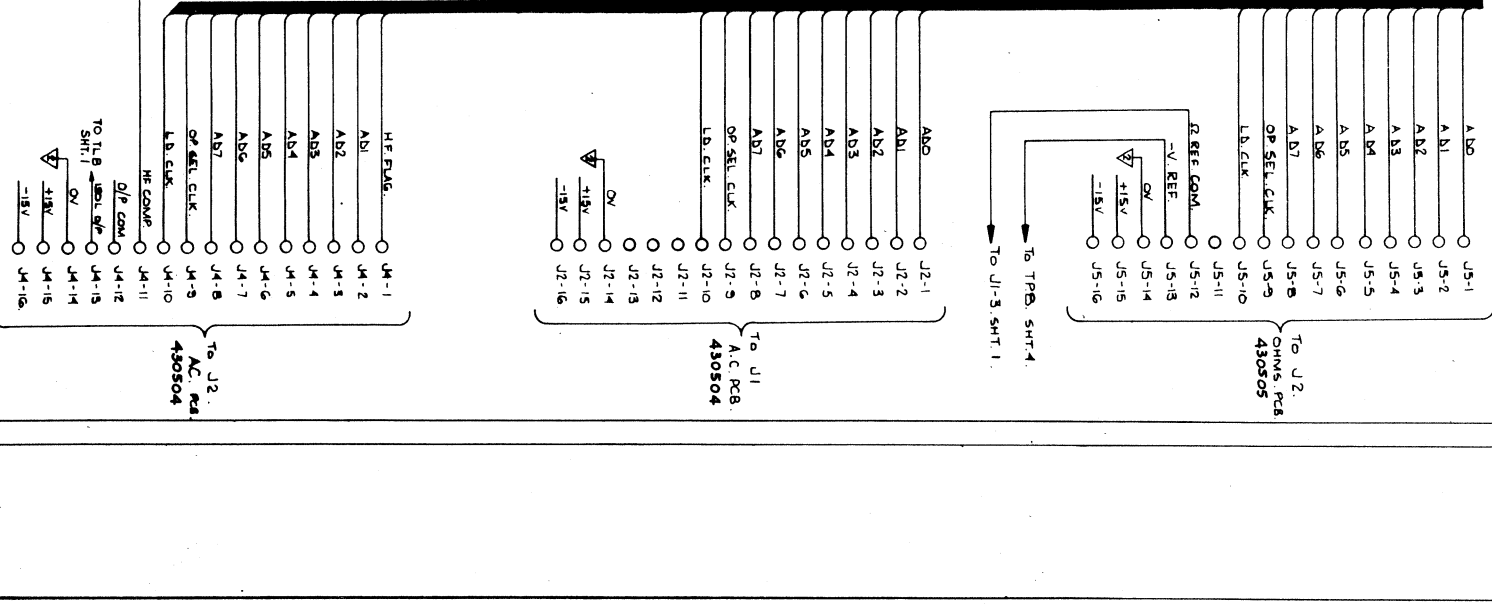
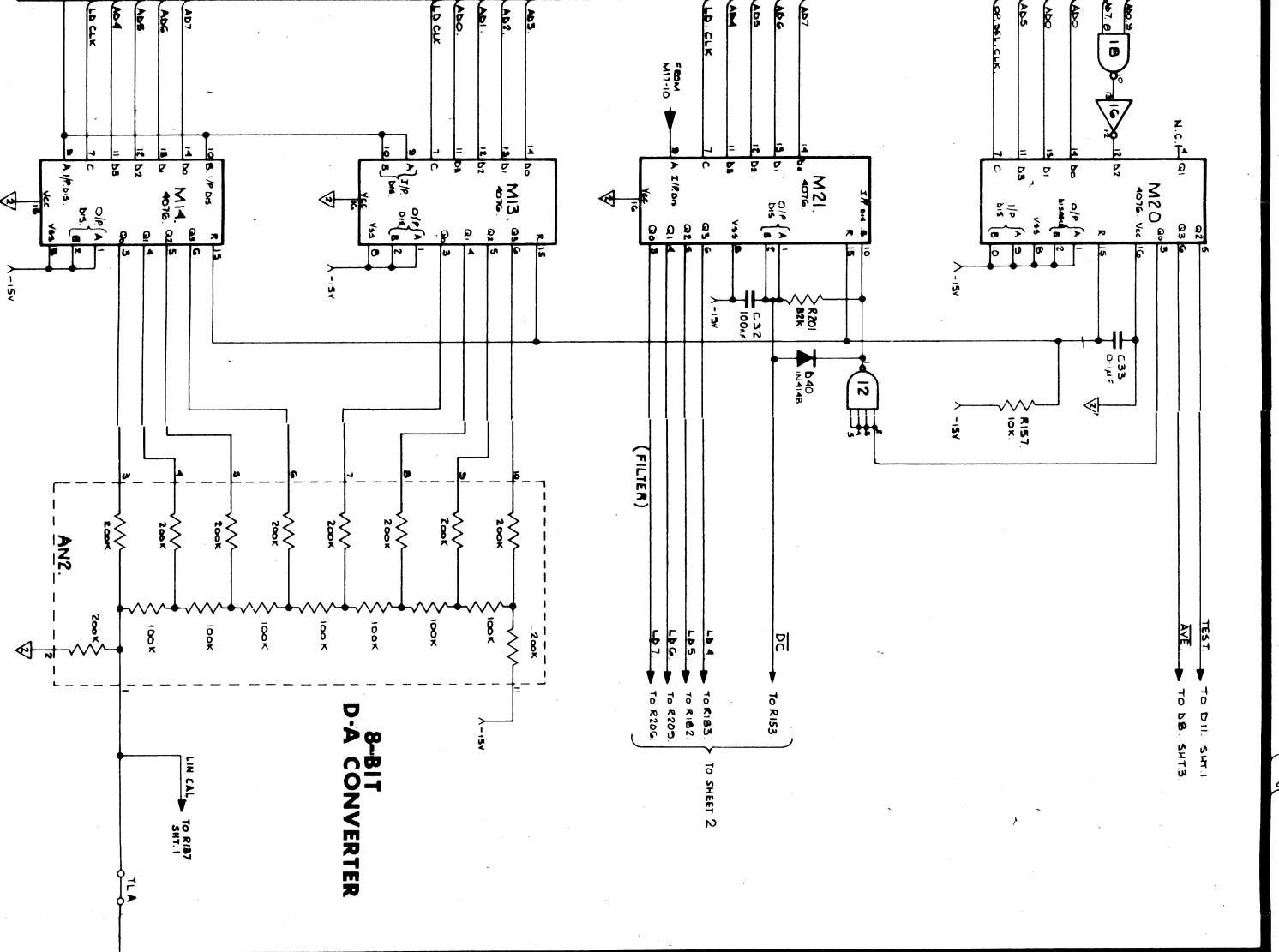
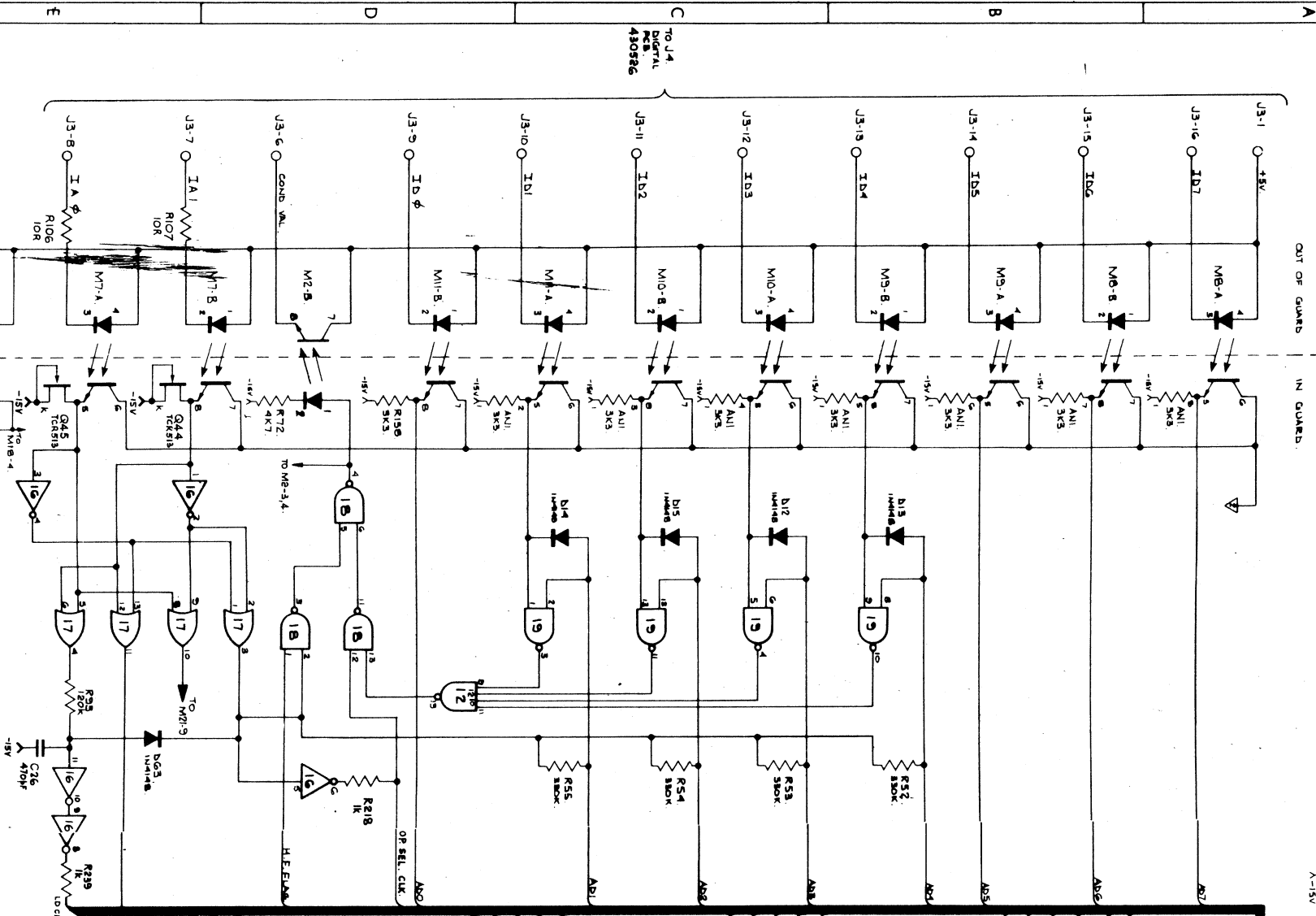
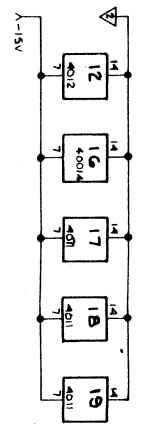
DRAWING No. 430503
FIRST USED ON

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

ALL BURS TO BE REMOVED

NOTES

1 RELEASED 31.3.83

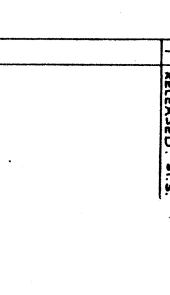
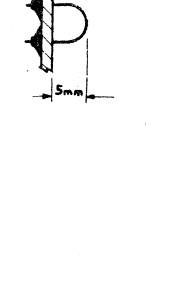
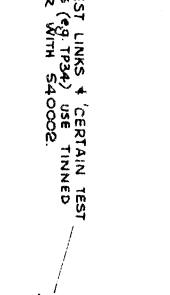
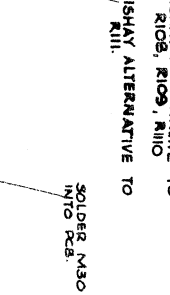
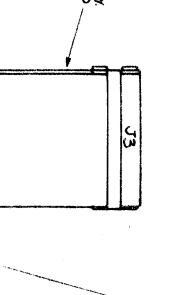
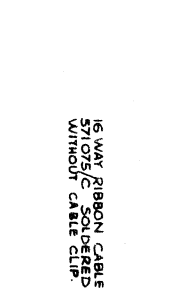
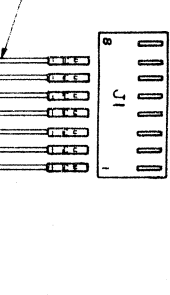


DRAWN	CHECKED	DIMENSIONS IN	NOTES	ANGULAR	MATERIAL
LOG	L.O.G.	MILLIMETRES	NOT DIMENSIONED PAGES + 005	005	
TRACED	APPROVED		DETAIL TO 3 PLACES + 010	1/44	
	RWF	SCALE	METRIC DIMENSIONS		
DATE	DATE	NOT TO BE SCALED	DETAIL TO 1 PLACE + 005	1mm	
25.1.83	31-3-83		UNLESS OTHERWISE STATED	2mm	

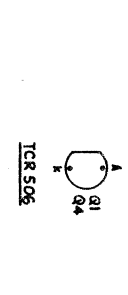
datron ELECTRONICS LTD. NORWICH.
ANALOGUE INTERFACE LOGIC 1081
DRAWING No. 430503
A1

ANALOGUE INTERFACE

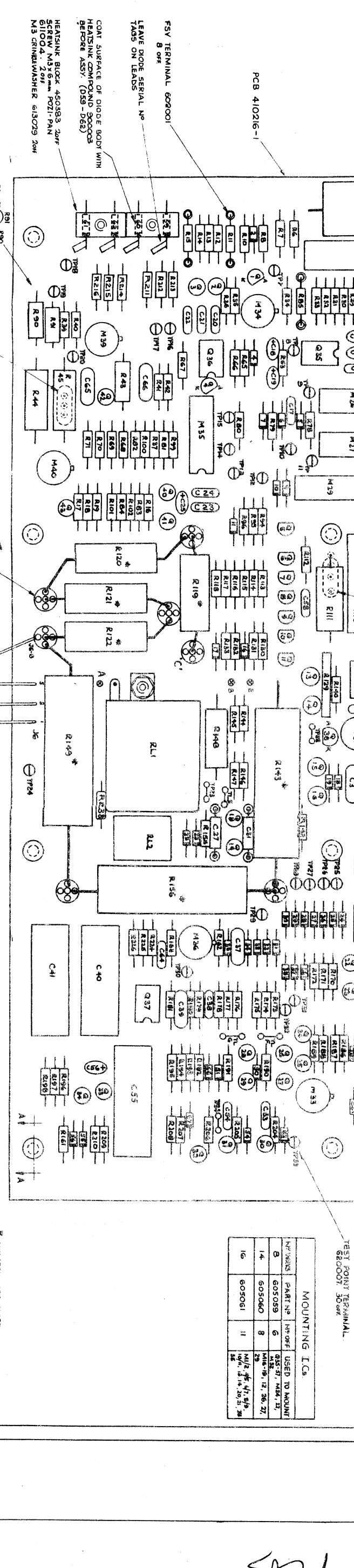
NOTE: - FIT RESG AS SHOWN ON DKS FIT RESG6 AS SHOWN WITH FLAT ON THE LEFT



NOTE: - ALL SINGLE PINS LESS IN THE ORDER SHOWN. ALL TRANSISTOR LEADS IN THE ORDER SHOWN.



PCB 410216-1

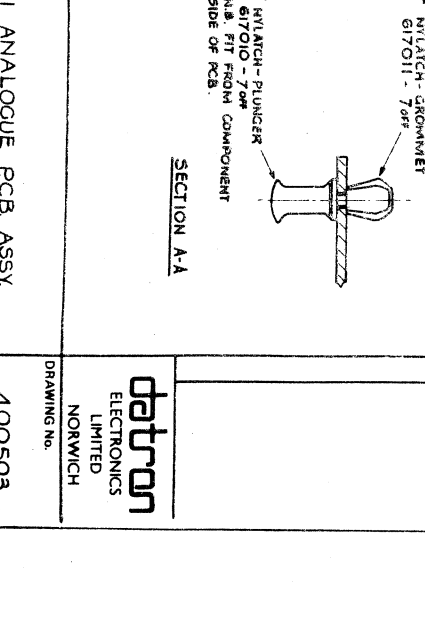
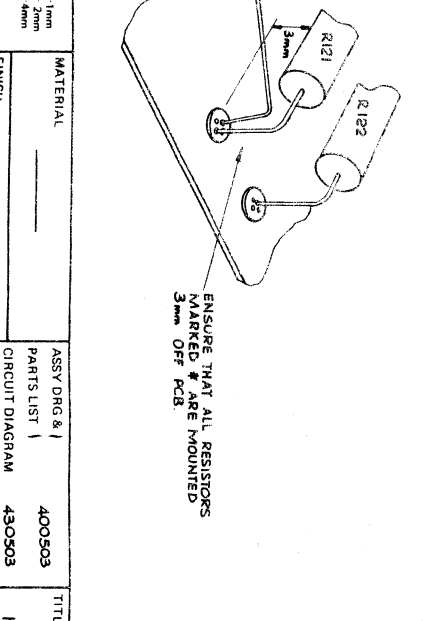
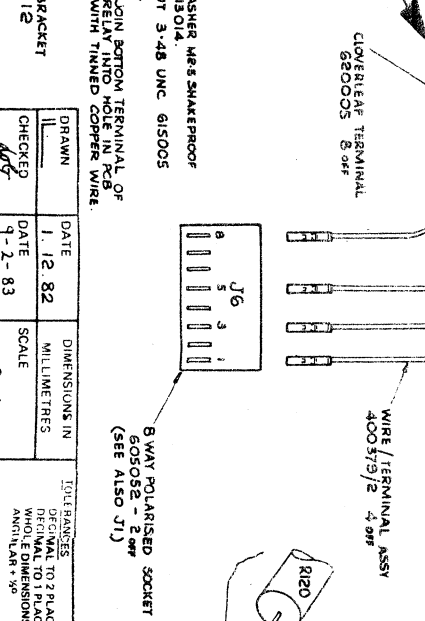
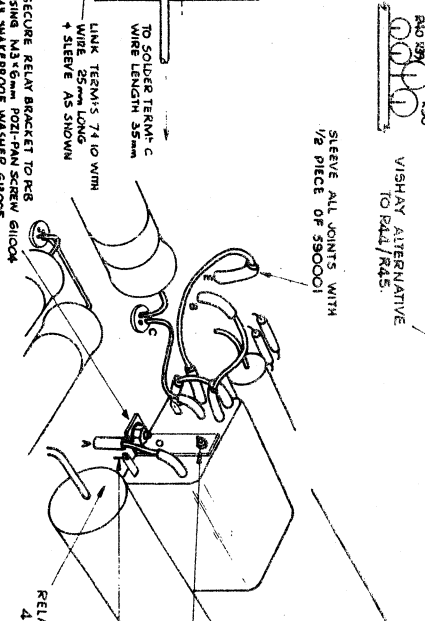


FSV TERMINAL 602001 8 0W
LEAVE PROJE SERIAL NO TAGS ON LEADS

COAT SURFACE OF DIODE BODY WITH HEATSINK COMPOUND 900003
HEATSINK ASSY (D59-D62)

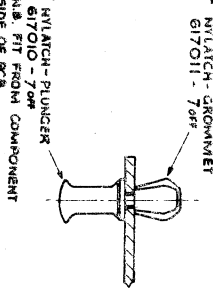
HEATSINK BLOCK 400383 20W
G100 4.15 20W
M3 GRINDWASHER 613029 20W

NOTE: - ALL RELAY WIRES USE 7/32 PINS INSULATED WHITE WIRE 440003 STRIP 5mm FROM EACH END.



MOUNTING ICs

NO	WAS	PART NO	NO OFF	USED TO MOUNT
1-4	605059	6	1.18, 1.2, 1.26, 1.32	
1-4	605060	8	1.18, 1.2, 1.26, 1.32	
1-6	605061	11	M/2 4/1 5/1 6/1 7/1 8/1 9/1 10/1 11/1 12/1 13/1 14/1 15/1 16/1	



ENSURE THAT ALL RESISTORS MARKED * ARE MOUNTED 3mm OFF PCB

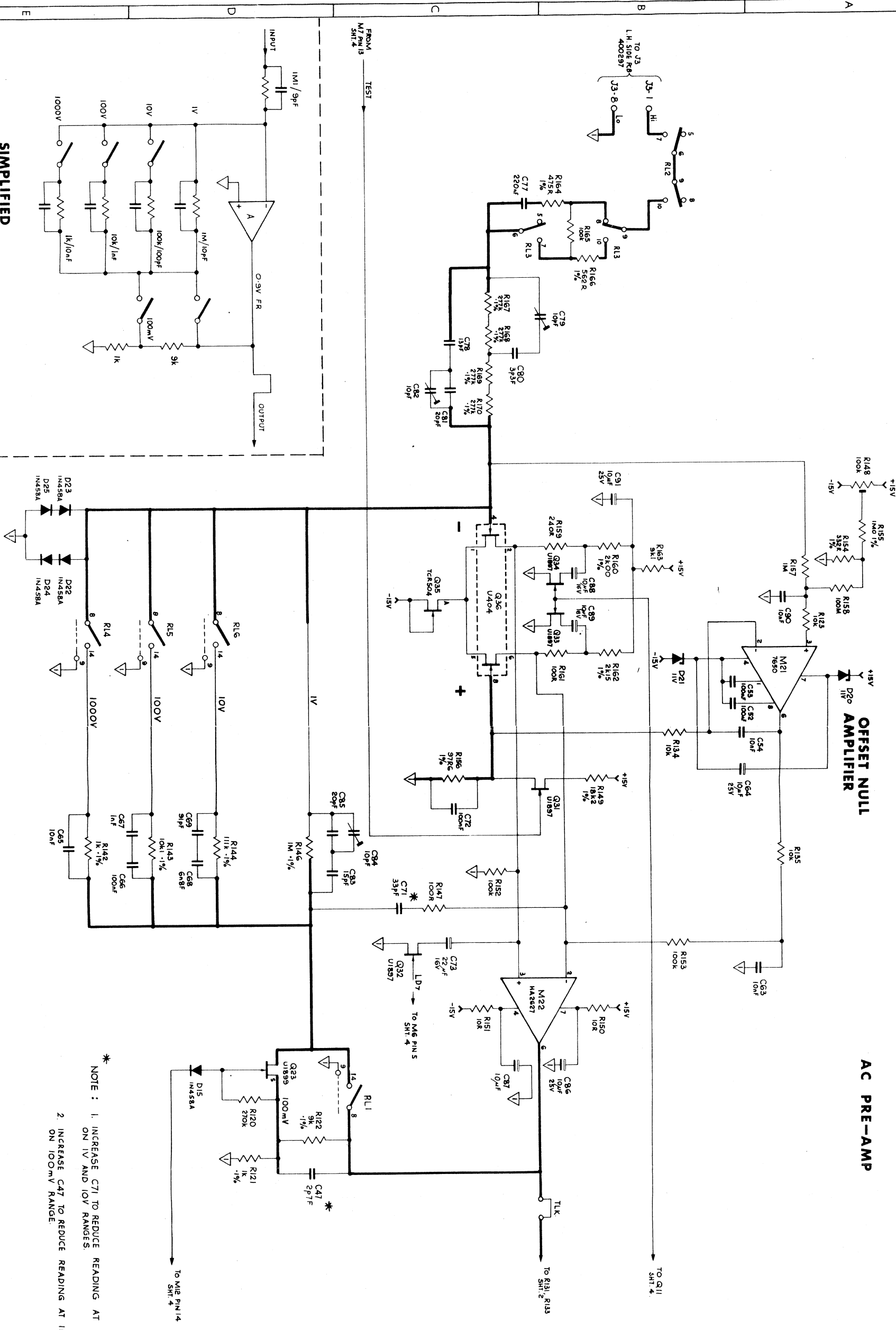
DATE	BY	DESCRIPTION
1-12-82	AWF	DRAWN
9-2-83	AWF	CHECKED
3-3-83	AWF	APPR

ANALOG PCB

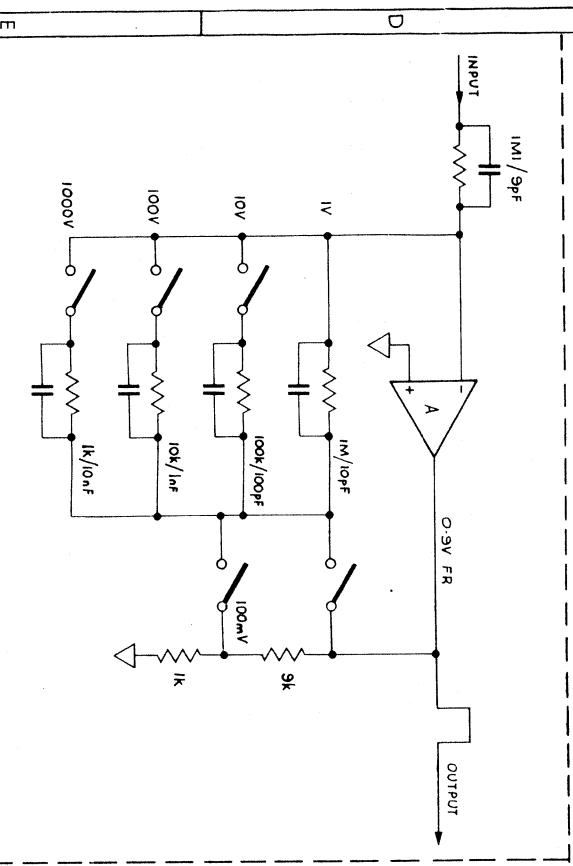
BIAS CURRENT

OFFSET NULL

AC PRE-AMP



SIMPLIFIED SCHEMATIC

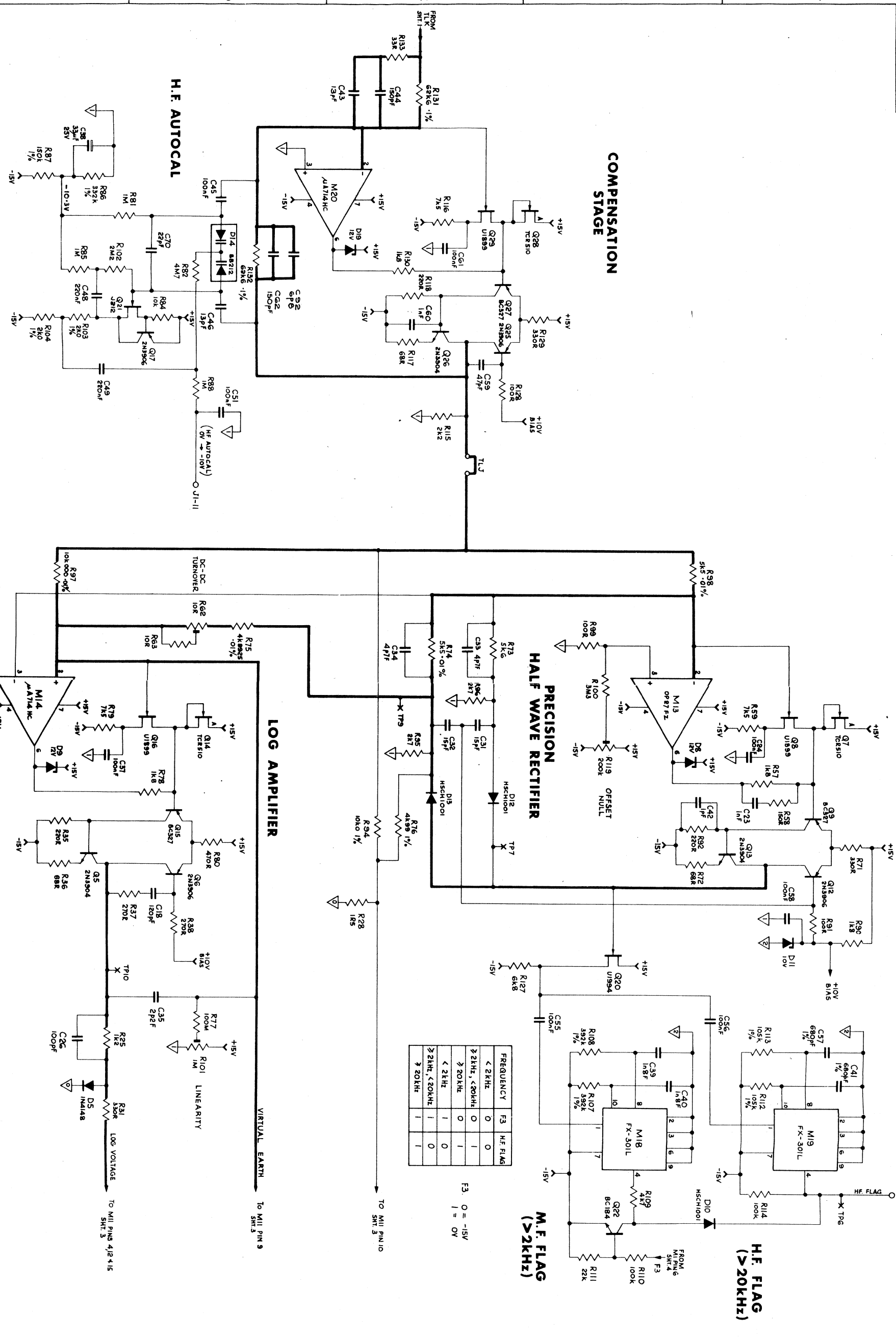


* NOTE : 1. INCREASE C71 TO REDUCE READING AT 1MHz ON 1V AND 10V RANGES.
2. INCREASE CAT TO REDUCE READING AT 1MHz ON 100mV RANGE

DRAWN	DATE	DIMENSIONS IN	TOLERANCES	MATERIAL	ASSY DRG & /	TITLE
CHECKED	DATE	MILLIMETRES	DECIMAL TO 2 PLACES : 1mm	FINISH	PARTS LIST	430504
APPR.	DATE	SCALE	ANGULAR TO 10 PLACES : 2mm		CHECK PROCEDURE	1081 AC PRE-AMP
R.V.W.F.	DATE	NOT TO BE SCALED	UNLESS OTHERWISE STATED		CHECK LIST	470504

ISS	CHANGES
1	RELEASED 12.4.83
2	ECO 14.8.83
3	2nd SHEET 2

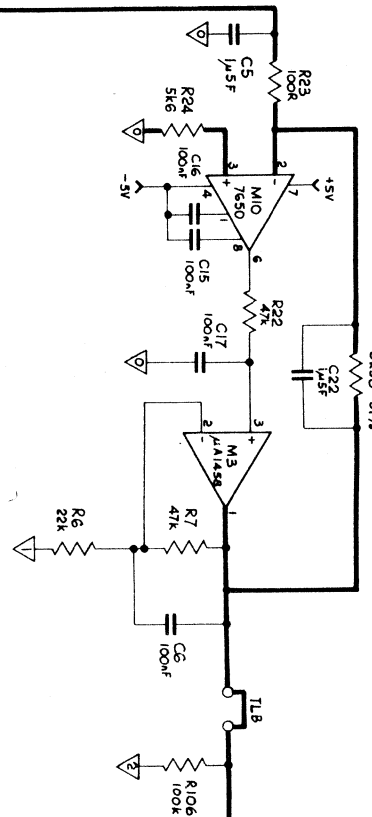
AC PRE-AMP



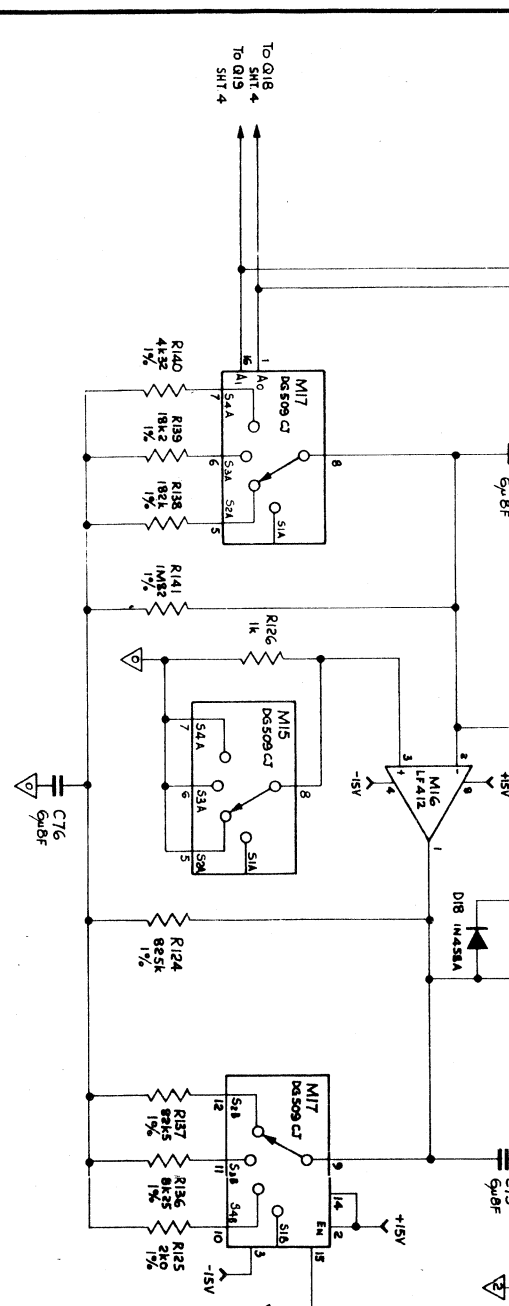
DRAWN	DATE	21.1.83	CONVERSIONS IN	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	TITLE
CHECKED	DATE	11.2.83	MILLIMETRES	DECIMAL TO 3 PLACES		430504	1081 AC
APPR.	DATE	12-4-83	SCALE	WHOLE DIMENSIONS	FINISH	460504	
				ANGULAR ± 1°		470504	
				UNLESS OTHERWISE STATED			
				FIRST ANGLE PROJECTION			

AC RECT. + LOG CONV.

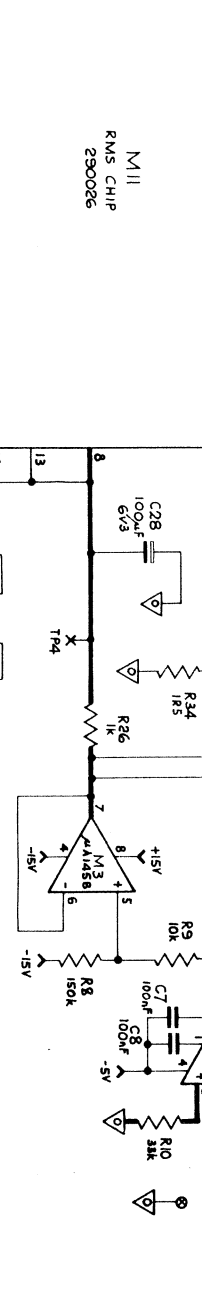
LOW PASS FILTER



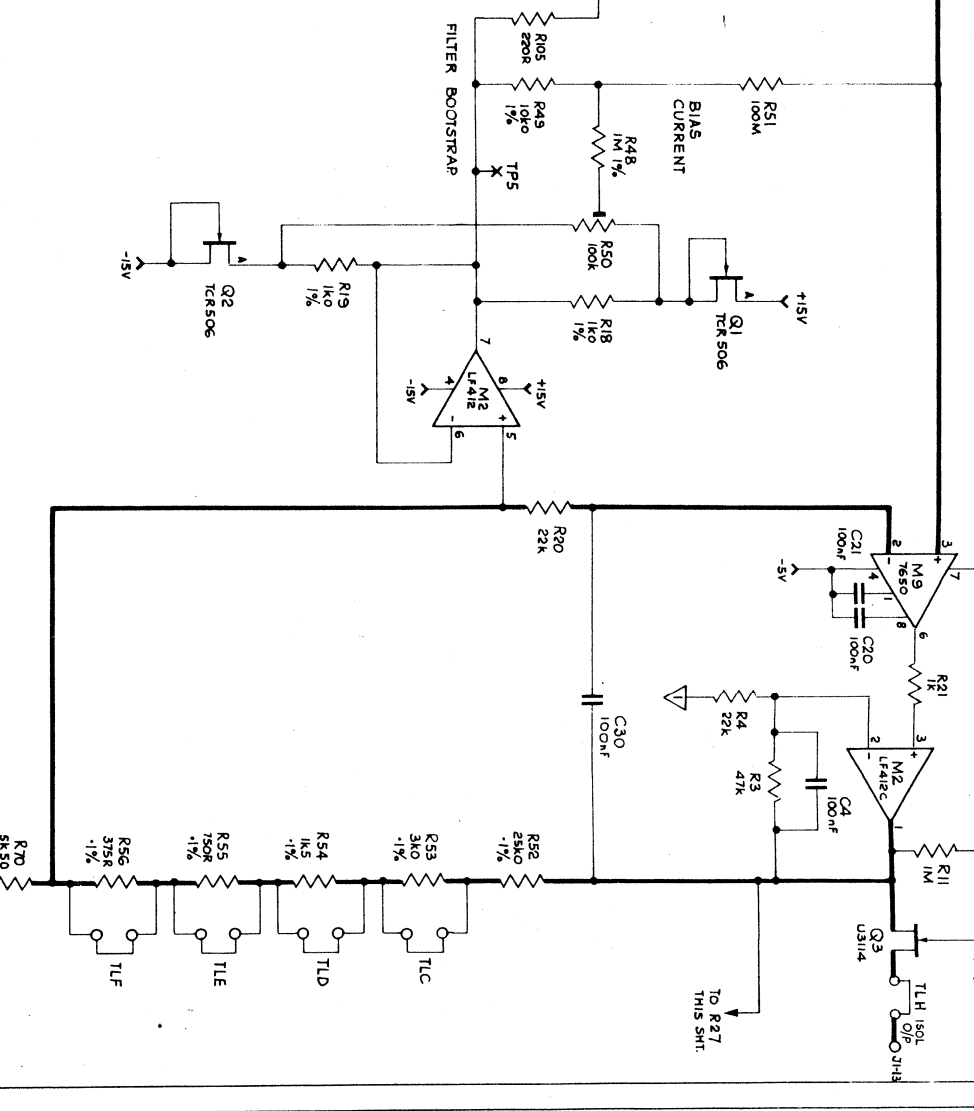
LF FILTERS



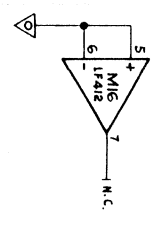
ANTI-STAGE



OUTPUT BUFFER



A1	A0	S1	S2	S3	S4	Filter	F0	F1	F2	F3
0	0	0	0	0	0	0.1Hz	0	0	0	0
0	0	0	0	0	0	1Hz	0	0	0	0
0	0	0	0	0	0	10Hz	0	0	0	0
0	0	0	0	0	0	100Hz	0	0	0	0

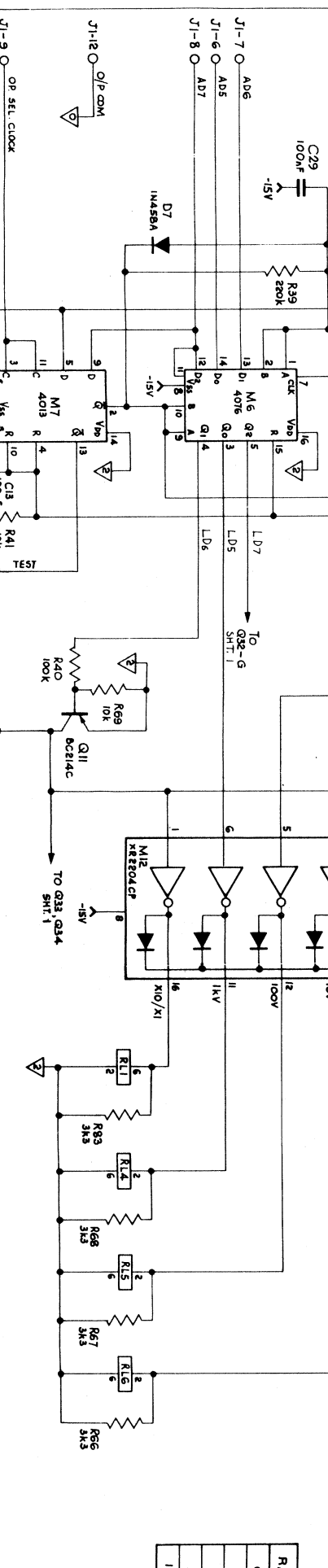
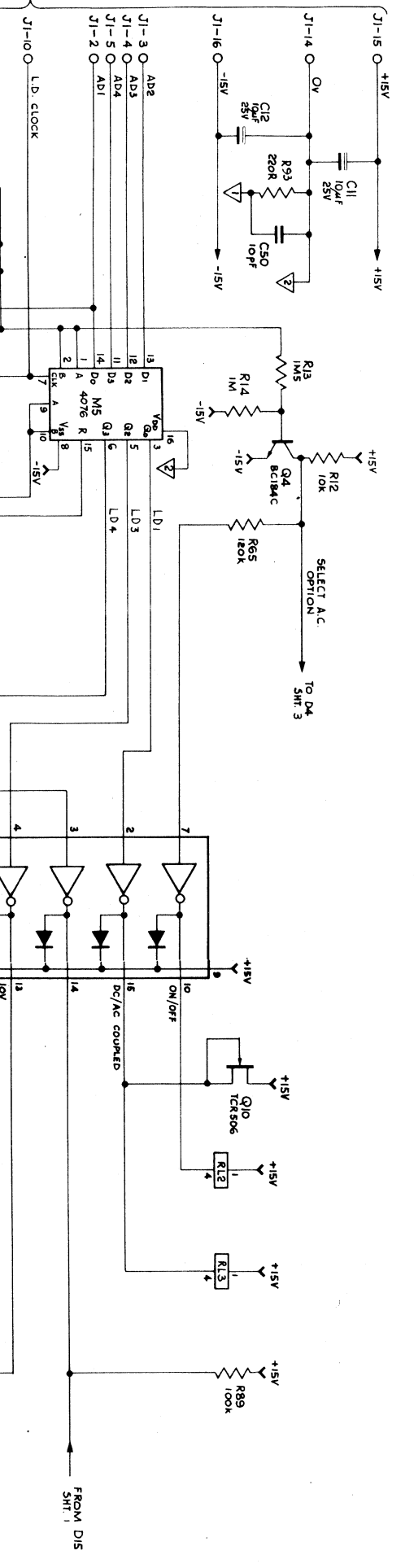
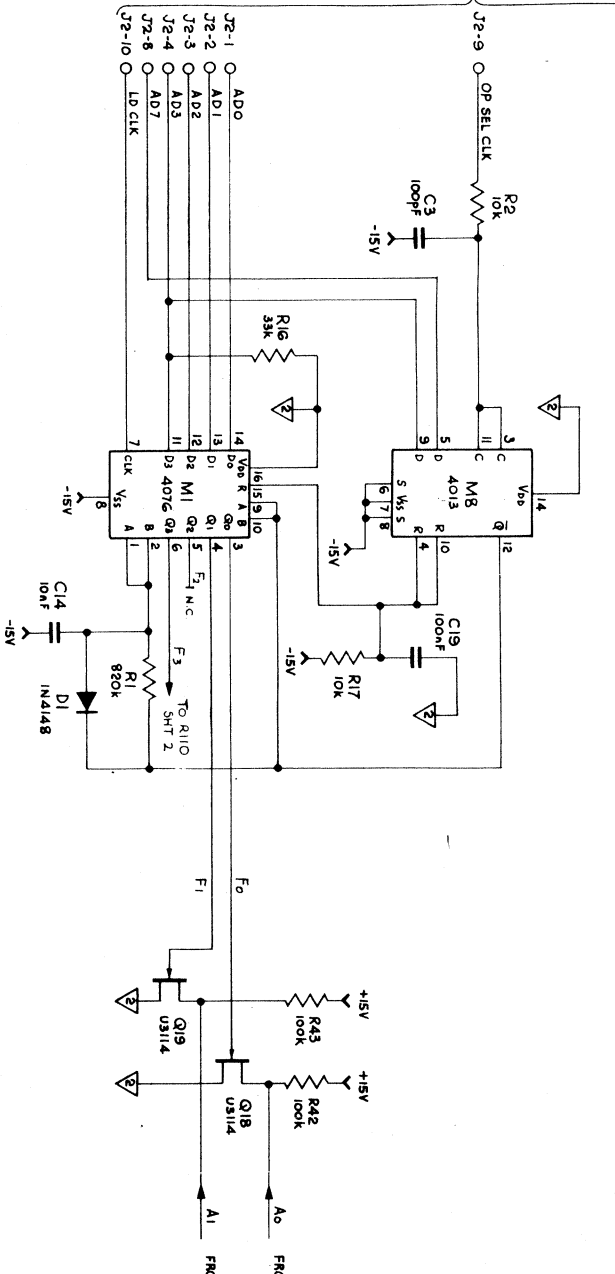
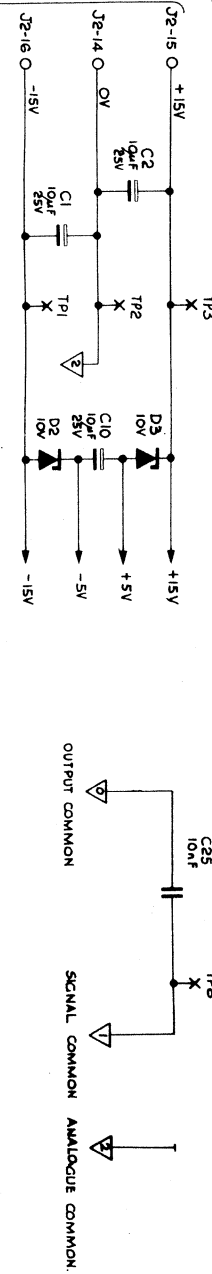


DRAWN	DATE	DIMENSIONS IN	TOLERANCES	MATERIAL	ASSY DRG & I	TITLE
L.O.G.	18.1.83	MILLIMETRES	TO 2 PLACES		430504	1081 AC RMS CONVERTER
CHECKED	DATE	SCALE	DECIMAL TO 1 PLACE	FINISH	CIRCUIT DIAGRAM	
R.W.F.	11.2.83		WHOLE DIMENSIONS		CHECK PROCEDURE	
APPR.	DATE	NOT TO BE SCALED	ANGULAR ± 30		CHECK LIST	
	12.4.83		UNLESS OTHERWISE STATED		470504	
			FIRST ANGLE PROJECTION			

TRANS CONV

DRAWING No.
430504

2 3 4 5 6 7



RANGE	LD ₁	LD ₂	LD ₃	LD ₄	LD ₅	LD ₆	LD ₇
0-1V	X	X	X	X	X	X	X
1V	X	X	X	X	X	X	X
10V	X	X	X	X	X	X	X
100V	X	X	X	X	X	X	X
1000V	X	X	X	X	X	X	X

DRAWN	DATE	SCALE	TOLERANCES	MATERIAL	ASSY. DRG. & PARTS LIST	TITLE
CHECKED	DATE	SCALE	DECIMAL TO 2 PLACES; 1mm		CHECK PROCEDURE	1081 AC RANGING
APPR.	DATE	SCALE	WHOLE DIMENSIONS TO 1mm		CHECK LIST	
R.V.V.F.	DATE	SCALE	UNLESS OTHERWISE STATED			
	DATE	SCALE	FIRST ANGLE PROJECTION			

430504
SHEET 4 OF 4

datron
ELECTRONICS
LIMITED
NORWICH

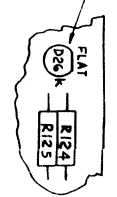
ISS	CHANGES
1	RELEASED 12.4.83
2	ECO 11.2.83
2	ECO 11.2.83

AC RANGING

GUARD SHEET 430388 TO BE SECURED WITH 2x10mm SCREWS 611007 3mm TO M3 HEX STANDOFFS.

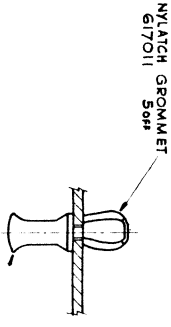
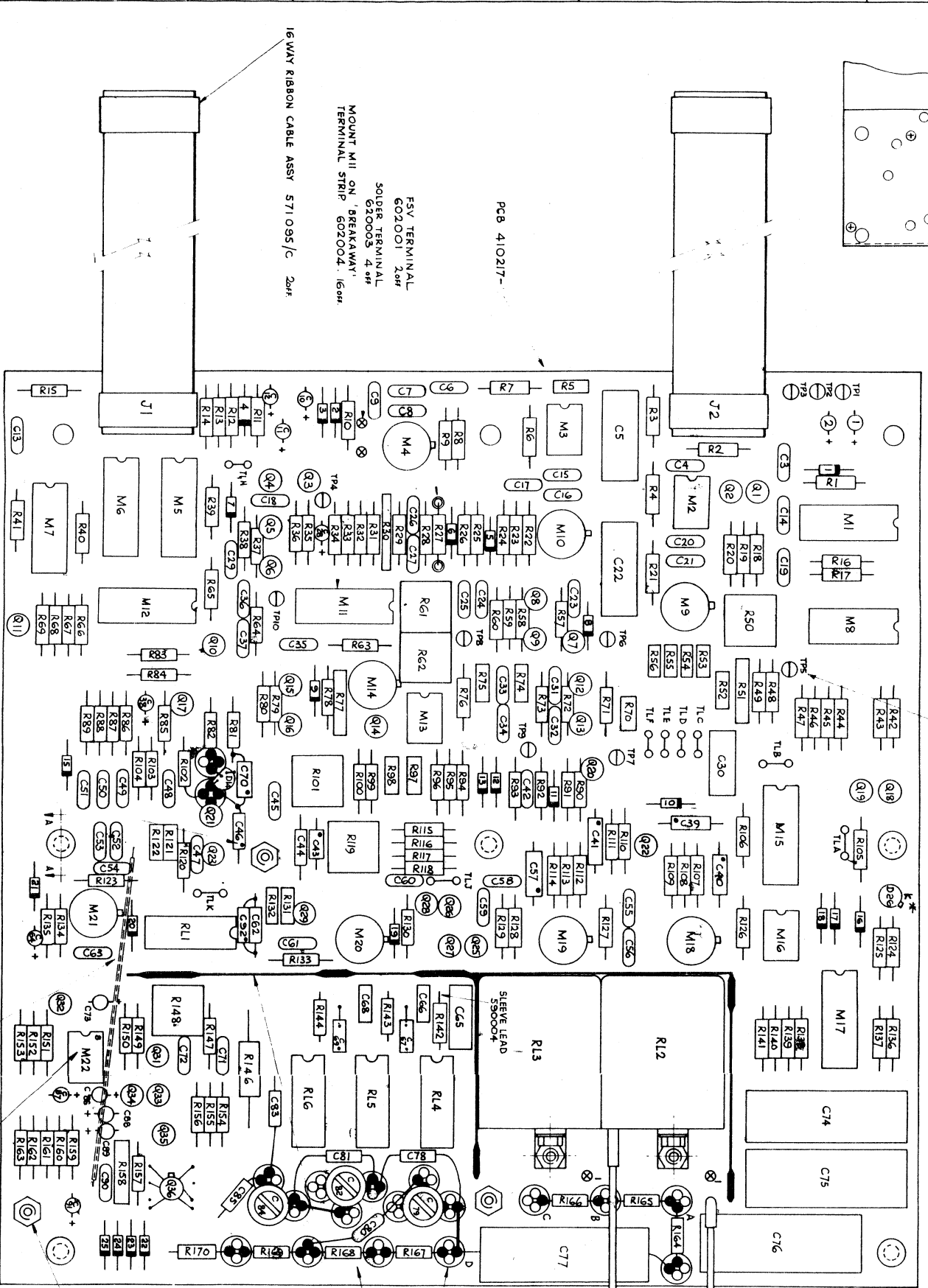
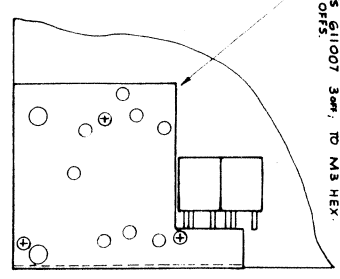
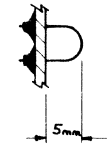
MOUNTING I.C.s		
NO OF WMS.	PART NO	USED TO MOUNT
8	605059	M2, M3, M13, M16
14	605060	M7, M8
16	605061	M1, 5, 6, 12, 15, 17

* N.B. WHEN FITTING SILICONIX DEVICE J14100 (E.P.S.) FIT AS SHOWN.



TEST POINT TERMINAL GPOO07 10.000

TEST LINKS MADE FROM 28 SWG. 540002 N/A.



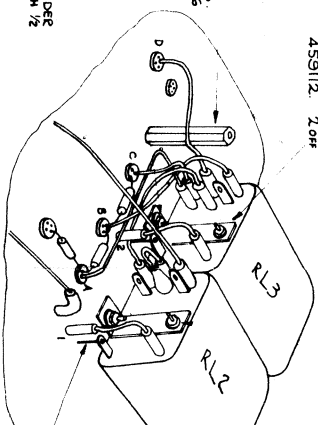
SECTION A-A

NYLATCH PLUNGER 617010 5.000 N.B. FIT FROM COMPONENT SIDE OF PCB.

DOT DENOTES OUTER FOIL (RED) END OF POLYSTYRENE CAPACITORS I.E. C39, C40, C41, C45, C46, C57, C70 C82.

CROP PIN 8 FROM M22 BEFORE FITTING INTO PCB
LINK MADE FROM 7/02 PTFE INSULATED WHITE WIRE 540008 X 70mm FIT TO UNDERSIDE OF PCB.

SOLDER WIRE ENDS TO SOLDER TERMINALS & SLEEVE WITH 1/2 PIECE OF 540001

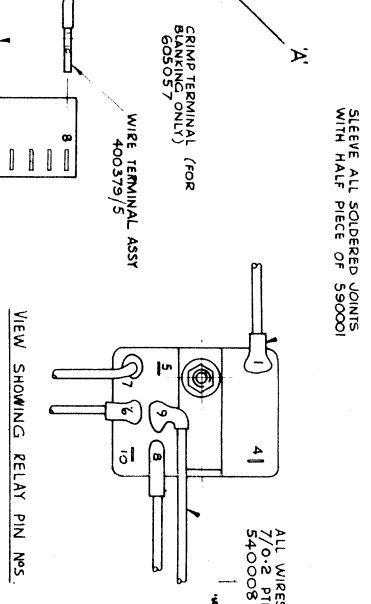


SOLDER WIRE LINKS BETWEEN RELAY TERMINALS AS SHOWN ON R13 & R15 540002

VIEW IN DIRECTION OF ARROW A

N.B. C77 REMOVED FROM VIEW, FOR CLARITY.

RELAY WIRING		
FROM	TO	LENGTH (mm)
R12 PIN 1	SOLDER PIN 1	25
R12 PIN 6	R12 PIN 9	25
R12 PIN 7	J3 PIN 1	120
R12 PIN 10	R13 PIN 9	40
R13 PIN 1	SOLDER PIN 2	25
R13 PIN 7	C/LEAF B	45
R13 PIN 6	C/LEAF D	35
R13 PIN 10	C/LEAF C	25
R13 PIN 8	C/LEAF A	55



SLEEVE ALL SOLDERED JOINTS WITH HALF PIECE OF 540001

CRIMP TERMINAL (FOR BLANKING ONLY) 605057

WIRE TERMINAL ASSY 605057/5

VIEW SHOWING RELAY PIN NOS.

WIRE 145mm PTFE INSULATED 7/0.2 WHITE 540008 PLUS COLD CRIMP TERMINAL 605057 FITTED AS SHOWN

8-WAY POLARISED SOCKET 605052

WIRE 145mm PTFE INSULATED 7/0.2 WHITE 540008 PLUS COLD CRIMP TERMINAL 605057 FITTED AS SHOWN

CLOVERLEAF TERMINAL GPOO05 18.000

SLEEVE LEADS OF CRO BEFORE SOLDERING LEADS INTO CLOVERLEAF POSITION CAP AND LEADS AWAY FROM CLOVERLEAF.

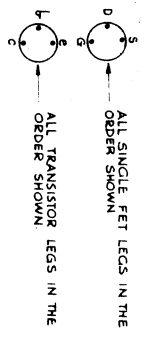
BRASS STRIP 220mm LONG 630107 N.B. STRIP SHOULD BE SOLDERED AS CLOSE AS POSSIBLE TO LEFT HAND SIDE OF COPPER LAND AS SHOWN.

DRAWN		DATE		DIMENSIONS IN		TOLERANCES		MATERIAL	
CHECKED	L.O.G.	21.12.82	SCALE	MILLIMETRES	TO 2 PLACES: ±1mm	DECIMAL TO 1 PLACE: ±0.2mm	WHOLE DIMENSIONS: ±0.5mm	ANGULAR: ±1°	FINISH
R.W.F.		14.4.83	2:1	NOT TO BE SCALED	UNLESS OTHERWISE STATED	FIRST ANGLE PROJECTION			

ASSY DRG & I		PARTS LIST		CIRCUIT DIAGRAM		CHECK PROCEDURE		CHECK LIST	
400504	430504	460504	470504	1081 AC PCB ASSY					

AC PCB

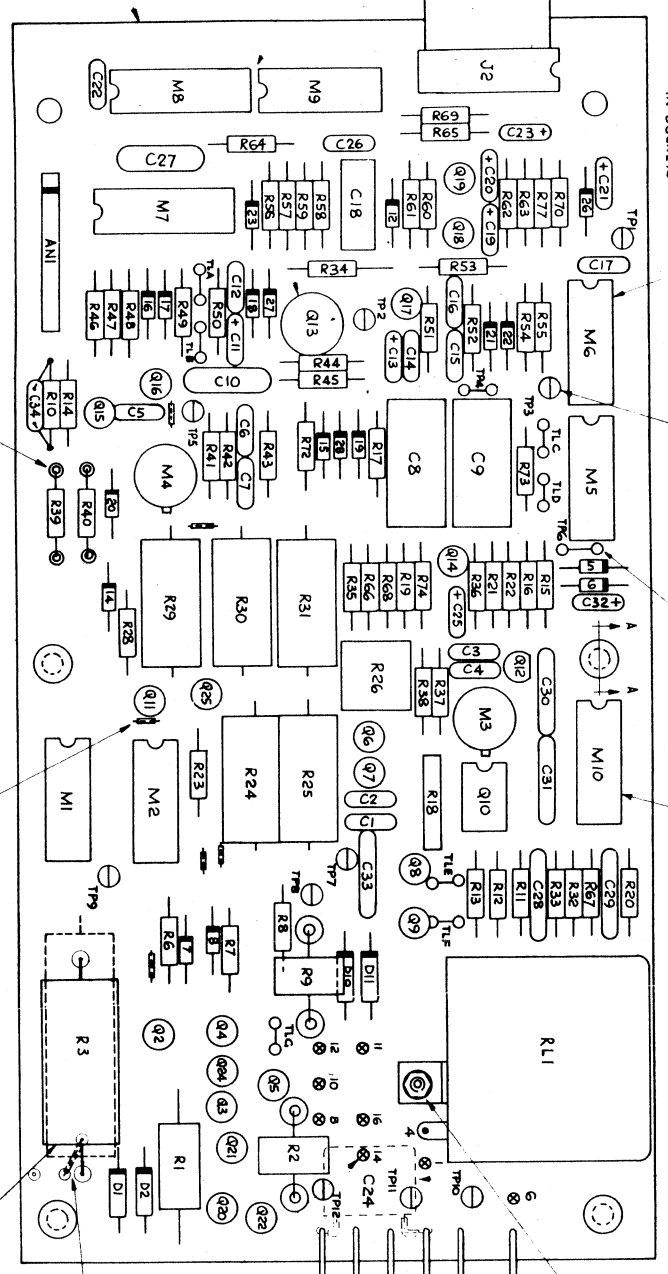
ISS	CHANGES
1	RELEASED 31.3.83
2	ECO 1484-1500 ECO ADDED PART N° 428-821 PART N° 15508 WIRE 1 L/JR 8.6.83



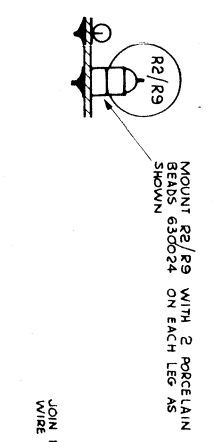
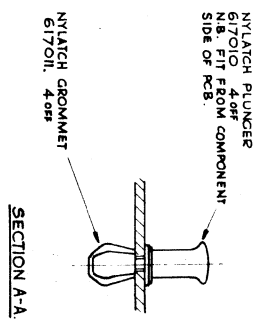
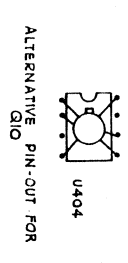
16 WAY RIBBON CABLE ASSY 571095 C SOLDERED END WITHOUT CABLE CLIP

ENSURE IC'S DO NOT TOUCH WHEN FITTED CORRECTLY IN SOCKETS

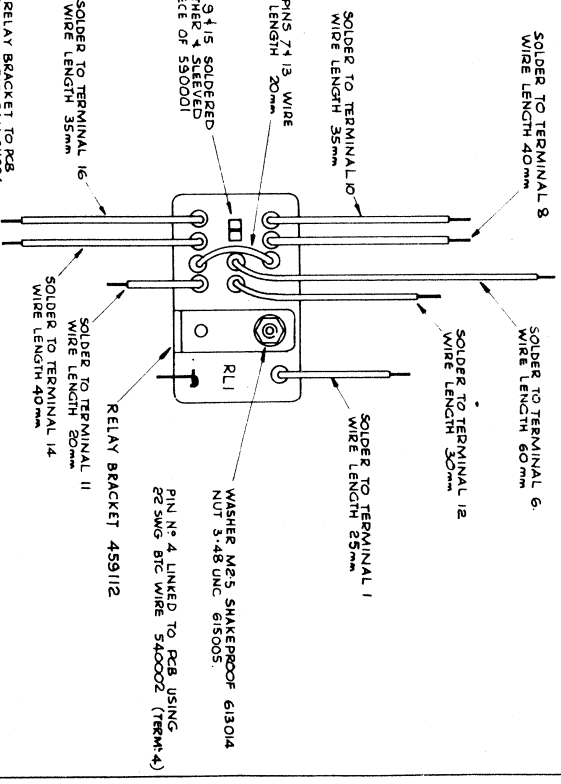
MOUNT Q13 ON T05 MOUNTING PCB 618002



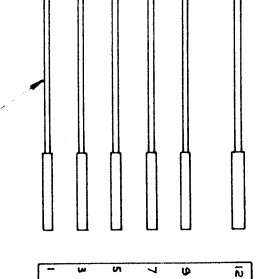
FSV TERMINAL 620001 4 off



FIT C24 ON UNDERSIDE OF PCB BETWEEN 01-1 AND 01-7 BEAD IN SMALL QUANTITY BEAD IN SMALL QUANTITY SLEEVE LEADS WITH 590004 AND WRAP AROUND PINS.



ALL RELAY WIRES USE 7/8 PTFE INSULATED WHITE WIRE 540008 SLEEVE ALL JOINTS WITH 1/2 PIECE OF 590001.



WIRE / TERMINAL ASSY 400379/2

SOLDER TERMINAL 620003 8 off

SLEEVED LINK ON UNDERSIDE OF PCB 540002 / 590004

R3 'MANN' COMPONENT (09007)

NO OF WAYS	PART N°	N° OFF	USED TO MOUNT
14	605060	5	M1, M2, M5, M6, M8
16	605061	2	M7, M8

DATE	DATE	DATE	DATE
9.12.82	9.2.83	3.3.83	

DRAWN	CHECKED	APPR.
		RWF

DATE	SCALE	TOLERANCES	MATERIAL	FINISH
9.12.82	2:1	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION		

ASSY DRG & PARTS LIST	CIRCUIT DIAGRAM	CHECK PROCEDURE	CHECK LIST
400505	430505	460505	470505

TITLE	DRAWING NO.
IOBI OHMS PCB ASSY	400505

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OHMS PCB

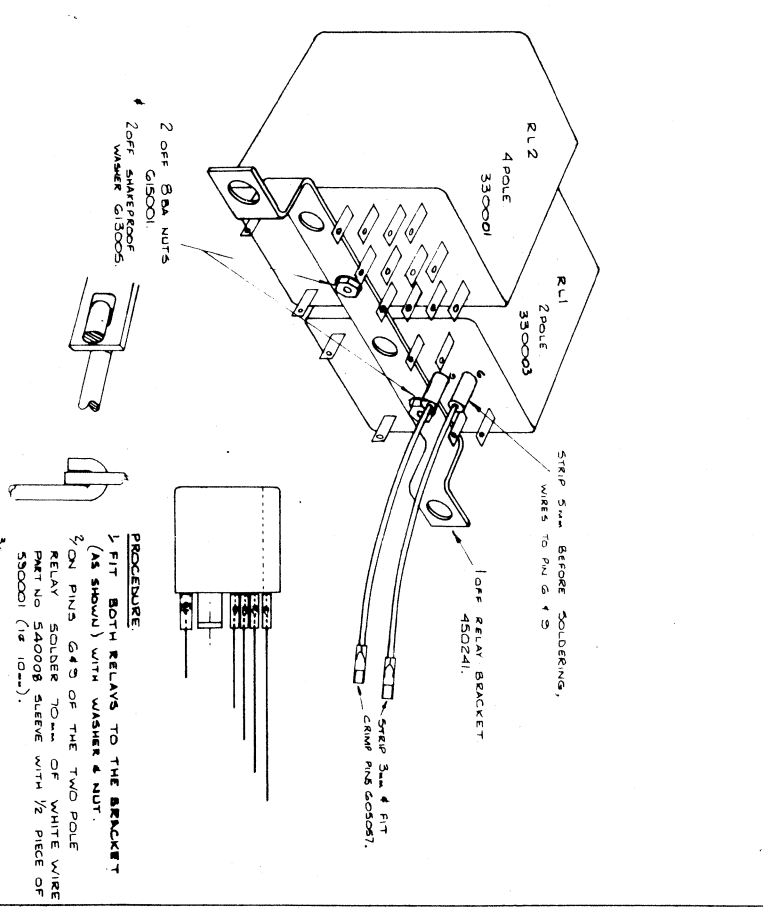
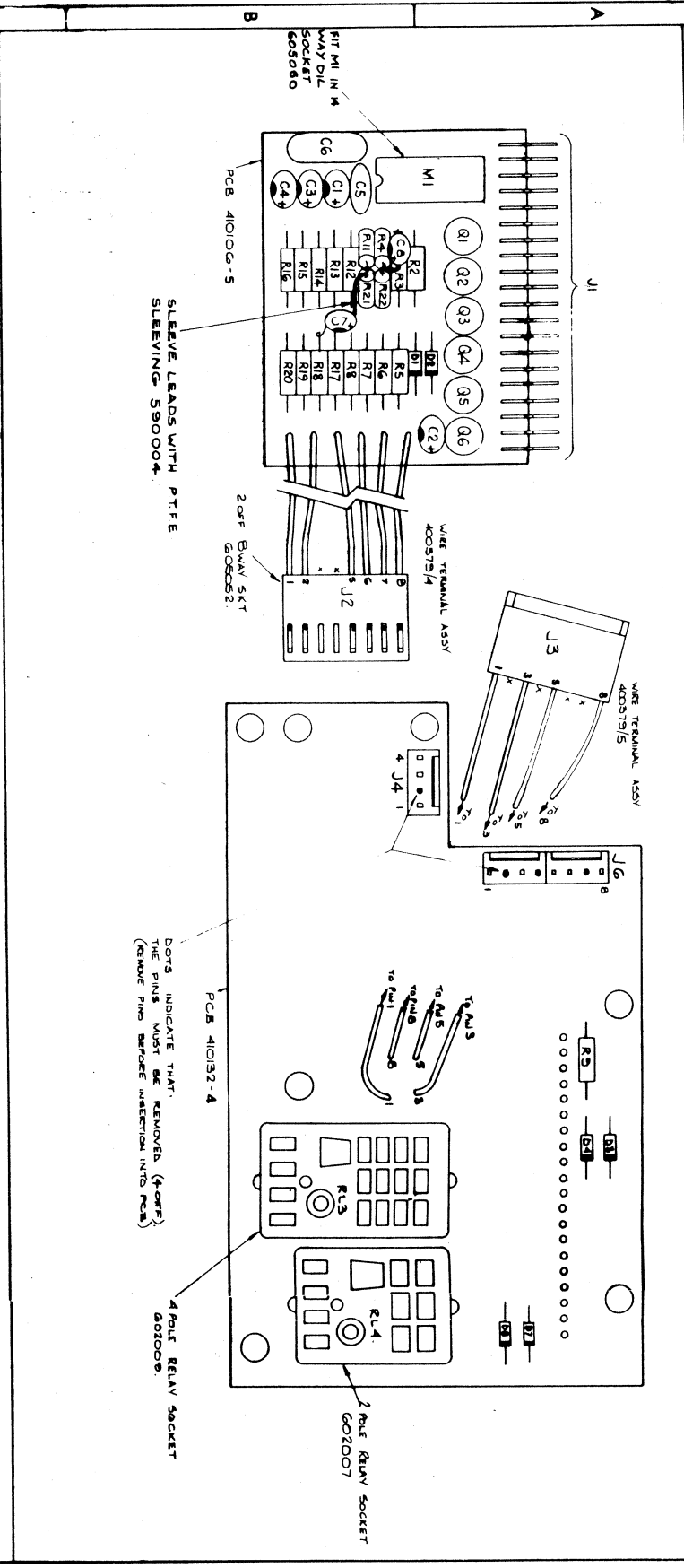
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

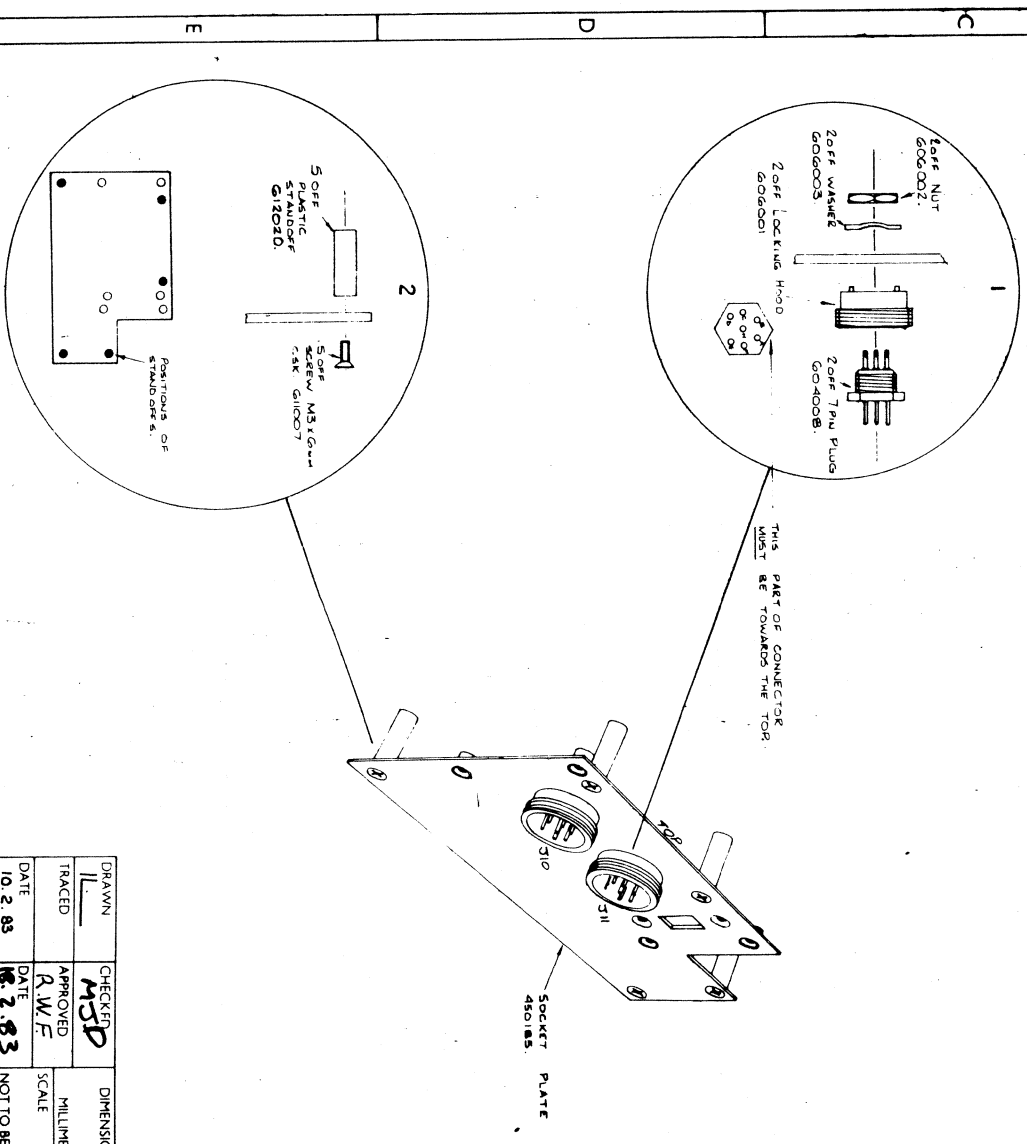
ALL BURS TO BE REMOVED

NOTES
 IMPORTANT
 FOR CRIMP PINS USE TOOL NO. HTR2222A.

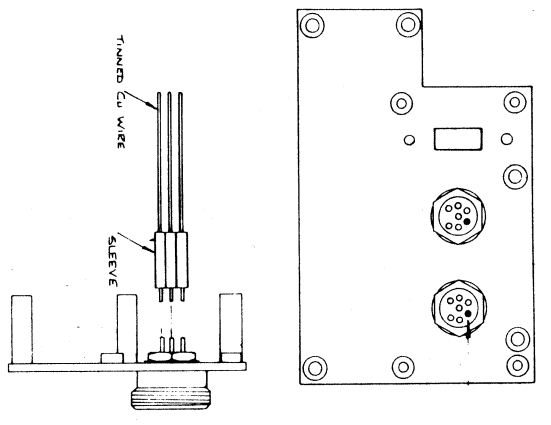
ISS.	CHANGES
1	RELEASED 31.3.83



PROCEDURE
 1 FIT BOTH RELAYS TO THE BRACKET (AS SHOWN) WITH WASHER & NUT.
 2 ON PINS G43 OF THE TWO POLE RELAY SOLDER 70% OF WHITE WIRE PART NO 540008 SLEEVE WITH 1/2 PIECE OF 590001 (10 1022).
 3 ALL OTHER CONTACTS ARE TO HAVE APPROXIMATELY 60mm OF 22 SWG TINNED COPPER WIRE PART NO 540002 & SLEEVE EACH WITH 1/2 PIECE OF 590001.
 4 STRAGGLE LENGTHS OF TINNED COPPER WIRE TO ASSIST FITTING TO PCB (AS SHOWN).



PROCEDURE
 1 ASSEMBLE THE 7 PIN PTFE PLUGS FIRST & ENSURE THAT THE CONNECTORS ARE SECURED IN THE POSITION SHOWN.
 2 ASSEMBLE THE 5 STANDOFF'S IN THE POSITION SHOWN BY THE LARGE DOTS.



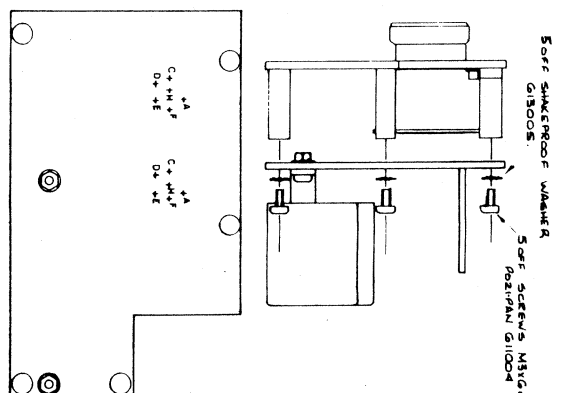
PROCEDURE
 1 ALL PINS ON EACH SOCKET EXCEPT PIN B (SHOWN SOLID) SOLDER ON 60% OF TINNED COPPER WIRE PART NO 540002 & SLEEVE ALL JOINTS WITH APPROXIMATELY 10mm OF SLEEVING PART NO 590001.
 THERE SHOULD NOW BE 12 WIRES.

DRAWN	CHECKED	DIMENSIONS IN	TOLERANCES	ANGULAR ±	MATERIAL
TRACED	MSD	MILLIMETRES	DECIMAL TO 3 PLACES ±	90°	
DATE	APPROVED	SCALE	DECIMAL TO 1 PLACE ±	100	FINISH
10.2.83	R.W.F.	NOT TO BE SCALED	DECIMAL TO 1 PLACE ±	100	
	DATE		UNLESS OTHERWISE STATED		

datron ELECTRONICS LTD. NORWICH.
 REAR INPUT / RATIO ASSY 1081

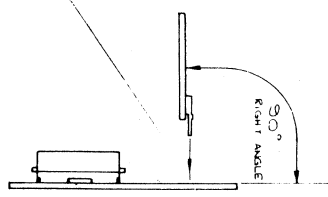
DRAWING No. 400506
 DRAWING SIZE A1
 SHEET 1 OF 8

REAR INPUT & RATIO PCB'S

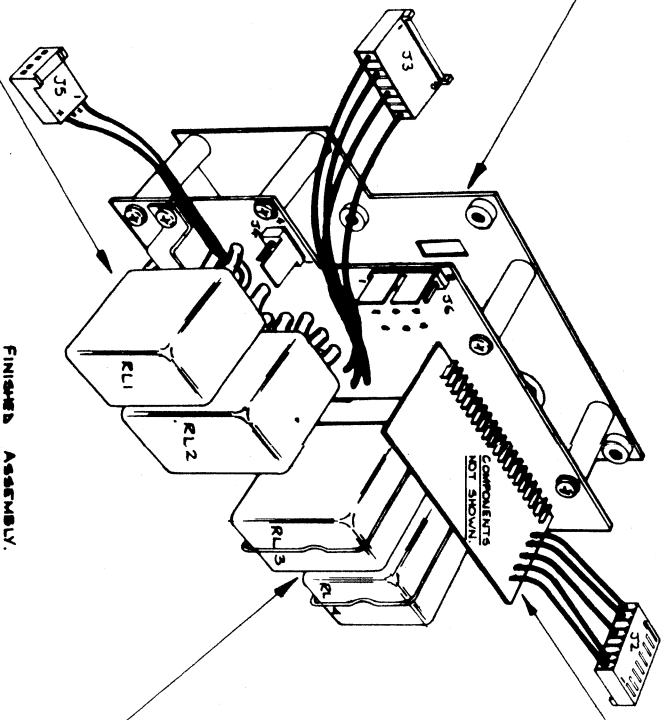


3/ BOTTOM VIEW SHOWS THE HOLES IN THE PCB (INDICATED BY CROSSES). THESE HOLES ARE FOR THE WIRES FROM THE TWO 7 PIN SOCKETS. IT IS A SUGGESTION THAT THE WIRES ARE STAGGERED TO MAKE ASSY EASIER (AS WIRING THE RELAY).

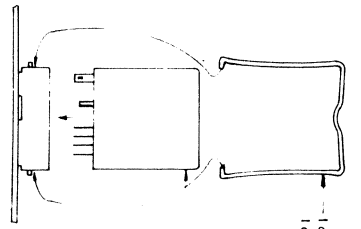
PROCEDURE:
 1/ THE WIRES SHOULD LINE UP WITH THE APPROPRIATE HOLES, I.E. WIRE FROM PIN A OF SOCKET SHOULD BE INSERTED INTO HOLE A, WIRE FROM PIN C TO HOLE C AND SO ON.
 2/ WHEN THE WIRES ARE INSERTED IN THE APPROPRIATE HOLES, SECURE THE 2 AWG'S TOGETHER WITH THE MIX-G-M 7021-PW SCREWS & SHAKEROOF WASHERS, SCREWED IN THE 5 STANDOFFS (AS DETAILLED).
 3/ LIGHTLY PULL ON THE TWO CORNER WIRES SO THE WIRE IS TIGHT THEN SOLDER & CRIP IN THE USUAL MANNER.



2/ INSERT CONNECTORS AS SHOWN. SOLDER ALL 20 AMP PINS & CRIP THE BOARD IS TO BE AT 90° WHEN SOLDERED IN.



FINISHED ASSEMBLY.

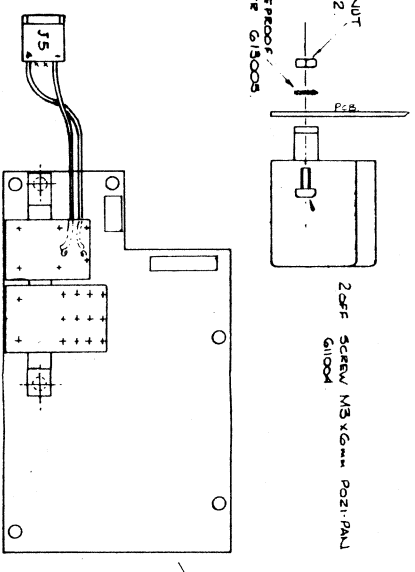


1 OFF CLIP 350005 (2 Pole)
 1 OFF CLIP 350028 (4 Pole)
 1 OFF 2 POLE RELAY 350005
 1 OFF 4 POLE RELAY 350001

4/ THE LAST PROCEDURE IS TO PLUG IN THE 4 & 2 POLE RELAYS & HOLD IN PLACE BY THE CLIPS PROVIDED AS DETAILED IN ABOVE SKETCH & FINISHED VIEW.

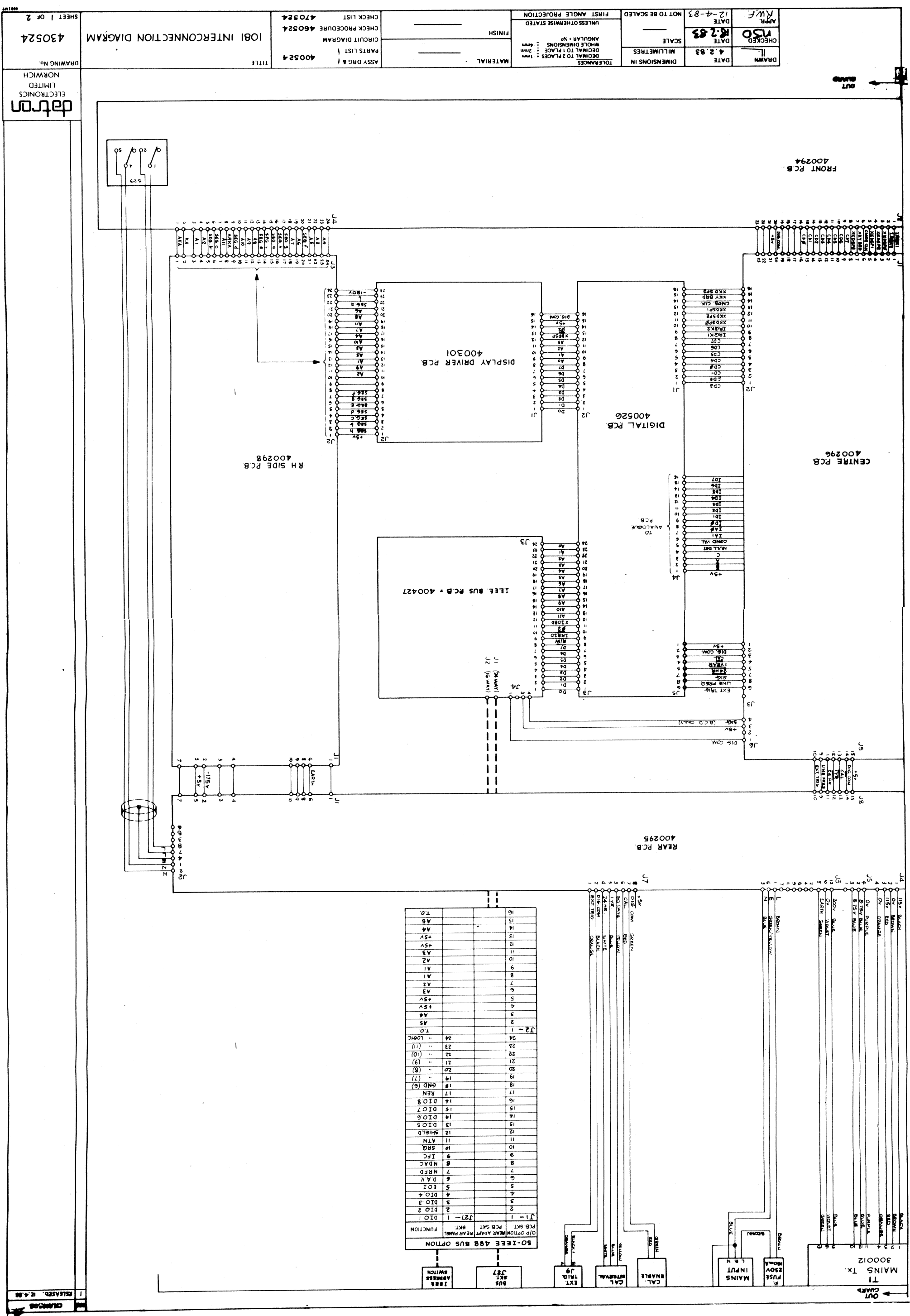
1/ SKETCH BELOW SHOWS THE 2 RELAY & BRACKET ASSEMBLY (FROM SHEET 1). THE CROSSES INDICATE HOLES IN THE PCB INTO WHICH THE WIRES FROM THE RELAYS ARE INSERTED.

PROCEDURE:
 1/ INSERT THE WIRES INTO THE APPROPRIATE HOLES IN THE PCB (WIRES CUT AT DIFFERENT LENGTHS TO AID ASSEMBLY).
 2/ WHEN THE WIRES ARE ALL IN PLACE SECURE THE BRACKET TO THE PCB USING THE SCREWS, WASHERS & NUTS SHOWN BELOW.
 3/ SOLDER & CRIP WIRES IN THE USUAL MANNER. INSERT THE CRIMP PINS INTO SOCKET J5. PINS OF RELAY TO PINS 4 OF J5 & PINS 5, P.M.I. AS SHOWN BELOW.



DRAWN	CHECKED	DIMENSIONS IN	TOLERANCES	ANGULAR	MATERIAL	TITLE	DRAWING No.	DRAWING SIZE
11	MSD	MILLIMETRES	DECIMAL TO 2 PLACES FRACTIONAL HENCE DIMENSIONS IN PLACES DECIMAL TO 1 PLACE WITHOUT DIMENSION SYMBOL	0.05 0.10 0.15 0.20 0.25 0.30 0.40 0.50 0.60 0.70 0.80 0.90 1.00 1.50 2.00 3.00 4.00 5.00 6.00 8.00 10.00	FINISH	REAR INPUT / RATIO ASSY. 1081	400506	A1
TRACED	APPROVED	SCALE	UNITS DIMENSIONS SHOWN	UNITS DIMENSIONS SHOWN				SHEET
DATE	DATE	NOT TO BE SCALED						2 OF 3
10.2.83	18.3.83							

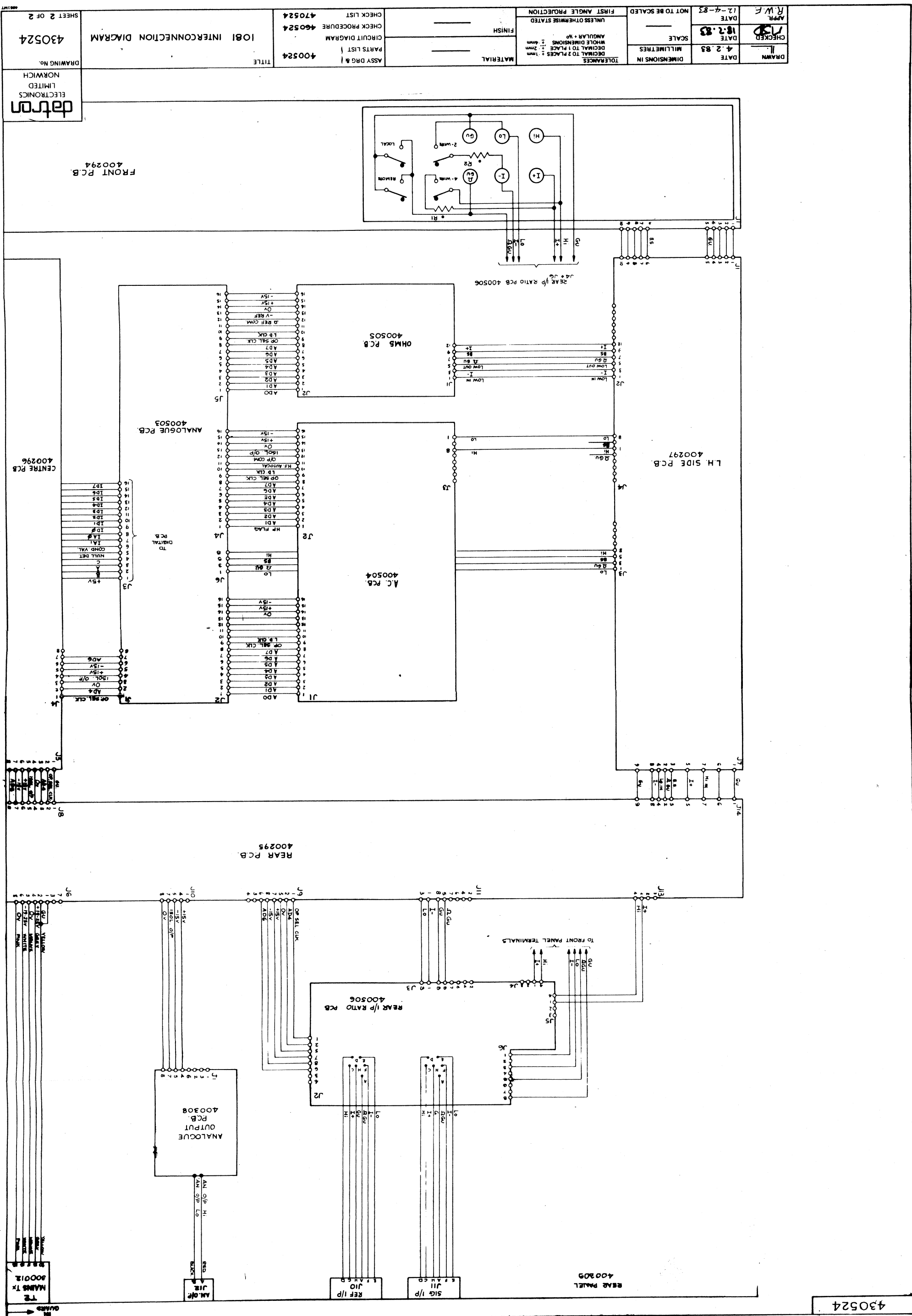
REAR INPUT/RATIO RELAYS



DRAWING No. 430524
 SHEET 1 OF 2
 daton ELECTRONICS LIMITED NORWICH
 CHECKED DATE 12-4-83
 SCALE 1:1
 DIMENSIONS IN MILLIMETRES
 UNLESS OTHERWISE STATED
 FIRST ANGLE PROJECTION
 FINISH
 MATERIAL
 ASSY DRG # 400524
 PARTS LIST
 CHECK PROCEDURE 460524
 CHECK LIST 470524
 TITLE 1081 INTERCONNECTION DIAGRAM
 RELEASED: 12-4-83
 1

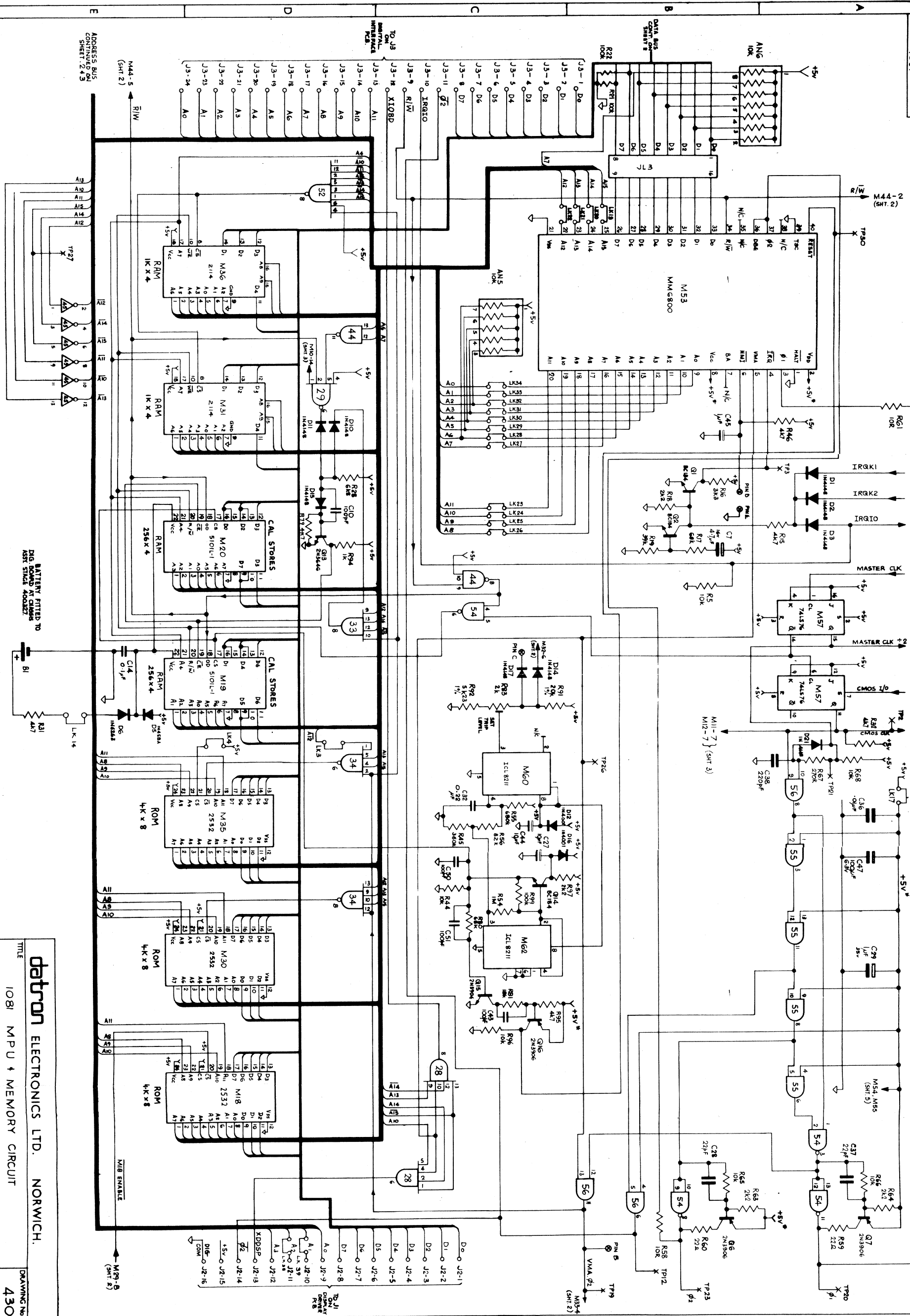
INTERCONNECTIONS 1

INTERCONNECTORS 2



DATE: 12-4-83	APPR. R.W.F.	FINISH	CHECK LIST	470524	430524
DATE: 18.2.83	CHECKED: J.S.D.	MATERIAL	CIRCUIT DIAGRAM	460524	430524
DATE: 4.2.83	DRAWN: J.L.	TOLERANCES	PARTS LIST	400524	430524
DIMENSIONS IN MILLIMETRES	SCALE: 1:1	DECIMAL TO 2 PLACES: 1mm	ASSY DRG & I	TITLE	1081 INTERCONNECTION DIAGRAM
NOT TO BE SCALED	UNLESS OTHERWISE STATED	WHOLE DIMENSIONS: 1mm	CHECK PROCEDURE	DRAWING NO.	430524
FIRST ANGLE PROJECTION	ANGULAR: 1/2	ANGULAR: 1/2	CHECK LIST	SHEET 2 OF 2	

datron ELECTRONICS LIMITED NORWICH



datron ELECTRONICS LTD. NORWICH.
 TITLE IOBI MPU + MEMORY CIRCUIT
 DRAWING No. 430526
 SHEET 1 OF 3
 DRAWING SIZE A1

BATTERY FITTED TO
 DIG. BOARD AT CHANGE
 ASST. STAGE 400227

ADDRESS BUS
 CONTINUED ON
 SHEET 2, 3

DIGITAL 1 MPU + MEMORY

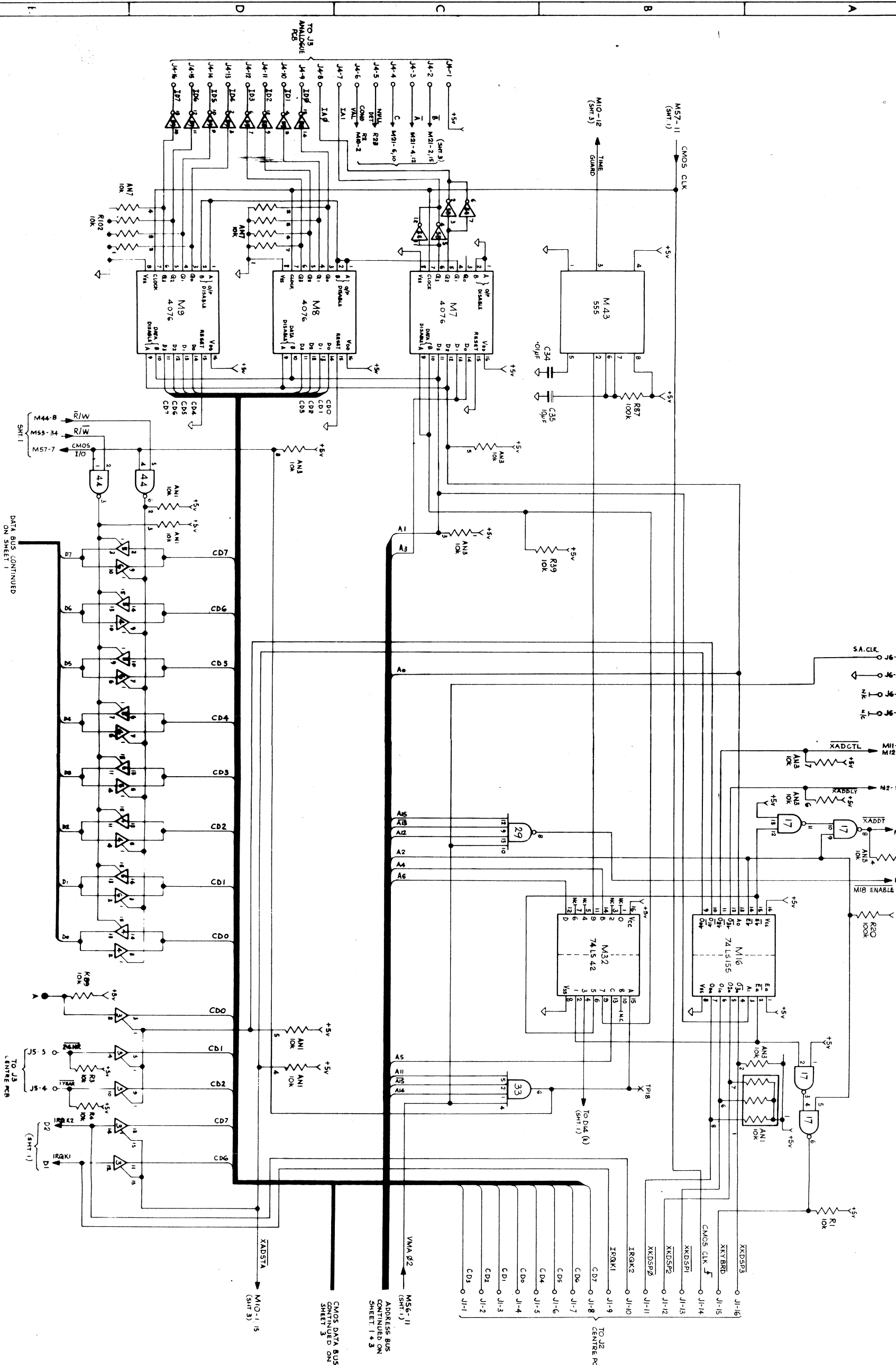
DRAWING No. 43052G
FIRST USED ON

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

ALL BURS TO BE REMOVED

NOTES

ISS	CHANGES
1	RELEASED 31.3.83



DATA BUS CONTINUED ON SHEET 1

TO J3 CENTRE PCB

ADDRESS BUS CONTINUED ON SHEET 1 + 3

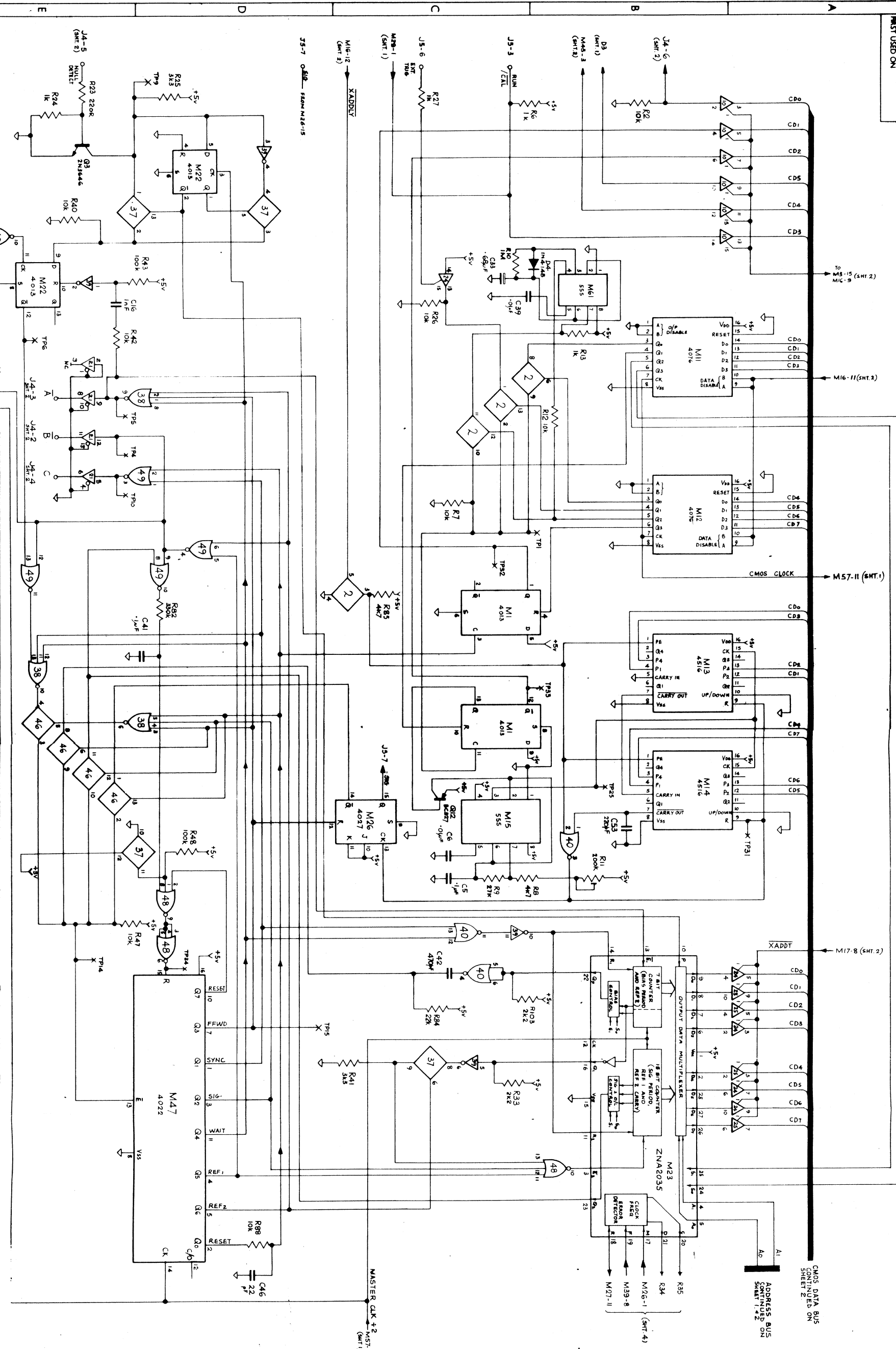
CMOS DATA BUS CONTINUED ON SHEET 1 + 3

DRAWN	CHECKED	DIMENSIONS IN	UNITS
TRACED	APPROVED	MILLIMETRES	
DATE	DATE	UNITS	
28.1.83			

datron ELECTRONICS LTD. NORWICH 11
1081 CMOS ADDRESS DECODE + I/O CCT

DRAWING No. 43052G
SHEET 2 OF 5

DIGITAL 2 CMOS



DRAWN	11	CHECKED	L.O.G.	DIMENSIONS IN	TOLERANCES	ANGULAR	MATERIAL
TRACED		APPROVED	R.W.F.	MILLIMETRES	UNLESS OTHERWISE SPECIFIED		
DATE	31.1.83	DATE	31.3.85	SCALE	NOT TO BE SCALED		

datron ELECTRONICS LTD. NORWICH.
 TITLE 1081 A-D CONVERTER.

DRAWING No. 430526
 SHEET 3 OF 3

DIGITAL 3 ADC

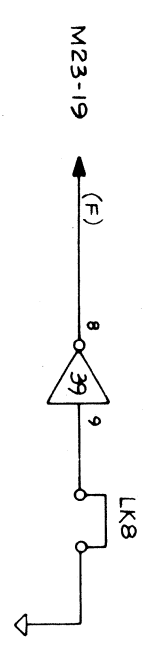
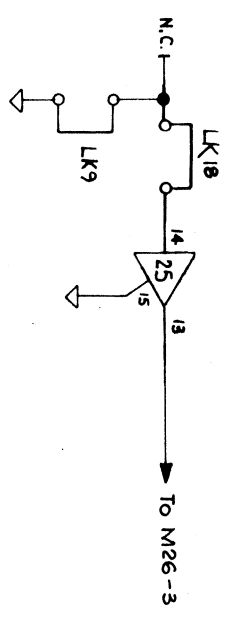
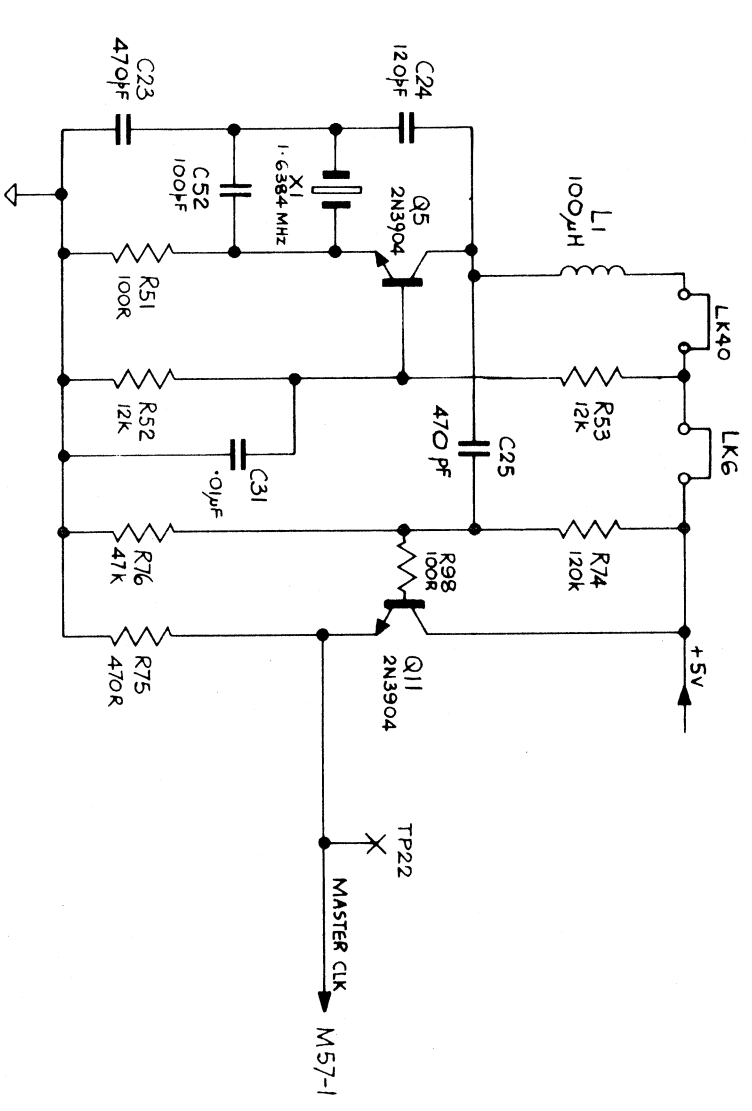
DRAWING No. 430526
FIRST USED ON

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

ALL BURS TO BE REMOVED

NOTES

BS 1
RELEASED 2/15



DRAWN	CHECKED	DIMENSIONS IN	TOLERANCES
L.O.G.	L.O.G.	MILLIMETRES	INCH DIMENSIONS: DECIMAL TO 3 PLACES ± 0.05 DECIMAL TO 2 PLACES ± 0.10 FRACTIONAL ± 1/64
DATE	DATE	SCALE	METRIC DIMENSIONS: DECIMAL TO 2 PLACES ± 0.10mm DECIMAL TO 1 PLACE ± 0.20mm WHOLE DIMENSIONS UNLESS OTHERWISE STATED
28.1.83	31-3-83	NOT TO BE SCALED	ANGULAR ± 0.5°

MATERIAL	FINISH

datron ELECTRONICS LTD. NORWICH.
TITLE 1081 1.6 MHz CLOCK CIRCUIT

DRAWING No. 430526
DRAWING SIZE **A2**
SHEET 4 OF 5

DIGITAL 4 clock

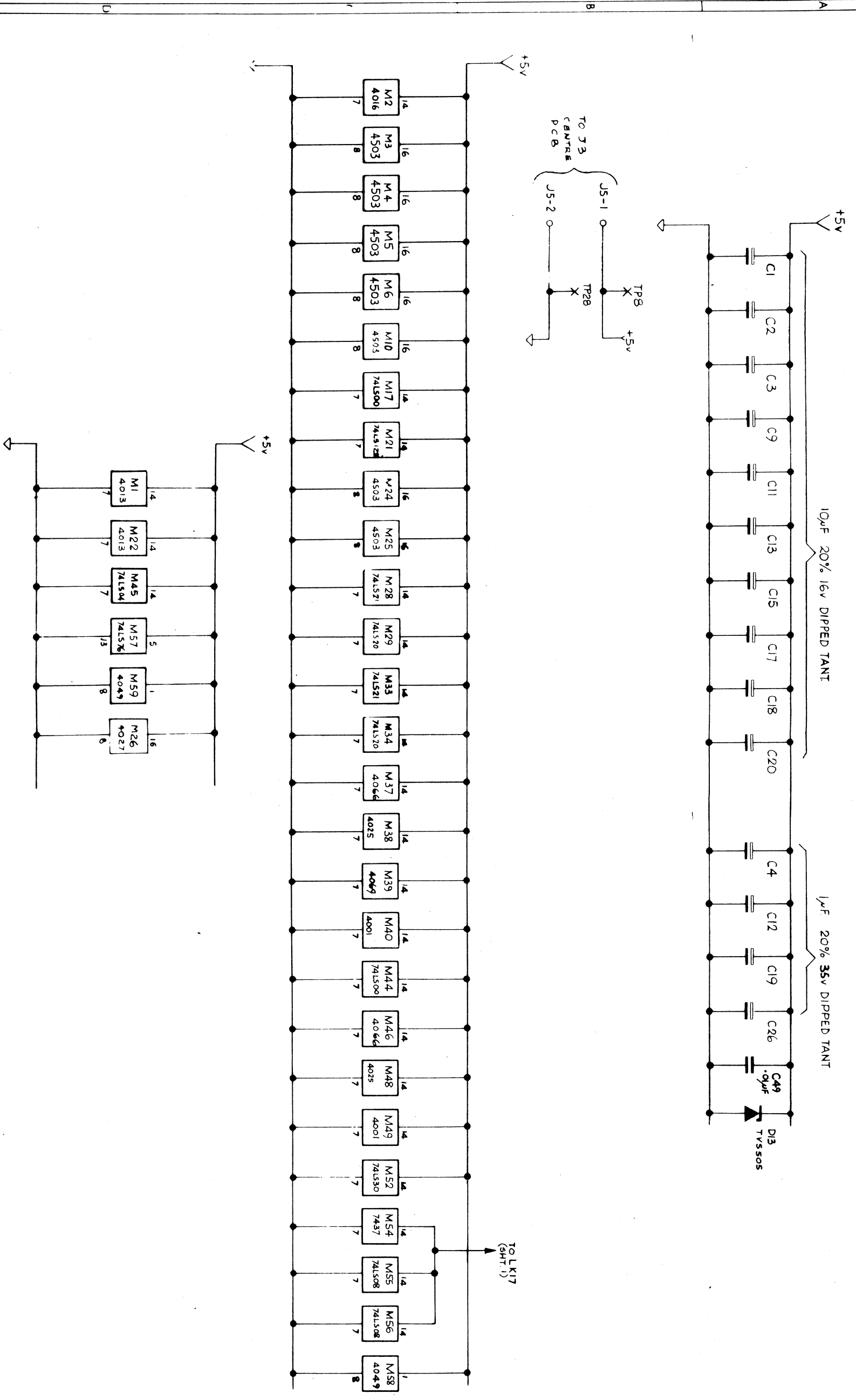
DRAWING No. 430526
FIRST USED ON

THIRD ANGLE PROJECTION
DRAWN IN ACCORDANCE WITH BS 308

ALL SURFS TO BE REMOVED

NOTES

ISS 1
RELEASED 3.5.88



DRAWN	CHECKED	DIMENSIONS IN	TOLERANCES
TRACED	L.O.G.	MILLIMETRES	INCH DIMENSIONS
DATE	APPROVED	SCALE	DECIMAL TO 3 PLACES +
28.1.83	R.W.F.	NOT TO BE SCALED	FRACTIONAL
	DATE		ANGULAR + °
	31-3-83		005
			010
			1/64
			1mm
			2mm
			4mm
			UNLESS OTHERWISE STATED

MATERIAL	FINISH

datron ELECTRONICS LTD. NORWICH.
1081 DIGITAL PCB ASSY.

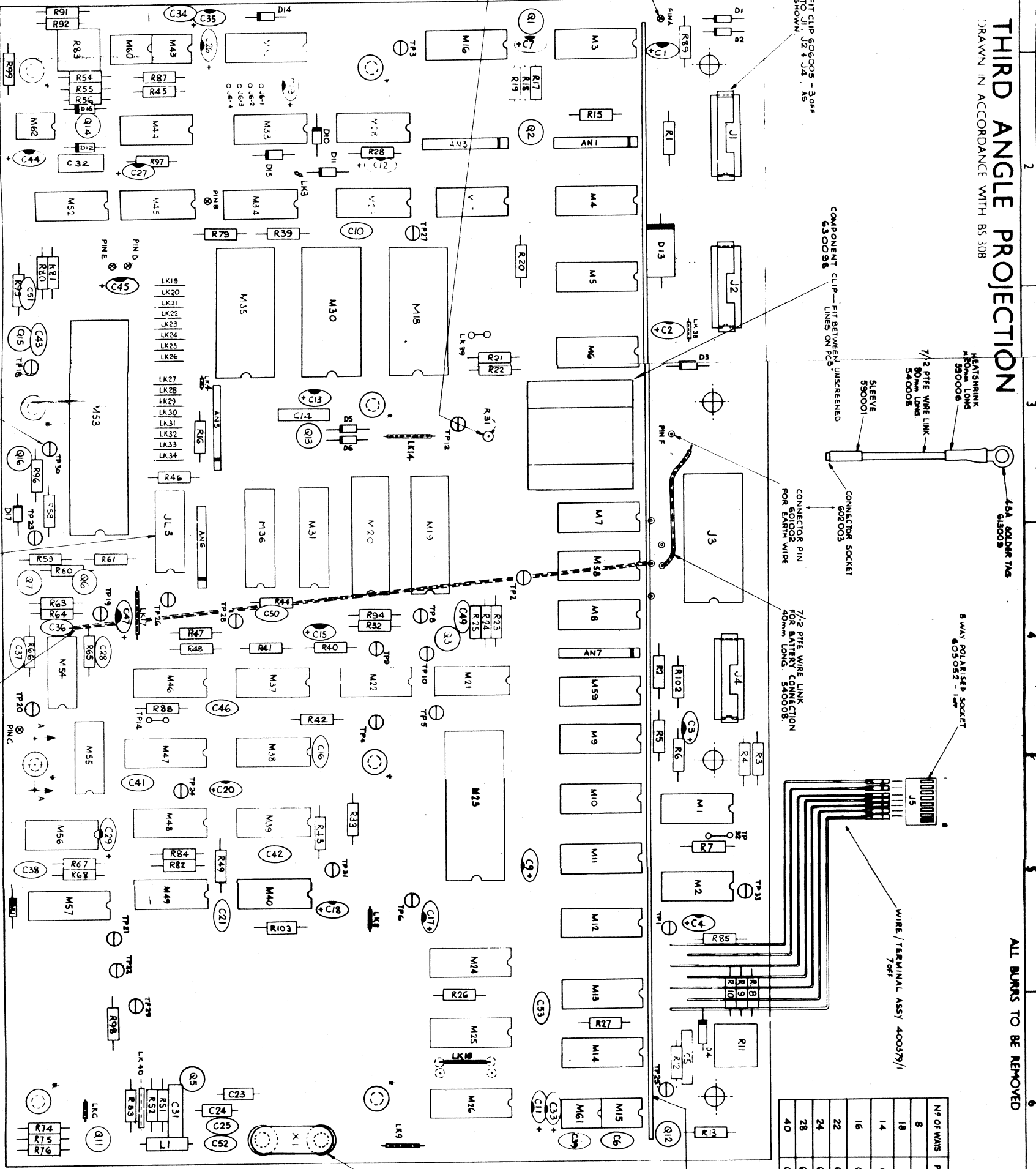
DRAWING No. 430526
DRAWING SIZE A2
SHEET 5 OF 5

DIGITAL 5 POWER DIS.

400526

THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308



ALL BURNS TO BE REMOVED

NOTES

- 1 MAKE TP14-TP28 FROM 22 SWG B7C WIRE - PART # 540002
- 2 LINKS (LX) MADE FROM 22 SWG B7C WIRE (540002) AND SLEEVED (EXCEPT FOR LK19) 540004

No OF WMS	PART NO	No OFF	USE TO MOUNT
8	605059	1	M62
18	605062	2	M31, 36
14	605060	22	M1, 2, 17, 21, 22, 23, 29, 33, 34, 37-40, 44-46, 48, 49, 52, 54, 55, 56
16	605061	24	M3-14, 16, 24-27, 32, 43/40, 47, 57, 58, 15/61, 59
22	605063	2	M19, 20
24	605064	3	M18, 30, 35
28	605065	1	M23
40	605070	1	M33

ISS	CHANGES
1	RELEASED 31.3.83
2	FCG 1479:1487:1488 B.T. 18.5.83
3	EARTH WIRE ADDED. LINK (ONE COM. LOW IMPEDANCE) BETWEEN BUS STRIP & CASE (M62)
4	EQD 1803 1.4.83 WIRE ISSUE 20.6.83

TEST POINT TERMINAL	TEST POINT TERMINAL
620007 24 OFF	620007 24 OFF

LOG	APPROVED	DATE
R.W.F.		13/12/82

datron ELECTRONICS LTD. NORWICH.

1081 DIGITAL PCB ASSY

DRAWING No. 400526

DRIVING SIZE A1

DIGITAL PCB