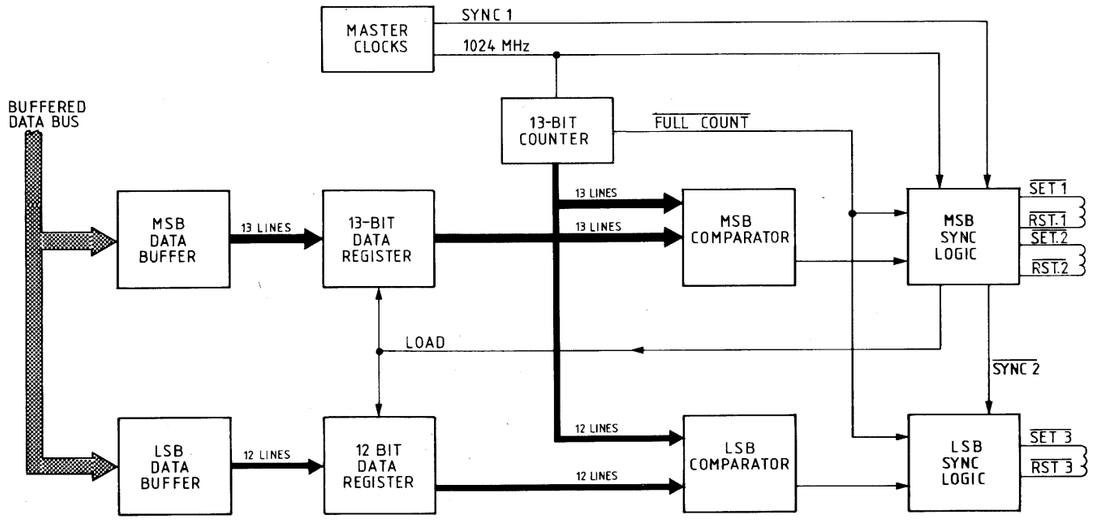


FIG. 4.22 PRECISION DIVIDER OUT-GUARD CIRCUITRY – SIMPLIFIED BLOCK DIAGRAM

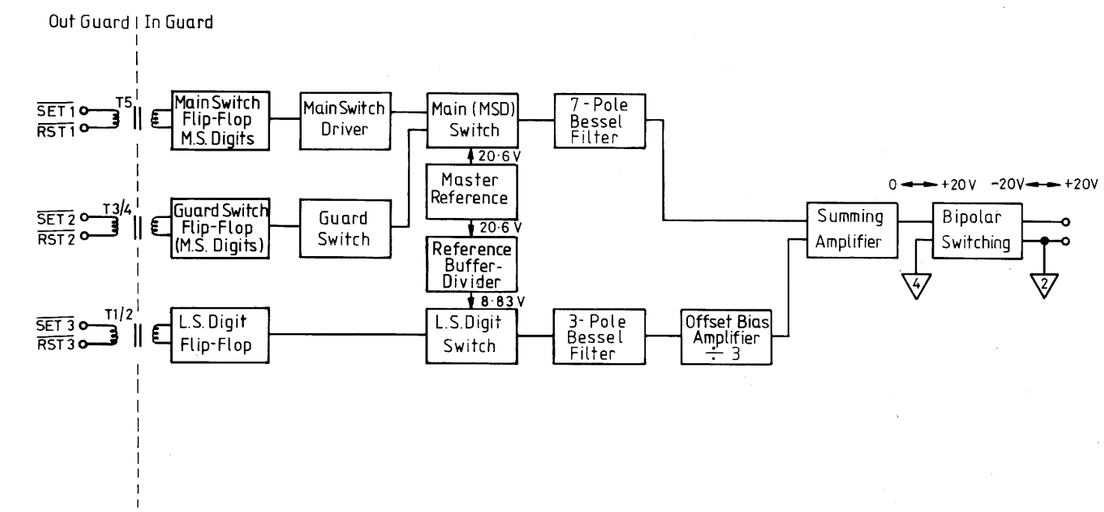


FIG. 4.23 PRECISION DIVIDER IN-GUARD CIRCUITRY – SIMPLIFIED BLOCK DIAGRAM

4.6 PRECISION DIVIDER

The out-guard circuitry described in this section performs the following functions:

(1) Receives the demanded output value from the CPU in the form of a 25-bit data word.

(2) Generates a continuous 13-bit count from the 1.024 MHz Master clock (cycling frequency 125 Hz)

(3) Compares the 13-bit count with the 13 most-significant bits of the 25-bit word, generating "Set" and "Reset" pulses, which are transferred into guard to trigger the Reference Divider Main and Guard JFET switches

(4) Compares the 12 most-significant bits of the count with the 12 least-significant bits of the 25-bit word, generating "Set" and "Reset" pulses, which are transferred into guard to trigger the Reference Divider "Least-Significant" JFET switch.

The out-guard circuitry is located on the Analogue Interface PCB Assembly.

The in-guard circuitry performs the following functions:

(5) Generates a Master Reference Voltage (20.6V) which is chopped by the Main and Guard JFET switches; to provide a square-wave whose Mark/Period ratio is controlled by the 13 most-significant bits of the 25-bit word. The square-wave is smoothed by a 7-pole Bessel filter to provide a D.C. voltage whose value varies directly as the Mark/Period ratio of the square-wave

(6) Generates a Buffered Reference Voltage (8.83V) which is chopped by the Least-Significant JFET switch; to provide a square-wave whose Mark/Period ratio is controlled by the 12 least-significant bits of the 25-bit word. The square-wave is smoothed by a 3-pole Bessel filter to provide a DC voltage whose value varies directly as the Mark/Period ratio of the square-wave.

(7) Sums the two DC voltages produced by the 7-pole and 3-pole filters, to generate a "Working Reference Voltage" between 0V and +20V; whose value is accurately proportional to the value demanded by the CPU's 25-bit word

(8) Switches the polarity of the Working Reference Voltage to output a reference voltage between -20V and +20V DC. This is used as reference on "DC" and "I" Functions of the instrument.

The in-guard circuitry is located on the Reference Divider PCB Assembly.

4.6.1 Precision Divider Comparators (Circuit Diagram No. 430443)

4.6.1.1 General

The precision divider comparators translate information from the central processing unit into time-related pulses which control the mark/period switching of the reference divider. Two comparators are used; one to translate the 13 most-significant bits of MPU data; the other, the 12 least-significant bits. The comparators perform concurrently, cycling continuously at 125Hz, taking 8mS per full count. During the initial stages of each counting period, the comparators generate SET pulses to start the reference divider mark period. After precisely-measured delay times, reset pulses are generated to terminate the mark period.

4.6.1.2 Comparator Function (Fig. 4.22)

Binary data is entered into the MSB and LSB buffered data latches under the control of the CPU. The contents of the buffered data registers are up-dated to the working data latches at the end of each comparator counting cycle by the LOAD command. This is derived from the 13-bit counter FULL COUNT output, which is also used by the MSB and LSB sync logic circuits to initiate generation of the set pulses $\overline{\text{SET 1}}$, $\overline{\text{SET 2}}$ and $\overline{\text{SET 3}}$.

Translation of the binary data into reset pulses (whose time relationship to the set pulses is established by the demanded output value) is obtained in the MSB and LSB comparators.

4.6.1.3 13-Bit (MSB) Comparator (Circuit Diagram No. 430443 Sheet 2)

The 13 Exclusive-OR elements of the MSB Comparator are scanned in ascending sequence by the outputs of the 13-bit counter. The least-significant bit has a frequency of 512 kHz, and the most-significant a frequency of 125 Hz thus giving a natural division of 8192 time slots of 977 nS over the counting period of 8mS. Each time slot has a unique binary code; when this coincides with the bit-pattern set in the data register, the comparator provides an output pulse to the MSB sync logic. The latter initiates generation of reset pulses $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ and synchronizes them to SYNC 1 (2.048 MHz).

4.6.1.4 12-Bit (LSB) Comparator (Circuit Diagram 430443 Sheet 1)

This functions in the same manner as the MSB comparator but with 12 bits over the same 8mS counting period. This accommodates 4096 time slots and gives a 1954 nS period for each binary increment. Synchronizing of the $\overline{\text{RST3}}$ output from the LSB sync logic is performed by SYNC 2 pulses which are half the rate of the SYNC 1 pulses.

4.6.2 Comparator Circuit Action

4.6.2.1 Input Data Latches (Circuit Diagram No. 430443 Sheets 1 and 2)

The input buffered data latches M31 to M34 and M37 to M39 receive 27 data bits in four bytes from the buffered data bus. Latches are selected by signals REF DIV 1, 2, 3 or 4 from the memory address decoding on the digital pcb. Data is clocked to the "Q" outputs of the latches on the positive-going edge of WRT STRB.

Data from the input latches is used as follows:

25 bits form a data word to the comparator registers M47, M48, M49 (part), M51 and M52. One bit triggers monostable M29 (part), the Q output of which is inverted and buffered to provide the control UPD (OG) used in the relay drive logic for analogue switching. One bit, EXT FREQ ÷ 10, is not used in the 4000.

4.6.2.2 13-Bit Counter (Circuit Diagram No. 430443 Sheet 2) (refer to Fig. 4.24 for Waveforms)

The counter comprises three 4-bit binary counters M15, M16, M17 and J-K flip flop M42 (half dual package). The outputs required from the counter are 13 binary-coded lines, the first (least significant) being a 512 kHz squarewave, the others successively divided in frequency to the most significant output of 125 Hz.

Bit 1 is provided by J-K flip flop M42, which toggles on each falling edge of the 1.024 MHz clock to give 512 kHz Q and $\overline{Q}$ outputs. These outputs are used as follows:

(1) Q and $\overline{Q}$ complementary outputs together provide the least-significant input to the 13-bit comparator;

(2) The Q output controls the counting rate of M15, synchronizes M16 and M17, and is used in the gating of FULL COUNT.

Counters M15, M16 and M17 are cascaded as a 12-bit counter and synchronously clocked by the 1.024 MHz. M15 counting is enabled only when M42 Q output is logic-1 at the count-enable input M15-7. As M42 output is at 512 kHz, clocking of M15 occurs on the rising edge of alternate 1.024 MHz clocks, thus giving outputs of 256, 128, 64 and 32 kHz squarewaves from M15. Counter M16 is enabled by the carry output from M15 together with 512 kHz from M42 at the count-enable pins M16-10 and 7 respectively, thus giving outputs of 16, 8, 4 and 2 kHz squarewaves from M16. Counter M17 functions in a similar manner to give outputs of 1 kHz, 500, 250 and 125 Hz squarewaves.

The 2μS-long carry output from M17 occurs at the end of the 125 Hz output when all counter outputs are at logic-1. The carry output is NAND gated with M42 Q output to give the 1μS-long logic command FULL COUNT. The counting cycle continues, starting from bit 1.

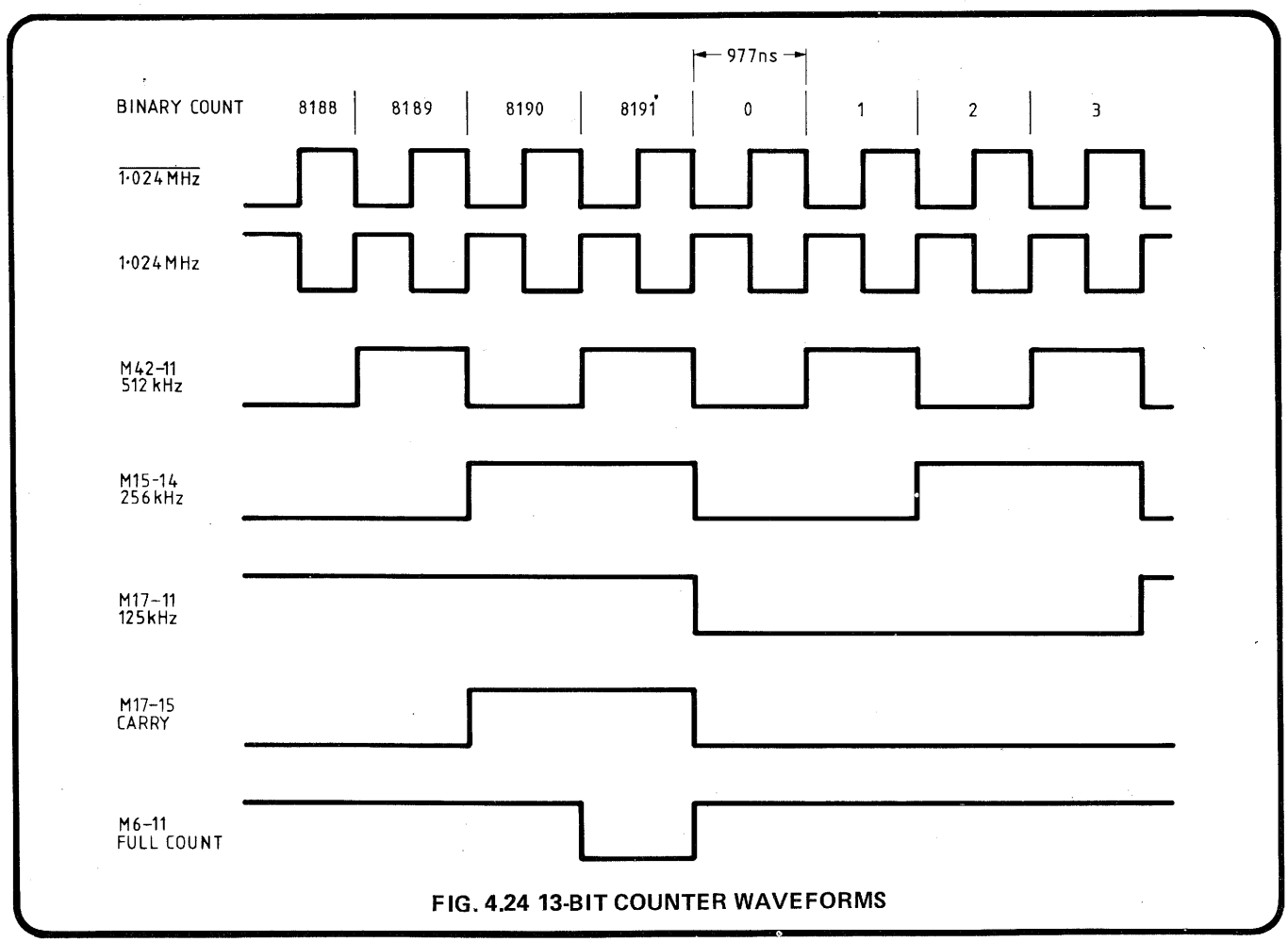


FIG. 4.24 13-BIT COUNTER WAVEFORMS

4.6.2.3 13-Bit Comparator Action (Circuit Diagram No. 430443 Sheet 2)

The 13-bit comparator provides a logic-1 output at TP12 whenever a coincidence occurs between the following two sets of data:

(1) Data set in registers M47, M48 and M49-1;

(2) Data from the 13-bit counter M42, M15, M16 and M17.

Twelve exclusive-OR elements M25, M26, M27 and three NOR gates of M12 are used to detect a coincidence. The data in the registers is preset by the CPU, while that presented by the 13-bit counter cycles through every binary combination possible on 13 lines. Two coincident inputs to an exclusive-OR gate provide a logic-0 to the 12-input NOR gates M24/M23; full coincidence in bits 2 to 13 is shown by a logic-0 at NAND M13-6. Coincidence at bit 1 is shown by logic-0 at M12-13 and M12-4 as follows:

M12 INPUT PINS			M12 OUTPUT PINS		
6	11	9/12	4	13	
0	1	0	0	0	only 4 input combinations available
0	1	1	1	0	
1	0	0	0	1	
1	0	1	0	0	

A $\overline{\text{BUSY}}$ signal is generated by the comparator at NAND M50-13 (TP2) when the 13-bit counter approaches full count. Bits 8 to 13 are at logic-1 for the period of 125μS preceding the end of the counter cycle (see Fig. 4.25). The $\overline{\text{BUSY}}$ level is applied to the D input at M49-9 and is clocked through as $\overline{\text{REF BUSY}}$ to buffer M45.2 by 1.024 MHz. When the CPU has data to load into the input data latches, it first interrogates the comparator by enabling buffers M45 through $\overline{\text{REV DIV RD}}$. A logic-1 on $\overline{\text{REF BUSY}}$ at M45-3 indicates to the CPU that sufficient time is available for the latch-loading process to take place (at least 125μS before LOAD pulse). The remaining elements of M45 buffer the five most significant data bits back to the CPU so that data parity can be confirmed.

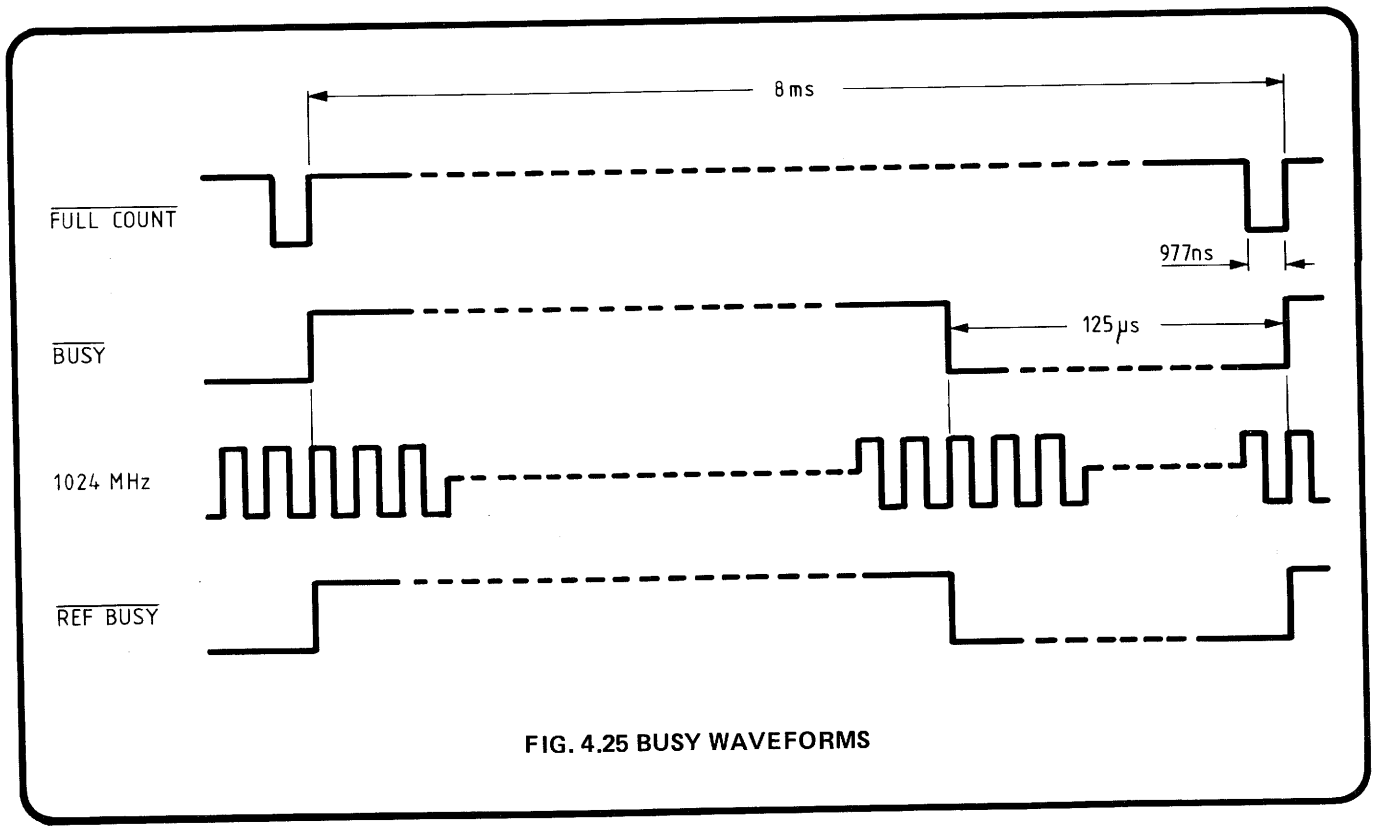


FIG. 4.25 BUSY WAVEFORMS

4.6.2.4 MSB Sync Logic (Circuit Diagram No. 430443 Sheet 2) (refer to Fig. 4.26 for waveforms)

This circuit, M14, M6, M7 and M8, provides the following signals: SYNC 2, LOAD, SET 1, SET 2, RST 1 and RST 2.

SYNC 2 is obtained by NAND gating 1.024 MHz and SYNC 1 to give a synchronizing pulse at half the rate of SYNC 1. (See Fig. 4.26)

The LOAD pulse, which enables the 13-bit counter registers, is generated at M14-6 towards the end of the counter's full-count output. FULL COUNT sets the D input M14-2 and the level is clocked, inverted, from M14-6 by the next two SYNC 2 pulses that occur.

The inverse of LOAD is used to time the pulse SET 1 by NOR gating at M7-4 with 1.024 MHz. The pulse at M7-4 is then NAND gated with SYNC 1 to provide SET 1 from M8-1. The pulse SET 2, which occurs 977 nS before SET 1, is obtained by gating FULL COUNT with 1.024 MHz at NOR M7-10 and then NAND gating at M8-10 with SYNC 1.

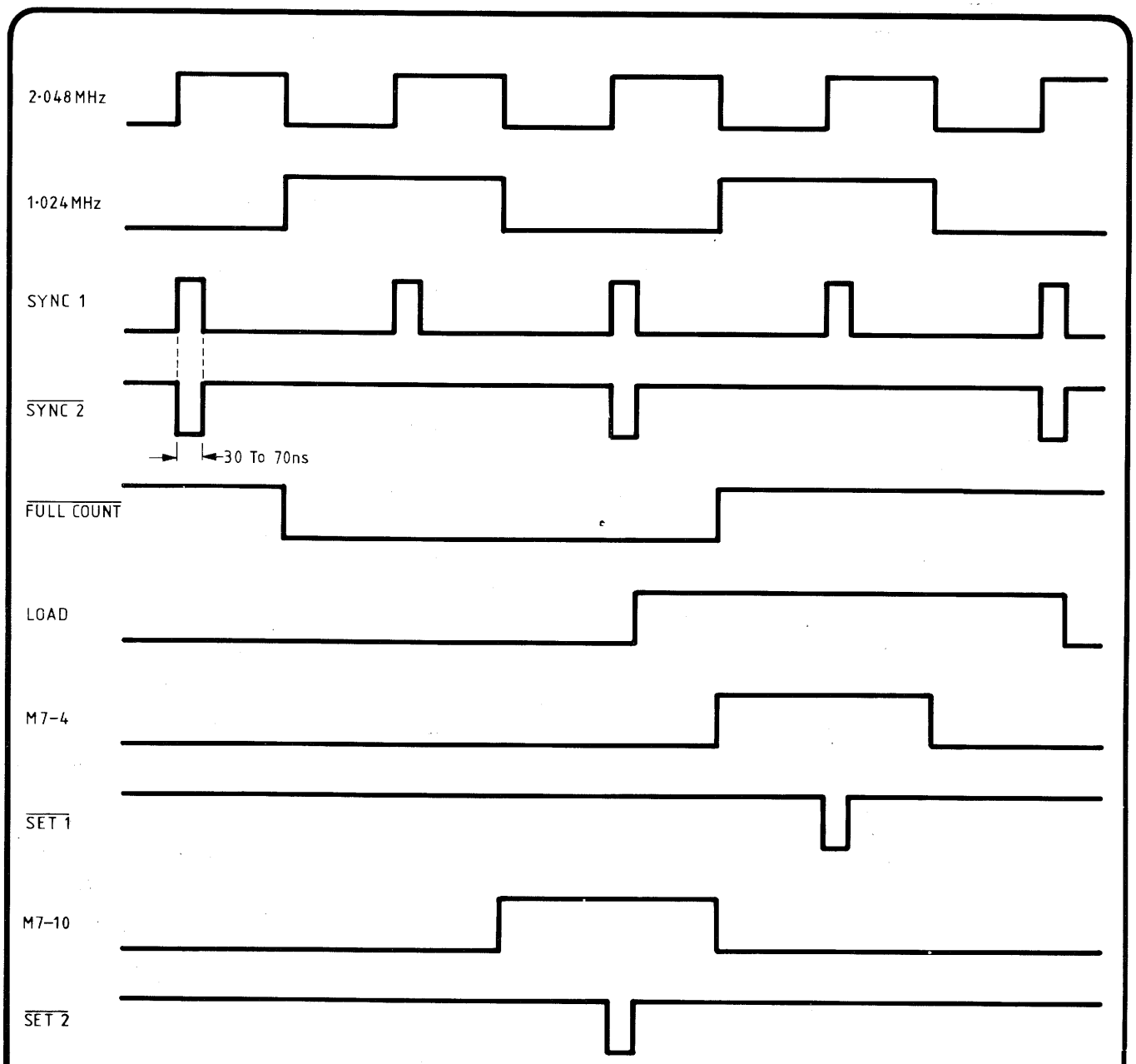


FIG. 4.26 MSB SYNC LOGIC WAVEFORMS

Reset pulse generation (see Fig. 4.27) is indicated by a logic-1 level at TP12. This can occur at any one of the 8192 binary counts of the 13-bit counter, the actual time slot in which it appears depends on the binary count at which the coincidence occurs.

The coincidence level at TP12 is NAND gated at M6-8; M6-10 being at logic-1 for all binary counts except 8191. The logic-0 at M6-8 is NOR-gated at M7-1 with 1.024 MHz, this is then used to select the next SYNC 1 pulse via NAND M8-4 to provide the pulse $\overline{\text{RST 1}}$.

The coincidence level at TP12 is used to set the D input at flip flop M14-12. This level is clocked to NAND M6-5 by the next $\overline{\text{SYNC 2}}$ pulse. NAND input M6-4 is at logic-1 except when LOAD is active, thus M14-9 output is inserted at M6-6 to be NOR-gated with 1.024 MHz at M7-13. This is then used to select the next SYNC 1 pulse via NAND M8-10 to provide the pulse $\overline{\text{RST 2}}$.

The pulse-timing example given in Fig. 4.27 shows the generation of $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ when coincidence occurs in the comparator at binary count = 0 (waveforms in unbroken lines). Coincidence occuring at binary count 1 causes $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ to increment in time by 977 nS with respect to the $\overline{\text{SET 1}}$ and $\overline{\text{SET 2}}$ pulses (waveforms in broken lines). $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ will be generated with the same relationship in time to the comparator coincidence when the latter occurs in any binary count time slot from 0 to 8190 (inclusive); note that $\overline{\text{SET 1}}$ and $\overline{\text{SET 2}}$ remain staionary with respect to $\overline{\text{FULL COUNT}}$ and LOAD and that $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ increment, in time, away from these.

$\overline{\text{RST1}}$ and $\overline{\text{RST 2}}$ are inhibited when coincidence occurs at binary count 8191 to allow for the re-loading of the input registers at the end of the counter cycle. The inhibit is performed by the $\overline{\text{FULL COUNT}}$ level going to logic-0 at NAND M6-10 which prevents $\overline{\text{RST 1}}$ being generated, and by flip flop M14-5 output going to logic-0 for the period of the load pulse which inhibits $\overline{\text{RST 2}}$.

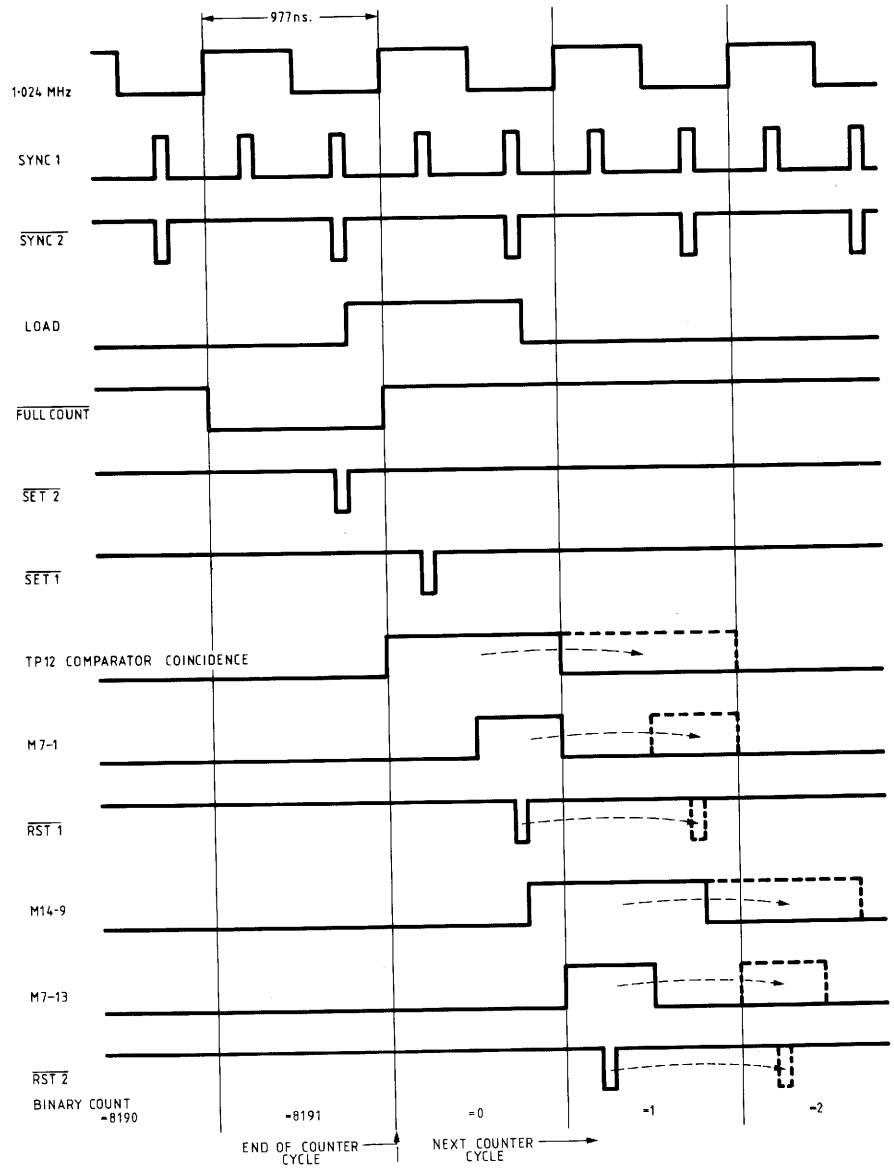


FIG. 4.27 MSB SET/RESET PULSE GENERATION

4.6.2.5 12-Bit Comparator Action (Circuit Diagram No. 430443 Sheet 1)

This functions in an identical manner to the 13-bit comparator previously described. Twelve exclusive OR gates, M19, M20 and M21, receive 12-bit binary output from the common counter and compare these bits with the data in the data registers. The least significant bit changes at a rate of 256 kHz, and the most significant bit at 125 Hz. Coincidence occurring in any of the 4096 binary count time slots available in the comparator cycle is shown as a logic-0 at TP5 for a period of 1954 nS.

4.6.2.6 LSB Sync Logic (Circuit Diagram 430443 Sheet 1) (refer to Fig. 4.28 for waveforms)

The timing of $\overline{\text{SET 3}}$ is controlled by the $\overline{\text{FULL COUNT}}$ pulse from the 13-bit counter. The inverted $\overline{\text{FULL COUNT}}$ at M43-6 is gated with the inverted $\overline{\text{SYNC 2}}$ from M43-11 to give, at M46-1, $\overline{\text{SET 3}}$. The comparator coincidence logic level is inverted to logic-0 at M12-1; M12-2 being at logic-0 except when $\overline{\text{FULL COUNT}}$ is low. The waveform at M12-1 is of 1954nS duration and therefore allows two consecutive $\overline{\text{SYNC 2}}$ pulses to be gated to M46-4 ($\overline{\text{RST 3}}$). This condition exists for all $\overline{\text{RST 3}}$ timings except at the binary count of 4095; in this instance, the $\overline{\text{FULL COUNT}}$ pulse occurs after the gating of the first $\overline{\text{SYNC 2}}$ pulse, sets M12-2 to logic-1 and so prevents the second pulse appearing at $\overline{\text{RST 3}}$. In practice, the second pulse of $\overline{\text{RST 3}}$ has no operational significance.

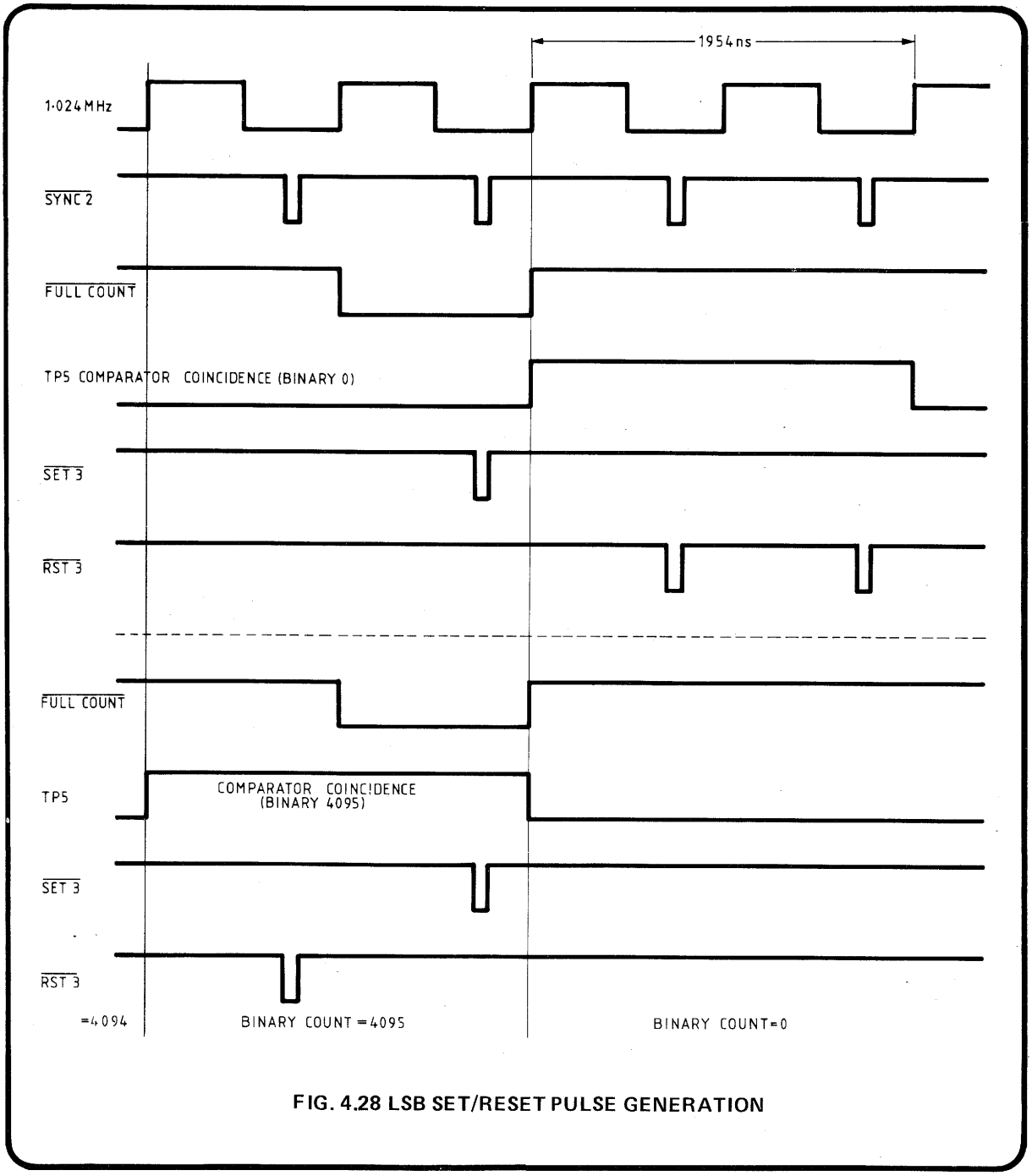


FIG. 4.28 LSB SET/RESET PULSE GENERATION

4.6.3 References and Reference Divider (Circuit Diagram No. 430444 and Fig. 4.23)

The set and reset pulses from the prevision divider comparators control the timing of FET-switches which chop Master Reference voltages. The chopped references are filtered to generate voltages whose level is proportional to the mark:period ratio (duty cycle). MSD and LSD voltages are added in the summation amplifier to generate a variable 0 ↔ 20V at high resolution (0.03ppm, ≙ 0.5μV increments).

Bipolar switching inverts the working reference for negative output selections.

4.6.4 Master Reference (Circuit Diagram No. 430452 and Fig. 4.29)

The Master Reference determines the fundamental long and short-term stability of the 4000. It is a separate pcb mounted on the Reference Divider assembly (Refer to Layout Drawings Nos. 400444 and 400452).

The basic circuit shown in Fig. 4.29 acts as a constant-current generator for a zener reference.

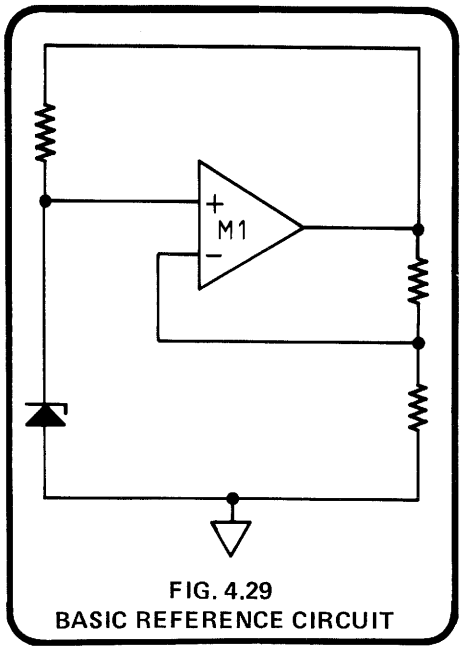


FIG. 4.29
BASIC REFERENCE CIRCUIT

The random character of zener drift in the short-to-medium term may in the long term be regarded as averaging to zero. The averaging action of the eight zener diodes in Drawing 430452 reduces the short and medium term variations (due to drift and noise) by a factor of $\sqrt{8}$, effectively 3 times more stable than a single zener diode.

The diodes and resistors are selected and matched for near-zero temperature coefficient; the overall instrument values are shown together with the stability and accuracy specifications in Section 6 of the User's Handbook.

Test links TLA1-6 and TLB1-5 are selectively removed during manufacture as a fine adjustment of zener operating current for zero temperature coefficient. The zener voltages of +24.5V at TP3 and TP1 wrt common-R1 are reduced by the star-point buffer M2 to approximately +20.6V at the Main Switch in the Reference Divider. This voltage is delivered to the Reference Divider by a full 4-wire sensed connection.

4.6.4.1 Buffer M2 — Temperature Compensation (Circuit Diagram 430452 Sheet 1)

In the 4000A instrument, the temperature compensation applied to M2 is adjusted at manufacture by R29 (set TC slope). This adjustment requires specialised test equipment and should not be attempted by users.

If a fault is suspected on the Reference PCB Assembly (400452), contact your Datron Service Centre.

4.6.5 Reference Buffer-Divider (Circuit Diagram No. 430444 Sheet 2)

R80/81 drop the 20.6V Master Reference voltage (V_{Ref}) to +8.83V. M23/Q40 is a voltage-follower providing +8.83V wrt common-4 at the star-point TP14 to supply the least-significant digit switch.

4.6.6 Least-Significant-Digits Switching (Fig. 4.30)

4.6.6.1 Switch Driver

$\overline{SET\ 3}$ and $\overline{RST\ 3}$ pulses from the LSD Comparator in the Analogue Interface Assembly are transferred into guard via pulse transformers T1 and T2, whose centre-tapped secondaries are balanced about 0V (T1) and +9V (T2). Q5-Q7 form a fast bistable using emitter-coupled logic, to switch TP1 between +9V (mark) and +20V (space). During the "Mark" time after $\overline{SET\ 3}$ pulse, Q29 and Q30 are switched ON, connecting LKA to +9V Ref. During the "Space" time after $\overline{RST\ 3}$ pulse, Q29 and Q30 disconnect LKA from +9V Ref. Q1 — Q4 have the same fast bistable action, Switching Q31 off during the "Mark" period by −11V at TP2, disconnecting LKA from common-4 (0V); and on during the "Space" period, connecting LKA to common-4 (0V). Fig. 4.30 demonstrates this action.

4.6.6.2 FET Switch and 3-pole Filter

The combined action of the switch FETs alternately provides charging current for the 3-pole filter (during "mark") and discharging current (during "space"). Two FETs in parallel (Q29 and Q30) are necessary to equalise the charging and discharging time constants by matching the "ON" resistances. This preserves linearity of the filter output voltage over the full range of mark/period ratios applied via the set and reset pulses.

The 3-pole filter has the advantage of not being in series with the DC output signal. The 125Hz ripple content is reduced to an acceptable level for the overall instrument specification. The filter output is buffered by voltage-follower M16.

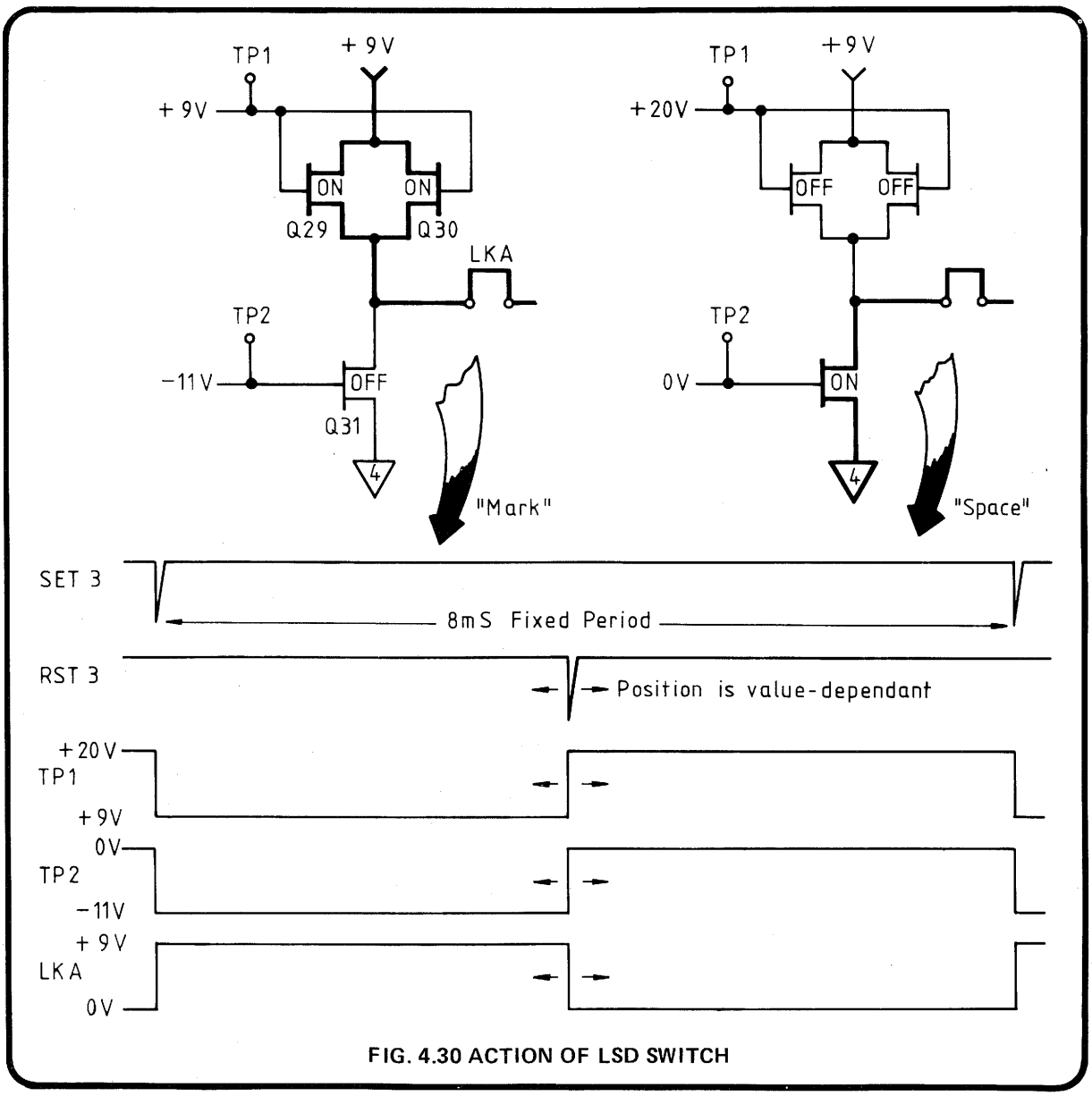


FIG. 4.30 ACTION OF LSD SWITCH

4.6.6.3 Offset Bias Amplifier

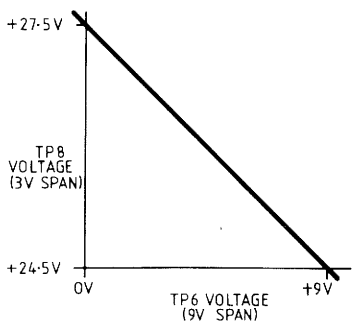
M20 performs a dual role:

(1) Its gain is set to $-\frac{1}{3}$ by R64/65

(2) Its output is level-shifted to provide an offset bias for the summing amplifier (This allows the summing amplifier output to have a negative zero offset).

Also a small thermal coefficient zero correction is factory-preset (D10/R85).

M20 transfer function is approximately as follows:



The actual values are as set digitally in software, affecting the mark:period ratio of the FET switches, using stored calibration constants.

4.6.7 Most-Significant-Digits Switching (Circuit Diagram No. 430444 Sheet 1)

The large reference voltage (20.6V) and the need for higher resolution makes the MSD Switching circuitry more complex than for LSD; but the principle is the same: the set and reset pulse-timing adjusts the mark:period ratio of the square wave fed to the filter.

The arrangement used for the MSD switching satisfies two essential requirements:

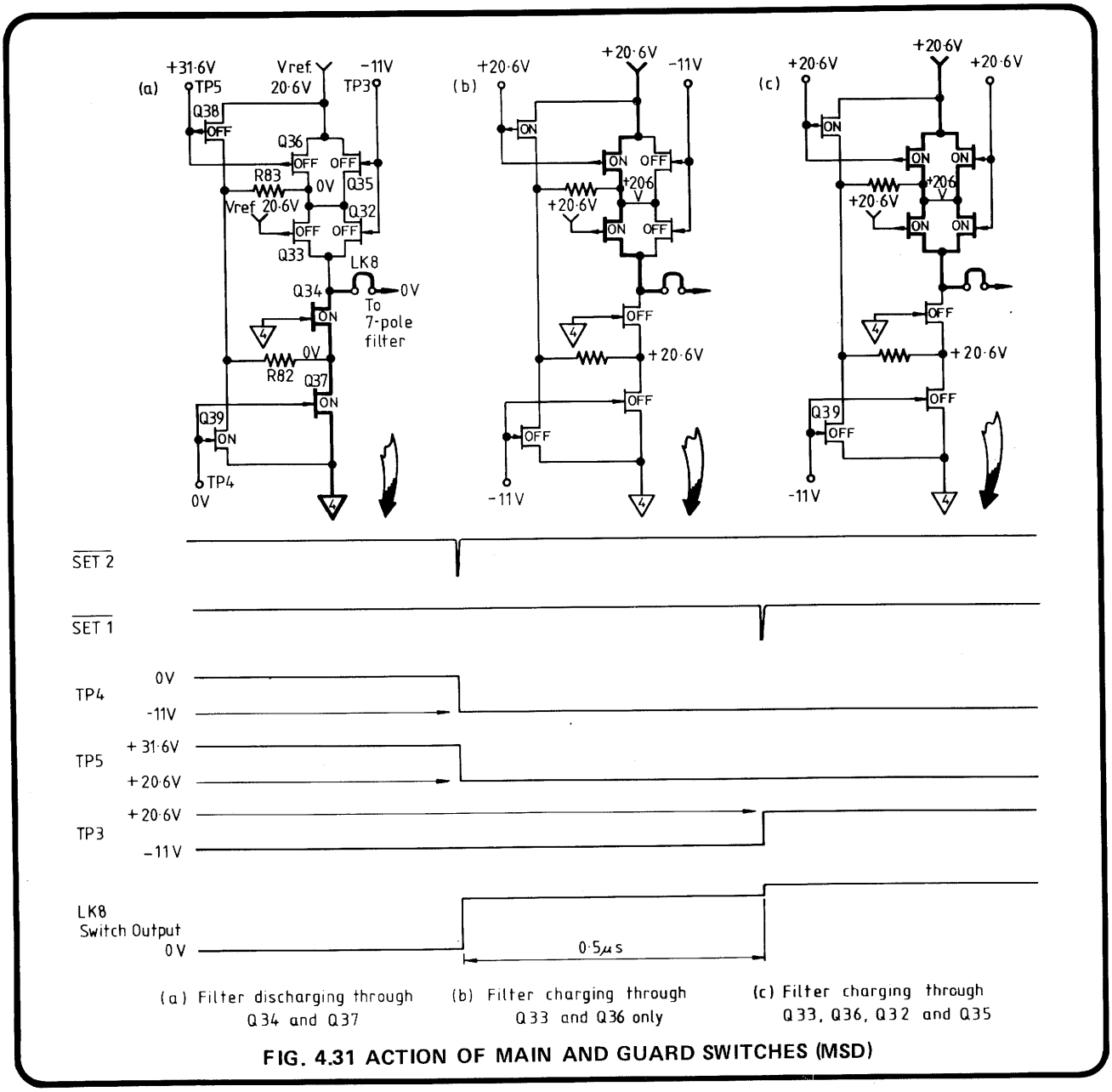
(1) The charge and discharge path resistances for the 7-pole filter must be closely matched.

(2) The leakage current of the path switched off must be minimal.

Requirement (1) demands that the matched devices used in both paths are of the same type (P-channel JFETs have approximately 10 times the "on" resistance of N-channel types). But without the voltage standoff and leakage-current shunt created by the guard switch, the pinch-off gate voltage for one of the paths would be high enough to generate gate-leakage current in excess of requirement (2).

4.6.8 Main and Guard Switches (Fig. 4.31 and Circuit Diagram No. 430444 Sheet 1)

Refer to Fig. 4.31, in which only the Space → Mark state-transfer a-b-c is shown. (The Mark → Space transfer is symmetrical c-b-a). The switch driver flip flops establish the voltage shown at TP3, 4 and 5 as controlled by the set and reset pulses. The drivers are ECL fast bi-stables, but note that Q19 and Q20 are included in the main switch driver as a level-shifter for Q32/Q35.



(a) Filter discharging through Q34 and Q37

(b) Filter charging through Q33 and Q36 only

(c) Filter charging through Q33, Q36, Q32 and Q35

FIG. 4.31 ACTION OF MAIN AND GUARD SWITCHES (MSD)

4.6.8.1 Switch Timing

$\overline{\text{SET 1}}$ pulse is delayed by 0.5μSec after $\overline{\text{SET 2}}$ pulse, and $\overline{\text{RST 2}}$ is delayed by 0.5μSec after $\overline{\text{RST 1}}$.

$\overline{\text{SET 2}}$ and $\overline{\text{RST 2}}$ pulses control the timing of the guard switch Q38 and Q39, and Q36, Q33, Q34 and Q37 in the main switch (TP4 and 5).

$\overline{\text{SET 1}}$ and $\overline{\text{RST 1}}$ pulses turn Q35 and Q32 on and off (TP3). Because of the 0.5μSec delays, Q35 and Q32 conduct only during the time that Q36 and Q33 are also conducting.

4.6.8.2 Filter Discharge Path

In Fig. 4.31(a) the switches are in "space" state. Any leakage current due to the high voltage of Q36/Q35/Q38 gates is shunted via Q39/R83, eliminating Q33/Q32 leakage by zero source-drain voltage. During "space" state the 7-pole filter capacitors have a discharge time constant which includes Q34 and Q37 'On' resistance (3-5 ohms each).

4.6.8.3 Filter Charge Path

To preserve linearity over the full range of Mark: Period ratios, the filter charging path must also have the same time constant, so Q35 and Q32 form a matched set with Q34 and Q37, all N-channel J-FETs (The "on" resistance of P-channel FETs is much higher: 30 – 40 ohms). But to avoid high voltages being developed across Q35/Q32 when changing between states (causing excessive leakage), P-channel FETs Q36/Q33 are switched on before (and switched off after) Q35/Q32.

Fig. 4.31(b) shows this intermediate state after $\overline{\text{SET 2}}$ and before $\overline{\text{SET 1}}$, and Fig. 4.31(c) shows the fully-conducting state after $\overline{\text{SET 1}}$. Note that the second step on LK8 waveform is heavily exaggerated for descriptive purposes, and is not readily viewed on an oscilloscope. The longer charging time-constant during this half-microsecond is not sufficient to disturb the linearity of the filter in excess of specification.

To minimise leakage during "mark" state, Q34 source-drain voltage is maintained at zero by R82 connection. Thus Q34, Q33 and Q32 act as isolators in their "OFF" state, giving rise to the name "Guard Switch" for Q38/39.

4.6.9 7-pole Filter

M26, M28, M32, Q41 and Q42, together with associated capacitors and resistors, form a 7-pole Bessel Function filter in three active elements; providing approximately 135dB of attenuation at the 125Hz switching frequency and increasing at 140dB/decade. This allows sufficient bandwidth to avoid execessive settling time whilst reducing the output ripple to within instrument specification. Q41 and Q42 source-followers provide input bias currents for M26 and M28 from the 15V supplies, and buffer the line from bias-current effects.

The filter output at TP11 is fed to the summing amplifier to be added to the output from the Least-significant digits offset-bias amplifier. R101 and C51 prevent spikes from the chopper-stabilised summing amplifier being fed back into the filter.

4.6.10 Summing Amplifier (Circuit Diagram No. 430444 Sheet 3)

M33, M34 and Q44 sum together the MSD and LSD voltages. M35, D14, D15, Q48 and Q49 provide bootstrapped supplies to preserve full dynamic-range linearity. Q46 and Q47 establish 3mA constant-current drives for D14 and D15, over the range of BS-common voltage variation.

M33 is a high-gain, chopper stabilised integrator with a bandwidth of approx. 10Hz, and Q44 provides additional bandwidth for rejection of HF common-mode noise.

M34/Q45 provide the output and feedback drive, buffering the summed outputs of M33 and Q44. The summing amplifier acts as a voltage-follower to the MSD input, but divides and inverts the LSD input. The LSD gain ratio is set by R100 ÷ R99 = 475 ÷ 555,410 ≙ 8.552×10^{-4}. The span of LSD inputs of approximately 3V (+27.5V at zero LSD filter output to +24.5V at LSD filter output of +9V) leads to a span of approximately 2.5mV subtracted from the MSD voltage at the emitter of Q45.

The reference voltages and reference division circuitry are chosen to allow for software calibration adjustments, so the span of the summing amplifier overlaps the required Full Scale of 0 to 19.999999V at both extremes :

Zero:

At zero count the MSD input voltage is approx. 3.2mV. Zero count on the LSD comparator produces an output at TP6 of approx. 1.1mV, which translates into an output voltage to the summing Amplifier of approx. +27.5V. The combined output at Q45 emitter is found by

$$Vo = V_{msd} - (V_{lsd} - V_{msd}) \times \frac{R100}{R99}$$

$$= 0.0032V - (27.5V - 0.0032V) \times \frac{475}{555410} \triangleq \underline{-20.3mV}$$

This overlap of approx. -20.3mV allows a zero offset to be stored in the digital calibration memory to align the zero output to a defined external zero.

Full Scale:

A full count of 8191 on the MSD Comparator would produce a +20.6V input to the summing amplifier. Similarly a full count of 4095 on the LSD Comparator would produce +8.83V at TP6, and +24.5V at TP8 at the input to the summing amplifier. The combined output is again found by $V_o = V_{msd} - (V_{lso} - V_{msd}) \times \frac{R100}{R99}$

The maximum value is

$$20.6V - (24.5V - 20.6V) \times \frac{475}{555410} \triangleq \underline{+20.597V}$$

This value cannot be achieved in practice as the software modifies all digital demands by a factor of approx 0.97. Use of 20.6V Master Reference and this gain factor gives a margin for accurate calibration, from digital gain factors held in the non-volatile calibration memory.

4.6.11 Bipolar Reference Switching

The polarity-reversal relay RL1 is driven from M31 pin 4, M14 and M29 (Circuit Diagram 430444 Sheet 4). For positive outputs RL1 is energised; and for negative outputs, de-energised.

For positive DC Voltage outputs, common-4 is connected via RL1-8 as DC Ref Lo which is tied to the DC Assembly common-1 and the front panel Lo terminal. The summing amplifier output star-point connects via RL1-5 to become positive DC Ref Hi for the Error Amplifier on the DC Assembly.

For negative DC Voltage outputs. RL1-10 connects the summing amplifier output star-point to Common-1 as DC Ref Lo, and Common-4 becomes negative DC ref Hi via RL1-7.

When option 20 is fitted, RL2 can be energised for current outputs by selection of I function (M19 pin 7 on sheet 4).

In this case the summing amplifier output is used as positive or negative DCI Ref, to drive the voltage-to-current converter on the I/Ω pcb.

4.6.12 Power Supplies

To avoid the effects of common-mode transients on the lines from the in-guard common-4 power supply at the rear of the instrument, the +36V, +18V and −15V supplies entering Reference Divider pcb are heavily filtered. The +18V supply is regulated after filtering to generate +15V supply.

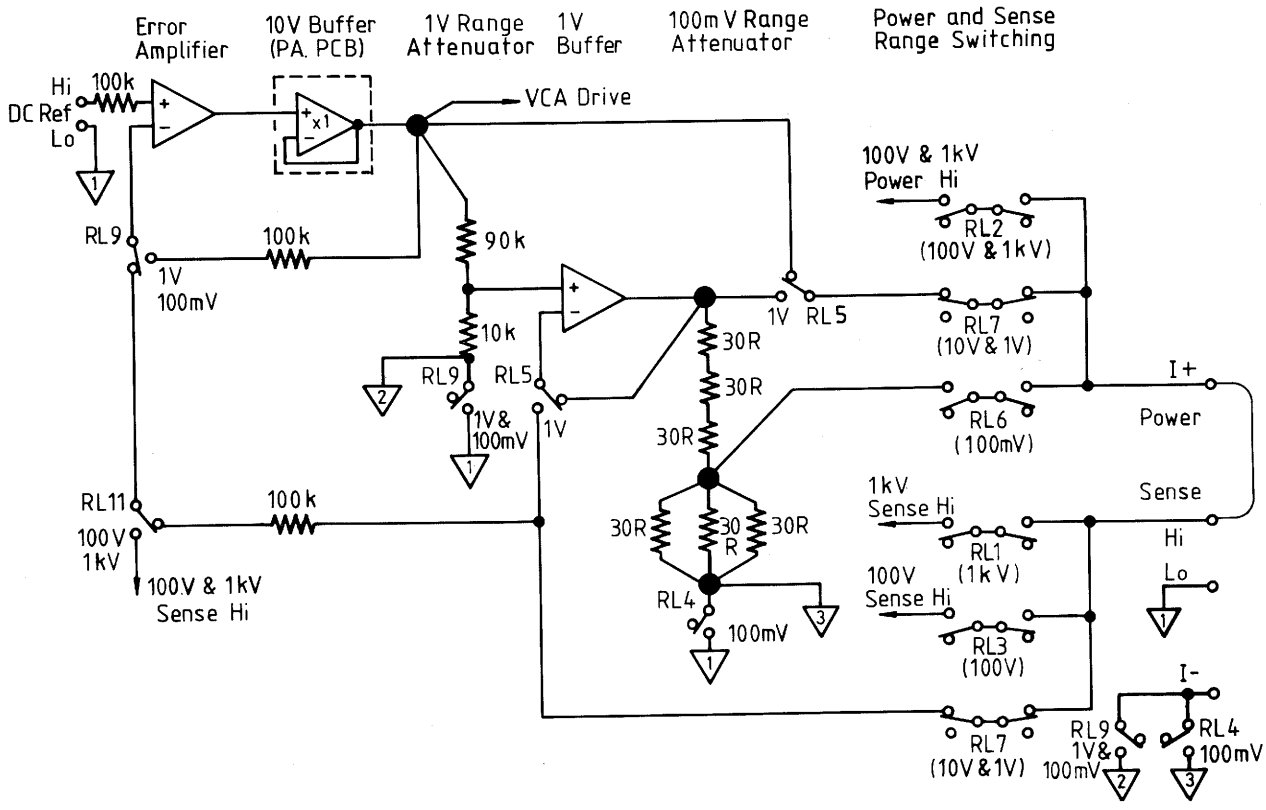


FIG. 4.32 LOW VOLTAGE – SIMPLIFIED FUNCTIONAL DIAGRAM