CALIBRATION AND SERVICING HANDBOOK

4000
4000A

datron
INSTRUMENTS

AUTOCAL STANDARD

CALIBRATION AND SERVICING HANDBOOK

for

THE DATRON 4000 & 4000A
AUTOCAL STANDARD

(for operating procedures
refer to the User's Handbook)

850055 Issue 3 (JAN 1988)

For any assistance contact your nearest Datron Sales and Service Centre.
Addresses can be found at the back of this handbook.

Due to our policy of continuously updating our products, this handbook may contain minor differences in specification, components and circuit design to the instrument actually supplied. Amendment sheets precisely matched to your instrument serial number are available on request.

DANGER
HIGH VOLTAGE

THIS INSTRUMENT IS CAPABLE OF DELIVERING

A LETHAL ELECTRIC SHOCK !

FRONT or REAR terminals carry the Full Output Voltage.

THIS CAN KILL !

Guard terminal is sensitive to over-voltage

It can damage your instrument !

Unless **you** are **sure** that it is **safe** to do so, **DO NOT TOUCH** the **I+ I− Hi** or **Lo leads** and **terminals**

DANGER

CONTENTS

Section	Title	Page

ILLUSTRATIONS

SECTION 1

CALIBRATION

1.1 INTRODUCTION

1.1.1 Manufacturer's Initial Calibration

The 4000 is fully calibrated before leaving the factory, and remains within the appropriate specification for the time periods detailed in Section 6 of the User's Handbook.

1.1.2 Need to Recalibrate

Sections 1.2 to 1.5 detail the procedures necessary to recalibrate instrument functions to known specifications. The occasions for re-calibration are as follows:

(1) PERIODIC ROUTINE AUTOCALIBRATION
The specifications for the 4000 are based on standard intervals of up to 24 hours, 90 days or 1 year from calibration. User's may wish to choose alternative schemes, accounting for:

(a) The accuracy required when in use,

(b) The scheduled calibration intervals normally adopted by the user's organisation, and

(c) The instrument specifications (User's Handbook Section 6)

(2) RE-STANDARDISATION
Occasions may arise when it is necessary to trim the instrument internal Master Reference.

For example, when the 4000 is to be made traceable to a different National Standard, after transportation from one country to another.

The procedure for "STD" autocalibration is detailed in Section 1.2.8 (Refer to Section 1.28 para 3 note C).

(3) BATTERY CHANGE
The Lithium battery which powers the non-volatile calibration memory should be replaced after 5 years (Refer to Section 5.3).

After replacement, a full Pre-calibration (Precal – Section 1.4) followed by a Routine Autocalibration (Section 1.2) is required.

(4) CRITICAL PARTS
Recalibration will be required after replacement of a critical pcb assembly or critical component. These are listed in Table 1.1, indicating the extent of recalibration necessary.

1.1.3 Recalibration Procedures in this Section

Routine Autocalibration (Section 1.2)

The Routine Calibration procedures are sufficient for all normal recalibration purposes, except when "Pre-cal" is called for (Refer to Table 1.1).

Remote Calibration over the IEEE 488 Bus (Section 1.3)

Section 1.3 describes the device-dependent commands necessary for routine calibration of the 4000 over the IEEE 488 bus, as a supplement to Section 5 of the User's Handbook. A guideline example is given, but this needs to be adapted for the bus controller in use.

Pre-calibration Procedures (Section 1.4)

In an initial internal calibration process at manufacture, certain "Pre-cal" parameters are established in a special calibration memory. Under certain conditions (detailed in Table 1.1) these parameters need to be re-established by the "Pre-cal" procedure in Section 1.4, before the Routine Autocalibration of Section 1.2.

Ω Option Internal Adjustment (Section 1.5)

If a standard resistor value has been changed by subjecting to undue stress, it may be possible to recalibrate by internal adjustment. Refer to Section 5.4 for further information.

Table 1.1

PCB Assembly	Components Replaced	Precal (Sect. 1.4)	Routine Autocalibration (Sect. 1.2)
Digital (400442)	Complete Assembly	Full	Full
	Lithium Battery (Sect. 5.3)	Full	Full
	Non-volatile RAM (M10/26/27)	Full	Full
	Non-volatile RAM Supply Commutator components	Full	Full
Reference Divider (400444)	Complete Assembly	Full	Full
	Reference PCB Assembly (400452)	Full	Full
	Any set of main, guard or LSD switch FETs	Full	Full
	Reference Buffer	Full	Full
	Switch Driver Flip Flops or their preselected resistors	Full	Full
	R79	Full	Full
DC (400445)	Complete Assembly	–	DC (All Ranges) only.
	1V attenuator R73/R74	–	DC (1V, 100mV, 10mV, 1mV, 100μV Ranges) only.
	100mV attenuator R69/70/71 72/75/76	–	DC (100mV, 10mV, 1mV, 100μV Ranges) only.
	100V/1000V Attenuator R8/9/25/26/46/47/64/65 88/95/98	–	DC (100V, 1000V Ranges) only
I/Ω (400448)	Complete Assembly (N.B. Internal Adjustment required – refer to Section 5.5)	–	I and Ω (All Ranges) only
	÷ 10 attenuator (R43/44) (I Function)	–	I (All Ranges) only
	Current shunts R8/9/10/79/80 (I Function)	–	I (All Ranges) only
	Standard resistors, associated pre-selected or variable trimmer resistors (Ω Function)	Ω Option internal adjustment (Sect. 1.5)	Ω (Replaced Values) only

Table 1.1 List of Critical pcbs and components

1.2 ROUTINE AUTOCALIBRATION

1.2.1 Introduction

The 4000 possesses excellent short and long term stability. Some users will wish to maintain the highest accuracy by recalibrating at short intervals (e.g. every 24 Hours). In these cases, recalibration of the 4000 becomes a routine task. For this reason, Routine Autocalibration procedures are repeated in section 8 of the User's Handbook. It is emphasised that the 4000 can be used immediately after recalibration.

1.2.2 The 4000 Autocal Feature

Full or part calibration may be carried out for all routine purposes from the front panel. Removal of covers is unnecessary, therefore avoiding thermal disturbance. Calibration corrections are stored in an internal memory which remains energised by a battery even when the instrument power supply is switched off. The life of the battery is estimated at 10 years, and it is normally changed at 5-year intervals. On power-up, the 4000 performs a self-test which includes a check of the contents of the calibration memory.

1.2.3 Equipment Requirements

DC Voltage

– A Standard DC Voltage source of suitable accuracy
Example: Series bank of 10 standard cells and Datron 4904 Standard Cell buffer.

– A Precision Divider:
Example: Datron 4902 High Voltage divider and Datron 4903 DC Switching Unit

– A battery-operated null detector with variable sensitivity, able to withstand 1200V across its input terminals
Example: Keithley Instruments Model 155

Resistance

– a set of standard resistors covering 1Ω to 10MΩ. The 1Ω to 10kΩ should be 4-wire type.

– an accurate resistance bridge, or other ratiometric device for measuring resistance to the required accuracy.

– a Datron 1071 used as a transfer-measurement device.

DC Current

– A DC Voltage source, calibrated to suitable accuracy at approximately 1V and 100mV
Example: The standard voltage source used for DC Voltage, with the Datron 4903 DC Switching Unit.

– The battery-operated null detector used for DC Voltage.

– A set of calibrated current shunts of suitable accuracy.

N.B. To allow the same value to be set on the DC Voltage source for each range, the shunts may be of five decade values. Then the same Null Detector sensitivity can be used on each range.

CAUTION When choosing a set of current shunts ensure that their power dissipation ratings are sufficient to avoid permanent degradation from the self-heating effects of the current being checked. This applies particularly to the 1 Amp shunt.

– alternatively, a dmm of sufficient accuracy may be used to measure the voltage across the set of calibrated current shunts.
Example: Datron 1071 using "compute" mode.

1.2.3.1 Notes on the Use of the Null Detector

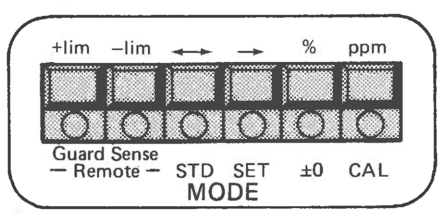
The null detector is connected to the Hi lead between the DC Voltage Source and the 4000. A high-impedance-input device should be chosen to reduce off-null currents due to differences in the outputs of the DC voltage source and the 4000. A battery-operated instrument is preferred to ensure adequate isolation. Some null detectors possess high input impedance only when their readings are on-scale, so care should be taken to ensure that drain currents from the DC Voltage source do not become excessive. This applies particularly if the DC source is a standard cell or a bank of cells. Five points are important:

1. The null detector should be connected to the 4000 (or 4000 load resistor) only when the 4000 OUTPUT OFF LED is lit. (With Output OFF, the I+, I−, Hi and Lo terminals are at high impedance).
2. Always set the null detector to its lowest sensitivity before connecting up, and increase sensitivity only when the voltages output by the DC Voltage source and the 4000 are close in value.
3. Do not change polarity of the 4000 or DC Voltage source without first switching the 4000 OUTPUT OFF. Care must be taken to ensure that the correct-polarity ON key is pressed, to avoid excessive voltages being connected across the null detector, particularly when checking the 4000 directly against a standard cell.
4. **WARNING During Performance checks and calibration a common mode voltage equal to the full range voltage is present at the Null Detector input terminals. On ± 1000V checks this voltage is potentially lethal, so EXTREME CAUTION must be observed when making adjustments to the null detector sensitivity.**
5. **CAUTION** The Null Detector used must be able to withstand voltages up to 1200V between its input terminals. Such voltages will be present during the time that the 4000 is ramping from zero to 1000V Full Range after setting OUTPUT ON. Inadvertent disconnection of the Precision Divider terminals can transfer full output across the Null detector.

1.2.4 Interconnections

Interconnection instructions in this section are necessarily simple and basic, and are mainly intended to show connections to the 4000. It is recognised that they may need to be adapted to meet an individual user's requirements. It is assumed that users will possess knowledge of the operation and use of standards equipment such as that mentioned above.

1.2.5 Calibration Modes



Four of the Mode Keys have 'Autocal' functions:

STD, SET, ±0 and CAL

These are printed in red below the keys and are activated only when the cal legend is present on the MODE display. The normal key modes, (Spec, Error, Offset and Test) are disabled by the selection of CALIBRATION ENABLE on the rear-panel keyswitch. The STD, SET and ±0 keys have toggle action (e,g, when a mode is set it may be deselected by a second key-press).

1.2.5.1 General Procedure

The OUTPUT display is set to the Calibration Standard value, the 4000 output is switched ON, and one of the calibration mode preselector keys (SET, STD or ±0) is pressed. The 4000 output is adjusted to obtain a null at the Calibration Standard value, and the CAL key is pressed to execute the calibration.

1.2.5.2 Autocal Facilities

SET The SET key allows calibration to any value in the selected Range (e.g. at a standard cell voltage). If the value initially set on the OUTPUT display is below 2% of Full Range value, the 4000 assumes that an offset calibration is requested, and if at 2% or above, a gain calibration is assumed.

±0 The ±0 key is used to align the ON+ and ON− zeros of all voltage and current ranges, by a two-part calibration on the 10V range. It is only necessary when the ON+ and ON− zeros on the 10V range do not coincide at the same null.

STD The STD key allows a user to trim the value of the internal Master Reference voltage. The facility can be used to correct for any long-term drift, or to avoid a full recalibration of the 4000 when Laboratory References have been re-standardised. STD calibration effectively changes the gain of all voltage and current ranges in the same ratio, by a simple procedure available either on 1V or 10V range.

CAL only The CAL key executes the preselected AUTOCAL mode. If the CAL key is pressed without first pressing SET, ±0 or STD, the 4000 assumes that a calibration at either Zero or Full Range is required. It uses the value set on the OUTPUT display to distinguish between Zero (Offset calibration) and Full Range (Gain calibration) as for SET mode.

1.2.5.3 Autocal Availability

As the Autocal keys perform specific tasks, they are available only as defined by Table 1.2. The message "Error 3" appears on the MODE display for any attempt to select an inappropriate mode.

AUTOCAL Mode		DC Voltage (DC)	DC Current (I)	Resistance (Ω) Local Sense (2-wire)	Resistance (Ω) Remote Sense (4-wire)
SET and CAL	Zero offset for range at User's selected value	100mV–1000V Ranges only	All Ranges		
	Gain for range at User's standard value				
+0 and CAL	Alignment of internal ON+ and ON− zeros	10V Range only			
STD and CAL	Internal Reference gain at User's Standard value	1V and 10V Range only			
CAL ONLY	Zero offset for range	All Ranges	All Ranges	1Ω–1MΩ Ranges only	
	Gain for range at Full Range Value	10mV–1000V Ranges only			All Ranges

Table 1.2 Autocal availability

1.2.6 Zero Calibration

It is common practice to accept a small offset in the output of a voltage calibration standard, providing that the same offset is present at all output values, including zero.

The output of the 4000 is fully floating, so its output may be referred to any common mode voltage within the range specified on page 6.1 of the User's Handbook. In particular, its zero may be aligned to absolute zero in Local Sense by calibration to a null across its Hi and Lo (Sense) terminals. But if it is then gain-calibrated against an offset standard without re-zeroing to that standard's offset zero, normal mode gain errors will result.

It is therefore essential that each voltage and current range zero is first calibrated to a standard's zero before using that standard to calibrate the range gain.

If the 4000 zero output is to be regarded as absolute Laboratory Reference Zero, then AFTER range gain calibration its range zero output may be recalibrated to a null across the Hi and Lo (Sense) terminals.

1.2.7 Calibration Sequence

The sequence of operations for full calibration of a 4000 Autocal Standard is given below:

Preparation	Section 1.2.7.1
DC Voltage	1.2.8
DC Current	1.2.9
Resistance	1.2.10
Return to Use	1.2.7.2

If only a partial recalibration is to be done, step 1 of the DC Voltage sequence should be carried out immediately after the preparation.

WARNING **During performance checks and calibration a common mode voltage equal to the full range voltage may be present at the Null Detector input terminals. On ±1000V checks this voltage is potentially lethal, so EXTREME CAUTION must be observed when making adjustments to the null detector sensitivity.**

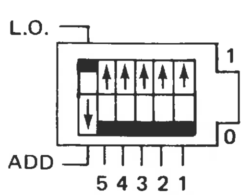
CAUTION The Null Detector used must be able to withstand voltages up to 1200V between its input terminals. Such voltages will be present during the time that the 4000 is ramping from zero to 1000V. Full Range after setting OUTPUT ON. Inadvertent disconnection of the Precision Divider terminals can transfer full output across the Null detector.

1.2.7.1 Preparation

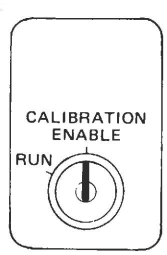
Before any calibration from the front panel is carried out, prepare the 4000 as follows:

1. Turn on the instrument to be checked and allow minimum of 4 hours to warm-up in the specified environment.

2. IEEE 488 Address switch: Set to ADD 11111 as shown (Address 31)



3. CALIBRATION ENABLE key switch: Insert Calibration Key and turn to ENABLE.



These actions activate the four calibration modes (labelled in red) and present the cal legend on the MODE display.

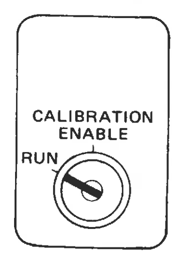
4. Ensure that OUTPUT OFF LED is lit.

1.2.7.2 Return to Use

When any calibration is completed, return the 4000 to use as follows:

1. Ensure that OUTPUT OFF LED is lit.

2. CALIBRATION ENABLE key switch: Turn to RUN and withdraw calibration key.



3. IEEE 488 Address switch: Restore to correct address if the 4000 is to be used in an IEEE 488 system.

DANGER

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I+ I− Hi or **Lo leads**
and **terminals**

DANGER

1.2.8 DC VOLTAGE CALIBRATION

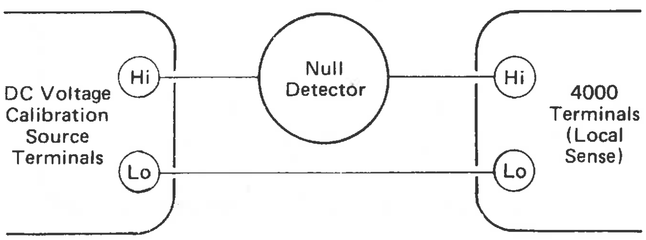
CAUTION First read the Notes on the use of the Null Detector in Section 1.2.3.1.

1. Ensure that the 4000 OUTPUT OFF LED is lit.

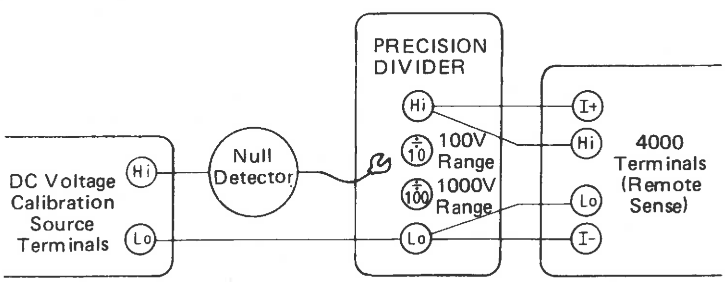
   Select DC and connect the DC Voltage Calibration source and Null Detector to the 4000 terminals as shown in Fig. 1.1. Use short leads and ensure that Null Detector is set to Low Sensitivity.

Fig. 1.1 4000 connections for DC Voltage Calibration

(a) Low Voltage: 100μV – 10V Ranges



(b) High Voltage: 100V and 1000V Ranges



Ensure that the interconnecting circuit has thermally stabilised before carrying out each "Autocal" operation

2. Calibrate the DC Voltage Ranges in the step sequence of Table 1.3 using the Calibration Routine at each step (except steps 2 and 3).

3. **Calibration Routine:** Calibration of DC Voltage to a Standard voltage calibration source.

NOTES: A For calibration at any value, this routine may be used as printed.

B For calibration at zero or positive nominal Full Range only, operation (g) may be omitted.

C To trim internal Master Reference Voltage on 1v or 10V Range, substitute "STD" for "SET" at operation (g). (Refer to earlier description of "STD").

D In Table 1.3(a), use interconnections as Fig. 1.1(a) (Low Voltage), obtaining the correct calibration voltage from the source.

In Table 1.3(b), use interconnections as Fig. 1.1(b) (High Voltage) selecting ÷ 10 at steps 10 and 11, ÷ 100 at steps 12 and 13.

CAUTION Below 2% of Range, the 4000 corrects for an assumed offset error; at 2% of Range and above the correction is for an assumed gain error.

a) Null Detector	Set to Low sensitivity
b) 4000	Ensure OUTPUT OFF
c) DC Source	Set to the required polarity and value
d) 4000	Select correct FUNCTION and RANGE
e) 4000	Use full Range, Zero or OUTPUT ↑/↓ keys to set the required polarity and value on OUTPUT display.

N.B. Operation (f) must be carried out before operation (g)

f) 4000 — Press the correct-polarity ON key

Omit Operation (g) if calibrating at zero or Full Range value

g) 4000	Press SET Key: SET LED lights green OUTPUT display reading also appears on MODE display
h) Null Detector	Increase sensitivity to give an off-null reading and use 4000 OUTPUT ↑/↓ keys to back off to null. Repeat until null lies between two values of the OUTPUT display least-significant digit.
j) Null Detector	Set to LOW sensitivity
k) 4000	Press CAL key CAL LED flashes once Not applicable if operation (g) omitted: MODE display value is transferred to OUTPUT display; MODE display is cleared; SET LED goes OFF

The 4000 is now calibrated at this value.

4. **±0 Alignment Routine:** Alignment of 10V Range positive and negative zeros if necessary at step 3 of Table 1.3.

a) Null Detector	Set to low sensitivity
b) 4000	Ensure OUTPUT OFF on DC 10V Range.
c) Calibration Source	Ensure set to zero and thermally stable.
d) 4000	Press OUTPUT Zero Key Press ON+ Key Press ±0 Key: ±0 LED lights, OUTPUT display at zero
e) Null Detector	Increase sensitivity to give an off-null reading and use 4000 OUTPUT ↑/↓ keys to back off to null. Repeat until null lies between two values of the OUTPUT display least-significant digit.
f) 4000	Press CAL key: CAL LED lights No change to OUTPUT display.
g) 4000	Press ON – key
h) Null Detector	Obtain accurate null as in (e) above
j) 4000	Press CAL key: CAL LED goes OFF ±0 LED goes OFF OUTPUT display falls to zero

The 4000 positive and negative zeros are now both aligned to the Calibration Source zero.

Table 1.3 DC Voltage Calibration

(a) Low Voltage – connect as Fig. 1.1(a)

Step	Calibration Operation	4000 Range	Calibration Source Voltage (Nominal value)[1]	4000 Output Setting (Nominal value)[1]	AUTOCAL Key Used[2]
1	10V Range ON+ zero	10	0.000000V	(ON+) 0.000000V	–
2	10V Range ON– zero check only – do not calibrate	10	0.000000V	(ON–) 0.000000V	Check only 0.000000V
3	±0 Alignment	10	0.000000V	Refer to ±0 Alignment Routine	'±0'
4	100mV Range zero	100m	0.00000mV	0.00000mV	–
5	100mV Range gain	100m	+100.00000mV	(ON+) 100.00000mV	'SET' for non-nominal
6	1V Range zero	1	.0000000V	(ON+) .0000000V	–
7[3]	1V Range Gain	1	+1.0000000V	(ON+) 1.0000000V	'SET' for non-nominal → CAL
8	10V Range zero	10	0.000000V	(ON+) 0.000000V	–
9[3]	10V Range gain	10	+10.000000V	(ON+) 10.000000V	'SET' for non-nominal → CAL

(b) High Voltage – connect as Fig. 1.1(b)

Step	Calibration Operation	4000 Range	Calibration Source Voltage	Precision Divider Select	4000 Output Setting (Nominal value)[1]	AUTOCAL Key Used[2]
10	100V Range zero	100	0.00000V	÷ 10	(ON+) 0.00000V	–
11	100V Range gain	100	+10.000000V	÷ 10	(ON+) 100.00000V	'SET' for non-nominal → CAL
12	1000V Range zero	1000	0.0000V	÷ 100	(ON+) 0.0000V	–
13	1000V Range Gain LETHAL VOLTAGE	1000	+10.000000V	÷ 100	(ON+) 1000.0000V* *Enter High Voltage state using interlock procedure (User's Handbook Sect. 4)	'SET' for non-nominal → CAL

NOTES [1] it is expected that many users will wish to calibrate Range gains at values other than the nominals shown. In these cases set the Calibration Source voltage and 4000 OUTPUT display to in-house standard values near nominal.

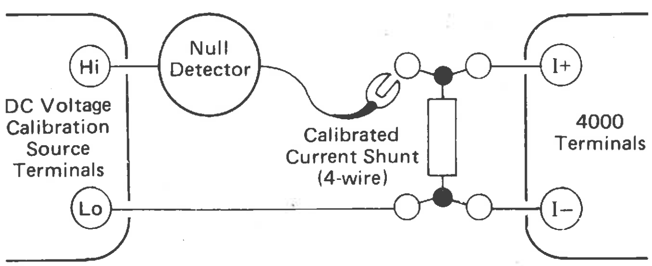
[2] Except for Step 2, use CAL key as trigger (Refer to Calibration Routine).

[3] To trim the internal Master Reference voltage, substitute 'STD' for 'SET' for 1V or 10V Range (Refer to Calibration Routine and description of 'STD').

1.2.9 DC CURRENT CALIBRATION

1. Ensure that the 4000 OUTPUT OFF LED is lit. Select I and connect the DC Voltage calibration source, null detector and calibrated current shunt to the 4000 OUTPUT terminals as shown below. Do not connect null detector to shunt until the voltage across the shunt and the source voltage are close in value.

Fig. 1.2 4000 connections for DC Current Calibration



Preferred shunt values are as follows:

				Calibration Source Output Voltage for Full Range
100μA range	–	10kΩ	1mW min	1V
1mA range	–	1kΩ	10mW min	1V
10mA range	–	100Ω	100mW min	1V
100mA range	–	10Ω	1 Watt min	1V
1A range	–	0.1Ω	1 Watt min	100mV

Ensure that the calibration source voltage is set to zero and that the interconnecting circuit has thermally stabilized.

2. Calibrate the DC Current ranges in the step sequence of Table 1.4, using the Calibration Routine at each step.

3. **Calibration Routine:** Calibration of DC Current using a DC Voltage Calibration Source and a series of calibrated current shunts.

NOTES:

A. For calibration at any value, the routine may be used as printed.

B. For calibration at zero or positive nominal Full Range only, operation (g) may be omitted.

CAUTION: Below 2% of Range, the 4000 corrects for an assumed offset error; at 2% of Range and above the correction is for an assumed gain error.

a) Null Detector	Set to Low sensitivity
b) 4000	Ensure OUTPUT OFF
c) DC Source	Set to the required polarity and value
d) 4000	Select correct FUNCTION and RANGE
e) 4000	Use Full Range, Zero or OUTPUT ↑/↓ keys to set the required polarity and value on OUTPUT display

N.B. Operation (f) must be carried out before operation (g)

f) 4000	Press the correct polarity ON key **CAUTION:** Pressing the wrong ON key will result in twice the OUTPUT being connected across the null detector.

Omit operation (g) if calibrating at Zero or Full Range value

g) 4000	Press SET key: SET LED lights green OUTPUT display reading also appears on MODE display
h) Null Detector	Increase sensitivity to give an off-null reading and use 4000 OUTPUT ↑/↓ keys to back off to null. Repeat until null lies between two values of the OUTPUT display least-significant digit.
j) Null Detector	Set to LOW sensitivity
k) 4000	Press CAL key CAL LED flashes once Not applicable if operation (g) omitted: { MODE display value is transferred to OUTPUT display MODE display is cleared SET LED goes OFF }

Table 1.4 DC Current Calibration

Step	Calibration Operation	Shunt Value	Calibration Source Voltage [1]	4000 OUTPUT Current		AUTOCAL Key Used [2]
				Range	OUTPUT Setting [1]	
1	100μA Range zero	10kΩ	.0000000V	100μ	0.0000μA	–
2	100μA Range gain	10kΩ	+ 1.0000000V	100μ	+100.0000μA	'SET' for non-nominal
3	1mA Range zero	1kΩ	.0000000V	1m	.000000mA	–
4	1mA Range gain	1kΩ	+ 1.0000000V	1m	+ 1.000000mA	'SET' for non-nominal
5	10mA Range zero	100Ω	.0000000V	10m	0.00000mA	–
6	10mA Range gain	100Ω	+ 1.0000000V	10m	+ 10.00000mA	'SET' for non-nominal
7	100mA Range zero	10Ω	.0000000V	100m	0.0000mA	–
8	100mA Range gain	10Ω	+ 1.0000000V	100m	+100.0000mA	'SET' for non-nominal
9	1A Range zero	0.1Ω	0.00000mV	1	.000000A	–
10	1A Range gain	0.1Ω	+100.00000mV	1	+ 1.000000A	'SET' for non-nominal

NOTES

[1] It is expected that many users will wish to calibrate Range gains at values other than the nominals shown. In these cases set the Calibration Source voltage and the 4000 OUTPUT display to in-house standard values near nominal.

[2] At each step, use CAL key as a trigger (Refer to Calibration Routine).

1.2.10 RESISTANCE CALIBRATION

1. Calibration Memory

In Ω function, each RANGE key selects a nominal-value standard resistor. Routine adjustment of the resistor is not necessary. During calibration the actual value is measured and stored in the calibration memory to be displayed whenever that range is selected. Separate memory stores exist for Remote Sense (4-wire), Local Sense (2-wire) and Local Sense zero.

2. 4-Wire Calibration Limits

The value measured in 4-wire Remote Sense does not include the resistance of internal or external wiring. The 4000 accepts any value within ±200 ppm of nominal as a valid calibration.

3. 2-Wire Calibration Limits

The value measured in 2-wire Local Sense is greater than for 4-wire Remote Sense, as it includes the resistance of internal wiring and relay contacts. The 4000 will not accept any 2-wire value less than the stored value for 4-wire, so the 4-wire Remote Sense calibration must be carried out before attempting 2-wire Local Sense. The extra internal resistance varies between Ranges, so the 4000 accepts the following values (x) as valid 2-wire calibrations:

Zero calibration.
1Ω – 1MΩ Ranges:
$0 \leqslant x \leqslant 0.900\Omega$

Value calibrations
1Ω Range:
4-wire value $\leqslant x \leqslant$ (4-wire value + 0.999Ω)
10Ω – 1MΩ Ranges:
4-wire value $\leqslant x \leqslant$ (4-wire value + 1.999Ω)

4. "Error 6" message

"Error 6" appears on the MODE display for any attempt to enter a value outside the 4-wire or 2-wire limits quoted above.

NOTE: When resistance is calibrated in Remote Sense, the 4000 overwrites the Local Sense calibration memory with the new 4-wire value.

5. 4-wire and 2-wire Connections

Fig. 1.3 (a)
4-wire calibration

Remote Sense
Energising Current Source

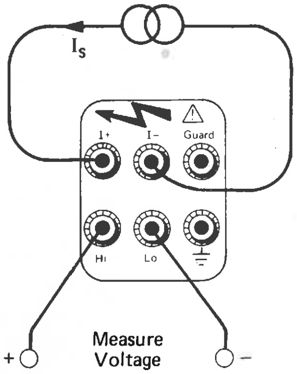
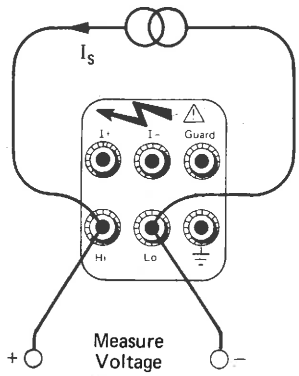


Fig. 1.3 (b)
2-wire calibration
(using 4-wire method externally)

Local Sense
Energising Current Source



6. Calibration sequence

Press Ω key and calibrate the resistors in the step sequence of Table 1.5 (a and b), using the Calibration Routine at para 7 (a or b). Refer to para 5 for connections to the measuring equipment. For 4-wire connections in Remote Sense, only the value of the internal Standard Resistor is measured. In Local Sense, a 4-wire method is used to exclude the resistance of the external leads from the measured value.

7. Calibration Routine: Measurement and Storage of the values of an internal resistor.

a) **Remote Sense** (Internal 4-wire, connected as Fig. 1.3(a).)
Full Range values – Routine for Table 1.5(a)

i)	4000	Select OUTPUT OFF and Ω Select Remote Sense
ii)	4000	Press required resistor (RANGE) key: The previously calibrated value appears on the OUTPUT display
iii)	4000 and resistance-measuring equipment	Press OUTPUT ON+ and measure the value of the internal resistor
iv)	4000 OUTPUT ↑/↓ Keys	Set the measured value on the OUTPUT display
v)	4000 CAL Key	Press to store OUTPUT display value
vi)	4000	Set OUTPUT OFF
vii)	Repeat operations (ii) to (vi) for each step of Table 1.5(a)	

b) **Local Sense** (Internal 2-wire, connected as Fig. 1.3(b).), Remote Sense OFF)
Full Range and Zero values – Routine for table 1.5(b)

i)	4000	Select OUTPUT OFF and Ω Deselect Remote Sense
ii)	4000	Press required resistor (RANGE) Key: The previously-calibrated value appears on the OUTPUT display.
iii)	4000 and resistance-measuring equipment	Press OUTPUT ON+ and measure the value of the internal resistance
iv)	4000 OUTPUT ↑/↓ Keys	Set the measured value on the OUTPUT display
v)	4000 CAL Key	Press to store OUTPUT display value
vi)	4000 Zero Key	Press and repeat operations (iii) to (v) for this RANGE selection.
vii)	4000	Set OUTPUT OFF
viii)	Repeat operations (ii) to (vii) for each step of Table 1.5(b).	

Resistance Calibration

Table 1.5 Internal Resistor value measurement and storage

a) **Remote Sense** (Internal 4-wire, connect as Fig. 1.3(a).)
Calibration at Full Range. Resolution 7½ digits, Tolerance ±199.9ppm (±1999 digits).

Step	Range	Measured resistance value, Calibration Limits			
1	10MΩ	9.998,001	to	10.001,999	MΩ
2	1MΩ	.999,800,1	to	1.000,199,9	MΩ
3	100kΩ	99.980,01	to	100.019,99	kΩ
4	10kΩ	9.998,001	to	10.001,999	kΩ
5	1kΩ	.999,800,1	to	1.000,199,9	kΩ
6	100Ω	99.980,01	to	100.019,99	Ω
7	10Ω	9.998,001	to	10.001,999	Ω
8	1Ω	.999,800,1	to	1.000,199,9	Ω

b) **Local Sense** (Internal 2-wire, connect as Fig. 1.3(b), Remote Sense OFF)
Calibration at Full Range and Zero. Resolution as listed in table.
Tolerances – 0Ω + 0.999Ω on 1 Ω Range, 0Ω + 1.999Ω on 10Ω – 1MΩ Ranges, –0Ω + 0.900Ω for zero on 1Ω – 1MΩ Ranges.

Step	Range	Resolution (digits)	Resistance value Limits	Zero Limits			
9	1MΩ	7½	Step 2 value, –0 +19 digits	.000,000,0	to	.000,000,9	MΩ
10	100kΩ	7½	Step 3 value, –0 +199 digits	0.000,00	to	0.000,90	kΩ
11	10kΩ	7½	Step 4 value, –0+1999 digits	0.000,000	to	0.000,900	kΩ
12	1kΩ	6½	Step 5 value, –0+1999 digits	.000,000	to	0.000,900	kΩ
13	100kΩ	5½	Step 6 value, –0+1999 digits	0.000	to	0.900	Ω
14	10Ω	4½	Step 7 value, –0+1999 digits	0.000	to	0.900	Ω
15	1Ω	3½	Step 8 value, –0 +999 digits	.000	to	.900	Ω

1.3 REMOTE CALIBRATION GUIDELINES

1.3.1 Introduction

The operation of the 4000 in systems applications via the IEEE 488 Interface, is described in Section 5 of the User's Handbook.

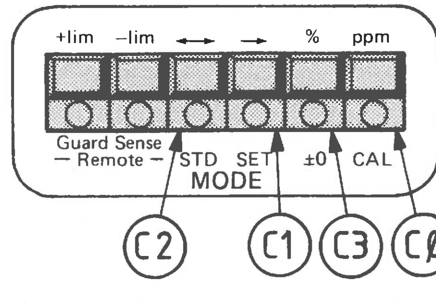
In addition to its capability as a programming calibrator, the 4000 can itself be calibrated under remote control. Full autocalibration of the instrument over the bus implies availability of programmable standards, a programmable null-detector and a suitably-programmed controller.

The Datron 4900 Series DC Voltage Calibration System is designed to be programmable, requiring only the addition of a bank of ten standard cells and a null detector.

1.3.2 Calibration Commands

Table 1.6 lists the device-dependent commands used in the 4000. The relevant calibration codes are described in Fig. 1.4 and Table 1.6.

Fig. 1.4 Transfer of front-panel calibration controls to System Operation



These commands can only be activated when two conditions have been fulfilled:

The CALIBRATION ENABLE Keyswitch on the 4000 Rear Panel must be set to ENABLE, **and** the IEEE Interface command-code W1 must have been received and activated.

When the 4000 is under remote control over the bus, the command-code Wϕ disables the 'C' codes, regardless of the keyswitch setting.

Table 1.6 Availability of Command Codes

Command Codes	AUTOCAL Mode		DC Voltage (DC)	DC Current (I)	Resistance (Ω) Local Sense (2-wire)	Resistance (Ω) Remote Sense (4-wire)
C1 and Cϕ	SET and CAL	Zero offset for range at User's selected value	100mV–1000V Ranges only	All Ranges		
		Gain for range at User's standard value				
C3 and Cϕ	±0 and CAL	Alignment of internal ON+ and ON– zeros	10V Range only			
C2 and Cϕ	STD and CAL	Internal Reference gain at user's Standard value	1V and 10V Range Only			
Cϕ Only	CAL Only	Zero offset for range	All Ranges	All Ranges	1Ω – 1MΩ Ranges Only	
		Gain for range at Full Range Value	100mV–1000V Ranges Only			All Ranges

1.3.2.1 General Procedure

The Main Register is set to the Calibration Standard value (M***...), the 4000 Output is switched ON (O1), and one of the calibration mode command codes (C1, C2, C3) may be transmitted. The 'M' Code is adjusted to obtain a null at the Calibration Standard value, and Cϕ is transmitted to execute the calibration.

1.3.2.2 Command Code Facilities

C1 (SET) — C1 allows calibration to any value in the selected Range (e.g. at a standard cell voltage). If the value initially input by 'M' Code is less than ±2% of Full Range value, the 4000 assumes that an offset calibration is requested, and if at ±2% or greater, a gain calibration is assumed.

C2 (STD) — C2 allows a user to trim the value of the internal Master Reference voltage. The facility can be used to correct for any long-term drift, or to avoid a full recalibration of the 4000 when Laboratory References have been restandardised. C2 (STD) calibration effectively changes the gain of all voltage and current ranges in the same ratio, by a simple procedure available either on 1V or 10V range.

C3(±0) — C3 is used to align the ON+ and ON– zeros of all voltage and current ranges, by a two-part calibration on the 10V range. It is only necessary when the ON+ and ON– zeros on the 10V range do not coincide at the same null.

Cϕ (CAL only) — Cϕ executes the preselected AUTO-CAL mode. If it is sent without first sending SET, ±0 or STD, the 4000 assumes that a calibration at either Zero or Full Range is required. It uses the value input by 'M' Code to distinguish between Zero (Offset calibration) and Full Range (gain calibration) as for C1 (SET) mode.

1.3.3. Guidelines — An Example

The following sequence suggests a method of calibrating the 4000 IV Range Gain against a standard cell value of +1.018057V. It is assumed that the 4000 is correctly addressed with its Calibration Keyswitch set to ENABLE, that the 4000 Output is OFF; and that a Null Detector set to Low Sensitivity is connected between Standard Cell buffer and 4000 Hi/Lo terminals as in Fig. 1.1 (a) of Section 1.2.8.

	4000 Codes
(a) Command the 4000:	
DC Volts	Fϕ
1V Range	R5
Local Guard and Sense	Gϕ Sϕ
Calibration Enable	W1
Output Value to calibration point	M+1.018057
Select "SET" Calibration mode	C1
Output ON	O1

(b) Establish null tolerance limits

(c) Command the null detector:
Recall Sensitivity Range and Reading
Increase Sensitivity Range and repeat recall until reading exceeds half-scale

(d) Calculate 4000 setting for null
Set 4000 output to calculate value — M****...

(e) Repeat (c) and (d) until null is within limits

(f) Command the 4000 to execute "CAL"Cϕ

The example suggests only the broad outline of one of many sequences which could be used to perform 4000 calibration.

1.4 PRECALIBRATION

For all normal purposes, the routine procedures detailed in Section 1.2 (and repeated in User's Handbook Section 8) are sufficient to maintain 4000 calibration.

In an initial internal calibration process at manufacture, certain 'pre-cal' parameters are established in a special calibration memory to define the overall linearity of the 4000, and to allow maximum routine calibration memory span for adjustments. Thus all routine calibrations may be performed from the front panel or over the IEEE Interface without removing any covers.

The stored parameters are invalidated by replacement of certain critical parts of the instrument:

1) The Lithium battery which powers the whole calibration memory when the instrument supply is switched off. This should be replaced at five-year intervals (refer to Section 5.3).
2) The Digital Assembly
3) The Reference Divider Assembly
4) Critical components in the Digital or Reference Divider assemblies

(2–4: Normally replaced only on failure. A full list is given in Section 1.1 Table 1.1)

After replacement of any of these parts, new parameters are generated and stored in the "pre-cal" memory by the procedures detailed in this section.

Pre-calibration must be followed by a full Routine Calibration of the whole instrument (Section 1.2).

1.4.1 Pre-calibration Procedure

1.4.1.1 Validity

The adjustments detailed in the following sequences include intentionally clearing the instrument's calibration memory, which loses all previous calibration information. Therefore, before proceeding make certain that the reasons for carrying out a complete recalibration are valid. (If in any doubt, consult your Datron Service Centre)

1.4.1.2 Calibration Standards Equipment Required

1. A DC Voltage Calibration source of 10V ±20ppm
2. A ÷2 precision divider, capable of dividing 20.000,000V to 10.000,000V ± 0.1ppm, D.C.
3. A battery-operated null detector with variable sensitivity.

Example: Keithley Instruments Model 155
Read the "Notes on the Use of the Null Detector" at Section 1.2.3.1.

1.4.1.3 Identification of Access Holes (Fig. 1.5)

a) Release 6 screws retaining the top cover
b) Lift the top cover at the front of the instrument and locate two holes giving access to the two-position "pre-cal Enable" switch and the press-button "Clear Calibration Memory" switch.

DO NOT OPERATE EITHER SWITCH YET

c) Replace the top cover, do not secure

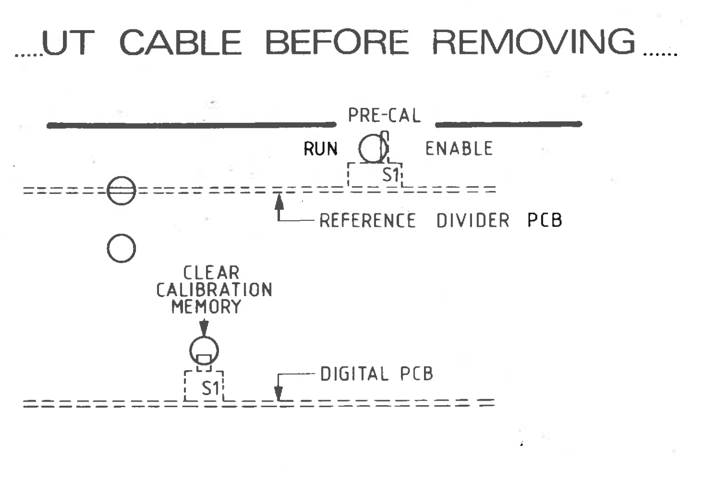


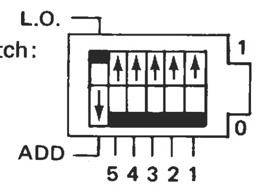
Fig. 1.5 Location of "PRECAL" and "CLEAR" Switches

1.4.1.4 Preparation

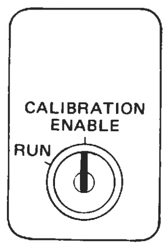
Before any calibration is carried out, prepare the 4000 as follows:

1. Turn on the instrument to be checked and allow minimum of 4 hours to warm-up in the specified environment

2. IEEE 488 Address switch: Set to ADD 11111 as shown (Address 31)



3. CALIBRATION ENABLE key switch: Insert Calibration Key and turn to ENABLE.



1.4.1.5 Interconnections

CAUTION: First read the Notes on the use of the Null Detector in Section 1.2.3.1.

(a) Ensure that the 4000 OUTPUT OFF LED is lit.

(b) Select DC and connect the DC Voltage Calibration source, Precision Divider and Null Detector to the 4000 terminals as shown. Use short leads.

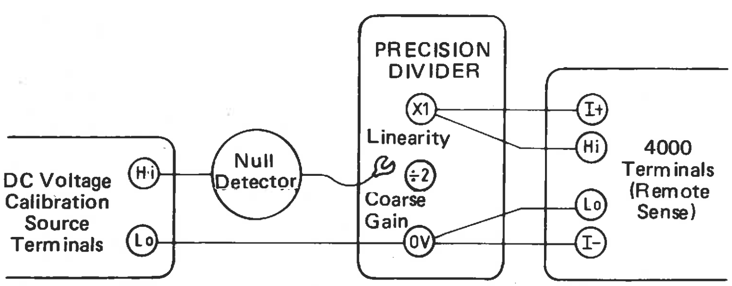


Fig. 1.6 Interconnections for Pre-calibration (Coarse Gain and Linearity)

(c) Ensure that the calibration source voltage is set to zero and that the interconnecting circuit has thermally stabilized. Do not connect the Null Detector yet.

1.4.1.6 "Pre-cal Enable" and Calibration Memory "Clear" Switches

(a) 4000	Lift the top cover at the front. Locate the hole which gives access to the pre-cal enable switch.
(b) "Enable"	Insert an insulated tool in the hole and move the pre-cal switch to the right (Enable). The legend Cal appears on the OUTPUT display also.
(c)	Locate the hole which gives access to the Calibration Memory "Clear" push button.
(d) "Clear"	Insert an insulated tool in the hole and press the button to clear the calibration memory. Refit the top cover but do not secure.

1.4.1.7 ±0

(a) Null Detector	Set to Low sensitivity.
(b) 4000	Ensure OUTPUT OFF in 10V DC range. Ensure Remote Sense LED is unlit.
(c) 4000	Press OUTPUT Zero Key Connect the Null Detector between Hi and Lo terminals Press ON+ Key Press ±0 Key: ±0 LED lights, OUTPUT display at zero.
(d) Null Detector	Increase sensitivity to give an off-null reading (approx. −20mV) and use 4000 OUTPUT ↑/↓ keys to back-off to null. Repeat until null lies between two values of the output display least-significant digit.
(e) 4000	Press CAL key: CAL LED lights No change to OUTPUT display
(f) 4000	Press ON− key
(g) Null Detector	Obtain accurate null as in (d) above.
(h) 4000	Press CAL key: CAL LED goes OFF ±0 LED goes OFF OUTPUT display falls to zero
(j) Null Detector	Set to Low sensitivity

The 4000 positive and negative zeros are now both aligned to zero.

(k) 4000	Disconnect the Null Detector

1.4.1.8 Coarse Gain

(a)	Null Detector	Set to Low sensitivity
(b)	4000	Ensure OUTPUT OFF
(c)	4000	Select Remote Sense and ensure LED is lit
(d)	4000	Press the SET Key: SET LED lights green OUTPUT display reading goes to zero.
(e)	4000	Use OUTPUT ↑/↓ keys to set the OUTPUT display to +19.999,999V
(f)	4000	Press the ON+ Key
(g)	Null Detector	Connect between Calibration Source Hi and Precision Divider ÷2 terminal (Fig. 1.6)
(h)	Null Detector	Increase sensitivity to give an off-null reading and use 4000 ↑/↓ keys to back-off to null. Repeat until null lies between two values of the OUTPUT display least-significant digit.
(j)	4000	Press CAL Key: CAL LED flashes once. OUTPUT display changes to +19.999,999V. SET LED goes OFF
(k)	Null Detector	Set to Low Sensitivity.
(l)	4000	Set OUTPUT OFF

1.4.1.9 Linearity

(a)	Null Detector	Disconnect from Precision Divider
(b)	4000	Ensure set to OUTPUT OFF Select Remote Sense and ensure LED is lit.
(c)	4000	Press the STD Key: STD LED lights green OUTPUT display reading goes to zero.
(d)	4000	Use OUTPUT ↑/↓ keys to set the OUTPUT display to +10.000,000V
(e)	4000	Press the ON+ Key
(f)	Null Detector	Connect between Calibration Source Hi and Precision Divider X1 terminal.
(g)	Null Detector	Increase sensitivity to give an off-null reading and use 4000 ↑/↓ keys to back-off to null. Repeat until null lies between two values of the OUTPUT display least-significant digit.
(h)	4000	Press CAL Key: CAL LED flashes once OUTPUT display changes to +10.000,000V STD LED goes OFF.
(j)	Null Detector	Set to Low sensitivity. Disconnect.
(k)	4000	Set OUTPUT OFF.

1.4.1.10 Pre-cal Enable Switch (See CAUTION below)

(a) 4000 — Lift the top cover at the front.

Locate the hole which gives access to the pre-cal Enable switch.

Insert an insulated tool in the hole and move the pre-cal switch to the left (RUN).

The legend "cal" on the OUTPUT display disappears, but the same legend remains on the MODE display.

CAUTION: DO NOT re-press the calibration memory "clear" button. If this is done, the micro-zero, coarse gain and linearity adjustments will have to be repeated.

(b) 4000 — Refit and secure the top cover.

1.4.1.11 Routine Calibration

The 4000 is now ready for full Routine Calibration as detailed in Section 1.2.

1.5 Ω OPTION INTERNAL ADJUSTMENT (Refer to Section 5.4)

The Autocal procedure for routine calibration of the 4000 Resistance Function is described in Section 1.2.10.

The method of calibration is to measure the value of each standard resistor, and store the measured value in non-volatile calibration memory. Subsequently, each time a resistance RANGE is selected, the previously calibrated value is displayed.

If a standard resistor has been subjected to undue stress, its value may have moved outside its tolerance (signalled by an Error 6 message during Routine Autocalibration). If the value is less than approx. 50ppm outside tolerance, it can be adjusted internally using a variable trimmer. For values out of tolerance in excess of 50ppm it is likely that the resistor has been over-stressed — consult your Datron Service Centre.

1.5.1 Manual Trimming Procedure

The following procedure is a supplement to Routine Autocalibration. It is necessary only when the 4-wire calibration of Section 1.2.10 has resulted in an "Error 6" message.

It can also be used when, for operational reasons, it is necessary to calibrate a resistor at its nominal value. For this purpose a continuously-reading method of measurement is convenient.

(a) Release eight screws retaining the top cover.

(b) Lift the top cover at the front of the instrument and locate the 8 holes giving access for "Ω OPTION ADJUSTMENT"

(c) Insert an insulated screw driver tool in the hole for the range selected, and adjust the preset resistor (rotating clockwise increases the resistance value)

(d) Re-measure the 4-wire value and repeat operation (c) until the desired value is obtained

(e) Re-calibrate the range for 4-wire and 2-wire connections as detailed in section 1.2.10.

(f) Repeat the manual trimming procedure above for all ranges as required.

(g) Finally refit and secure the top cover using the eight screws removed in (a), above.

SECTION 2

FAULT DIAGNOSIS

WARNING HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.

ELECTRIC SHOCK CAN KILL!

CAUTION The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

2.1 INTRODUCTION

2.1.1 Use of diagnostic guides

The diagnostic guides given in Section 2.2 are intended to aid the user in locating a failed printed circuit board or other assembly. The self-diagnostic capabilities of the 4000 provide the first step in fault analysis by displaying a FAIL message on the mode display. Initial actions to be taken after the occurrence of a FAIL message are given, where applicable, in the diagnostic guides (section 2.2). The FAIL message localizes the failure into a distinct functional area and the "Fault Condition" summary in each guide relates the function failure into a probable hardware boundary. The identities of the assemblies involved in the failure are given beneath the fault condition summary, but it is unlikely that all assemblies listed will prove to be faulty.

For successful failure analysis, it is advisable to be familiar with the electronic functioning of the instrument and with the physical location of the assemblies. To assist in these aspects,, the diagnostic guides include references to relevant parts of this publication.

2.1.2 Effects of protective measures on diagnosis

2.1.2.1 Protective suppression of fault conditions

The 4000 incorporates built-in protection in hardware and software. To minimise damage, protective circuitry acts immediately, backed up by a pre-programmed CPU response to detected failure symptoms. The CPU informs the user by presenting a failure message on the MODE display.

When investigating a failure, it should therefore be anticipated that protective measures will have suppressed the original fault conditions. A useful starting-point is to identify the origin of the failure message to localise the area of search.

2.1.2.2. FAIL 5 as default state

Faults which result in display messages FAIL 2, 3 or 4 can pose a safety hazard to the operator, and apply excessive voltage to external circuitry. To protect against this, the instrument is programmed to default to FAIL 5 state as rapidly as possible after its initial response to the failure symptoms. The CPU switches Output OFF, trips the safety monitor (Watchdog) and changes the display to FAIL 5.

In normal use, an operator will probably notice only FAIL 5, and miss the original failure message. In FAIL 5 state, front panel control is inhibited until Safety Reset is pressed. This returns the instrument to the state for which the original fault conditions and failure message were produced, but with Output OFF.

2.1.2.3 To observe the original failure message

Two procedures can be used:

(a) Carry out the self-test routine (section 2.3) The failure message may recur during this test.

(b) Reset the instrument to reproduce the fault, carefully watching the MODE display. The original failure message should reappear momentarily, prior to defaulting into FAIL 5.

Then select the appropriate diagnostic guide in section 2.2.

2.2 DIAGNOSTIC GUIDES

2.2.1 FAIL 1 display message

DISPLAY: FAIL 1

Excessive internal temperature

INITIAL ACTION

1. Switch Power OFF
2. Allow to cool for 15 minutes
3. Switch Power ON – If FAIL 1 persists, repeat 1 & 2
4. Select operating mode when FAIL 1 clears
5. No failure display – no further action

   FAIL 1 recurs – fault persists

FAULT CONDITION

High temperature sensed in:

1. Positive Heatsink Assembly

or 2. Negative Heatsink Assembly

Fault indication signal $\overline{\text{TEMP ST}}$ active

POSSIBLE FAULT LOCATION

1.	Positive Heatsink Assembly	400454
2.	Negative Heatsink Assembly	400461
3.	Power Amplifier (dc) Assembly	400449

FURTHER INFORMATION IN THIS HANDBOOK

Circuit diagram number:	430449
Layout drawing numbers:	400449
	400454
	400461

Technical descriptions: Section 4.8

2.2.2 FAIL 2 display message

DISPLAY: FAIL 2

Over-voltage

INITIAL ACTION

NB. This failure can be caused by injection of an external voltage exceeding 130V across the 4000 terminals.

1. Ensure that OUTPUT is OFF (4000 should have tripped to FAIL 5).
2. Disconnect external leads from 4000 terminals.
3. Press Safety Reset.
4. Carry out self-test sequence.
5. FAIL 2 recurs – fault persists.
6. No failure display – Reproduce original conditions in Local Sense with no external connections.
7. No failure display – check external circuit and proceed with careful use.
8. FAIL 2 recurs – fault persists.

FAULT CONDITION

1. Over voltage circuit on DC pcb has detected a voltage in excess of 130V between PHi and PLo lines, and has activated $\overline{\text{HV ST}}$ signal to the CPU. AND
2. The CPU has recognised that the instrument is not in High Voltage State, so has generated FAIL 2 display. THEN
3. The CPU has switched output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

1.	Injection of external voltage	
2.	DC pcb assembly	400445
3.	Power Amplifier (dc) pcb assembly	400449

FURTHER INFORMATION IN THIS HANDBOOK

Circuit diagram numbers: 430449, 430445
Layout drawing numbers: 400449, 400445
Self-test procedure: Section 2.3
Technical descriptions: Section 4.7, 4.8

2.2.3 FAIL 3 display message

DISPLAY: FAIL 3

Control data corrupted

INITIAL ACTION

No immediate action required

FAULT CONDITION

1. Control data corrupted
2. CPU has detected errors in serial transfer of data between out-guard and in-guard circuits, and generated FAIL 3 display. THEN
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

1. Reference Divider PCB Assembly 400444
2. Analogue Interface PCB Assembly 400443

FURTHER INFORMATION IN THIS HANDBOOK

Circuit diagram numbers: 430443; 430444
Layout drawing numbers: 400443; 400444
Technical descriptions: Section 4.5

2.2.4 FAIL 4 display message

DISPLAY: FAIL 4

Precision divider fault

INITIAL ACTION

No immediate action required

FAULT CONDITION

1. Precision divider fault
2. CPU has detected errors in the most-significant data bits set in the precision divider input data latches, and generated FAIL 4 display. THEN
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

Analogue Interface PCB Assembly 400443

FURTHER INFORMATION IN THIS HANDBOOK

Circuit diagram number: 430443
Layout drawing number: 400443
Technical description: Section 4.6

2.2.5 FAIL 5 display message

DISPLAY: FAIL 5

Safety Monitor (Watchdog) tripped

INITIAL ACTION

Use the checking sequence below, watching the MODE display carefully at each stage to detect any FAIL number appearing momentarily before FAIL 5. If no failure message occurs, carry on to the next stage.

Stage 1: Press Safety Reset

Stage 2: Carry out Self-test sequence (Section 2.3)

Stage 3: Set Output ON

Stage 4: Proceed with careful use.

If FAIL 2 occurs at stage 3, ensure that it is not due to injection of an external voltage in excess of 130V by disconnecting the 4000 terminals and repeating the checks. If FAIL 5 alone occurs, proceed to "Fault Condition" below. For any FAIL other than FAIL 5, transfer to the diagnostic guide for that message.

FAULT CONDITION

18mS monostable (M10 in reference divider) has been deprived of at least two trigger pulses and has timed out, activating "BARK" and "BARK DELAYED" (BARK + 47mS) signals from M13 in the reference divider pcb.

Summary of "BARK" effects:

1. 16KHz drive to PA is inhibited
2. PA output disconnected from HV transformer
3. HV transformer primaries shorted
4. Standard resistors in I/Ω pcb isolated
5. Current output OFF – 100μA range selected
6. BARK status message sent to CPU
7. CPU starts controlled shut-down

Summary of "BARK DELAYED" effects:

1. DC pcb RL 13 and 14 de-energised (Output OFF)
2. Outputs from control latches in reference divider pcb are disabled by setting into "Tristate". Each output line has a pull-up or pull-down resistor which sets the analogue circuitry into a safe condition.

POSSIBLE FAULT LOCATION

Digital PCB Assembly (No gated WRT STRB pulses at J2/J3–29)	400442
Analog Interface PCB Assembly (No SSDA strobe pulses; or Watchdog disabled)	400443
Reference Divider PCB Assembly (Incorrect functioning of Watchdog setup circuitry)	400444

NB The Watchdog is designed primarily to ensure that CPU malfunctions do not set up dangerous conditions in the analogue circuitry.

FURTHER INFORMATION IN THIS HANDBOOK

Circuit diagram numbers:	430442 430443 430444
Layout drawing numbers:	400442 400443 400444

Technical description: Section 4.5

2.2.6 FAIL 6 display message

DISPLAY: FAIL 6

Calibration memory fault

INITIAL ACTION

1. Select Output OFF, Spec OFF, Error OFF
2. Perform self-test sequence (Section 2.3)
3. No failure display — no further action
4. FAIL 6 recurs — recalibration required
5. Select Cal. } Refer to Section 1
6. Recalibrate } Refer to Section 1
7. Calibration failure — fault persists

FAULT CONDITION

Calibration memory fault on Digital pcb assembly

POSSIBLE FAULT LOCATION

Digital PCB Assembly 400442

FURTHER INFORMATION IN THIS HANDBOOK

Circuit diagram number: 430442
Layout drawing number: 400442
Self-test procedures: Section 2.3
Calibration procedures: Section 1
Technical descriptions: Section 4.2

2.2.7 FAIL 7 display message

DISPLAY: FAIL 7

P.A. 15V/50V power failure or 50V Regulator over temperature

INITIAL ACTION

1. Switch power OFF
2. Allow to cool for 15 minutes
3. Check line supply is correct for input voltage setting
4. Switch power on — If FAIL 7 persists, repeat 1 & 2
5. Select operating mode when FAIL 7 clears
6. No failure display — no further action
7. FAIL 1 recurs — fault persists

FAULT CONDITION

1. ± 15V common 2 power supply failure;
2. ± 50V power supply failure;
3. Power Supply/I Heatsink overtemperature;
4. Fault indication signals $\overline{\text{PS ST}}$ or DC ST active;
5. Line input voltage too high?

POSSIBLE FAULT LOCATIONS

1.	Power Amplifier (dc) PCB Assembly	400449
2.	In-guard power supply PCB assembly	400451
3.	Power Supply/I Heatsink Assembly	400455
4.	Interconnection PCB Assembly	400439

FURTHER INFORMATION IN THIS HANDBOOK

Circuit diagram numbers: 430439; 430449; 430451; 430455
Layout drawing numbers: 400439; 400449; 400451; 400455
Technical descriptions: Section 4.8

2.2.8 Error OL display message

DISPLAY: ERROR OL

DC Volts: Output current limited at 25mA
I : Output voltage compliance limited at 3V

INITIAL ACTION

1. If DC Voltage range selected:
   (a) Set Output OFF (Automatic if 100 or 1000V range selected)
   (b) Disconnect external circuit
   (c) Set Ouput ON
   — If no Error OL or FAIL message, check external circuit for low resistance, drawing output current in excess of 25mA limit.
   — If Error OL recurs, internal fault persists.

2. If I range selected:
   (a) Set Output OFF
   (b) Short Output terminals I+ to I—
   (c) Set Output ON
   — If no Error OL or FAIL message, check external circuit for high resistance, developing output voltage in excess of 3V compliance limit
   — If Error OL recurs, internal fault persists

FAULT CONDITION

1. If Low DC Voltage range (100μV — 10V): Overcurrent sense circuit (M9/M8 in DC pcb) has detected a current in the I— line of approx 28mA or more, and has activated $\overline{\text{LIM ST 1}}$ signal to the CPU.

2. If High Voltage range (100V or 1000V):
   Either (a) Opto-isolator detector (M11 in the Power Amp (DC) pcb) has detected a current in the I+ line of approx 35mA or more,
   or (b) Over Voltage detector (M9 in the Power Amp (DC) pcb) has detected an output voltage in excess of 1440V.

   In either condition (a) or (b), M10 in the power amplifier removes the 16KHz drive from the input to the PA, and generates $\overline{\text{HI I ST}}$ signal to the CPU; which responds by setting Output OFF, and DC Reference voltage to zero.

3. If I range selected:
   Overvoltage detector circuit (M15 in I/Ω pcb) has detected a terminal voltage of 4.4V or more and has activated $\overline{\text{LIM ST1}}$ signal to the CPU. If 100mA or 1A range selected, the CPU switches Output OFF and reduces DC Reference voltage to zero

POSSIBLE FAULT LOCATIONS

1.	External circuit	
2.	DC PCB Assembly	400445
3.	Power Amp (DC) Assembly	400449
4.	I/Ω PCB Assembly	400448

FURTHER INFORMATION IN THIS HANDBOOK

1. Circuit diagram numbers: 430445, 430449, 430448
2. Layout drawing numbers: 400445, 400449, 400448
3. Technical descriptions:
   Low DC Voltage ranges: Section 4.7
   100 or 1000V ranges: Section 4.8
   I ranges: Section 4.9

2.3 SELF-TEST SEQUENCE

2.3.1 General

The self-test sequence is performed in two stages:

Stage 1 is a fully automated test of safety monitoring and high-voltage safety interlocks;

Stage 2 is a semi-automatic test of keyboard and display functions and requires operator-involvement.

2.3.2 Stage 1 (Fig. 2.1)

Entry into Stage 1 is selected automatically whenever the TEST key is pressed for the first time (the test is not allowed if OUTPUT ON, ERROR or SPEC are selected or when in remote control). Indication of test mode is given by the LED in the TEST key being lit. The full sequence of Stage 1 must be completed before exit from the test mode can be made. The tests performed in Stage 1 are as follows:

1. Safety Monitor Watchdog Test. In this, the safety monitor is tripped causing the word SAFETY to appear in the Mode display. It is necessary for the operator to reset the safety monitor by pressing the SAFETY RESET key, after which, the SAFETY display is cancelled and the test sequence continues.

2. Calibration Memory Test. The contents of the non-volatile calibration RAM are checked for validity. Failure results in the message FAIL 6 appearing on the Mode display.

3. High-voltage Protection. This test ensures that a voltage demand made to the power amplifier does not trip the software voltage detector when immediately below the detector threshold level, but when raised to a level above the detector threshold the detector is tripped. Incorrect detect action is shown by the message FAIL 2 on the Mode display. No voltages appear at the output terminals during this test. Fail messages are up-dated as the test sequence progresses through the calibration memory and high-voltage tests. After completion of the high-voltage test, the test mode ends and the test LED is cancelled. If faults were encountered the last FAIL message will remain on the display. Fault diagnosis can now be performed. If no faults are encountered during Stage 1, the message PASS is displayed. The calibrator may now be returned to normal operation, or Stage 2 of the self-test sequence can be selected.

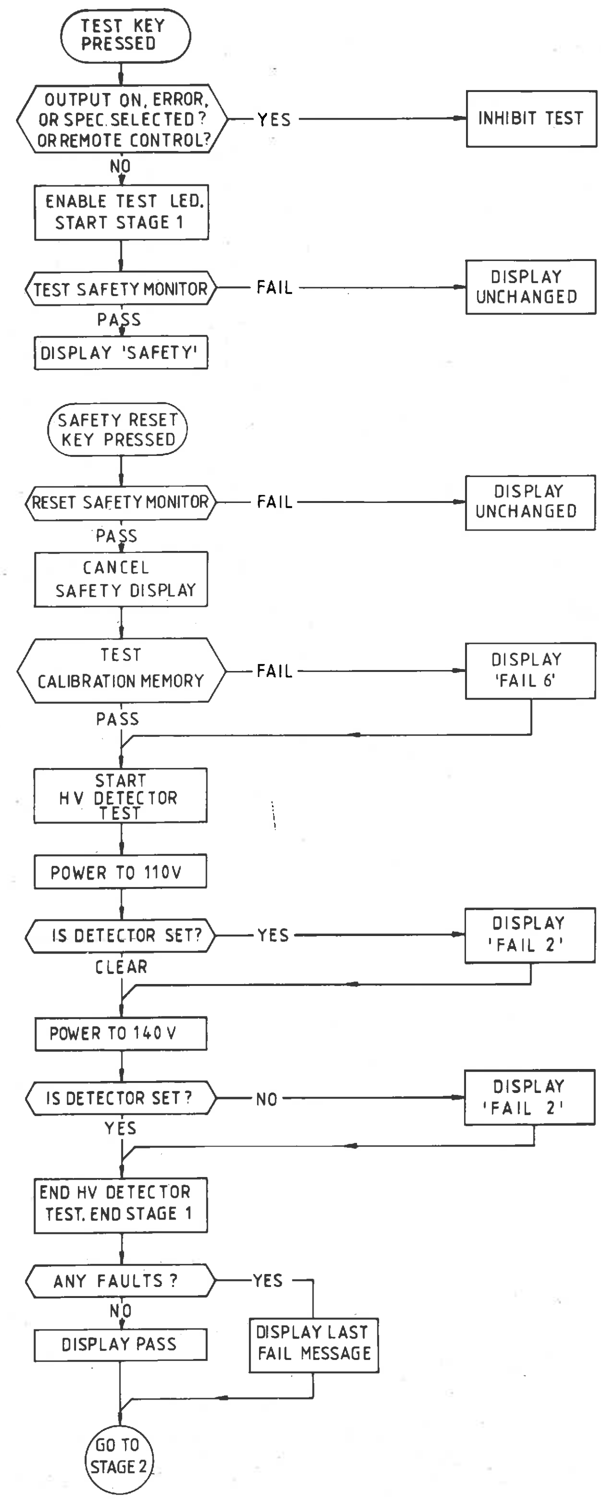


FIG. 2.1 SELF TEST SEQUENCE STAGE 1

2.3.3. Stage 2 (Fig. 2.2)

Entry into Stage 2 of the self-test sequence is made when the TEST key is pressed AFTER the completion of Stage 1. The test proceeds by sequentially displaying all segments and legends. The test continues, showing segment-by-segment, all seven-segment digits, legends and commas. After all digits have been displayed, the keyboard LED indicators are lit in a sequence which proceeds from left to right. (TEST LED remains lit).

The next test in the sequence requires operator participation in order to check key functions. Two half-digit symbols are shown on the mode display to indicate that the keys are ready to be checked. Operation of Up, Down and Output Selection keys are shown by a symbol on the display immediately above the key; operation of Mode, Range, Function and Output keys are shown by the key's LED. In these tests the display or LED remains lit until another key is pressed. At any part of Stage 2, pressing TEST or ZERO key will end the test and cancel the TEST LED.

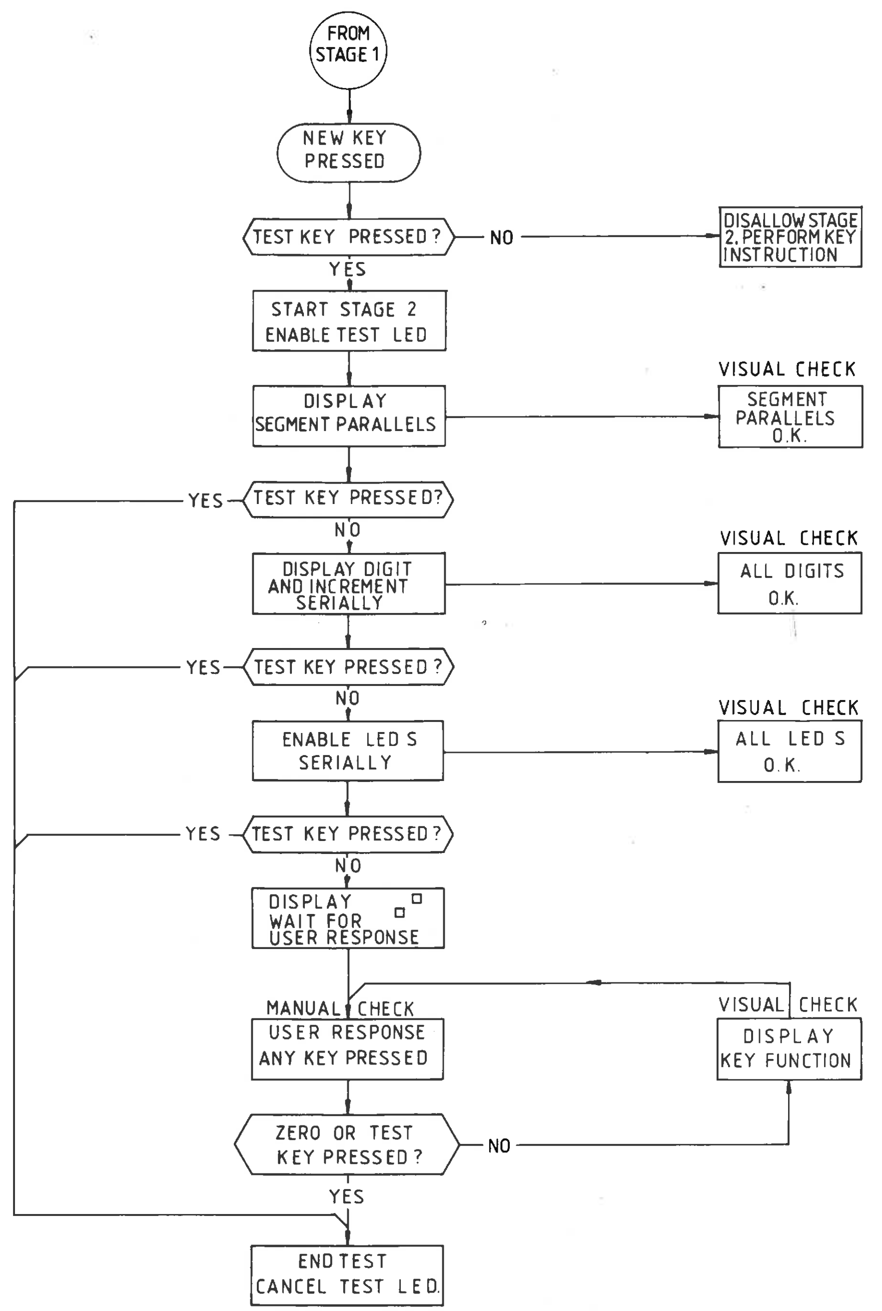


FIG. 2.2 SELF TEST SEQUENCE STAGE 2

2.4 Fuse Protection

In addition to the electronic protection devices used in the 4000, fuses are provided to protect against catastrophic component failure.

2.4.1 Fuse Replacement

A blown fuse is merely a symptom of failure, in the large majority of cases the cause lies elsewhere.

CAUTION Every occurrence of a blown fuse should be investigated to find the cause. Only when satisfied that the cause is known, and has been removed, should a user replace a fused link by a serviceable item.

2.4.2 Reasons for fusing

The fuses in the 4000 fall into two main groups:

(i) Clip-in anti-surge fuses in the Power Supplies and Power Amplifier protect the power source from extreme loading.

(ii) Solder-in fuses on the DC and I/Ω assemblies protect the low voltage, current and resistance circuits from the application of high voltages in the event of relay failure.

Table 2.1 lists their locations.

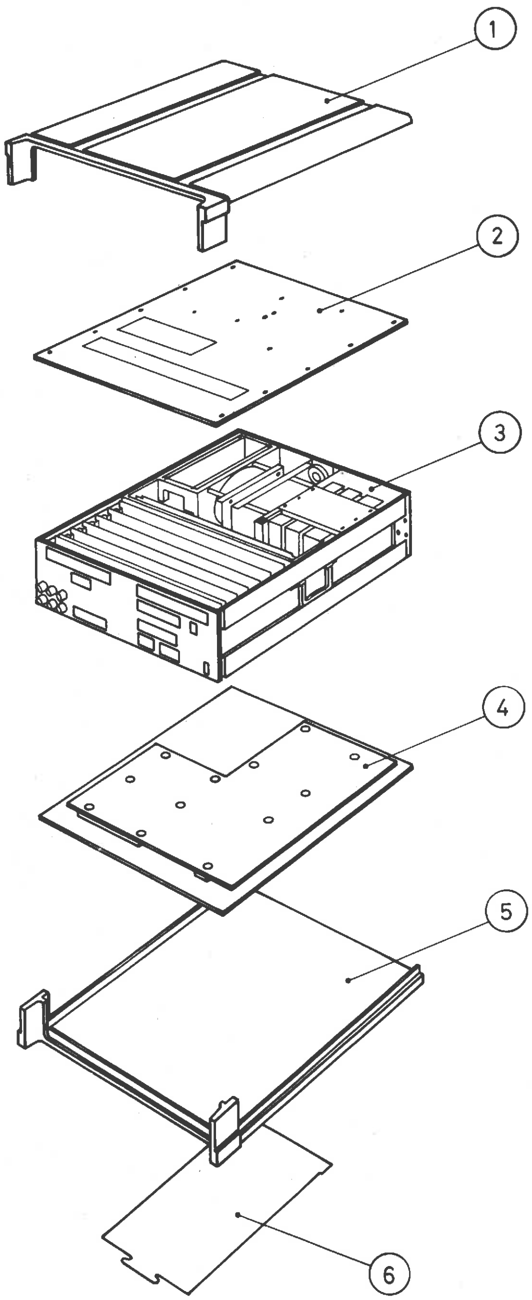
2.4.3 Locating a Blown Fuse

The ultimate causes of blown fuses are so extensive that it is impractical to list them. In many cases the underlying cause, or the blown fuse itself, will activate an electronic protective process which can conceal some of the symptoms.

Fault location in the 4000 should proceed from the primary indications of fault condition (eg failure messages described in section 2.2). These will lead to particular areas of investigation, and at this point the relevant circuit fuses should be checked first. Whether fuses are blown or not, the checks will add to the information available for further diagnosis. Table 2.1 is indexed in PCB Circuit Diagram number order, giving fuse values. The types of fuses to be used can be found in the component lists of Section 6.

Location and Circuit Diagram	Designator/Value	Protected Circuits
Power Input Module 430439	F1 (3A/230V) (6.25A/115V)	(Power Input fuse)
DC PCB		
430445 Sheet 1	F1 1A	Error Amp and 1V Buffer Sense Inputs
Sheet 1	F2 1A	(10V and 1V Buffer outputs (1V and 100mV Attenuators
Sheet 1	F3 1A	100mV Attenuator
Sheet 3	F4 1A)	
Sheet 3	F5 1A}	DC Voltage Circuitry (from excess external voltages)
Sheet 3	F6 1A)	
I/Ω PCB		
430448 Sheet 1	F1 375mA	Not used unless Ext I Option fitted.
Sheet 3	F2 375mA)	Standard resistors (I+ and I- terminal lines)
Sheet 3	F4 375mA)	
Sheet 3	F3 1A	Standard resistors (Hi terminal line)
Sheet 1	F5 2.5A	Current Source (I+ terminal line)
Power Amp (dc) PCB		
430449 Sheet 2	F1 4A)	Line transformer (50V Secondaries)
Sheet 2	F2 4A)	
Sheet 1	F3 4A	Power Amp. Output Stages
Power Supply (In Guard) PCB		
430451 Sheet 1	F1 4A)	Current Option Supply diode bridge and Line transformer secondaries.
Sheet 1	F2 4A)	
Sheet 1	F3 2A)	Common - 2 Supply diode bridge and Line transformer secondaries.
Sheet 1	F4 2A)	
Power Supply (Out Guard) PCB		
430470 Sheet 1	F1 4A	Main Digital Supply Full-wave rectifier and Transformer Secondary.

Table 2.1 Fuse Locations and Purpose



1. TOP COVER
2. TOP GROUND/GUARD ASSEMBLY
3. CHASSIS ASSEMBLY
4. BOTTOM GROUND/GUARD ASSEMBLY
5. BOTTOM COVER
6. INSTRUCTION CARD

FIG. 3.1 OPEN VIEW OF INSTRUMENT

1. DIGITAL PCB ASSEMBLY (BLACK EJECTOR)
2. ANALOG INTERFACE PCB ASSEMBLY (BROWN E
3. REFERENCE DIVIDER PCB ASSEMBLY (RED EJE
4. DC PCB ASSEMBLY (ORANGE EJECTOR)
5. I/Ω LINK PCB (WHEN OPTION 20 NOT FITTED)
6. I/Ω PCB ASSEMBLY (BLUE EJECTOR) (OPTION 2
7. PCB EJECTOR
8. COMMON 2 SCREEN
9. GUARD SHIELD
10. GROUND SHIELD
11. FILTER
12. FILTER GRILLE
13. REAR PANEL ASSEMBLY
14. CHASSIS ASSEMBLY
15. RH EXTRUSION
16. REAR SPACER
17. HANDLE
18. MOTHER PCB ASSEMBLY
19. FRONT PANEL ASSEMBLY
20. FRONT PCB ASSEMBLY
21. LH EXTRUSION

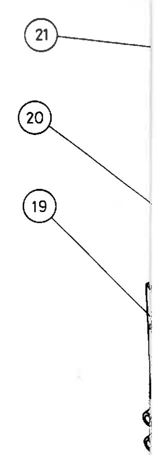


FIG. 3.2 EXPLODED VIEW OF INSTRUMENT (For detai

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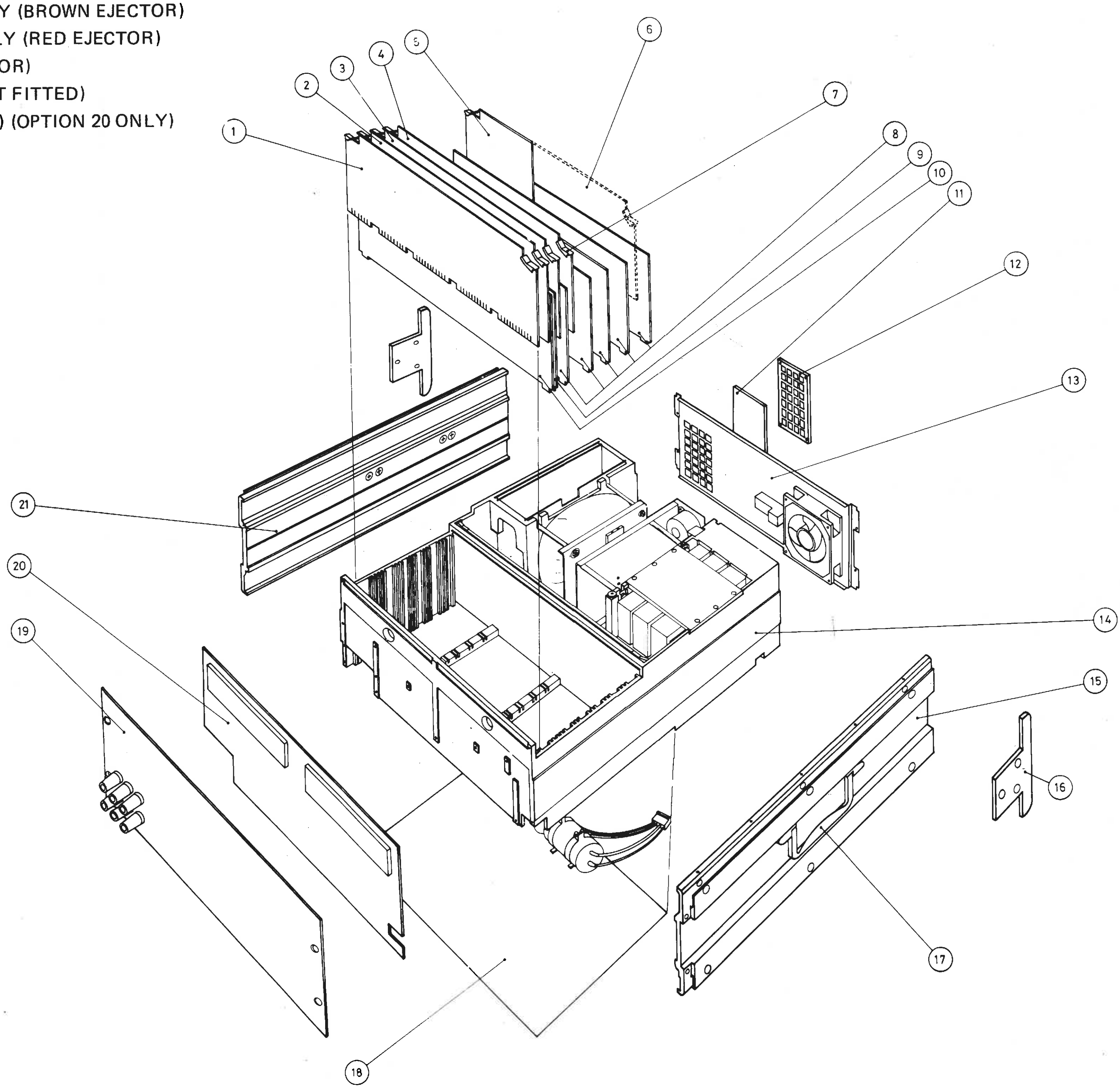
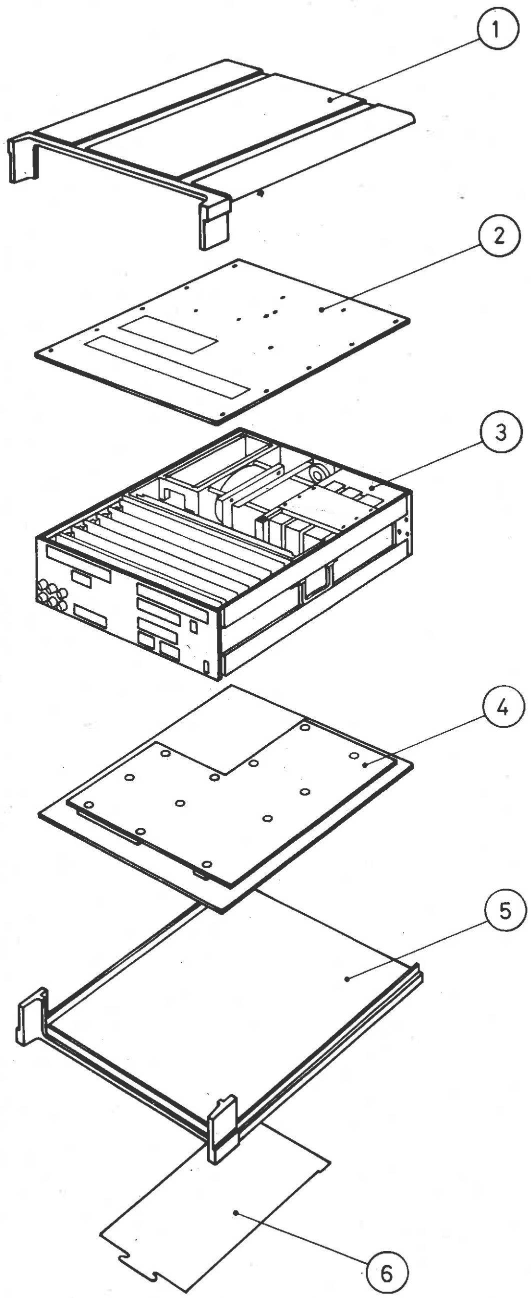
_Y (BROWN EJECTOR)
LY (RED EJECTOR)
TOR)
)T FITTED)
R) (OPTION 20 ONLY)



ENT (For details of Rear Section Components, refer to Fig. 3.3)



1. TOP COVER
2. TOP GROUND/GUARD ASSEMBLY
3. CHASSIS ASSEMBLY
4. BOTTOM GROUND/GUARD ASSEMBLY
5. BOTTOM COVER
6. INSTRUCTION CARD

FIG. 3.1 OPEN VIEW OF INSTRUMENT

1. DIGITAL PCB ASSEMBLY (BLACK EJECTOR)
2. ANALOG INTERFACE PCB ASSEMBLY (BROWN EJE
3. REFERENCE DIVIDER PCB ASSEMBLY (RED EJECT
4. DC PCB ASSEMBLY (ORANGE EJECTOR)
5. I/Ω LINK PCB (WHEN OPTION 20 NOT FITTED)
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7. PCB EJECTOR
8. COMMON 2 SCREEN
9. GUARD SHIELD
10. GROUND SHIELD
11. FILTER
12. FILTER GRILLE
13. REAR PANEL ASSEMBLY
14. CHASSIS ASSEMBLY
15. RH EXTRUSION
16. REAR SPACER
17. HANDLE
18. MOTHER PCB ASSEMBLY
19. FRONT PANEL ASSEMBLY
20. FRONT PCB ASSEMBLY
21. LH EXTRUSION

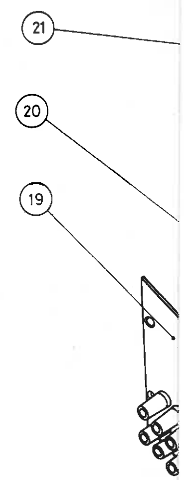

FIG. 3.2 EXPLODED VIEW OF INSTRUMENT (For details o

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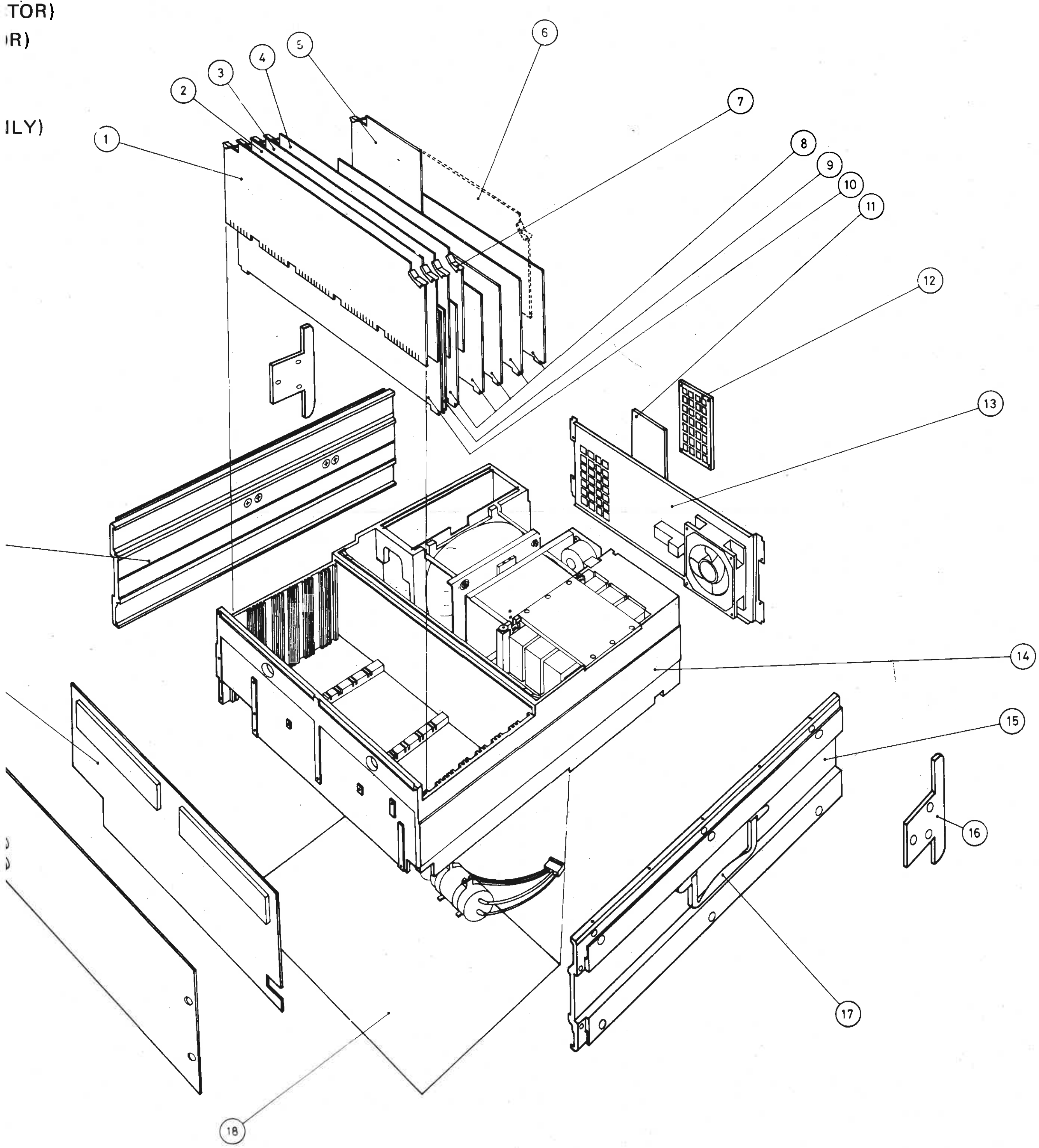


Rear Section Components, refer to Fig. 3.3)

SECTION 3

DISMANTLING AND REASSEMBLY

WARNING

1) ISOLATE FROM POWER SUPPLIES BEFORE DISMANTLING AND REASSEMBLING.
2) REMOVING TOP AND BOTTOM COVERS AND GROUND/GUARD ASSEMBLIES AND THE REAR PANEL ASSEMBLY LEAVES THE MOULDED INTERNAL CHASSIS UNSUPPORTED. THIS CAN CONSTITUTE A SAFETY HAZARD TO BOTH PERSONNEL AND EQUIPMENT.

CAUTION

1) Do not touch the pcb edge connectors with the hands.
2) Ensure no wires are trapped when fitting ground/guard assemblies.

3.1 GENERAL MECHANICAL DESCRIPTION

The 4000 AUTOCAL STANDARD can be used as a bench-top instrument or may be rack mounted in a standard 19" rack. All circuits are housed within a single unit on printed circuit boards, the seven major pcb's being plugged into a "mother" pcb. An open view of the instrument is shown in Fig. 3.1; exploded views are shown in Fig. 3.2 and Fig. 3.3.

3.1.1 Front Panel

Six output terminals with captive, insulated caps are provided; this facility can be fitted to the rear panel at manufacture (Option 41). A printed overlay on the front panel labels all the controls, and retains polarizing filters for the displays.

3.1.2 Rear Panel

The recessed Power Input plug, Power Fuses and Line Voltage Selector are contained in an integral filtered module at the centre of the rear panel.

The Calibration Enable switch (with removable key), and the External reset socket (J53) are mounted directly on the panel between the Power Input module and the cooling-air intake filter. The filter is retained by a grille but is removable for cleaning. At the extreme left of the panel an extractor fan draws the cooling air through the intake filter and internal heat exchangers, finally discharging to atmosphere.

The IEEE488 standard connector socket (J27) and instrument address switch, the Calibration Interval Switch and switch S53 (not used on the 4000); are all mounted on an interconnection pcb assembly. This is fitted on spacers to the inside face of the panel with external components protruding to the rear.

3.1.3 External Construction

Rigid side extrusions together with the front and rear panel assemblies form the basic chassis of the instrument. The side extrusions have handles and rear spacers fitted for bench-top use or are fitted with 'ears' and slides for rack mounting (see User's Handbook, Section 2). The top cover locates into the side extrusions and is secured by screws. The bottom cover is attached in the same way, and includes six domed feet. An operator's instruction card pulls forward from below.

3.1.4 Internal Construction

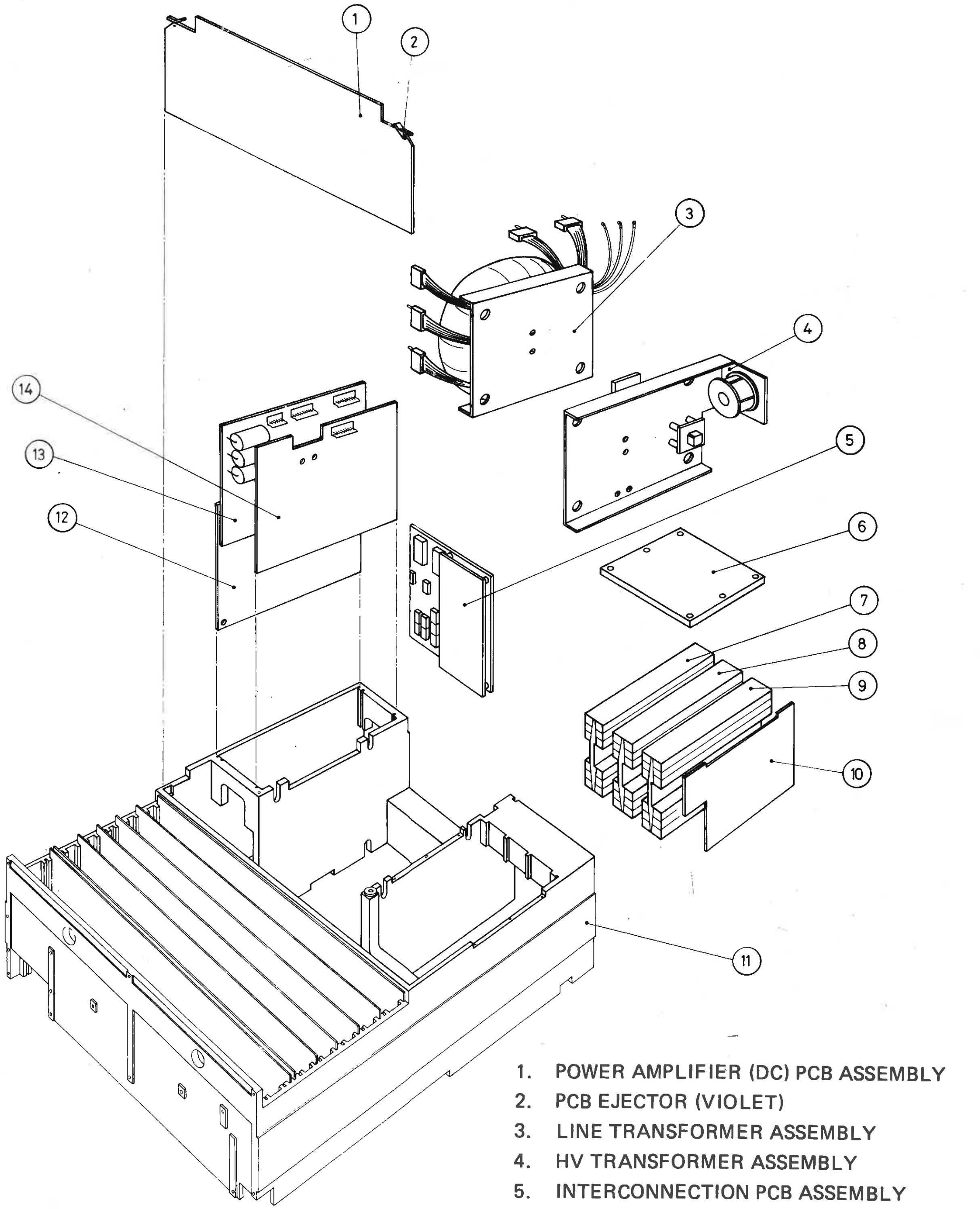
The chassis is enclosed top and bottom by ground and guard assemblies. The upper ground and guard screens allow internal adjustments to be performed without removal. Locations of adjustable components, instructions and warnings are printed on the outer surface.

The interior of the chassis is thermally divided into two compartments. One compartment occupies the forward half of the chassis and is used to house the low power, precision printed circuit boards (pcb's). The rear compartment contains high power components and is air cooled.

The rear compartment is further sub-divided: one houses two power supply pcb's and provides anchorage for the line transformer assembly, these are positioned across the grille of the air intake filter; the other houses three heatsink assemblies, provides anchorage for the HV transformer assembly and ducts the cooling air into the extractor fan. Filtered air is drawn over the power supplies and line transformer, over the power amplifier pcb (which is situated at the front wall of the rear compartment) and through the heatsink assemblies, to be expelled from the instrument by the extractor fan. Guard screens are provided against the outer walls of the power supply sub-compartment and the heatsink compartment.

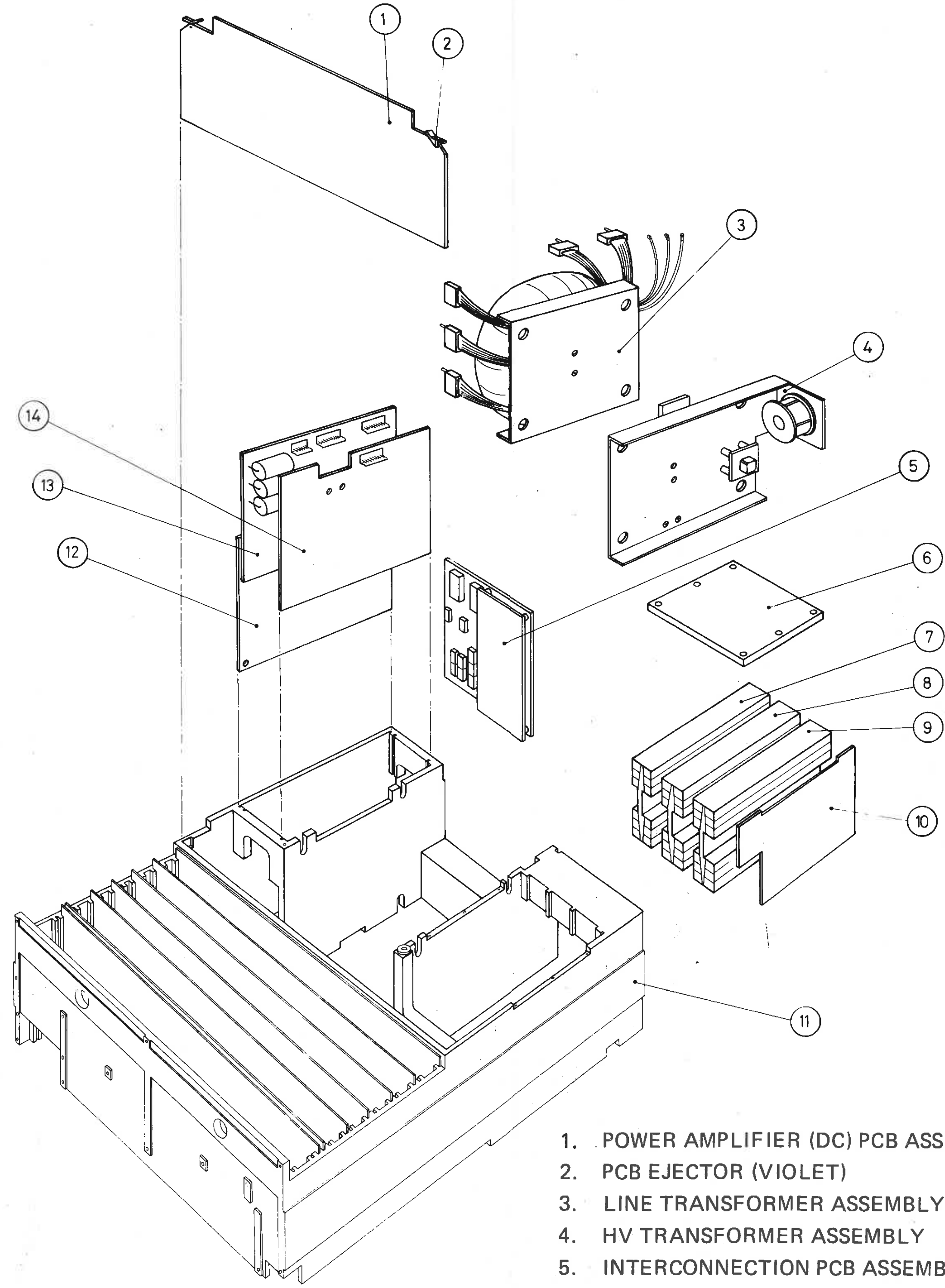
Interconnections between the power amplifier, all forward compartment printed circuit boards and the front pcb assembly are made via a mother pcb. The latter is fitted across the bottom of the forward compartment and out to the front pcb. Four moulded stiffeners keep the mother pcb rigid and provide lateral locating slots for the front compartment printed circuit boards and guard screens. The main printed circuit boards in the forward compartment, the guard screens and the power amplifier pcb fit across the full width of the instrument chassis and slide into vertical slots cut into the moulded chassis. Each pcb edge-connector make electrical contacts with sockets on the mother pcb. The power amplifier also has discrete connectors for high power lines. The front pcb, which carries the display components, connects into the front end of the mother pcb outside the thermally-insulated compartment.

Each printed circuit board has a unique edge connector configuration which prevents incorrect fitting. The printed circuit boards are identified by colour coding of the circuit board ejector levers as shown in Fig. 3.2 and Fig. 3.3.



1. POWER AMPLIFIER (DC) PCB ASSEMBLY
2. PCB EJECTOR (VIOLET)
3. LINE TRANSFORMER ASSEMBLY
4. HV TRANSFORMER ASSEMBLY
5. INTERCONNECTION PCB ASSEMBLY
6. HEATSINK RETAINING PLATE
7. NEGATIVE HEATSINK ASSEMBLY
8. POSITIVE HEATSINK ASSEMBLY
9. POWER SUPPLY/I HEATSINK ASSEMBLY
10. HEATSINK GUARD SCREEN
11. CHASSIS ASSEMBLY
12. POWER SUPPLY GUARD SCREEN
13. IN-GUARD POWER SUPPLY PCB ASSEMBLY
14 OUT-GUARD POWER SUPPLY PCB ASSEMBLY

FIG. 3.3 EXPLODED VIEW OF REAR SECTION



1. POWER AMPLIFIER (DC) PCB ASSEMBLY
2. PCB EJECTOR (VIOLET)
3. LINE TRANSFORMER ASSEMBLY
4. HV TRANSFORMER ASSEMBLY
5. INTERCONNECTION PCB ASSEMBLY
6. HEATSINK RETAINING PLATE
7. NEGATIVE HEATSINK ASSEMBLY
8. POSITIVE HEATSINK ASSEMBLY
9. POWER SUPPLY/I HEATSINK ASSEMBLY
10. HEATSINK GUARD SCREEN
11. CHASSIS ASSEMBLY
12. POWER SUPPLY GUARD SCREEN
13. IN-GUARD POWER SUPPLY PCB ASSEMBLY
14. OUT-GUARD POWER SUPPLY PCB ASSEMBLY

FIG. 3.3 EXPLODED VIEW OF REAR SECTION

3.2 TOP COVER (FIG. 3.1)

3.2.1 Removal

a. Remove the eight M4 x 12mm Socket head countersunk screws from cover.

b. Remove cover by lifting at the front.

3.2.2 Fitting

Reverse procedure of para 3.2.1 (locate cover at rear first, then lower the front).

3.3 BOTTOM COVER (FIG. 3.1)

3.3.1 Removal

a. Invert the instrument.

b. Remove the eight M4 x 12mm Socket head countersunk screws from cover.

c. Remover cover by lifting at the front.

3.3.2 Fitting

Reverse procedure of para 3.3.1 (locate cover at rear first, then lower the front)

3.3.3. Replacing Instruction Card

a. Pull the instruction card forward to its fullest extent.

b. Bow the card and release the rear lugs from the slots.

c. Refit in reverse procedure.

3.4 TOP GROUND/GUARD ASSEMBLY (FIG. 3.1)

3.4.1 Removal

a. Remove top cover (para. 3.2.1).

b. Refer to Fig. 3.4 and remove:

1) from position 'a', ten M4 x 8mm pozi-countersunk screws;

2) from position 'b', six M3 x 6mm pozi-pan screw and M3 shakeproof washers;

3) from position 'c', one M3 x 12mm pozi-pan screw and M3 shakeproof washer.

c. Remove top ground/guard assembly.

3.4.2 Fitting

Reverse procedure of para. 3.4.1.

3.5 BOTTOM GROUND/GUARD ASSEMBLY (FIG. 3.1)

3.5.1 Removal

a. Remove bottom cover (para. 3.3.1).

b. Refer to Fig. 3.5 and remove:

1) from positions 'a', ten M4 x 8mm pozi-countersunk screws;

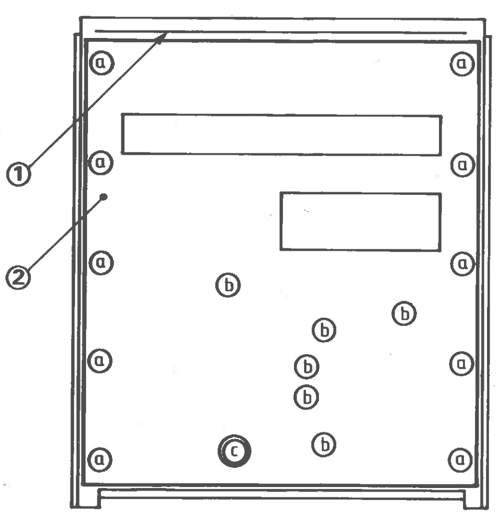
2) from positions 'b', four M3 x 6mm pozi-pan screws and M3 shakeproof washers;

3) from position 'c', one M3 x 12mm pozi-pan screw and M3 shakeproof washer.

c. Remove bottom ground/guard assembly.

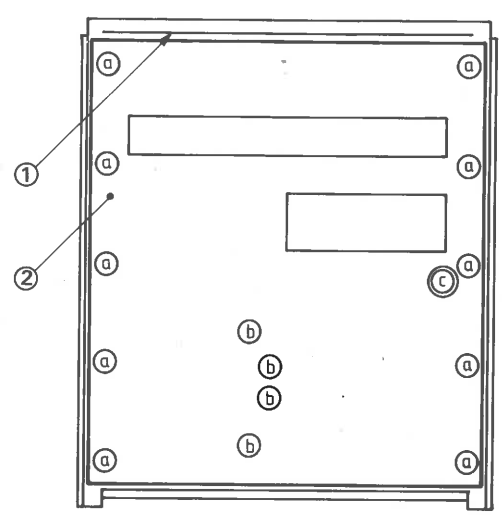
3.5.2 Fitting

Reverse procedure of para 3.5.1.



1. FRONT PANEL ASSEMBLY
2. TOP GROUND/GUARD ASSEMBLY

FIG. 3.4 FITTING TOP GROUND/GUARD



1. FRONT PANEL ASSEMBLY
2. BOTTOM GROUND/GUARD ASSEMBLY

FIG. 3.5 FITTING BOTTOM GROUND/GUARD

NOTE In the procedures 3.6 to 3.20, numbers in parenthesis indicate the call-out number of the referenced diagram.

N.B. Remove top cover (para 3.2) and top ground/guard assembly (para. 3.4) before performing procedures 3.6 to 3.12.

3.6 PCB ASSEMBLIES (FIG. 3.2)

DIGITAL (1)	DC (4)
ANALOG INTERFACE (2)	I/Ω LINK (5) (when option 20 not fitted)
REFERENCE DIVIDER (3)	I/Ω (6) (option 20 only)

3.6.1 Removal

a. Ensure instrument power is OFF.

b. Identify the pcb assembly to be removed (see table 3.1).

c. Place the thumb of each hand under the lip of the two pcb ejectors (7) on the pcb assembly to be removed.

d. Gently pull the pcb ejectors upwards and outwards to release the pcb edge connectors.

NOTE The I/Ω Link pcb has only one pcb ejector. To remove this pcb, grip the top edge of the pcb and pull gently while moving the pcb ejector lever upwards.

e. Remove the pcb.

3.6.2 Fitting

a. Ensure instrument power is OFF.

b. Identify the chassis location of the pcb assembly to be fitted (see table 3.1).

NOTE The single ejector of the I/Ω link pcb locates to the 'BLU' identifier of the chassis.

c. Ensure the pcb ejectors are in the 'down' position.

d. Insert the pcb sides into the respective slots in the side walls of the chassis.

e. Allow the pcb to slide down to the mother pcb, then press home by gently pushing down on the ejectors.

PCB ASSEMBLY	EJECTOR COLOUR	MAIN CHASSIS PCB IDENTIFIER	COMPONENT SIDE TO FACE:
Digital	black	BLK	rear
Analog Interface	brown	BRN	front
Reference Divider	red	RED	rear
DC	orange	ORG	rear
Not fitted	—	YEL	—
Not fitted	—	GRN	—
I/Ω Link	blue	BLU	—
I/Ω	blue	BLU	rear
Power Amplifier	violet	VLT	rear

TABLE 3.1 LOCATION AND ORIENTATION OF PCB ASSEMBLIES

3.7 COMMON-2 SCREENS, GUARD SHIELD AND GROUND SCREEN

NOTE These items are interchangeable, designation is according to location as shown at (8), (9) & (10), Fig. 3.2.

3.7.1 Removal

Grip the plate and slide out from chassis.

3.7.2 Fitting

NOTE Each plate mates with a miniature connector on the mother pcb adjacent to the side wall of the chassis. Do not touch the connecting edge of the plate.

a. Insert the plate into the respective slots in the side walls of the chassis (orientation is not important).

b. Allow the plate to slide down to the mother pcb, then gently press home.

3.8 POWER AMPLIFIER (DC) PCB ASSEMBLY (FIG. 3.6)

3.8.1 Removal

CAUTION. Do not pull on the connector wires.

a. Disconnect the six connectors (1), (2), (4), (5), (6) and (7) from the pcb (8).

NOTE Some resistance to movement will be felt from the locking clips of the connector bases.

b. Fold back the connectors and wires clear of the pcb (8).

c. Place the thumb of each hand under the lip of the two pcb ejectors (3).

d. Gently pull the pcb ejectors upwards and outwards to release the pcb edge connectors.

e. Remove the pcb.

3.8.2 Fitting

a. Ensure all wires and connectors are clear of the pcb area.

b. Insert the pcb sides into the respective plots in the side walls of the chassis; pcb component side facing the rear of the instrument.

c. Allow the pcb to slide down to the mother pcb taking care not to trap any wires.

d. Ensure the pcb ejectors (3) are in the 'down' position then press the pcb home by gently pushing down on the ejectors.

e. Identify and fit the six connectors (1), (2), (4), (5), (6) and (7) as shown in Fig. 3.6, with reference to the legend.

3.9 IN-GUARD POWER SUPPLY PCB ASSEMBLY (FIG. 3.6)

3.9.1 Removal

CAUTION. Do not pull on the connector wires.

a. Disconnect the three connectors (10), (11) and 13 from the pcb (9).

NOTE. Some resistance to movement will be felt from the locking clips of the connector bases.

b. Fold back the connectors and wires clear of the pcb (9).

c. Grip the top edge of the pcb and pull gently from the chassis.

d. Remove the pcb.

3.9.2 Fitting

a. Ensure all wires and connectors are clear of the pcb area.

b. Insert the pcb sides into the respective slots in the chassis sub-compartment.

c. Allow the pcb to slide down to the miniature connectors on the chassis, taking care not to trap any wires.

d. Press the pcb home by gently pushing the top edge of the pcb.

e. Identifv and fit the three connectors (10), (11) and (13) as shown in Fig. 3.6, with reference to the legend.

3.10 OUT-GUARD POWER SUPPLY PCB ASSEMBLY (FIG. 3.6)

3.10.1 Removal

CAUTION. Do not pull on the connector wires.

a. Disconnect the three connectors (10), (11) and (13) from pcb (9), and connector (17) from pcb (15).

NOTE. Some resistance to movement will be felt from the locking clips of the connector bases.

b. Fold back the connectors and wires clear of the pcb (15).

c. Grip the top edge of the pcb and pull gently from the chassis.

3.10.2 Fitting

a. Ensure all wires and connectors are clear of the pcb area.

b. Insert the pcb sides into the respective slots in the chassis sub-compartment.

c. Allow the pcb to slide down to the miniature connectors on the chassis, taking care not to trap any wires.

d. Press the pcb home by gently pushing the top edge of the pcb.

e. Identify and fit the three connectors (10), (11) and (13) to pcb (9) and connector (17) to pcb (15) as shown in Fig. 3.6, with reference to the legend.

3.11 HEATSINK ASSEMBLIES (FIG. 3.6)

3.11.1 Removal

a. Remove the six M3 x 12mm pozi-countersunk screws from the heatsink retaining plate (21).

b. Remove the heatsink retaining plate (21).

NOTE. Although the heatsink assemblies are discrete items, removal is simplified when performed in the following order.

1. Negative heatsink assembly (25);
2. Positive heatsink assembly (24);
3. Power supply/I heatsink assembly (23);

when disconnecting connectors, some resistance to movement will be felt from the locking clips of the connector bases.

CAUTION. Do not pull on the connector wires.

c. 1) Disconnect connector (6) from the power amplifier (dc) pcb assembly (8).

   2) Remove negative heatsink assembly (25).

d. 1) Disconnect connector (5) from the power amplifier (dc) pcb assembly (8).

   2) Remove positive heatsink assembly (24).

e. 1) Disconnect connector (4) from the power amplifier (dc) pcb assembly (8).

   2) Disconnect connector (22) from the mother pcb.

   3) Disconnect connector (10) from the in-guard power supply pcb assembly (9).

   4) Remove power supply/I heatsink assembly (23).

3.11.2 Fitting

Reverse procedure of para. 3.11.1.

WARNING. Ensure rear panel assembly is fitted before removing top and bottom covers and ground/guard assemblies. Refer to warning 2 at start of Section 3.

3.12 HV TRANSFORMER ASSEMBLY (FIG. 3.6)

N.B. Remove top cover (para. 3.2), top ground/guard assembly (para. 3.4), bottom cover (para. 3.3) and bottom ground/guard assembly (para. 3.5) before performing para. 3.12 and para. 3.13.

3.12.1 Removal

a. Remove positive heatsink assembly (24) and negative heatsink assembly (25) (see para. 3.11.1).

b. Disconnect connector (7) from the power amplifier (dc) pcb assembly (8).

c. Turn the instrument to stand on its right hand side (on R.H. extrusion (15), Fig. 3.2).

d. Remove the HV transformer assembly (19).

3.12.2 Fitting

Reverse procedure of para. 3.12.1 and refer to Fig. 3.7 for reassembly of items to the M8 transformer bolts.

3.13 LINE TRANSFORMER ASSEMBLY (FIG. 3.6)

3.13.1 Removal

a. Remove the in-guard and out-guard power supply pcb assemblies (9) and (15) (see paras 3.9 and 3.10).

b. Turn the instrument to stand on its left side (on L.H. extrusion (21), Fig. 3.2).

c. Disconnect connector (1) from the power amplifier (dc) pcb assembly (8).

d. Disconnect the line transformer 4-way connector from the interconnection pcb assembly (5), Fig. 3.3) fixed on the rear panel.

e. Release the four M8 x 110mm bolts, washers and nylock nuts.

f. Remove the M3 x 8mm pozi-countersunk screw, M3 steel nut and shakeproof washer which secure the solder tag terminals of four ground wires. Fold back the wire which is fitted to the rear panel assembly.

g. Remove the line transformer assembly.

3.13.2 Fitting

Reverse procedure of para. 3.13.1, and refer to Fig. 3.7 for reassembly of items to the M8 transformer bolts.

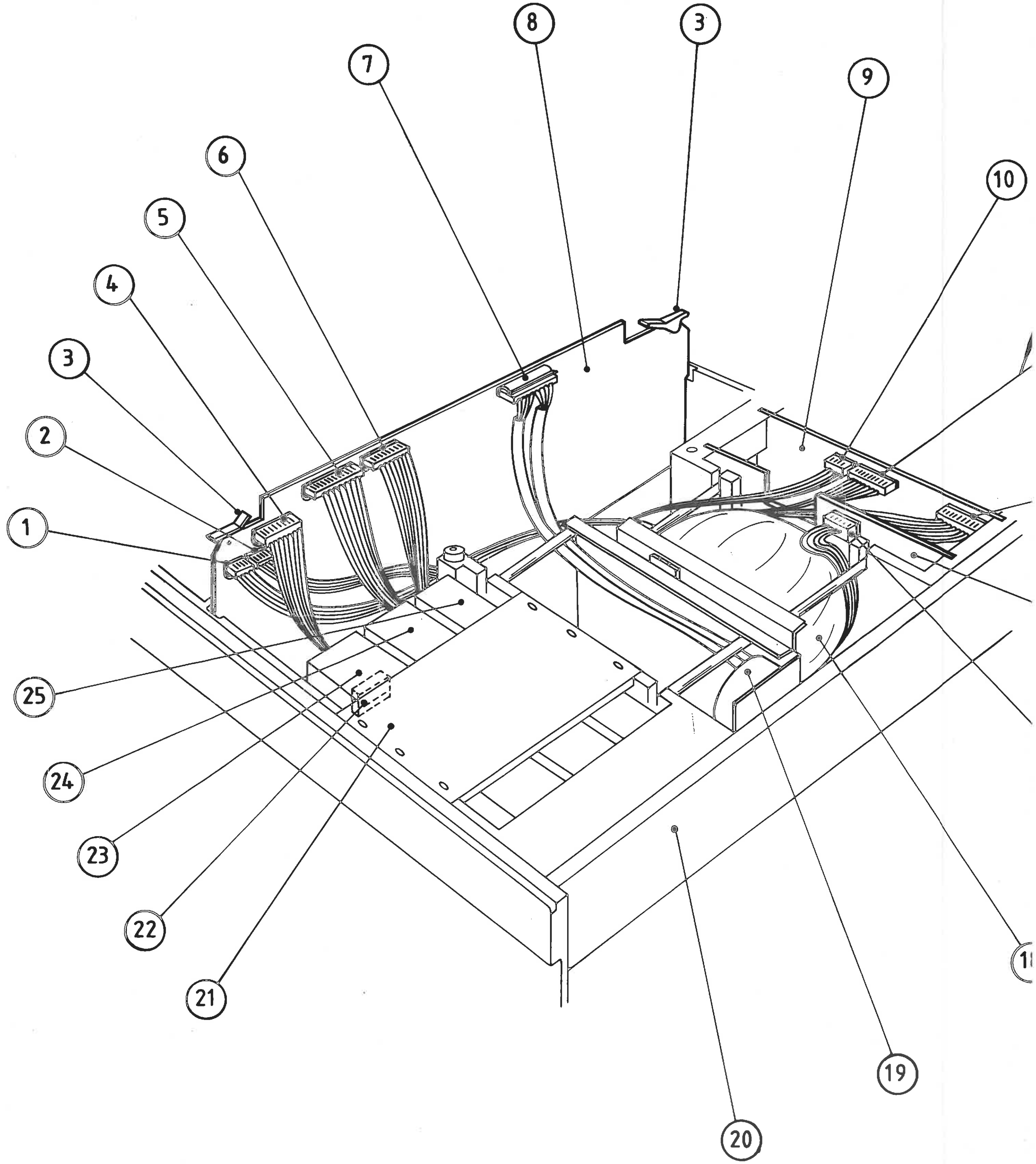
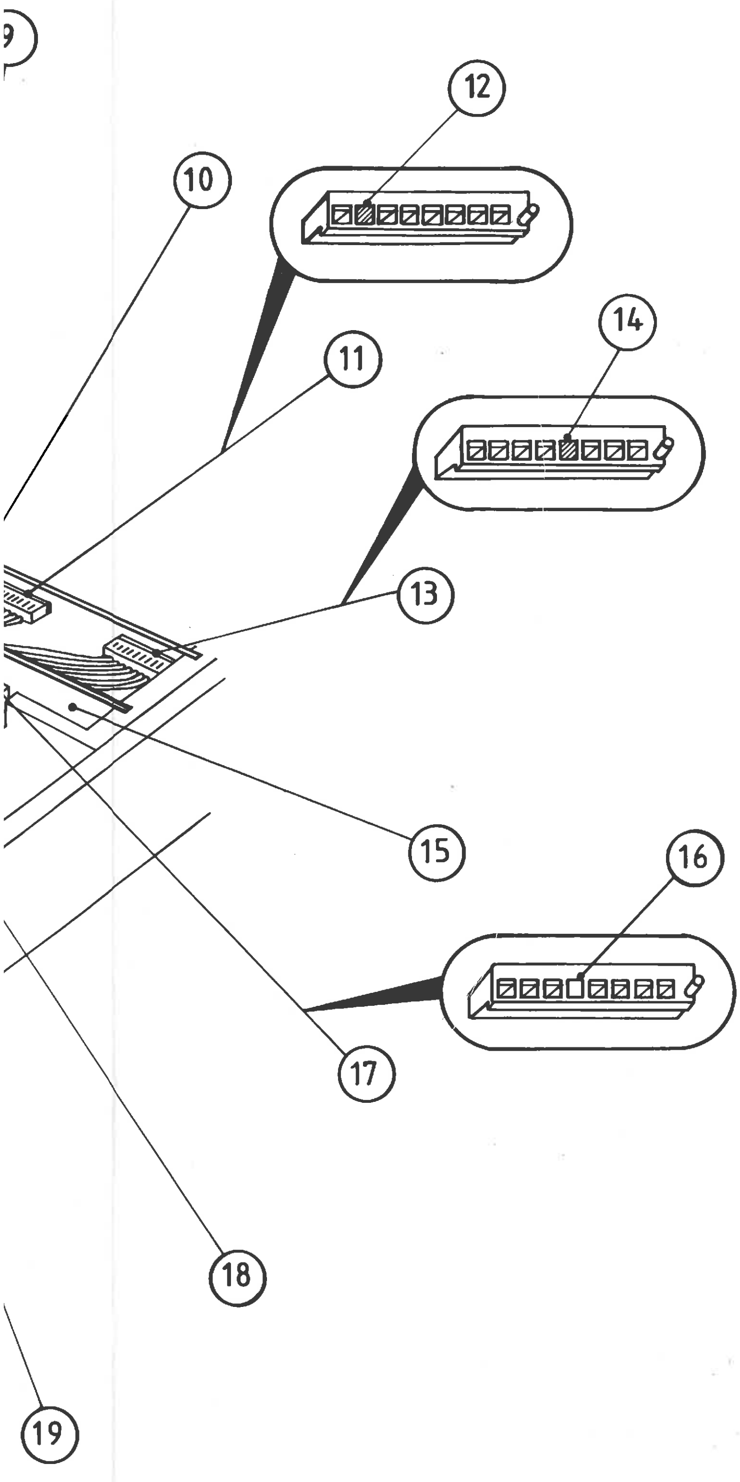
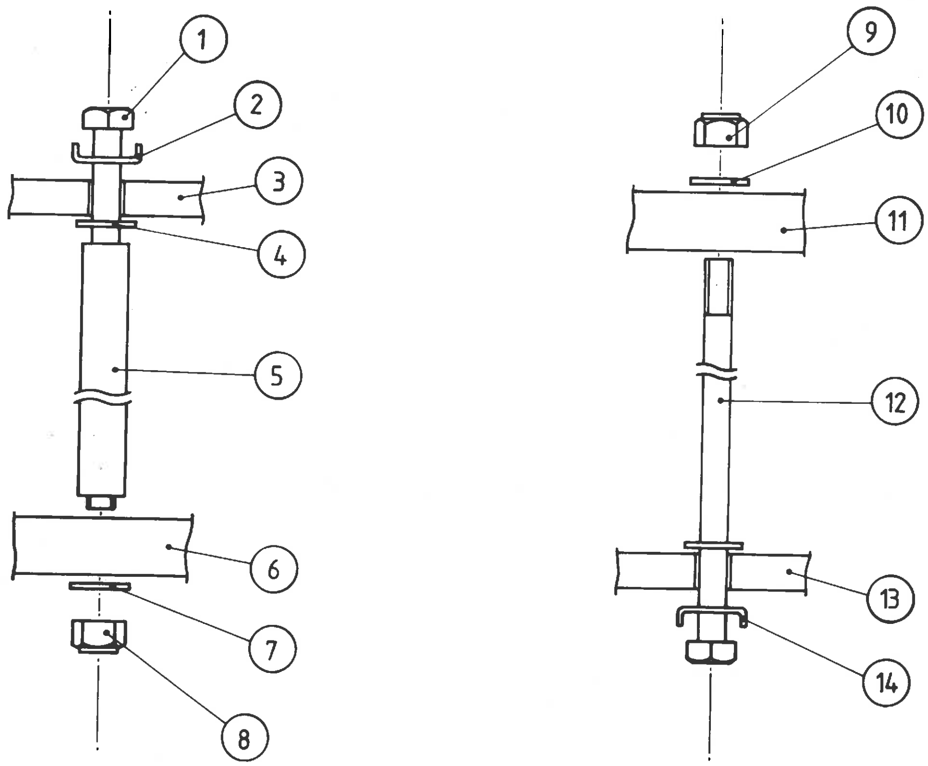


FIG. 3.6 CONNECTION DETAILS OF REAR C



1. CONNECTOR J5, 4-WAY WITH LOCATING PIN, CARRIES FOUR WIRES FROM LINE TRANSFORMER ASSEMBLY.
2. CONNECTOR J4, 4-WAY, NO LOCATING PIN- CARRIES FOUR WIRES FROM CAPACITORS ON MOTHER PCB.
3. PCB EJECTOR (VIOLET)
4. CONNECTOR J3, 8-WAY WITH LOCATING PIN. CARRIES EIGHT WIRES FROM POWER SUPPLY/I HEATSINK ASSEMBLY (20)
5. CONNECTOR J1, 12-WAY WITH LOCATING PIN. CARRIES EIGHT WIRES FROM POSITIVE HEATSINK ASSEMBLY (21)
6. CONNECTOR J2, 8-WAY WITH LOCATING PIN. CARRIES SEVEN WIRES FROM NEGATIVE HEATSINK ASSEMBLY (22)
7. CONNECTOR J6, 12-WAY WITH LOCATING PIN. CARRIES WIRES OF TWO CABLES FROM HV TRANSFORMER ASSEMBLY (16)
8. POWER AMPLIFIER (DC) PCB ASSEMBLY
9. IN-GUARD POWER SUPPLY PCB ASSEMBLY
10. CONNECTOR J1, 4-WAY WITH LOCATING PIN. CARRIES TWO WIRES FROM POWER SUPPLY/ I HEATSINK ASSEMBLY (20).
11. CONNECTOR J2, 8-WAY WITH SIX-BLANK-ONE PIN GROUPING FROM LOCATING PIN. CARRIES SEVEN WIRES FROM LINE TRANSFORMER ASSEMBLY (15)
12. PLASTIC BLANKING PLUG
13. CONNECTOR J3, 8-WAY WITH THREE-BLANK-FOUR PIN GROUPING FROM LOCATING PIN. CARRIES SEVEN WIRES FROM LINE TRANSFORMER ASSEMBLY (15)
14. PLASTIC BLANKING PLUG
15. OUT-GUARD POWER SUPPLY PCB ASSEMBLY
16. SPACE (NO SOCKET TERMINAL FITTED)
17. CONNECTOR J3, 8-WAY WITH FOUR-SPACE-THREE PIN GROUPING FROM LOCATING PIN. CARRIES SEVEN WIRES FROM LINE TRANSFORMER ASSEMBLY (15)
18. LINE TRANSFORMER ASSEMBLY
19. HV TRANSFORMER ASSEMBLY
20. REAR PANEL ASSEMBLY
21. HEATSINK RETAINING PLATE
22. CONNECTOR J19 (MOTHER PCB), 7-WAY CARRIES WIRES FROM POWER SUPPLY/I HEATSINK ASSEMBLY
23. POWER SUPPLY/I HEATSINK ASSEMBLY 400455
24. POSITIVE HEATSINK ASSEMBLY 400454
25. NEGATIVE HEATSINK ASSEMBLY 400461

)ETAILS OF REAR COMPARTMENT ASSEMBLIES



a. HV TRANSFORMER BOLT

1. M8 x 100mm BOLT
2. TRANSFORMER BOLT PLATE
3. MOULDED CHASSIS (PART)
4. M8 FLAT STEEL WASHER
5. CLEAR SPACER
6. HV TRANSFORMER ASSY (PART)
7. M8 FLAT STEEL WASHER
8. M8 NYLOCK NUT

b. LINE TRANSFORMER BOLT

9. M8 NYLOCK NUT
10. M8 FLAT STEEL WASHER
11. LINE TRANSFORMER ASSY (PART)
12. M8 x 110mm BOLT
13. MOULDED CHASSIS (PART)
14. TRANSFORMER BOLT PLATE

FIG. 3.7 RE-ASSEMBLY OF TRANSFORMER BOLTS

3.14 REAR PANEL ASSEMBLY (FIG. 3.8)

3.14.1 Removal

WARNING. DO NOT REMOVE THE REAR PANEL ASSEMBLY WHEN TOP AND BOTTOM COVERS AND GROUND/GUARD ASSEMBLIES ARE REMOVED. REFER TO WARNING 2 AT START OF SECTION 3.

N.B. Rear panel-mounted components are accessed by releasing the rear panel assembly and moving it away from the chassis to the extent allowed by internal wiring connections. Perform this operation (para. 3.14) with top and bottom covers and ground/guard assemblies fitted, or with AT LEAST the top OR bottom ground/guard assembly fitted. This procedure provides access to rear panel-mounted components; it does not provide for complete removal of the rear panel assembly.

a. Remove the six screws (10).
b. Remove the two rear spacers (9).
c. Remove the four screws (11).
d. Remove filter grille (12) and filter (13).
e. Remove screw (6) and the screw from position (4).
f. Remove the four screws (8).

CAUTION. Do not stress the wires.

g. Gently pull away the rear panel assembly (1) away from the chassis (3) to the extent allowed by the wiring.

3.14.2 Fitting

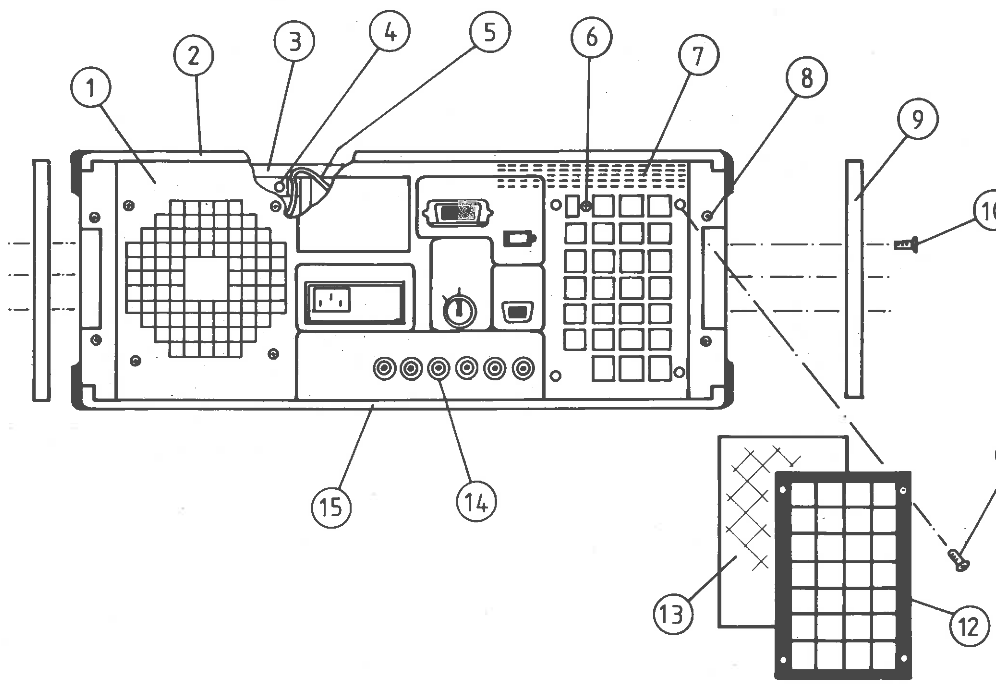
a. Press the rear panel assembly (1) to the chassis (3) whilst ensuring that:

1) The wires (5) lay in the cut-out in the moulded internal chassis;

2) The ribbon cables (7) fit in the recess in the moulded internal chassis;

3) All other wires are free and not trapped by the rear panel assembly.

b. Fit screws, filter, filter grille and rear spacers, reversing the procedure of para. 3.14.1.



1. REAR PANEL ASSEMBLY
2. TOP COVER
3. MOULDED INTERNAL CHASSIS
4. POSITION FOR M3 x 6mm POZI-PAN SCREW AND M3 SHAKEPROOF WASHER
5. WIRES FROM FAN PASSING THROUGH CUT-OUT IN MOULDED INTERNAL CHASSIS
6. M3 x 6mm POZI-PAN SCREW AND M3 SHAKE-PROOF WASHER
7. RIBBON CABLES FIT IN RECESS IN MOULDED INTERNAL CHASSIS
8. M4 x 8mm TAPTITE SCREW IN FOUR POSITIONS
9. REAR SPACER
10. M4 x 12mm SOCKET HEAD COUNTERSUNK SCREW IN SIX POSITIONS
11. M3 x 10mm POZI-COUNTERSUNK SCREW IN FOUR POSITIONS
12. FILTER GRILLE
13. FILTER
14. OUTPUT TERMINALS (WHEN REAR-PANEL MOUNTED)
15. BOTTOM COVER

FIG. 3.8 REMOVAL OF REAR PANEL ASSEMBLY

3.15 FRONT PANEL ASSEMBLY

1. RED, BLACK, WHITE, BLUE AND BROWN – CODED TERMINALS
2. TERMINAL COLOUR CODE
3. WRAP SOLDER JOINT FOR RED, WHITE AND BLUE WIRES
4. } METHOD NOT USED ON 4000
5. }
6. SPECIAL SOLDER TAG
7. SPACER
8. WASHER
9. NUT
10. NUT
11. SOLDER TAG
12. GREEN/YELLOW WIRE
13. GREEN – CODED TERMINAL
14. METHOD NOT USED ON 4000
15. SECTION OF PANEL

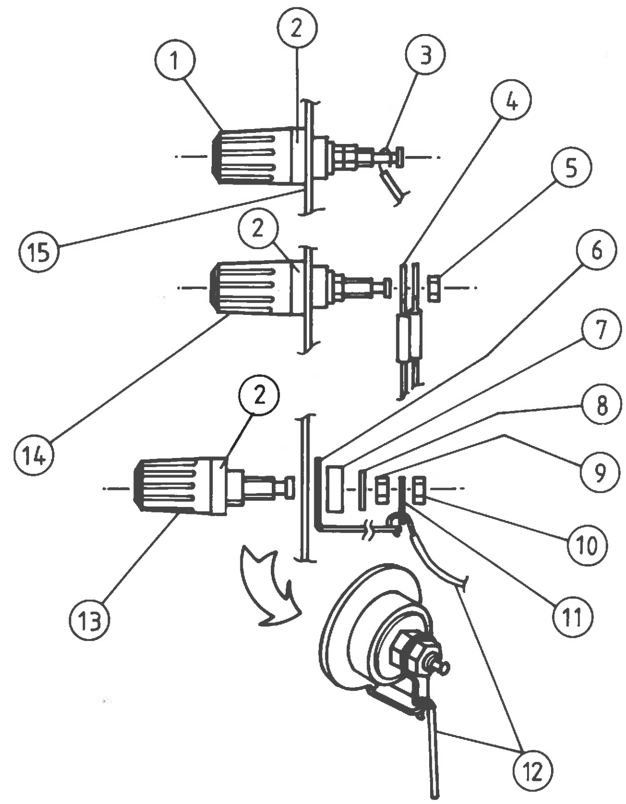


FIG. 3.9 DISMANTLING/REASSEMBLY OF TERMINALS

1. BRACKET
2. MOTHER PCB
3. RED WIRE TO BROWN-CODED 1 + TERMINAL
4. BLUE WIRE TO BLUE-CODED I – TERMINAL
5. RED WIRE TO BROWN-CODED I + TERMINAL
6. BLUE WIRE TO BLACK-CODED LO TERMINAL
7. } WHITE WIRES TO WHITE-CODED TERMINAL
8. }
9. GREEN/YELLOW WIRE TO GREEN-CODED TERMINAL

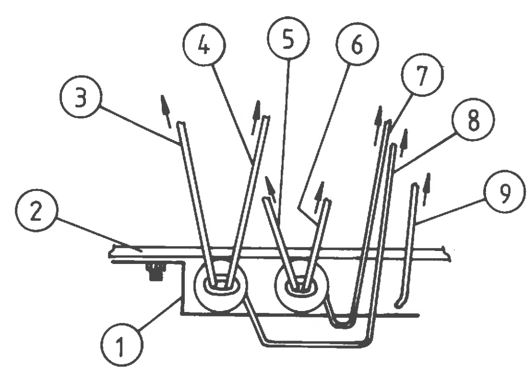


FIG. 3.10 FRONT PANEL ASSEMBLY TERMINAL WIRING

3.15.1 Removal

N.B. Remove top cover (para. 3.2) and bottom cover (3.3) before performing the following procedure.

a. Remove the four M4 x 8mm taptite screws from the front panel assembly.

CAUTION. Do not stress the wires.

NOTE. Steps b. and c. do not apply when output terminals are rear panel-mounted.

b. Move the front panel assembly away from the chassis to the extent allowed by the wires to the output terminals.

c. Referring to Fig. 3.9

1) Unsolder the wrap joints (3) and remove the red, black, white, blue and brown-coded terminals (1).

2) Remove nut (10) from green-coded terminal (13); ease soldertag (11) from the terminal taking care not to strain the connection with wire (12) and special solder tag (6); remove nut (9) washer (8) and spacer (7); removal special solder tag (6), together with solder tag (11) and green/yellow wire (12); reassemble items (7), (8), (9) and (10) to the terminal.

d. Remove the front panel assembly.

3.15.2 Fitting

Reverse the procedure of para. 3.15, referrring to Fig. 3.10 for terminal wiring identities, and to Fig. 3.9 for terminal connection methods.

3.16 FRONT PCB ASSEMBLY (FIG. 3.11)

3.16.1 Removal

a. Remove front panel assembly (para. 3.15.1)

b. Remove two screws (4), together with two shakeproof washers (5) and four plain washers (6).

c. Fold the power switch (3) and its cable clear of the pcb (1).

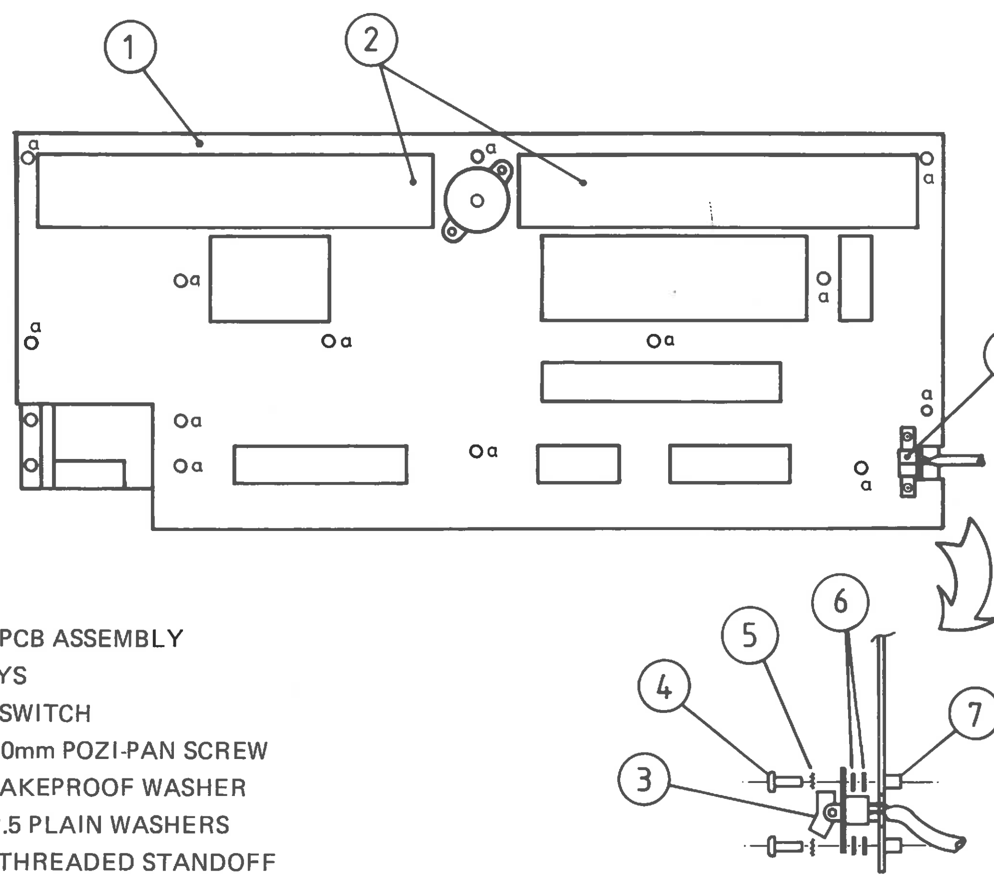
d. Remove the M3 x 6mm pozi-pan screws from 13 positions on the circuit board (1), marked 'a' on Fig. 3.11.

e. Ease the lower edge away of pcb (1) away from the mother pcb to disengage the mating connectors.

f. Remove the pcb.

3.16.2 Fitting

Reverse the procedure of para. 3.16.1. Ensure all mating connectors are fully engaged and that the surfaces of displays (2) are clean.



1. FRONT PCB ASSEMBLY
2. DISPLAYS
3. POWER SWITCH
4. M2.5 x 10mm POZI-PAN SCREW
5. M2.5 SHAKEPROOF WASHER
6. TWO M2.5 PLAIN WASHERS
7. FIXED, THREADED STANDOFF

FIG. 3.11 REMOVAL AND FITTING OF FRONT PCB ASSEMBLY

SECTION 4

TECHNICAL DESCRIPTION

4.1 PRINCIPLES OF OPERATION (FIG. 4.1)

SIMPLIFIED FUNCTIONAL DIAGRAM

FIG. 4.1 illustrates the general circuit division and signal flow within the 4000.

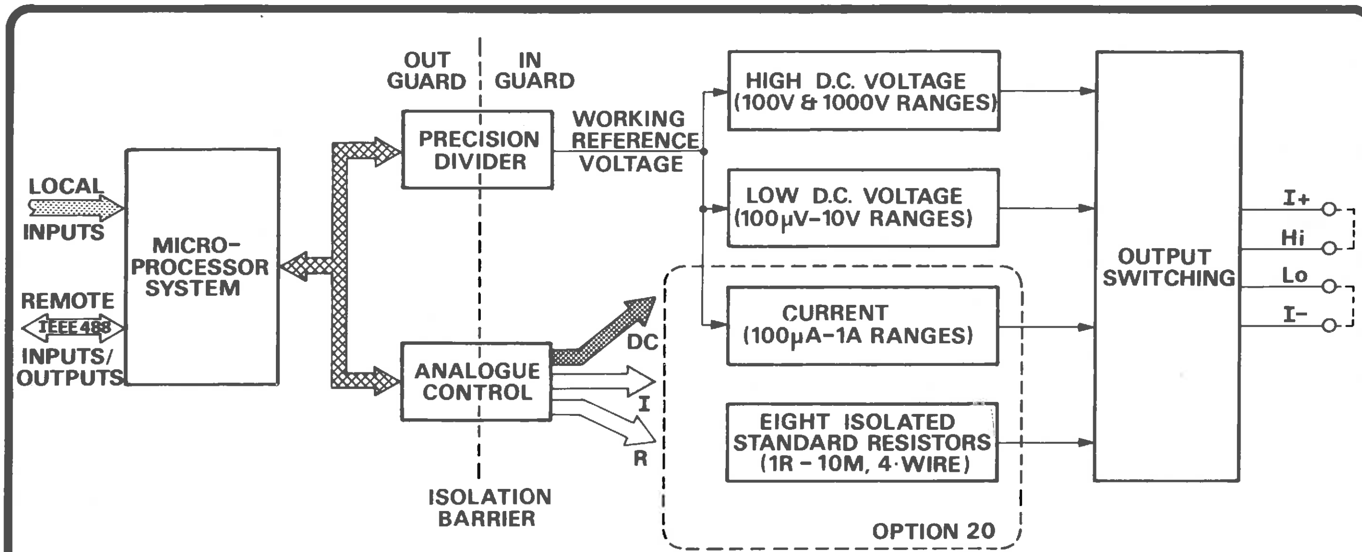


Fig. 4.1 4000 SIMPLIFIED BLOCK DIAGRAM

4000 BLOCK DIAGRAM

FIG. 4.2 (overleaf) breaks the main functional division down into smaller blocks. It can be thrown clear of the handbook to provide a functional overview and index to other subsections of section 4.

4.1.1 Inputs

The microprocessor system accepts inputs from two main sources:

(i) The front panel keyboard provides local control inputs.

(ii) The IEEE 488 bus system provides remote control inputs.

The microprocessor system outputs digital information to two main areas:

(i) The precision divider which is used in setting the terminal output.

(ii) Various decoding circuitry which controls function and range selection.

4.1.2 Precision Divider

The circuit produces a DC voltage, called the "Working Reference", which can be accurately set between 0 and ± 20V. It is divided into two main areas:

(i) The period division comparator, outside guard, consists of a comparator and a binary counter, both 25 bits. The comparator is set by data from the microprocessor system and the counter is driven by a crystal-controlled clock. When the binary count matches the data set in the comparator, a switching pulse (reset) is produced. The binary counter continues to overflow point when a second switching pulse (set) is produced. In this way, accurately variable mark-space timing is generated.

(ii) The switching integrator receives the pulses across guard. They are used to drive a solid state switch which chops the output from a very stable 20V DC Master Reference. This in turn produces a square wave which is very accurately defined both in period and amplitude. This resultant square wave is integrated by an active low-pass filter with high rejection at the chopping frequency, to finally produce the 0 — ± 20V Working Reference.

4.1.3 Analogue Control

The analogue circuitry is controlled by data held in a 48 bit in-guard latch. The microprocessor regularly updates the latch contents, using a serial link to pass the data (through opto-isolators) across the isolation barrier.

4.1.4 Low Voltage Output

The basic range of the 4000 is ± 10V (± 19.999,999 FS). This is a buffered output derived directly from the Working Reference. All lower voltage outputs are produced by additional buffers and precision attenuators.

4.1.5 High Voltage Output

Outputs on the 100V and 1kV ranges are produced using an AC Voltage Amplifier/Rectifier system.

The Working Reference is used to control the amplitude of a sine wave output from a voltage controlled amplifier. This drives an AC step-up transformer via a Power Amplifier, which after rectification and filtering produces the high voltage DC outputs.

4.1.6 Current Ouput (Option 20)

For Current outputs the Working Reference is switched to drive a voltage-to-current convertor. The various ranges are selected by digital control signals from the microprocessor system.

4.1.7 Resistance Output (Option 20)

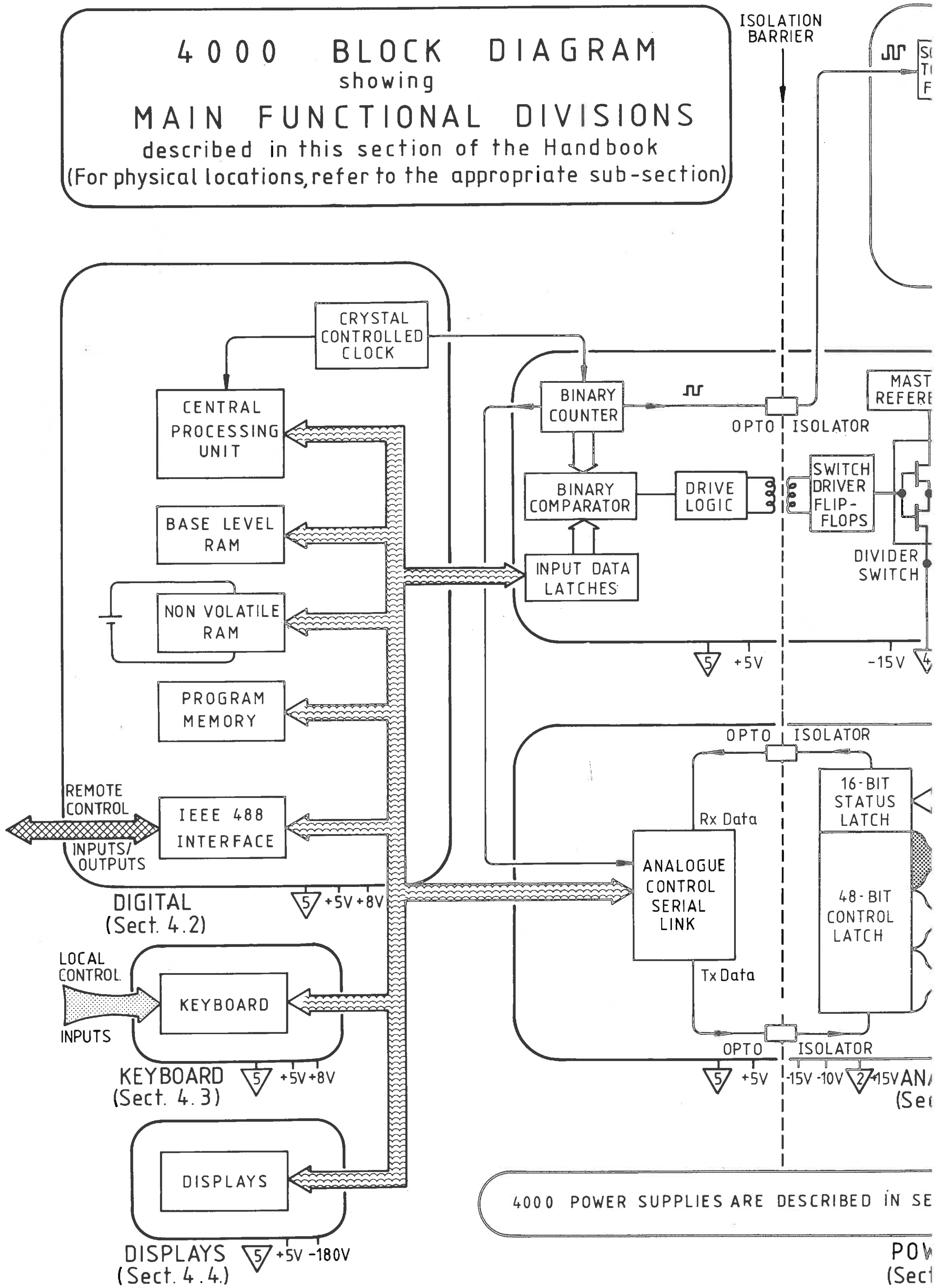
For resistance outputs a range of eight fixed-value precision resistors are fitted. They are fully floating and selected by relays under control of digital signals from the microprocessor system.

4.1.8 Model 4000A — Features Additional to Model 4000

The following features extend the 4000A DC Voltage and Current specifications to 23°C ± 5°C.

(1) Buffer M2 on the Reference PCB (400452) is temperature-compensated. Refer to Section 4.6.4.1.

(2) On the DC PCB Assembly (400445), the 100mV, 1V and 100V/1000V range precision attenuators are uprated. Refer to Sections 4.7.8.1 and 4.8.10.1.



4000 BLOCK DIAGRAM
showing
MAIN FUNCTIONAL DIVISIONS
described in this section of the Handbook
(For physical locations, refer to the appropriate sub-section)
ISOLATION BARRIER
CRYSTAL CONTROLLED CLOCK
CENTRAL PROCESSING UNIT
BASE LEVEL RAM
NON VOLATILE RAM
PROGRAM MEMORY
REMOTE CONTROL
INPUTS/ OUTPUTS
IEEE 488 INTERFACE
DIGITAL (Sect. 4.2)
+5V +8V
LOCAL CONTROL
INPUTS
KEYBOARD
KEYBOARD (Sect. 4.3)
+5V +8V
DISPLAYS
DISPLAYS (Sect. 4.4.)
+5V -180V
BINARY COUNTER
BINARY COMPARATOR
INPUT DATA LATCHES
DRIVE LOGIC
OPTO ISOLATOR
SWITCH DRIVER FLIP-FLOPS
MAST REFER
DIVIDER SWITCH
+5V
-15V
OPTO ISOLATOR
Rx Data
ANALOGUE CONTROL SERIAL LINK
Tx Data
16-BIT STATUS LATCH
48-BIT CONTROL LATCH
OPTO ISOLATOR
+5V
-15V -10V
+15V
4000 POWER SUPPLIES ARE DESCRIBED IN SE

Fig. 4.2

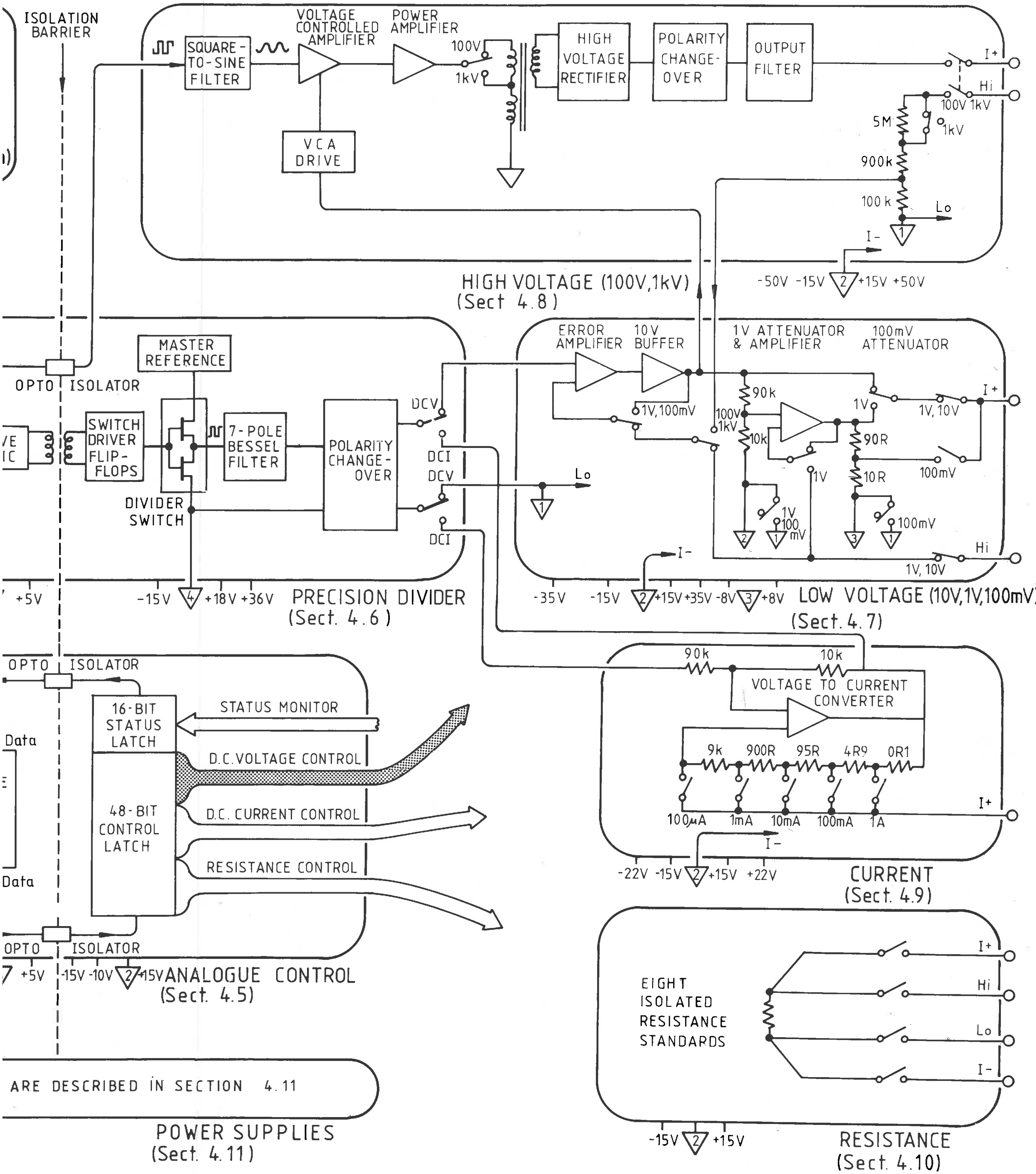


Fig. 4.2 4000 BLOCK DIAGRAM

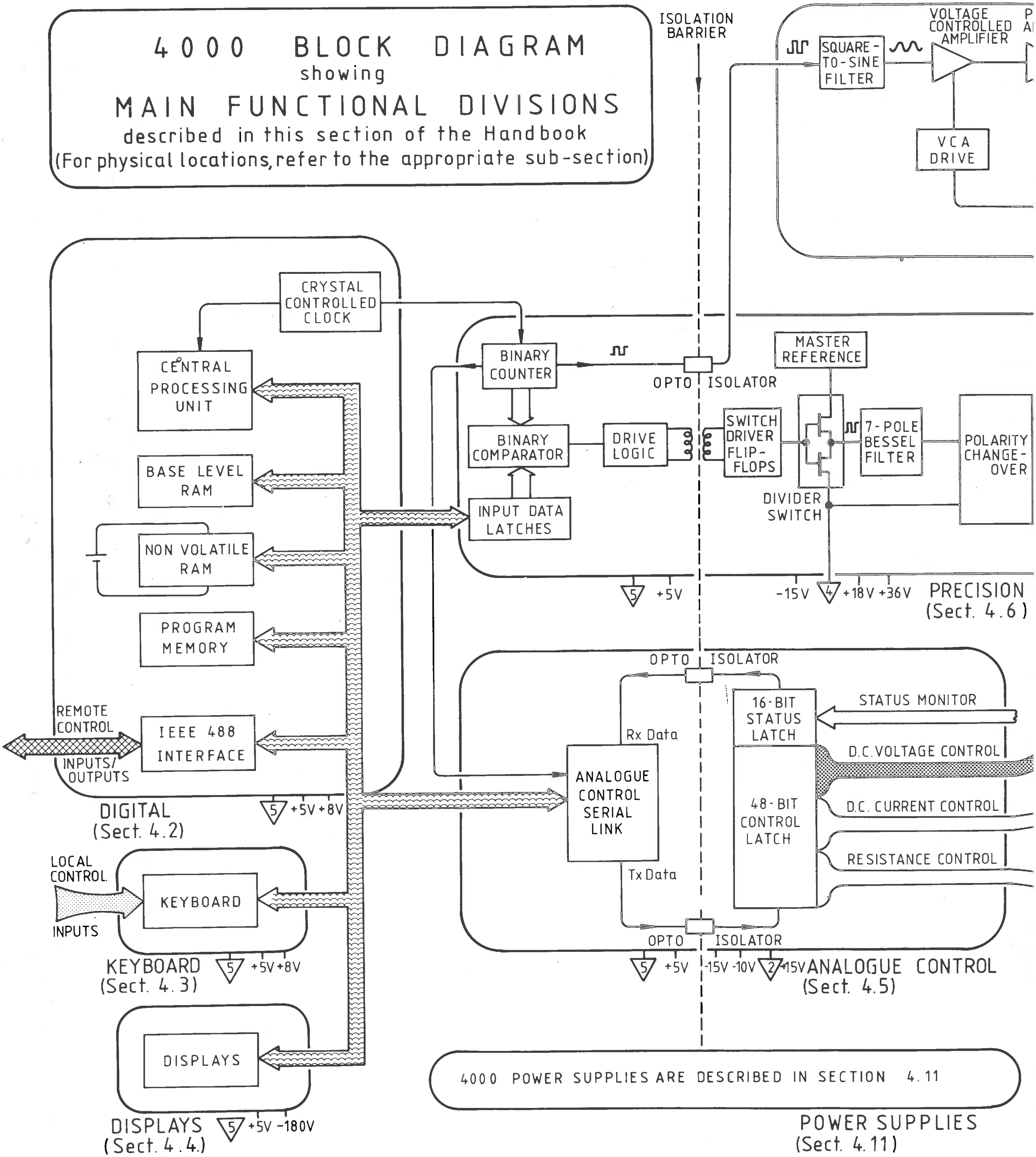
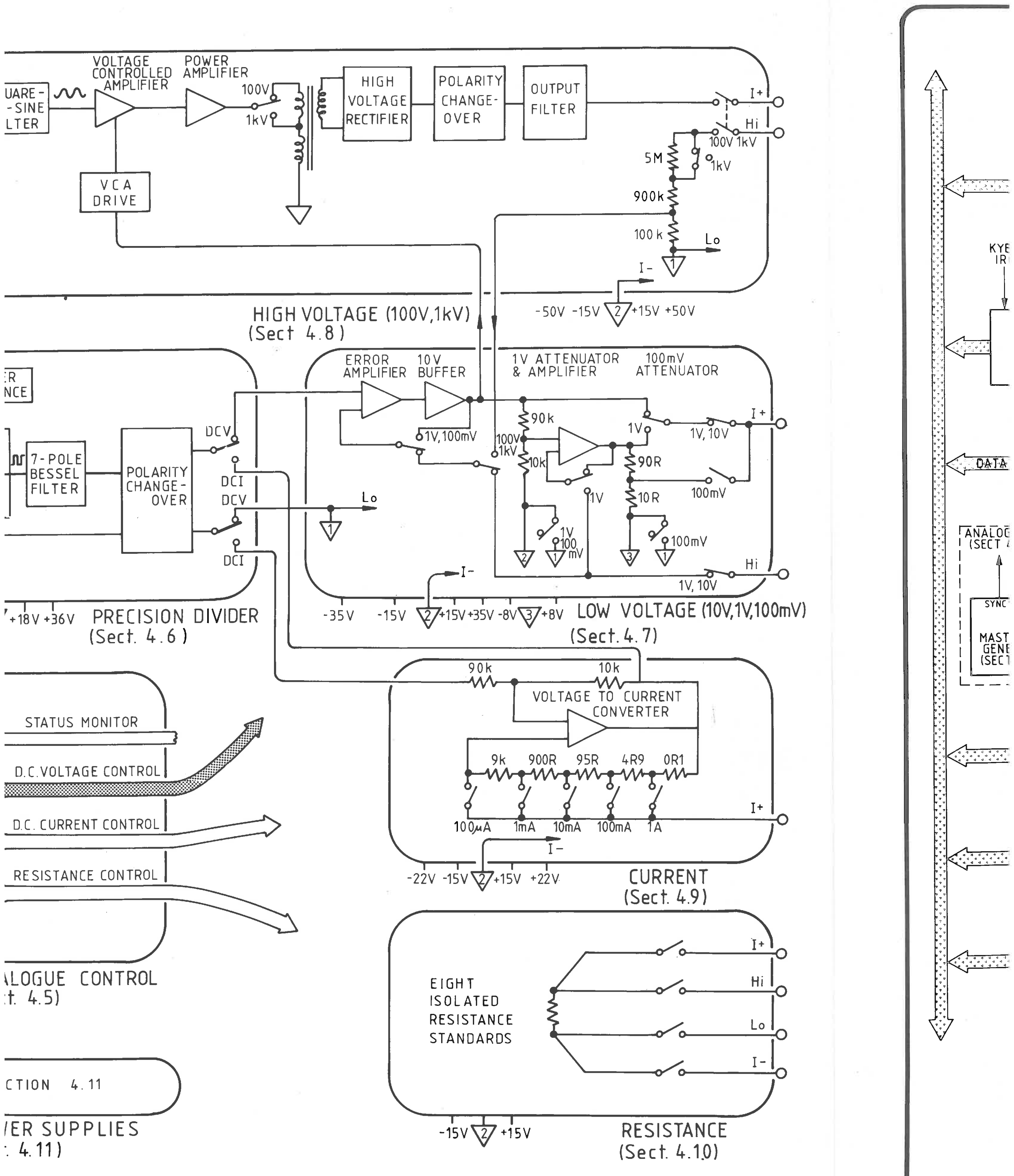


Fig. 4.2 4000 BLOCK DIAGRAM



4000 BLOCK DIAGRAM

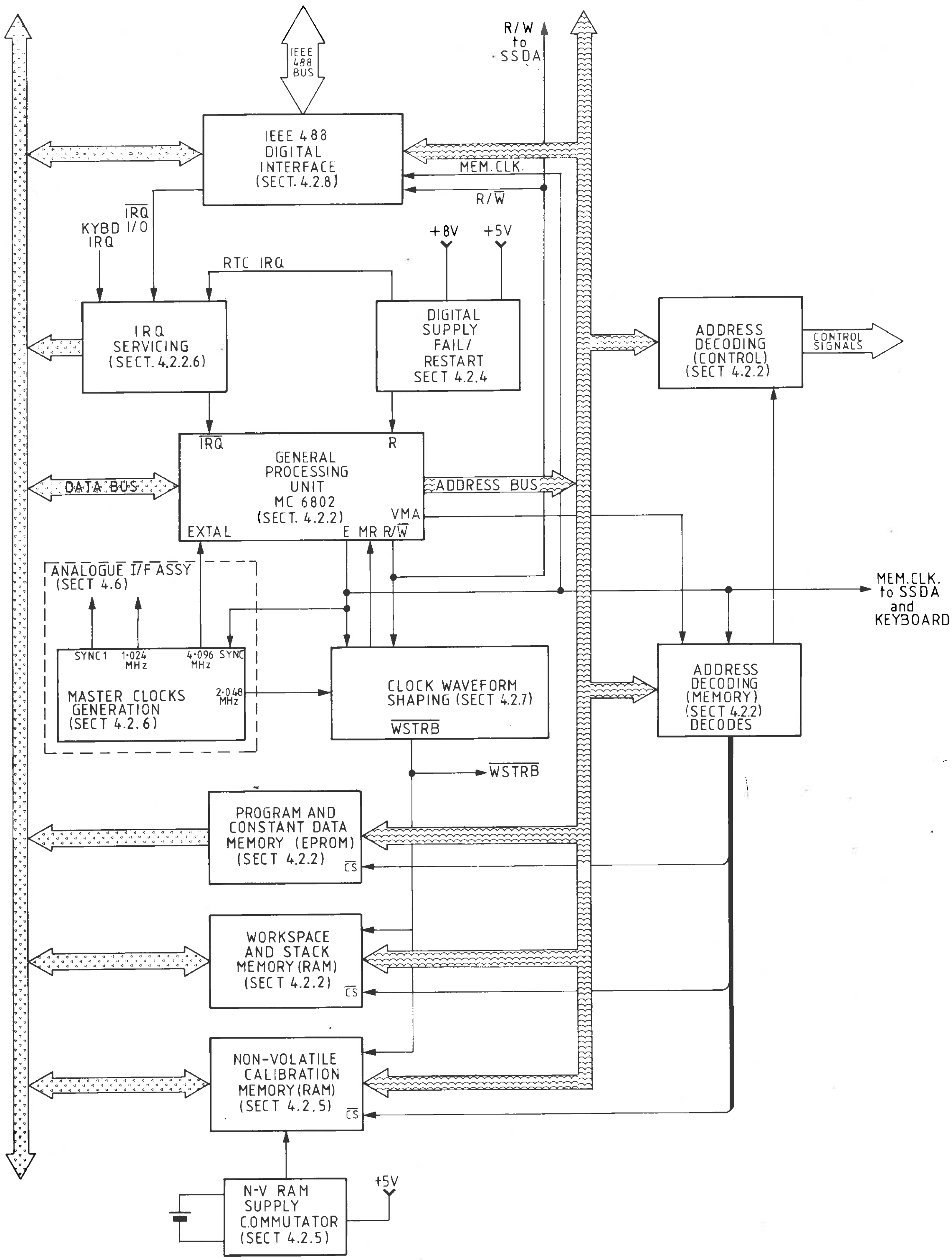


FIG. 4.3 4000 DIGITAL FUNCTION BLOCK DIAGRAM

4.2 DIGITAL

The circuits described in this section perform the following functions:

(1) Central processing, with supporting memory, for management of instrument operation.

(2) Storage of calibration constants in non-volatile memory.

(3) Generation of Master clocks, with clock-waveform shaping.

(4) Address decoding to generate control signals.

(5) Controlled power-up and power-down of digital circuits.

(6) Servicing IRQs from asynchronous sources.

(7) Interfacing the 4000 to the IEEE 488 bus.

The functions are performed by circuits located mainly on the Digital PCB Assembly (400442). Master Clock generation, synchronisation and division is carried out by circuits on the Analogue Interface PCB Assembly (400443).

Fig. 4.3 shows the arrangement and main interconnections of the central digital circuits.

4.2.1 General

The 4000 is managed by a 6802-series micro-processor system, under the control of an operating program held in 20k bytes of EPROM. All front and rear panel controls provide direct inputs to the system, except for the Power ON/OFF switch and Safety Reset Key. The system ensures that the processor reverts to a safe state on power-up and power-down.

1k bytes of random-access memory (RAM) are used for work space and stack. A further 256 bytes of CMOS RAM act as a non-volatile memory to hold calibration constants, powered by a back-up Lithium battery when the instrument is turned off.

4.2.1.1 Synchronous Operation

The operating program manipulates the internal circuitry by activating control signals. These result from providing peripheral decoders with specific address combinations. The program is run at 680kHz cycling frequency derived from a 4.096 MHz external oscillator.

4.2.1.2 Asynchronous Operation

Any Key operation (other than Safety Reset) generates an asynchronous interrupt to the processor, which suspends its current task to receive data and schedule new tasks associated with this data. The processor then continues with the interrupted task and returns to the amended task schedule to complete the initial operation synchronously. Three sources of interrupt are used:

Remote Command

Keyboard Command

Real-time Clock Pulses (8mS intervals)

These are identified by polling the data bus each time the 6802 receives an IRQ interrupt.

4.2.1.3 Output Generation

Having stored user inputs for output value, offset, error and calibration constants, the processor uses them to compute a binary value to a resolution of 25 bits. This is used to adjust the mark/period ratio of the Reference Divider switch which ultimately controls the Working Reference Voltage for the output analogue circuitry.

4.2.1.4 Display Refresh

The gas discharge display is continuously refreshed by cycling through character data stored in a separate display-image RAM. To alter the display the processor merely alters the contents of the RAM.

4.2.2 Central Processor and Memory (Circuit Diagram No. 430442 Sheets 2 and 3)

A 6802 microprocessor [M34] together with its memory, controls communication throughout the whole instrument.

4.2.2.1 Memory

The memory can be split into five main areas:

(1) Program Memory (M18, 19, 20, 21 and 22) – defines and controls the operational functions of the whole instrument system.

(2) Constant Data Memory (held in EPROM with the Program Memory). – eg Instrument specification for use in 'Spec' mode, key mapping tables and other fixed factors.

(3) Non-volatile Calibration Memory (M26 and 27) – stores all the calibration constants determined during the 'Auto-cal' cycle which are used for each output value.

(4) Volatile Memory (M24, 25) – used for volatile data storage, eg display images, computational stores, present output value.

(5) Operating Memory (M24, 25) – used for scratch pad operations and storage

The 6802 microprocessor internal RAM is not used.

Separate memory is used for special purposes, such as the Display Image RAM (M16) which is synchronously loaded but asynchronously read, the storage areas in the IEEE 488 GPIA (M29) and the keyboard interface (M6 on Front Assembly), and the Memory Address decoder PROM (M3). These are described in later sections.

4.2.2.2 Central Processing Unit [Circuit Diagram 430442 Sheet 2]

The MC6802 [M34] is a monolithic 8-bit microprocessor with Interrupt and Clock-stretching facilities. It is driven by a single phase 4.096 MHz square wave generated by the Master Clock circuit in the Analogue Interface Assembly. (This clock synchronises the reference divider switch with the processor cycle).

4.2.2.3 Address and Data Lines

Address lines A_{15-11} are decoded as chip-select signals for the RAM/ROM circuit, and lines A_{12-0} are connected to the instrument address bus. Data lines D_{7-0} are linked via programming plug JL1 to the instrument data bus.

4.2.2.4 E, MR and MEMCLK

The 4.096 MHz clock input at M34-39 (EXTAL) is divided by four and used as output at M34-37(E). Although the natural frequency of E is 1.024 MHz, the action of the waveform shaping input to MR reduces it to approx. 680 kHz as MEMCLK for the Front and Analogue-Interface assemblies.

4.2.2.5 $\overline{\text{NMI}}$

The internal switch S1 provides a non-maskable hardware interrupt which has two functions:

(1) With the external CALIBRATION switch set to RUN, $\overline{\text{NMI}}$ initialises the processor system

(2) With the CALIBRATION switch set to ENABLE, $\overline{\text{NMI}}$ clears the non-volatile calibration memory (M26/27) before initialising the processor system.

4.2.2.6 $\overline{\text{IRQ}}$

Any one of three asynchronous Interrupt Request signals are able to activate the maskable $\overline{\text{IRQ}}$ input at M34-4:

(1) RTC IRQ is a real-time clock which occurs every 8mS to provide timing information for the processor's monitoring facility.

(2) KB IRQ occurs each time a key is pressed on the front panel. (Not Safety Reset)

(3) $\overline{\text{IRQ IO}}$ occurs when the IEEE 488 Interface has a transaction to communicate to the processor.

D1, D2 and Q1 constitute a DTL OR-gate to isolate the IRQ inputs from one another. On receipt of Logic-0 on pin 4, M34 stores its register contents in stack RAM, and vectors to IRQ service addresses FFF8 and FFF9, saving the current processor environment. The IRQ service routine addresses M51 and M52, generating logic-0 at M52-9 which enables the tristate buffers M36 and M37 at M36-1 and 15, M37-15. This sets IRQ data bits D5, D6 and D7 on the data bus so that the processor can identify the source of the IRQ and select the appropriate sub-routine to service the interrupt request. The IRQ inputs are released as part of the service sub-routine, and after its completion, the processor recovers its environment from stack RAM and proceeds with the interrupted operation.

4.2.2.7 Software IRQ

The 6802 will also recognise Opcode 3F on the data bus as an interrupt request ('Implied' addressing mode). In the 4000 this code is hard-wired via R9, R10 and AN3 onto the data bus so that if the processor tries to access a non-available address, the floating bus will be pulled to 3F, initiating the software IRQ. The processor vectors to FFFA and FFFB, whose contents cause the 6802 to re-initialise the whole system.

4.2.2.8 Read-write line $\overline{\text{R/W}}$

The processor sets the R/$\overline{\text{W}}$ line to logic 1 when it is in Read state, and logic-0 when it has data to write into the addressed device. The R/$\overline{\text{W}}$ signal is passed only to the SSDA on the Analogue Interface assembly, and to the IEEE 488 GPIA (M29). All other devices which require read-write control, operate from $\overline{\text{RSTRB}}$ and $\overline{\text{WSTRB}}$ signals generated from R/$\overline{\text{W}}$ by M49/50.

4.2.3 Software Overview

The software management organization is shown in Figure 4.4. The machine cycle, which progresses through the task schedule shown, is modified by the requirements of real time-conscious activities and by those dedicated to remote commands. Real time and remote command interrupts suspend the current activity of the processor in order to service the immediate task requirement; the suspended task is then resumed.

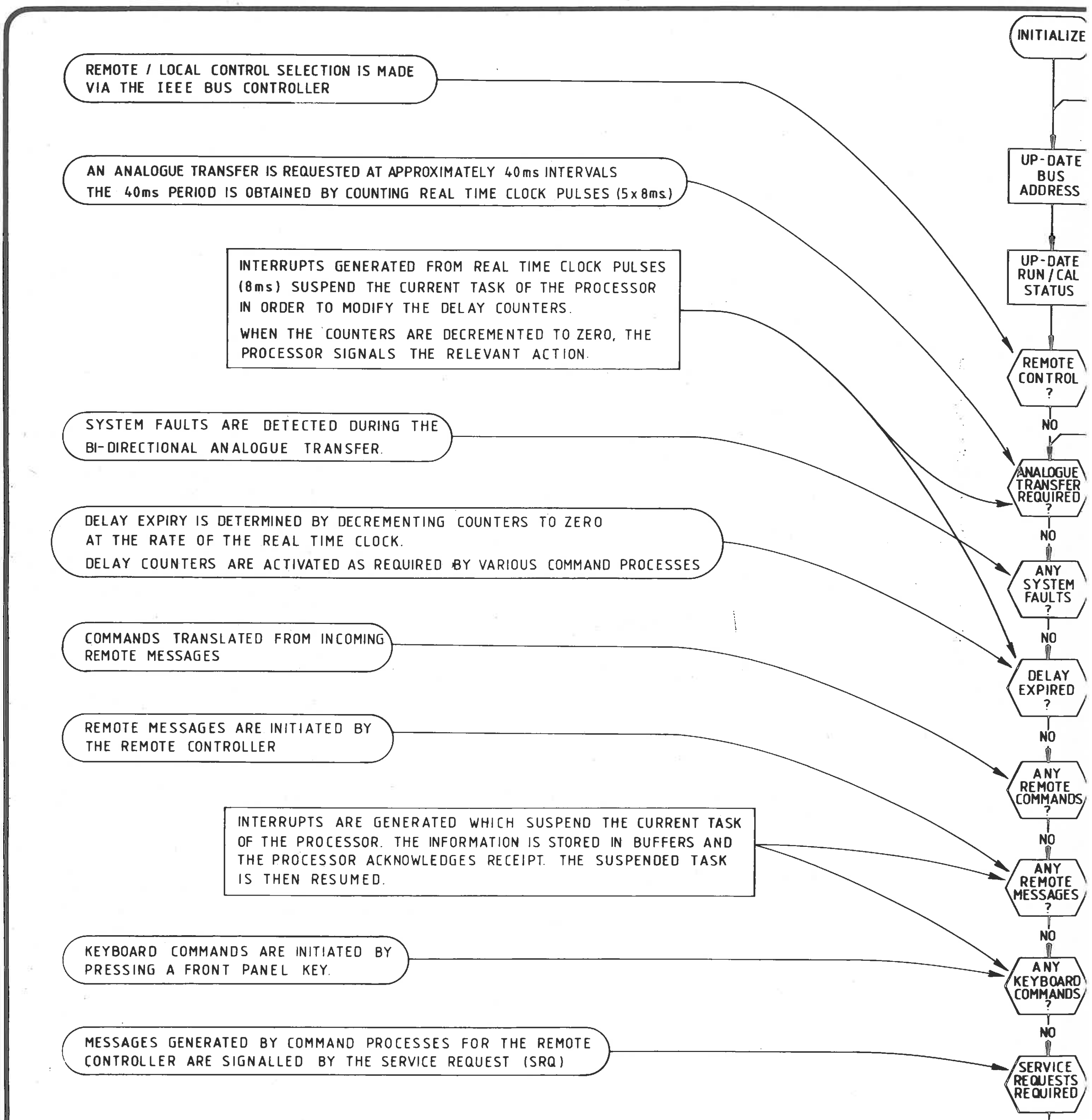


FIG. 4.4 SOFTWARE OVERVIEW

n remote commands. Real time and remote command
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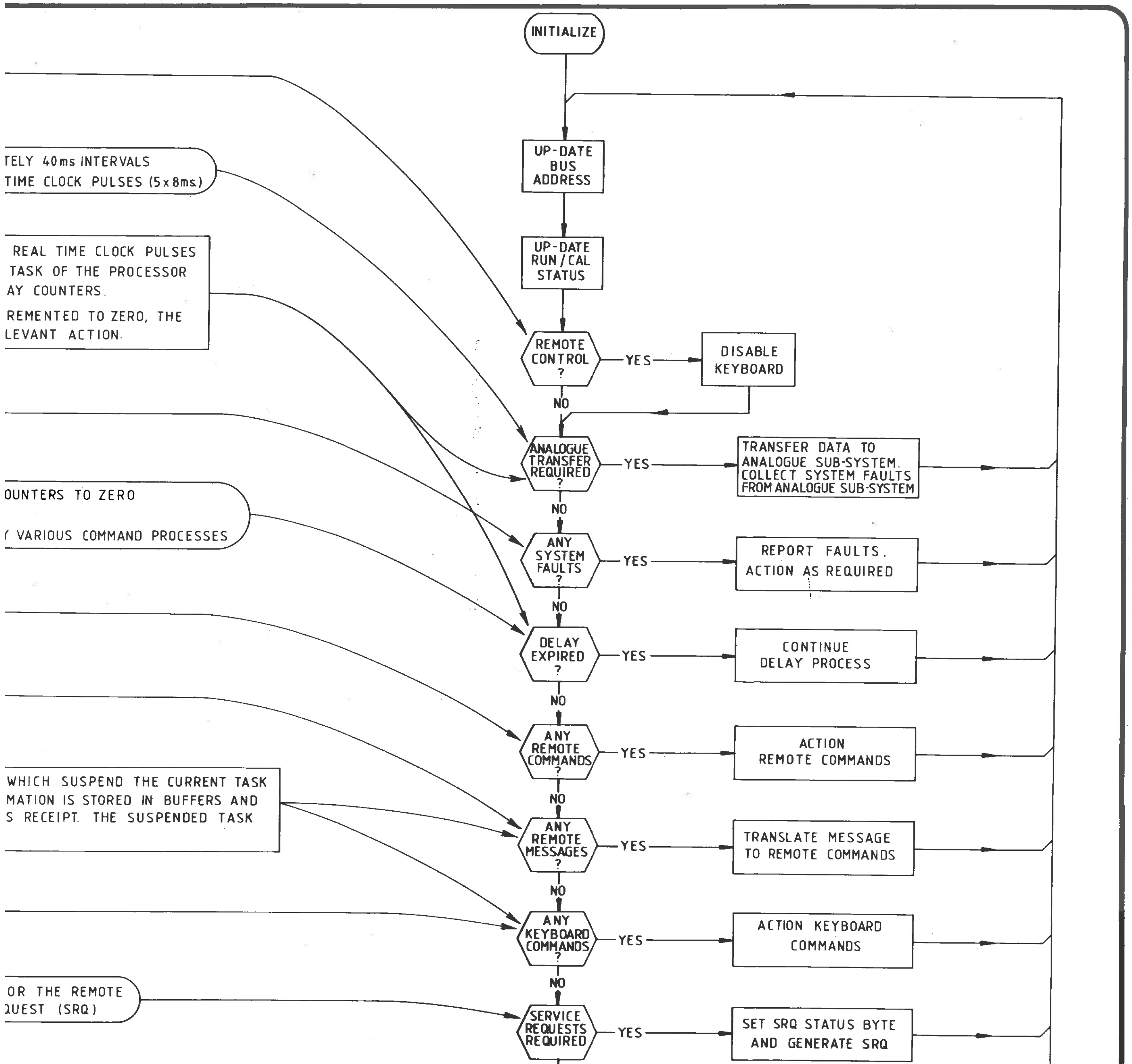


VERVIEW

4.2.4 Digital Supply Fail/Restart Circuitry

Power-up, restart and shut-down of the digital circuitry are performed in a controlled sequence to safeguard against hardware failures or a software crash. A continuous surveillance of the software management is performed by the safety monitor (watchdog — refer to Section 4.5). This will shut-down the instrument in the event of a failure in the digital control circuits or in software management.

4.2.4.1 Power-up Sequence (Circuit Diagram No. 430442)

Power-on is first sensed by the Supply Fail Detector circuit. This draws its supplies from the +8V dc unregulated supply, which is the first of the power supplies to rise to a working level. The comparator circuit of M28 has a nominal threshold of 7.1V dc, above which a good working level of the + 5V dc supply is assured. M28 will give a logic-0 output below the 7.1V threshold level which will prevent the start-up sequence progressing.

As power supplies rise towards a working level, flip flop M8 is held in RESET state with its $\overline{Q}$ output at M8-2 at logic-1. This will initiate the following actions:

1) $\overline{\text{PWR ON RST}}$ active; fed to the front panel assembly, this logic -1 level holds keyboard encoder M6 in Reset and disables the LED cathode driver decoder M4.
2) $\overline{\text{PWR ON RST}}$ active (via inverter M6-4). In the digital pcb assembly, this logic -0 level holds the microprocessor M34 and the IEEE 488 GPIA M29 in Reset. It is also fed to the analogue interface pcb assembly where it holds SSDA M44 in Reset.

PWR ON RST and $\overline{\text{PWR ON RESET}}$ are held active until flip flop M8 is clocked from counter M9. This is a 14-bit binary counter clocked at 2.048 MHz, thus giving a delay of 8mS from start of count to output from M9-3. The counter is enabled by a logic-0 at its Reset input; the conditions which allow this at power-on reset are as follows:

1) Comparator M28 output at logic-1 (High)
2) Microprocessor M34-5 VMA output at logic 0; this is forced by logic-0 at its reset input, thus inhibiting address decoder M3 and setting all M3 address outputs to logic -1. This combination gives logic -1 at M5-13, but M6-2 at logic-0 gives logic-1 at M5-11 and subsequently logic-1 at M7-2.

At full count, M9-3 output clocks flip flop M8, taking M8-1 to logic-1 and M8-2 to logic-0.

This initiates the following actions:

(1) PWR ON RST at logic-0. Enables keyboard encoder M6 and LED cathode driver decoder M4 on the front pcb assembly.

(2) $\overline{\text{PWR ON RST}}$ at logic-1:
   - (a) Lifts reset level to microprocessor M34 allowing software initialization to commence, and enables IEEE bus controller M29 on the digital pcb assembly. (Part of the instrument initialisation procedure is a software reset for M29).
   - (b) Lifts reset level to the SSDA M44 on the analogue interface pcb assembly.

(3) M8-1 at logic-1.
   - (a) Enables RTC IRQ. The action of M9, M8 and M51 generates a "Real-time clock IRQ" at 8mS intervals. M51-5 is normally at logic-1; but after a RTC IRQ has been serviced, the CPU addresses M51, pulsing M51-5 (M7-12) to logic-0 (RTC RST). M7-12 is pulsed to logic-1, resetting M8-13 (RTC IRQ) to logic-0. At the next full count of M9; M8-13 is clocked to logic-1, initiating the next RTC IRQ.
   - (b) Provides an enabling input to M10-1 (See Non-volatile RAM Supplies Section 4.2.5).
   - (c) Triggers monostable M53-4. This monostable has a relaxation period of 470 mS; during which time it holds the $\overline{\text{FP RST}}$ output at logic-0 which allows the watchdog circuits to reset on the reference divider pcb (see Safety Monitor Section 4.5).

M9-3 pulses also regularly clock the binary state of M8-5 through to M8-1, monitoring the supply status. When running normally, M8-5 and M8-1 are both logic-1, but if the supply fails a fast reset is provided by M7-1 logic-0 to M8-4 logic-1, rather than waiting for the next clock pulse. M7-3 also resets the 8mS counter at M9-11.

4.2.4.2 CPU Re-start (Circuit Diagram No. 430442)

Memory addressing by the CPU is monitored by the NAND logic of M4, M5 (four elements) and M7-3. In the correct addressing sequence there are two basic conditions:

(1) CPU VMA = logic-0
M3-D1 to D8 = logic-1

(2) Valid memory address –
CPU VMA = logic-1
CPU E = Logic-1
M3-D1 to D8 = One address line logic-0

Conditions (1) and (2) both result in a logic-0 From M7-3, allowing clock M9 and flip flop M8 to function normally. The possibility of a glitch occuring at the change-over between conditions (1) and (2) is gated from the control line by switching at M5-5. Incorrect addressing sequence in the CPU would be shown by:

CPU VMA = Logic-1, CPU E = Logic-1 – The CPU indicates that it has selected a valid external address

M3-D1 to D8 = Logic-1 – No address is selected.

This situation is most likely with a software failure. The logic control line M4, M5 now gives a logic-0 at M7-2 and thus a logic-1 at M7-3 which:

(1) Resets counter M9 to zero;

(2) Forces M8-1 to Logic-0. This forces RTC RST at M7-11 and removes an enable from M10-1 (see Non-volatile RAM supplies – Section 4.2.5).

(3) Forces M8-2 to logic-1. This change:

a. Resets the CPU by M34-40 to logic-0. VMA is forced to logic-0 which in its turn removes the reset from M9-11 and M8-4 via M6-2 at logic-0.

b. Makes PWR ON RST and $\overline{\text{PWR ON RST}}$ signals active, thus resetting the other software controlled areas.

After 8mS from CPU reset, flip flop M8-3 is triggered from clock M9. M8-1 and M8-2 change state and the start-up sequence commences.

4.2.5 Non-volatile RAM Supply Commutation

4.2.5.1 Non-volatile RAM Inhibit ($\overline{\text{NV INHIBIT}}$)

Chip-select to the two non-volatile memories, M26 and M27, is inhibited during power-up, re-start and power-down operations. Memory access to the two non-volatile RAMs is enabled during normal running by the chip-select input $\overline{\text{NV INHIBIT}}$ being held at logic-1. The NAND logic gates M10, used to control the inhibit, remain powered from the RAM standby supply after power-down.

Conditions for normal running are as follows:

(1) Supply fail detector circuit provides a logic-1 (supplies valid) output to opto-coupler M11. This causes the coupled transistor of M11 to conduct and hold M10-2 at logic-1.

(2) M10-3 is held at logic-1 (to +5V via R6);

(3) M10-1 is held at logic-1 by flip flop M8-1.

The above conditions ensure a logic-1 output from M10-10 ($\overline{\text{NV INHIBIT}}$ not active).

During power-up, $\overline{\text{NV INHIBIT}}$ is held active (logic-0) until the power supplies have settled and the CPU has been reset. The input to M10-3 is delayed on the +5V supply by the time-constant C8, R6. Also, the input to M10-1 is held at logic-0 by flip flop M8-1 until the CPU has been reset. At power-down, or in the event of a supply failure, the $\overline{\text{NV INHIBIT}}$ becomes active (logic-0) before the +5V supply fails. The first indication of supply failure is made by supply fail detector M28 output going to logic-0. This cuts-off the opto-coupler M11 which takes M10-2 to logic-0. M10-3 is held at logic-1 by the +5V supply, thus M10-9 is taken to logic-1 and M10-10 to logic-0 ($\overline{\text{NV INHIBIT}}$ active).

In the event of a CPU reset, the $\overline{\text{NV INHIBIT}}$ is made active for the period of reset by the switching action of M8-1 and M10-9.

4.2.5.2 Supply Commutator

This circuit provides the non-volatile RAMs M26 and M27 with a battery-driven standby supply when the instrument is in the power-down condition. It ensures continuity of supply in the change-over between main and standby, and minimizes battery current leakage. In the power-down condition, the battery circuit is to M10, M26 and M27, with the return from battery common 5B via D7 and R60. The battery common 5B is isolated from the general common 5A by transistor Q2, which is cut-off.

During power-up, operational amplifier M28 is powered from the +8V supply before the +5V supply voltage is established. As long as the +5V supply voltage is less than the battery voltage, Q3-4 is biased negatively, and Q3 is unbalanced in favour of heavy conduction through Q3-6. M28-5 is held low, so M28-7 remains at Common-5A potential, and opto-coupler M39 is not energised. Q2 remains cut off, maintaining isolation of Common-5B and the battery supply. M10, M26 and M27 remain powered from the battery.

As the +5V supply voltage increases, D7 cathode potential rises, reducing Q3-4 bias, reaching zero when its voltage is equal to the battery voltage (less than 10mV is developed across R60).

When the +5V supply voltage exceeds the battery voltage, Q3 becomes biassed in favour of heavy conduction through M3-2, pulling M28-6 low and reversing the differential input to M28. M28-7 rises to the +8V rail and energises the opto-coupler M39, which switches Q2 on, connecting common-5B to common-5A. M10, M26 and M27 are now powered from the +5V supply and the standby battery is isolated by reverse-biased diode D7.

During power down, Q3 compares the +5V supply against the battery, switching Q2 off via M28 and M39 when the supply voltage falls below the battery voltage, and the non-volatile RAM supply commutates to standby battery. Alternatively, Q2 is switched off by failure of the +8V supply to M28 if this occurs before the +5V supply voltage falls below the battery voltage.

Eventually the +5V and +8V supplies both fall to zero, the battery supplies the non-volatile RAM, and common-5B is isolated from common-5A by Q2.

4.2.6 Master Clock Generation (Circuit Diagram No. 430443 Sh. 3) (refer to Fig. 4.5 for waveforms)

The master clock generator is based on crystal X1 which, with positive feedback buffers M1-2/M1-4, provides a precision 4.096 MHz squarewave reference frequency output.

The primary frequency of 4.096 MHz is divided by JK flip flop stages M41, both of which are connected to toggle when clocked. The first division stage is synchronized at its reset input, M41-3, to the memory clock via flip flop M42. This ensures correct phasing of the 2.048 MHz squarewave output from M41-14 (for description of synchronising action, refer to section 4.2.7.3). M41-11 and M41-10 outputs provide complementary 1.024 and $\overline{1.024}$ MHz squarewaves respectively. Monostable M40, triggered at 2.048 MHz from M41-15 provides the positive-going 2.048 MHz synchronizing pulses, SYNC 1.

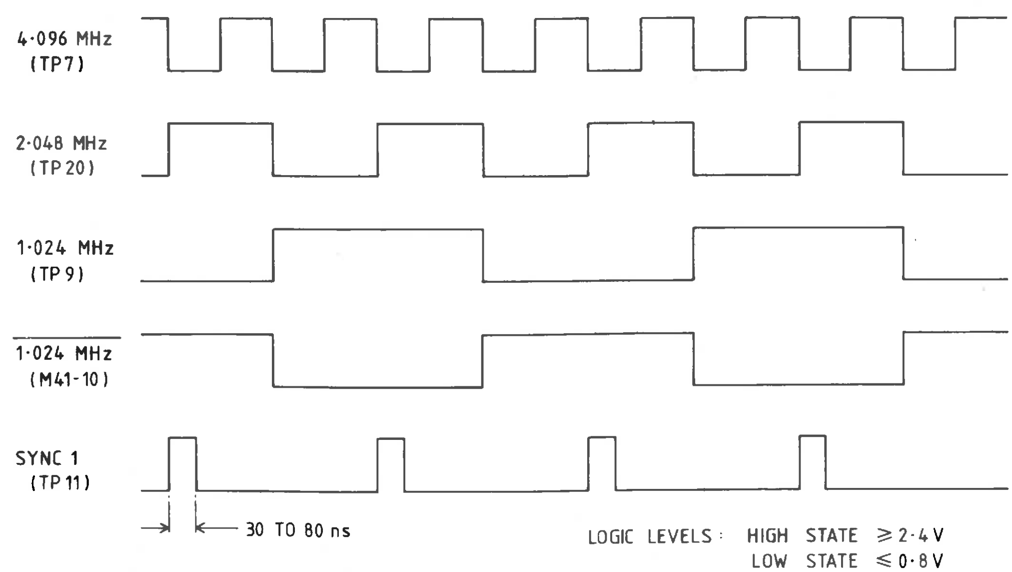


FIG. 4.5 MASTER CLOCK GENERATOR WAVEFORMS

4.2.7 Clock Waveform Shaping (Circuit Diagrams Nos. 430442 Sheet 2 and 430443 sheet 3)

NB As the locations of the circuits in fig. 4.7 are clearly marked, and as there are no duplicate designators in the circuits, this description does not refer to a component's location except where necessary.

NOTE To avoid confusion, the terms "high" and "low" are used to replace "logic-1" and "logic-0" respectively in this description.

The crystal oscillator on the Analogue interface assembly provides a 4.096 MHz Master Clock signal (M1-4) for the whole instrument. This signal drives the 6802 microprocessor at M34-39 (EXTAL) so M34-38 is not connected. M41 divides the 4.096 MHz to generate a 2.048MHz clock for the Memory Clock Stretching Circuit (M35/M49).

M34 divides the EXTAL input internally by 4 and outputs the result as E (Enable) at M34-37, to act as a "ϕ2" Memory Clock for the SSDA on the analogue interface assembly and the keyboard controller on the front assembly.

If M34-3 (MR – Memory Ready) were permanently held at +5V, the E signal would be 1.024 MHz. But in the 4000, a "stretching" circuit (M35/M49) doubles the Logic High (+5V) time of E by switching MR to Logic Low (0V) for part of the cycle. This is shown on Fig. 4.6.

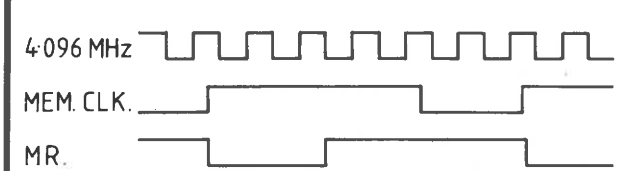


FIG. 4.6 MEMCLK TIMING

As a result, the frequency of E is reduced to approximately 680kHz. With 1μS available for access to the SSDA, Keyboard Controller, IEEE GPIA and memory.

4.2.7.1 Memory Clock Stretching Circuit (Fig. 4.7)

The action of M35 and M49 is dependent upon the finite propagation time between clocks at M35-1/ M35-6 and Q output at M35-15.
When M34-3 (MR) is +5V; M34-37 (E) is toggled by alternate positive-going edges of the 4.096 MHz clock, with a propagation delay of approximately 80nS.
Also, the 4.096MHz signal is divided by 2 in M41, resulting in 2.048MHz signal whose negative-going edges clock M35.

M35 cascade action is controlled by the condition of the Memory Clock (E) and affected by its own propagation times.

4.2.7.2 Shaping Action (Figs. 4.7 and 4.8)

The 4.096MHz clock edge at T1 causes E to rise from low to high at T2. As M35-10 is also high, MR changes from high to low at T2, holding E high. M35 pin state is 4 and 10 high, 9, 12 and 16 low.

At T3 the 2.048MHz falling edge clocks M35, and M35-9 rises to high awaiting the next clock edge (not until T5). M35-10 remains high, so MR is held low and E stays high.

At T4, MR is still low, so the 4.096MHz clock has no effect on E, and E is stretched.

At T5, MR is returned to high when the logic-1 on M35-9 is clocked as a logic-0 to M49-4. This allows the 6802 to toggle E at the next effective clock edge.

At T6 the rising edge of the 4.096MHz clock causes E to fall to low, setting up M35-4 to low, M35-12 and 16 to high. M35-9 is already high.

At T7, M35-10 is toggled to high, but as M49-5 is now low, MR remains high to allow E to be toggled at the next effective processor clock edge (not until the next T1). Also at T7, M35-15 is clocked to low to set M35-9 ready for the next (T3) clock edge. The circuit is now set up to its initial (pre-T1) condition so the action repeats.

4.2.7.3 2.048MHz Clock Synchronisation (Figs. 4.7 and 4.9)

Unless M41 is synchronised, it could toggle in reverse phase, upsetting the timing of the stretching circuit. In Figs. 4.7 and 4.9, M42 acts as a monostable to provide a negative reset pulse into M41-3, coincident with the negative-going edge of E. If M41 starts up in the wrong phase, its state is corrected just prior to T7. Once established in the correct phase, M41 will already be in reset when the pulse appears, and is not affected.

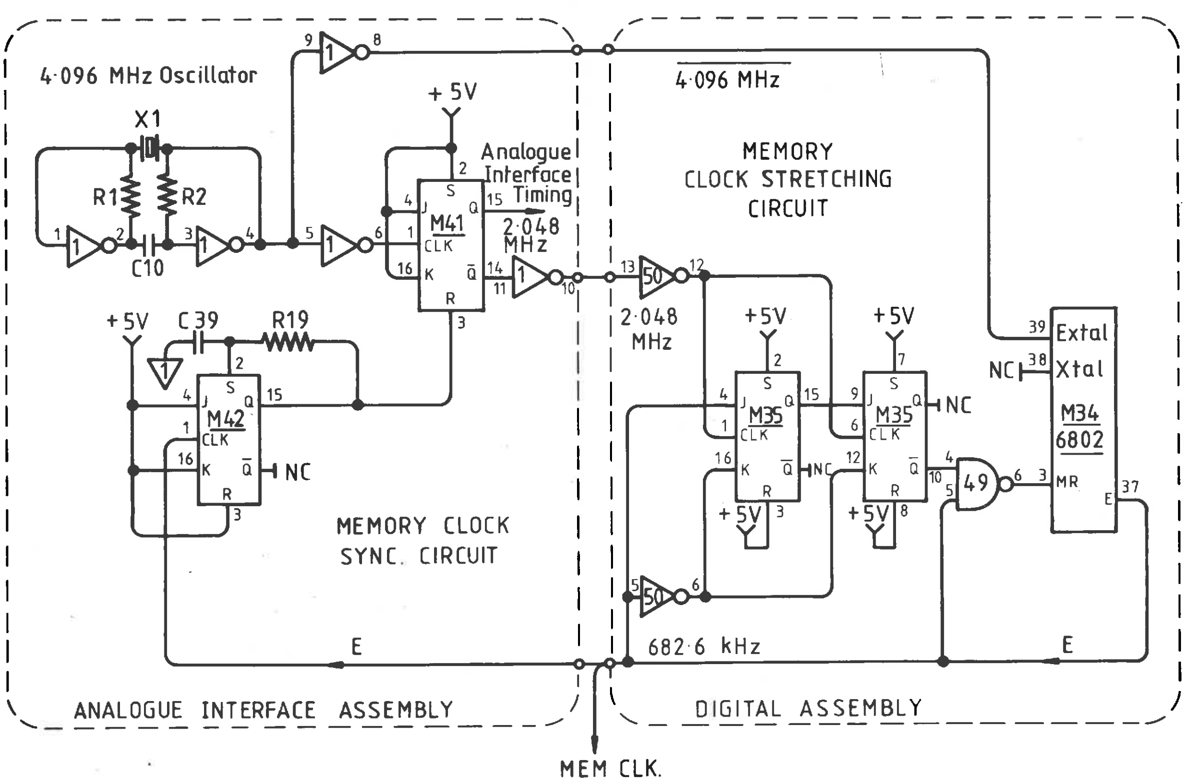


FIG. 4.7 CLOCK SHAPING CIRCUIT

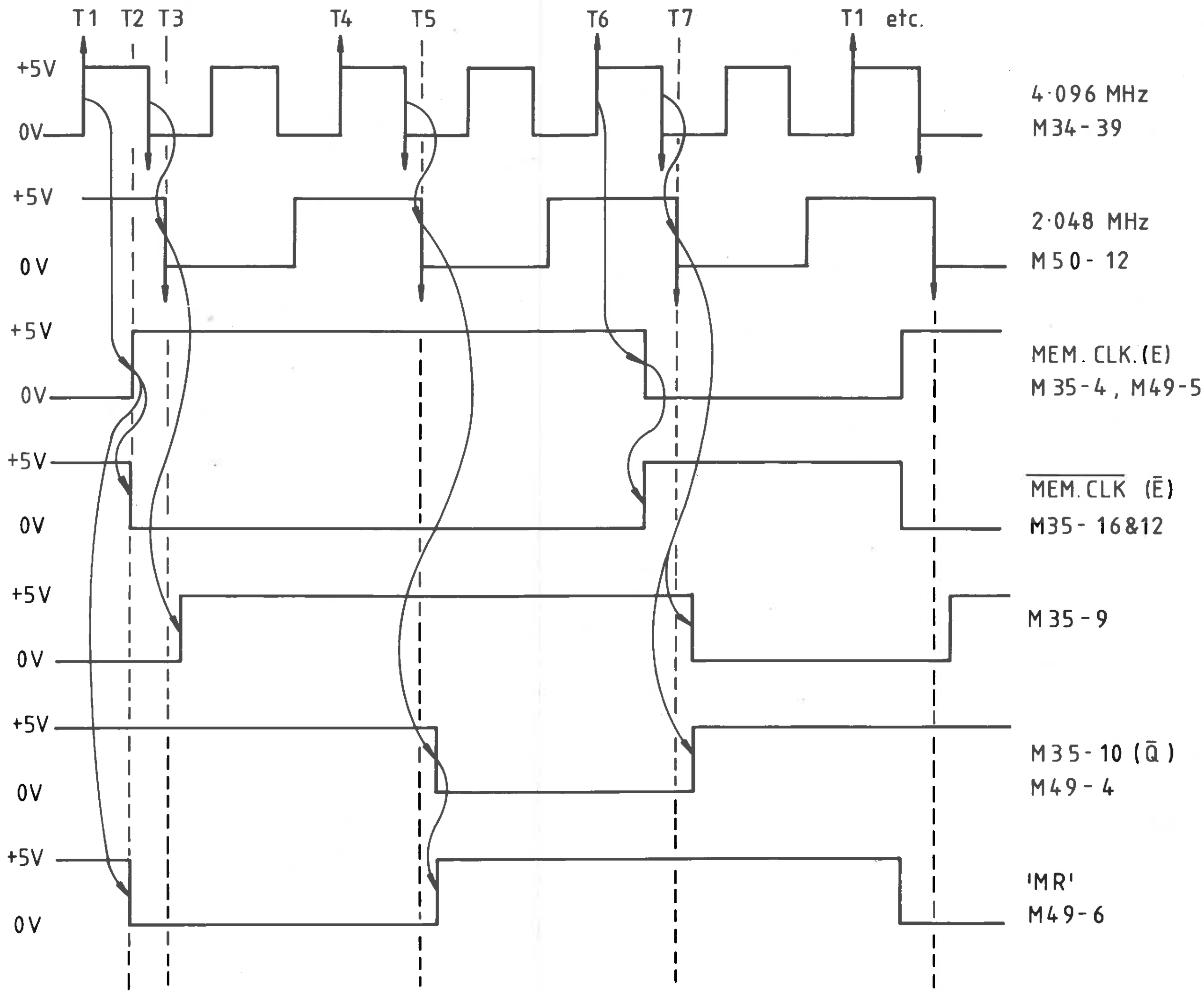


FIG. 4.8 CLOCK SHAPING WAVEFORMS

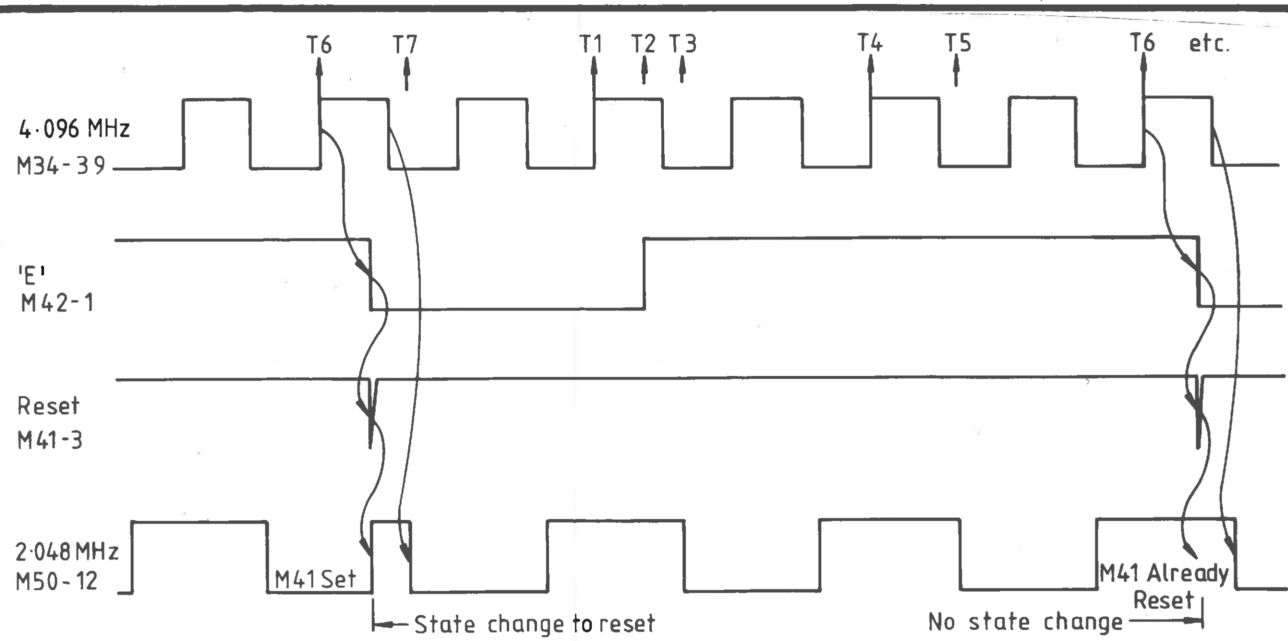


FIG. 4.9 2.048MHz CLOCK PHASE-SYNCHRONISATION

4.2.8 IEEE 488 Digital Interface (Circuit Diagram No. 430442 Sheet 4)

The IEEE Interface circuitry is located on the bottom right-hand corner of the Digital PCB (viewed from the front of the instrument). M29, M40, M47 and M48 execute and decode interface functions, and perform data input/output transfers.

The General Purpose Interface Adaptor (GPIA) M29, is software-driven by the 6802 CPU, as part of its normal function. M29 is addressed at $\overline{CS}$ by $\overline{XIOBBD}$ from M51, and its internal registers are accessed by A_0, A_1 and A_2 from the address bus.

The GPIA is clocked by Memory Clock E, with read or write control direct from the processor R/$\overline{W}$ signal at M29-5, and at 4000 power-on M29 is initialised at M29-19 by the $\overline{PWR\ ON\ RST}$ signal from the Restart Generator circuit (M6-4).

Information is passed between M29 and the CPU (M34), via the data bus $D_0 - D_7$. The address switch data is linked to $D_0 - D_6$ by tristate buffers M47. During initialisation, and periodically thereafter, the state of M29-4 (ASE) changes from +5V to 0V, enabling M47. The status of the address switches on the 4000 rear panel are transferred into M29 via M47 and the data bus for comparison with the received address.

M40 and M48 are bidirectional bus driver arrays. The drivers for bus management lines: IFC, ATN and REN are permanently held in Receive state, and the SRQ driver in Transmit state. The EOI line driver is switched from Receive to Transmit by M29-28 (T/$\overline{R}$1) changing from 0V to +5V as required by M29. M29-7 (T/$\overline{R}$2) is normally held at 0V for reception of system data via DIO 1 – 8 bus lines, and set to +5V for 4000 data to be sent over the bus.

Some system controllers output excessive noise along the $\overline{REN}$ line. To avoid spurious switching of M29 between Local and Remote control states, R58 and C31 act as a filter for this noise.

M29-40 ($\overline{IRQ}$) is used to inform the CPU when certain states occur. In particular, $\overline{IRQ}$ is generated at each byte-transfer over the bus, whether the type is sent or received. Additionally, $\overline{IRQ}$ is activated whenever certain specific commands are received, e.g. DCA, SPA and Remote/Local Change. When the CPU receives $\overline{IRQ}$, it addresses M39's Interrupt Status Register to identify the reason via the instrument data bus.

For further information refer to "Getting Aboard the 488 bus" published by Motorola, or the appropriate device data sheets.

4.3 KEYBOARD

The circuitry described in this section performs the following functions:

(1) Provides front-panel operator control of 4000 Output, Function, Range and Mode circuitry, by push-button keys. Key operation is detected internally and transferred to the CPU via the instrument data bus.

(2) Indicates the current instrument state by means of LEDs fitted in the Keys.

(3) Generates audible warning of high voltage at the Output Terminals.

In addition a rocker switch sets instrument Power ON and OFF (refer to Section 4.11) and a "Safety Reset" Key provides a hardware reset for the safety monitor (Watchdog) circuits (Refer to Section 4.5). The circuitry is located on the Front PCB Assembly (400441), linked to the CPU by control signals and the data bus.

Circuit Diagram No. 430441 sheet 1 shows the arrangement and interconnections of the Keyboard circuits.

4.3.1 Key and LED Matrices (Circuit Diagram No. 430441 sheet 1)

The keys are electrically arranged in a 7 x 8 matrix as shown in the diagram. The 7 columns are scanned by M5; any key contact is memorised by M6 and signal KBIRQ is passed to the microprocessor, which responds by interrogating M6 Keyboard memory and acting on the specific key command.

The key LEDs are electrically arranged in an 8 x 3 matrix. The three rows are scanned by M4, and the 8 columns receive the appropriate bit patterns from M6 display memory. This memory is up-dated as required from the microprocessor data bus $D_0 - D_7$.

4.3.2 Programmable Interface M6 (Fig. 4.10)

M6 interfaces the keyboard and LEDs to the instrument data bus. It is addressed by $\overline{CSKB}$ from the digital assembly, to chip-select $\overline{CS}$ which enables commands or data to flow via the data bus at DB_{0-7}. For data flow, the processor address Ao = logic-0 and for programming the interface during initialisation or for mode change, A0 = logic-1.

4.3.2.1 Read/Write Control

The $\overline{WSTRB}$ signal from the digital assembly is applied to M6 $\overline{WR}$. Data or Command is input to M6 from the processor data bus during $\overline{WR}$ low and $\overline{CS}$ low, and is latched on the $\overline{WR}$ positive-going edge. The $\overline{RSTRB}$ signal from the digital assembly is applied to M6 $\overline{RD}$. Data is output from M6 on to the data bus during $\overline{RD}$ low and $\overline{CS}$ low.

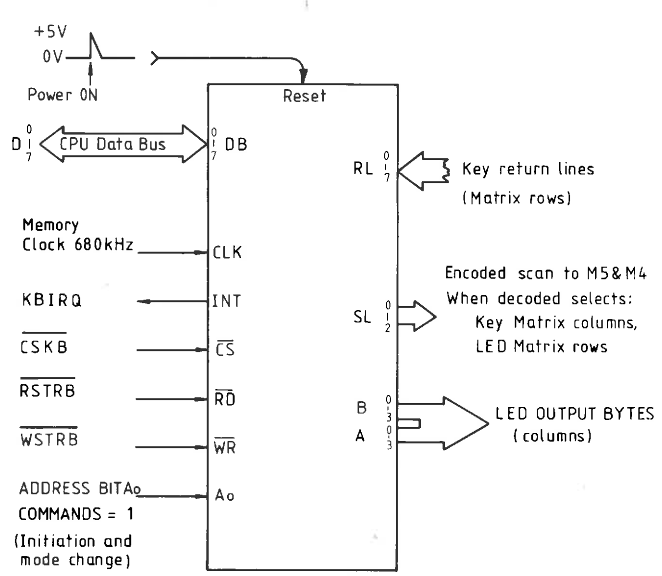


FIG. 4.10 M6 INTERFACE (P8279) SIMPLIFIED SCHEMATIC

4.3.2.2 M6 Initialisation

When the 4000 is switched on, M6 is cleared by the PWR ON RESET pulse from the digital assembly. The interface is then programmed during initialisation as follows:

Clock divider set to ÷ 8 – The memory clock (E) at approx. 680 kHz is divided by 8 to give internal clock frequency of 85kHz, an inherent division by 16 reduces the scan clock to 5kHz giving a scan cycling frequency of 333Hz.

Encoded Keyboard Scan – The scan output from SL_{3-0} is a 4-bit binary count. SL_3 is not used; SL_{2-1} scans M4, and SL_{2-0} scans M5.

Keyboard Mode – The internal keyboard RAM is programmed as FIFO, input via RL_{7-0} return lines. Two-key lockout is employed with debounce.

Display Mode – 8 Character left entry for the LED display.
– Inter-digit blanking: all 1's on B_{0-3}, A_{0-3} between digits.

4.3.2.3 M6 Reprogramming

The 13 dual ↑/↓ keys and the zero key (below the two displays) have a reprogramming function. When one of these keys is pressed, the P8279 is reprogrammed into Scanned Sensor Mode. When released, the P8279 reverts to Encoded Keyboard Scan Mode.

4.3.3 Scan Decoding

The encoded scan output from M6 (approximately 333Hz cycle frequency at SL_{2-0}) is decoded by M5 to energise each key-matrix column line once every scan cycle. SL_{2-1} scan outputs are also decoded by M4 to energise each LED-matrix cathode driver once in every scan cycle for a period of two digits.

4.3.4 Key Selection

The keys are electrically grouped within a matrix of 8 rows of 7 (some positions vacant). This does not conform to their physical grouping on the front panel. The eight return lines RL_{0-7} each define a row in the matrix whose columns are scanned by M5 (Low active). In M6, the internally-synchronised keyboard memory stores the state of each of the 48 keys. The use of 2-key lockout rejects two or more simultaneous contacts. Any single key depression is debounced, initiating the interrupt KBIRQ to the processor which interrogates the keyboard RAM. The next action is dependent upon the Key's function:

'Zero' or ↑/↓ key pressed –
a) M6 is reprogrammed into Scanned-Sensor mode for as long as the key is pressed, as the processor acts on the key information.
b) If an appropriate ↑ key is pressed whilst 'Zero' is held down, the resolution of the Output display is changed.
c) If a single ↑ or ↓ key is held down longer than approximately ½ second the display enters "auto increment/decrement" mode, running at approximately 6 digits/second.
d) When the key is released, M6 is returned to Encoded Keyboard Scan mode.

Any other key pressed (not Safety Reset) –
a) M6 remains in Encoded Keyboard Scan mode; the scan continues as the processor acts on the key information.
b) KBIRQ interrupts are generated only by the low-going edges of the key contact pulses, so M6 remains sensitive to other key depressions.

4.3.5 Key LED Operation

After performing the change requested by the key depression, the processor changes the bit-patterns stored in M6 internal display RAM. As this is scanned internally in synchronism with the decoded outputs of M4, each output byte of B_{0-3} A_{0-3} drives the row of LEDs accessed by M4 output lines. The bit-pattern of the byte selects the LEDs to be lit in that row (B_{0-3}, A_{0-3} bits high = unlit, low = lit). As B_{0-3} A_{0-3} lines change from one byte to the next, they are all set high to avoid spurious LED flashes. Q25-32 drive the LED anodes from a +5V supply regulated by M2, and Q21-23 Darlingtons drive the LED cathodes.

4.3.6 Audible Warning Buzzer

M4B and M1 act as a control latch for the quartz warning buzzer. With $\overline{\text{ALARM}}$ at logic-1 (+5V) M1 remains unchanged; but with $\overline{\text{ALARM}}$ at logic-0 (0V) the state of M1 depends on the condition of Ao:

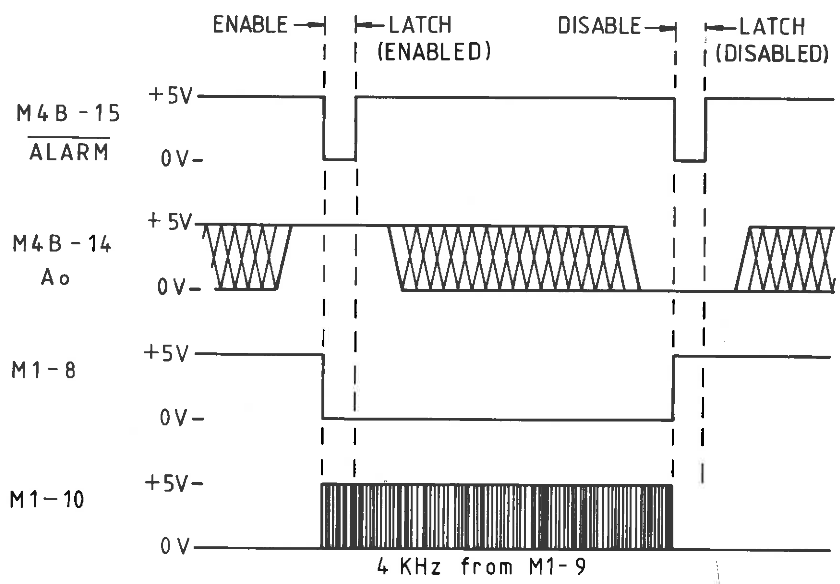
Ao at logic-1 the alarm sounds a 4kHz tone.

Ao at logic-0, the alarm is silent

The latch is operated at processor speed. Two $\overline{\text{ALARM}}$ pulses are used for each burst of sound. The first, with Ao at logic-1, starts the burst; and the second, with Ao at logic-0, ends it. The waveforms and truth table in Figure 4.11 illustrate the action of the latch. Note that Ao may be used for other purposes when $\overline{\text{ALARM}}$ is at logic-1, but this will not affect the buzzer state.

During Power ON initialisation the combination: $\overline{\text{ALARM}}$ – 0, Ao – 0 are applied to M48 to ensure that the latch powers up in the Disabled condition.

The 4kHz tone signal at M1-9 originates in the precision-divider counter on the Analogue Interface pcb (Circuit Diagram No. 430443 sheet 1).



M4B / M1 TRUTH TABLE

$\overline{E_B}$ (ALARM)	A_B (A_o)	$Q0_B$	$Q1_B$	M1 - 8	BUZZER
0	0	1	0	1	DISABLED
0	1	0	1	0	ENABLED
1	X	0	0	NO CHANGE	NO CHANGE
0 = 0V, 1 = +5V, X = either 1 or 0					

FIG. 4.11 ACTION OF BUZZER CONTROL LATCH

4.4 DIGITAL DISPLAYS

The circuits described in this section perform the following functions:

(1) Storage of display data in a Display Image RAM, updated under CPU control.

(2) Generation of a multiplex count which selects segment data from the RAM, and energises the appropriate digital blocks in synchronism.

(3) Distribution of high voltage supplies to energise the plasma displays.

Part of the Digital PCB Assembly (400442) houses the display multiplexer, which includes the display image RAM, the interdigit and multiplex counters, and control circuitry.

The two plasma displays, the block multiplex decoder, segment drivers and high voltage circuits are located on the Front PCB Assembly (400441). Figure 4.12 shows the arrangement and main interconnections of the display circuitry.

4.4.1 General (Fig. 4.12)

Basically, the Display Image RAM stores the current display data, which is read out to drive the display segments. A Display Block Counter generates a 4-bit count at 2kHz which scans the 11 digit-blocks of both displays in parallel. The same count scans the RAM, selecting segment information for each block in turn. As there are two displays, and therefore two RAM bytes to read for each block, the Mode display data is first entered into a holding latch during the inter-digit blanking period before its block is selected.

To update the displayed characters, the CPU writes into the RAM at high speed (680 kHz), using signal XDDSP to connect the Address bus through the Address Source Switch to the RAM. XDDSP also connects the Data Bus to the RAM through the Data Bus Buffers, writing the new segment data into the selected RAM Address. The high transfer speeds avoids spurious effects on the displays.

Each RAM address contains only 8 bits, but there are nine segments in each display block. Comma-segment information is therefore not written into its normal block address in the RAM, but stored as a bit in a separate "Comma" byte, which holds the data for all eight blocks which have a comma. The byte is read out into a Commas Data Holding Latch, once every block scan cycle, and then selected for display by a Commas Multiplexer 8-into-1 switch.

4.4.2 Static Conditions (Circuit Diagram 430441 sheet 2)

The plasma displays are driven from +5V (anode supply and -175V (cathode supply). The supplies are connected by conduction of anode driver transistors (Q10 – Q20), and cathode driver transistors (Q2 – Q9 and Q41 –Mode display, and Q33 – Q40 and Q42 – OUTPUT display).

When not selected, all anodes and cathodes are held at -70V by the action of 75V zener D17. When selected, a block anode driver conducts and lifts its two anodes to +5V. At the same time the segment cathodes selected for display are pulled to -175V by their cathode drivers, striking the discharge. Four keep-alive electrodes in each digit block (2 anodes and 2 cathodes) are maintained at +5V and -175V respectively. This ensures a rapid strike when a digit is energised, and helps to prevent inter-block "streaming".

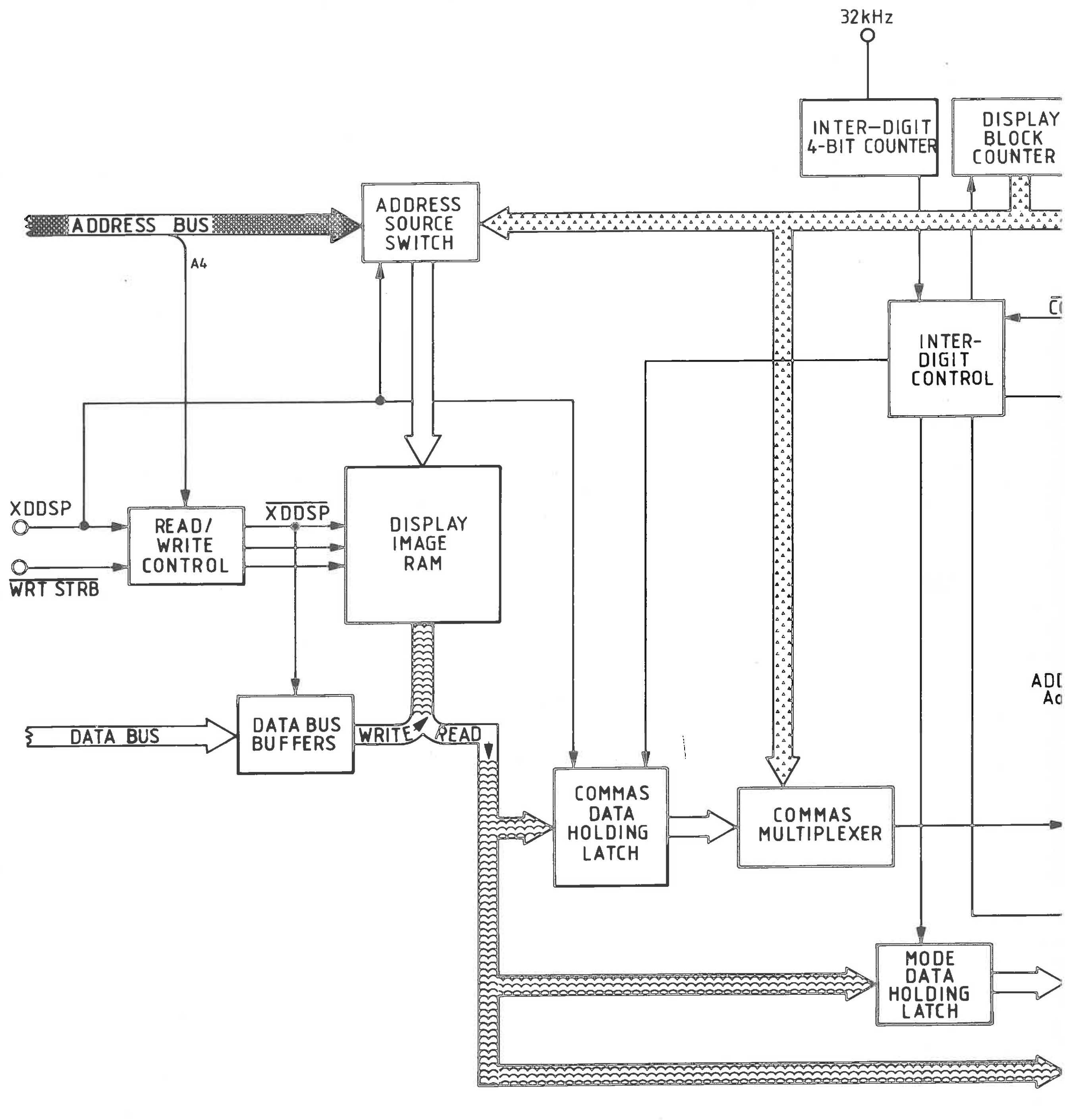
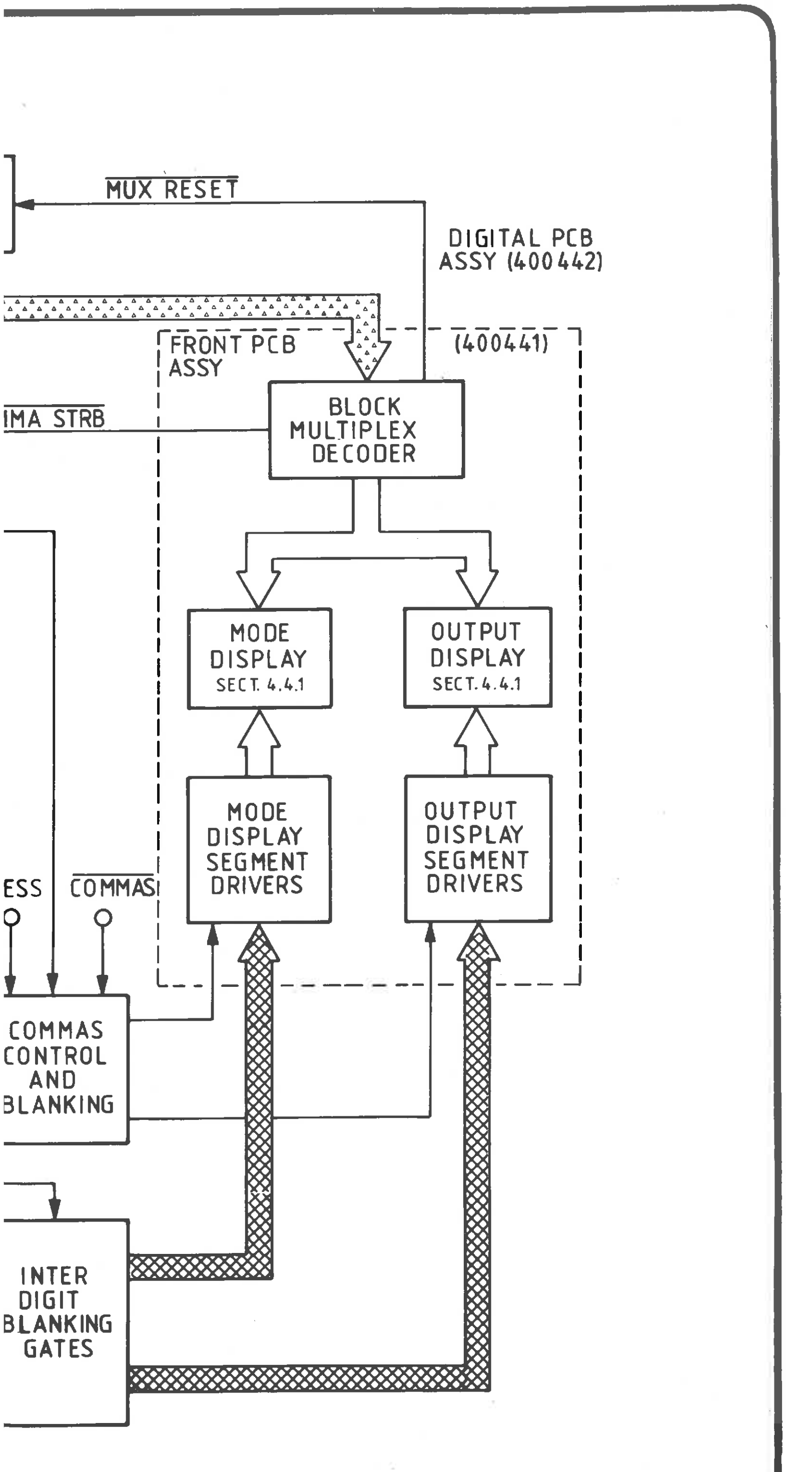


FIG. 4.12 MODE AND OUTPUT DISPLAYS – FUNCTIONAL BLOCK D



MUX RESET
DIGITAL PCB ASSY (400442)
FRONT PCB ASSY
(400441)
IMA STRB
BLOCK MULTIPLEX DECODER
MODE DISPLAY SECT. 4.4.1
OUTPUT DISPLAY SECT. 4.4.1
MODE DISPLAY SEGMENT DRIVERS
OUTPUT DISPLAY SEGMENT DRIVERS
ESS
COMMAS
COMMAS CONTROL AND BLANKING
INTER DIGIT BLANKING GATES

AGRAM

4.4.3 Write Mode (Fig. 4.13)

Whenever the CPU has cause to update a display (e.g. Range, Function, Mode or Value change) it sets address decode XDDSP to logic-1 with each byte of data to be transferred. This causes M31 and M33 to select the CPU address lines A_{4-0} which are mapped directly to the RAM address input lines A_{4-0}. The RAM is placed into its write mode by signal XDDSP at logic-0 (M17-8, TP5, M16-16)

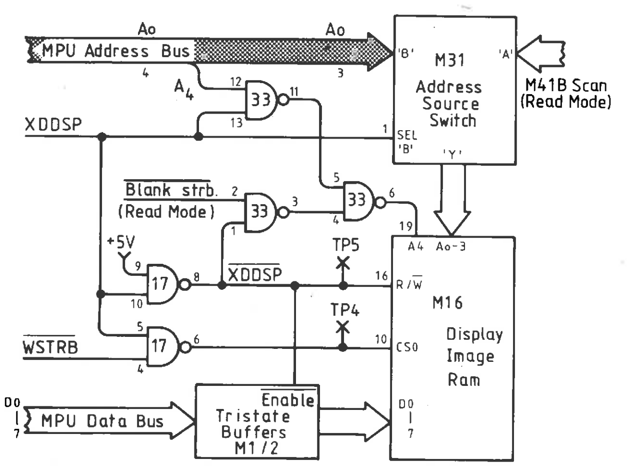


FIG. 4.13 RAM ACCESS – WRITE MODE LOGIC

The address line A_4 is used to differentiate between Output and Mode display images. If the CPU is loading the RAM with Output display data, it sets A_4 = 1, but for Mode or Comma display data, A_4 = 0 (M33-4 and 13 at Logic-1 in write mode).

The two images are written into separate sections of M16 memory. (In read mode the A_4 input (M16-19) is again used to differentiate between the two image sections)

The signal $\overline{XDDSP}$ (M17-8) enables the tri-state buffers M1 and M2, connecting the CPU data bus to M16 data input/output lines D_{0-7}. The CPU also generates the write strobe signal $\overline{WSTRB}$ with each byte of display data. This is combined with XDDSP (M17-6, M16-10, TP4) to enable M16 internal Input/Ouput tristate buffers to accept the data byte (chip select CSO). Once the display data has been loaded into the RAM, XDDSP remains at logic-0, and the RAM reverts to read mode.

4.4.4 Read Mode (Fig. 4.14)

Unless the CPU has data to update, the signal XDDSP remains at logic-0, to hold the display multiplexer circuitry in read mode. The RAM data bus is isolated from the CPU data bus by tristate buffers M1/M2 and M16 is chip-selected in read mode by M17-6 and 17-8 at logic-1.

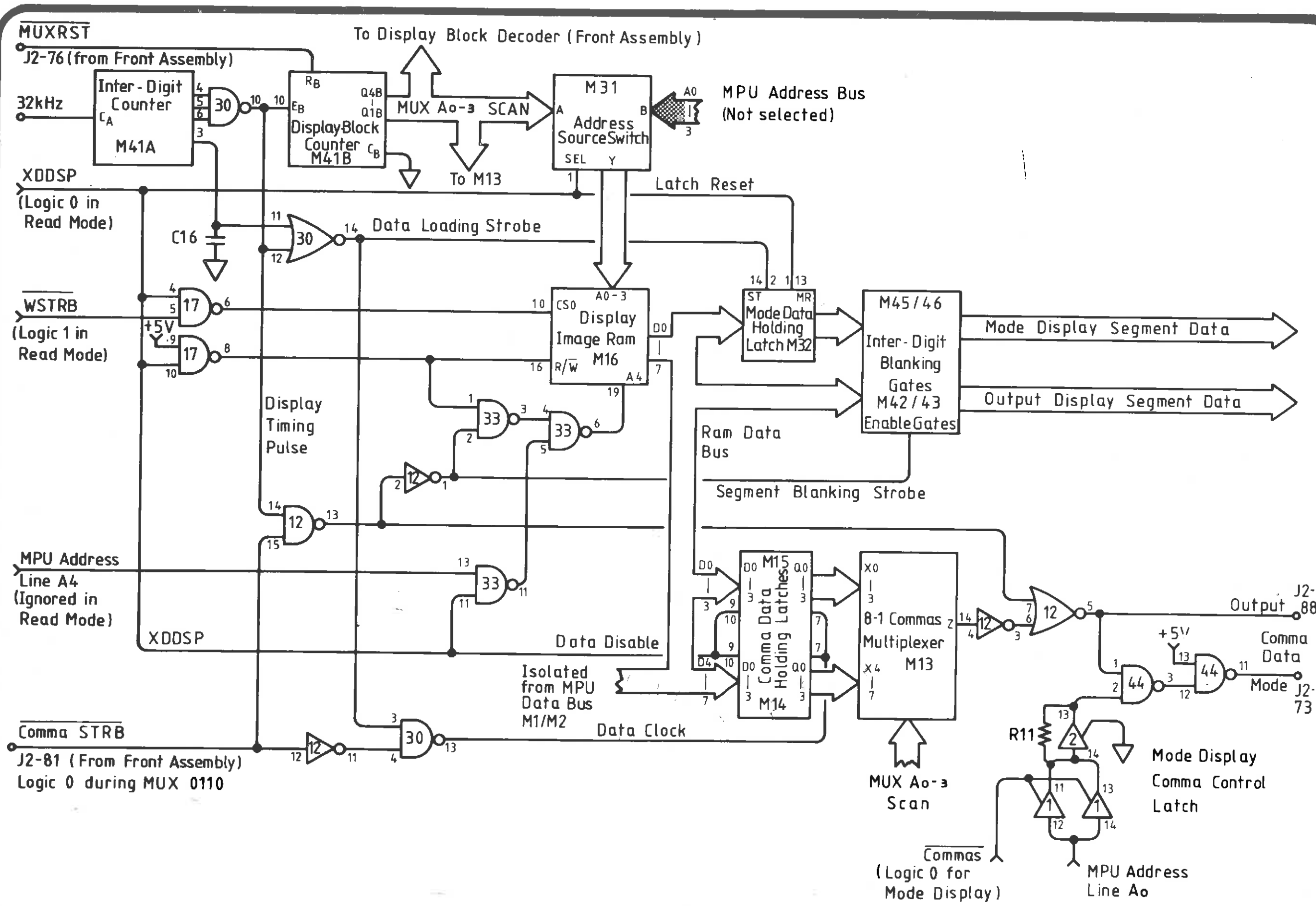


FIG. 4.14 READ MODE LOGIC – RAM ACCESS AND SEGMENT SWITCHING

4.4.4.1 Display Scan Address Interlacing (Fig. 4.15)

M31-1 (SEL) at logic-0 addresses the RAM from the display block scan, mapping M41B outputs: Q4B, Q3B, Q2B, Q1B to RAM address input lines: A_0, A_3, A_2, A_1 respectively. This provides interlacing of the extracted data to synchronize with alternate block selection by the Front Assembly Scan decoder.

4.4.4.2 Block Multiplex Decoding (Circuit Diagram 430441 Sheet 2)

The 4-bit Block scan output MUX A_{3-0} from the multiplex scan counter M41B (dig) is used at $DATA_{4-1}$ input to M3, which decodes it into a low-active 16-line scan S_{15-0}.

M3 output S_6 generates the comma strobe signal $\overline{\text{COMMA STRB}}$, S_{13} terminates each scan by resetting M41 B (dig) ($\overline{\text{MUX RESET}}$), and S_7, S_{14} and S_{15} are not used.

The other eleven outputs from M3 switch Q10 – Q20 on sequentially, to drive the anodes of both plasma displays in synchronism. The anodes of both displays are activated alternately to prevent inter-block "streaming". Figure 4.15 details the interlacing sequence.

MUX A_{3-0} SCAN A_3	A_2	A_1	A_0	M3 (Front Assy.) M3 Output (Low Active)	Energised Line (Both displays' Anodes and Signals)
M3 $DATA_{4-1}$ Input D_4	D_3	D_2	D_1		
M_{16} (Dig.Assy) A_{3-0} Input (Display Image RAM) A_0	A_3	A_2	A_1		
0	0	0	0	S_0	A_1
0	0	0	1	S_1	A_3
0	0	1	0	S_2	A_5
0	0	1	1	S_3	A_7
0	1	0	0	S_4	A_9
0	1	0	1	S_5	A_{11}
0	1	1	0	S_6	$\overline{\text{COMMA STRB}}$
0	1	1	1	S_7	Not used
1	0	0	0	S_8	A_2
1	0	0	1	S_9	A_4
1	0	1	0	S_{10}	A_6
1	0	1	1	S_{11}	A_8
1	1	0	0	S_{12}	A_{10}
1	1	0	1	S_{13}	$\overline{\text{MUX RESET}}$
1	1	1	0	S_{14}	Not included in cycle
1	1	1	1	S_{15}	($\overline{\text{MUX RESET}}$ at S_{13})

FIG. 4.15 DISPLAY SCAN ENERGISING SEQUENCE

4.4.4.3 Output and Mode Display Data Selection

When the processor writes display data into the Display Image RAM, the A_4 input is used to select the "Mode" or "Output" data storage area. In read mode, A_4 is set to logic-1 for the "Output" data memory and to logic-0 for "Mode" or "Comma" data. At any instant, 18 bits of data are required for the display:

One byte for the Output display block segments
One byte for the Mode Display block segments
Two bits for commas

The problem of transferring two bytes of data along the single-byte RAM data bus is overcome by strobing each Mode display segment byte into a holding latch (M32), during the first 30μS of its block selection period. The mode display section of the RAM is selected by setting its A_4 input to Logic-0 for this 'Inter-digit' period, during which the inter-digit blanking gates (M2/43, M45/46) set all segment lines to the Front Assembly at logic-0 (segments OFF). Commas are stored as a separate byte as described in section 4.4.4.6.

4.4.4.4 Display Timing (Fig. 4.16)

Read mode is driven by a 32kHz square wave (Waveform 'A', generated from the 13-bit counter in the Analog Interface Assembly M15-16), used as clock for a 4-bit counter (M41A). The three most-significant bits are combined at M30-10 to produce Waveform B, the display master-timing pulse, used also for Inter-digit blanking.

The following example explains how the display data is set up for the next display block in sequence, during the 62.5μSec of the display timing pulse.

Example: M41B count has already reached 1001, and the block 4 anodes of both displays are energised (Fig. 4.15). The Output display data for block 4 is selected in the display image RAM (M16) to drive the segment cathodes for a figure "6", which appears on the output display. Block 4 of the mode display is showing a figure "3", and the data for this is being output from the Mode display holding latch (M32). The data held in M16 for the next byte (Block 6 of both displays) is: Figure "8" (output display) and figure "7" (mode display). The changeover to the next block occurs during the display master timing pulse (Fig. 4.16, Waveform B).

(a) The negative-going leading edge triggers the scan counter (M41B) whose output advances to 1010 (block 6). On the Front Assembly, M3 de-energises A_4 anodes and energises A_6 anodes.

(b) For the duration of the display master timing pulse (Logic-0 at M12-14), the A_4 input to M16 is set to logic-0 as A_{3-0} inputs are advanced to 0101. Mode display data for figure "7" is loaded onto the RAM data bus as follows:

(i) M17-6 at logic-1 chip-selects M16 at M16-10,

(ii) M17-8 at logic-1 holds M16 in Read mode,

(iii) RAM address $A_{4\text{-}0}$ = 00101 loads block 6 Mode display data byte onto the RAM data bus (M1/M2 isolates from the CPU data bus),

(iv) M30-14 at logic-1 strobes the byte into M32 during the 30μS of waveform D, then returns to logic-0 leaving figure "7" data latched at M32 output

(v) M12-1 at logic-0 blanks the two displays by setting M45/M46/M42/M43 outputs at logic-0, regardless of their inputs from M32 and the RAM data bus.

(c) The positive-going edge of waveform B lifts the RAM A_4 input (M16-19) to logic-1, addressing the Output display section of memory. $A_{3\text{-}0}$ is still at 0101, selecting block 6 display data (in our example a figure "8"), which it loades on to the RAM data bus. The end of the master timing pulse also releases the blanking by enabling M42/43 and M45/46, so the display data for both Mode and Output displays are now delivered to the correct cathode drivers on the Front Assembly, to strike the gas discharge in the two blocks A_6. This condition persists for 437.5μS until the next master timing pulse, when waveform B repeats the process for the next block of stored display data.

At any time during the cycle, the CPU can re-activate write mode. This does not disturb the scan from M41B, but XDDSP resets M32 outputs to logic-0 (M32 — 1/13). The speed of byte transfer from the CPU ensures that spurious information is not visible on the Output display, but each display will follow its new stored data.

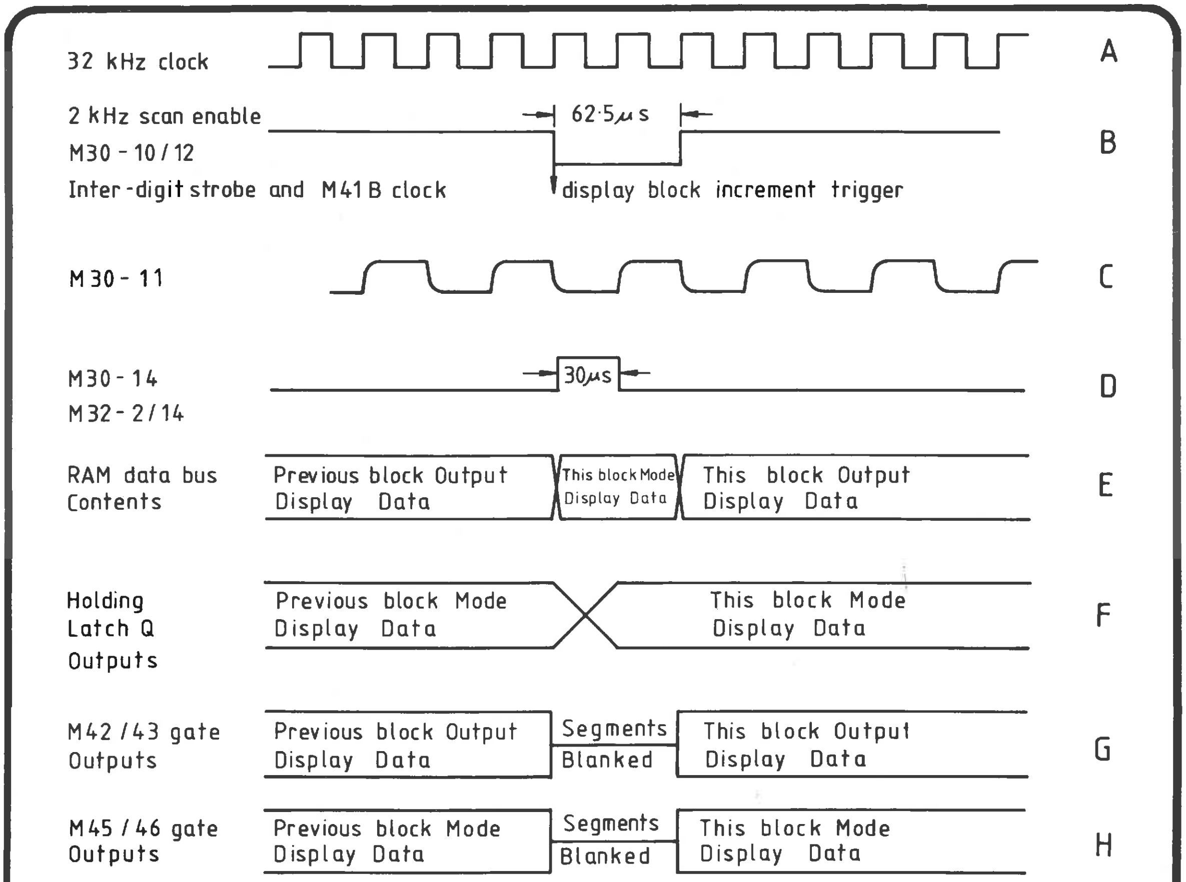


FIG. 4.16 DISPLAY TIMING WAVEFORMS

4.4.4.5 Display Segment Drive

The strobed segment signals from the Digital assembly are input to the Front Assembly on J1 — 67 to J1 — 75 (MODE display) and J1 — 82 to J1 — 90 (OUTPUT display). These are already synchronised to their blocks by the 4-bit block scan MUX $A_{3\text{-}0}$ within the Digital assembly.

For each block in sequence, the appropriate segment bit-pattern is set at the input to the segment drivers. For bits at logic-1, the rise is passed through line capacitors to reverse-bias DC restoration diodes and forward bias their driver — transistor bases. The resultant collector currents pull the segment cathodes from their quiescent -70V, to -170V. The correct block anode is simultaneously lifted from -70V to +5V by its anode driver transistors, striking the gas discharge and displaying its digit. For bits at logic-0 the cathode drivers remain cut off.

The driver emitter resistors control the segment cathode currents for uniform brilliance.

During changeover between blocks, all segment inputs at logic-1 are returned to logic-0 by the inter-digit blanking strobes M42, 43, 45 and 46 (dig). This turns off the drive transistors and blanks the display. As the scan frequency is high enough, the blanking is not observed on the display.

4.4.4.6 Comma Logic (Fig. 4.17 and Circuit Diagram No. 430442 Sheet 1)

The comma is the ninth segment (i) in each of the numerical display blocks. It cannot fit into a block's byte in memory, as there are only eight bits per byte. Although there are nine numerical blocks, the ninth block does not require a comma, and segment i in blocks A_{10} and A_{11} are not connected. So the full comma information (8 bits) can therefore be stored in a single byte of memory in the RAM. (RAM address 01100). This is updated by the CPU in write mode, and is read out (as though it were another display block) by M41B scan 0110 during the master display pulse (waveform B sets RAM A_4 input to logic-0). The same MUX combination 0110 selects S_6 output from M3 decoder on the Front Assembly, which sets the signal COMMA STRB to logic-0. Thus for the duration of S_6 = 0 (500μS), the common data is on the RAM data bus but the blanking gates prevent it reaching the display segments a – h.

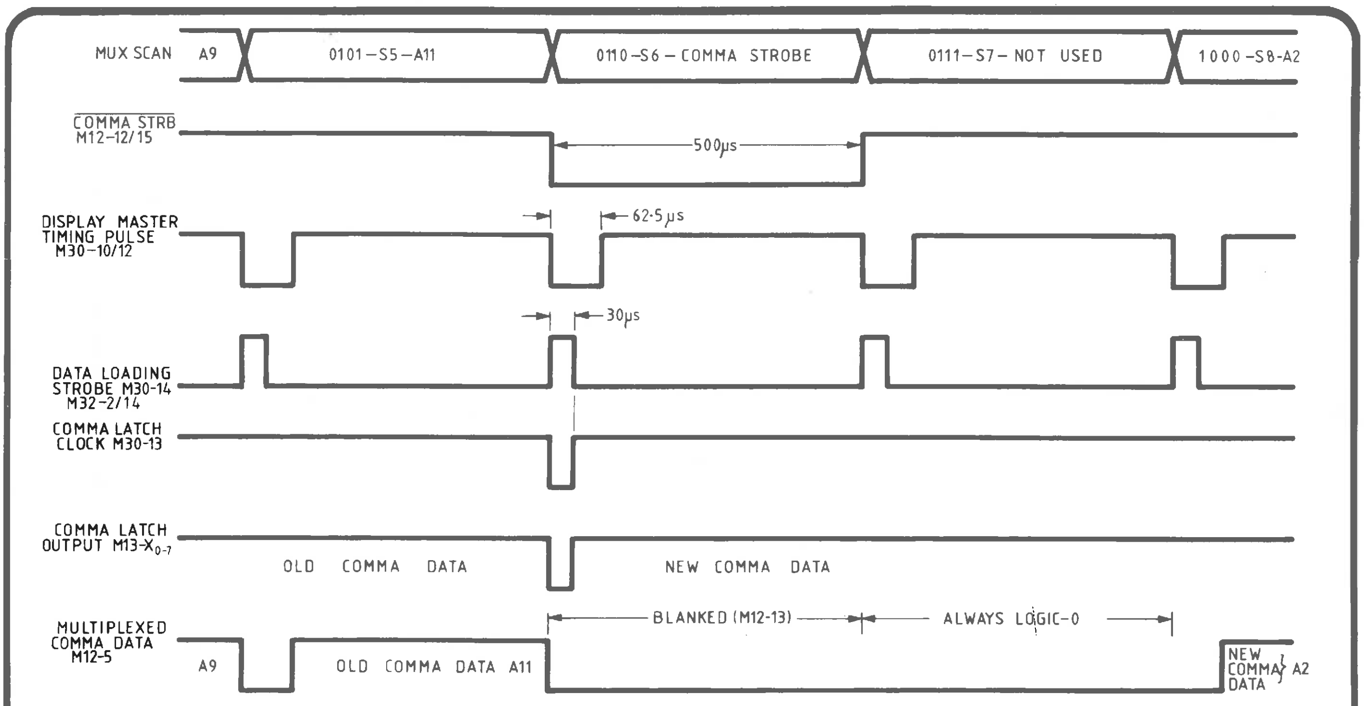


FIG. 4.17 COMMA LOGIC – TIMING WAVEFORMS

4.4.4.7 Comma Drive Multiplexing

Signal $\overline{\text{COMMA STRB}}$ is also inverted and combined with the Data Loading Strobe at M30-13 as a logic-0 pulse, whose positive-going edge clocks the comma data into latches M14/15, approx. 30μSec after it has been loaded on to the RAM data bus. The permanently-enabled outputs from these latches are input as X_{0-7} into the 8-into-1 multiplexer M13 for a complete MUX scan until the next $\overline{\text{COMMA STRB}}$ signal. The block-multiplex scan from M41B selects the correct X input to synchronise with activation of its display block anode. This is output from M13-14 (Z), into blanking gates M12. Comma information is blanked during $\overline{\text{COMMA STRB}}$ and by inter-digit blanking during display-block changeover (M12-7). The comma drive line, from M12-5 to the front panel via J2-88, controls segment "i" cathode driver for the Output display. If commas are required on the Mode display (e.g. in "Offset" Mode) they are always in the same display blocks as the Output display. The CPU pulses the $\overline{\text{COMMAS}}$ line to logic-0 at the same time as Address line A_0 goes to logic-1. Tristate buffer outputs M1-11 and 13 go to +5V, setting M2-13 output to +5V (logic-1). Outputs M1-13 and 11 go tristate when the $\overline{\text{COMMAS}}$ line returns to logic-1, leaving M2-13 latched to +5V by the positive feedback action of R11. So M44-2 enables the comma data to the Mode display segment driver via J2-73 to copy the Output display commas on to the Mode display. When mode display commas are not required, A_0 is set to logic-0 (0V) with $\overline{\text{COMMAS}}$ signal at logic-0. In this case M2-13 is latched to logic-0 and M44-2 disables the flow of comma data to the Mode display.

4.5 ANALOG CONTROL INTERFACE

The circuitry described in this section performs the following functions:

(1) Provides a two-way interface via a serial data link between out-guard digital processing and in-guard analogue control circuitry on the reference divider pcb. (See Fig. 4.18)

(2) Monitors the CPU operation, serial transfer, digital supply failure and restart operations (watchdog), imposing a controlled safety default condition if there is a danger of losing digital control of the analogue functions.

A manual reset of the safety monitor is provided on the front panel. (See Fig. 4.21)

4.5.1 General

Safety and Control information is input from Digital (400442) and Front (440441) Assemblies to out-guard circuits located on the Analogue Interface Assembly (400443), processed and transferred across the "Guard" isolation barrier to in-guard circuits in the Reference Divider Assembly (400444). After further processing in the Reference Divider Assembly, safety and control information is output to the DC Assembly (400445), I/Ω Assembly (400448) and PA (DC) Assembly (400449).

Certain selected "Status" signals, originating in the analogue assemblies, are returned to the CPU during the data transfer. Thus, the data link forms a forward and return loop, as illustrated by Fig. 4.18.

4.5.2 Serial Data Transfer (Fig. 4.18 and Circuit Diagrams Nos. 430442 Sheet 2, 430443 Sheet 3, 430444 Sheets 4 and 5)

A bi-directional serial data link passes information across the guard isolation screen; conveying instructions from the CPU to control the in-guard analogue circuitry, and transferring critical status signals from the guarded circuits back to the CPU. The link is managed by a synchronous serial data adapter (SSDA) which, having first been loaded with three bytes of control instructions by the microprocessor; transmits the resultant 24-bit word across guard one bit at a time, via its Tx DATA channel. The 48 bits necessary to control the analogue circuitry thus require two successive 24-bit transmissions. Simultaneously with each 24-bit transmission, the SSDA receives a 24-bit word via its Rx DATA channel, enabling the CPU to obtain the status of the analogue functions.

4.5.2.1 The Transfer Cycle (Fig. 4.18)

The CPU uses an address-code signal $\overline{\text{AN I/F STRT}}$ to initiate each 24-bit shift, by triggering a separate clock generator (M2, M3, M4) which produces a burst of 24 clocks per shift. Data is clocked in a serial string through the 48-bit, serial in/parallel out, analogue control shift register; through the 16-bit, parallel in/serial out, status shift register; and back to the SSDA receiver interface in a continuous loop. The serial data string is correctly located after two 24-bit shifts, so then the SSDA generates a strobe pulse which:

(1) Latches the data present in the serial data string of the six 8-bit analogue-control shift registers (M27, M25, M31, M19, M30, M15) into their enabled parallel output registers and onto the analogue control bus.

(2) Injects the status data at each of the parallel inputs of the two 8-bit status shift registers (M18, M22) into corresponding locations in the serial data string. When the strobe ends, the parallel inputs to the status registers are disabled.

After the strobe pulse, the CPU initiates a further circulation of serial data (including the status data); in order to confirm that the data latched onto the analogue control bus was without error, and to obtain the status data. This requires three more 24-bit shifts, so a complete data transfer consists of five shifts if no error is detected.

If an error is detected on the first transfer, the CPU activates a second, and then a third transfer if an error is detected on the second. If the error persists after the third transfer, the instrument will shut-down under the control of the watchdog safety monitor. With no error, the SSDA provides a trigger-enable to allow updates to the watchdog circuits.

All interfacing between out-guard and in-guard circuits is achieved using electrically-isolating opto-couplers.

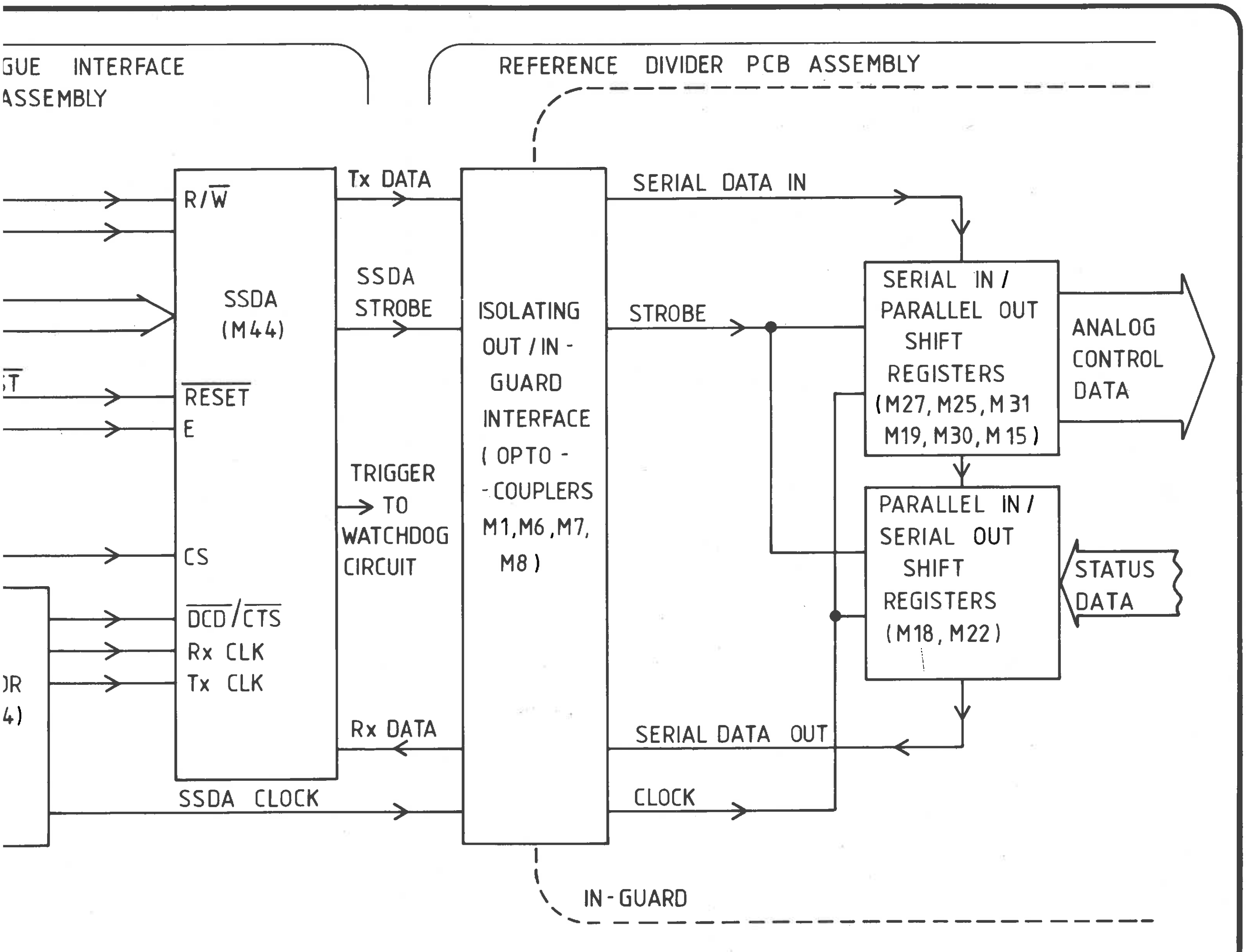


FIG. 4.18 SERIAL DATA LINK — SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

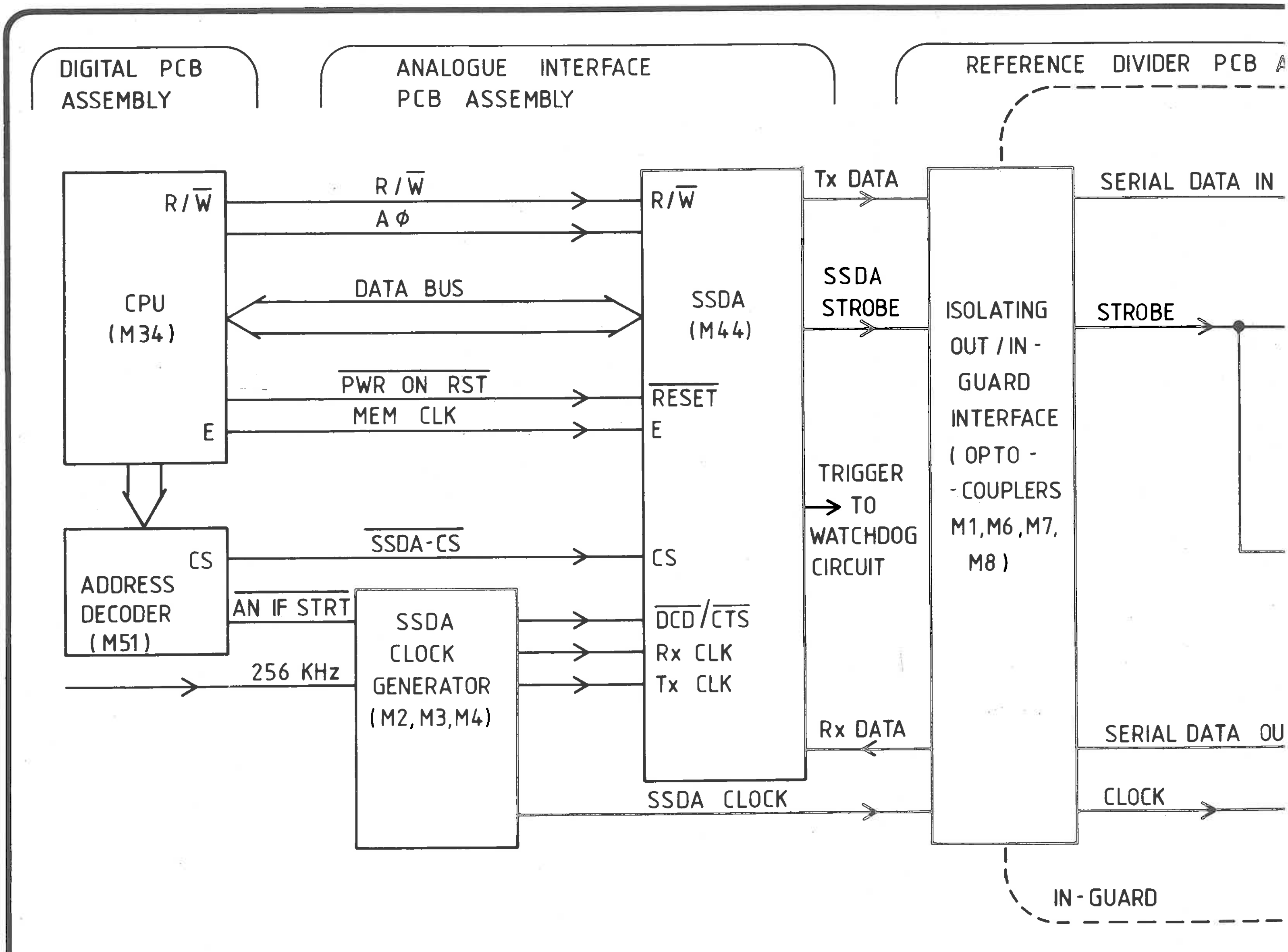


FIG. 4.18 SERIAL DATA LINK — SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

4.5.2.2 Data Transfer Organization (Fig. 4.19)

Data is transferred serially via the SSDA, control registers and status registers under the control of the CPU. The exchange of data between the CPU and SSDA is made on the 8-bit instrument data bus, each exchange comprising three bytes (24 bits) of data. The serial shifts of data are synchronized by clocks which are controlled from the CPU, and the SSDA receiver registers are cleared when read by the CPU. Transfer of the serial data to the parallel outputs of the control registers, and transfer of status data from the parallel inputs of the status registers to the serial data string; is enabled only when a strobe is generated by the SSDA. The transfer operation requires five serial data shifts, each of three bytes, through the registers. During this operation: the control registers are loaded with bytes of new data (ND); the status registers are loaded with new status data (NS); and the whole of the ND and NS data is returned to the CPU. The CPU verifies that the data transfer has been made with no error and acts upon the status data received.

4.5.2.3 Transfer Sequence

The sequence of events in the transfer operation is as follows, refer to Fig. 4.19:

(A) Three bytes of new data, ND1, 2 and 3 are loaded into the SSDA transmitter registers; this data is destined for control registers D1, 2 and 3. The SSDA receiver registers were cleared when last read by the CPU.

(B) A burst of 24 clock pulses, initiated by the CPU, shifts all data three bytes to the right. After the shift is completed, the transmitter registers are loaded with new data bytes ND4, 5 and 6 (destined for control registers D4, 5 and 6). During this period, no transfers are made between the serial data string and the parallel control or status registers.

(C) A second burst of 24 clock pulses again shifts all data three bytes to the right. New data bytes ND1 to 6 are now correctly positioned in control registers D1 – D6. After completion of the shift, three dummy bytes are loaded into the transmitter registers. Old data (OD) in the receiver register is ignored.

(D) With new data bytes ND1 to 6 correctly located, the SSDA generates a strobe pulse. This pulse:

(1) latches the 48 bits of bytes ND1 to 6 at the parallel outputs of control registers D1 to 6;

(2) enables the parallel inputs of status registers S1 and 2, loading two new status bytes NS1 and 2 and clearing old data OD5 and 6 from the registers.

(E) A third burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes NS1, NS2 and ND1 from the SSDA receiver registers (the CPU may take immediate action on NS returns). After the shift is complete, new data bytes ND1, 2 and 3 are re-loaded into the transmitter registers.

(F) A fourth burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes ND2, 3 and 4 from the receiver registers. After the shift is complete, new data bytes ND4, 5 and 6 are re-loaded into the transmitter registers.

(G) A fifth burst of 24 clocks again shifts all data three bytes to the right. Bytes ND5 and 6 are read from the receiver registers. The CPU has now read all new data and status bytes and the transfer sequence ends. If an error is detected between new data transmitted and new data received, the transfer process is repeated; three attempts are allowed before a fault condition is declared.

4.5.3 Synchronous Serial Data Adaptor (Circuit Diagram 430443, Sheet 3)

4.5.3.1 SSDA Initialization

When power supplies are first switched-on or an external reset EXT RST is applied, the signal $\overline{\text{PWR ON RST}}$ is held at logic-0 for approximately 8mS. During this period, the SSDA is latched in a reset condition to prevent erroneous output transitions at its Tx and Rx interfaces; the internal transmit registers are inhibited to prevent the loading of data from the data bus and the SSDA strobe output is held at logic-1. After $\overline{\text{PWR ON RST}}$ returns to logic-1; the latches, registers and SSDA strobe are cleared in software, during the initialisation routine.

4.5.3.2 Parallel Data Input from CPU

The conditions for parallel data on the data bus to be accepted by the SSDA are as follows:

(1) Chip-select $\overline{\text{SSDA}}$ CS at logic-0.

(2) Read/Write command R/$\overline{\text{W}}$ at logic-0. This controls the direction of data flow via the Data Bus through the SSDA input/output port. When R/$\overline{\text{W}}$ is at logic-0, data on the Data Bus is written into a selected register within the SSDA.

(3) The memory clock "MEMCLK" 682.6 kHz square wave is present to synchronise the SSDA operating cycle to that of the CPU.

With input conditions present as above and register address bit Aϕ at logic-1, the SSDA accepts data from the data bus into an internal 3-byte FIFO register. The data is entered over several MEMCLK cycles and stored in the FIFO register in readiness for serial transmission from the SSDA.

Software programming of the SSDA is performed when the address bit Aϕ is at logic-0. For details of "Control Byte" operation, refer to Motorola 6852 data sheet.

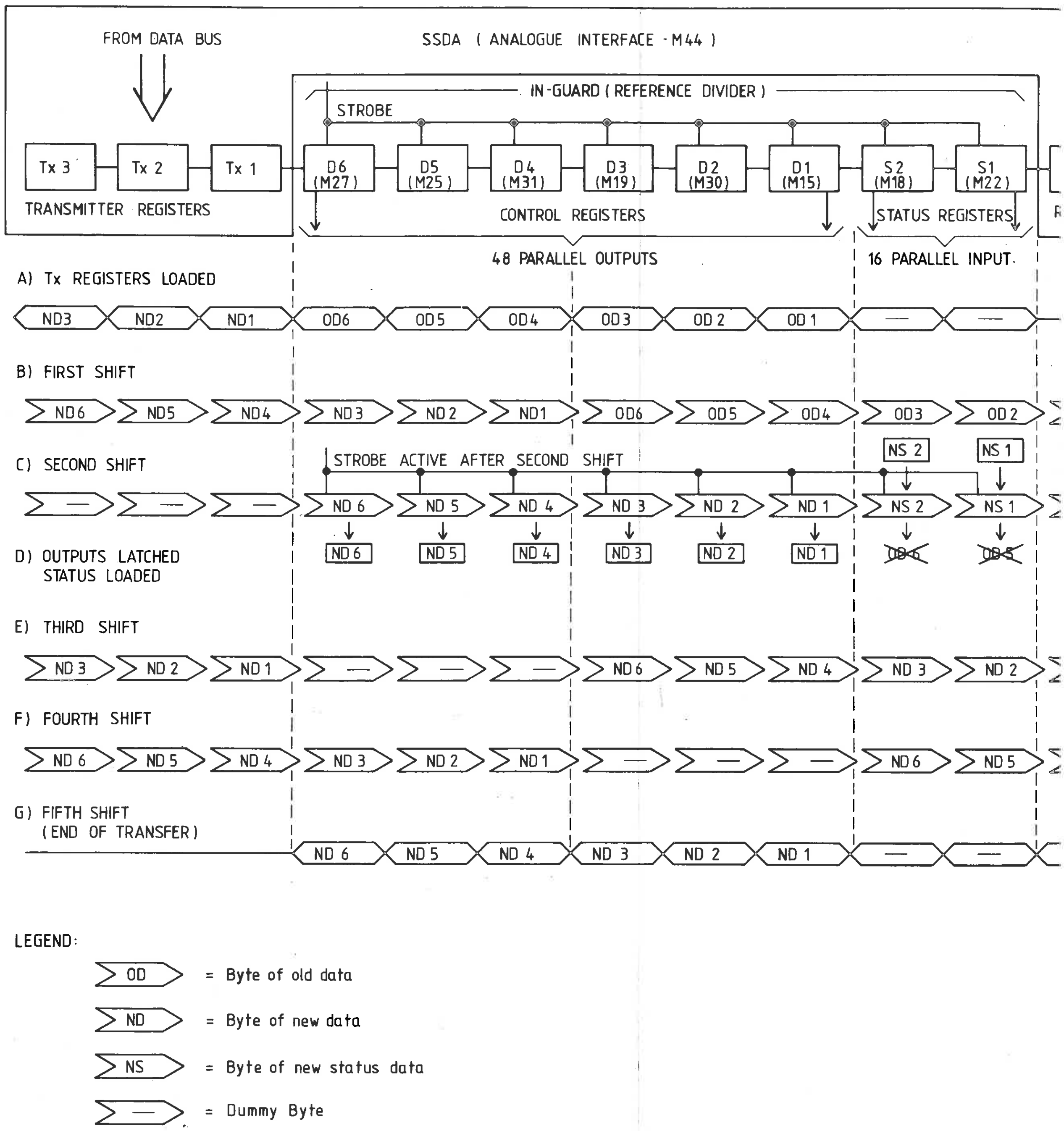
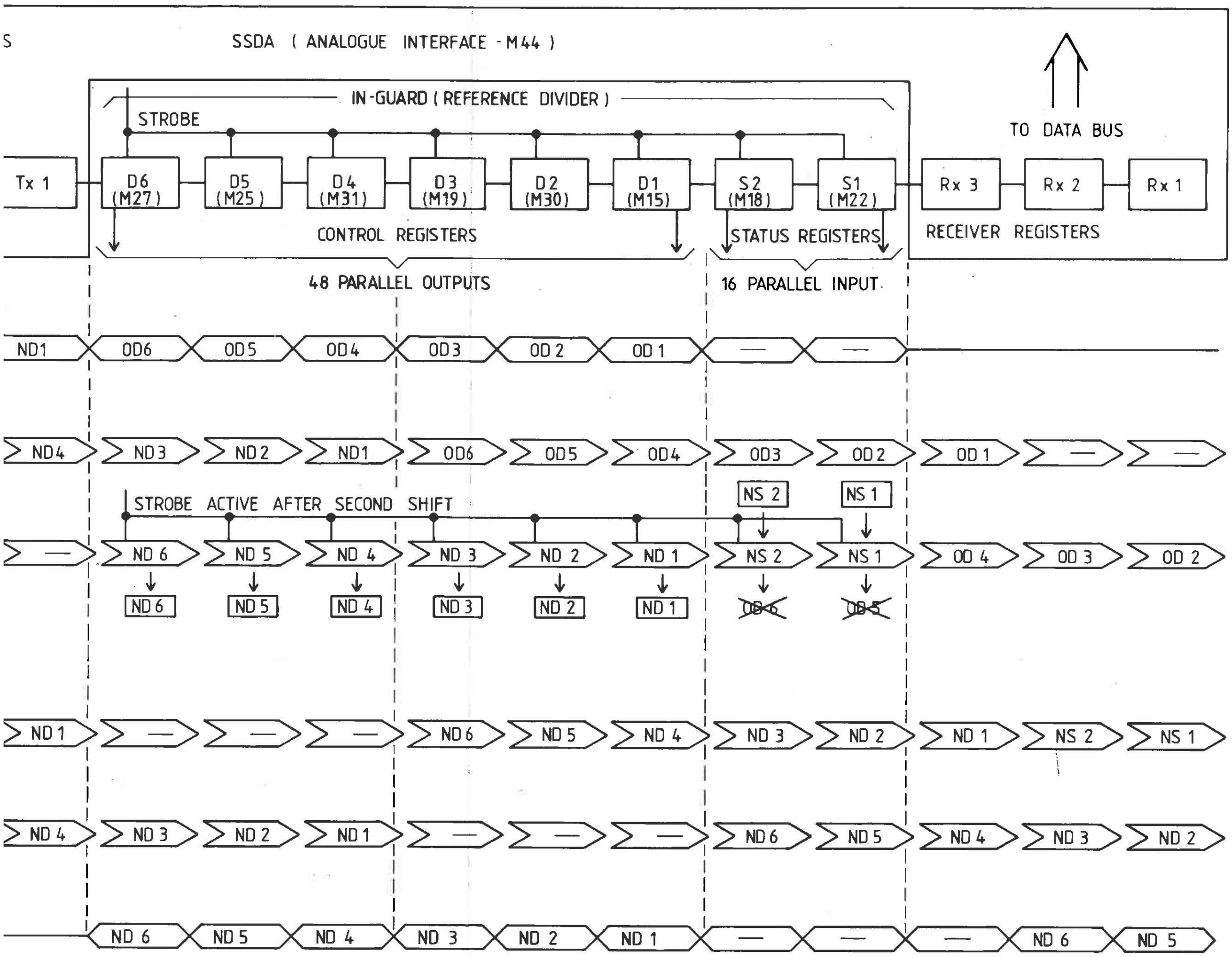


FIG. 4.19 SERIAL DATA TRANSFER ORGANIZATION



Byte of old data

Byte of new data

Byte of new status data

Dummy Byte

FIG. 4.19 SERIAL DATA TRANSFER ORGANIZATION

4.5.3.3 Parallel Data Output to CPU

The conditions for data to be read from the SSDA on to the data bus are as follows:

(1) Chip select $\overline{\text{SSDA CS}}$ at logic-0.

(2) Memory clock, MEM CLK, present.

(3) Read/Write command R/$\overline{\text{W}}$ at Logic-1.

The data read from the SSDA may be from one of two sources, selection being made by the address bit Aϕ. With Aϕ at logic-1, received data from the serial data input FIFO is transferred to the data bus; with Aϕ at logic-0, an internal status register is read.

4.5.3.4 Serial Data Transmission

Serial data transmission is controlled by the $\overline{\text{CTS}}$ (clear to send) input to the SSDA. Transmission is inhibited by $\overline{\text{CTS}}$ at logic-1, and enabled when $\overline{\text{CTS}}$ is set to logic-0 by the CPU address-code signal $\overline{\text{AN I/F STRT}}$. The first serial bit is transmitted by the negative transmission of the first full positive Tx clock pulse (256 kHz) after $\overline{\text{CTS}}$ has been set to logic-0. $\overline{\text{CTS}}$ is held at logic-0 by the $\overline{\text{AN I/F STRT}}$ latch for the duration of 24 full Tx clock pulses, thus enabling the serial shift transmission of the 24 data bits from the Tx Data FIFO in the SSDA.

4.5.3.5 Serial Data Reception

Serial data is received by the SSDA, controlled by the $\overline{\text{DCD}}$ (data carrier detect) level and clocked by Rx CLOCK. $\overline{\text{DCD}}$ is common to the transmit control $\overline{\text{CTS}}$ so that transmission to, and reception from the serial/parallel shift registers is synchronous. Both Rx CLOCK and Tx CLOCK have the same frequency but Rx CLOCK is inverted with respect to the latter. The first bit arriving at its Rx DATA input is clocked into the SSDA Receive FIFO register on the positive transition of the first full Rx clock after $\overline{\text{DCD}}$ is set to logic-0.

4.5.4 SSDA Clock Generation

Serial data is transmitted and received in bursts of 24 data bits. Three clocks are used to time the flow of bits, ensuring that:

(1) Data has time to settle before being clocked along the shift registers.

(2) The first Rx data sample is taken before it is lost by the first bit-shift.

(3) Subsequent Rx data has time to settle before being sampled by the SSDA.

(4) Exactly 24 bits are shifted in each burst.

4.5.4.1 SSDA, Tx and Rx Clock Action (Fig. 4.20)

The three clocks are derived from the 256 kHz square wave output from the 13-bit counter (Circuit drawing No. 430443 sheet 2): The 256 kHz squarewave is used directly as "Tx clock" into the SSDA. The negative transition of the first full positive pulse after $\overline{\text{CTS}}$ is set to logic-0; triggers the first serial Tx data bit setup (Refer to Fig. 4.20 waveforms G and H).

"Rx clock" is an inverted version of the 256 kHz squarewave. The positive transition of the first full Rx clock cycle, after $\overline{\text{DCD}}$ is set to logic-0; triggers the SSDA to sample the first Rx data bit before the first SSDA clock has triggered the shift registers. (Refer to Fig. 4.20 waveforms K and J)

"SSDA clock" is also an inverted version of the 256 kHz squarewave. The inversion allows approx. 2mS of data setup time for all serial data bits prior to clocking the data along the shift registers. SSDA clock is gated at M2-3 by the action of M3-12 to ensure that the first Rx data is sampled before it is lost by the first bit-shift. 24 SSDA clock pulses are counted by M4, allowing 24 bits to be shifted before resetting AN I/F start latch M2-11 (TP3) to logic-1. (Refer to Fig. 4.20 waveform I).

4.5.4.2 SSDA Clock Circuitry (Circuit Diagram 430443 Sheet 3)

The following paragraphs describe the action of the SSDA clock generator circuitry.

The action of the SSDA clock generator is initiated by the command $\overline{\text{AN I/F STRT}}$ from the CPU. This occurs after the parallel data has been loaded into the SSDA transmit registers from the data bus. The logic-0 pulse of $\overline{\text{AN I/F STRT}}$ sets flip-flop M2-10/11 to give a logic-0 at TP3 which then:

(1) Sets the D input level of flip flop M3-5;

(2) Removes 'set' to enable flip-flops M3 at M3-6 and M3-8;

(3) Removes 'reset' to enable counters M4 at M4-7 and M4-15. (Refer to Fig. 4.20 Waveforms And C)

At the next rising edge of the inverted 256 kHz (Rx clock) from M43-8 after $\overline{\text{AN I/F STRT}}$, the two flip-flops M3 are clocked but only M3-1 "Q" output changes state to logic-0. This is applied to the SSDA $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs, thus releasing the inhibits on the SSDA transmit and receive registers. (Refer to Fig. 4.20 Waveforms D and E). At the next (second) rising edge of the clock to flip-flop M3, M3-12 changes to logic-1. This allows NAND M2-3 to pass 256 kHz clock pulses via buffer M5-12 to the reference divider pcb for the analogue-control and status shift registers. (Refer to Fig. 4.20 Waveforms D, F and I). The 256 kHz clock at NAND M2-3 is applied to the 4-bit up-counter clock input at M4-1, each rising edge causing the counter to increment by 1. The divide-by-16 output M4-6 is applied to the enable input at M4-10; the falling edge of this output occurs at count-16 and increments the second counter to give, at M4-11, a logic-1 output. At count-24, M4-6 changes again to logic-1, and together with M4-11 output, gives a logic-0 from NAND M2-4, causing the following actions:

(1) Flip-flop M2-12 is reset to give logic-1 at TP3.

(2) The logic-1 at TP3 sets flip flops M3 to give: logic-1 at M3-1, thus inhibiting $\overline{DCD}$ and $\overline{CTS}$; and logic-0 at M3-12, stopping NAND M2-3 passing any further SSDA clocks.

(3) The logic-1 at TP3 resets the up-counters M4 causing: the counter outputs to fall to logic-0, inhibiting further counting; and NAND M2-5 to logic-1, pre-setting flip-flop M2-12 to prepare for the next $\overline{\text{AN I/F STRT}}$ input. (Refer to Fig. 4.20 Waveforms I, B, C, E and F).

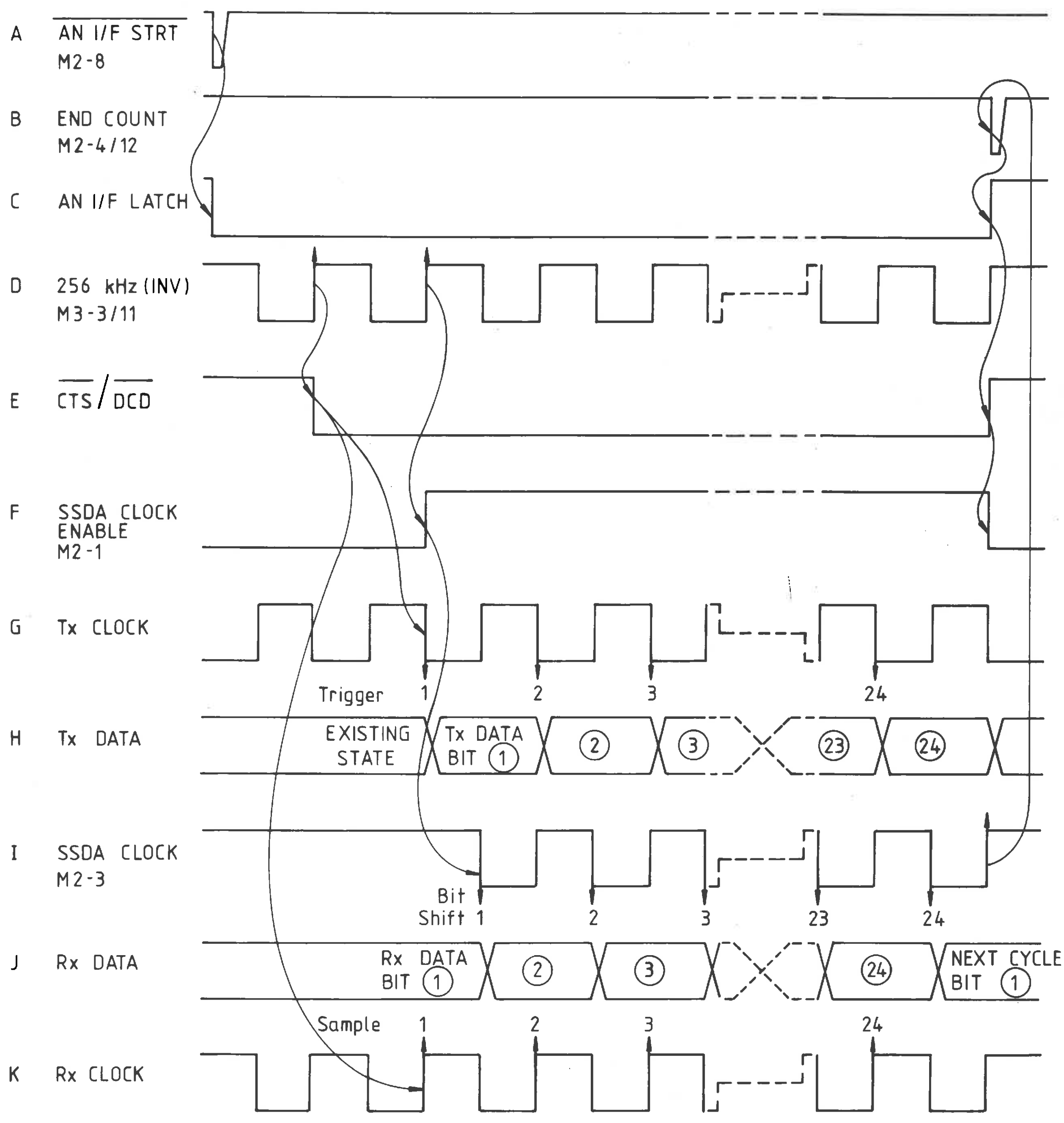


FIG. 4.20 SSDA CLOCK GENERATOR WAVEFORM

4.5.5 Serial/Parallel Data Converter (Circuit Diagram No. 430444 Sheet 4 and Sheet 5)

Serial control data transmitted from the SSDA (Analogue Interface Assembly), together with its control signals (SSDA strobe and SSDA clock), enters the Reference Divider Assembly via the Mother pcb.

The data and signals cross the isolation barrier through opto-isolators M6, M7 and M8 into guard.

Serial control and status data is returned out of guard to the SSDA receiver via opto-isolator M1.

4.5.5.1 Logic Levels

The nominal logic levels used in the out-guard SSDA circuits (logic-1 = +5V, logic-0 = 0V) are offset at the opto-isolator outputs to logic-1 = 10V, logic-0 = 15V; and level-shifted to logic-1 = 0V, logic-0 = 15V for the in-guard circuitry.

4.5.5.2 Serial-in/Parallel-out Control-Data Converters

Six 8-bit serial shift registers M27, M25, M31, M19, M30 and M15 each have latchable parallel outputs. Their serial "D" inputs and "Q's" outputs are cascaded to form a single 48-bit serial shift register. M27 receives "serial data in" from M8 via level-shifting buffer M36-4, and M15 passes serial data on to the Parallel-in/Serial-out Status-Data converters.

4.5.5.3 Parallel-in/Serial-out Status-Data converters

Two 8-bit serial shift registers M18 and M22 each have parallel inputs. M18 serial "Ds" input accepts serial data from M15; M18 "Q8" output is cascaded to M22 "Ds" input; and M22 "Q8" output delivers "serial data out" to buffer M11-11 and back to the SSDA via M1 opto-isolator.

M18 and M22 thus form a 16-bit serial shift register whose 16 parallel inputs states can be inserted into the serial data string.

4.5.5.4 Serial Data Cycling

The serial data, organised in five blocks of three bytes (Refer to Section 4.5.2.2) is accompanied by synchronized bursts of 24 clock pulses. The latter are buffered from opto-coupler M7 via level-shifter M36-2 and then inverted at M14-6, to ensure that all bits of serial data distributed throughout the shift registers have had time to stabilise before being clocked on. Subsequent bursts of data and clock pulses continue under the control of the CPU until the six control registers M27, M25, M31, M19, M30 and M15 are filled with their correct data. A strobe from the SSDA now latches the data in the registers' parallel outputs and at the same time, enables the parallel inputs of status registers M18 and M22, allowing these two registers to fill with status bits. At the end of the strobe period, the parallel-serial status data transfer and serial-parallel control data transfer are disabled.

The control and status bits in the registers are then circulated by further bursts of clock pulses, until the CPU has read the returned status bits and all the control bits that were latched at the control register outputs. Verification that the control data received was the same as the data sent ends the transfer.

If after three attempts the returned data does not match the transmitted data the CPU omits to retrigger monostable M10 on the reference divider pcb, which times out and allows $\overline{\text{BARK DEL}}$ to go to logic-0. This isolates the 48 parallel data outputs by "tri-stating" the registers M27, M25, M31, M19, M30 and M15.

4.5.5.5 Parallel Control-Data Outputs and Status-Data Inputs

The operation of these control lines is described in the sub-sections relevant to their destinations.

As this is a multi-purpose converter, designed for use in more than one model of instrument, some of the control lines are not used.

4.5.6 Safety Monitor (Watchdog) (Fig. 4.21)

The watchdog circuits provide a continuous monitor of the CPU/SSDA functional process. Detection of a processor malfunction by the watchdog results in the following actions:

BARK. This removes the 16 kHz power amplifier drive signal.
$\overline{\text{BARK}}$. This is returned as a status bit to the CPU via the SSDA to signal a failure.
BARK DELAYED. This occurs 47mS after BARK and is used to switch the power amplifier into the low voltage condition.
$\overline{\text{BARK DELAYED}}$. This disables the registers of the serial/parallel data converters.
The watchdog outputs are manipulated by the power-on reset circuits as follows:

(1) BARK DELAYED and $\overline{\text{BARK DELAYED}}$ are held active for 80mS from power-on and then are allowed to the inactive state only after two SSDA strobes have been detected.

(2) BARK is forced active until CPU/SSDA gunctioning has been verified; the latter must occur within 470mS of power-on.

(3) $\overline{\text{BARK}}$ is held inactive for 470mS from power-on, after which it provides a FAIL message to the CPU.

Operation of the Safety Reset control on the front panel provides a further 100 mS period for the CPU/SSDA functional process to settle, during which time the watch-dog circuits must verify correct functioning before its outputs are reset.

The watchdog is tripped if a failure to transmit analogue-control updates to the analogue circuitry occurs. The updates are of two types:

Transfer of "Output value" data via the Analogue Interface comparators,

Transfer of analogue switching data via the SSDA every 40 mS.

The CPU generates pulses at 8 mS intervals to verify that the correct output value has been latched into the Analogue Interface comparators. These pulses are allowed to pass into guard only if the SSDA verifies that the analogue switching data is being transferred normally at 40 mS intervals. Once in guard, the pulses prevent the watchdog flip-flops from generating their four BARK and BARK DELAYED output signals; by re-triggering a monostable (M10-4 : 18 mS).

If two or more pulses are missing, M10 releases the hold, and the watchdog flip flops "Bark", activating the safety circuitry. They will be missing if the output value comparators are incorrectly updated, or if the SSDA fails to generate "Transmit" IRQ pulses for a period exceeding 220 mS, or if the CPU crashes.

The in-guard watchdog circuits are located on the Reference Divider pcb; the out-guard control signals originate in the Digital pcb and are processed in the Analogue Interface pcb.

4.5.6.1 Out-guard Watchdog (Circuit Diagram No. 430443 and 430444)

Each time the CPU verifies that an exchange of data performed via the serial link is valid, the CPU instructs the SSDA to generate a watchdog enable trigger. This pulse termed $\overline{\text{W.DOG ENBL SET}}$, is used to trigger monstable M29-11 (circuit drawing No. 430443 Sheets 1 and 3). The relaxation period of this monostable is 220 mS but is extended by re-triggering to give a logic-0 $\overline{\text{W. DOG ENABLE}}$ output at M29-9. Absence of $\overline{\text{W. DOG ENBL SET}}$ triggers for a period exceeding 220 mS will allow M29-9 to return to logic-1 level. The $\overline{\text{W.DOG ENABLE}}$ level is inverted at M43-3 and applied to NAND M46-12.

During each processor cycle, the CPU decoded address at M51-9 (circuit drawing No. 430442 sheet 2) is gated with WRT STRB to give, at M49-11, the active-low output. W. DOG. The latter is fed via the mother pcb to the analogue interface, to be gated at NAND M46 with W. DOG ENABLE. The resulting output at M46-13, W. DOG, comprises positive-going pulses at 8 mS intervals when the CPU/SSDA system is working normally, or a logic-1 level if the SSDA has failed. The signal W. DOG is fed, via the mother pcb, to the in-guard circuits on the reference pcb.

4.5.6.2 In-guard Watchdog (Circuit Diagram No. 430444 sheet 5)

NOTE. The operating levels of the in-guard CMOS circuits are negatively displaced as follows (nominal voltages):

Opto-coupler output circuits

logic-1: −10V dc
logic-0: −15V dc

Digital CMOS circuits

logic-1 : 0V
logic-0 : −15V

Interfacing between levels is performed by level-shifter M36.

The signal, W.DOG, is opto-coupled into guard via M9. During normal operation these positive-going 8 mS pulses trigger, and successively re-trigger the monstable M10-4 to give a continuing logic-0 at M10-7. The 18 mS relaxation time of the monostable allows for the absence of one pulse, but the absence of two or more pulses allows the monostable to reset, taking M10-7 to logic-1.

The logic level from M10-7 is applied to the set input of flip-flop M13-6. With reset M13-4 at logic-0 during normal operation, the output conditions of M13-1 and M13-2 are as follows:

(1) Set input M13-6 = logic-0 (no fault);
M13-1 (Q) = logic-0 – BARK not active
M13-2 ($\overline{\text{Q}}$) = logic-1 – $\overline{\text{BARK}}$ not active

(2) Set input M13-6 = logic-1 (malfunction);
M13-1 (Q) = logic-1 – BARK active
M13-2 ($\overline{\text{Q}}$) = logic-0 – $\overline{\text{BARK}}$ active.

The action of M13-2 changing to logic-0 triggers monstable M10-11, which has a relaxation time of 47 mS. After 47 mS, M10-9 output clocks flip-flop M13-11 to give the command BARK DEL from M13-13 and $\overline{\text{BARK DEL}}$ from inverter M14-12.

4.5.6.3 Power-on Reset (Circuit Diagram No. 430444 Sheet 5)

When power is first applied, the flip-flop latch circuit of M37 is forced to give a logic-0 output at M37-2 by R122/C7 holding the Reset inputs at logic-1 for approximately 80 mS, the Set input being at logic-0. M37-1 holds M10 inactive at M10-3, thus preventing random triggering at M10-4 from erratic W.DOG inputs whilst the SSDA/CPU function starts up. M37-2 imposes logic-1 at the Set input M13-8 of flip-flop M13. The Reset inputs M13-4 and M13-10 are held at logic-1 for a period of 470 mS from power-on by the action of the signal $\overline{\text{FP RST}}$ from the digital pcb. Therefore, the Set/Reset inputs M13-8/M13-10, initially both at logic-1, force M13-13 output to logic-1 to give active BARK DELAYED and $\overline{\text{BARK DELAYED}}$ outputs.

The Set/Reset inputs M13-6 and M13-4, also initially both at logic-1, force: M13-1 to logic-1 to give an active BARK output which inhibits the 16 kHz drive at M24-3; and M13-2 to logic-1 which makes the $\overline{\text{BARK}}$ output inactive.

The output conditions of M37 (M37-1 = logic-0, M37-2 = logic-1) remain unchanged after the 80mS time constant at M37 Reset inputs, but then M37-11 is free to be triggered from the SSDA strobe input. Two strobe inputs must occur before M37-1 clocks to logic-1 and M37-2 to logic-0. M13-13 now changes to logic-0, making BARK DELAYED and $\overline{\text{BARK DELAYED}}$ inactive, and the inhibit is removed from M10-3.

The outputs M13-1 and M13-2 remain unchanged until M10-7 falls to logic-0 by the clocking action of pulses on the W. DOG input. This must occur before M13-4 returns to logic-0 (at 470 mS from power-on) for BARK to be made inactive, otherwise BARK remains active and $\overline{\text{BARK}}$ is set to logic-0, giving a fail status bit to the CPU.

4.5.6.4 Safety Reset

Detection of a failure by the watchdog circuits results in permanent activation of BARK, $\overline{\text{BARK}}$, BARK DELAYED and $\overline{\text{BARK DELAYED}}$. The watchdog can be reset, if the malfunction has cleared, by the operation of the Safety Reset control on the front panel. The safety reset input to the watchdog circuit, $\overline{\text{FP RST}}$, is active for 100 mS from Safety Reset. (M53-9 on Digital Assembly – Circuit Diagram 430442 Sheet 2) During this period, the Reset inputs to M13-4 and M13-10 are held at logic-1 thus allowing correct pulse inputs from the processor and SSDA to hold M13-6 at logic-0, and to reset M13-13 to logic-0. The watchdog will not reset if the malfunction persists.

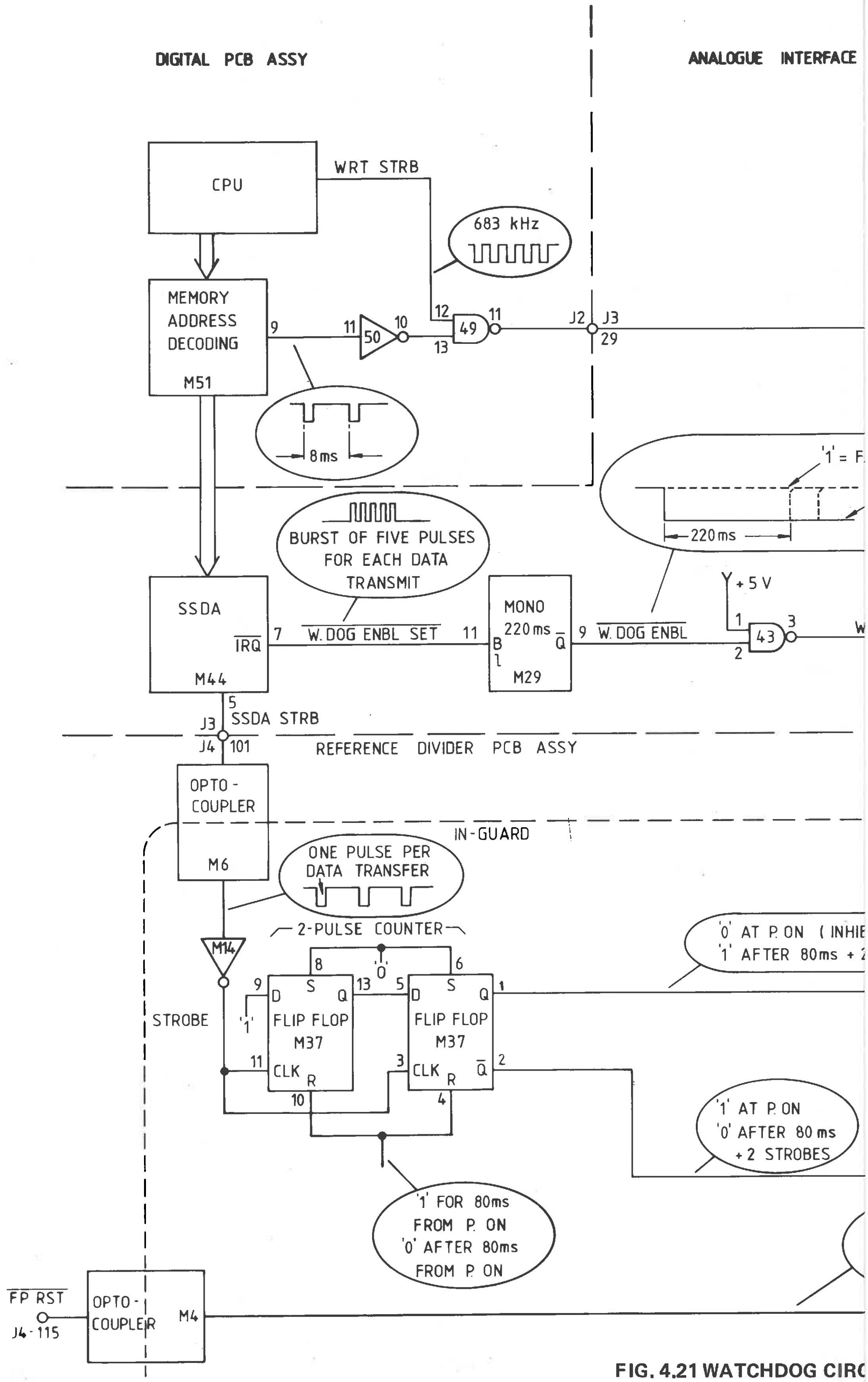
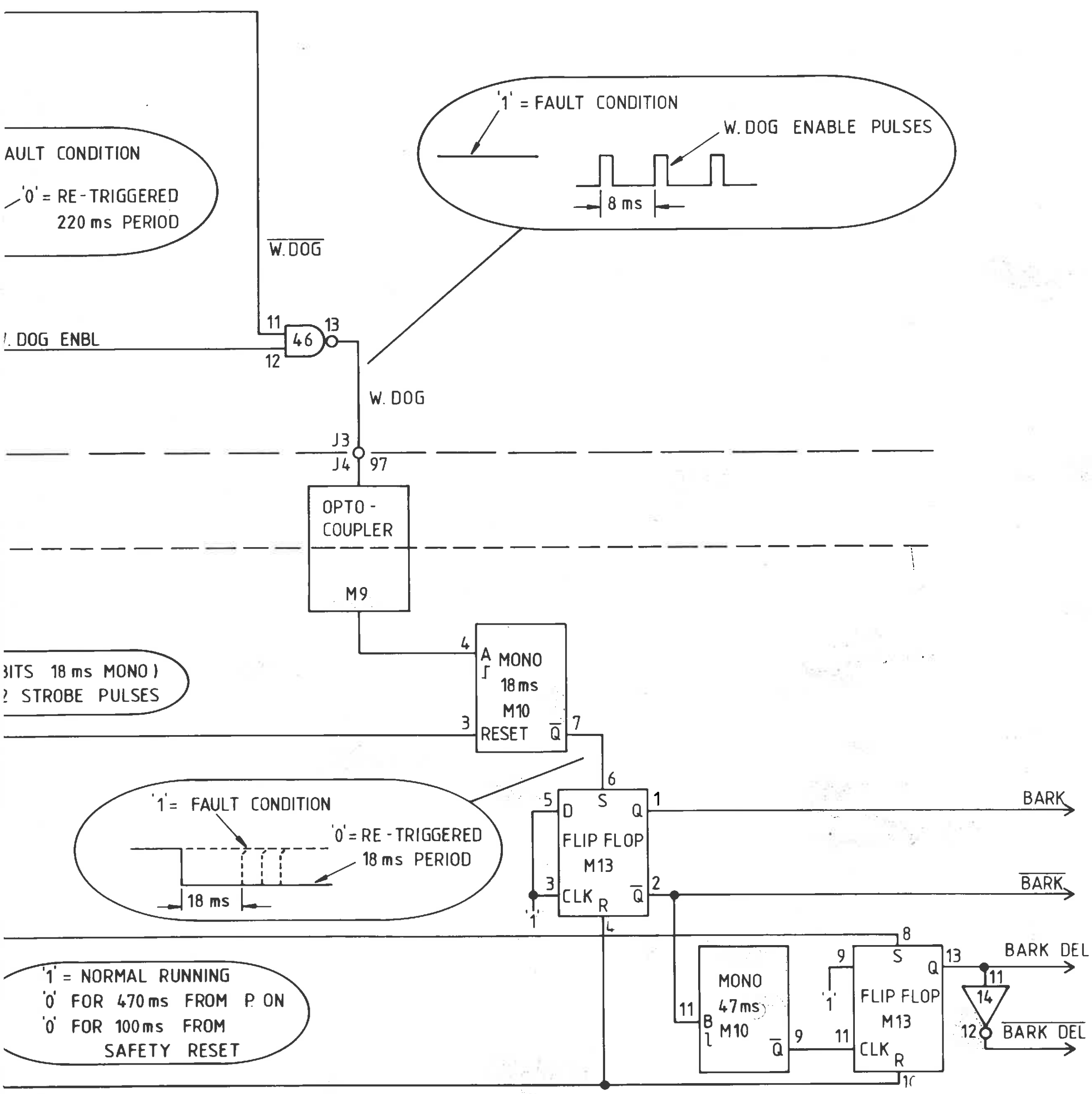


FIG. 4.21 WATCHDOG CIRC

PCB ASSY



:UITRY — SIMPLIFIED BLOCK DIAGRAM

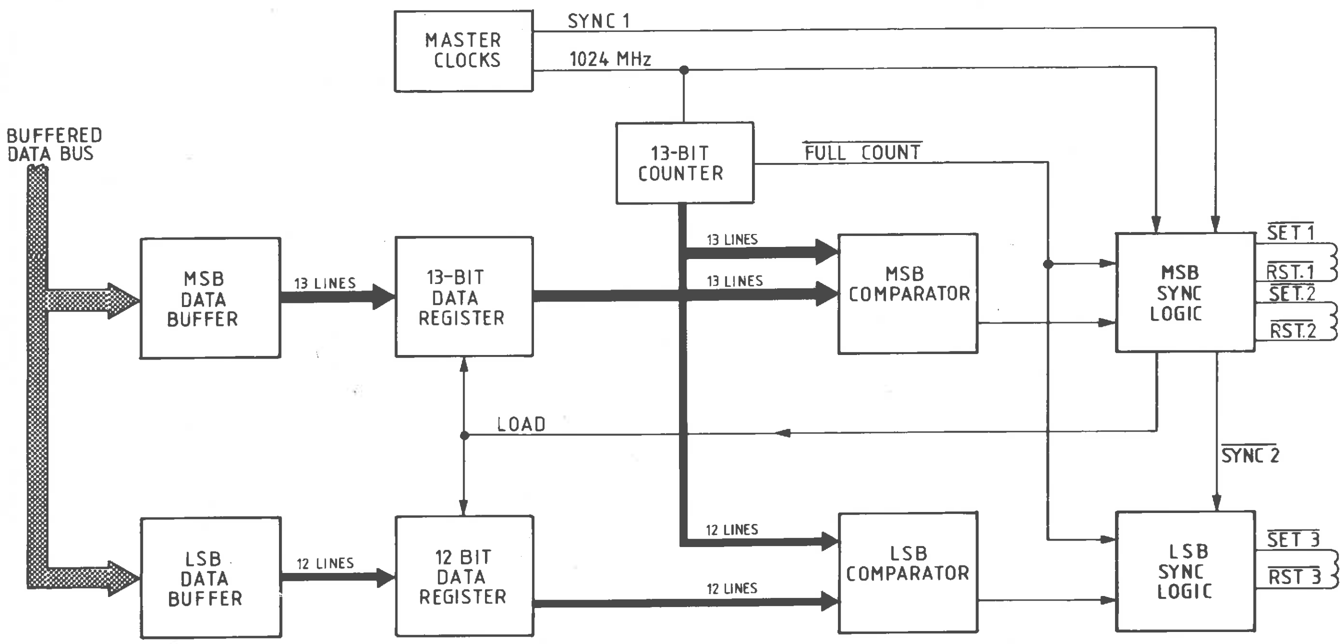


FIG. 4.22 PRECISION DIVIDER OUT-GUARD CIRCUITRY — SIMPLIFIED BLOCK DIAGRAM

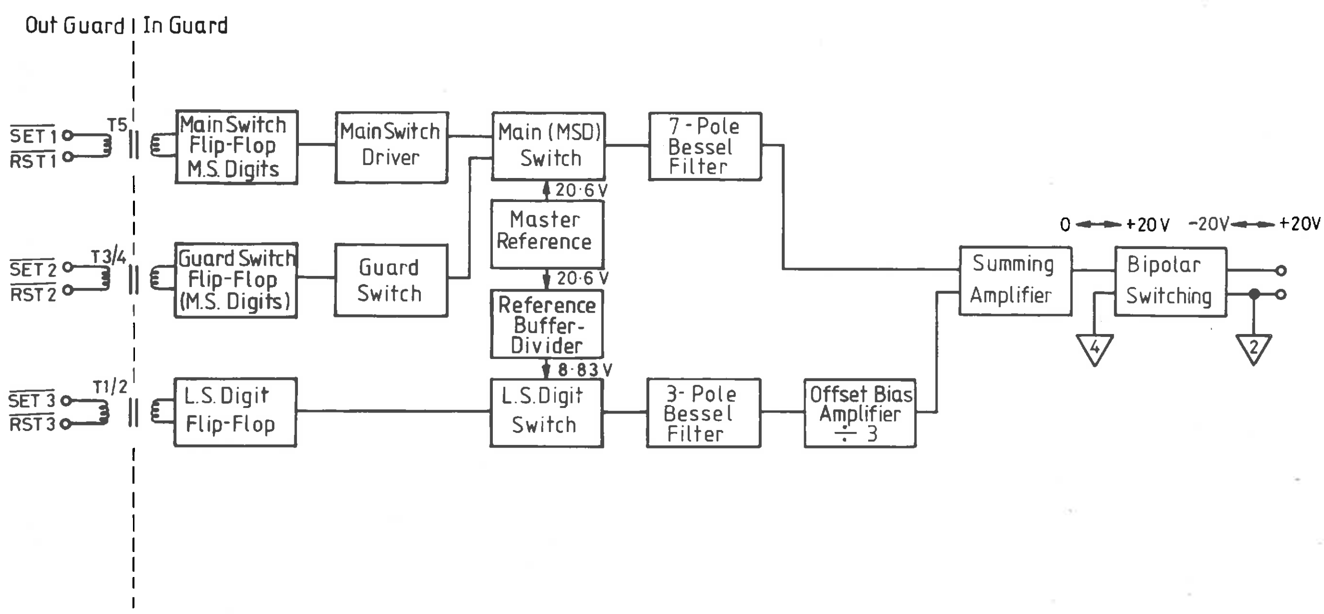


FIG. 4.23 PRECISION DIVIDER IN-GUARD CIRCUITRY — SIMPLIFIED BLOCK DIAGRAM

4.6 PRECISION DIVIDER

The out-guard circuitry described in this section performs the following functions:

(1) Receives the demanded output value from the CPU in the form of a 25-bit data word.

(2) Generates a continuous 13-bit count from the 1.024 MHz Master clock (cycling frequency 125 Hz)

(3) Compares the 13-bit count with the 13 most-significant bits of the 25-bit word, generating "Set" and "Reset" pulses, which are transferred into guard to trigger the Reference Divider Main and Guard JFET switches

(4) Compares the 12 most-significant bits of the count with the 12 least-significant bits of the 25-bit word, generating "Set" and "Reset" pulses, which are transferred into guard to trigger the Reference Divider "Least-Significant" JFET switch.

The out-guard circuitry is located on the Analogue Interface PCB Assembly.

The in-guard circuitry performs the following functions:

(5) Generates a Master Reference Voltage (20.6V) which is chopped by the Main and Guard JFET switches; to provide a square-wave whose Mark/Period ratio is controlled by the 13 most-significant bits of the 25-bit word. The square-wave is smoothed by a 7-pole Bessel filter to provide a D.C. voltage whose value varies directly as the Mark/Period ratio of the square-wave

(6) Generates a Buffered Reference Voltage (8.83V) which is chopped by the Least-Significant JFET switch; to provide a square-wave whose Mark/Period ratio is controlled by the 12 least-significant bits of the 25-bit word. The square-wave is smoothed by a 3-pole Bessel filter to provide a DC voltage whose value varies directly as the Mark/Period ratio of the square-wave.

(7) Sums the two DC voltages produced by the 7-pole and 3-pole filters, to generate a "Working Reference Voltage" between 0V and +20V; whose value is accurately proportional to the value demanded by the CPU's 25-bit word

(8) Switches the polarity of the Working Reference Voltage to output a reference voltage between -20V and +20V DC. This is used as reference on "DC" and "I" Functions of the instrument.

The in-guard circuitry is located on the Reference Divider PCB Assembly.

4.6.1 Precision Divider Comparators (Circuit Diagram No. 430443)

4.6.1.1 General

The precision divider comparators translate information from the central processing unit into time-related pulses which control the mark/period switching of the reference divider. Two comparators are used; one to translate the 13 most-significant bits of MPU data; the other, the 12 least-significant bits. The comparators perform concurrently, cycling continuously at 125Hz, taking 8mS per full count. During the initial stages of each counting period, the comparators generate SET pulses to start the reference divider mark period. After precisely-measured delay times, reset pulses are generated to terminate the mark period.

4.6.1.2 Comparator Function (Fig. 4.22)

Binary data is entered into the MSB and LSB buffered data latches under the control of the CPU. The contents of the buffered data registers are up-dated to the working data latches at the end of each comparator counting cycle by the LOAD command. This is derived from the 13-bit counter FULL COUNT output, which is also used by the MSB and LSB sync logic circuits to initiate generation of the set pulses SET 1, SET 2 and SET 3.

Translation of the binary data into reset pulses (whose time relationship to the set pulses is established by the demanded output value) is obtained in the MSB and LSB comparators.

4.6.1.3 13-Bit (MSB) Comparator (Circuit Diagram No. 430443 Sheet 2)

The 13 Exclusive-OR elements of the MSB Comparator are scanned in ascending sequence by the outputs of the 13-bit counter. The least-significant bit has a frequency of 512 kHz, and the most-significant a frequency of 125 Hz thus giving a natural division of 8192 time slots of 977 nS over the counting period of 8mS. Each time slot has a unique binary code; when this coincides with the bit-pattern set in the data register, the comparator provides an output pulse to the MSB sync logic. The latter initiates generation of reset pulses RST 1 and RST 2 and synchronizes them to SYNC 1 (2.048 MHz).

4.6.1.4 12-Bit (LSB) Comparator (Circuit Diagram 430443 Sheet 1)

This functions in the same manner as the MSB comparator but with 12 bits over the same 8mS counting period. This accommodates 4096 time slots and gives a 1954 nS period for each binary increment. Synchronizing of the RST3 output from the LSB sync logic is performed by SYNC 2 pulses which are half the rate of the SYNC 1 pulses.

4.6.2 Comparator Circuit Action

4.6.2.1 Input Data Latches (Circuit Diagram No. 430443 Sheets 1 and 2)

The input buffered data latches M31 to M34 and M37 to M39 receive 27 data bits in four bytes from the buffered data bus. Latches are selected by signals $\overline{\text{REF DIV 1, 2, 3}}$ or $\overline{4}$ from the memory address decoding on the digital pcb. Data is clocked to the "Q" outputs of the latches on the positive-going edge of $\overline{\text{WRT STRB}}$.

Data from the input latches is used as follows:

25 bits form a data word to the comparator registers M47, M48, M49 (part), M51 and M52. One bit triggers monostable M29 (part), the Q output of which is inverted and buffered to provide the control $\overline{\text{UPD (OG)}}$ used in the relay drive logic for analogue switching. One bit, EXT FREQ ÷ 10, is not used in the 4000.

4.6.2.2 13-Bit Counter (Circuit Diagram No. 430443 Sheet 2) (refer to Fig. 4.24 for Waveforms)

The counter comprises three 4-bit binary counters M15, M16, M17 and J-K flip flop M42 (half dual package). The outputs required from the counter are 13 binary-coded lines, the first (least significant) being a 512 kHz squarewave, the others successively divided in frequency to the most significant output of 125 Hz.

Bit 1 is provided by J-K flip flop M42, which toggles on each falling edge of the 1.024 MHz clock to give 512 kHz Q and $\overline{Q}$ outputs. These outputs are used as follows:

(1) Q and $\overline{Q}$ complementary outputs together provide the least-significant input to the 13-bit comparator;

(2) The Q output controls the counting rate of M15, synchronizes M16 and M17, and is used in the gating of $\overline{\text{FULL COUNT}}$.

Counters M15, M16 and M17 are cascaded as a 12-bit counter and synchronously clocked by the 1.024 MHz. M15 counting is enabled only when M42 Q output is logic-1 at the count-enable input M15-7. As M42 output is at 512 kHz, clocking of M15 occurs on the rising edge of alternate 1.024 MHz clocks, thus giving outputs of 256, 128, 64 and 32 kHz squarewaves from M15. Counter M16 is enabled by the carry output from M15 together with 512 kHz from M42 at the count-enable pins M16-10 and 7 respectively, thus giving outputs of 16, 8, 4 and 2 kHz squarewaves from M16. Counter M17 functions in a similar manner to give outputs of 1 kHz, 500, 250 and 125 Hz squarewaves.

The 2μS-long carry output from M17 occurs at the end of the 125 Hz output when all counter outputs are at logic-1. The carry output is NAND gated with M42 Q output to give the 1μS-long logic command $\overline{\text{FULL COUNT}}$. The counting cycle continues, starting from bit 1.

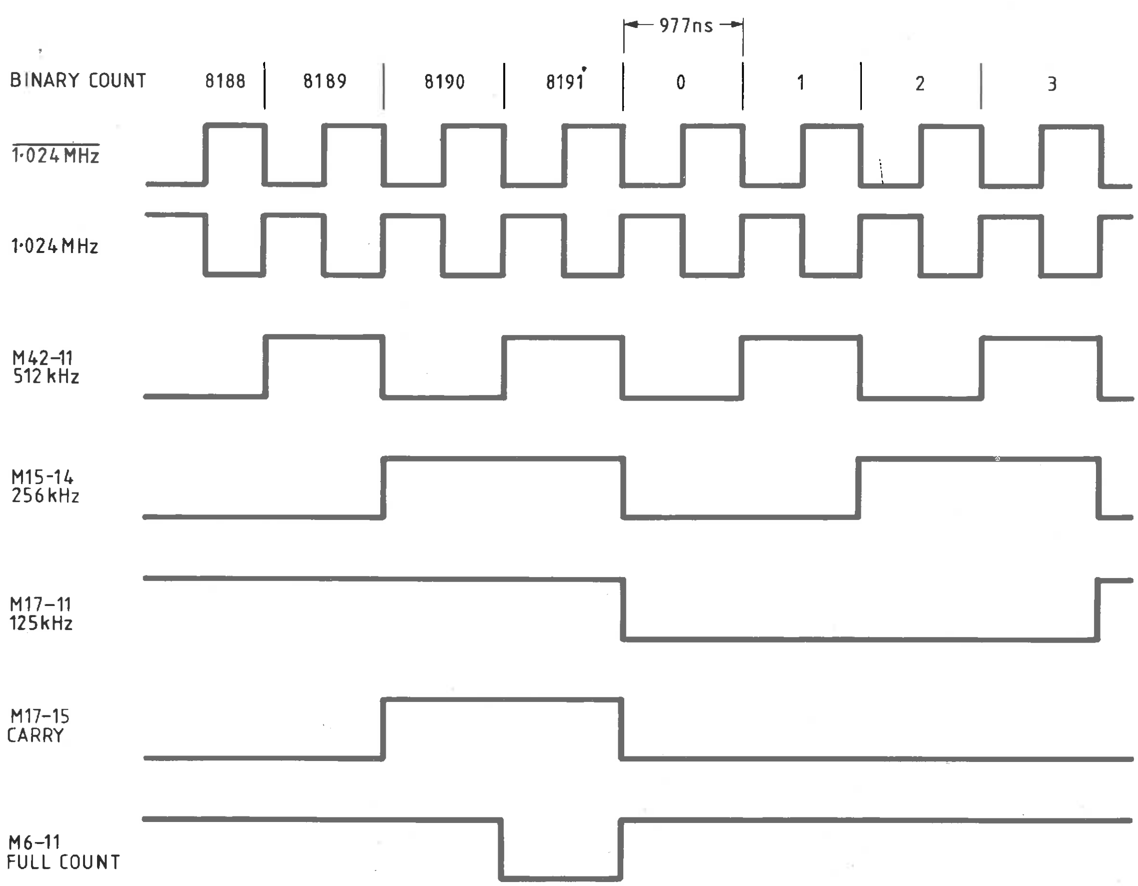


FIG. 4.24 13-BIT COUNTER WAVEFORMS

4.6.2.3 13-Bit Comparator Action (Circuit Diagram No. 430443 Sheet 2)

The 13-bit comparator provides a logic-1 output at TP12 whenever a coincidence occurs between the following two sets of data:

(1) Data set in registers M47, M48 and M49-1;

(2) Data from the 13-bit counter M42, M15, M16 and M17.

Twelve exclusive-OR elements M25, M26, M27 and three NOR gates of M12 are used to detect a coincidence. The data in the registers is preset by the CPU, while that presented by the 13-bit counter cycles through every binary combination possible on 13 lines. Two coincident inputs to an exclusive-OR gate provide a logic-0 to the 12-input NOR gates M24/M23; full coincidence in bits 2 to 13 is shown by a logic-0 at NAND M13-6. Coincidence at bit 1 is shown by logic-0 at M12-13 and M12-4 as follows:

M12 INPUT PINS			M12 OUTPUT PINS	
6	11	9/12	4	13
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0

only 4 input combinations available

A BUSY signal is generated by the comparator at NAND M50-13 (TP2) when the 13-bit counter approaches full count. Bits 8 to 13 are at logic-1 for the period of 125µS preceding the end of the counter cycle (see Fig. 4.25). The BUSY level is applied to the D input at M49-9 and is clocked through as REF BUSY to buffer M45.2 by 1.024 MHz. When the CPU has data to load into the input data latches, it first interrogates the comparator by enabling buffers M45 through REV DIV RD. A logic-1 on REF BUSY at M45-3 indicates to the CPU that sufficient time is available for the latch-loading process to take place (at least 125µS before LOAD pulse). The remaining elements of M45 buffer the five most significant data bits back to the CPU so that data parity can be confirmed.

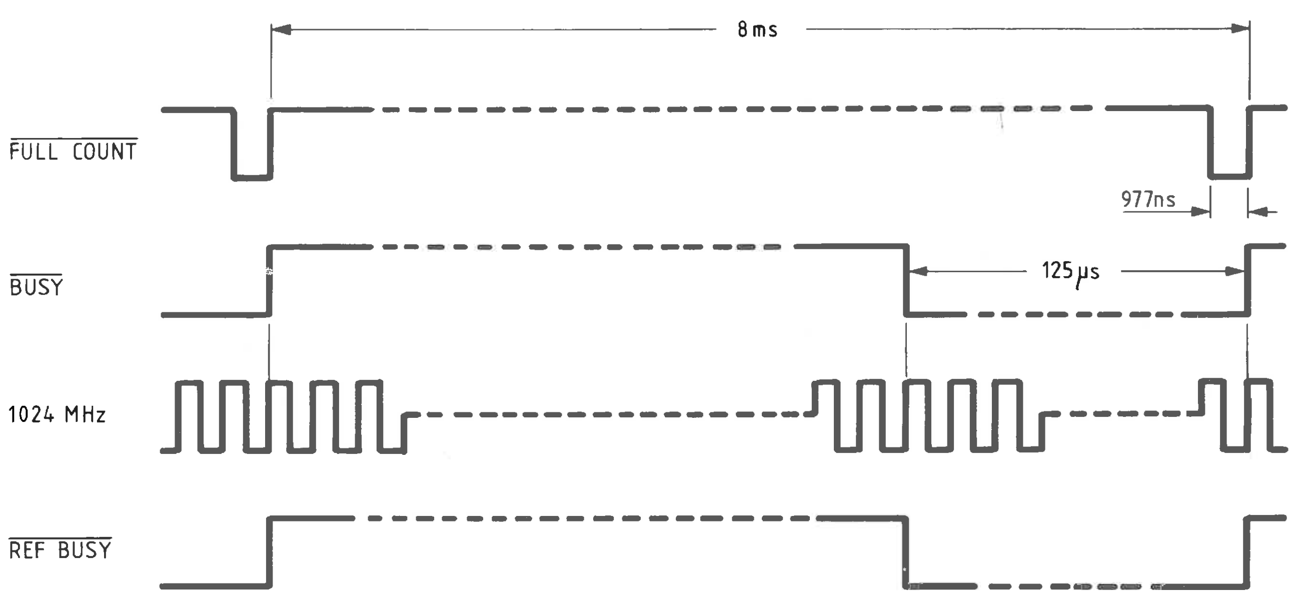


FIG. 4.25 BUSY WAVEFORMS

4.6.2.4 MSB Sync Logic (Circuit Diagram No. 430443 Sheet 2) (refer to Fig. 4.26 for waveforms)

This circuit, M14, M6, M7 and M8, provides the following signals: $\overline{\text{SYNC 2}}$, LOAD, $\overline{\text{SET 1}}$, $\overline{\text{SET 2}}$, $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$.

$\overline{\text{SYNC 2}}$ is obtained by NAND gating $\overline{\text{1.024 MHz}}$ and SYNC 1 to give a synchronizing pulse at half the rate of SYNC 1. (See Fig. 4.26)

The LOAD pulse, which enables the 13-bit counter registers, is generated at M14-6 towards the end of the counter's full-count output. $\overline{\text{FULL COUNT}}$ sets the D input M14-2 and the level is clocked, inverted, from M14-6 by the next two $\overline{\text{SYNC 2}}$ pulses that occur.

The inverse of LOAD is used to time the pulse $\overline{\text{SET 1}}$ by NOR gating at M7-4 with $\overline{\text{1.024 MHz}}$. The pulse at M7-4 is then NAND gated with SYNC 1 to provide $\overline{\text{SET 1}}$ from M8-1. The pulse $\overline{\text{SET 2}}$, which occurs 977 nS before $\overline{\text{SET 1}}$, is obtained by gating $\overline{\text{FULL COUNT}}$ with 1.024 MHz at NOR M7-10 and then NAND gating at M8-10 with SYNC 1.

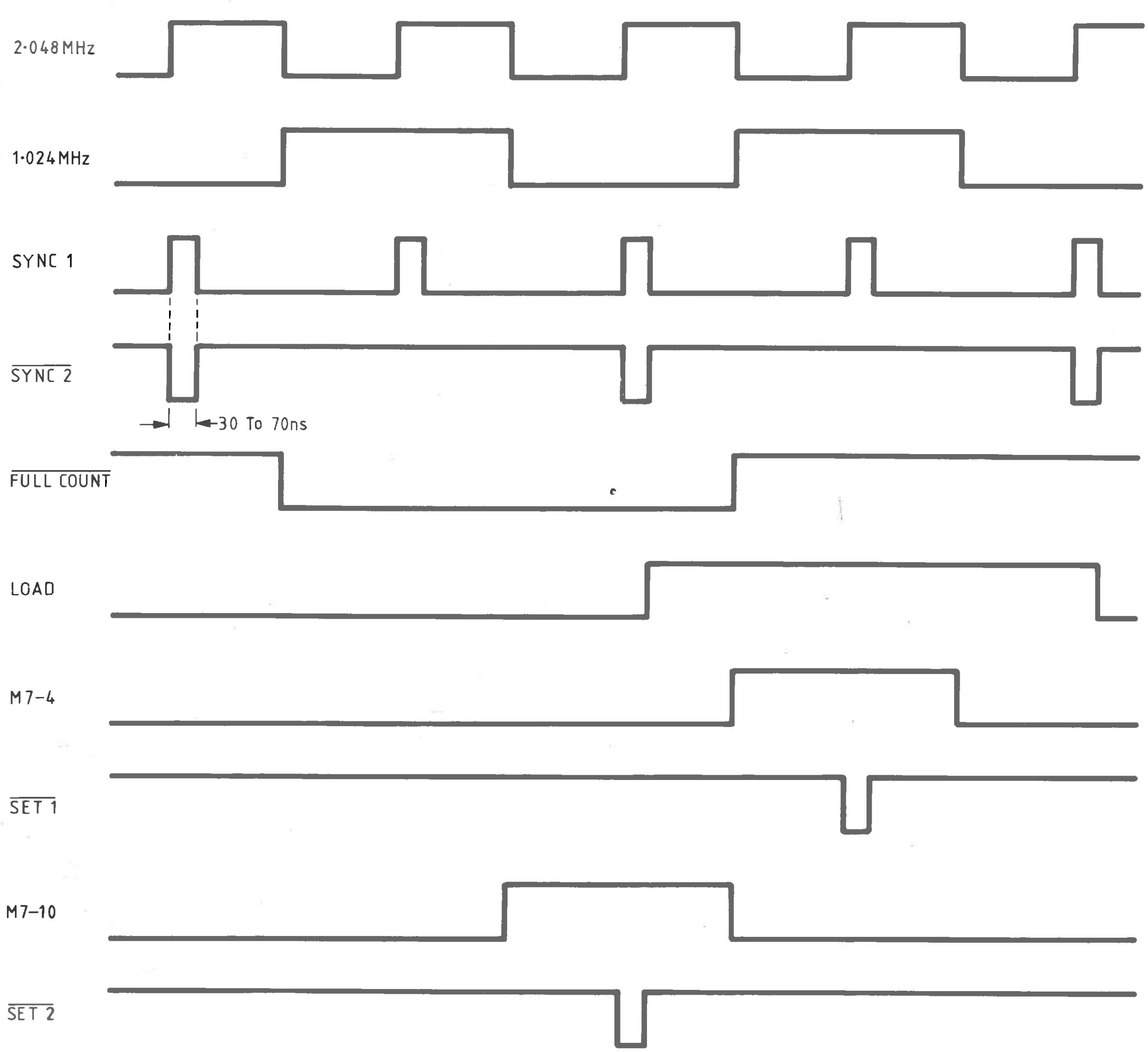


FIG. 4.26 MSB SYNC LOGIC WAVEFORMS

Reset pulse generation (see Fig. 4.27) is indicated by a logic-1 level at TP12. This can occur at any one of the 8192 binary counts of the 13-bit counter, the actual time slot in which it appears depends on the binary count at which the coincidence occurs.

The coincidence level at TP12 is NAND gated at M6-8; M6-10 being at logic-1 for all binary counts except 8191. The logic-0 at M6-8 is NOR-gated at M7-1 with 1.024 MHz, this is then used to select the next SYNC 1 pulse via NAND M8-4 to provide the pulse RST 1.

The coincidence level at TP12 is used to set the D input at flip flop M14-12. This level is clocked to NAND M6-5 by the next SYNC 2 pulse. NAND input M6-4 is at logic-1 except when LOAD is active, thus M14-9 output is inserted at M6-6 to be NOR-gated with 1.024 MHz at M7-13. This is then used to select the next SYNC 1 pulse via NAND M8-10 to provide the pulse RST 2.

The pulse-timing example given in Fig. 4.27 shows the generation of RST 1 and RST 2 when coincidence occurs in the comparator at binary count = 0 (waveforms in unbroken lines). Coincidence occuring at binary count 1 causes RST 1 and RST 2 to increment in time by 977 nS with respect to the SET 1 and SET 2 pulses (waveforms in broken lines). RST 1 and RST 2 will be generated with the same relationship in time to the comparator coincidence when the latter occurs in any binary count time slot from 0 to 8190 (inclusive); note that SET 1 and SET 2 remain staionary with respect to FULL COUNT and LOAD and that RST 1 and RST 2 increment, in time, away from these.

RST1 and RST 2 are inhibited when coincidence occurs at binary count 8191 to allow for the re-loading of the input registers at the end of the counter cycle. The inhibit is performed by the FULL COUNT level going to logic-0 at NAND M6-10 which prevents RST 1 being generated, and by flip flop M14-5 output going to logic-0 for the period of the load pulse which inhibits RST 2.

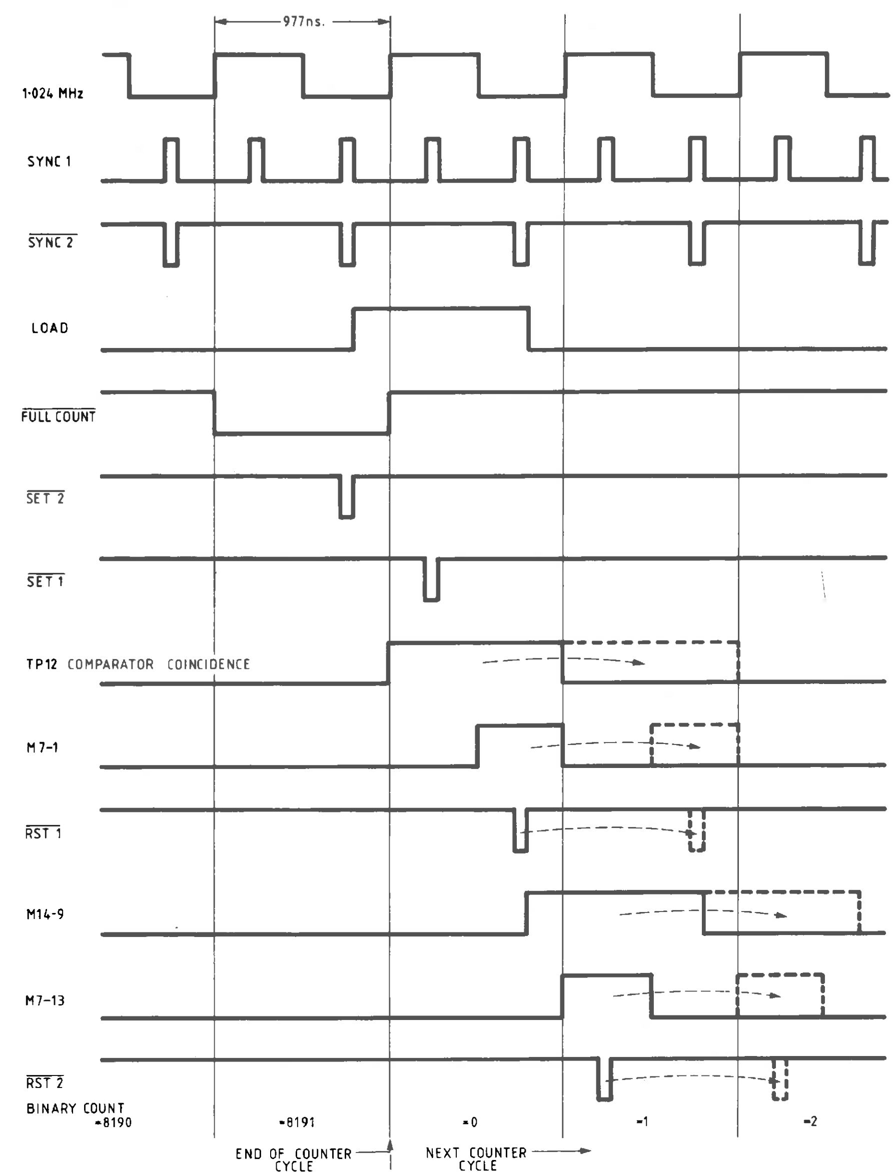


FIG. 4.27 MSB SET/RESET PULSE GENERATION

4.6.2.5 12-Bit Comparator Action (Circuit Diagram No. 430443 Sheet 1)

This functions in an identical manner to the 13-bit comparator previously described. Twelve exclusive OR gates, M19, M20 and M21, receive 12-bit binary output from the common counter and compare these bits with the data in the data registers. The least significant bit changes at a rate of 256 kHz, and the most significant bit at 125 Hz. Coincidence occurring in any of the 4096 binary count time slots available in the comparator cycle is shown as a logic-0 at TP5 for a period of 1954 nS.

4.6.2.6 LSB Sync Logic (Circuit Diagram 430443 Sheet 1) (refer to Fig. 4.28 for waveforms)

The timing of $\overline{\text{SET 3}}$ is controlled by the $\overline{\text{FULL COUNT}}$ pulse from the 13-bit counter. The inverted $\overline{\text{FULL COUNT}}$ at M43-6 is gated with the inverted $\overline{\text{SYNC 2}}$ from M43-11 to give, at M46-1, $\overline{\text{SET 3}}$. The comparator coincidence logic level is inverted to logic-0 at M12-1; M12-2 being at logic-0 except when $\overline{\text{FULL COUNT}}$ is low. The waveform at M12-1 is of 1954nS duration and therefore allows two consecutive $\overline{\text{SYNC 2}}$ pulses to be gated to M46-4 ($\overline{\text{RST 3}}$). This condition exists for all $\overline{\text{RST 3}}$ timings except at the binary count of 4095; in this instance, the $\overline{\text{FULL COUNT}}$ pulse occurs after the gating of the first SYNC 2 pulse, sets M12-2 to logic-1 and so prevents the second pulse appearing at $\overline{\text{RST 3}}$. In practice, the second pulse of $\overline{\text{RST 3}}$ has no operational significance.

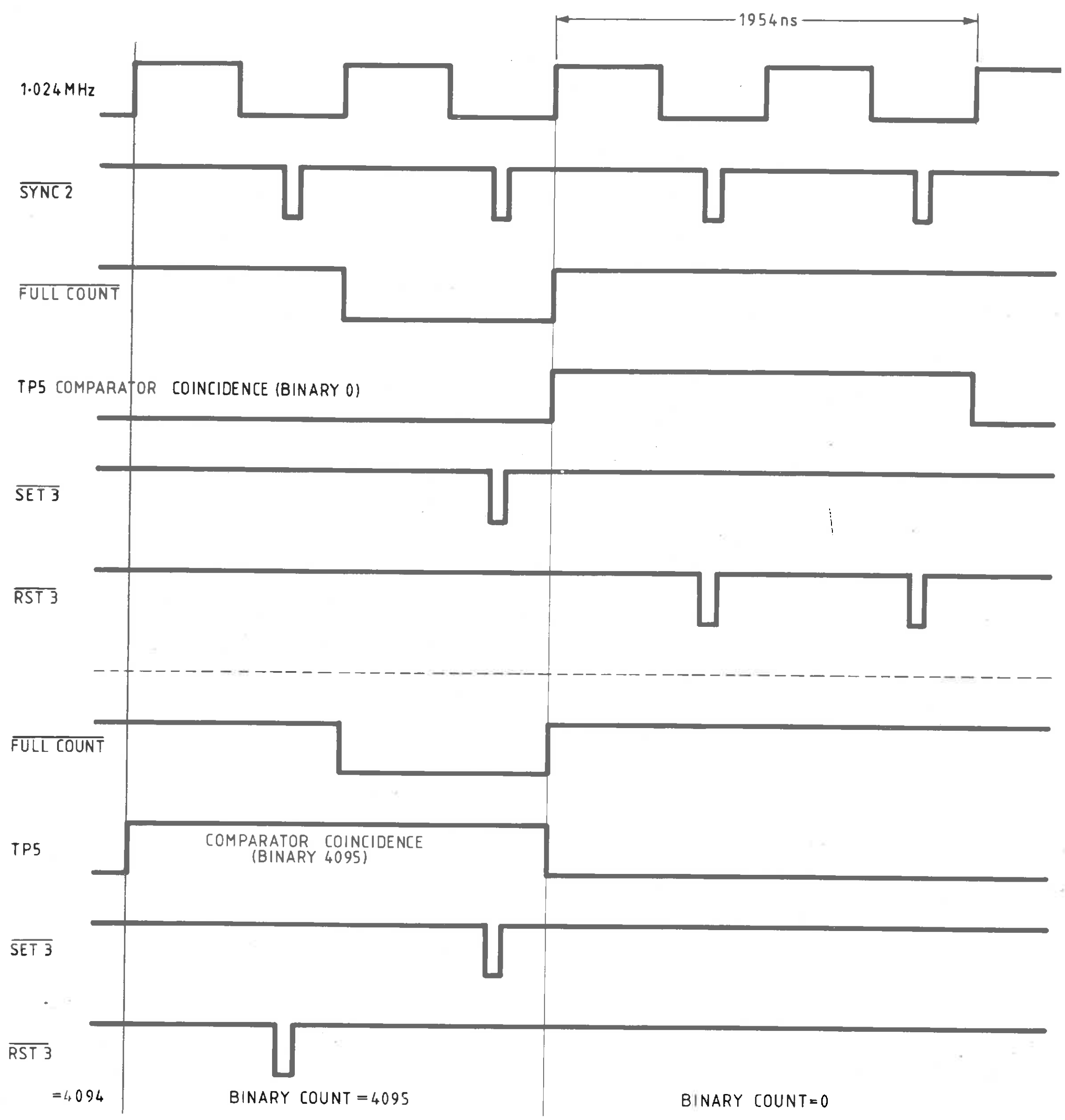


FIG. 4.28 LSB SET/RESET PULSE GENERATION

4.6.3 References and Reference Divider (Circuit Diagram No. 430444 and Fig. 4.23)

The set and reset pulses from the prevision divider comparators control the timing of FET-switches which chop Master Reference voltages. The chopped references are filtered to generate voltages whose level is proportional to the mark:period ratio (duty cycle). MSD and LSD voltages are added in the summation amplifier to generate a variable 0 ↔ 20V at high resolution (0.03ppm, ≏ 0.5μV increments).

Bipolar switching inverts the working reference for negative output selections.

4.6.4 Master Reference (Circuit Diagram No. 430452 and Fig. 4.29)

The Master Reference determines the fundamental long and short-term stability of the 4000. It is a separate pcb mounted on the Reference Divider assembly (Refer to Layout Drawings Nos. 400444 and 400452).

The basic circuit shown in Fig. 4.29 acts as a constant-current generator for a zener reference.

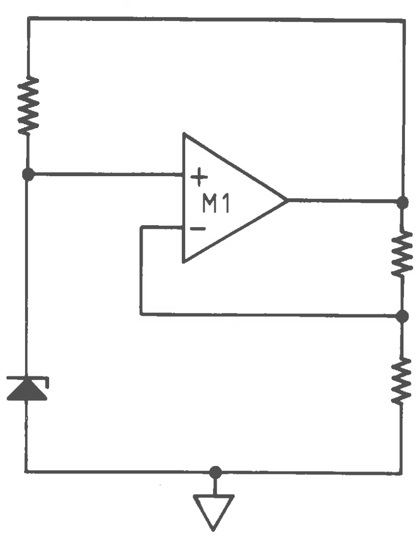


FIG. 4.29
BASIC REFERENCE CIRCUIT

The random character of zener drift in the short-to-medium term may in the long term be regarded as averaging to zero. The averaging action of the eight zener diodes in Drawing 430452 reduces the short and medium term variations (due to drift and noise) by a factor of √8, effectively 3 times more stable than a single zener diode.

The diodes and resistors are selected and matched for near-zero temperature coefficient; the overall instrument values are shown together with the stability and accuracy specifications in Section 6 of the User's Handbook.

Test links TLA1-6 and TLB1-5 are selectively removed during manufacture as a fine adjustment of zener operating current for zero temperature coefficient. The zener voltages of +24.5V at TP3 and TP1 wrt common-R1 are reduced by the star-point buffer M2 to approximately +20.6V at the Main Switch in the Reference Divider. This voltage is delivered to the Reference Divider by a full 4-wire sensed connection.

4.6.4.1 Buffer M2 – Temperature Compensation (Circuit Diagram 430452 Sheet 1)

In the 4000A instrument, the temperature compensation applied to M2 is adjusted at manufacture by R29 (set TC slope). This adjustment requires specialised test equipment and should not be attempted by users.

If a fault is suspected on the Reference PCB Assembly (400452), contact your Datron Service Centre.

4.6.5 Reference Buffer-Divider (Circuit Diagram No. 430444 Sheet 2)

R80/81 drop the 20.6V Master Reference voltage (V_{Ref}) to +8.83V. M23/Q40 is a voltage-follower providing +8.83V wrt common-4 at the star-point TP14 to supply the least-significant digit switch.

4.6.6 Least-Significant-Digits Switching (Fig. 4.30)

4.6.6.1 Switch Driver

$\overline{\text{SET 3}}$ and $\overline{\text{RST 3}}$ pulses from the LSD Comparator in the Analogue Interface Assembly are transferred into guard via pulse transformers T1 and T2, whose centre-tapped secondaries are balanced about 0V (T1) and +9V (T2). Q5-Q7 form a fast bistable using emitter-coupled logic, to switch TP1 between +9V (mark) and +20V (space). During the "Mark" time after $\overline{\text{SET 3}}$ pulse, Q29 and Q30 are switched ON, connecting LKA to +9V Ref. During the "Space" time after $\overline{\text{RST 3}}$ pulse, Q29 and Q30 disconnect LKA from +9V Ref. Q1 – Q4 have the same fast bistable action, Switching Q31 off during the "Mark" period by −11V at TP2, disconnecting LKA from common-4 (0V); and on during the "Space" period, connecting LKA to common-4 (0V). Fig. 4.30 demonstrates this action.

4.6.6.2 FET Switch and 3-pole Filter

The combined action of the switch FETs alternately provides charging current for the 3-pole filter (during "mark") and discharging current (during "space"). Two FETs in parallel (Q29 and Q30) are necessary to equalise the charging and discharging time constants by matching the "ON" resistances. This preserves linearity of the filter output voltage over the full range of mark/period ratios applied via the set and reset pulses.

The 3-pole filter has the advantage of not being in series with the DC output signal. The 125Hz ripple content is reduced to an acceptable level for the overall instrument specification. The filter output is buffered by voltage-follower M16.

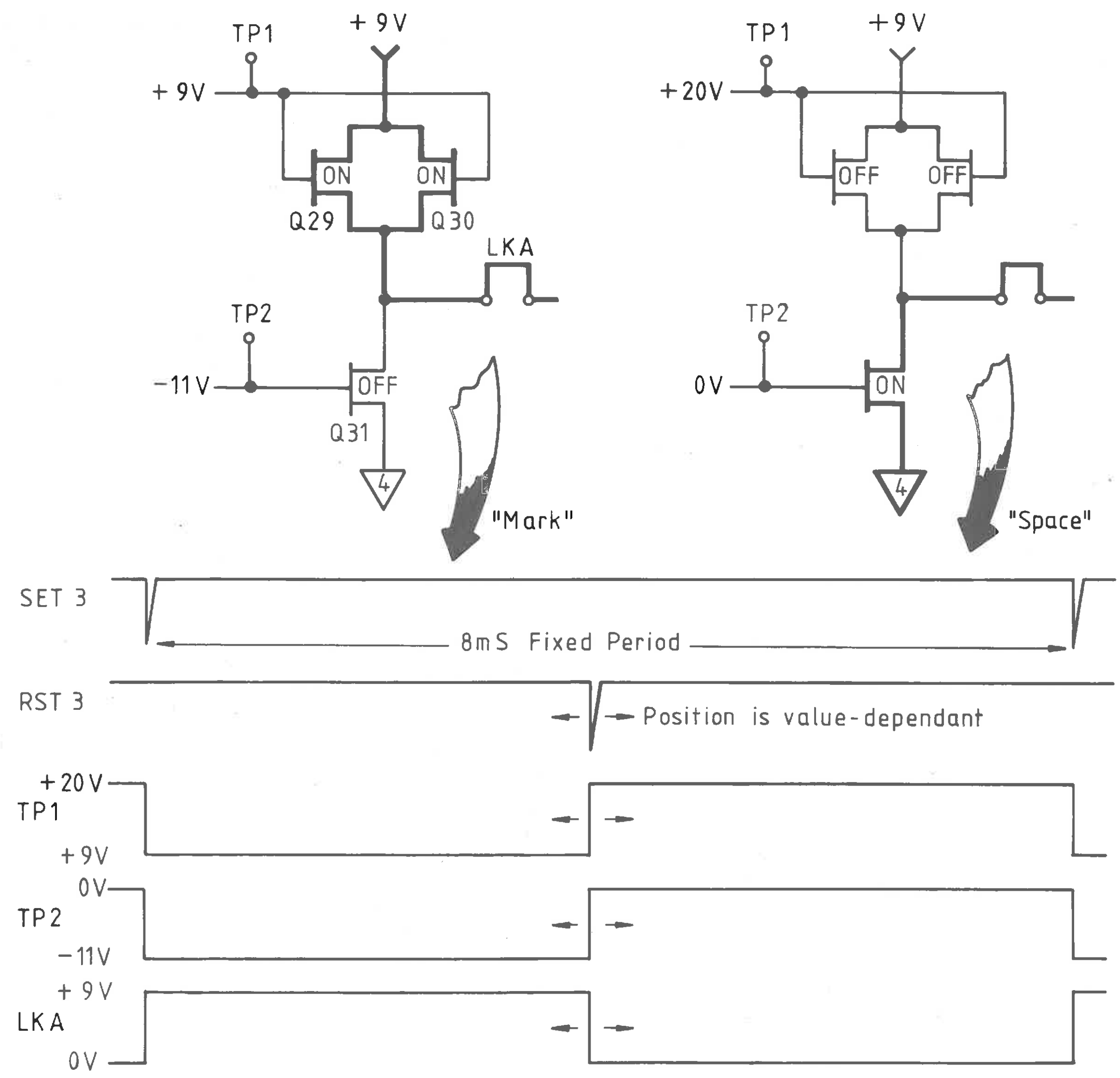


FIG. 4.30 ACTION OF LSD SWITCH

4.6.6.3 Offset Bias Amplifier

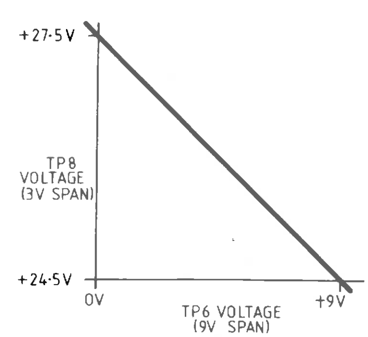
M20 performs a dual role:

(1) Its gain is set to $-\frac{1}{3}$ by R64/65

(2) Its output is level-shifted to provide an offset bias for the summing amplifier (This allows the summing amplifier output to have a negative zero offset).

Also a small thermal coefficient zero correction is factory-preset (D10/R85).

M20 transfer function is approximately as follows:



The actual values are as set digitally in software, affecting the mark:period ratio of the FET switches, using stored calibration constants.

4.6.7 Most-Significant-Digits Switching (Circuit Diagram No. 430444 Sheet 1)

The large reference voltage (20.6V) and the need for higher resolution makes the MSD Switching circuitry more complex than for LSD; but the principle is the same: the set and reset pulse-timing adjusts the mark:period ratio of the square wave fed to the filter.

The arrangement used for the MSD switching satisfies two essential requirements:

(1) The charge and discharge path resistances for the 7-pole filter must be closely matched.

(2) The leakage current of the path switched off must be minimal.

Requirement (1) demands that the matched devices used in both paths are of the same type (P-channel JFETs have approximately 10 times the "on" resistance of N-channel types). But without the voltage standoff and leakage-current shunt created by the guard switch, the pinch-off gate voltage for one of the paths would be high enough to generate gate-leakage current in excess of requirement (2).

4.6.8 Main and Guard Switches (Fig. 4.31 and Circuit Diagram No. 430444 Sheet 1)

Refer to Fig. 4.31, in which only the Space → Mark state-transfer a-b-c is shown. (The Mark → Space transfer is symmetrical c-b-a). The switch driver flip flops establish the voltage shown at TP3, 4 and 5 as controlled by the set and reset pulses. The drivers are ECL fast bi-stables, but note that Q19 and Q20 are included in the main switch driver as a level-shifter for Q32/Q35.

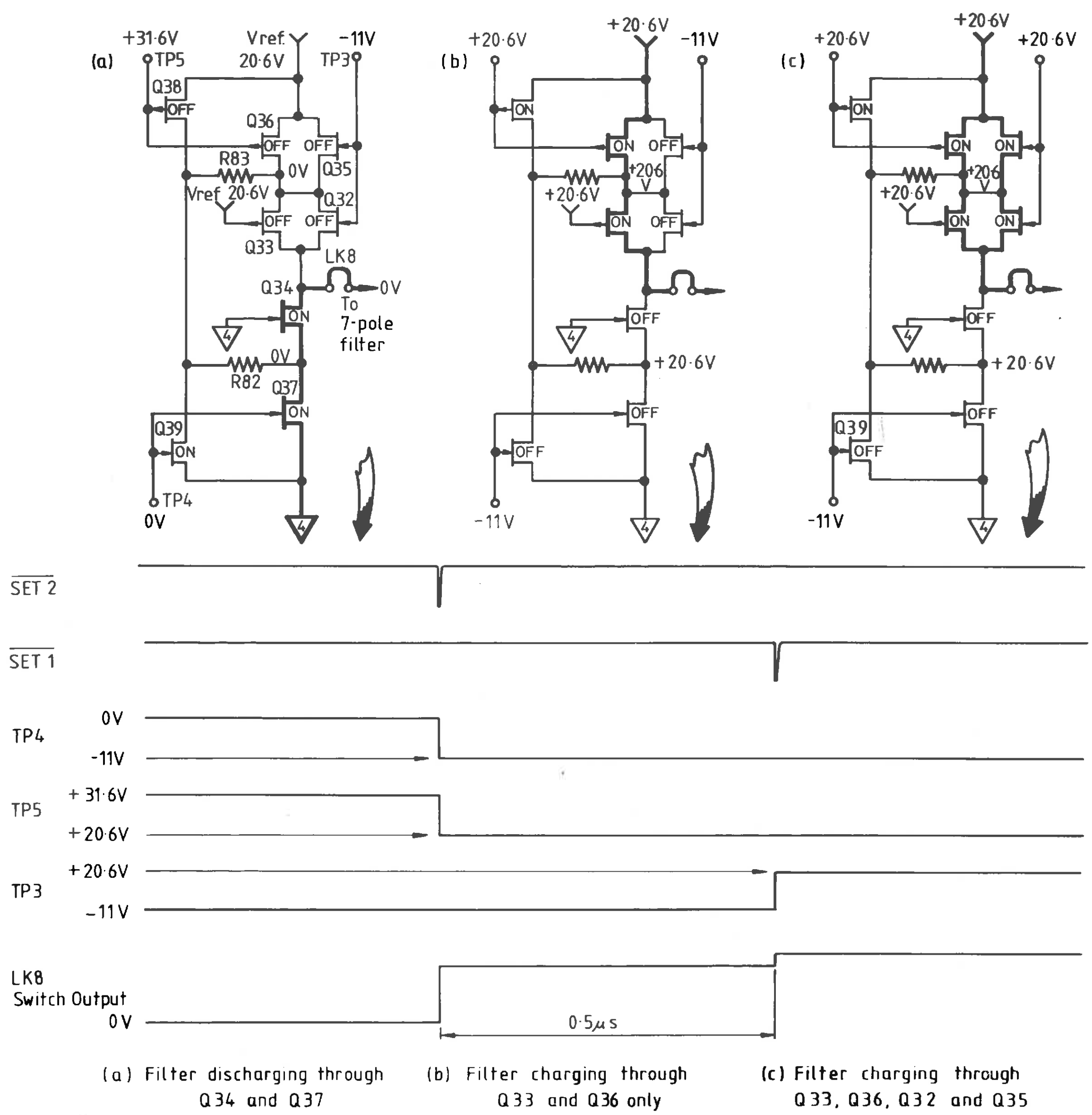


FIG. 4.31 ACTION OF MAIN AND GUARD SWITCHES (MSD)

4.6.8.1 Switch Timing

$\overline{SET\ 1}$ pulse is delayed by 0.5µSec after $\overline{SET\ 2}$ pulse, and $\overline{RST\ 2}$ is delayed by 0.5µSec after $\overline{RST\ 1}$.

$\overline{SET\ 2}$ and $\overline{RST\ 2}$ pulses control the timing of the guard switch Q38 and Q39, and Q36, Q33, Q34 and Q37 in the main switch (TP4 and 5).

$\overline{SET\ 1}$ and $\overline{RST\ 1}$ pulses turn Q35 and Q32 on and off (TP3). Because of the 0.5µSec delays, Q35 and Q32 conduct only during the time that Q36 and Q33 are also conducting.

4.6.8.2 Filter Discharge Path

In Fig. 4.31(a) the switches are in "space" state. Any leakage current due to the high voltage of Q36/Q35/Q38 gates is shunted via Q39/R83, eliminating Q33/Q32 leakage by zero source-drain voltage. During "space" state the 7-pole filter capacitors have a discharge time constant which includes Q34 and Q37 'On' resistance (3-5 ohms each).

4.6.8.3 Filter Charge Path

To preserve linearity over the full range of Mark: Period ratios, the filter charging path must also have the same time constant, so Q35 and Q32 form a matched set with Q34 and Q37, all N-channel J-FETs (The "on" resistance of P-channel FETs is much higher: 30 – 40 ohms). But to avoid high voltages being developed across Q35/Q32 when changing between states (causing excessive leakage), P-channel FETs Q36/Q33 are switched on before (and switched off after) Q35/Q32.

Fig. 4.31(b) shows this intermediate state after $\overline{SET\ 2}$ and before $\overline{SET\ 1}$, and Fig. 4.31(c) shows the fully-conducting state after $\overline{SET\ 1}$. Note that the second step on LK8 waveform is heavily exaggerated for descriptive purposes, and is not readily viewed on an oscilloscope. The longer charging time-constant during this half-microsecond is not sufficient to disturb the linearity of the filter in excess of specification.

To minimise leakage during "mark" state, Q34 source-drain voltage is maintained at zero by R82 connection. Thus Q34, Q33 and Q32 act as isolators in their "OFF" state, giving rise to the name "Guard Switch" for Q38/39.

4.6.9 7-pole Filter

M26, M28, M32, Q41 and Q42, together with associated capacitors and resistors, form a 7-pole Bessel Function filter in three active elements; providing approximately 135dB of attenuation at the 125Hz switching frequency and increasing at 140dB/decade. This allows sufficient bandwidth to avoid execessive settling time whilst reducing the output ripple to within instrument specification. Q41 and Q42 source-followers provide input bias currents for M26 and M28 from the 15V supplies, and buffer the line from bias-current effects.

The filter output at TP11 is fed to the summing amplifier to be added to the output from the Least-significant digits offset-bias amplifier. R101 and C51 prevent spikes from the chopper-stabilised summing amplifier being fed back into the filter.

4.6.10 Summing Amplifier (Circuit Diagram No. 430444 Sheet 3)

M33, M34 and Q44 sum together the MSD and LSD voltages. M35, D14, D15, Q48 and Q49 provide boot-strapped supplies to preserve full dynamic-range linearity. Q46 and Q47 establish 3mA constant-current drives for D14 and D15, over the range of BS-common voltage variation.

M33 is a high-gain, chopper stabilised integrator with a bandwidth of approx. 10Hz, and Q44 provides additional bandwidth for rejection of HF common-mode noise.

M34/Q45 provide the output and feedback drive, buffering the summed outputs of M33 and Q44. The summing amplifier acts as a voltage-follower to the MSD input, but divides and inverts the LSD input. The LSD gain ratio is set by R100 ÷ R99 = 475 ÷ 555,410 ≏ 8.552 x 10^{-4}. The span of LSD inputs of approximately 3V (+27.5V at zero LSD filter output to +24.5V at LSD filter output of +9V) leads to a span of approximately 2.5mV subtracted from the MSD voltage at the emitter of Q45.

The reference voltages and reference division circuitry are chosen to allow for software calibration adjustments, so the span of the summing amplifier overlaps the required Full Scale of 0 to 19.999999V at both extremes :

Zero:

At zero count the MSD input voltage is approx. 3.2mV. Zero count on the LSD comparator produces an output at TP6 of approx. 1.1mV, which translates into an output voltage to the summing Amplifier of approx. +27.5V. The combined output at Q45 emitter is found by

$$V_o = V_{msd} - (V_{lsd} - V_{msd}) \times \frac{R100}{R99}$$

$$= 0.0032V - (27.5V - 0.0032V) \times \frac{475}{555410} \triangleq \underline{-20.3mV}$$

This overlap of approx. −20.3mV allows a zero offset to be stored in the digital calibration memory to align the zero output to a defined external zero.

Full Scale:

A full count of 8191 on the MSD Comparator would produce a +20.6V input to the summing amplifier. Similarly a full count of 4095 on the LSD Comparator would produce +8.83V at TP6, and +24.5V at TP8 at the input to the summing amplifier. The combined output is again found by $V_o = V_{msd} - (V_{lso} - V_{msd}) \times \frac{R100}{R99}$

The maximum value is

$$20.6V - (24.5V - 20.6V) \times \frac{475}{555410} \triangleq \underline{+20.597V}$$

This value cannot be achieved in practice as the software modifies all digital demands by a factor of approx 0.97. Use of 20.6V Master Reference and this gain factor gives a margin for accurate calibration, from digital gain factors held in the non-volatile calibration memory.

4.6.11 Bipolar Reference Switching

The polarity-reversal relay RL1 is driven from M31 pin 4, M14 and M29 (Circuit Diagram 430444 Sheet 4). For positive outputs RL1 is energised; and for negative outputs, de-energised.

For positive DC Voltage outputs, common-4 is connected via RL1-8 as DC Ref Lo which is tied to the DC Assembly common-1 and the front panel Lo terminal. The summing amplifier output star-point connects via RL1-5 to become positive DC Ref Hi for the Error Amplifier on the DC Assembly.

For negative DC Voltage outputs. RL1-10 connects the summing amplifier output star-point to Common-1 as DC Ref Lo, and Common-4 becomes negative DC ref Hi via RL1-7.

When option 20 is fitted, RL2 can be energised for current outputs by selection of I function (M19 pin 7 on sheet 4).

In this case the summing amplifier output is used as positive or negative DCI Ref, to drive the voltage-to-current converter on the I/Ω pcb.

4.6.12 Power Supplies

To avoid the effects of common-mode transients on the lines from the in-guard common-4 power supply at the rear of the instrument, the +36V, +18V and −15V supplies entering Reference Divider pcb are heavily filtered. The +18V supply is regulated after filtering to generate +15V supply.

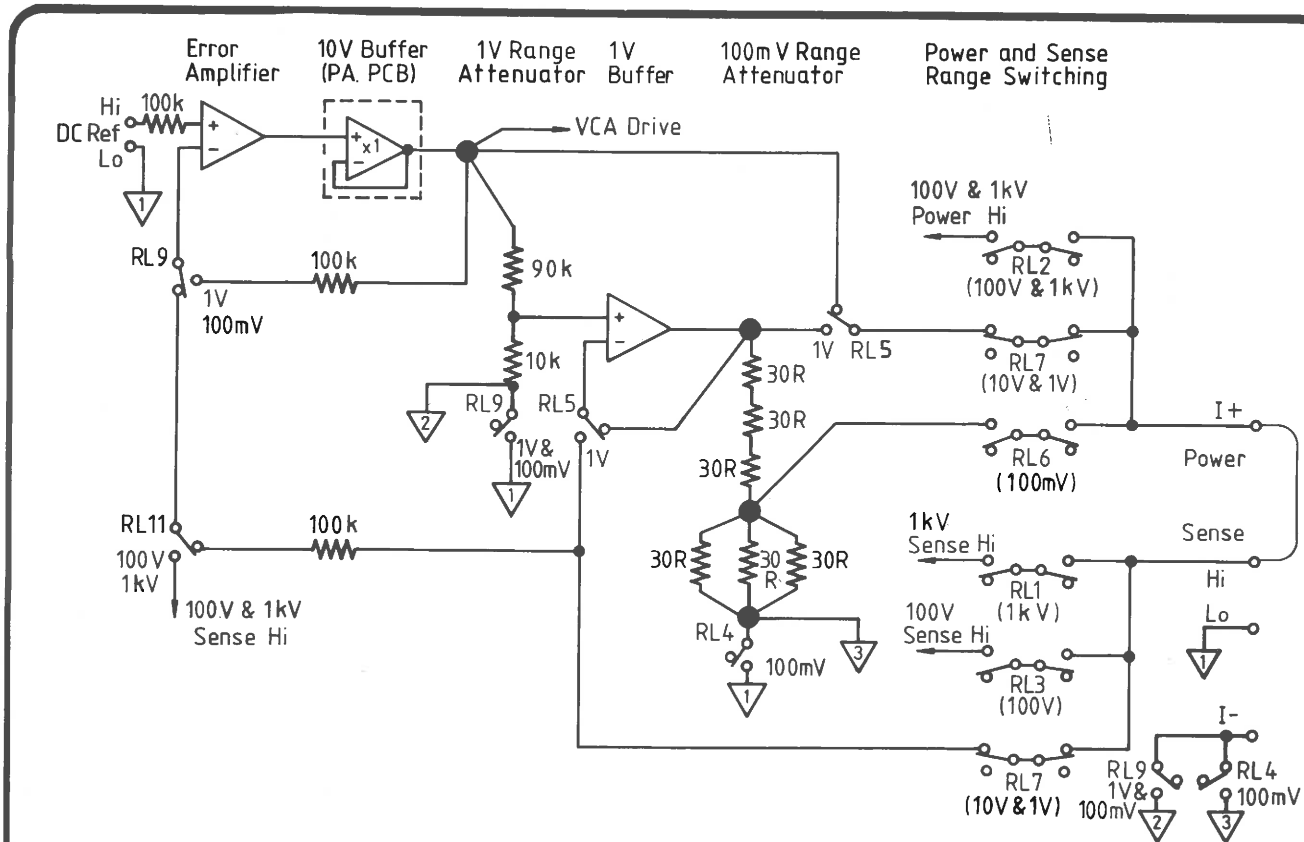


FIG. 4.32 LOW VOLTAGE — SIMPLIFIED FUNCTIONAL DIAGRAM

4.7 LOW VOLTAGE

The circuits described in this section perform the following functions:

(1) Buffer the DC REF voltage (−20V to +20V) and provide output voltages to the instrument terminals, on 10V DC Range.

(2) Attenuate the 10V Range voltages and provide output voltages (−2V to +2V) on 1V DC Range.

(3) Further attenuate the 1V Range voltages and provide output voltages:

−200mV to +200mV	on	100mV Range
−20mV to +20mV	on	10mV Range
−2mV to +2mV	on	1mV Range
−200µV to +200µV	on	100µV Range

(4) Sense the voltages at the output terminals (or at the load in Remote Sense) in closed negative-feedback loops which compare the output voltage with the DC REF (or attenuated DC REF) voltages from the Precision Divider, generating analogue control signals to correct the output voltage on 10V and 1V ranges.

(5) Provide switching of DC Voltage Ouput, Range, Guard and Sense, under the control of signals from the Analogue Control Interface.

(6) Sense excess currents in the output circuit, providing a $\overline{\text{LIM ST 1}}$ status signal to the CPU via the Analogue Control Interface.

(7) Sense excess voltages (>130V) on the PHi (I+) output line, providing a $\overline{\text{HVST}}$ status signal to the CPU via the Analogue Control Interface. The low voltage generation circuitry and Range switching are illustrated in fig. 4.32.

All the circuits described in this section are located on the DC PCB Assembly, except the 10V Buffer, which is placed on the PA (DC) Assembly.

4.7.1 General

When DC Function is selected, RL2 on the Reference Divider pcb feeds the output of the summing amplifier into the DC pcb Assembly as DC REF (Hi and Lo), the value of which represents the demanded output voltage and polarity.

The DC Voltage circuitry selects the required range, from switching data transmitted into guard via the Serial Data Link. The appropriate range circuit generates the demanded voltage at the output terminals. Output switching and protection is provided.

4.7.2 10V Range (Fig. 4.32 and Circuit Diagram No. 430445)

In Fig. 4.32 the relay contacts are shown in positions set for the 10V Range. The 1V buffer and attenuators have no effect.

DC Ref is variable between −20V and +20V with respect to common-1 (Instrument Lo terminal). The Error Amplifier and 10V Buffer are connected as a voltage-follower when I+ is connected to Hi (either local or remote sense).

The output from the 10V Buffer is connected directly to I+ via RL5 and RL7 power contacts, and the sense feedback connects via RL7 sense contacts, RL11 and RL9 back to the Error Amplifier inverting input. The Output voltage at the Hi line is adjusted by the feedback until it equals the DC Ref Value, i.e. for zero differential input to the Error Amplifier.

4.7.3 1V Range

Relays RL5 and RL9 change over to provide the 1V Range Switching. (Four positions on Fig. 4.32). RL9 transfers the sense point of the Error Amplifier and 10V Buffer to the star-point at the top of the 1V Range attenuator, and also connects the lower end of the attenuator to Common-1.

The DC Ref Voltage now appears across the 1V Attenuator, which applies one tenth of its value to the 1V Buffer. RL5 connects the 1V Buffer output to the I+ terminal, and its Feedback point is the Hi terminal.

The output voltage at the terminals is adjusted by the feedback until it equals one tenth of the DC Ref Voltage.

4.7.4 100mV Range

Relay RL5 switches the 1V Buffer feedback to its own output, which drives the 100mV Range Attenuator. RL4 connects the lower star-point of the attenuator to common-1 (I- and Lo terminals).

All RL7 contacts are disconnected and RL6 connects the attenuated output to the I+ terminal.

(Note that on 100mV Range, the Hi and Lo terminals are permanently connected to the I+ and I− terminals, i.e. Remote Sense is not available).

On the 100mV Range the DC Ref Voltage is divided by 10 in the 1V Range Attenuator, and again by 10 in the 100mV Attenuator. Full Range voltage of 100mV is thus derived from 10V DC Ref, and the same full span of the Reference Divider output is employed.

4.7.5 100μV – 10mV Ranges

These ranges use the same relay settings as 100mV Range, so the output voltages remain at 1/100 of the DC Ref voltages. The differences lie in the spans of DC Ref voltages used.

To achieve the correct DC Ref span, the appropriate scaling is computed digitally and the 4-byte binary words set in the 13- and 12-bit comparator latches of the Analogue Interface. The DC Ref spans are scaled as follows:

10mV Range	–	−2V ↔ +2V	(÷ 10)
1mV Range	–	−200mV ↔ +200mV	(÷ 100)
100μV Range	–	−20mV ↔ +20mV	(÷ 1000)

Because of this scaling, the resolution available on these ranges is reduced in proportion to the scaling ratio. The displayed output resolution is automatically adjusted according to range selection:

10V, 1V and 100mV Ranges	7½ digits
10mV Range	6½ digits
1mV Range	5½ digits
100μV Range	4½ digits

4.7.6 Error Amplifier (Circuit Diagram No. 430445 Sheet 1)

The DC Ref Voltage from the Reference Divider is applied to two amplifiers: M20 is a high-gain chopper-stabilised integrator of approximately 10Hz bandwidth, Q11 provides additional bandwidth for rejection of HF common-mode noise. M19 provides additional gain and the output drive to the 10V Buffer through a diode clamp circuit for transient suppression. The whole amplifier is bootstrapped by M18, D44, D45, Q7 and Q10. Q8 and Q9 provide 1.4mA constant-current drives for D44 and D45 over the range of BS-common variation (−20 to +20V). Extensive screening and filtering is employed to eliminate the effects of the chopping spikes at inputs and output of M20.

4.7.7 10V Buffer (Circuit Diagram No. 430449 Sheet 5)

The discrete, complementary, 10V Range buffer-amplifier is located on the PA pcb. Its power stage provides the full output current, so the heat from its power stage is developed outside the Chassis Assembly (Thermal shield) and dissipated by forced-air cooling from the fan. Its output is fed back on to the DC pcb for range and output switching.

4.7.8 1V Buffer (Circuit Diagram No. 430445 Sheet 2)

The output from the 10V buffer (10V O/P A) is divided by 10 in the 1V Attenuator (R73/R74) and applied to dual source-follower Q6 and chopper-stabilised integrator M16. This is a simplified version of the Error Amplifier, but with one tenth of its dynamic range. M17 drive to output buffer is clamped to suppress transients. On 10V range the 1V amplifier is isolated from the instrument output circuit by relays RL5 and RL9. On 1V Range it acts as a voltage follower, feeding the instrument I+ terminal, and receiving its sense feedback from the instrument Hi terminal. On 100mV – 100μV Ranges its sense is directly fed back from the star-point at TP12. On these lower ranges one tenth of its output at the TP9 star-point feeds the instrument I+ terminal, so there is no remote sensing.

The 1V amplifier is bootstrapped by M13, D25, Q3 and dual op-amp M14. M15 (1V Output buffer) is not bootstrapped, Q4, Q5, D28 and D29 provide current limiting.

4.7.8.1 Model 4000A – 1V and 100mV Precision Attenuators (Layout Drawing 400445 Sheet 1 and Circuit Diagram 430445 Sheet 2)

In the Model 4000A, the DC PCB is fitted with uprated 1V and 100mV attenuators, to hold the specification over a wider temperature range than the 4000:

(1) R73 and R74 are combined in one 90k/10k unit (part no. 090058/A).
(2) R69, R70, R71, R72, R75, R76 are combined with changed values in one 1k/111.11R unit (part no. 090059/A).

4.7.9 Output Switching (Circuit Diagram No. 430445 Sheet 3)

The PHI and SHI outputs from the Range relays (sheet 1) are passed to the instrument output terminals via relay contacts which provide switching for Remote/Local Sense and Guard, and Output On/Off; for DC Voltage Ranges. The terminal lines are switched for function changes on the I/Ω PCB Assembly if option 20 is fitted. When option 20 is not fitted, the I/Ω Link pcb (Part No. 410182-3) is fitted in place of the I/Ω PCB Assembly, providing direct connections to the instrument terminals.

4.7.9.1 Remote Sense Switching

Relays RL10 and RL12 connect PHI to SHI and PLO to SLO when Remote Sense is not selected. In Remote Sense the contacts are opened, for full 4-wire sensing at the load external to the instrument. For DC Voltage Ranges with Output On, the Lo terminal is connected to common-1 by RL8-14, completing the circuit to the 100mV and 1V attenuators' low-impedance points, and to DC Ref Lo. At the same time, the I+ terminal is connected through R32 to common 2A or 3A, by RL8 and RL9, or RL8 and RL4.

The current passing through the load is monitored as a voltage across R32 by M9.

4.7.9.2 Remote Guard Switching

The internal guard shields are connected directly to the Instrument Guard terminal (J5 – 15 to J5 – 11). When Remote Guard is not selected, RL15 – 8 connects the guards to I– (PLO) at the junction of F5 and F6. In Remote Guard the contact is opened to isolate the guards from I–.

4.7.9.3 Output On/Off

With Output selected On in DC Voltage Function RL14 connects PHi to I+, and SHi to Hi terminals. RL13 connects PLo to I–, and SLo to Lo terminals.

4.7.10 Over Current and Over Voltage Sensing (Circuit Diagram No. 430445 Sheet 3)

The circuit shown on sheet 3 may be divided into two separate functions providing two separate outputs, which are passed to the CPU via the serial data link:

$\overline{\text{LIM ST 1}}$ (Limit status 1) is normally logic-1 (pulled to 0V by AN 2 on the Reference Divider pcb), and logic-0 (–15V) when the 4000 Output current exceeds 25mA (at approximately 28.5mA).

$\overline{\text{HV ST}}$ (High Voltage Status) is logic-1 (pulled to 0V by AN 2 on the Reference Divider pcb) when the output voltage is below 110V, and logic-0 (–15V) when the output voltage exceeds 110V (at approximately 130V).

4.7.10.1 Over Current Sense

The current taken by the instrument load is diverted from common-1 (used as reference common only) and returned through R32 to common-2 (common-3 on 1V range for 1V buffer).

The voltage developed across R32 is buffered by M9 op-amps. M9 pin 1 output voltage is level-shifted by D11 and D7, divided by R12, R11 and R18, R17 and applied to M8 pin 5 (M9 pin 1 voltage + approx. 650mV) and M8 pin 1 voltage – approx. 650mV).

M8 pins 6 and 10 are referred to common by M9 pin 7.

Under normal operation, when the output current is less than 25mA, both M8 outputs at pins 7 and 8 are at +15V, reverse-biassing D9 and D8, so that the $\overline{\text{LIM ST 1}}$ is at 0V (logic-1).

If the output current through R32 exceeds approximately ± 28.5mA, the voltage across it exceeds ± 650mV. Either D8 or D9 is forward-biassed by –15V at its cathode as its M8 op-amp input polarity reverses. R14 and R15 ensure rapid switching action in case of a short-circuited output.

D9 or D8 conduction sets $\overline{\text{LIM ST 1}}$ to logic-0 (–15V). The CPU responds by presenting "Error OL" on the MODE display. If 100V or 1000V is selected, the output is switched off.

The 10V and 1V buffers are protected by current limiters which operate between 30 – 40mA. The 100mV – 100μV ranges are not protected by current limiters, and on these ranges the over current sense circuit is disabled by RL4 and RL9.

4.7.10.2 Over Voltage Sense

M9 pin 1 is referred to Common-1 (Sense Lo) either through RL12 (Local Sense) or via the external load circuit (Remote Sense). R29 and R22 divide the output voltage by 54 at TP 17, buffered by M10. M8 forms the comparator, using D11 as 2.45V reference for positive, and D7 for negative, output voltages.

For output voltages between –110V and +110V, TP7 is between –2.1V and +2.1V so both D5 and D6 are reverse-biassed by +15V on their cathodes, and $\overline{\text{HVST}}$ is at logic-1. For output voltages greater than approximately ± 130V, TP17 voltage is greater than ± 2.45V. Either D6 (positive voltages) or D5 (negative voltages) is forward-biassed by –15V at its cathode, as its M8 op-amp input polarity reverses.

D5 or D6 conduction sets $\overline{\text{HV ST}}$ to logic-0 (–15V). The CPU is now aware that the 4000 output voltage exceeds ± 110V. If High Voltage state has not been commanded, a fault is assumed and FAIL 2 message is presented on the MODE display.

4.7.11 DC PCB Switching Logic (Circuit Diagram 430445 Sheet 4)

The analogue control signals are transferred into guard on the Reference Divider pcb, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is employed (0 = −15V, 1 = 0V) for the signals entering the DC pcb via J5 from the Mother pcb.

M1 and M2 are Darlington open-collector Inverter/Drivers. The Relay Drive Logic places a logic-1 (0V) on the input of selected drivers, and logic-0 (−15V) on those not required. A selected driver operates its relay(s) by pulling its output Voltage to −14V.

Whenever a switching command has been received, the CPU performs a control data transfer and the UPD (IG) line from J 5 — 104 is pulsed to −15V for 50mS.

Q1 is turned on, applying +15V to the relays connected to its collector (Relays Rl 1, 2, 3 and 15 are permanently connected to +15V). The selected relays are thus energised by 30V, but after the UPD (IG) pulse has finished they are held on by 10.5V between −3.5V at the anode of D2 and −14V at the selected driver output. This method reduces the local heat generated by energised relay coils, in the relay contacts.

4.7.11.1 Range Switching Logic

Range control data is input as a 3-bit code on DC Rϕ, DC R1 and DC R2 lines. The bit-pattern is decoded by M4 to energise the correct relays for the selected range. As the 100μV, 1mV, 10mV and 100mV ranges all use the same analogue circuitry, only one bit-combination is required for these four ranges. The resulting five combination variations are listed in Table 4.1 against the range selections, showing the states of M4 'Q' output pins and the relays energised for each range.

Note that deselection of DC function de-energises all range relays except RL4, RL5 and RL9, regardless of the range code being transferred.

Range	Bit Pattern			M4 Output pins					Range Relays Energised								
	DC R2	DC R1	DC RØ	7	9	10	11	12	RL4	RL6	RL9	RL5	RL7	RL3	RL2	RL11	RL1
100mV	1	0	0						✓	✓	✓						
1V	0	1	1	1	1						✓	✓	✓				
10V	0	1	0			1							✓				
100V	0	0	1				1							✓	✓	✓	
1000V	0	0	0					1							✓	✓	✓

Notes. 1. 1 = 0V, 0 = −15V

2. All M4 Output pins at 0 unless shown at 1.

3. Unless shown energised on the table, all relays are de-energised. (Relay contacts on Circuit Drawing 430445 shown in de-energised state.)

TABLE 4.1 RANGE SWITCHING VARIATIONS

4.7.11.2 Function and Output Switching Logic

The DC output voltages are passed through the DC pcb on all ranges. RL13 and RL14 connect the PHi, PLo, SHi and SLo to the I+, I−, Hi and Lo terminals of the instrument. Four signals control these relays:

OFF at logic-0 when Output is selected ON.
BARK DEL at logic-0 unless the watchdog has tripped
AC FUNCT always at logic-1.
DC FUNCT at logic-1 if DC Function is selected

Under these conditions M5 pins 1, 2 and 8 are set to logic-0, M5 — 9 is at logic-1 so RL13 and RL14 are energised. Any change in one of the three switchable inputs will disconnect the terminals from the output.

Additionally, when Ω or I function is selected, DC FUNCT changes to logic-0, and RL8 is energised (DC). This disconnects SLo from common-1, and PLo from the Over voltage and Over current Sense circuit.

4.8 HIGH VOLTAGE

The circuits described in this section perform the following functions:

(1) Generate a 16kHz sine wave by band-pass filtering a 16kHz squarewave from the Reference Divider Assembly

(2) Control the amplitude of the 16kHz sine wave in a voltage-controlled amplifier, followed by power amplification to drive a step-up HV transformer.

(3) Rectify and filter the HV transformer secondary voltage to provide DC voltages to the I+ terminal:

-200V to +200V on 100V Range
-1200V to +1200V on 1000V Range

(4) Sense the voltages at the output terminals (or at the load in Remote Sense)

(5) Attenuate the sensed voltage and compare against the DC Reference Voltage in the Error Amplifier, using the error voltage as drive to the Voltage-Controlled Amplifier.

The circuits together form a negative-feedback loop which refers the output DC voltage to the value of the DC Reference Voltage, using AC drive transformation and DC sense attenuation as means of achieving the required high voltage outputs. This is illustrated in Fig. 4.33, which shows 100V Range selected, positive output in remote sense with output on.

In the main, the circuits are located on the Power Amplifier (DC) Assembly. The Error Amplifier, VCA drive circuitry, sense attenuator, overvoltage and overcurrent detectors and output switching are located on the DC PCB Assembly. Some of these circuits are common to the Low Voltage DC functions.

4.8.1 General (Fig. 4.33)

AC transformation is carried out at 16kHz, derived from M16 in the Analogue Interface 13-bit counter, and transferred into guard as a square wave through opto-coupler M3 on the Reference Divider pcb.

The square wave is filtered to provide a 16kHz sine wave. The filter has high selectivity at 16kHz to eliminate harmonic distortion.

The sine wave amplitude is controlled by the DC loop-error drive in a Voltage-Controlled Amplifier (VCA), and power-amplified to drive the step-up transformer primary. Range switching is achieved by changing the step-up ratio, both primary windings being connected in series on the 100V Range.

A constant-current source acts as a shunt to sustain the current drawn from the high-voltage secondary winding through the bridge rectifier, and polarity is switched with respect to common-2 via the LC-filtered ± 15V common-2 supplies. Positive polarity output is referred to -15V at zero output, to provide an overlap with Negative polarity output referred to +15V. The overlap allows digital calibration constants to be used to align zero voltage output in both polarities to the same calibrated zero.

The main output filter is placed in the output line. This is a low-pass filter with a high rejection at 16kHz, reducing the ripple voltage to within specification limits.

Shutdown of the high voltage power-circuitry occurs when an output current of 30 – 40mA is detected in the Current Limit circuitry. The output voltage is fed out through the Range switch on the DC pcb, where it is subject to Remote Sense and Output On/Off switching and over voltage detection, before being passed to the I+ terminal by the same route as for low voltage ranges. The external current is sunk into common-2 via the over-current detector, which warns the control processor when the output current exceeds approximately 28.5mA. On 100V and 1000V ranges the processor will switch the output off on receipt of the overcurrent signal from either the current limit circuit or the overcurrent detector.

The output voltage is sensed between the Hi and Lo terminals. Lo is referred to Sense attenuator Lo and DC Ref Lo. The Hi sense voltage is divided in the Sense Attenuators by 10 (100V Range) or 60 (1000V Range). The attenuated output is compared against DC Ref Hi in the Error Amplifier, and modifies its output to the 10V Buffer and VCA drive. The 10V Bootstrap, in addition to supplying the Error Amplifier, also buffers DC Ref Hi as reference for the VCA Drive circuit.

The error voltage between the buffered DC Ref Hi and the 10V buffer output is conditioned by the VCA drive to provide a suitable control signal for the VCA itself.

The Sense loop thus stabilises the High Voltage DC output to a value which on 100V range is 10 times the DC Ref voltage and on 1000V range is 60 times the DC Ref voltage. On 1000V range, the DC Ref voltage is scaled digitally so that Full Scale of 20V corresponds to 1200V on the OUTPUT display and at the output terminals.

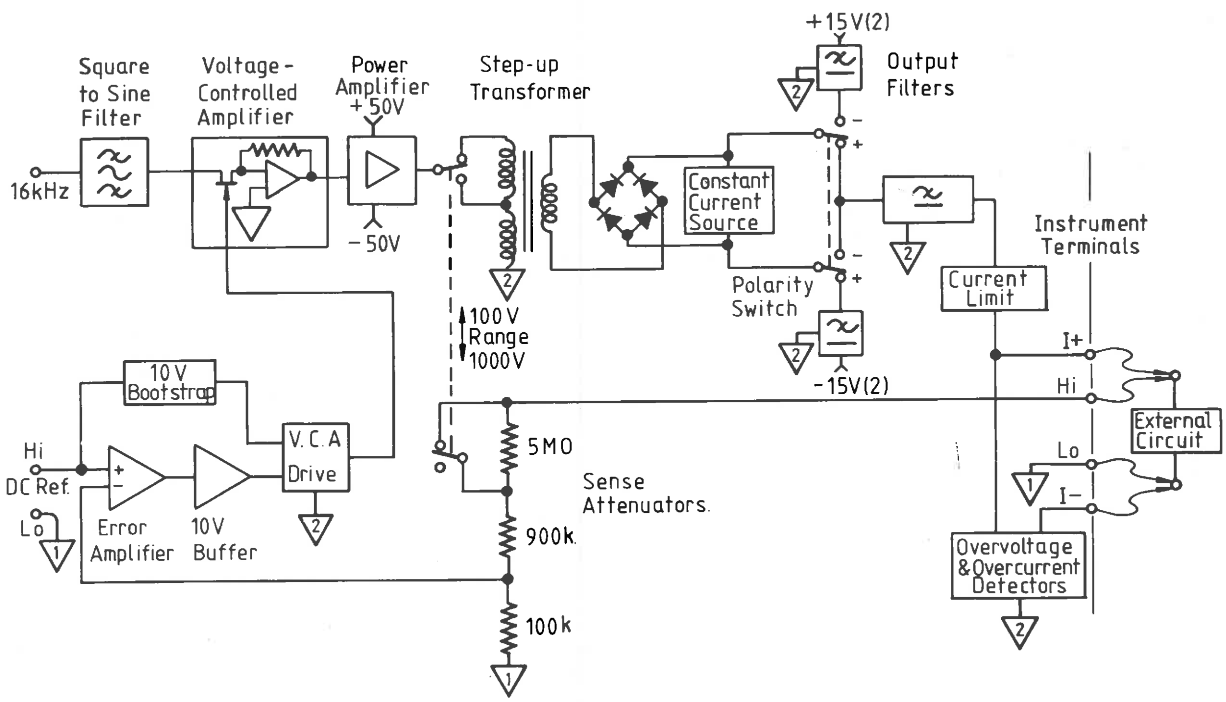


FIG. 4.33 100V AND 1000V RANGES – OUTPUT LOOPS

4.8.2 Square-Sine Filter (Circuit Diagram No. 430449 Sheet 4)

The 13-bit counter in the Analogue Interface generates 16kHz at M16-14 (Circuit Diagram 430443 Sheet 2), which is transferred into guard through opto-isolator M3 on the Reference Divider (Circuit Diagram 430444 Sheet 4). The 16kHz square wave, switching between logic-1 = 0V and logic-0 = −15V, enters the Power Amplifier pcb on J9-86.

M8 buffers apply the full 15V p-p squarewave to coupling capacitors C38 and C39. M3 input circuit is a 16kHz series-tuned filter. This, together with M3 active low-pass filter, produces a sine wave at TP15 of 0.6V to 0.8V pk-to-pk amplitude and approx 5% distortion.

4.8.3 Voltage Controlled Amplifier

The DC loop error voltage is applied from the VCA drive to Q26 to control the input resistance to M4. Q26 and R66 are matched to standardise the gain range (mid-range gain of approx 0.5). A manual gain adjustment (Q28, R68, R65) is provided for test purposes.

M4 output is AC-coupled as drive to the power amplifier.

4.8.4 Output Clamp (Circuit Diagram No. 430449 Sheet 1)

When the CPU switches the Power Amplifier on or off in 100V or 1000V ranges, it controls the 16kHz drive to the high voltage power amplifier. For both ranges, a signal PA OFF is provided at M15 pin 5 on the Reference Divider (Circuit Diagram No. 430444 Sheet 4) which is buffered by M8/Q43 on the Power Amplifier (Circuit Diagram No. 430449 Sheet 4), as PA OFF B signal.

With output off, the Output Clamp circuit is allowed to operate by D47 reverse bias. The ± 2.5V Reference from the 50V Power Supply is divided by R70/71/73/74 to provide ± 0.45V bias for M5 on 100V range. Q27 conducts only when the CPU has selected 1000V range, reducing M5 bias to ± 0.025V.

Example of clamp action

On 100V range, the bias on M5 pin 5 is −0.45V. If the PA output voltage is less negative than −5.95 volts, M5 pin 6 is more positive than pin 5 and D46 is non-conducting due to −15V at TP26. If the PA output is more negative than −5.95V, M5 pin 6 is more negative than −0.45V, TP26 rises to cause D46 conduction and Q33 starts to conduct. The 16kHz drive to the PA is reduced due to the extra volts drop across R87, which limits the negative half-cycles of the PA output at approx. −6V.

In similar fashion, D49 conducts on positive output half-cycles to start limiting at +6V and on 1000V range, positive and negative half-cycles start limiting at approx. 0.3V.

This limiting action ensures that when the 4000 output is off, the PA output to the step-up transformer is limited to less than 10V peak on 100V range, and less than 3V peak on 1000V range.

As the PA OFF B input is low (−15V) when output is on in 100V or 1000V range, Q33 is pinched off, and the PA output is not clamped.

Q34 in the PA drive line is pinched-off by $\overline{\text{I LIM}}$ at −15V when the output Current Limit is activated (see Section 4.8.9).

4.8.5 Power Amplifier (Circuit Diagram No. 430449 Sheet 1)

The Power Amplifier deals with AC and DC separately. The overall purpose is to stabilize the mean output level at zero DC, whilst driving the step-up transformer with a large enough voltage swing to provide DC output voltages at the I+ terminal of 200V (100V range) and 1200V (1kV range). The power delivered to the transformer is sufficient to provide output loading for each range of 25mA, with a little in reserve.

C46 is the only DC blocking capacitor in the whole amplifier, so Q36 and Q35 form the AC preamplifier as one half of an emitter-coupled cascode amplifier with Q38 and Q37. Q40 provides the constant current which reduces common mode disturbances at Q37 collector.

The DC path through the power amplifier passes through M6 and the Q38/Q37 half of the long-tailed pair. The DC loop is self-zeroing at input and output due to its three inversions in M6, Q38 and Q39. M6 is converted into an integrator by C48, so acts as a low-pass filter with unity gain at around 15Hz. Q32, Q39 and Q42 shift the DC level and provide high driver gain into the output Darlington amplifier. Q5 establishes the correct bias on Q24 to reduce crossover distortion, compensating four output V_{be} variations with temperature by being in thermal contact with the positive heat sink. Q41 provides constant current pull-down for the driver stage.

Q29 and Q30 current limiters prevent damage in the event of an output short circuit.

The d.c. output level is therefore referred to common-2 by R116 at M6 non-inverting input.

The AC loop also includes three inversions, so feedback controls both AC and DC to R96/(R87 + R88).

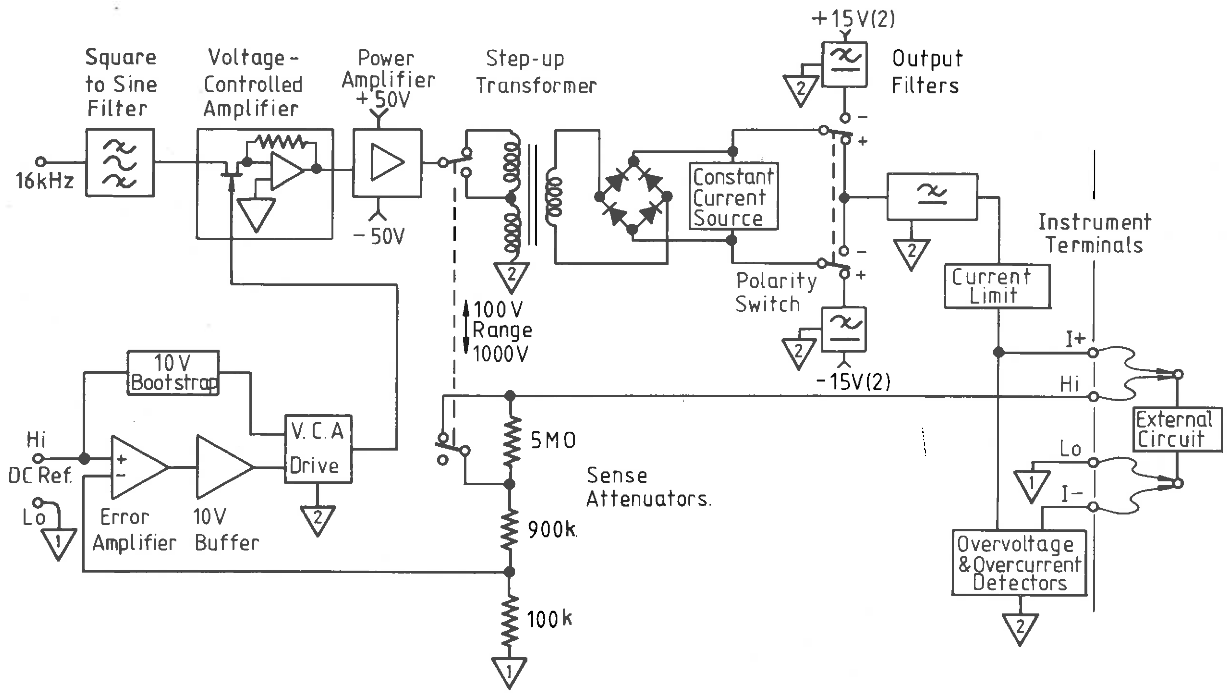


FIG. 4.33 100V AND 1000V RANGES — OUTPUT LOOPS

4.8.6 High Voltage Transformer and Rectifier (Circuit Diagram No. 430449 Sheet 3)

Relay RL2 is energised permanently when the watchdog BARK signal is low (−15V). The 16kHz PA output passes via RL2 pins 7 and 10 to RL1 contacts and to the High Voltage transformer.

When the watchdog BARK signal goes high (0V), the drive is removed and the transformer primary is shorted to common-2 as RL2 is de-energised.

RL1 is only energised on 1000V range with switch S1 ON (indicated by LED D37 lit on the PA (DC) Assembly. On 100V range it is set as shown on the circuit drawing, selecting both primaries in series for a step-up ratio of 9.2. For 1000V range, RL1 connects the PA output to only one primary winding (J6-1 to J6-4), a step up ratio of 49.2.

These ratios generate secondary voltage outputs sufficiently large to provide DC outputs from the instrument of 200V (100V range) and 1200V (1000V range).

The rectifier bridge uses to series diodes in each arm. Each diode is current-rated at 1A, with a p.i.v. of 1.5kV.

N.B. The transformer secondary, and bridge rectifier are not directly referred to any common. This allows the rectifier output to float so that it may be used for either polarity.

4.8.7 Constant-Current Source and Overvoltage Detector Assembly (400472)

4.8.7.1 Constant-Current Source

Q1-12 form a series Darlington chain, connected across the bridge rectifier output as a constant-current source, having two functions:

(1) It provides a discharge path which is a "constant" current at all output voltages, of approx 1.2mA above 120V, rising to 7mA at 0V.

(2) It maintains diode bridge D56-D63 conduction in no-load conditions. At higher voltages, D14-D17 limit Q11 base voltage to +2.4V, limiting the series current in R11 to 1.2mA, with Q13 pinched off. At lower voltages Q13 conducts, shunting R11 with 170-180 Ω (R10 plus Q13 'On' resistance which falls to approx 125Ω), and increasing the discharge current to approx 7mA.

Note that the minimum voltage applied across the constant-current source is 15V. Even at zero output voltage and current, the diode bridge generates 15V to back off the positive or negative 15V connected to RL3.

4.8.7.2 Overvoltage Detection

Zener diodes D1 – D13 form a series chain across the High Voltage supply. When the voltage exceeds 1440V this chain conducts, lifting D13 cathode and driving opto-isolator M9. M9 emitter rises, and provides a "Reset" logic-1 (0V) input to M10-10, resulting in a logic-0 (−15V) output from M10 – 13.

The operation of M10 and subsequent action is described in section 4.8.9.

4.8.8 Polarity Switching and Ouput Filter

Double-pole relay RL3 performs the polarity-reversal. With RL3 de-energised as shown the output filter is connected to rectifier negative, and +15V Common-2 supply is connected to rectifier positive. During zero calibration, the +15V is backed off to give a true zero output by an output from the rectifier.

When RL3 is energised by the POSITIVE signal from the serial data-link parallel output registers at logic-1 (0V), the output filter is connected to the rectifier positive rail, referred to −15V common-2 supply. Again, this −15V is backed off to zero when calibrated.

Filtering is accomplished in three stages:

(1) L8, R128, C58, C59 2-pole filter attenuates 16kHz by approx 30dB and 32kHz by approx 42dB.

(2) L9, L10 and associated capacitors form a 5-pole filter with elliptic characteristics, attenuating by at least 60dB above 16kHz.

(3) The final stage is formed by C1 on the Mother PCB (Refer to Circuit Diagram 430440 Sheet 1) and the output resistance (approx 500Ω) of the high voltage circuitry on the Power Amplifier PCB (Circuit Diagram 430449 sheet 3). This gives attenuations of approx. 30dB at 16kHz and 36dB at 32kHz.

4.8.9 High Voltage Output Current Limit Detector

Section 4.7.10 describes over-current sensing circuitry on the DC pcb Assembly, which provides LIM ST 1 signal when the output current exceeds approximately 28.5mA. It also generates HV STATUS signal when the output voltage exceeds 130V.

In addition to these signals; the two high voltage ranges are protected against over-voltage (see Section 4.8.7.2) and over-current on the Power Amplifier pcb itself.

4.8.9.1 Over-Current Detector

An output current of approx. 35mA will cause the output to be shutdown. Opto-isolator M11 is set to respond to a threshold level of approximately 5.25V across R143, causing conduction between pins 6 and 5.

4.8.9.2 Protection Logic

On Power-up, M10 settles into its stable state with Q (pin 2) and Q (pin 13) both at logic-1 (0V). Both sections have set and reset pins at logic-0 (−15V), and PA OFF B signal at logic-1. Q44 is cut off, as also are M9 and M11 output emitter-followers, holding M10 reset (pin 10) at −15V (logic-0).

By selecting Output On in 100 or 1000V range, PA OFF B goes to logic-0. M10 is not clocked by the negative edge, but Q44 is turned on, providing the supply to M11, which remains cut-off unless overcurrent is detected.

When an over-current is detected M11 Output stage conducts, lifting pin 5 from −15V to approximately −1V (logic-1 on M10 pin 10). $\overline{\text{The Q output of M10}}$ (pin 13) is forced into reset state. $\overline{\text{HI I ST}}$ and $\overline{\text{I LIM}}$ fall to logic-0 (−15V).

The $\overline{\text{I LIM}}$ signal switches off Q34 at the input to the Power Amplifier (sheet 1), removing the 16kHz drive, and reducing the output voltage to zero, thus providing instantaneous shut-down. $\overline{\text{HI I ST}}$ signal is returned via the serial data link to the CPU, which presents "Error OL" on the MODE display and carries out the normal Output OFF routine, disconnecting the external load, reducing R143 current to zero, hence cutting off M11 Output stage. M10 pin 10 reverts to Logic-0, sensitising the flip-flop to any positive clock-edge on pin 11.

At the same time, the PA OFF B signal rises to Logic-1, cutting off Q44, and clocking the logic-1 on M10 pin 5 through to pin 1 (Q) so Q (pin 2) goes to logic-0.

Pin 4 rises on time constant C61 R135, and the monostable times out after 8mS by forcing Reset state. Pin 1 falls to logic-0 and rapidly sets pin 4 to logic-0, sensitising the monostable to any positive clock-edge on pin 3. Meanwhile, pin 2 has reverted to logic-1, clocking $\overline{\text{the logic-1 on pin}}$ 9 through to pin 13, and returning $\overline{\text{HI I ST}}$ and $\overline{\text{I LIM}}$ signals to their non-active logic-1 state. The detector remains in this state until output is again switched ON on 100V or 1000V range. The "Error OL" presentation is retained until the user makes a further Front Panel or Remote selection.

If the instrument is operating normally with Output ON in 100V or 1000V range, and Output OFF is selected, M10 monostable pin 2 again delivers its negative 8mS pulse to Pin 11 and the logic-1 at pin 9 is clocked in. $\overline{\text{But as pin}}$ 13 $\overline{\text{is already}}$ at logic-1 this does not disturb the $\overline{\text{HI I ST}}$ and $\overline{\text{I LIM}}$ signals.

4.8.10 Output Switching, Sense Attenuator and Guard (Circuit Diagram No. 340445)

The high voltage output is taken from the Power Amplifier to be Range-switched on the DC pcb (RL2 on Circuit Diagram No. 430445 Sheet 1). On 100V or 1000V the selected PHi voltage is Remote/Local and Output ON/OFF switched before passing to the instrument output I+ terminal. Any output current drawn by the external load is returned via the I− terminal and the over-current sensor to common-2 (Refer to section 4.7.10).

The external load Lo is connected directly to the Lo terminal and hence to common-1 in the DC pcb. Load Hi is returned via the Hi terminal to the head of a high-voltage attenuator (R10, R27, R48, R66, R89, R96, R99 of circuit drawing 430445 Sheet 1), which is also referred to common-1.

The attenuator is range-switched by RL3 between 1000V and 100V ranges. On 1000V range the attenuation is 60:1, reducing Full Scale load voltage of 1200V to 20V for comparison against the DC Ref Hi voltage. On 100V range; R89, R96 and R99 divide the voltage by 10. The attenuator and DC Ref Lo are both returned to common-1.

To guard the necessarily high-impedance attenuator each connection between resistors is shielded. The potential divider R8, R9, R25, R26, R46, R47, R64, R65, R88, R95 and R98 connected between the Power Amplifier output voltage and common-2 maintains each screen at the potential of the connection it is shielding, to reduce leakage. RL3 shorts part of the divider on 100V Range to equalise potentials.

4.8.10.1 Model 4000A — 100V/1000V Precision Sense Attenuator (Layout Drawing 400445 Sheet 1 and Circuit Diagram 430445 Sheet 1)

In the Model 4000A, the DC PCB is fitted with an uprated 100V/1000V attenuator, to hold the specification over a wider temperature range than the 4000:

(1) R10, R27, R46 and R48 (1M25) are replaced by five 1MΩ resistors.

(2) R89, R96 and R99 are replaced by one 900k/100k unit.

The whole attenuator set is referenced as part no. 090057/A.

4.8.11 VCA Drive and Control

The attenuated sense signal is applied to the inverting input of the Error Amplifier via RL11-10 and RL9-14. This bootstrapped, high-gain amplifier compares the sense signal with DC Ref Hi. When both are equal: the output from the 10V buffer at TP5 star-point, the bootstrap common BS2, DC Ref Hi and the sense signal are all at the same level. Therefore the differential input to M12 (VCA error amplifier) is zero at R42/R43.

The gain from M12-1 to I+ terminal is approx. x2000 on the 1000V Range and approx. x400 on the 100V Range. Components R97, C33 at the Error Amplifier input, and R33, C16 on M11 provide frequency compensation for the overall loop.

The second M12 stage acts as a polarity switch. With OUTPUT ON + LED lit, the POSITIVE control signal is at logic-1 (0V). Q2 conducts setting M12 non-inverting input (pin 5) to zero volts, so the amplifier inverts the pin 6 input. If OUTPUT ON- LED is lit the POSITIVE signal is at logic-0 (-15V) cutting off Q2, M12 pin 5 follows the pin 1 voltage, so the amplifier acts as a voltage follower.

The polarity switching is necessary to adapt the bi-polar action of the error amplifier to the unipolar sensitivity of the Voltage Controlled Amplifier.

4.8.11.1 VCA Action

If a user increases a positive OUTPUT display value, the positive DC REF Hi voltage will increase, (a demand to increase a positive output voltage). The polarity switch inverts the positive input from M12-1. So M12-7 feeds a negative output to M11. This is inverted and fed, via the Mother pcb, to D36 on the Power Amplifier Assembly as an error signal (Circuit Diagram No. 430449 Sheet 4).

On the Power Amplifier Assembly; as the VCA control signal becomes more positive the gain of M4 between TP15 and TP19 is increased, thus increasing the output at I+. The attenuated sense voltage rises to equallise the differential inputs to the error amplifier, and the I+ voltage stabilises at its new value.

M4 has a maximum gain of x12 when TP24 is at 0V and a minimum gain of x0.01 when TP24 is at -12V or lower.

4.8.12 Decoding Logic (Circuit Diagram 430499 Sheet 4)

4.8.12.1 "PA OFF"

The PA OFF signal is originated by the CPU and latched at M15 Q2 (pin 5) Serial/Parallel data converter on the Reference Divider pcb (Circuit Diagram No. 430444 Sheet 4); as logic-1 (0V) for PA OFF, and logic-0 (-15V) to provide the DC 100V/1kV drive from the Power Amplifier Assembly. Under normal use test link TLJ is made, but for test purposes link TLJ can be unsoldered, and TLH made. PA OFF is buffered by M8 and Q43 as PA OFF B, which has two functions:

(1) At logic-1 it allows the output clamp to operate but at logic-0 removes the clamp from the PA input. (Refer to Section 4.8.4).

(2) A 0-1 transition by PA OFFB clocks the over-voltage and over-current detector M10 to reset. (Refer to Section 4.8.9).

4.8.12.2 "POSITIVE"

The polarity of 100V and 1000V Range outputs is determined by the CPU. In addition to changing the polarity of the DC Ref Hi signal fed from the Reference Divider into the DC Error Amplifier, the POSITIVE signal performs polarity switching in the VCA drive (refer to sections 4.6.11 and 4.8.11). On the Power Amplifier pcb it energises RL3 when at logic-1 (0V), connecting the positive rectified voltage from the HV transformer to the Output Filter (Refer to Section 4.8.8). At logic-0 (-15V), RL3 is de-energised, and the drive to the output filter is negative.

The POSITIVE signal is latched at M31 Q1 (pin 4) on the Reference Divider pcb serial/parallel data converter. (Refer to Section 4.5.5).

4.8.12.3 "HV ENBL"

On 1000V Range, HV ENBL signal is at logic-1 (0V) to energise RL1, whose contacts apply the P.A. output to the single primary winding (J6-1 to J6-4) of the high voltage transformer. (Refer to Section 4.8.6). The Output Clamp circuit requires reduced reference voltages on this range, so HV ENBL is buffered as PA 1kV signal and applied to Q27 for this purpose (Refer to Section 4.8.4). Switch S1 on the PA pcb can be set to disable the 1kV Range output by releasing RL1 and shorting the 16kHz drive to the PA. When the switch is in the "Enable" position, LED D37 lights as a visible warning.

4.8.12.4 "DC ST"

The DC ST line returns to the Reference Divider pcb, (Circuit Diagram No. 430444 Sheet 4), and is connected there to M21 pin 5. An identical line from the DC pcb also connects to M21 pin 5. Each line is pulled down to -15V through a 15kΩ resistor. When both lines are correctly connected, M21 pin 7 (TP17) is at logic-0 (-15V), input to M22-13 Parallel/Serial data converter. The DC status bit is read out of the SSDA "Receive" register by the CPU on each data transfer. If at logic-0, DC function may be selected by a user. If at logic-1, the CPU inhibits selection. The same method is used for AC ST, but as AC is not fitted in the 4000, M22-4 will always be at logic-1.

4.8.12.5 "BARK"

The Safety Monitor (Watchdog) produces the BARK signal when the CPU or SSDA is functioning incorrectly, and the SAFETY message is presented on the MODE display. The BARK signal is normally at logic-0 (-15V) so that RL2 is energised, applying the PA output to the HV transformer. When a failure trips the watchdog, BARK goes to logic-1, de-energising RL2, which disconnects the PA output and shorts the HV primary to common-2, reducing the 4000 output voltage to zero. (Refer to Section 4.5.6 for information on the Safety Monitor).

4.8.13 50V Power Supply (Circuit Drawing No. 430449 Sheet 2)

The power supply on the PA pcb provides ± 50 volts regulated power for the Power Amplifier. It incorporates "Foldback" current limiting and "excess input voltage" limiting for both polarities. Overheating of the positive or negative heatsink (PA Output stages) generates a $\overline{\text{TEMP ST}}$ signal to the CPU via the serial data link. Overheating of the PS/I heatsink, failure of the ± 15V supply or ± 50V output undervoltage; generates a $\overline{\text{PS ST}}$ signal to the CPU.

In both cases the CPU sets 4000 Output Off and displays a FAIL message:

FAIL 1 – $\overline{\text{TEMP}}$ ST at Logic-0
FAIL 7 – PS ST at Logic-0

When the power supply is operating normally, both signals are at logic-1. The logic levels for these signals at TP3 and TP22 are Logic-0 = –15V, Logic-1 = 0V (common-2).

4.8.13.1 50V Supply Regulation

Power is input from the Line Transformer secondaries, both fused at 4A. R1 provides an adjustment to eliminate line frequency hum on the guard shields, in conjunction with R52/C4 on the Mother pcb. (For adjustment procedure refer to Section 5.7).

The secondaries are referred to common-2, and the rectified outputs are smoothed by reservoir capacitors C2 and C3 at the rear of the Mother pcb.

The series regulation elements Q3 and Q4 are mounted on the PS/I heatsink assembly. These Darlingtons are driven by Q10 and Q9.

NB. The following description refers only to the positive 50 Volt supply. The action in the negative supply is similar.

Q17 generates constant current of 3mA to activate D15 2.45V Zener diode. The +2.45V provides the positive reference supply for the Output Clamp circuit (Refer to Section 4.8.4.). It is also the reference for comparator M2-2. The output voltage is sensed on the +50V rail and divided down to Reference potential at M2-3. M2-1 output drives Q6 whose collector voltage at TP18 controls Q3 (PS/I Heatsink) conduction via Q10. If the +50V rail voltage falls due to loading, TP18 voltage rises, increasing the conduction of Q3 to restore the output rail voltage.

4.8.13.2 50V Current Limit (Positive 50V only described)

R24 is the series current detector, which drops 0.4V at 2.7A. Q19 generates a constant current of approximately 3mA which can be shared between Q12 and Q11. Q12 is saturated, generating approximately 200mV across R39. With little or no load current passing through R24, Q11 is off. When the current through R24 reaches approximately 2.7A, Q11 is switched on.

Q11 collector voltage rapidly falls below Q10 base voltage, D25 conducts and pulls Q10 base voltage down, reducing Q3 conduction. This reduces the current through R24, but with Q11 fully conducting, it is held on by the voltage across R39. As a result, Q3 conduction can fall to approximately 500mA, and with the overload still present, the 50V rail voltage can fall to approximately 12.5V. This is a stable condition which persists until the 4000 is powered-down. As the voltage falls below +43V the under-voltage detector is activated (Refer to Section 4.8.13.3).

4.8.13.3 Under-Voltage Detection

With the Power Supply operating normally, the positive rail voltage lies between +49.5V and +52.2V. M1-3 is held at approximately +2.85V, and as the +2.45V Reference is connected to M1-2, D11 is reverse-biassed by +15V at M1-1. (D11 anode is normally pulled to 0V by AN2 on the Reference Divider pcb – Refer to Circuit Drawing No. 430444 Sheet 4).

When the rail voltage falls below approximately +43V, M1-3 falls below +2.45V, and M1-1 changes polarity to –15V, forward-biassing D11, and setting $\overline{\text{PS ST}}$ to logic-0. This is detected by the CPU, which presents FAIL 7 on the MODE display and sets 4000 Output OFF.

4.8.13.4 50V Power Supply Shutdown

At normal operating temperatures, the PS/I heatsink thermal detector has high resistance (approximately 100kΩ). Q3 base is biassed by approximately +1V from the junction of R13/R9, so Q3 is saturated, holding approximately 150mV across R7 – R6, cutting Q1 off. The same 150mV holds p-channel FET Q4 On, which in turns holds Q2 cut off. D5 is unbiassed so $\overline{\text{PS ST}}$ is at logic-1 (0V).

If either the +15V or –15V supply fails, the voltage at Q3 base falls and cuts Q3 off. The clamp on Q1 base is removed, and it draws collector-current through R26, turning off the conduction in Q3 (PS/I heatsink). In the negative supply, Q4 is cut off, and Q2 turns off Q4 (PS/I heatsink) conduction. D5 is forward-biassed by –15V from the unregulated supply, clamped by D4, setting $\overline{\text{PS ST}}$ to logic-0 (–15V).

If the PS/I heatsink overheats, the temperature is detected by R3 (NTC thermistor). R3 resistance falls from 100kΩ to 100Ω (approximately) as its temperature rises from 80°C to 90°C, reducing Q3 V_{be} to approximately 200mV. Q3 cut-off initiates the power supply shutdown as for loss of ±15V supply.

4.8.13.5 PA Overheating

The Positive and Negative Heat Sink assemblies house the Power Amplifier output transistors. Each assembly is sensed by a NTC thermistor. These are connected in parallel, in series with R35 across the –15V supply. If either heatsink overheats, the $\overline{\text{TEMP ST}}$ signal changes from logic-1 to logic-0, the CPU presents FAIL 1 on the MODE display, and turns the 4000 Output OFF.

4.9 CURRENT (Option 20)

The circuits described in this section perform the following functions:

(1) Divide the DCI REF voltage (−20V to +20V) by 10 (−2V to +2V)

(2) Generate output currents whose value varies directly as the value of the DCI REF Voltage.

(3) Provide switching of DC Current Output and Range, under the control of signals from the Analogue Control Interface.

(4) Sense excess output voltage, providing a LIM ST 1 status signal to the CPU via the Analogue Control Interface.

The basic arrangement of the voltage-to-current convertor is shown at Fig. 4.34.

The Voltage to Current converter is located on the I/Ω pcb. It provides five ranges of current output, drawn from the 4000 I+ and I− terminals; the Hi and Lo terminals are not used. The five ranges are 1A, 100mA, 10mA, 1mA and 100μA, each extending to 100% overrange.

The output currents are bipolar, controlled within each range by the value of reference voltage (DC 1 Ref) applied from the Reference Divider. The two higher ranges have their reference scaled in software to optimise the choice of circuit components.

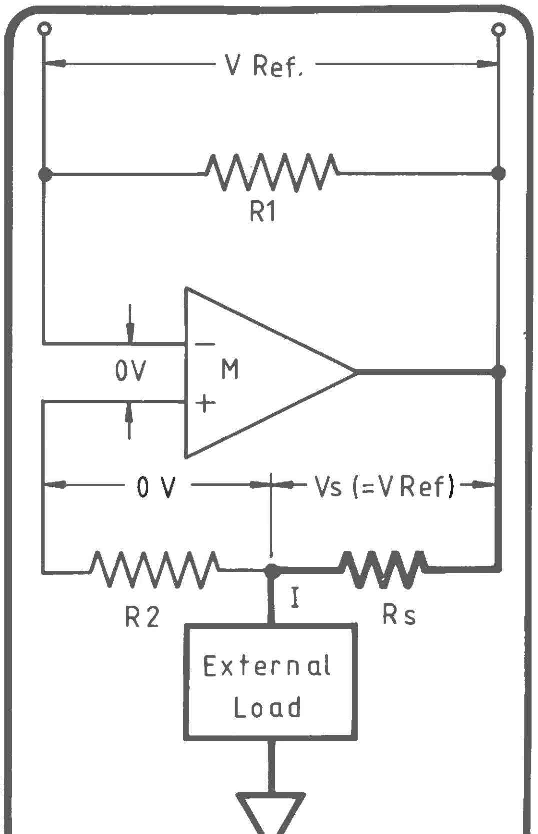


FIG. 4.34 BASIC VOLTAGE-TO-CURRENT CONVERTER

4.9.1 Basic Voltage-to-Current Converter

The basic arrangement is shown on Fig. 4.34. A variable reference voltage V_{REF} is developed across R1 between output and inverting input of the high-gain operational amplifier M. The non-inverting input is connected to the output via a resistor network, part or all of which is current-carrying. With both positive and negative feedback, the amplifier will force its differential input voltage to zero. It can only do this by adjusting the current in the current-carrying path until the full value of V_{REF} is developed across the path. (e.g. in Fig. 4.34 no current flows in R_2, so all of V_{REF} is developed across Rs). The values of V_{REF} and "shunt" Rs thus determine the value of current flowing in the external circuit. In the 4000, the values of Rs are switched to select the Range in use, and V_{REF} is adjusted to vary the output current within the selected Range.

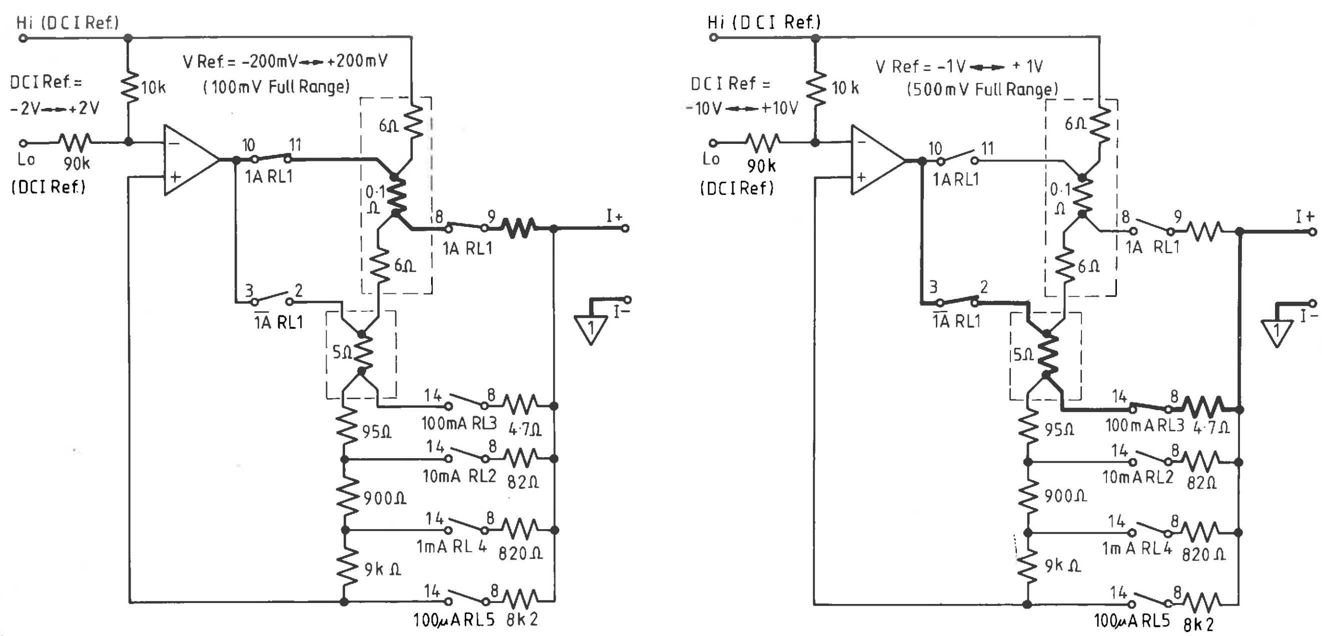
4.9.2 Range Selection

Fig. 4.35 shows two Range configurations of the voltage-to-current converter. In each case V_{REF} is 0.1 x DCI Ref. RL1 is a bistable latching relay, in which solenoid current is required only to change state (Two solenoids are incorporated, one for each state).

In the 4000, the voltage across the I+ and I− terminals is permitted to rise to 3V with full compliance. Each range incorporates a series resistive element connecting the range selection relay contact to the I+ terminal. These resistors enhance the stability of the circuit, with reactive loads.

4.9.2.1 1A Range (Refer to Fig. 4.35a)

The only current path available is through the 0.1Ω shunt. As V_{REF} is scaled to 100mV Full Range the current in the 0.1Ω shunt must be $\frac{100mV}{0.1\Omega}$ = 1A. The 0.1Ω shunt is made up of ten 1Ω precision resistors in parallel, mounted on a separate pcb assembly 400510. As the 0.1Ω shunt is a composite 4-wire parallel arrangement, each 1Ω precision resistor feeds its voltage to the joint sense lines through two summing networks of ten 61Ω resistors. As they carry no net current except when switching, they are represented on Fig. 4.35 as two 6Ω resistors.



(a) 1A Range (b) 100mA Range

FIG. 4.35 CURRENT RANGE CONFIGURATIONS

4.9.2.2 100mA, 10mA, 1mA and 100μA Ranges (Refer to Fig. 4.35b)

With RL1 contact 2 closed, and contacts 8, 11 open, Relays 3, 2, 4 and 5 select the 100mA, 10mA, 1mA and 100μA ranges respectively.

(1) 100mA Range: Fig. 4.35b is shown with 100mA Range selected. The 5Ω 100mA shunt is located on a heatsink on the I/Ω pcb assembly. DCI Ref is scaled in software for 5V Full Range, so that V_{REF} is 500mV FR. This voltage appears across the 5Ω shunt, to generate 100mA at Full Range in the I+ line.

(2) 10mA, 1mA and 100μA Ranges: The DCI Ref is scaled in software to 10V for each of these three full ranges, giving V_{REF} of 1V FR.

Each Full Range drive current is set by the resistance between the range relay contact and RL1 pin 2. These currents are listed below against the total shunt value:

100mAFR	=	500mVFR	across	5Ω
10mAFR	=	1 VFR	across	100Ω
1mAFR	=	1 VFR	across	1kΩ
100μAFR	=	1 VFR	across	10kΩ

4.9.3 Voltage-to-Current Conversion Amplifier (Circuit Diagram No. 430448 Sheet 1)

N.B. This amplifier is dual purpose AC/DC. In the 4000 it is used for DC only.

The Conversion Amplifier is driven by the DCI Ref input from the Reference Divider pcb. The value of DCI Ref determines the output current, and is scaled for range as described in Section 4.9.2. DC Ref I is coupled: Hi to the output, and Lo to the inverting input through the 10:1 divider R43/R44.

4.9.3.1 Voltage Preamplifier

M3, M4 and Q6 form a high-gain, chopper-stabilised voltage amplifier. The input offset of Q6 is trimmed by M3, itself a chopper-stabilised amplifier of high gain and approximately 10Hz bandwidth. Q6 provides additional bandwidth for rejection of HF common-mode noise. M4 contributes additional gain and drives the high current output stage through Q7. Additional frequency compensation is provided by C43/R81. The whole of the voltage pre-amplifier is bootstrapped by M7 and its associated circuitry to increase its input impedance and linearise its dynamic response. Extensive screening and filtering is employed to eliminate the effects of the chopping spikes at inputs and output of M3.

4.9.3.2 High Current Output Stage

The current output stages are located on the PS/I heatsink, current-limited by Q5/Q6. Q7 acts as a thermal detector on the heatsink to derive temperature compensation for the output stages, maintaining the quiescent current through Q1 and Q2.

The quiescent current acts to reduce the output resistance of Q1 and Q2, improving the linearity of the output current. This also suppresses any tendency for the drive from M4 to fluctuate for output currents around zero; as the drive voltage must slew through approx. 1.3V after switching one output device off, before the other is switched on.

The current shunts complete the feedback and output circuits as described in Sections 4.9.1 and 4.9.2, and the output current is fed to the I+ terminal via protection and output switching.

4.9.4 Output Protection

D14, D15, D18 and D19 are 5V, 5 Watt zeners. D14 and D15 limit the excursion of the power amplifier output voltage in the event of the circuit going "open-loop"; D18 and D19 place an absolute limit on the output voltage. The output compliance specification is valid only up to a maximum of 3V across the output terminals (Refer to User's Handbook for maximum load resistance values). Nevertheless, occasions may arise when a user overloads the circuit by attempting to drive current into an open circuit (e.g. by disconnecting from a load with Output On). In this case the two Zener diodes D18 and D19 protect the Amplifier power stages by limiting the output voltage to 5V. But before the voltage reaches 5V the overvoltage detection circuit generates $\overline{\text{LIM ST 1}}$ signal.

4.9.4.1 Guard Buffers

M1 guards out the leakage of the four high-power protection zener diodes in normal operation and protects against other leakage, by maintaining the guarding and screens around the output at the output potential.

In addition to its bootstrap function, M7 acts as a buffer for guards around the amplifier input, thus preventing any local common-mode disturbances from affecting the performance of the main amplifier.

4.9.4.2 Overvoltage Detection

The output guard buffer drives the overvoltage detection circuit. M15 divides the output voltage by two and acts as an inverting full-wave rectifier, to accommodate both positive and negative voltages. The voltage at M15-4 increases negatively as the terminal voltage increases positively or negatively. M15-6 is biassed to −2.2V, so M15-7 reverse-biasses D10 unless the terminal voltage exceeds ± 4.4V, when M15-7 will swing to the negative rail and pull the $\overline{\text{LIM ST1}}$ line to −15V (logic-0).

The CPU receives the $\overline{\text{LIM ST1}}$ signal via the serial datalink. When at logic-0, the message "Error OL" is presented on the MODE display and if 1A or 100mA range is selected, the 4000 Output is set off and DCI Ref voltage is set to zero, to limit the power developed as heat within the calibrator.

4.9.5 Current Switching Logic (Refer to Circuit Diagram No. 430448 Sheet 2)

The analogue control signals are transferred into guard on the Reference Divider pcb, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is employed: 0 = 15V, 1 = 0V for the signals entering the I/Ω pcb via J8 from the Mother pcb. The Ohms switching logic is described in Section 4.10.

M12 and M14 are Darlington open-collector Inverter/Drivers. The relay drive logic places a logic-1 (0V) on the input of selected drivers and logic-0 (−15V) on those not required. A selected driver operates its relay(s) by pulling its output voltage to −14V.

Whenever a switching command has been received the CPU performs a control-data transfer and the UPD (IG) line from J8-60 is pulsed to logic-0 for 50mS. Q1 is turned on, applying +15V to the relays connected to its collector (Current relays RL11, 12 and 1). The selected relays are thus energised by 30V but after the UPD (IG) pulse has ended they are held on by 10.5V between −3.5V at the cathode of D1 and −14V at the selected driver output. This method reduces the local heat generated by energised relay coils, in the relay contacts.

RL1 is a bistable latching relay with two operating solenoids. A logic-0 at pin 6 switches the 1 Amp range on, and at pin 1 switches it off. Normally both pins are floating on an open collector, so the relay remains latched in one bistable state with both solenoids de-energised. During the 50mS UPD (IG) pulse, M16-1 and M16-12 are enabled, allowing the 1 amp range switching-logic state to change RL1 over (if required) before the UPD (IG) pulse ends.

4.9.5.1 Range Switching Logic

Range control data is input as a 3-bit code on IRϕ, IR1 and IR2 lines. The bit-pattern is decoded to "1 of 8" by M6, to energise the correct relay(s) for the selected range. The resulting variants are listed in Table 4.2 against range selections. Note that RL5 (100µA range) is selected whenever the I function is deselected or if the watchdog has tripped and BARK signal is at logic-1.

4.9.5.2 Output Switching

The I FUNCT, BARK and OFF signals are decoded so that RL11 and RL12 are energised only when the 4000 I function has been selected, Output is ON and the watch-dog has not barked (i.e. RL11/12 energised if M12-7 = I• OFF• BARK).

Range	Bit Pattern			M6 output pins (pin 9 not connected)							Range Relays Energised						
	IR2	IR1	IRϕ	4	5	6	7	10	11	12	RL5	RL4	RL2	RL3	RL1 (6–7)	RL1 (1–12)	RL6
100µA	1	1	0					1			√					√	
1mA	1	0	1						1			√				√	
10mA	1	0	0							1			√			√	
100mA	0	1	1				1							√		√	
1A	0	1	0			1									√		
10A	0	0	1		1	External current option. When not fitted, software programs 1A range, from 10A and 100A selections										√	√
100A	0	0	0	1												√	√

Notes:
1. 1 = 0V, 0 = −15V
2. All M6 Output pins at 0 unless shown at 1
3. Unless shown energised on the table, all relays de-energised as in 430448 Sheet 1
4. One RL1 solenoid energised only during UPD (IG)
5. RL5 energised when I function deselected or if watchdog has BARKed

TABLE 4.2 CURRENT RANGE SWITCHING LOGIC SELECTIONS

4.10 RESISTANCE (Option 20) (Circuit Diagram No. 430448 Sheet 3)

Eight standard resistors are mounted on the I/Ω PCB Assembly (400448), each being 4-wire connected to the instrument terminals by range-selection relays.

4.10.1 4-Wire Connection Symmetry

For any given resistor, the connections on the Hi side are made through contacts of the same relays used for the Lo side. The range relays are two-way and their connections ensure that in the sense (Hi-Lo) loop, all thermal contact voltages on the Hi side of any resistor are backed off by those on the Lo side. This symmetrical, 4-wire arrangement transfers the stability and accuracy of each resistor to the front (or rear) panel terminals.

4.10.2 4-wire Junctions and Pre-set Trimming

R63-72 are 4-wire resistors, so for 1Ω – 10KΩ selections the 4-wire junction is at the standard resistor itself. These resistors are parallel-trimmed.

R62, R74 and R73 are two-wire resistors. For these higher resistance values, 100KΩ, 1MΩ and 10MΩ, series trimming is employed and the 4-wire junctions enclose the series chain.

Trimming resistors are selected and adjusted in the factory, under carefully-controlled environmental conditions, against traceable standards.

4.10.3 Methods of Calibration

Although each RANGE key is labelled with the nominal value, it is the calibrated value of each standard resistor which is presented on the OUTPUT display when selected. Routine recalibration consists of accurately measuring the resistor value and setting the display to that value without removing the instrument covers (Refer to Section 1.2.10). For many users, the main criterion is that the actual value is known, whereas exact alignment to the nominal is unimportant.

"Error 6" is displayed if the value entered by the user during calibration is outside the resistor's tolerance (Section 1.2) i.e. outside the calibration memory span. Under normal use the resistor drift is well within the tolerance, so "Error 6" appears only if the user enters an erroneous value.

If the resistor has been subjected to undue stress, it is possible that its value may have changed slightly, and be outside its tolerance. If it is less than approx. 50ppm outside tolerance an internal trimmer can be adjusted, and the value can be calibrated.

A stressed resistor may have been damaged if its value is greater than 50ppm outside its tolerance. It is advisable to have such a resistor tested or replaced by an agent of Datron Instruments.

Follow the procedure detailed in Section 1.5 to adjust the resistor value. If this is unsuccessful contact your Datron Instruments Service Centre.

4.10.4 Two-wire Connections

To avoid the intrusion of extra thermal voltages, no switching is employed for selection of 2-wire connections. Users are recommended to connect only to the Hi/Lo terminals, so the 2-wire mode should be recalibrated at these terminals.

4.10.5 4-wire/2-wire Display Values

When the 4000 is in Ω function, selection of Remote Sense mode (Key LED lit) displays the calibrated value for the 4-wire connection, but with the Remote Sense LED unlit, the 2-wire value is displayed.

4.10.6 Ohms Zero

With the 4000 in Ω function, pressing the zero key on the front panel energises relay RL10. This provides a true 4-wire short, the existing range remaining selected.

If Remote Sense LED is lit, the displayed value is zero and cannot be calibrated; but if unlit, the displayed value may be adjusted to the measured value as a calibrated 2-wire zero.

4.10.7 Output Connections-Function switching

The front terminal connections are routed via the I/Ω pcb, and it is there that they are switched between functions. With RL14 and RL19 de-energised as shown in Circuit Diagram No. 430448 Sheet 3, the DC Voltage Power and Sense connections to the DC pcb are routed Out to the I+, I−, Hi and Lo terminals.

NB If Option 20 is not fitted, the I/Ω Link pcb is fitted in its place to make direct connection from the DC Voltage output to the terminals (Refer to Section 3 Fig. 3.2)

4.10.8 Resistance Switching Logic (Refer to Circuit Diagram No. 430448 Sheet 2)

The analogue control signals are transferred into guard on the Reference Divider pcb, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is employed: 0 = −15V, 1 = 0V for the signals entering the I/Ω pcb via J8 from the Mother pcb. The Current switching logic is described in Section 4.9.

M13 and M14 are Darlington open-collector Inverter/Drivers. The relay drive logic places a logic-1 (0V) on the input of selected drivers and logic-0 (−15V) on those not required. A selected driver operates its relay(s) by pulling its output voltage to −14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD (IG)}}$ line from J8-60 is pulsed to logic-0 for 50mS. Q1 is turned on, applying +15V to the Ω relays, which are connected to its collector. The selected relays are thus energised by 30V but after the $\overline{\text{UPD (IG)}}$ pulse has ended they are held on by 10.5V between −3.5V at DC cathode and −14V at the selected driver output. This method reduces the local heat generated by energised relay coils, in the relay contacts.

When DC (Voltage) is not selected, the connections from the DC pcb are isolated by open contacts of RL13 and RL14 on the DC pcb. (Circuit Diagram No. 430445 Sheet 3).

The output connections from the Current section of the I/Ω pcb are linked directly to the I+ and I− terminals, but if I is not selected, Relays RL11 and RL12 are de-energised, isolating the Current output Hi and Lo from the common lines to the I+ and I− terminals. (Circuit Diagram No. 430448 Sheet 1).

When Ω is selected, relays RL14 and RL19 are energised, breaking the circuit to DC pcb Power and Sense, and connecting the four lines from the selected standard resistor to the I+, I−, Hi and Lo terminals. (Circuit Diagram No. 430448 Sheet 3).

4.10.8.1 Range Switching Logic

Range control data is input as a 3-bit code on ΩRϕ, ΩR1 and ΩR2 lines. The bit-pattern is decoded by M10/M18/M19 to energise the correct relay(s) for the selected range. The resulting variants are listed in Table 4.3 against range selections. Note that unless Ω function is selected M11 is disabled so that the hardware defaults to the 1Ω range, with no range relays energised. The same default condition occurs when Ω is selected, but the watchdog has BARKed.

Range	Bit Pattern			Relay Drive Signals							Range Relays Energised							Ω Zero Relay
				M18 pins				M19 pins										
	ΩR2	ΩR1	ΩRϕ	2/13	3/6	4	11	3/8	10	11	RL13	RL9	RL15	RL8	RL17	RL18	RL16	RL10
Zero	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	√
1Ω	0	0	0															
10Ω	0	1	0							1							√	
100Ω	0	1	0					1							√			
1KΩ	0	1	1					1	1						√	√		
10KΩ	1	0	0	1							√							
100KΩ	1	0	1	1			1				√			√				
1MΩ	1	1	0	1							√	√						
10MΩ	1	1	1	1	1	1					√	√	√					

Notes: 1. 1 = 0V, 0 = −15V.

2. All Relay Drive Signals at 0 unless shown at 1. X = 0 or 1

3. Unless shown energised on the table, all relays de-energised as in 430448 Sheet 3. X = 0 or 1

4. 1Ω range is Hardware default condition so all range relays de-energised.

5. Range Selections enabled by Ω FUNCT and $\overline{\text{BARK}}$ at the inputs of M11.

TABLE 4.3 RESISTANCE RANGE SWITCHING LOGIC SELECTIONS

4.10.8.2 Ω Output Switching

The $\overline{\Omega\ \text{FUNCT}}$, BARK and OFF signals are decoded so that RL14 and RL19 are energised only when the 4000 Ω function has been selected, Output is ON and the watchdog has not barked (i.e. RL14/19 energised if M13-7 = Ω•$\overline{\text{OFF}}$• $\overline{\text{BARK}}$).

4.10.8.3 Ω Zero

The $\overline{\Omega\ \text{FUNCT}}$, BARK and Ω ZERO signals are decoded so that RL10 is energised only when the 4000 Ω function has been selected, the Zero Key has been pressed and the watchdog has not barked (i.e. RL10 is energised if M13-2 = Ω • ZERO• $\overline{\text{BARK}}$)

4.11 POWER SUPPLIES

The circuits described in this section perform the following functions:

(1) Line power switching, fusing, filtering, voltage selection and transformation.

(2) Main digital supply generation and distribution (Outguard)

(3) Display high voltage supply generation.

(4) In-guard stabilized supply generation for Common-2, Common-3 and Common-4 circuitry.

A simplified power distribution block diagram appears at Fig. 4.36.

The power input module is mounted on the rear panel. The line transformer is located in the rear section of the instrument, close to the In-guard and Out-guard Power Supply PCB Assemblies. (For details of location and attachment, refer to Section 3, Fig. 3.3).

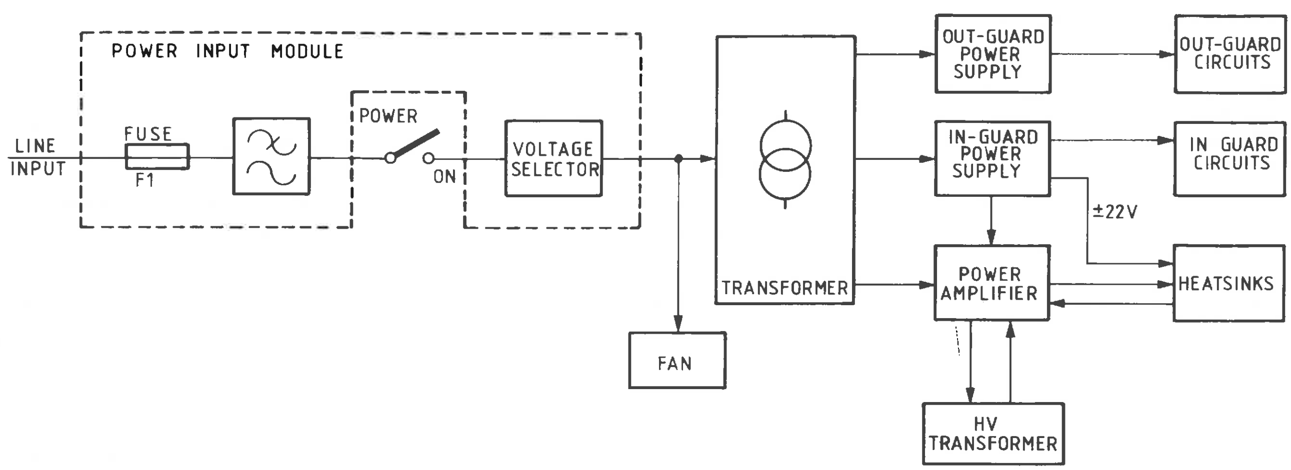


FIG. 4.36 POWER DISTRIBUTION BLOCK DIAGRAM

4.11.1 Line Power Distribution (Fig. 4.36 and Circuit Diagram No. 430439)

The single phase line supply enters the 4000 via a 3-pole input cable at the rear of the instrument. The cable connector plugs into a power input module (Circuit Diagram No. 430439) which contains a fuse, filter and line voltage selector pcb. (For details of fuse values and operating voltage selection, refer to the User's Handbook, Section 2). Both "line" and "neutral" rails are filtered by a low-pass LC network before being fed through the instrument to the two-pole "Power" switch on the front panel.

The switched supply is fed back to the power input module voltage selector pcb which configures the line transformer primary circuit as determined by the user. Power for the air circulation fan is provided directly from the power input module.

All line transformer secondaries are electrostatically decoupled from the primaries by a ground screen between the windings. The secondaries which supply the Common-2, Common-3 and Common-4 in-guard circuits are decoupled by an additional internal screen which is connected to the instrument guard.

4.11.2 Out-Guard Power Supplies (Circuit Diagram No. 430470)

4.11.2.1 Digital Main Supply

This circuit provides:

(1) +8V unregulated supply for use in the Front and Digital PCB Assemblies

(2) +5V regulated supply for out-guard digital circuits

4.11.2.2 +8V Unregulated Supply

This is taken directly from full-wave rectifier D1, D2 via fuse F1 (rated at 4A).

4.11.2.3 +5V Regulated Supply

The output voltage is controlled by series regulator Q5, Q6. Load current is sensed by R1 in the base-emitter circuit of Q1, which increases the conduction of Q5 and Q6 parallel combination for increases of load current. The 2.45 Zener D4 provides the reference voltage for comparators M1 at M1-3. The output voltage is sensed between the +5V and DIG common rails on the Mother PCB Assembly, and divided down to reference potential at M1-2. R8 and R9 ensure that regulation persists even if the sense links are disconnected.

M1 output drives Q2 whose collector voltage controls Q5 and Q6 conduction. If the +5V rail voltage falls due to loading, Q2 collector voltage rises, increasing Q5 and Q6 conduction to restore the rail voltage. Zener D5 prevents the positive excursion of the +5V rail in the event of regulation breakdown, and Zener D3 provides current limiting by restricting positive excursions of Q2 base voltage, and thus limiting the drive to Q5 and Q6. C9 and C10 provide a controlled fast response to reduce the effects of voltage transients on the +5V rail.

PTC thermistor R7 protects the power supply from high ground-leakage currents, notably in the external circuits of the IEEE 488 bus system. R7 presents a minimum of 80Ω between the digital common line and ground; this resistance increasing with increasing current.

4.11.2.4 – 180V Display Supply

180 Volts are required to operate the plasma digital displays on the Front PCB Assembly. Because the display anode drivers are powered from the Digital Main Supply +5V rail, the 180V positive pole is referred to this rail in the power supply. The display cathode is therefore at a potential of –175V. (Refer to Section 4.4 for further details).

Series regulation is provided by D6, R16 and Q3, and shunt regulation by D7 and Q4. A supplementary +5V supply is fed out to the Front PCB Assembly from J4-21. This is available to power the LEDs in the front panel keys, but is not used on the 4000.

4.11.2.5 Common Mode Null

This circuit provides a line-hum cancelling (bucking) output to the instrument guard network. (For details of adjustment refer to Section 5.7).

4.11.3 In-guard Power Supplies (Circuit Diagram No. 430451)

4.11.3.1 In-guard Common-2 Supplies

Stabilized supplies for the Common-2 circuits are provided by five integrated-circuit regulators as follows:

+15V from M2, protected at 2A by fuse F3;

+8V from M4, driven from M2 +15V output;

–15V from M1, protected at 2A by fuse F4;

–8V from M3, driven from M1 –15V output;

–10V from M6, driven from M1 –15V output.

Chokes L4, L5 and L6 in the supply lines from the line transformer secondary windings attenuate high frequency transients on the ac input.

4.11.3.2 Current Option Supply

This provides +22V and –22V unregulated power outputs to the Power Supply/I Heatsink assembly. Both supplies are protected at 4A by fuses F1/F2. High frequency filtering of the ac inputs is provided by chokes L1, L2 and L3. The ± 22V common return is maintained near to the common-2 return by resistor R1.

4.11.3.3 Reference Divider Common-4 Supplies

This circuit provides +36V, +18V and –15V regulated outputs to the reference divider in-guard circuits. The +36V supply is also used to power the +20V Master Reference.

Two secondary windings of the line transformer are used and inter-supply transients are reduced by the special coupling arrangements of common mode choke L10. The rectified output from bridge W4 is series regulated by Q4 with load current sensed by R3, Q2. Stabilization of the +36V output is performed by the feedback loop M5, Q1. A tendency for the output voltage to fall with an increased power demand will cause M5 non-inverting input to fall with-respect-to the 2.45V reference voltage at M5 inverting input. The corresponding fall at M5 output reduces the current flow through Q1 thus taking Q4 base potential more positive and increasing the output power. The output current is limited by the action of Q2 which conducts when R3 current is approximately 180mA. This additional drain from constant current source Q3 reduces the current through Q1 and therefore limits the load current through Q4. Zener diode D5 provides base/emitter bias for Q1.

The 36V output is dropped across Zener D6 to provide 18V (nominal) to the reference divider pcb where further regulation takes place.

The –15V supply is provided via bridge W3 and regulator M7.

4.11.3.4 In-guard Common-3 Supplies

The dc outputs from bridge W2 are regulated by integrated circuits M9 and M8 to produce +8V and –8V outputs respectively for the DC pcb assembly.

SECTION 5

SERVICING AND INTERNAL ADJUSTMENTS

WARNING HAZARDOUS ELECTRICAL POTENTIALS

ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.

ELECTRIC SHOCK CAN KILL!

CAUTION The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

5.1 INTRODUCTION

This section provides procedures for maintenance operations which require removal of covers or partial dismantling. The operations fall into three categories, as described in Table 5.1 below.

Category A	Servicing Required	Time Interval	Procedure	Calibration Required	Calibration Procedure
Routine Servicing	Clean the Air Intake Filter	1 year (or less in adverse conditions)	Section 5.2	No	–
	Change the Lithium Battery (non-volatile calibration memory)	5 years	Section 5.3	(a) Full pre-cal THEN (b) Full routine recalibration	Section 1.4 Section 1.2

Category B	Indication	Adjustment Required	Procedure	Calibration Required	Calibration Procedure
Ω Function Standard Resistor value adjustment	"Error 6" during Routine Recalibration	Re-set internal trimmers	Section 5.4	Routine Recalibration 4-wire and 2-wire Resistance only	Section 1.2

Category C[1]	PCB Assembly	Adjustments	Procedure Section 5	Calibration required: Pre-cal (Sect. 1.4)	Calibration required: Routine Recalibration (Section 1.2)
Adjustment following replacement of PCBs	Digital	–	–	Full	Full
	Reference Divider	–	–	Full	Full
	DC	–	–	–	DC (all ranges)
	I/Ω pcb	I Quiescent current	5.5	–	I and Ω (all ranges) only
	Power Amp (dc)	PA Quiescent current bucking null	5.6 5.7	–	–
	Power Supply (Out-guard)	bucking null	5.7	–	–
	Positive / Negative Heatsink	P.A. Quiescent current	5.6	–	–
	Power Supply/I Heatsink	I Quiescent current	5.5	–	–
	Line Transformer	bucking null	5.7	–	– –

Note [1] When an internal assembly is replaced, carry out the relevant adjustments before finally re-assembling the instrument.

TABLE 5.1 CATEGORIES OF SERVICING AND INTERNAL ADJUSTMENTS

CAUTION After any maintenance operations which include removal of top or bottom ground/guard assembly, carry out the Full Self-Test sequence (Section 2.3) before returning to normal use.

5.2 CLEANING THE AIR INTAKE FILTER (REFER TO SECTION 3.14, FIG. 3.8) DATRON PART NO. 450277-1

5.2.1 Servicing Frequency

The filter should be cleaned at intervals no greater than one year. In dusty conditions the frequency should be increased.

5.2.2. Removal (Fig. 3.8)

(a) Remove the four M3 x 10mm pozi-countersunk screws (11) which retain the filter grille (12)

(b) Remove the filter grille and reticulated foam filter.

5.2.3 Cleaning

(a) Wash the foam filter in a dilute solution of household detergent (hand-hot). Rinse thoroughly in clean hand-hot water and dry completely, without using excessive heat.

(b) Clean the grille, and the grille holes in the rear panel. (Use a vacuum cleaner and soft brush on the rear panel).

5.2.4 Inspection

Examine the foam filter for wear, replacing if links are broken.

5.2.5 Reassembly

Place the filter in the grille housing and secure the grille to the rear panel using the screws removed in 5.2.2 above.

5.3 LITHIUM BATTERY (DATRON PART NO. 920101)

This procedure is to be performed at intervals of 5 years from new.

CAUTION The **full** Pre-cal and Routine Recalibration Procedures (Section 1.4 and 1.2) **must** follow the fitting of a new battery, before the instrument specification can be realised, as calibration data will be corrupted. It is therefore recommended that the battery be replaced immediately prior to a scheduled full recalibration.

5.3.1 Procedure

(a) Ensure that power OFF is selected.

(b) Remove the top cover (Section 3.2.1) and top ground/guard assembly (Section 3.4.1)

(c) Remove the digital pcb assembly from the chassis (Section 3.6.1)

CAUTION Do not place the digital pcb on any conducting surface.

(d) Remove battery as follows (Refer to Fig. 5.1)

(1) Push sleeve (4) back along the red wire to expose the solder joint.

(2) Unsolder red wire (3) from positive terminal of the battery (5)

(3) Unsolder the negative terminal of the battery (5) from resistor R60 at the wrap-joint

(4) Remove battery (5) from battery clip (2)

(e) Fit a new battery, reversing the procedure of step (d)

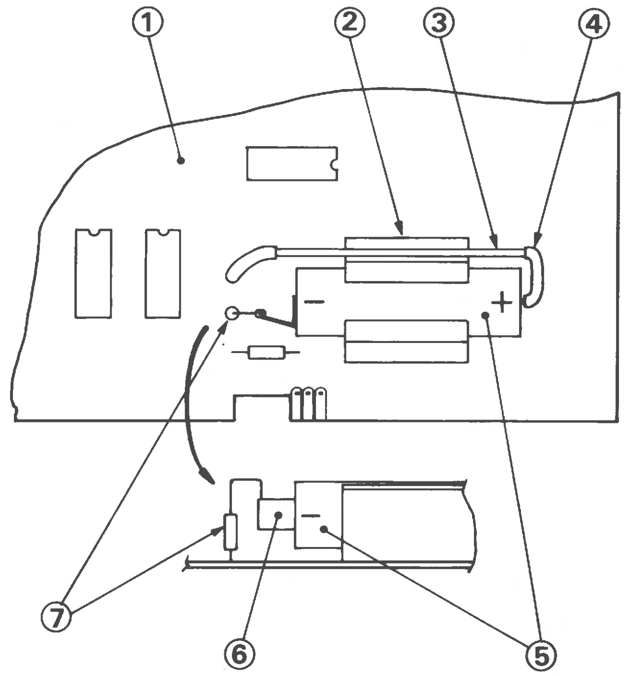
(f) Refit the digital pcb assembly into the chassis (Section 3.6.2)

(g) Refit the top ground/guard assembly to the instrument (Section 3.4.2)

(h) Refit the top cover (Section 3.2.2)

NB The top cover will need to be removed again for Pre-calibration.

5.3.2 Carry out full Pre-calibration then full Routine Calibration in accordance with Section 1.4 and 1.2 respectively.



1. DIGITAL PCB ASSEMBLY
2. BATTERY CLIP
3. RED WIRE
4. SLEEVE
5. BATTERY
6. NEGATIVE BATTERY TERMINAL WRAPPED AROUND WIRE FROM RESISTOR R60
7. RESISTOR R60

FIG. 5.1 DIGITAL PCB BATTERY REPLACEMENT

5.4 Ω FUNCTION – STANDARD RESISTOR ADJUSTMENT

5.4.1 Introduction

Routine adjustment of the standard resistors used in Ω function is not required. A resistor is calibrated by the user entering its measured value into a non-volatile calibration memory. This value is subsequently recalled and displayed to the user each time the resistor is selected.

5.4.2 "Error 6" Message

"Error 6" is displayed if the value entered by the user during calibration is outside the resistor's tolerance (Section 1.2) i.e. outside the calibration memory span. Under normal use the resistor drift is well within the tolerance, so "Error 6" appears only if the user enters an erroneous value.

5.4.3 Undue Resistor Stress

If the resistor has been subjected to undue stress, it is possible that its value may have changed slightly, and be outside its tolerance. If it is less than approx. 50ppm outside tolerance an internal trimmer can be adjusted, and the value can be calibrated.

5.4.4 Possible Damage

A stressed resistor may have been damaged if its value is greater than 50ppm outside its tolerance. It is advisable to have such a resistor tested or replaced by an agent of Datron Instruments.

5.4.5 To Reset Internal Trimmers

Follow the procedure detailed in Section 1.5 to adjust the resistor value. If this is unsuccessful contact your Datron Instruments agent.

5.5 I/Ω PCB – I FUNCTION QUIESCENT CURRENT ADJUSTMENT

Replacement I/Ω assemblies are set up by the manufacturer to ensure correct operation. The final adjustment of the quiescent current in the power stage of the Voltage-to-Current converter is delayed until the pcb is installed in the user's instrument. For this procedure, a 0.1Ω resistor is inserted in series with each 22V supply line to the power stage (Located in the Power Supply/I Heatsink assembly). The quiescent current is set to 10mA by adjusting the voltage across one of the resistors to 1mV using R23 on the I/Ω assembly.

5.5.1 Test Equipment Required

(1) Digital Voltmeter (Datron Instruments model 1071)

(2) Two 2.5 watt resistors, 0.1Ω, ± 10%, Wire Wound. (Welwyn W21 or equivalent),

5.5.2 Initial Conditions

4000 Power OFF
Top cover removed (Section 3.2.1)
Top ground/Guard assembly removed (Section 3.4.1)
Replacement I/Ω pcb assembly not yet fitted into J8 (mother pcb)

5.5.3 Procedure (Refer to Layout Drawing No. 400448 and Circuit Diagram No. 430448)

(a) Before fitting the I/Ω pcb assembly, ensure that R23 is set fully counter-clockwise.

(b) Fit the I/Ω pcb assembly (Section 3.6.2)

(c) Break the 22V supply connections to the Voltage-to-current converter power stage by removing connector J1 from the In-guard power supply pcb.

(d) Re-make each 22V supply connection from its female pin on the freed J1 connector to its corresponding male pin on the In-guard P.S. pcb, using one 0.1Ω resistor in series with each supply line (Red and Brown wires)

(e) Connect the digital voltmeter across one of the 0.1Ω resistors fitted in step (d)

(f) Set 4000 power ON

(g) Ensure 10V range selected with Output OFF

CAUTION In the following step (h), use a thin insulated screwdriver.

(h) Carefully adjust R23 on I/Ω pcb assembly for a digital voltmeter reading of 1mV±50μV (equivalent to 10mA through 0.1Ω resistor).

(j) Switch 4000 Power OFF

(k) Disconnect and remove both 0.1Ω resistors and the digital voltmeter from J1. Reconnect J1 to the In-guard Power Supply pcb pins.

5.5.4 Return to Use

(a) Refit top ground/guard assembly (Section 3.4.2) and Top cover (3.2.2)

(b) Carry out Routine Calibration of current and resistance in accordance with Section 1.2.7.3 and 1.2.7.4.

5.6 POWER AMPLIFIER (DC) PCB – PA QUIESCENT CURRENT ADJUSTMENT

Replacement PA (dc) assemblies are set up by the manufacturer to ensure correct operation. The final adjustment in the PA power stage quiescent current must be carried out when installed in the user's instrument. For this procedure, the quiescent current is set to 20 mA by adjusting the voltage between TP5 and TP13 to 6mV

5.6.1 Test Equipment Required

Digital Voltmeter (Datron Instruments model 1071)

5.6.2 Initial Conditions

4000 Power OFF
Top cover removed (Section 3.2.1)
Top ground/guard assembly removed (Section 3.4.1)
Replacement Power Amplifier assembly already fitted into J9 (Mother pcb), and connectors J1, J2, J3, J4, J5 and J6 already connected (Section 3, Fig. 3.6)

5.6.3 Procedure

(a) Connect the digital voltmeter between TP5 and TP13 on Power Amplifier (dc) pcb assembly

(b) Set 4000 power ON. Ensure that Output is OFF and DC selected

(c) Select 100V Range

(d) Adjust R82 on Power Amp (dc) Assembly for a reading of 6mV ± 100μV

(e) Set 4000 power OFF and disconnect the digital voltmeter

5.6.4 Return to Use

(a) Ensure that all internal assemblies are correctly fitted and connected (Section 3)

(b) Refit Top ground/guard assembly (Section 3.4.2)

(c) Refit Top cover (Section 3.2.2)

(d) Recalibration is not required after replacing a Power Amp (dc), pcb, but the dc voltage specification may be verified (if desired) in accordance with the User's Handbook, Section 7.

5.7 BUCKING CIRCUIT NULL ADJUSTMENT

After replacing the Power Amplifier (dc), the Power Supply (Outguard) or the Line Transformer, it is necessary to ensure that line-frequency breakthrough on the Lo and Guard terminals is reduced to minimum. In these procedures, R12 on the Out-guard Power Supply Assembly is adjusted to minimise the voltage between Lo and Ground, and R1 on the Power Amplifier (dc) Assembly is adjusted to minimise between Guard and Ground.

5.7.1 Test Equipment required

Oscilloscope (with AC input and sensitivity to 100mV/div.)

5.7.2 Initial Conditions

Power OFF
Top and Bottom ground/guard assemblies fitted and secured (Section 3.4.2 and 3.5.2)
Top cover removed (Section 3.2.1)

5.7.3 Procedure

(a) Set 4000 Power ON

(b) Ensure that DC 10V Range selected with Output OFF

(c) Ensure that Ouput display is 0.000,000V

(d) Connect oscilloscope AC input between 4000 ⏚ (Ground) and Lo Terminals

(e) Locate R12 on the Out-guard Power Supply pcb through the hole in the Top ground/guard assembly (refer to Layout Drawing No. 400470)

(f) Select Output ON +

(g) Adjust oscilloscope controls to obtain a line-frequency wave-form

(h) Without touching the Top ground/guard assembly, adjust R12 for minimum wave-form amplitude. This should not exceed 1V peak-to-peak

(j) Select Remote Guard, transfer the oscilloscope AC input connection from Lo to Guard terminal and obtain a line-frequence waveform.

(k) Locate R1 on the Power Amplifier (dc) pcb through the hole in the Top ground/guard assembly (refer to Layout Drawing No. 400449)

(l) Without touching the Top ground/guard assembly, adjust R1 for minimum waveform amplitude.

(m) Select Power OFF

(n) Disconnect the oscilloscope

5.7.4 Return to Use

(a) Refit Top cover (Section 3.2.2)

(b) Recalibration is not required after this adjustment.

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	400438	REAR PANEL ASSY			1
	400440	MOTHER PCB ASSY			1
	400441	FRONT PCB ASSY			1
	400454	PA (POS) HEATSINK ASSY			1
	400455	PS/I HEATSINK ASSY			1
	400456	MAINS TRANSFORMER ASSY.			1
	400457	MF TRANSFORMER ASSY.			1
	400461	PA (NEG) HEATSINK ASSY.			1
	400462	MAINS SWITCH CABLE ASSY.			1
	400463	DIGITAL PS CABLE ASSY.			1
	400464	FRONT O/P CABLE ASSY.			2
	400469	IN GUARD POWER SUPPLY CABLE ASSY			1
	400471	16 WAY RIBBON CABLE ASSY.			2
	450290-1	GUARD SHEET			2
	450291-1	EARTH SHEET			2
	450292-1	EARTH/GUARD SPACER			8
	450293-1	PCB RETAINING BAR			3.
	450265-1	MOULDED CHASSIS	HALLAMS		1
	450270-1	PCB GUARD SCREEN	GOULD ADVANCE		7
	450271-1	FILTER GRILLE	" "		1
	450272-1	TRANSFORMER BOLT PLATE	" "		4
	450275-1	MAINS TRANSFORMER PLATE	" "		1

NOTES.

SEE SHEET 7 FOR LATEST ISSUE

ISS.	A	1	2	3	4	5	6	7
E.C.O.	—	RELEASED	1333.1336 1345.1348	1363. 1377	1399, 1406	1438	1467	1480
DATE	2-10-81	23-3-82	6.7.82	23.8.83	26-11-82	16-2-83	11-4-83	6.6.83
CHKD.								

DATE 2nd OCT 81 | DRAWN B. JACKSON | CHECKED | APPROVED | DATE 16.9.82

datron ELECTRONICS LTD

TITLE 4000/4000A CHASSIS ASSEMBLY

DRAWING NUMBER 400437 400437A | SHEET 9 OF 12

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	450277-1	FOAM FILTER			1
	450278-1	HEATSINK RETAINER			1
	450280-1	HANDLE, PIVOT PINS & BLOCKS			2
	450300-1	REAR SPACER	GOULD ADVANCE		2
	450301-1	EARTH BRACKET	" "		1
	450310-1	R.H. SIDE EXTRUSION	" "		1
	450311-1	L.H. SIDE EXTRUSION	" "		1
	450315-1	HEATSINK GUARD SCREEN	" "		1
	450316-1	POWER SUPPLY GUARD SCREEN	" "		1
	SEE TABLE	CALIBRATOR OVERLAY			1
	450320-3	FRONT PANEL.	GOULD ADVANCE		1
	450321-1	GUARD CONTACT PLATE	" "		1
	450323-1	CABLE BRIDGE	GOULD ADVANCE		1
	450367-1	POLAROID			2
	521006	16/0.2 PVC INSULATED 1KV GREEN/YELLOW WIRE.			840 mm
	510999	7/0.2 " " " WHITE WIRE			410 mm
	590006	HEATSHRINK SLEEVE φ2.4 INT	RS OR HELLERMANN ELECTRIC	399-495 OR LVR 24	120 mm
	590032	HEATSHRINK SLEEVE φ4.8 INT	" OR " "	399-518 OR LVR 48	15 mm
	590013	TY-RAP. CABLE TIE.	PANDUIT	PLT 1.5L	1

NOTES.

INSTRUMENT	CHASSIS ASSY	OVERLAY
4000	400437	450319/A-4
4000A	400437A	450319/E-1

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DRAWING NUMBER 400437 400437A | SHEET 10 OF 12

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	611004	SCREW M3x6mm STEEL POZI-PAN ZINC PLATED. GKN.			32
	611015	SCREW M3X8mm STEEL POZI-CSK. ZINC PLATED. GKN.			2
	611016	SCREW M3X8mm STEEL POZI-PAN. ZINC PLATED. GKN.			11
	611023	SCREW M2·5X10mm STEEL POZI-PAN. ZINC PLATED. GKN.			2
	611046	SCREW M8 X 100mm STEEL HEX HEAD.			4
	611047	SCREW M5X12mm STEEL POZI-CSK. ZINC PLATED. GKN.			8
	611048	SCREW M4X8mm TAPTITE POZI-CSK. ZINC PLATED. BLACK GKN.			8
	611024	SCREW M5x8mm STEEL POZI-PAN ZINC PLATED. GKN.			2
	611012	SCREW M3X 12mm STEEL POZI-CSK. ZINC PLATED GKN.			6
	611038	SCREW M4X 12mm H.T.STEEL SKT HD CSK.			6
	611051	SCREW M8 X 110mm STEEL HEX HEAD.			4
	613005	WASHER M3 INT/SHAKEPROOF STEEL. GKN DISTRIBUTORS			20
	613009	SOLDER TAG 4BA TINNED BRASS. R.S.			6
	613012	WASHER M2·5 FLAT STEEL. GKN DISTRIBUTORS.			4
	613014	WASHER M2·5 INT/SHAKEPROOF STEEL. GKN DISTRIBUTORS.			2
	613028	WASHER M5 INT/SHAKEPROOF	GKN DISTRIBUTORS.		2
	613025.	WASHER M8 FLAT STEEL.	GKN DISTRIBUTORS.		12
	613024	SOLDER TAG M4.	FARNELL.	101·479	1
	613029	WASHER M3 WAVEY	LEWIS SPRING	LS 508/54	25
	614008	SPACER 75mmLG x 10·7OD x 8·5ID.	SPIROL	8·0 X 75 STD-FT	4
	615002	NUT M3 FULL HEX STEEL. ZINC PLATED			3
	615015	NUT M8 FULL HEX STEEL 'NYLOCK'.			8
	611008	SCREW M3X10mm STEEL POZI-CSK ZINC PLATED GKN			4

NOTES.

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J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	606005	DIL SOCKET CLIP	CA	CA16-200-DL	2
	613007	WASHER M3 FLAT STEEL.	GKN. DISTRIB		7
	613031	5/16" SPECIAL SOLDER TAG	ROSS COURTNEY	TAG No 201011	1
	630004	'P' CLIPS ϕ 1/4"	RICHCO OR SES	N4 OR CN6	3
	630029	TAPE DOUBLE SIDED 1/4" x 1/32"	3M	4032	204 mm
	630167	FOAM TAPE 6mm T x 7mm W	TESA	TESAMOLL 761/4763	375 mm
	630168	POLYESTER TAPE 50mm WIDE	3M	683	200 mm
	630020	CABLE CLIP	3M	708	1
	630003	'P' CLIP ϕ 3/16"	RICHCO OR SES	N3 OR CN5	4
	630162	FOAM TAPE 12mm x 12mm	TESA	TESAMOLL 761/4766	1080 mm
	900009	LOCKING COMPOUND	LOCTITE	270	A/R
	920122	TERMINAL COPPER BLACK	DATRON	SEE DRG	1
	920123	TERMINAL COPPER RED/BLK	DATRON	SEE DRG	1
	920134	TERMINAL COPPER BRN/BLK	DATRON	SEE DRG	1
	920135	TERMINAL COPPER BLU/BLK	DATRON	SEE DRG	1
	920136	TERMINAL BRASS WHT/BLK	DATRON	SEE DRG	1
	920137	TERMINAL BRASS GRN/BLK	DATRON	SEE DRG	1

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J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	410167-3	PCB			1
	450296-1	EARTH SCREEN			1
C1	101103	10nF 25% 250V CER DISC	ITT	CD10.	1
J3-J8	604033	4 CCT POLARISING WAFER	MOLEX	22-29-2041 GOLD	12
J1, J2	605002	16 WAY DIL SOCKET	CA	CA-16S-10SD	2
J27	605086	24 WAY PCB MNT RECEPTACLE	AMPHENOL	57-20240-8	1
	611004	M3X6 POZIPAN SCREW	GKN	ZINC PLATED	2
	612004	M3X4 STANDOFF 1/16" PCB	HARWIN	CS 2116-B	2
	612008	M3X6 STANDOFF 1/16" PCB	CAMBION	350-5138-09-07	2
	613029	M3 CRINKLE WASHER			2
S1	700046	SWITCH 6 POSN D.I.L S.P.S.T	AMP. OR CONTRAVES	435166-4 OR DSS-6	1
	700047	SWITCH COVER	AMP	435238-3	1
S2	700080	SP3P SLIDE P.C.B MNT	ALCO	SLS-131-PC	1
S53	700081	SPDT SLIDE P.C.B MNT	ALCO	SLS-121-PC	1
	614003	STANDOFF 3-3 CLEAR X 6mm BRASS	HARWIN	CS 2117-A	2
	900004	SILICONE RUBBER COMPOUND	RS.	544-311	A/R

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	B	1	2
E.C.O.	—	RELEASED	1466
DATE	5-8-81	29-3-82	11-4-83
CHKD.	—	MD	MD

DATE 27. 7. 81	datron ELECTRONICS LTD
DRAWN JK	TITLE 4000 INTERCONNECTION P.C.B ASSY
CHECKED B. JACKSON	
APPROVED B Hame	DRAWING NUMBER 400439
DATE 27th AUG 81	SHEET 2 OF 2

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	008035	33R 5% 2½W. WIREWOUND	WELWYN	W21	2
R2	008035	33R 5% 2½W. WIREWOUND	WELWYN	W21	—
R3	000103	10k 5% ¼W CARBON	MULLARD	CR25	38
R4		NOT USED			—
R5		NOT USED			—
R6	000103	10k 5% ¼W CARBON	MULLARD	CR25	—
R7	000103	" " " "	"	"	—
R8	000103	" " " "	"	"	—
R9	000103	" " " "	"	"	—
R10		NOT USED			—
R11	000103	" " " "	"	"	—
R12	000103	" " " "	"	"	—
R13	000103	" " " "	"	"	—
R14	000103	" " " "	"	"	—
R15	000103	" " " "	"	"	—
R16	000103	" " " "	"	"	—
R17	000103	" " " "	"	"	—
R18	000103	" " " "	"	"	—
R19	000103	" " " "	"	"	—
R20	000103	" " " "	"	"	—
R21	000103	" " " "	"	"	—
R22	000103	" " " "	"	"	—
R23	000103	" " " "	"	"	—

NOTES.

SEE SHEET 3 FOR LATEST ISSUE

ISS	C	1	2	3	4	5
E.C.O.	—	RELEASED	1330.34	1387	1397	1511
DATE		29-3-82	13.5.82	24.8.82	9.9.82	12.7.83
CHKD.		MD	MD	MD	MD	MD

DATE 16.11.81
DRAWN [illegible]
CHECKED [illegible]
APPROVED [illegible]
DATE 2.4.82

datron ELECTRONICS LTD

TITLE 4000 MOTHER P.C.B. ASSY.

DRAWING NUMBER 400440 SHEET 3 OF 8

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	000103	10k 5% ¼W CARBON	MULLARD	CR25	—
R25	000103	" " " "	"	"	—
R26	000103	" " " "	"	"	—
R27	000103	" " " "	"	"	—
R28		NOT USED			
R29	000103	10K 5% ¼W CARBON	MULLARD	CR25	—
R30	000103	" " " "	"	"	—
R31	000103	" " " "	"	"	—
R32	000103	" " " "	"	"	—
R33	000103	" " " "	"	"	—
R34	000103	" " " "	"	"	—
R35	000103	" " " "	"	"	—
R36		NOT USED			—
R37		NOT USED			—
R38	000103	10k " " "	"	"	—
R39		NOT USED			
R40	000103	10k 5% ¼W CARBON	MULLARD	CR25	—
R41	000473	47k " " "	"	"	4
R42	000103	10k " " "	"	"	—
R43	000103	10k " " "	"	"	—
R44	000103	10k " " "	"	"	—
R45	000103	10k " " "	"	"	—
R46	000103	10k " " "	"	"	—

NOTES.

SEE SHEET 3 FOR LATEST ISSUE

ISS.						
E.C.O.						
DATE						
CHKD.						

DATE 26-MAR 82
DRAWN BJ
CHECKED
APPROVED
DATE

datron ELECTRONICS LTD

TITLE 4000. MOTHER PCB ASSY.

DRAWING NUMBER 400440 SHEET 4 OF 8

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R47	000103	10k 5% 1/4W CARBON	MULLARD	CR25	–
R48	000103	10k 5% 1/4W CARBON	MULLARD	CR25	–
R49	000473	47k 5% 1/4W CARBON	MULLARD	CR25	–
R50	000473	47k 5% 1/4W CARBON	MULLARD	CR25	–
R51	000473	47k 5% 1/4W CARBON	MULLARD	CR25	–
R52	000104	100k 5% 1/4W CARBON	MULLARD	CR25	1
R53	001223	22K 5% 1/2W CARBON	MULLARD	CR37	2
R54	001223	22K 5% 1/2W CARBON	MULLARD	CR37	–
AN1	090090	47k x 8 2% NETWORK	AB	761-3-47k	6
AN2	090095	47k x 4 2% NETWORK	AB	850-83-47k	3
AN3	090090	47k x 8 2% NETWORK	AB	761-3-47k	–
AN4	090095	47k x 4 2% NETWORK	AB	850-83-47k	–
AN5	090095	47k x 4 2% NETWORK	AB	850-83-47k	–
AN6	090090	47k x 8 2% NETWORK	AB	761-3-47k	–
AN7	090090	47k x 8 2% NETWORK	AB	761-3-47k	–
AN8	090090	47k x 8 2% NETWORK	AB	761-3-47k	–
AN9	090090	47k x 8 2% NETWORK	AB	761-3-47k	–

NOTES.

SEE SHEET 3 FOR LATEST ISSUE

ISS.												
E.C.O.												
DATE												
CHKD.												

DATE 26·MAR 82
DRAWN BJ
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DATE

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TITLE 4000. MOTHER PCB ASSY.

DRAWING NUMBER 400440 SHEET 5 OF 8

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1	140045	1µF 20% 1K5V POLYPROP	NORTRONICS (MFD)	NSC 2027	1
C2	180036	4700µF 100V AL. ELECT	MULLARD / ITT	050-1-9472 / KS20 472T 100KD	2
C3	180036	4700µF " " "	" "	" "	–
C4	104032	220pF 10% 2KV CER DISC	ITT	HD09	1
L1	370017	COMMON MODE CHOKE	SIGA	SEE DRG	1
	410163-6	PCB			1
	540008	7/·2 PTFE INSUL. (WHITE) WIRE			A/R
	590001	SLEEVE MAX CABLE ϕ 3·0	HELLERMANN ELECTRIC	H15 X 20mm BLACK HELSYN	6
	530000	24/·2 PVC INSUL. WIRE		1·5kV RMS BLACK	350mm
	530111	24/·2 PVC INSUL. WIRE		1·5kV RMS BROWN	240mm
	530222	24/·2 PVC INSUL. WIRE		1·5kV RMS RED	350mm
	530666	24/·2 PVC INSUL. WIRE		1·5kV RMS BLUE	240mm
J19	604042	4WAY ·156" PLUG GD PL	MOLEX	09-72-2041	2

NOTES.

SEE SHEET 3 FOR LATEST ISSUE

ISS.												
E.C.O.												
DATE												
CHKD.												

DATE 25th MAR 82
DRAWN B.J
CHECKED
APPROVED
DATE

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TITLE 4000 MOTHER PCB ASSY

DRAWING NUMBER 400440 SHEET 6 OF 8

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
J28	605071	4WAY ·156" HOUSING	MOLEX	90-50-3041	1
J1	605111	24+24 WAY ·1" P.C.B SOCKET	AMP	2-141592-4	3
	605077	CRIMP TERMINAL GD.PL	MOLEX	08-56-0106	4
	605087-1	24 WAY PCB EDGE CONN.	SEE DRG		10
	605088-1	18 WAY PCB EDGE CONN.	SEE DRG		8
J2-J16	605089-1	12 WAY PCB EDGE CONN.	SEE DRG		7
	605090-1	6 WAY PCB EDGE CONN.	SEE DRG		8
	605091-1	6 WAY SPECIAL EDGE CONN.	SEE DRG		9
	605092-1	3 WAY PCB EDGE CONN.	SEE DRG		13
	612013	M3 x 8mm STANDOFF	CAMBION	350-5182-24-07	1
	613029	M3 CRINKLE WASHER S.S.			5
	611006	M3 x 10mm POZI-PAN STEEL	ZN PL		1
	611016	M3 x 8mm POZI-PAN STEEL	ZN PL		5
	611019	M3 x 35mm POZI-PAN STEEL	ZN PL		4
	612004	STANDOFF M3 x 4mm BRASS	HARWIN	CS2116/B	6
	613005	WASHER M3 INT/SHAKEPROOF	ZN/PLTD GKN		5
	615002	NUT M3 FULL HEX STEEL	ZN/PLTD GKN		10

NOTES.

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ISS.												
E.C.O.												
DATE												
CHKD.												

DATE 26 MAR 82
DRAWN BJ
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APPROVED
DATE

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TITLE 4000 MOTHER PCB ASSY.

DRAWING NUMBER 400440 SHEET 7 OF 8

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	617010	NYLATCH PLUNGER	ORDER FROM C.J. FOX + SONS	HN3P-32-4-1	20
	617011	NYLATCH GROMMET	ORDER FROM C.J. FOX + SONS	HN3G-32-1	20
	620003	SOLDER PIN	HARWIN	H2105A01	2
	620005	CLOVERLEAF P.T.F.E. TERMINAL	SEALECTRO	FTE 15 P59	10
	620006	SOLDER TURRET	HARWIN	H9001-01	47
	630115	CAPACITOR CLIP Ø 35mm	RS	543-383	4
	630131	CAPACITOR CLIP Ø 45mm	RS	543-068	1

NOTES.

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ISS.												
E.C.O.												
DATE												
CHKD.												

DATE 26-3-82
DRAWN BJ
CHECKED
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DATE

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TITLE 4000 MOTHER PCB ASSY

DRAWING NUMBER 400440 SHEET 8 OF 8

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000334	330k 5% ¼W CARBON	MULLARD	CR25	22
R2	000334	" " " "	"	"	—
R3	000334	" " " "	"	"	—
R4	000334	" " " "	"	"	—
R5	000334	" " " "	"	"	—
R6	000334	" " " "	"	"	—
R7	000334	" " " "	"	"	—
R8	000334	" " " "	"	"	—
R9	000334	" " " "	"	"	—
R10	000334	" " " "	"	"	—
R11	000334	" " " "	"	"	—
R12	000334	" " " "	"	"	—
R13	000334	" " " "	"	"	—
R14	000334	" " " "	"	"	—
R15	000334	" " " "	"	"	—
R16	000334	" " " "	"	"	—
R17	000334	" " " "	"	"	—
R18	000334	" " " "	"	"	—
R19	000334	" " " "	"	"	—
R20	000334	" " " "	"	"	—
R21	000334	" " " "	"	"	—
R22	000334	" " " "	"	"	—
R23	000102	1k " " "	"	"	11

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	C	1	2	3	4
E.C.O.	—	RELEASED	1352	1386	1405/30
DATE	22.10.81	12.5.82	1.7.82	24.8.82	25-11-82
CHKD.	MJD	MD	MD	MD	MD

DATE 10.4.81
DRAWN IL
CHECKED MJD
APPROVED B Hume
DATE 22.10.81.

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TITLE 4000 FRONT PCB. ASSY.

DRAWING NUMBER 400441

SHEET 2 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	000102	1k 5% ¼W CARBON	MULLARD	CR25	—
R25	000102	1k " " "	"	"	—
R26	000104	100k " " "	"	"	3
R27	000102	1k " " "	"	"	—
R28	000102	1k " " "	"	"	—
R29	000102	1k " " "	"	"	—
R30	000102	1k " " "	"	"	—
R31	000102	1k " " "	"	"	—
R32	000102	1k " " "	"	"	—
R33	000102	1k " " "	"	"	—
R34	000102	1k " " "	"	"	—
R35	000103	10k " " "	"	"	4
R36	000103	10k " " "	"	"	—
R37	000103	10k " " "	"	"	—
R38		NOT USED			—
R39	000472	4k7 " " "	"	"	6
R40	000688	6R8 " " "	"	"	8
R41	000688	6R8 " " "	"	"	—
R42	000688	6R8 " " "	"	"	—
R43	000272	2k7 " " "	"	"	18
R44	000272	2k7 " " "	"	"	—
R45	000472	4k7 " " "	"	"	—
R46	000272	2k7 " " "	"	"	—

NOTES.

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ISS.					
E.C.O.					
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CHKD.					

DATE 10.4.81
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DATE

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TITLE 4000 FRONT PCB. ASSY.

DRAWING NUMBER 400441

SHEET 3 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R47	000182	1k8 5% 1/4W CARBON	MULLARD	CR25	2
R48	000272	2k7 " " "	"	"	—
R49	000272	2k7 " " "	"	"	—
R50	000222	2k2 " " "	"	"	2
R51	000222	2k2 " " "	"	"	—
R52	000272	2k7 " " "	"	"	—
R53	000272	2k7 " " "	"	"	—
R54	000472	4k7 " " "	"	"	—
R55	000272	2k7 " " "	"	"	—
R56	000272	2k7 " " "	"	"	—
R57	000272	2k7 " " "	"	"	—
R58	000182	1k8 " " "	"	"	—
R59	000272	2k7 " " "	"	"	—
R60	000272	2k7 " " "	"	"	—
R61	000272	2k7 " " "	"	"	—
R62	000272	2k7 " " "	"	"	—
R63	000272	2k7 " " "	"	"	—
R64	000272	2k7 " " "	"	"	—
R65	000272	2k7 " " "	"	"	—
R66	000272	2k7 " " "	"	"	—
R67	000688	6R8 " " "	"	"	—
R68	000688	6R8 " " "	"	"	—
R69	000688	6R8 " " "	"	"	—

NOTES.

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DATE 10.4.81
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TITLE 4000 FRONT PCB. ASSY

DRAWING NUMBER 400441 SHEET 4 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R70	000688	6R8 5% 1/4W CARBON	MULLARD	CR25	—
R71	000688	6R8 " " "	"	"	—
R72	000563	56k " " "	"	"	1
R73, R74, R75	000472	4k7 " " "	"	"	—
R76	000103	10k " " "	"	"	—
R77, R78	000104	100k " " "	"	"	—
AN1. AN2	090017	100k x 7 2% NETWORK	BECKMAN	L08-1-R100k	2
AN3. AN4	090041	4k7 x 7 2% NETWORK	BECKMAN	L08-1-R4k7	2
AN5. AN6	090121	100k x 8 2% NETWORK	BECKMAN	L09-1-R100k	2
C1	150002	10µF 20% 16V DIP TANT	UNION CARBIDE	K10E16	2
C2	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	3
C3	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C4	150001	22µF 20% 16V DIP TANT	UNION CARBIDE	K22E16	1
C5	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C6		NOT USED			—
C7		NOT USED			—
C8	110013	100nF 20% 250V POLYESTER	MULLARD	C280AEP100k	19
C9	110013	" " " "	"	"	—
C10	110013	" " " "	"	"	—
C11	110013	" " " "	"	"	—
C12	110013	" " " "	"	"	—

NOTES.

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TITLE 4000 FRONT PCB ASSY

DRAWING NUMBER 400441 SHEET 5 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C13	110013	100nF 20% 250V POLYESTER	MULLARD	C280AE P100K	—
C14	110013	" " " "	"	"	—
C15	110013	" " " "	"	"	—
C16	110013	" " " "	"	"	—
C17	110013	" " " "	"	"	—
C18	110013	" " " "	"	"	—
C19	110013	" " " "	"	"	—
C20	110013	" " " "	"	"	—
C21	110013	" " " "	"	"	—
C22	110013	" " " "	"	"	—
C23	110013	" " " "	"	"	—
C24	110013	" " " "	"	"	—
C25	110013	" " " "	"	"	—
C26	110013	" " " "	"	"	—
C27	150002	10µF 20% 16V DIP TANT	UNION CARBIDE	K10E16	—
C28	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	K1R035	1
D1	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	18
D2	200001	" " " " "	"	"	—
D3	200001	" " " " "	"	"	—
D4	200001	" " " " "	"	"	—
D5	200001	" " " " "	"	"	—
D6	200001	" " " " "	"	"	—
D7	200001	" " " " "	"	"	—

NOTES

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DATE 10.4.81 | DRAWN IL | CHECKED | APPROVED | DATE

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TITLE 4000 FRONT PCB. ASSY

DRAWING NUMBER 400441 | SHEET 6 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D8	200001	75mA 75V GP Si. DIODE	FAIRCHILD	1N4148	—
D9	200001	" " " " "	"	"	—
D10	200001	" " " " "	"	"	—
D11	200001	" " " " "	"	"	—
D12	200001	" " " " "	"	"	—
D13	200001	" " " " "	"	"	—
D14	200001	" " " " "	"	"	—
D15	200001	" " " " "	"	"	—
D16	200001	" " " " "	"	"	—
D17	213005	75V 1/2W ZENER	MOTOROLA	BZX79C75	1
D18	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	—
D19	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	—
D20	213006	5V1 5W ZENER	UNITRODE	TVS 505	1
Q1		NOT USED			—
Q2	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	18
Q3	240009	" " "	"	"	—
Q4	240009	" " "	"	"	—
Q5	240009	" " "	"	"	—
Q6	240009	" " "	"	"	—
Q7	240009	" " "	"	"	—
Q8	240009	" " "	"	"	—

NOTES

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TITLE 4000 FRONT PCB ASSY

DRAWING NUMBER 400441 | SHEET 7 OF 11

J.W 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q9	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01/T018	–
Q10	250009	Si. PNP TRANSISTOR	NATIONAL	2N5401/T018	11
Q11	250009	" " "	"	"	–
Q12	250009	" " "	"	"	–
Q13	250009	" " "	"	"	–
Q14	250009	" " "	"	"	–
Q15	250009	" " "	"	"	–
Q16	250009	" " "	"	"	–
Q17	250009	" " "	"	"	–
Q18	250009	" " "	"	"	–
Q19	250009	" " "	"	"	–
Q20	250009	" " "	"	"	–
Q21	240025	Si NPN TRANSISTOR	"	MPSA13	3
Q22	240025	" " "	"	"	–
Q23	240025	" " "	"	"	–
Q24		NOT USED			–
Q25	250011	Si PNP TRANSISTOR	"	BC327/T018	8
Q26	250011	" " "	"	"	–
Q27	250011	" " "	"	"	–
Q28	250011	" " "	"	"	–
Q29	250011	" " "	"	"	–
Q30	250011	" " "	"	"	–
Q31	250011	" " "	"	"	–

NOTES

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TITLE 4000 FRONT PCB. ASSY.

DRAWING NUMBER 400441 SHEET 8 OF 11

JW 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q32	250011	Si PNP TRANSISTOR	NATIONAL	BC327/T018	–
Q33	240009	Si NPN TRANSISTOR	"	MPSL01/T018	–
Q34	240009	" " "	"	"	–
Q35	240009	" " "	"	"	–
Q36	240009	" " "	"	"	–
Q37	240009	" " "	"	"	–
Q38	240009	" " "	"	"	–
Q39	240009	" " "	"	"	–
Q40	240009	" " "	"	"	–
Q41	240009	" " "	"	"	–
Q42	240009	" " "	"	"	–
M1	280023	QUAD 2-I/P NOR GATE	MOTOROLA	MC14001 BCP.	1
M2	260005	5V 1A REGULATOR	MOTOROLA	MC7805CP	1
M3	280043	4 BIT LATCH/4 To 16 LINE DECODER	MOTOROLA	MC14515 BCP.	1
M4	280090	DUAL BINARY 1 of 4 DECODER	MOTOROLA	MC 14555 BCP.	1
M5	270071	DUAL 1 of 4 DECODER LS	NATIONAL	DM74LS156N	1
M6	280084	PROGRAMMABLE KEYBOARD/DISP.	INTEL	8279	1

NOTES.

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TITLE 4000 FRONT PCB. ASSY

DRAWING NUMBER 400441 SHEET 9 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
S1- S27	700079	KEYBOARD × ½ SWITCH. BLACK	NSF	K12/HALF KEY. BLACK	28
S34-S43	700061	KEYBOARD SWITCH. RED LED.	SCHADOW	SRL-RED LED	19
S44-S45	700062	KEYBOARD SWITCH GREEN. LED.	SCHADOW	SRL-GREEN LED.	2
S46-S50, S52-S55	700061	KEYBOARD SWITCH. RED LED	SCHADOW	SRL-RED LED	–
S56	700079	KEYBOARD × ½ SWITCH. BLACK	NSF	K12/HALF KEY. BLACK	–
	410144-7	PCB			1
J1	604060	24+24 WAY ·1" PCB. PLUG GOLD	AMP	2-825440-4	3
	605098	40 PIN DIL. LOW PROFILE SKT.	CAMBION	703-4340-01-06-00	1
	605060/L	14 WAY DIL. " " "			1
	605061/L	16 WAY DIL. " " "			2
	605097	24 WAY DIL. " " "	CAMBION	703-4324-01-06-00	1
	612023	STANDOFF M2.5×4 LG. BRASS ⅛" KE	CAMBION	350-5181-22-07	2
	800017	8½ DIGIT DISPLAY WITH LEGEND	DALE	SEE DRG.	2
	920096	BUZZER PIEZOELECTRIC	TOKO	PB 2720	1
	620003	SOLDER PCB TERMINAL LUG	HARWIN	H210SA	2

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DRAWING NUMBER 400441 SHEET 10 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	611016	M3×8mm POZI PAN STEEL	ZN PL		1
	611054	M2×6mm SLOT CSK STEEL	ZN PL		2
	613005	M3 INT. SHAKEPROOF			1
	613026	M2 WASHER STEEL ZN PL			2
	613027	M2 INT SHAKEPROOF			2
	615002	M3 FULL NUT STEEL ZN PL			1
	615016	M2 FULL NUT STEEL ZN PL			2
	620007	TEST POINT TERMINAL	MICROVAR	C30	8
	630029	TAPE DOUBLE SIDED ¼" × 1/32"	3M	4032	580mm
	900004	SILICONE RUBBER COMPOUND	RS	555-588	A/R

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DRAWING NUMBER 400441 SHEET 11 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000332	3k3 5% 1/4W CARBON	MULLARD	CR25	2
R2	000472	4k7 " " "	"	"	10
R3	000472	4k7 " " "	"	"	–
R4	000472	4k7 " " "	"	"	–
R5	000472	4k7 " " "	"	"	–
R6	000103	10k " " "	"	"	5
R7	000104	100k " " "	"	"	9
R8	000122	1k2 " " "	"	"	2
R9	000104	100k " " "	"	"	–
R10	000104	100k " " "	"	"	–
R11	000103	10k " " "	"	"	–
R12	000472	4k7 " " "	"	"	–
R13	000472	4k7 " " "	"	"	–
R14	000561	560R " " "	"	"	1
R15	000104	100k " " "	"	"	–
R16	000182	1k8 " " "	"	"	1
R17	014751	4k75 1% 1/8W 50ppm MF	HOLCO	H8C	1
R18	000122	1k2 5% 1/4W CARBON	MULLARD	CR25	–
R19	012491	2k49 1% 1/8W 50ppm MF	HOLCO	H8C	1
R20	000102	1k 5% 1/4W CARBON	MULLARD	CR25	21
R21	000472	4k7 " " "	"	"	–
R22	000223	22k " " "	"	"	1
R23	000103	10k " " "	"	"	–

NOTES.

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E.C.O.	RELEASED	1339,46	1349	1379	1401	1404. 1408. 1418	1443. 53	1456	1488	1511	1533
DATE	12.5.82	30.6.82	23.8.82	14.9.82	14.9.82	24.11.82	22-2-83	11.4.83.	6.6.83	12.7.83	29.9.83
CHKD.	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD

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DATE 13.5.82	DRAWING NUMBER 400442 400442A — SHEET 2 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	000332	3k3 5% 1/4W CARBON	MULLARD	CR25	–
R25	011002	10k0 1% 1/8W 50ppm MF	HOLCO	H8C	2
R26	000104	100k 5% 1/4W CARBON	MULLARD	CR25	–
R27	011002	10k0 1% 1/8W 50ppm MF	HOLCO	H8C	–
R28	000471	470R 5% 1/4W CARBON	MULLARD	CR25	3
R29	000104	100k " " "	"	"	–
R30	000472	4k7 " " "	"	"	–
R31	000102	1k " " "	"	"	–
R32	000104	100k " " "	"	"	–
R33	000102	1k " " "	"	"	–
R34	000102	1k " " "	"	"	–
R35	000102	1k " " "	"	"	–
R36	000102	1k " " "	"	"	–
R37	000102	1k " " "	"	"	–
R38	000102	1k " " "	"	"	–
R39	000102	1k " " "	"	"	–
R40	000102	1k " " "	"	"	–
R41	000102	1k " " "	"	"	–
R42	000103	10k " " "	"	"	–
R43	000102	1k " " "	"	"	–
R44	000102	1k " " "	"	"	–
R45	000102	1k " " "	"	"	–
R46	000102	1k " " "	"	"	–

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J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R47	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R48	000102	1k " " "	"	"	—
R49	000102	1k " " "	"	"	—
R50	000102	1k " " "	"	"	—
R51	000102	1k " " "	"	"	—
R52	000472	4k7 " " "	"	"	—
R53	000104	100k " " "	"	"	—
R54	000104	100k " " "	"	"	—
R55	000103	10k " " "	"	"	—
R56	000471	470R " " "	"	"	—
R57	000471	470R " " "	"	"	—
R58	000102	1k " " "	"	"	—
R59	000391	390R " " "	"	"	1
R60	000472	4k7 " " "	"	"	—
AN1	090050	3k3 x 7 2% NETWORK	BECKMAN	764-1-R3k3	1
AN2	090017	100k x 7 2% NETWORK	BETWEEN	764-1-R100k	1
AN3	090046	10k x 7 2% NETWORK	BECKMAN	764-1-R10k	2
AN4	090046	10k x7 2% NETWORK	BETWEEN	764-1-R10k	—
AN5	090085	12k x8 2% NETWORK	AB	761-3-12k	1
C1	150002	10µF 20% 16V DIP. TANT.	UNION CARBIDE	K10E16	9
C2	150002	10µF 20% 16V DIP. TANT.	UNION CARBIDE	K10E16	—

NOTES.

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DRAWING NUMBER 400442 400442A SHEET 4 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C3	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	14
C4	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C5	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C6	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C7		NOT USED			
C8	150016	1µF 20% 35V DIP. TANT.	UNION CARBIDE	K1R035	3
C9	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C10	150002	10µF 20% 16V DIP. TANT.	UNION CARBIDE	K10E16	—
C11	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C12	150002	10µF 20% 16V DIP. TANT.	UNION CARBIDE	K10E16	—
C13	150002	10µF 20% 16V DIP. TANT.	UNION CARBIDE	K10E16	—
C14	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C15	150002	10µF 20% 16V DIP. TANT.	UNION CARBIDE	K10E16	—
C16	102102	1nF 10% 500V CER DISC	ITT	CD10	1
C17	150002	10µF 20% 16V DIP. TANT	UNION CARBIDE	K10E16	—
C18	150016	1µF 20% 35V DIP. TANT	UNION CARBIDE	K1R035	—
C19	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C20	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C21	150002	10µF 20% 16V DIP. TANT.	UNION CARBIDE	K10E16	—
C22	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C23	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C24	150002	10µF 20% 16V DIP. TANT	UNION CABBIDE	K10E16	—
C25	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—

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DRAWING NUMBER 400442 400442A SHEET 5 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C26	101103	10nF 25% 250V CER DISC	ITT	CD10	2
C27	104026	47nF +50 -20 % 50V CER DISC	SIEMENS	B37449	–
C28	150006	4μ7F 20% 16V DIP TANT	UNION CARBIDE	K4R7E16	1
C29	150016	1μF 20% 35V DIP TANT	UNION CARBIDE	K1R035	–
C30	150024	47μF 20% 16V DIP TANT	UNION CARBIDE	K47E16	1
C31	101103	10nF 25% 250V CER DISC	ITT	CD10	–
C32	104026	47nF +50 -20 % 50V CER DISC	SIEMENS	B37449	–
D1	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	5
D2	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	–
D3	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	–
D4	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	–
D5	210047	4V7 400mW ZENER	MULLARD	BZY88C4V7	1
D6	214012	2V45 30ppm ZENER	FERRANTI	ZN458	1
D7	220010	Si HOT CARRIER DIODE	H.P.	HSCH1001 / 1N6263	1
D8	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	–

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J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q1	240001	Si NPN TRANSISTOR	NATIONAL	BC184 / TO18	2
Q2	240001	Si NPN TRANSISTOR	NATIONAL	BC184 / TO18	–
Q3	230031	N-CHAN DUAL JFET	TELEDYNE	SU2656M	1

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J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M1	280024	TRI-STATE HEX. NON-INV. BUFFER	MOTOROLA	MC14503 BCP	4
M2	280024	TRI-STATE HEX. NON-INV. BUFFER	MOTOROLA	MC14503 BCP	—
M3	290091-1	74S188 PROM PROGRAMMED	DATRON (SEE DRG)	SN74S188N (RED)	1
M4	270056	8 I/P NAND LS	NATIONAL	DM74LS30N	1
M5	270048	QUAD 2 I/P NAND LS	NATIONAL	DM74LS00N	4
M6	270050	HEX. INVERTER	NATIONAL	74LS04	2
M7	280008	QUAD 2 I/P 'NAND' GATE	MOTOROLA	MC14011 BCP	2
M8	280011	DUAL D FLIP-FLOP	MOTOROLA	MC14013 BCP	1
M9	280102	14 BIT BINARY COUNTER	MULLARD	HEF 4020 BP	1
M10	280091	UN-BUFFERED TRIPLE 3 I/P 'NAND'	MOTOROLA	MC14023 UBCP	1
M11	220015	5kV OPTO ISOLATOR	FAIRCHILD	FCD 820C	2
M12	280077	HEX. INVERTER	MOTOROLA	MC14572 BCP	1
M13	280033	8-CHAN DATA SELECTOR	MOTOROLA	MC14512 BCP	1
M14	280015	QUAD LATCH	MOTOROLA	MC14076 BCP	2
M15	280015	QUAD LATCH	MOTOROLA	MC14076 BCP	—
M16	280062	8-BIT STATIC RAM	MOTOROLA	MC6810A	1
M17	270048	QUAD 2 I/P NAND GATE	NATIONAL	74LS00	—
M18	SEE TABLE	2532 EPROM PROGRAMMED	DATRON	TMS 2532	1
M19	SEE TABLE	2532 EPROM PROGRAMMED	DATRON	TMS 2532	1
M20	SEE TABLE	2532 EPROM PROGRAMMED	DATRON	TMS 2532	1
M21	SEE TABLE	2532 EPROM PROGRAMMED	DATRON	TMS 2532	1
M22	SEE TABLE	2532 EPROM PROGRAMMED	DATRON	TMS 2532	1
M23		NOT FITTED			—

NOTES.

INSTRUMENT	4000	4000A
DIG. ASSY	400442	400442A
M18	290092-11	290092/A-11
M19	290093-11	290093/A-11
M20	290094-11	290094/A-11
M21	290095-11	290095/A-11
M22	290098-11	290095/A-11

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DRAWING NUMBER 400442 400442A | SHEET 8 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M24	280096	1k x 4 BIT STATIC RAM	FAIRCHILD	2114 LPC	2
M25	280096	1k x 4 BIT STATIC RAM	FAIRCHILD	2114 LPC	—
M26	280066	256 x 4 BIT STATIC CMOS RAM	SEE DRAWING		2
M27	280066	256 x 4 BIT STATIC CMOS RAM	SEE DRAWING		—
M28	260043	358 DUAL OP. AMP	NATIONAL	LM358N	1
M29	280064	IEEE 488 INTERFACE CHIP	MOTOROLA	MC68488P	1
M30	280005	TRIPLE GATE	MOTOROLA	MC14501 BCP	1
M31	270045	QUAD 2 TO 1 LINE MUX LS	NATIONAL	DM74 LS157N	1
M32	280092	DUAL 4-BIT LATCH	MOTOROLA	MC14508 BCP	1
M33	270048	QUAD 2 I/P NAND LS	NATIONAL	DM74LS00N	—
M34	280087	MICRO-PROCESSOR CHIP	MOTOROLA	MC6802	1
M35	270057	DUAL J-K FLIP-FLOP LS	NATIONAL	DM74 LS76N	1
M36	280024	TRI-STATE HEX. NON-INV. BUFFER	MOTOROLA	MC14503 BCP	—
M37	270077	TRI-STATE HEX. BUFFER LS	NATIONAL	DM74LS367	1
M38		NOT USED			—
M39	220015	5kV OPTO ISOLATOR	FAIRCHILD	FCD 820C	—
M40	280086	BI-DIRECTIONAL BUS TRANSCEIVER	MOTOROLA	MC3447	2
M41	280059	DUAL BINARY UP COUNTER	MOTOROLA	MC14520 BCP	1
M42	280085	QUAD 2 I/P 'AND' GATE	MOTOROLA	MC14081 BCP	4
M43	280085	QUAD 2 I/P 'AND' GATE	MOTOROLA	MC14081 BCP	—
M44	280008	QUAD 2 I/P 'NAND' GATE	MOTOROLA	MC14011 BCP	—
M45	280085	QUAD 2 I/P 'AND' GATE	MOTOROLA	MC14081 BCP	—
M46	280085	QUAD 2 I/P 'AND' GATE	MOTOROLA	MC14081 BCP	—

NOTES.

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DRAWING NUMBER 400442 400442A | SHEET 9 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M47	280024	TRI-STATE HEX NON-INV BUFFER	MOTOROLA	MC14503 BCP	—
M48	280086	BI-DIRECTIONAL BUS TRANSCEIVER	MOTOROLA	MC3447	—
M49	270048	QUAD 2 I/P NAND LS	NATIONAL	DM74LS00N	—
M50	270050	HEX. INVERTER	NATIONAL	74LS04	—
M51	270058	DUAL 2 TO 4 LINE DEMUX. LS	NATIONAL	DM74LS155N	2
M52	270058	DUAL 2 TO 4 LINE DE MUX. LS	NATIONAL	DM74LS155N	—
M53	280068	DUAL PRECISION MONOSTABLE	MOTOROLA	MC14538 BCP	1
	605059	8 WAY DIL SOCKET			2
	410156-5	PCB			1
TP's	540002	22 SWG BTC WIRE			A/R
JL1	604037	PROGRAMMING CLASS 160 PLUG	AUGAT	8136-475G-8	1
	605050	40 WAY DIL LOW PROFILE SKT.			2
	605060	14 WAY DIL SOCKET			15
	605061	16 WAY DIL SOCKET			19
	605062	18 WAY DIL SOCKET			2
	605063	22 WAY DIL SOCKET			2
	605064	24 WAY DIL. SOCKET			10
	605066	6 WAY DIL SOCKET			2
	620003	SOLDER PCB. TERMINAL LUG	HARWIN	H2105A	1
	630098	COMPONENT CLIP	RICHCO	KKU-8	1
	630112	CIRCUIT BOARD EJECTOR	RICHCO	CBE BLACK	2
S1	700065	KEYSWITCH 1P1W MOMENT.	LIPA + ISOSTAT	D6	1
	620007	TEST POINT TERMINAL	MICROVAR	C30	16

NOTES.

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TITLE 4000/4000A DIGITAL PCB. ASSY.
DRAWING NUMBER 400442 400442A
SHEET 10 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	618004	MOUNTING PAD TO18	JERMYN	TO18-008D	1

NOTES.

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TITLE 4000/4000A DIGITAL PCB ASSY.
DRAWING NUMBER 400442 400442A
SHEET 11 OF 11

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000102	1k 5% 1/4W CARBON	MULLARD	CR25	5
R2	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R3		NOT USED			—
R4		NOT USED			—
R5	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	4
R6	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	—
R7	000474	470k 5% 1/4W CARBON	MULLARD	CR25	2
R8	000124	120k 5% 1/4W CARBON	MULLARD	CR25	1
R9	000471	470R 5% 1/4W CARBON	MULLARD	CR25	8
R10	000474	470k 5% 1/4W CARBON	MULLARD	CR25	—
R11	012372	23k7 1% 1/8W 50ppm MF	HOLCO	H8C	4
R12	012372	23k7 1% 1/8W 50ppm MF	HOLCO	H8C	—
R13	012372	23k7 1% 1/8W 50ppm MF	HOLCO	H8C	—
R14	012372	23k7 1% 1/8W 50ppm MF	HOLCO	H8C	—
R15	000392	3k9 5% 1/4W CARBON	MULLARD	CR25	3
R16	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R17	000392	3k9 5% 1/4W CARBON	MULLARD	CR25	—
R18	000392	3k9 5% 1/4W CARBON	MULLARD	CR25	—
R19	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	1
R20	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R21	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R22	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R23	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—

NOTES.

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TITLE 4000. ANALOG INTERFACE PCB. ASSY.

DRAWING NUMBER 400443 — SHEET 2 OF 9

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R25	000331	330R 5% 1/4W CARBON	MULLARD	CR25	1
R26	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R27	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R28	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R29	000561	560R 5% 1/4W CARBON	MULLARD	CR25	4
R30	000561	560R 5% 1/4W CARBON	MULLARD	CR25	—
R31	000561	560R 5% 1/4W CARBON	MULLARD	CR25	—
R32	000561	560R 5% 1/4W CARBON	MULLARD	CR25	—
R33	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R34	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	—
R35	000472	4K7 5% 1/4W CARBON	MULLARD	CR25	—
AN1	090079	5k6 × 8 2% NETWORK	AB	850-91-5k6	2
AN2	090079	5k6 × 8 2% NETWORK	AB	850-91-5k6	—

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TITLE 4000 ANALOG INTERFACE PCB. ASSY.

DRAWING NUMBER 400443 — SHEET 3 OF 9

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1	104026	47nF +50/-20 % 50V CER.DISC	SIEMENS	B37449	42
C2	104026	47nF " " " "	"	"	—
C3	104026	47nF " " " "	"	"	—
C4	104026	47nF " " " "	"	"	—
C5	104026	47nF " " " "	"	"	—
C6	104026	47nF " " " "	"	"	—
C7	104026	47nF " " " "	"	"	—
C8	104026	47nF " " " "	"	"	—
C9		NOT USED			—
C10	101103	10nF 25% 250V CER.DISC	ITT	CD10	1
C11	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	—
C12	104026	47nF " " " "	"	"	—
C13	104026	47nF " " " "	"	"	—
C14	104026	47nF " " " "	"	"	—
C15	104026	47nF " " " "	"	"	—
C16	104026	47nF " " " "	"	"	—
C17	104026	47nF " " " "	"	"	—
C18	104026	47nF " " " "	"	"	—
C19	104026	47nF " " " "	"	"	—
C20	104026	47nF " " " "	"	"	—
C21	104026	47nF " " " "	"	"	—
C22	104026	47nF " " " "	"	"	—
C23	104026	47nF " " " "	"	"	—

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TITLE 4000. ANALOG INTERFACE PCB. ASSY.

DRAWING NUMBER 400443 SHEET 4 OF 9

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C24	104026	47nF +50/-20 % 50V CER.DISC	SIEMENS	B37449	—
C25	104026	" " " " "	"	"	—
C26	104026	" " " " "	"	"	—
C27	104026	" " " " "	"	"	—
C28	104026	" " " " "	"	"	—
C29	150008	470nF 20% 35v DIP. TANT	UNION CARBIDE	KR47E35	1
C30	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	—
C31	150002	10µF 20% 16v DIP TANT	UNION CARBIDE	K10E16	1
C32	150012	100nF 20% 35v DIP. TANT	UNION CARBIDE	KR10E35	1
C33	104026	47nF +50/-20 % 50V CER. DISC	SIEMENS	B37449	—
C34	104026	" " " " "	"	"	—
C35	104026	" " " " "	"	"	—
C36	104026	" " " " "	"	"	—
C37	104026	" " " " "	"	"	—
C38	104026	" " " " "	"	"	—
C39	102220	22pF 5% 500V CER.DISC	ITT	CD10	1
C40	102330	33pF 5% 500V CER DISC	ITT	CD10	1
C41	104026	47nF +50/-20 % 50V CER.DISC	SIEMENS	B37449	—
C42	104026	" " " " "	"	"	—
C43	104026	" " " " "	"	"	—
C44	104026	" " " " "	"	"	—
C45	104026	" " " " "	"	"	—
C46	104026	" " " " "	"	"	—

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DRAWING NUMBER 400443 SHEET 5 OF 9

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C47	150024	47µF 20% 16V DIP. TANT	UNION CARBIDE	K47E16	1
C48	104026	47nF $^{+50}_{-20}$% 50V CER.DISC	SIEMENS	B37449	—
C49	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C50	120010	1µ5F 10% 160V POLYCARB	ASHCROFT	A2B152058	1
C51	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
D1	220010	Si HOT CARRIER DIODE	HP	HSCH1001/1N6263	2
D2	220010	Si HOT CARRIER DIODE	HP	HSCH1001/1N6263	—
Q1	240007	Si NPN TRANSISTOR	NATIONAL	2N3646	1
M1	270050	HEX INVERTER LS	NATIONAL	DM74LS04N	1
M2	280008	QUAD 2 I/P 'NAND' GATE	MOTOROLA	MC14011BCP	2
M3	280011	DUAL D FLIP-FLOP	MOTOROLA	MC14013BCP	2
M4	280059	DUAL BINARY UP COUNTER	MOTOROLA	MC14520BCP	1
M5	280037	HEX BUFFER	MOTOROLA	MC14050BCP	1
M6	270048	QUAD 2 I/P 'NAND' LS	NATIONAL	DM74LS00N	2
M7	270072	QUAD 2 I/P 'NOR' LS	NATIONAL	DM74LS02N	2
M8	270002	QUAD 2 I/P O/C NAND	NATIONAL	DM7401N	2
M9		NOT USED			—
M10		NOT USED			—
M11		NOT USED			—

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DRAWING NUMBER 400443 — SHEET 6 OF 9

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M12	270072	QUAD 2 I/P 'NOR' LS	NATIONAL	DM74LS02N	—
M13	270055	DUAL 4 I/P 'NAND' LS	NATIONAL	DM74LS20N	1
M14	270075	DUAL D FLIP-FLOP LS	NATIONAL	DM74LS74N	1
M15	280095	4BIT SYNC. BINARY COUNTER	MULLARD	HEF40163BP	3
M16	280095	4BIT SYNC. BINARY COUNTER	MULLARD	HEF40163BP	—
M17	280095	4BIT SYNC. BINARY COUNTER	MULLARD	HEF40163BP	—
M18	280010	DECADE COUNTER	MOTOROLA	MC14160BCP	1
M19	280093	QUAD EXCLUSIVE-OR GATE	MOTOROLA	MC14070BCP	6
M20	280093	QUAD EXCLUSIVE-OR GATE	MOTOROLA	MC14070BCP	—
M21	280093	QUAD EXCLUSIVE-OR GATE	MOTOROLA	MC14070BCP	—
M22	270074	TRIPLE 3 I/P 'NOR' LS	NATIONAL	DM74LS27N	3
M23	270074	TRIPLE 3 I/P 'NOR' LS	NATIONAL	DM74LS27N	—
M24	270074	TRIPLE 3 I/P 'NOR' LS	NATIONAL	DM74LS27N	—
M25	280093	QUAD EXCLUSIVE-OR GATE	MOTOROLA	MC14070BCP	—
M26	280093	QUAD EXCLUSIVE-OR GATE	MOTOROLA	MC14070BCP	—
M27	280093	QUAD EXCLUSIVE-OR GATE	MOTOROLA	MC14070BCP	—
M28	280008	QUAD 2 I/P 'NAND' GATE	MOTOROLA	MC14011BCP	—
M29	280068	DUAL PRECISION MONOSTABLE	MOTOROLA	MC14538BCP	1
M30	260029	311 VOLTAGE COMPARATOR	NATIONAL	LM311H	1
M31	280015	QUAD LATCH	MOTOROLA	MC14076BCP	7
M32	280015	QUAD LATCH	MOTOROLA	MC14076BCP	—
M33	280015	QUAD LATCH	MOTOROLA	MC14076BCP	—
M34	280015	QUAD LATCH	MOTOROLA	MC14076BCP	—

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TITLE 4000. ANALOG INTERFACE PCB. ASSY.

DRAWING NUMBER 400443 — SHEET 7 OF 9

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M35	270073	QUAD 2 I/P O/C 'AND' LS	NATIONAL	DM74LS09N	2
M36	270073	QUAD 2 I/P O/C 'AND' LS	NATIONAL	DM74LS09N	—
M37	280015	QUAD LATCH	MOTOROLA	MC14076BCP	—
M38	280015	QUAD LATCH	MOTOROLA	MC14076 BCP	—
M39	280015	QUAD LATCH	MOTOROLA	MC14076 BCP	—
M40	270036	MONOSTABLE	NATIONAL	DM74121N	1
M41	270057	DUAL JK FLIP-FLOP LS	NATIONAL	DM74LS76N	2
M42	270057	DUAL JK FLIP-FLOP LS	NATIONAL	DM74LS76N	—
M43	270048	QUAD 2 I/P NAND LS	NATIONAL	DM74LS00N	—
M44	280094	SYNC? SERIAL DATA ADAPTOR	MOTOROLA	MC6852P	1
M45	280024	TRI-STATE HEX. NON-INV. BUFFER	MOTOROLA	MC14503 BCP	1
M46	270002	QUAD 2 I/P O/C NAND	NATIONAL	DM7401N	—
M47	280038	HEX D FLIP-FLOP	MOTOROLA	MC14174 BCP	4
M48	280038	HEX D FLIP-FLOP	MOTOROLA	MC14174 BCP	—
M49	280011	DUAL D FLIP-FLOP	MOTOROLA	MC14013 BCP	—
M50	280105	8 I/P NAND	MOTOROLA	MC14068 BCP	1
M51	280038	HEX D FLIP-FLOP	MOTOROLA	MC14174 BCP	—
M52	280038	HEX D FLIP-FLOP	MOTOROLA	MC14174 BCP	—

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TITLE 4000. ANALOG INTERFACE PCB. ASSY.

DRAWING NUMBER 400443 SHEET 8 OF 9

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	410155-4	PCB			1
	605060/A	14 WAY DIL SOCKET			26
	605061/A	16 WAY DIL SOCKET			21
	605064/A	24 WAY DIL SOCKET			1
	630117	CIRCUIT BOARD EJECTOR	RICHCO	CBE BROWN	2
X1	800023	4·096 MHz CRYSTAL	IQD	A122A	1
	620007	TEST POINT TERMINAL	MICROVAR	C 30	22
	540002	22 SWG TINNED COPPER WIRE	R.S.		A/R

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TITLE 4000. ANALOG INTERFACE PCB. ASSY.

DRAWING NUMBER 400443 SHEET 9 OF 9

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	5
R2	000561	560R 5% 1/4W CARBON	MULLARD	CR25	8
R3	000622	6k2 5% 1/4W CARBON	MULLARD	CR25	4
R4	000561	560R 5% 1/4W CARBON	MULLARD	CR25	–
R5	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	–
R6	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	–
R7	000561	560R 5% 1/4W CARBON	MULLARD	CR25	–
R8	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	2
R9	000561	560R 5% 1/4W CARBON	MULLARD	CR25	–
R10	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	–
R11	000103	10k 5% 1/4W CARBON	MULLARD	CR25	7
R12	000102	1k 5% 1/4W CARBON	MULLARD	CR25	6
R13	000622	6k2 5% 1/4W CARBON	MULLARD	CR25	–
R14	000102	1k 5% 1/4W CARBON	MULLARD	CR25	–
R15	000103	10k 5% 1/4W CARBON	MULLARD	CR25	–
R16	013161	3k16 1% 1/8W 50ppm MF	HOLCO	H8C	4
R17	000101	100R 5% 1/4W CARBON	MULLARD	CR25	12
R18	014750	475R 1% 1/8W 50ppm MF	HOLCO	H8C	1
R19	013161	3k16 1% 1/8W 50ppm MF	HOLCO	H8C	–
R20	000101	100R 5% 1/4W CARBON	MULLARD	CR25	–
R21	013161	3k16 1% 1/8W 50ppm MF	HOLCO	H8C	–
R22	000101	100R 5% 1/4W CARBON	MULLARD	CR25	–
R23	012261	2k26 1% 1/8W 50ppm MF	HOLCO	H8C	1

NOTES.

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TITLE 4000 4000A REF. DIVIDER PCB. ASSY.
DRAWING NUMBER 400444 400444 A
SHEET 2 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	013161	3k16 1% 1/8W 50ppm MF	HOLCO	H8C	–
R25	000101	100R 5% 1/4W CARBON	MULLARD	CR25	–
R26	000102	1k 5% 1/4W CARBON	MULLARD	CR25	–
R27	000431	430R 5% 1/4W CARBON	MULLARD	CR25	2
R28	000101	100R 5% 1/4W CARBON	MULLARD	CR25	–
R29 (FSV)	019538	95R3 1% 1/8W 50ppm MF	HOLCO	H8C	4
R30	000431	430R 5% 1/4W CARBON	MULLARD	CR25	–
R31	000101	100R 5% 1/4W CARBON	MULLARD	CR25	–
R32	000102	1k 5% 1/4W CARBON	MULLARD	CR25	–
R33 (FSV)	019538	95R3 1% 1/8W 50ppm MF	HOLCO	H8C	–
R34	000562	5k6 5% 1/4W CARBON	MULLARD	CR25	4
R35	000561	560R 5% 1/4W CARBON	MULLARD	CR25	–
R36	000622	6k2 5% 1/4W CARBON	MULLARD	CR25	–
R37	000561	560R 5% 1/4W CARBON	MULLARD	CR25	–
R38	000562	5k6 5% 1/4W CARBON	MULLARD	CR25	–
R39	000562	5k6 5% 1/4W CARBON	MULLARD	CR25	–
R40	000561	560R 5% 1/4W CARBON	MULLARD	CR25	–
R41	000622	6k2 5% 1/4W CARBON	MULLARD	CR25	–
R42	000561	560R 5% 1/4W CARBON	MULLARD	CR25	–
R43	000562	5k6 5% 1/4W CARBON	MULLARD	CR25	–
R44	000202	2k0 5% 1/4W CARBON	MULLARD	CR25	1
R45	000222	2k2 5% 1/4W CARBON	MULLARD	CR25	1
R46	014320	432R 1% 1/8W 50ppm MF	HOLCO	H8C	4

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TITLE 4000 4000A REF. DIVIDER PCB. ASSY.
DRAWING NUMBER 400444 400444 A
SHEET 3 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R47	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R48 (FSV)	019538	95R3 1% 1/8W 50ppm MF	HOLCO	H8C	—
R49	014320	432R 1% 1/8W 50ppm MF	HOLCO	H8C	—
R50	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R51	014320	432R 1% 1/8W 50ppm MF	HOLCO	H8C	—
R52	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R53 (FSV)	019538	95R3 1% 1/8W 50ppm MF	HOLCO	H8C	—
R54	014320	432R 1% 1/8W 50ppm MF	HOLCO	H8C	—
R55	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R56	000474	470k 5% 1/4W CARBON	MULLARD	CR25	1
R57	000184	180k 5% 1/4W CARBON	MULLARD	CR25	1
R58	013742	37k4 1% 1/8W 50ppm MF	HOLCO	H8C	1
R59	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R60	000104	100k 5% 1/4W CARBON	MULLARD	CR25	4
R61	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—
R62	018872	88k7 1% 1/8W 50ppm MF	HOLCO	H8C	1
R63	017872	78k7 1% 1/8W 50ppm MF	HOLCO	H8C	2
R64	070144	36k0 ·01% 5ppm WW	MANN	MX125B	1
R65	070142	12k0 ·01% 5ppm WW	MANN	MX125B	2
R66	017872	78k7 1% 1/8W 50ppm MF	HOLCO	H8C	—
R67	000912	9k1 5% 1/4W CARBON	MULLARD	CR25	1
R68	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R69		NOT USED			—

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TITLE 4000 4000A REF. DIVIDER PCB. ASSY.

DRAWING NUMBER 400444 400444A SHEET 4 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R70		NOT USED			—
R71		NOT USED			—
R72	000682	6k8 5% 1/4W CARBON	MULLARD	CR25	1
R73	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	—
R74	000470	47R 5% 1/4W CARBON	MULLARD	CR25	2
R75	011183	118k 1% 1/8W 50ppm MF	HOLCO	H8C	1
R76	011001	1k00 1% 1/8W 50ppm MF	HOLCO	H8C	4
R77	011001	1k00 1% 1/8W 50ppm MF	HOLCO	H8C	—
R78	012672	26k7 1% 1/8W 50ppm MF	HOLCO	H8C	1
R79	080032	78k7 ·1% 1W 10ppm MF	VISHAY	VS3CS	1
R80	070143	16k0 ·01% 5ppm WW	MANN	MX125B	1
R81	070142	12k0 ·01% 5ppm WW	MANN	MX125B	—
R82		NOT USED			
R83		NOT USED			
R84	012212	22k1 1% 1/8W 50ppm MF	HOLCO	H8C	2
R85 (FSV)	015112	51K1 1% 1/8W 50ppm MF	HOLCO	H8C	1
R86	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R87	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—
R88		NOT USED			—
R89		NOT USED			—
R90	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—
R91	011182	11k8 1% 1/8W 50ppm MF	HOLCO	H8C	1
R92	011001	1k00 1% 1/8W 50ppm MF	HOLCO	H8C	—

NOTES.

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DRAWING NUMBER 400444 400444A SHEET 5 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R93	011001	1k00 1% 1/8W 50ppm MF	HOLCO	H8C	—
R94	014532	45k3 1% 1/8W 50ppm MF	HOLCO	H8C	1
R95	011402	14k0 1% 1/8W 50ppm MF	HOLCO	H8C	1
R96	019531	9k53 1% 1/8W 50ppm MF	HOLCO	H8C	1
R97		NOT USED			—
R98	011002	10k 1% 1/8W 50ppm MF	HOLCO	H8C	3
R99	070156	555k41 ·01% 5ppm WW	MANN	AX175B	1
R100	070145	475R ·01% 5ppm WW	MANN	AX175B	1
R101	012212	22k1 1% 1/8W 50ppm MF	HOLCO	H8C	—
R102	000473	47k 5% 1/4W CARBON	MULLARD	CR25	3
R103	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R104	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R105	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	—
R106	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R107	000393	39k 5% 1/4W CARBON	MULLARD	CR25	2
R108	012001	2k00 1% 1/8W 50ppm MF	HOLCO	H8C	2
R109	011302	13k0 1% 1/8W 50ppm MF	HOLCO	H8C	2
R110	012001	2k00 1% 1/8W 50ppm MF	HOLCO	H8C	—
R111	000393	39k 5% 1/4W CARBON	MULLARD	CR25	—
R112	011302	13k0 1% 1/8W 50ppm MF	HOLCO	H8C	—
R113	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R114	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R115	000470	47R 5% 1/4W CARBON	MULLARD	CR25	—

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TITLE 4000 4000A REF DIVIDER PCB. ASSY.
DRAWING NUMBER 400444 400444A
SHEET 6 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R116	012211	2k21 1% 1/8W 50ppm MF	HOLCO	H8C	1
R117	000621	620R 5% 1/4W CARBON	MULLARD	CR25	1
R118	006132	1k30 2% 1W MET-OX	ELECTROSIL	FP1	2
R119	006132	1k30 2% 1W MET-OX	ELECTROSIL	FP1	—
R120	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R121	000473	47k 5% 1/4W CARBON	MULLARD	CR25	—
R122	000823	82k 5% 1/4W CARBON	MULLARD	CR25	1
R123	000473	47k 5% 1/4W CARBON	MULLARD	CR25	—
R124	000152	1K5 5% 1/4W CARBON	MULLARD	CR25	1
R125	011002	10K0 1% 1/8W 50ppm MF	HOLCO	H8C	-
R126	011002	10K0 1% 1/8W 50ppm MF	HOLCO	H8C	-
AN1	090031	1k x7 2% NETWORK	BECKMAN	764-1-R1k	1
AN2	090096	1M x8 2% NETWORK	AB	850-91-1M	2
AN3	090096	1M x8 2% NETWORK	AB	850-91-1M	—
AN4	090085	12k x8 2% NETWORK	AB	761-3-12k	1

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TITLE 4000 4000A REF DIVIDER PCB ASSY
DRAWING NUMBER 400444 400444A
SHEET 7 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1		NOT USED			—
C2	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	23
C3		NOT USED			—
C4		NOT USED			—
C5	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C6	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C7	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	KIRO E35	2
C8	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C9	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C10	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C11	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C12	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C13	102101	100pF 10% 500V CER DISC	ITT	CD10	1
C14	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C15	110013	100nF 20% 250V POLYESTER	MULLARD	C280AE P100k	2
C16	110013	100nF 20% 250V POLYESTER	MULLARD	C280AE P100k	—
C17	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C18	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C19	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C20	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C21	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C22	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C23	140016	470nF 10% 250V POLYPROP	RIFA	PHE402 HFK	10

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J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C24	102470	47pF 5% 500V CER DISC	ITT	CD10	3
C25	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C26	102470	47pF 5% 500V CER DISC	ITT	CD10	—
C27	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C28	102102	1nF 10% 500V CER DISC	ITT	CD10	2
C29	140016	470nF 10% 250V POLYPROP	RIFA	PHE402HFK	—
C30	102470	47pF 5% 500V CER DISC	ITT	CD10	—
C31	140016	470nF 10% 250V POLYPROP	RIFA	PHE402 HFK	—
C32	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	—
C33	150020	10µF 20% 25V DIP. TANT.	UNION CARBIDE	K10E25	5
C34	180015	470µF 25V AL. ELECT.	MULLARD	017-16471	1
C35	150020	10µF 20% 25V DIP. TANT.	UNION CARBIDE	K10E25	—
C36		NOT USED			—
C37		NOT USED			—
C38	102102	1nF 10% 500V CER DISC	ITT	CD10	—
C39	150020	10µF 20% 25V DIP TANT	UNION CARBIDE	K10E25	—
C40	102270	27pF 5% 500V CER DISC	ITT	CD10	2
C41	140016	470nF 10% 250V POLYPROP	RIFA	PHE 402 HFK	—
C42	140016	470nF 10% 250V POLYPROP	RIFA	PHE 402 HFK	—
C43	140016	470nF 10% 250V POLYPROP	RIFA	PHE 402 HFK	—
C44	140016	470nF 10% 250V POLYPROP	RIFA	PHE 402 HFK	—
C45	102270	27pF 5% 500V CER DISC	ITT	CD10	—
C46	140016	470nF 10% 250V POLYPROP	RIFA	PHE 402 HFK	—

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DRAWING NUMBER 400444 / 400444A — SHEET 9 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C47	140016	470nF 10% 250V POLYPROP	RIFA	PHE 402 HFK	—
C48	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C49	150020	10µF 20% 25V DIP TANT	UNION CARBIDE	K10E25	—
C50	150020	10µF 20% 25V DIP TANT	UNION CARBIDE	K10E25	—
C51	140051 *	10nF 20% 400V POLYPROP	WIMA	MKP10	1
C52	110035	220nF 20% 63V POLYESTER	WIMA	MKS2	1
C53	140016	470nF 10% 250V POLYPROP	RIFA	PHE 402 HFK	—
C54	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	2
C55	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	—
C56	110039	470nF 20% 63V POLYESTER	WIMA	MKS2	2
C57	110039	470nF 20% 63V POLYESTER	WIMA	MKS2	—
C58	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	K1R0E35	—
C59	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C60	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C61	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C62	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C63	180021	3µ3F 63V AL ELECT	MULLARD	015-18338	2
C64	180021	3µ3F 63V AL ELECT	MULLARD	015-18338	—
C65	102221	220pF 10% 500V CER DISC	ITT	CD10	1

NOTES. * ALTERNATIVE 140044 STEATITE MKP1841.

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DRAWING NUMBER 400444 400444A SHEET 10 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D1	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	5
D2	210120	12V 400mW ZENER	MULLARD	BZY88C12	1
D3	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	—
D4	210043	4V3 400mW ZENER	MULLARD	BZY88C4V3	1
D5	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	—
D6	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	—
D7	213009	15V 5W ZENER	UNITRODE	TVS 515	4
D8	213009	15V 5W ZENER	UNITRODE	TVS 515	—
D9	213009	15V 5W ZENER	UNITRODE	TVS 515	—
D10	200008	200mA 125V LL Si DIODE	FAIRCHILD	1N458A	1
D11	213009	15V 5W ZENER	UNITRODE	TVS515	—
D12	200002	1A 50V GP Si DIODE	FAIRCHILD	1N4001	1
D13	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	—
D14	210062	6V2 400mW ZENER	MULLARD	BZY88C6V2	2
D15	210062	6V2 400mW ZENER	MULLARD	BZY88C6V2	—
D16	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	4
D17	210150	15V 400mW ZENER	MULLARD	BZY88C15	1
D18	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	—
D19	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	-
D20	200001	75mA 75V GP Si DIODE	FAIRCHILD	1N4148	-

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DRAWING NUMBER 400444 400444A SHEET 11 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q1	250004	Si PNP TRANSISTOR	NATIONAL	2N3906/TO18	12
Q2	240006	Si NPN "	NATIONAL	2N3904/TO18	13
Q3	250004	Si PNP "	NATIONAL	2N3906/TO18	—
Q4	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q5	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q6	250004	Si PNP "	NATIONAL	2N3906/TO18	—
Q7	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q8	250004	Si PNP "	NATIONAL	2N3906/TO18	—
Q9	250004	Si PNP "	NATIONAL	2N3906/TO18	—
Q10	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q11	250004	Si PNP "	NATIONAL	2N3906/TO18	—
Q12	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q13		NOT USED			—
Q14		NOT USED			—
Q15		NOT USED			—
Q16		NOT USED			—
Q17		NOT USED			—
Q18		NOT USED			—
Q19	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q20	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q21	250004	Si PNP "	NATIONAL	2N3906/TO18	—
Q22	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q23	250004	Si PNP "	NATIONAL	2N3906/TO18	—

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TITLE 4000 4000A REF. DIVIDER PCB. ASSY.

DRAWING NUMBER 400444 400444A

SHEET 12 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q24	240006	Si NPN TRANSISTOR	NATIONAL	2N3904/TO18	—
Q25	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q26	250004	Si PNP "	NATIONAL	2N3906/TO18	—
Q27	240006	Si NPN "	NATIONAL	2N3904/TO18	—
Q28	250004	Si PNP "	NATIONAL	2N3906/TO18	—
Q29	230039	P-CHAN JFET	SILICONIX	J175	2
Q30	230039	P-CHAN JFET	SILICONIX	J175	—
Q31	230038	N-CHAN JFET	SILICONIX	J112	1
Q32 *	239037-1	N-CHAN JFET SEL SET	DATRON (SEE DRG)	J108 (COLOUR)	1 SET OF 4
Q33	230048	P-CHAN J FET	TELEDYNE	J174	2
Q34 *	239037-1	N-CHAN JFET SEL SET	DATRON (SEE DRG)	J108 (COLOUR)	—
Q35 *	239037-1	N-CHAN JFET SEL SET	DATRON (SEE DRG)	J108 (COLOUR)	—
Q36	230048	P-CHAN J FET	TELEDYNE	J174	—
Q37 *	239037-1	N-CHAN JFET SEL SET	DATRON (SEE DRG)	J108 (COLOUR)	—
Q38		NOT USED			
Q39		NOT USED			
Q40	250004	Si PNP	NATIONAL	2N3906/TO18	—
Q41	230031	N-CHAN DUAL JFET	TELEDYNE	SU2656M	3
Q42	230031	N-CHAN DUAL JFET	TELEDYNE	SU2656M	—
Q43	250004	Si PNP	NATIONAL	2N3906/TO18	—
Q44	230031	N-CHAN DUAL JFET	TELEDYNE	SU2656M	—
Q45	240006	Si NPN	NATIONAL	2N3904/TO18	—
Q46	230042	N-CHAN CURRENT LIM. 3mA	TELEDYNE	TCR510	2

NOTES. * THESE 4 FETS MUST HAVE THE SAME COLOUR CODING

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TITLE 4000 4000A REF. DIVIDER PCB. ASSY.

DRAWING NUMBER 400444 400444A

SHEET 13 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q47	230042	N-CHAN CURRENT LIM 3mA	TELEDYNE	TCR510	—
Q48	250021	Si PNP TRANSISTOR	MOTOROLA	BD140	1
Q49	240031	Si NPN TRANSISTOR	MOTOROLA	BD139	1
Q50	240024	Si NPN TRANSISTOR	NATIONAL	TIP31A	1
M1	220027	HIGH CMR OPTO ISOL.	HP	HCPL-2601(5082-4361)	7
M2	220027	HIGH CMR OPTO ISOL.	HP	HCPL-2601(5082-4361)	—
M3	220027	HIGH CMR OPTO ISOL	HP	HCPL-2601(5082-4361)	—
M4	220017	2k5V DUAL OPTO ISOLATOR	FAIRCHILD	FCD 880	1
M5		NOT USED			—
M6	220027	HIGH CMR OPTO ISOL.	HP	HCPL-2601 (5082-4361)	—
M7	220027	HIGH CMR OPTO ISOL.	HP	HCPL-2601 (5082-4361)	—
M8	220027	HIGH CMR OPTO ISOL.	HP	HCPL-2601 (5082-4361)	—
M9	220027	HIGH CMR OPTO ISOL	HP	HCPL-2601 (5082-4361)	—
M10	280068	DUAL PRECISION MONOSTABLE	MOTOROLA	MC14538 BCP	1
M11	280037	HEX BUFFER	MOTOROLA	MC14050BCP	1
M12	260025	101 OP AMP	NATIONAL	LM101AH	3
M13	280011	DUAL-D FLIP.FLOP	MOTOROLA	MC14013 BCP	2
M14	280009	HEX INVERTER/BUFFER	MOTOROLA	MC14049 BCP	1
M15	280089	8 BIT SHIFT REGISTER	MOTOROLA	MC14094 BCP	6
M16	260025	101 OP AMP	NATIONAL	LM101 AH	—
M17		NOT USED			—

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DRAWING NUMBER 400444 400444A SHEET 14 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M18	280088	8 BIT STATIC SHIFT REGISTER	MOTOROLA	MC14021 BCP	2
M19	280089	8 BIT STATIC SHIFT REGISTER	MOTOROLA	MC14094 BCP	—
M20	260025	101 OP AMP	NATIONAL	LM101	—
M21	260028	1458 DUAL OP AMP	FAIRCHILD	µA1458 CTC	1
M22	280088	8 BIT STATIC SHIFT REGISTER	MOTOROLA	MC14021 BCP	—
M23	260027	714 OP AMP	FAIRCHILD	µA 714 HC	4
M24	280023	QUAD 2I/P NOR GATE	MOTOROLA	MC14001 BCP	1
M25	280089	8 BIT STATIC SHIFT REGISTER	MOTOROLA	MC14094 BCP	—
M26	260057	5534 OP AMP	SIGNETICS	NE5534N	2
M27	280089	8 BIT STATIC SHIFT REGISTER	MOTOROLA	MC14094 BCP	—
M28	260057	5534 OP AMP	SIGNETICS	NE5534N	—
M29	290090	7X DARLINGTON DRIVER	SPRAGUE/EXAR	ULN2002A/XR2202CP	1
M30	280089	8 BIT STATIC SHIFT REGISTER	MOTOROLA	MC14094 BCP	—
M31	280089	8 BIT STATIC SHIFT REGISTER	MOTOROLA	MC14094 BCP	—
M32	260027	714 OP AMP	FAIRCHILD	µA 714 HC	—
M33	260053	7650 OP AMP	INTERSIL	ICL7650 CPD	1
M34	260027	714 OP AMP	FAIRCHILD	µA 714 HC	—
M35	260027	714 OP AMP	FAIRCHILD	µA 714 HC	—
M36	280106	HEX LEVEL SHIFTER	MOTOROLA	MC14504 BCP	1
M37	280011	DUAL D FLIP FLOP	MOTOROLA	MC14013 BCP	—

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TITLE 4000 4000A REF DIVIDER PCB ASSY.

DRAWING NUMBER 400444 400444A SHEET 15 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
RL1	330018	RELAY 2P2W 7V HOLD-IN	AMF	SEE DRG	1
RL2	330019	RELAY 4P2W 7V HOLD-IN	AMF	SEE DRG	1
L1 - L7	370001	10μH 0.85Ω RF CHOKE	PLESSEY	58/10/0011/10	7
T1-T5	310002	PULSE Tx	NEWPORT	76616/4 HV	5
S1	700070	SLIDE SWITCH. EXTRA HI. LEVER	APR	25446A H6	1
	SEE TABLE	REF PCB ASSY			1
	410157-5	PCB			1
	459112	RELAY BRACKET			2
	540008	7/.2 PTFE COVERED WIRE			790mm
	540002	22SWG BTC WIRE			A/R
	590001	SLEEVE. MAXCABLE ⌀ 3.0	HELLERMANN ELECTRIC	H15X20mm BLACK HELSYN	15
	602001	FSV TERMINAL	MOLEX	02-04-5114	10
	605059	8WAY DIL. SOCKET			14
	605060	14 WAY DIL. SOCKET			4
	605061	16 WAY DIL. SOCKET			13
	611016	SCREW M3x8mm STEEL POZI-PAN	ZINC PLATED GKN		5
	604053	4 WAY ·1" PCB PLUG GD. PL.	MOLEX	4030-04 AG (·825" PINS)	2
	612004	STANDOFF M3x4mm BRASS	HARWIN	CS2116/B	1

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

INSTRUMENT	REF. DIV. ASSY.	REF. ASSY.
4000	400444	400452
4000A	400444A	400452A

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TITLE 4000 4000A REF. DIVIDER PCB. ASSY.

DRAWING NUMBER 400444 400444A SHEET 16 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	613005	WASHER M3 INT/SHAKEPROOF	STEEL. ZN/PLATED GKN		3
	613014	WASHER M2.5 INT/SHAKEPROOF	STEEL ZN/PLATED GKN		2
	613029	M3 CRINKLE WASHER SS.			2
	615005	NUT 3-48UNC FULL HEX-STEEL	ZINC PLATED GKN		2
	615002	NUT M3 FULL HEX STEEL	ZINC PLATED GKN		3
	620003	SOLDER PCB TERMINAL LUG	HARWIN	H2105A	16
	630024	STANDARD STEATITE INS. BEAD	PARK ROYAL PORCELAIN CO.	TYPE No 2 (16 SWG)	4
	630118	CIRCUIT BOARD EJECTOR	RICHCO	CBE RED	2
	620007	TEST POINT TERMINAL	MICROVAR	C30	26

NOTES.

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TITLE 4000 4000A REF. DIVIDER PCB. ASSY.

DRAWING NUMBER 400444 400444A SHEET 17 OF 17

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	1
R2	000103	10k 5% 1/4W CARBON	MULLARD	CR25	8
R3	000105	1M 5% 1/4W CARBON	MULLARD	CR25	4
R4	000105	1M 5% 1/4W CARBON	MULLARD	CR25	–
R5	000105	1M 5% 1/4W CARBON	MULLARD	CR25	–
R6	000105	1M 5% 1/4W CARBON	MULLARD	CR25	–
R7	000153	15k 5% 1/4W CARBON	MULLARD	CR25	1
R8	041005	10M0 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	8
R9	041005	10M0 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	–
R10	SEE TABLE	1M MATCHED SET	MANN	SEE DRG	1
R11	019091	9k09 1% 1/8W 50ppm MF	HOLCO	H8C	3
R12	012372	23k7 1% 1/8W 50ppm MF	HOLCO	H8C	2
R13	000562	5k6 5% 1/4W CARBON	MULLARD	CR25	2
R14	000106	10M 5% 1/4W CARBON	MULLARD	CR25	3
R15	000106	10M 5% 1/4W CARBON	MULLARD	CR25	–
R16	000682	6k8 5% 1/4W CARBON	MULLARD	CR25	1
R17	019091	9k09 1% 1/8W 50ppm MF	HOLCO	H8C	–
R18	012372	23k7 1% 1/8W 50ppm MF	HOLCO	H8C	–
R19	000273	27k 5% 1/4W CARBON	MULLARD	CR25	3
R20	000273	27k 5% 1/4W CARBON	MULLARD	CR25	–
R21	000222	2k2 5% 1/4W CARBON	MULLARD	CR25	2
R22	013403	340K 1% 1/8W 50ppm MF	HOLCO	H8C	1
R23	000562	5k6 5% 1/4W CARBON	MULLARD	CR25	–

NOTES.

INSTRUMENT	DC. ASSY	R10. 27. 48. 66. 89. 96.	R74	R75
4000	400445	090057/B-1	090058/B-1	090059/B-1
4000A	400445A	090057/A-1	090058/A-1	090059/A-1

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ISS.	1	2	3	4	5
E.C.O.	RELEASED	1376/85	1432	1440/44	1478/83
DATE	25.6.82	25.8.82	15.12.82	11.2.83	3.6.83
CHKD.		ND	ND	ND	ND

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DATE 2.7.82

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TITLE 4000 4000A DC PCB ASSY.

DRAWING NUMBER 400445 400445A

SHEET 2 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	000222	2k2 5% 1/4W CARBON	MULLARD	CR25	–
R25	041005	10M0 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	–
R26	041005	10M0 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	–
R27	SEE TABLE	1M MATCHED SET	MANN	SEE DRG	–
R28		NOT USED			
R29	050058	18M 1% 1W 7K5V MF	HOLCO	H801RE	1
R30	000103	10k 5% 1/4W CARBON	MULLARD	CR25	–
R31	000103	10k 5% 1/4W CARBON	MULLARD	CR25	–
R32	012378	23R7 1% 1/8W 50ppm MF	HOLCO	H8C	1
R33	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	2
R34	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	–
R35	000273	27k 5% 1/4W CARBON	MULLARD	CR25	–
R36	012261	2k26 1% 1/8W 50ppm MF	HOLCO	H8C	2
R37	012261	2k26 1% 1/8W 50ppm MF	HOLCO	H8C	–
R38	000102	1k 5% 1/4W CARBON	MULLARD	CR25	8
R39	000104	100k 5% 1/4W CARBON	MULLARD	CR25	3
R40	000228	2R2 5% 1/4W CARBON	MULLARD	CR25	2
R41	050055	10k0 ·5% 1/8W 50ppm MF	HOLCO	H8	4
R42	050055	10k0 ·5% 1/8W 50ppm MF	HOLCO	H8	–
R43	050055	10k0 ·5% 1/8W 50ppm MF	HOLCO	H8	–
R44	050055	10k0 ·5% 1/8W 50ppm MF	HOLCO	H8	–
R45	000101	100R 5% 1/4W CARBON	MULLARD	CR25	1
R46	041005	10M0 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	–

NOTES.

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TITLE 4000 4000A DC PCB ASSY

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SHEET 3 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R47	041005	10M0 1% ½W 100ppm CF	ALLEN BRADLEY	CC	–
R48	SEE TABLE	1M MATCHED SET	MANN	SEE DRG	–
R49		NOT USED			
R50		NOT USED			
R51	000912	9k1 5% ¼W CARBON	MULLARD	CR25	1
R52	011502	15k0 1% ⅛W 50ppm MF	HOLCO	H8C	2
R53	019091	9k09 1% ⅛W 50ppm MF	HOLCO	H8C	–
R54	070148	90k0 ·1% 10ppm WW	MANN	MX125	1
R55	070066	10k ·1% 5ppm WW	MANN	MX125B	1
R56	012748	27R4 1% ⅛W 50ppm MF	HOLCO	H8C	2
R57	000102	1k 5% ¼W CARBON	MULLARD	CR25	–
R58	011502	15k0 1% ⅛W 50ppm MF	HOLCO	H8C	–
R59	019531	9k53 1% ⅛W 50ppm MF	HOLCO	H8C	1
R60	000102	1k 5% ¼W CARBON	MULLARD	CR25	–
R61	000228	2R2 5% ¼W CARBON	MULLARD	CR25	–
R62	012748	27R4 1% ⅛W 50ppm MF	HOLCO	H8C	–
R63	000102	1k 5% ¼W CARBON	MULLARD	CR25	–
R64	041005	10M0 1% ½W 100ppm CF	ALLEN BRADLEY	CC	–
R65	041005	10M0 1% ½W 100ppm CF	ALLEN BRADLEY	CC	–
R66	SEE TABLE	1M MATCHED SET	MANN	SEE DRG	–
R67		NOT USED			–
R68		NOT USED			–
R69		NOT USED			–

NOTES.

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TITLE 4000 4000A DC PCB ASSY.

DRAWING NUMBER 400445 400445A SHEET 4 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R70		NOT USED			–
R71		NOT USED			–
R72		NOT USED			–
R73		NOT USED			–
R74	SEE TABLE	90k/10k	MANN	SEE DRG	1
R75	SEE TABLE	1k/111R11	MANN	SEE DRG	1
R76		NOT USED			–
R77	000102	1k 5% ¼W CARBON	MULLARD	CR25	–
R78	000473	47k 5% ¼W CARBON	MULLARD	CR25	4
R79	000103	10k 5% ¼W CARBON	MULLARD	CR25	–
R80	000102	1k 5% ¼W CARBON	MULLARD	CR25	–
R81	011001	1k00 1% ⅛W 50ppm MF	HOLCO	H8C	1
R82	000393	39k 5% ¼W CARBON	MULLARD	CR25	4
R83	011302	13k0 1% ⅛W 50ppm MF	HOLCO	H8C	4
R84	011302	13k0 1% ⅛W 50ppm MF	HOLCO	H8C	–
R85	000393	39k 5% ¼W CARBON	MULLARD	CR25	–
R86	012001	2k00 1% ⅛W 50ppm MF	MULLARD	CR25	4
R87	012001	2k00 1% ⅛W 50ppm MF	MULLARD	CR25	–
R88	008040	20M 5% 2500V MET-GLAZE	MULLARD	VR37	1
R89	SEE TABLE	1M MATCHED SET	MANN	SEE DRG	–
R90		NOT USED			
R91		NOT USED			
R92	000183	18k 5% ¼W CARBON	MULLARD	CR25	1

NOTES.

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TITLE 4000 4000A DC PCB ASSY

DRAWING NUMBER 400445 400445A SHEET 5 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R93	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R94	000202	2k 5% 1/4W CARBON	MULLARD	CR25	1
R95	041825	18M2 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	1
R96	SEE TABLE	900k/ 100k MATCHED SET	MANN	SEE DRG	—
R97	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—
R98	041824	1M82 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	1
R99		NOT USED			—
R100	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R101	011003	100k 1% 1/8W 50ppm MF	HOLCO	H8C	3
R102	011003	100k 1% 1/8W 50ppm MF	HOLCO	H8C	—
R103	011003	100k 1% 1/8W 50ppm MF	HOLCO	H8C	—
R104	000473	47k 5% 1/4W CARBON	MULLARD	CR25	—
R105	000393	39k 5% 1/4W CARBON	MULLARD	CR25	—
R106	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—
R107	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R108	012001	2k00 1% 1/8W 50ppm MF	HOLCO	H8C	—
R109	011302	13k0 1% 1/8W 50ppm MF	HOLCO	H8C	—
R110	011302	13k0 1% 1/8W 50ppm MF	HOLCO	H8C	—
R111	012001	2k00 1% 1/8W 50ppm MF	HOLCO	H8C	—
R112	000473	47k 5% 1/4W CARBON	MULLARD	CR25	—
R113	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R114	000473	47k 5% 1/4W CARBON	MULLARD	CR25	—
R115	000393	39k 5% 1/4 CARBON	MULLARD	CR25	—

NOTES.

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TITLE 4000 4000A DC PCB ASSY

DRAWING NUMBER 400445 400445A SHEET 6 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R116	000106	10M 5% 1/4W CARBON	MULLARD	CR25	—
R117	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R118	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R119	000512	5k1 5% 1/4W CARBON	MULLARD	CR25	2
R120	000512	5k1 5% 1/4W CARBON	MULLARD	CR25	—
R121	000152	1K5 5% 1/4W CARBON	MULLARD	CR25	2
R122	000152	1K5 5% 1/4W CARBON	MULLARD	CR25	—
AN1	090096	1M x 8 2% NETWORK	AB	850-91- 1M	1
AN2	090105	100R x 4 2% NETWORK	AB	850-83- 100R	1
C1	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	15
C2	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C3	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C4	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C5	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C6	180021	3μ3F 63V AL. ELECT	MULLARD	015-18338	2
C7	180021	3μ3F 63V AL. ELECT	MULLARD	015-18338	—
C8	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—
C9	104026	47nF +50 -20% 50V CER DISC	SIEMENS	B37449	—

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TITLE 4000 4000A DC PCB ASSY

DRAWING NUMBER 400445 400445A SHEET 7 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C10	110007	3μ3F 20% 100V POLYESTER	WIMA	MKS	1
C11	150016	1μF 20% 35V DIP TANT	UNION CARBIDE	KIROE35	5
C12	150016	1μF 20% 35V DIP TANT	UNION CARBIDE	KIROE35	–
C13	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	–
C14	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	–
C15	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	–
C16	110035	220nF 20% 63V POLYESTER	WIMA	MKS2	3
C17	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	–
C18	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	–
C19	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	–
C20	150020	10μF 20% 25V DIP TANT	UNION CARBIDE	K10E25	2
C21	150020	10μF 20% 25V DIP TANT	UNION CARBIDE	K10E35	–
C22	150016	1μF 20% 35V DIP TANT	UNION CARBIDE	KIROE35	–
C23	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	–
C24	104026	47nF +50/-20 % 50V CER DISC	SIEMENS	B37449	–
C25	120019	1μF 10% 63V POLYCARB	ASHCROFT	A2B1021B	1
C26	110041	10nF 20% 100V POLYESTER	WIMA	FKS2	1
C27	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	7
C28	150016	1μF 20% 35V DIP TANT	UNION CARBIDE	KIROE35	–
C29	150002	10μF 20% 16V DIP TANT	UNION CARBIDE	K10E16	2
C30	150002	10μF 20% 16V DIP TANT	UNION CARBIDE	K10E16	–
C31	110035	220nF 20% 63V POLYESTER	WIMA	MKS2	–
C32	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	–

NOTES.

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SHEET 8 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C33	140003	47nF 10% 400V POLYPROP	WIMA	MKP10	1
C34	110039	470nF 20% 63V POLYESTER	WIMA	MKS2	4
C35	110039	470nF 20% 63V POLYESTER	WIMA	MKS	–
C36	110039	470nF 20% 63V POLYESTER	WIMA	MKS2	–
C37	110039	470nF 20% 63V POLYESTER	WIMA	MKS	–
C38	110040	33nF 20% 63V POLYESTER	WIMA	MKS2	1
C39	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	–
C40	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	–
C41	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	–
C42	102101	100pF 10% 500V CER DISC	ITT	CD10	1
C43	150016	1μF 20% 35V DIP TANT	UNION CARBIDE	KIROE35	–
C44	110035	220nF 20% 63V POLYESTER	WIMA	MKS2	–
C45	120015	470pF 20% 100V POLYCARB	WIMA	FKC2MIN	1
C46	104031	2n2F +40/-20 % 2kV CER DISC	ITT	HD16	2
C47	104031	2n2F +40/-20 % 2kV CER DISC	ITT	HD16	–
C48	104032	220pF 10% 2kV CER DISC	ITT	HD09	1
C49	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	–
C50	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	–
C51	102221	220pF 10% 500V CER DISC	ITT	CD10	2
C52	102221	220pF 10% 500V CER DISC	ITT	CD10	–

NOTES.

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DRAWING NUMBER 400445 400445A

SHEET 9 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D1	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	9
D2	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	3
D3	213009	15V 5W ZENER	UNITRODE	TVS 515	4
D4	213009	15V 5W ZENER	UNITRODE	TVS515	–
D5	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	9
D6	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	–
D7	214012	2V45 30ppm ZENER	FERRANTI	ZN458	3
D8	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	–
D9	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	–
D10	220020	FET DIODE 100pA IR	TELEDYNE	PAD100/INSULATED CASE	6
D11	214012	2V45 30ppm ZENER	FERRANTI	ZN458	–
D12	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	–
D13	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	–
D14	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	–
D15	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	–
D16	220020	FET DIODE 100pA IR	TELEDYNE	PAD100/INSULATED CASE	–
D17	213009	15V 5W ZENER	UNITRODE	TVS515	–
D18	213009	15V 5W ZENER	UNITRODE	TVS515	–
D19	213006	5V 5W ZENER	UNITRODE	TVS 505	4
D20	213006	5V 5W ZENER	UNITRODE	TVS 505	–
D21	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	–
D22	210033	3V3 400mW ZENER	MULLARD	BZY88C 3V3	1
D23	213008	24V 5W ZENER	UNITRODE	TVS 524	4

NOTES.

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datron ELECTRONICS LTD

TITLE 4000 4000A DC PCB ASSY

DRAWING NUMBER 400445 400445A — SHEET 10 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D24	213008	24V 5W ZENER	UNITRODE	TVS 524	–
D25	214012	2V45 30ppm ZENER	FERRANTI	ZN458	–
D26	213008	24V 5W ZENER	UNITRODE	TVS 524	–
D27	213008	24V 5W ZENER	UNITRODE	TVS 524	–
D28	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	–
D29	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	–
D30	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	–
D31	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	–
D32	213006	5V 5W ZENER	UNITRODE	TVS 505	–
D33	213006	5V 5W ZENER	UNITRODE	TVS 505	–
D34	220020	FET DIODE 100pA IR	TELEDYNE	PAD100/INSULATED CASE	–
D35	220020	FET DIODE 100pA IR	TELEDYNE	PAD100/INSULATED CASE	–
D36	214014	1V22 100ppm ZENER	TELEDYNE	9491BJ	4
D37	214014	1V22 100ppm	TELEDYNE	9491BJ	–
D38	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	–
D39	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	–
D40	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	–
D41	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	–
D42	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	–
D43	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	–
D44	210062	6V2 400mW ZENER	MULLARD	BZY88C6V2	2
D45	210062	6V2 400mW ZENER	MULLARD	BZY88C6V2	–
D46	220020	FET DIODE 100pA IR	TELEDYNE	PAD100/INSULATED CASE	–

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TITLE 4000 4000A DC PCB ASSEMBLY

DRAWING NUMBER 400445 400445A — SHEET 11 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D47	220020	FET DIODE 100pA IR	TELEDYNE	PAD100/ INSULATED CASE	–
D48	200008	200mA 125V LL Si DIODE	FAIRCHILD	IN458A	2
D49	200008	200mA 125V LL Si DIODE	FAIRCHILD	IN458A	–
D50	214014	1V22 100ppm ZENER	TELEDYNE	9491BJ	–
D51	214014	1V22 100ppm ZENER	TELEDYNE	9491BJ	–
Q1	250004	Si PNP TRANSISTOR	NATIONAL	2N3906/TO92	1
Q2	230036	N-CHAN JFET	SILICONIX	J108	1
Q3	230042	N-CHAN CURRENT LIM	TELEDYNE	TCR510	1
Q4	250013	Si PNP TRANSISTOR	NATIONAL	BD136	1
Q5	240021	Si NPN TRANSISTOR	NATIONAL	BD135	1
Q6	230031	N-CHAN DUAL JFET	TELEDYNE	SU2656M	2
Q7	250025	Si PNP TRANSISTOR	MOTOROLA	MJE350	1
Q8	230001	N-CHAN CURRENT LIM.	TELEDYNE	TCR506	2
Q9	230001	N-CHAN CURRENT LIM	TELEDYNE	TCR506	–
Q10	240018	Si NPN TRANSISTOR	MOTOROLA	MJE340	1
Q11	230031	N-CHAN DUAL JFET	TELEDYNE	SU2656M	–

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TITLE 4000 4000A DC PCB ASSY

DRAWING NUMBER 400445 400445A

SHEET 12 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M1	290090	7x DARLINGTON DRIVER	SPRAGUE / EXAR	ULN2002A/XR2202CP	2
M2	290090	7x DARLINGTON DRIVER	SPRAGUE/ EXAR	ULN2002A/XR2202CP	–
M3	280079	QUAD 2 I/P OR GATE	MOTOROLA	MC14071 BCP	1
M4	280090	DUAL BINARY TO 1OF4 DECODE	MOTOROLA	MC14555BCP	1
M5	280045	TRIPLE 3 I/P NOR GATE	MOTOROLA	MC14025BCP	1
M6	280085	QUAD 2 I/P AND GATE	MOTOROLA	MC14081 BCP	1
M7	280009	HEX INVERTER	MOTOROLA	MC14049BCP	1
M8	260039	324 QUAD OP AMP	NATIONAL	LM324N	1
M9	260050	412 DUAL FET I/P OP AMP	NATIONAL	LF412N	2
M10	260050	412 DUAL FET I/P OP AMP	NATIONAL	LF412N	–
M11	260057	5534 OP AMP	SIGNETICS	NE5534N	1
M12	260042	5532 DUAL OP AMP	SIGNETICS	NE5532N	1
M13	260069	411 OP AMP	NATIONAL	LF411CH	1
M14	260043	358 DUAL OP AMP	NATIONAL	LM358N	1
M15	260059	0002 BUFFER AMP	NATIONAL	LH0002CH	1
M16	260053	7650 OP AMP	INTERSIL	ICL7650 CPD	2
M17	260027	714 OP AMP	FAIRCHILD	µA714 HC	3
M18	260027	714 OP AMP	FAIRCHILD	µA714 HC	–
M19	260027	714 OP AMP	FAIRCHILD	µA714 HC	–
M20	260053	7650 OP AMP	INTERSIL	ICL7650 CPD	–

NOTES.

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TITLE 4000 4000A DC PCB ASSY

DRAWING NUMBER 400445 400445A

SHEET 13 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
RL1	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	9
RL2	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	–
RL3	330019	RELAY 4P2W 5V HOLD-IN	AMF	SEE DRG	6
RL4	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	–
RL5	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	–
RL6	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	–
RL7	330019	RELAY 4P2W 5V HOLD-IN	AMF	SEE DRG	–
RL8	330019	RELAY 4P2W 5V HOLD-IN	AMF	SEE DRG	–
RL9	330019	RELAY 4P2W 5V HOLD-IN	AMF	SEE DRG	–
RL10	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	–
RL11	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	–
RL12	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	–
RL13	330019	RELAY 4P2W 5V HOLD-IN	AMF	SEE DRG	–
RL14	330019	RELAY 4P2W 5V HOLD-IN	AMF	SEE DRG	–
RL15	330018	RELAY 2P2W 5V HOLD-IN	AMF	SEE DRG	–
L1 – L6	370001	10µH 0.85Ω RF CHOKE	PLESSEY	58/10/0011/10	6

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TITLE 4000 / 4000A DC PCB ASSY

DRAWING NUMBER 400445 / 400445A SHEET 14 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
F1	920120	1A PICOFUSE	LITTLEFUSE	275 001	6
F2	920120	1A PICOFUSE	LITTLE FUSE	275 001	–
F3	920120	1A PICOFUSE	LITTLEFUSE	275 001	–
F4	920120	1A PICOFUSE	LITTLEFUSE	275 001	–
F5	920120	1A PICOFUSE	LITTLEFUSE	275 001	–
F6	920120	1A PICOFUSE	LITTLEFUSE	275 001	–
	410159-6	PCB		SEE DRG	1
	459112-2	RELAY BRACKET		SEE DRG	15
	540002	22SWG TINNED CU WIRE			A/R
	590001	SLEEVE MAX CABLE ϕ 3.0	HELLERMANN ELECTRIC	HIS x 20mm BLK. HELSYN	91
	540008	7/0.2 PTFE INSULATED WIRE		1kVrms To BS G210 TYPE C	2770 mm
	590004	SLEEVE – PTFE	HELLERMANN ELECTRIC	FE10	A/R
	605059/A	8 WAY DIL SOCKET			7
	605060/A	14 WAY DIL SOCKET			6
	605061/A	16 WAY DIL SOCKET			4
	611016	SCREW M3x8mm STEEL POZIPAN	ZINC PLATED GKN		15
	615002	NUT M3 FULL HEX STEEL	ZINC PLATED GKN		15
	613005	WASHER M3 SHAKEPROOF STEEL	ZINC PLATED GKN		15
	615005	NUT 3-48UNC FULL HEX STEEL	ZINC PLATED		15
	618004	TRANSISTOR MTG PAD FOR TO18	JERMYN	TO18-008D	5

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TITLE 4000 / 4000A DC PCB ASSY

DRAWING NUMBER 400445 / 400445A SHEET 15 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	620003	SOLDER PIN TERM^L LUG	HARWIN	H2105A	56
	630024	STEATITE BEAD 16 SWG	PARK ROYAL PORCELAIN	Nº 2	34
	630036	STEATITE BEAD 18 SWG	PARK ROYAL PORCELAIN	Nº 1	30
	630119	CCT BOARD EJECTOR	RICHCO	CBE ORANGE	2
	630132	POLYAMIDE TAPE	3M	5413	A/R
	620007	TEST POINT TERMINAL	MICROVAR	C 30	12
	613014	WASHER M2·5 SHAKEPROOF	STEEL. ZN. PLATED GKN		15

NOTES.

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TITLE 4000 4000A DC PCB ASSY

DRAWING NUMBER 400445 400445A

SHEET 16 OF 16

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	NOT USED				
R2	000820	82R 5% 1/4W CARBON	MULLARD	CR25	1
R3	000821	820R 5% 1/4W CARBON	MULLARD	CR25	1
R4	000822	8K2 5% 1/4W CARBON	MULLARD	CR25	1
R5	008002	4R7 5% 2½W WIREWOUND	WELWYN	W21	1
R6	000103	10K 5% 1/4W CARBON	MULLARD	CR25	3
R7	000103	10K 5% 1/4W CARBON	MULLARD	CR25	—
R8	080019-3	95R000 0·1% M FOIL	VISHAY	SEE DRG.	1
R9	080020-3	900R0 0·1% M FOIL	VISHAY	SEE DRG.	1
R10	080021-3	9K000 0·1% M FOIL	VISHAY	SEE DRG.	1
R11	000101	100R 5% 1/4W CARBON	MULLARD	CR25	8
R12	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R13	000393	39K 5% 1/4W CARBON	MULLARD	CR25	2
R14	000473	47K 5% 1/4W CARBON	MULLARD	CR25	4
R15	000473	47K 5% 1/4W CARBON	MULLARD	CR25	-
R16	000473	47K 5% 1/4W CARBON	MULLARD	CR25	-
R17	000473	47K 5% 1/4W CARBON	MULLARD	CR25	-
R18	012001	2K00 1% 1/8W 50ppm MF	HOLCO	HBC	2
R19	012001	2K00 1% 1/8W 50ppm MF	HOLCO	HBC	—
R20	011302	13K0 1% 1/8W 50ppm MF	HOLCO	HBC	2
R21	011302	13K0 1% 1/8W 50ppm MF	HOLCO	HBC	-
R22	000393	39K 5% 1/4W CARBON	MULLARD	CR25	-
R23	067202	2K POT 20TURN CERMET	BECKMAN	68X	1

NOTES.

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E.C.O.	RELE'6D	1434,36	1450	1481	1490,91	1529	1537
DATE	6.10.82	15-12-82	17-2-83	9.5.83	7.6.83	15.9.83	29.9.83
CHKD.		MD	MD	MD	MD	MD	MD

DATE 3.5.83 — DRAWN IL — CHKD MD — APPROVED — DATE 5.0.82

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TITLE 4000 I/Ω PCB ASSEMBLY.

DRAWING NUMBER 400448 — SHEET 3 OF 15

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R25	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R26	011001	1K00 1% 1/8W 50ppm MF	HOLCO	HBC	2
R27	012670	267R 1% 1/8W 50ppm MF	HOLCO	HBC	1
R28	011001	1K00 1% 1/8W 50ppm MF	HOLCO	HBC	-
R29	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R30	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R31	NOT USED				
R32	000472	4K7 5% 1/4W CARBON	MULLARD	CR25	1
R33	000103	10K 5% 1/4W CARBON	MULLARD	CR25	-
R34	000102	1K0 5% 1/4W CARBON	MULLARD	CR25	3
R35	000102	1K0 5% 1/4W CARBON	MULLARD	CR25	-
R36	NOT USED				
R37	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R38	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R39	013401	3K40 1% 1/8W 50ppm MF	HOLCO	HBC	1
R40	012002	20K0 1% 1/8W 50ppm MF	HOLCO	HBC	1
R41	000104	100K 5% 1/4W CARBON	MULLARD	CR25	1
R42		NOT USED			
R43	090089-2	10K000 RESISTOR SET.		SEE DRG.	1 SET
R44		90K00 RESISTOR SET.		SEE DRG.	
R45	NOT USED				
R46	NOT USED				

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TITLE '4000' I/Ω PCB ASSEMBLY

DRAWING NUMBER 400448 — SHEET 4 OF 15

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R47	NOT USED				
R48	NOT USED				
R49	000100	10R 5% 1/4W CARBON	MULLARD	CR25	2
R50	000100	10R 5% 1/4W CARBON	MULLARD	CR25	-
R51	000105	1M 5% 1/4W CARBON	MULLARD	CR25	1
R52	000153	15K 5% 1/4W CARBON	MULLARD	CR25	1
R53	067201	200R POT 20TURN CERMET	BECKMAN	68X	1
R54	067502	5K POT 20TURN CERMET	BECKMAN	68X	1
R55	067503	50K POT 20TURN CERMET	BECKMAN	68X	1
R56	067504	500K POT 20TURN CERMET	BECKMAN	68X	1
R57	067205	2M POT 20TURN CERMET	BECKMAN	68X	1
R58	067100	10R POT 20TURN CERMET	BECKMAN	68X	1
R59	000102	1K 5% 1/4W CARBON	MULLARD	CR25	-
R60	041585	15M8 1% 1/2W 100ppm CF.	ALLEN BRADLEY	CC	1
R61	011508	15R0 1% 1/8W 50ppm MF	HOLCO	HBC	1
R62	070134 - 3	99K980 50ppm WIREWOUND	MANN	SEE DRG.	1
R63	070133 - 3	10K0060 50ppm WIREWOUND	MANN	SEE DRG.	1
R64	070132 - 3	1K00040 50ppm WIREWOUND	MANN	SEE DRG.	1
R65	070131 - 3	100R040 50 " WIREWOUND	MANN	SEE DRG.	1
R66	012263	226K 1% 1/8W 50ppm MF	HOLCO	HBC	1
R67		NOT USED			
R68	042264	2M26 1% 1/2W 100ppm CF	ALLEN BRADLEY	CC	1
R69	011581	1K58 1% 1/8W 50ppm MF	HOLCO	HBC	1

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TITLE '4000' I/Ω PCB ASSEMBLY.

DRAWING NUMBER 400448 SHEET 5 OF 15

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R70	012262	22K6 1% 1/8W 50ppm MF	HOLCO	HBC.	1
R71	070129 - 3	1R00060 50ppm WIREWOUND	MANN	SEE DRG.	1
R72	070130 - 3	10R0040 50ppm WIREWOUND	MANN	SEE DRG.	1
R73	070136 - 3	9M9940 50ppm WIREWOUND	MANN	SEE DRG.	1
R74	070135 - 3	999K70 50ppm WIREWOUND	MANN	SEE DRG.	1
R75	014991	4K99 1% 1/8W 50ppm MF	HOLCO	HBC.	1
R76	012000	200R 1% 1/8W 50ppm MF	HOLCO	HBC.	1
R77	064201	200R POT 15TURN CERMET	BECKMAN	89P	1
R78	064202	2K POT 15TURN CERMET	BECKMAN	89P	1
R79	080023 - 3	5R000	VISHAY	SEE DRG	1
R80	400510	0R100 SHUNT ASSY	DATRON	SEE DRG	1
R81	000222	2K2 5% 1/4W CARBON	MULLARD	CR25	1
AN1	090096	1M x 8 2% NETWORK	A B	850-91-1M	2
AN2	090085	12K x 8 2% NETWORK	A B	761-3-12K	1
AN3	090096	1M x 8 2% NETWORK	A B	850-91-1M	-

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TITLE '4000' I/Ω PCB ASSEMBLY

DRAWING NUMBER 400448 SHEET 6 OF 15

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	16
C2	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C3	150002	10µF 20% 16V DIP TANT	UNION CARBIDE	KIOE16	1
C4	110035	220nF 20% 63V POLYESTER	WIMA	MKS2	1
C5	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C6	NOT USED				
C7	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C8	NOT USED				
C9	NOT USED				
C10	NOT USED				
C11	NOT USED				
C12	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C13	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	KIROE35	2
C14	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C15	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	2
C16	110042	100nF 20% 63V POLYESTER	WIMA	MKS2	-
C17	110026	6n8F 20% 100V POLYESTER	WIMA	FKS2	2
C18	110026	6n8F 20% 100V POLYESTER	WIMA	FKS2	-
C19	150020	10µF 20% 25V DIP TANT	UNION CARBIDE	KIOE25	4
C20	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C21	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C22	150004	100µF 20% 6V3 DIP TANT	UNION CARBIDE	K100E6V3	1
C23	150020	10µF 20% 25V DIP TANT	UNION CARBIDE	KIOE25	-

NOTES.

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DATE	DRAWING NUMBER 400448	SHEET 7 OF 15

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C24	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C25	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C26	150020	10µF 20% 25V DIP TANT	UNION CARBIDE	KIOE25	-
C27	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C28	150020	10µF 20% 25V DIP TANT	UNION CARBIDE	KIOE25	-
C29	150005	2µ2F 20% 16V DIP TANT	UNION CARBIDE	K2R2E16	2
C30	150005	2µ2F 20% 16V DIP TANT	UNION CARBIDE	K2R2E16	-
C31	102100	10pF 5% 500V CER DISC	ITT	CD10	2
C32	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	KIROE35	-
C33	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C34	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C35	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C36	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	2
C37	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	-
C38	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C39	104026	47nF $^{+50\%}_{-20\%}$ 50V CER DISC	SIEMENS	B37449	-
C40	NOT USED				
C41	140054	1 nF 20% 1kV DC 400V AC POLY PROP	WIMA	FKP1	2
C42	140054	1 nF 20% 1kV DC 400V AC POLY PROP	WIMA	FKP1	-
C43	102101	100pF 10% 500V CER DISC	ITT	CD10	1
C44	102100	10pF 5% 500V CER DISC	ITT	CD10	-
C45	150022	2µ2F 20% 35V DIP TANT	UNION CARBIDE	K2R2E35	1

NOTES.

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DATE	DRAWING NUMBER 400448	SHEET 8 OF 15

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D1	200002	1A 50V GP Si DIODE	FAIRCHILD	IN4001	1
D2	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	1
D3	210056	5V6 400mW ZENER	MULLARD	BZY88C5V6	2
D4	210056	5V6 400mW ZENER	MULLARD	BZY88C5V6	-
D5	213012	2V0 250mW ZENER	MULLARD	BZV46-2V0	1
D6	210033	3V3 400mW ZENER	MULLARD	BZY88C3V3	1
D7	213009	15V 5W ZENER	UNITRODE	TVS515.	4
D8	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	3
D9	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	-
D10	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	-
D11	213009	15V 5W ZENER	UNITRODE	TVS515	-
D12	213009	15V 5W ZENER	UNITRODE	TVS515	-
D13	213009	15V 5W ZENER	UNITRODE	TVS515	-
D14	NOT USED.				
D15	NOT USED.				
D16	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	2
D17	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	-
D18	213006	5V 5W ZENER	UNITRODE	TVS505	2

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TITLE '4000' I/Ω PCB ASSEMBLY

DRAWING NUMBER 400448 SHEET 9 OF 15

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D19	213006	5V 5W ZENER	UNITRODE	TVS 505	-
Q1	250004	Si PNP TRANSISTOR	NATIONAL	2N3906 / TO92	3
Q2	230001	N-CHAN I LIM 1·4mA	TELEDYNE	TCR506	3
Q3	250004	Si PNP TRANSISTOR	NATIONAL	2N3906 / TO92	-
Q4	230001	N-CHAN I LIM 1·4mA	TELEDYNE	TCR506	-
Q5	240006	Si NPN TRANSISTOR	NATIONAL	2N3904 / TO92	3
Q6	230031	N-CHAN DUAL J FET	TELEDYNE	SU2656M.	1
Q7	250004	Si PNP TRANSISTOR	NATIONAL	2N3906 / TO92	-
Q8	230042	N-CHAN I LIM 3·0mA	TELEDYNE	TCR510	1
Q9	230001	N-CHAN I LIM 1·4mA	TELEDYNE	TCR506	-
Q10	240006	Si NPN TRANSISTOR	NATIONAL	2N3904 / TO92	-
Q11	240006	Si NPN TRANSISTOR	NATIONAL	2N3904 / TO92	-

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DRAWING NUMBER 400448 SHEET 10 OF 15

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M1	260027	714 OP AMP	FAIRCHILD	µA714 HC	3
M2	NOT USED				
M3	260053	7650 OP AMP	INTERSIL	ICL7650 CPD	1
M4	260027	714 OP AMP	FAIRCHILD	µA714 HC	-
M5	280023	QUAD 2 I/P NOR	MOTOROLA	MC14001 UBCP	3
M6	280090	DUAL BINARY DECODER	MOTOROLA	MC14555 BCP	1
M7	260027	714 OP AMP	FAIRCHILD	µA 714 HC	-
M8	NOT USED				
M9	280023	QUAD 2 I/P NOR	MOTOROLA	MC14001 UBCP	-
M10	280017	HEX INVERTER	MOTOROLA	MC 14069 UBCP	2
M11		NOT USED			-
M12	290090	7x DARLINGTON DRIVER	SPRAGUE / EXAR	ULN 2002A / XR2202CP	4
M13	290090	7x DARLINGTON DRIVER	SPRAGUE / EXAR	ULN 2002A / XR2202CP	-
M14	290090	7x DARLINGTON DRIVER	SPRAGUE / EXAR	ULN2002A / XR2202CP	-
M15	260039	324 QUAD OP AMP	NATIONAL	LM324 N	1
M16	280023	QUAD 2 I/P NOR	MOTOROLA	MC 14001 UBCP	-
M17	280017	HEX INVERTER	MOTOROLA	MC14069 UBCP	-
M18	280035	BCD/DECIMAL DECODER	MOTOROLA	MC 14028 BCP	1
M19	280045	TRIPLE 3 I/P NOR	MOTOROLA	MC14025 BCP	1
M20	290090	7X DARLINGTON DRIVER	SPRAGUE / EXAR	ULN2002A/XR2202CP	-

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J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
RL1	330028	RELAY 4POLE LATCHING	NATIONAL	S3 - L2 - 24V	1
RL2	330012	RELAY REED 1A GUARDED	HAMLIN	HE721A5134	5
RL3	330012	RELAY REED 1A GUARDED	HAMLIN	HE721A5134	-
RL4	330012	RELAY REED 1A GUARDED	HAMLIN	HE 721A5134	-
RL5	330012	RELAY REED 1A GUARDED	HAMLIN	HE 721A5134	-
RL6	330012	RELAY REED 1A GUARDED	HAMLIN	HE 721A5134	-
RL7	NOT USED				-
RL8	330029	RELAY 2P2W	SDS	DS2E-M-DC24V	2
RL9	330029	RELAY 2P2W	SDS	DS2E-M-DC24V	-
RL10	330030	RELAY 4P N/O	SDS	S4-24V	13
RL11	330030	RELAY 4P N/O	SDS	S4-24V	-
RL12	330030	RELAY 4P N/O	SDS	S4-24V	-
RL13	330030	RELAY 4P N/O	SDS	S4-24V	-
RL14	330030	RELAY 4P N/O	SDS	S4-24V	-
RL15	330027	RELAY 1P2W MINIATURE	TAKAMISAWA	MZ12HSC	1
RL16	330030	RELAY 4P N/O	SDS	S4-24V	-
RL17	330030	RELAY 4P N/O	SDS	S4-24V	-
RL18	330030	RELAY 4P N/O	SDS	S4-24V	-
RL19	330030	RELAY 4P N/O	SDS	S4-24V	-
RL20, 23, 24, 25	330030	RELAY 4P N/O	SDS	S4-24V	-

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DRAWING NUMBER 400448 SHEET 12 OF 15

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
L1	370001	10μH 0·85Ω RF CHOKE	PLESSEY	58/10/0011/10	2
L2	370001	10μH 0·85Ω RF CHOKE	PLESSEY	58/10/0011/10	-
	410262-2B	I/Ω PRINTED CIRCUIT	BOARD		1
	450419-1	CURRENT HEATSINK			1
	530222	24/0·2 P.V.C INS. WIRE	RED 1·5KV RMS		240mm
	530444	24/0·2 P.V.C INS. WIRE	YELLOW 1·5KV RMS		240mm
	530666	24/0·2 P.V.C INS. WIRE	BLUE 1·5KV RMS		240mm
	530999	24/0·2 P.V.C INS. WIRE	WHITE 1·5KV RMS		240mm
	540002	22SWG TINNED COPPER WIRE.			A/R
	540008	7/0·2 WHITE PTFE INSULATED	WIRE		A/R
	540006	1/0·4 BLK. PTFE INS! WIRE		TO BSG210 TYPE A	A/R
	560006	2 CORE PTFE SCREENED 19	/0·15 CABLE	SEE DRG.	310mm
	590001	SLEEVE MAX.CABLE Ø 3·0	HELLERMANN ELECTRIC	H15 x 20mm BLK. HELSYN	8
	590003	HEATSHRINK SLEEVE Ø 6·4 INT	RS OR HELLERMANN ELECTRIC	399-524 OR LYR 64	40mm
	590004	SLEEVE - PTFE	HELLERMANN ELECTRIC	FE 10	A/R
	590002	SLEEVE MAX.CABLE Ø 6·0	HELLERMANN ELECTRIC	H15 x 25mm BLK HELSYN	2

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TITLE '4000' I/Ω PCB ASSEMBLY

DRAWING NUMBER 400448 SHEET 13 OF 15

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	602001	FSV TERMINAL	MOLEX	02-04-5114	16
	605060	14 WAY LOW PROFILE DIL	SOCKET		8
	605061	16 WAY LOW PROFILE DIL	SOCKET		6
	605072	8 WAY ·156" HOUSING	MOLEX	90-50-3081	1
	605077	CRIMP TERMINAL GD.PL.	MOLEX	08-56-0106	4
	611006	M3 x 10mm POZI-PAN STEEL.	ZN.PL.		2
	611004	M3 x 6mm POZI-PAN STEEL.	ZN.PL.		3
	611015	M3 x 8mm POZI-C.S.K STEEL.	ZN.PL.		2
	613005	M3 INT SHAKEPROOF			2
	613007	M3 WASHER STEEL ZN.PL.			2
	613029	M3 CRINKLE WASHER SS			5
	615002	M3 FULL NUT STEEL ZN.PL.			4
	620001	CLOVERLEAF PTFE INSUL.	SEALECTRO	FTE12P59	18
	620003	SOLDER PIN	HARWIN	H 2105 A01	15
	620005	CLOVERLEAF PTFE INSUL.	SEALECTRO	FTE 15P59	19
	620007	TEST POINT TERMINAL	MICROVAR	TYPE C30	1

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DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	630003	'P' CLIP ϕ 4·8 mm	SES	CN6	2
	630024	STEATITE BEAD 16 SWG	PARK ROYAL PORCELAIN	N°2	18
	630036	STEATITE BEAD 18 SWG	PARK ROYAL PORCELAIN	N°1	14
	630122	PCB EJECTOR BLUE	RICHCO	CBE	2
	900003	HEAT SINK COMPOUND	RS	554-311	A/R
F1	920124	FUSE 375mA 125V 7mm	LITTLE FUSE	275 ·375	3
F2	920124	FUSE 375mA 125V 7mm	LITTLE FUSE	275 ·375	—
F3	920120	FUSE 1 A 125V 7mm	LITTLE FUSE	275 001	1
F4	920124	FUSE 375mA 125V 7mm	LITTLE FUSE	275 ·375	—
F5	920125	FUSE 2½ A 125V 7mm	LITTLE FUSE	275 02·5	1

NOTES.

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TITLE '4000' I/Ω PCB ASSEMBLY

DRAWING NUMBER 400448

SHEET 15 OF 15

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	066205	2M POT 3/8 SQ VERT CERMET	BECKMAN	72XW	1
R2	000101	100R 5% 1/4W CARBON	MULLARD	CR25	5
R3	000121	120R 5% 1/4W CARBON	MULLARD	CR25	3
R4	000392	3k9 5% 1/4W CARBON	MULLARD	CR25	3
R5	000393	39k 5% 1/4W CARBON	MULLARD	CR25	3
R6	000682	6K8 5% 1/4W CARBON	MULLARD	CR25	1
R7	000393	39k 5% 1/4W CARBON	MULLARD	CR25	—
R8	000104	100k 5% 1/4W CARBON	MULLARD	CR25	5
R9	000471	470R 5% 1/4W CARBON	MULLARD	CR25	5
R10	000183	18k 5% 1/4W CARBON	MULLARD	CR25	8
R11	000183	18k 5% 1/4W CARBON	MULLARD	CR25	—
R12	000223	22k 5% 1/4W CARBON	MULLARD	CR25	6
R13	000682	6k8 5% 1/4W CARBON	MULLARD	CR25	2
R14	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—
R15	000682	6k8 5% 1/4W CARBON	MULLARD	CR25	—
R16	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R17	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	4
R18	000102	1k 5% 1/4W CARBON	MULLARD	CR25	5
R19	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R20	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	—
R21	000181	180R 5% 1/4W CARBON	MULLARD	CR25	5
R22	000181	180R 5% 1/4W CARBON	MULLARD	CR25	—
R23	008034	0R15 10% 2½W WIREWOUND	WELWYN	W21	4

NOTES.

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E.C.O.	RELEASED	1331	1353/6	1364.1366.1368.1375.1381 1388	1458	1518	1529		
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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 2 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	008034	0R15 10% 2½W WIREWOUND	WELWYN	W21	—
R25	000183	18k 5% 1/4W CARBON	MULLARD	CR25	—
R26	000183	18k 5% 1/4W CARBON	MULLARD	CR25	—
R27	000123	12k 5% 1/4W CARBON	MULLARD	CR25	2
R28	011962	19k6 1% 1/8W 50ppm MF	HOLCO	H8C	2
R29	011001	1k00 1% 1/8W 50ppm MF	HOLCO	H8C	2
R30	000123	12k 5% 1/4W CARBON	MULLARD	CR25	—
R31	011962	19k6 1% 1/8W 50ppm MF	HOLCO	H8C	—
R32	011001	1k00 1% 1/8W 50ppm MF	HOLCO	H8C	—
R33	005103	10k 2% ½W MET-OX	ELECTROSIL	TR5	1
R34	008026	2k7 5% 2½W WIREWOUND	WELWYN	W21	1
R35	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	—
R36	008034	0R15 10% 2½W WIREWOUND	WELWYN	W21	—
R37	000183	18k 5% 1/4W CARBON	MULLARD	CR25	—
R38	000331	330R 5% 1/4W CARBON	MULLARD	CR25	2
R39	000181	180R 5% 1/4W CARBON	MULLARD	CR25	—
R40	000151	150R 5% 1/4W CARBON	MULLARD	CR25	2
R41	000222	2k2 5% 1/4W CARBON	MULLARD	CR25	3
R42	000392	3k9 5% 1/4W CARBON	MULLARD	CR25	—
R43	000183	18k 5% 1/4W CARBON	MULLARD	CR25	—
R44	000181	180R 5% 1/4W CARBON	MULLARD	CR25	—
R45	000331	330R 5% 1/4W CARBON	MULLARD	CR25	—
R46	000151	150R 5% 1/4W CARBON	MULLARD	CR25	—

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DRAWING NUMBER 400449 SHEET 3 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R47	000392	3k9 5% 1/4W CARBON	MULLARD	CR25	—
R48	000222	2k2 5% 1/4W CARBON	MULLARD	CR25	—
R49	008034	OR15 10% 2½W WIREWOUND	WELWYN	W21	—
R50	000183	18k 5% 1/4W CARBON	MULLARD	CR25	—
R51	000152	1k5 5% 1/4W CARBON	MULLARD	CR25	3
R52	000152	1k5 5% 1/4W CARBON	MULLARD	CR25	—
R53	000183	18k 5% 1/4W CARBON	MULLARD	CR25	—
R54	000560	56R 5% 1/4W CARBON	MULLARD	CR25	5
R55	000560	56R 5% 1/4W CARBON	MULLARD	CR25	—
R56	000228	2R2 5% 1/4W CARBON	MULLARD	CR25	2
R57	000228	2R2 5% 1/4W CARBON	MULLARD	CR25	—
R58	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R59	011002	10k0 1% 1/8W 50ppm M.F.	HOLCO	H8C	2
R60	013920	392R 1% 1/8W 50ppm M.F.	HOLCO	H8C	1
R61	016810	681R 1% 1/8W 50ppm M.F.	HOLCO	H8C	1
R62	011002	10k0 1% 1/8W 50ppm M.F.	HOLCO	H8C	—
R63	014751	4k75 1% 1/8W 50ppm M.F.	HOLCO	H8C	3
R64	014751	4k75 1% 1/8W 50ppm M.F.	HOLCO	H8C	—
R65	064104	100k POT 15 TURN CERMET	BECKMAN	89P	1
R66		PART OF Q26 KIT			—
R67	014751	4k75 1% 1/8W 50ppm M.F.	HOLCO	H8C	—
R68	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R69	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—

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J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R70	000822	8k2 5% 1/4W CARBON	MULLARD	CR25	3
R71	000182	1k8 5% 1/4W CARBON	MULLARD	CR25	3
R72	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—
R73	000822	8k2 5% 1/4W CARBON	MULLARD	CR25	—
R74	000182	1k8 5% 1/4W CARBON	MULLARD	CR25	—
R75	000182	1k8 5% 1/4W CARBON	MULLARD	CR25	—
R76	000223	22k 5% 1/4W CARBON	MULLARD	CR25	—
R77	000152	1k5 5% 1/4W CARBON	MULLARD	CR25	—
R78	000560	56R 5% 1/4W CARBON	MULLARD	CR25	—
R79	000221	220R 5% 1/4W CARBON	MULLARD	CR25	3
R80	000821	820R 5% 1/4W CARBON	MULLARD	CR25	1
R81	000103	10k 5% 1/4W CARBON	MULLARD	CR25	7
R82	066501	500R POT 3/8 SQ VERT CERMET	BECKMAN	72XW	1
R83	000470	47R 5% 1/4W CARBON	MULLARD	CR25	3
R84	000560	56R 5% 1/4W CARBON	MULLARD	CR25	—
R85	000478	4R7 5% 1/4W CARBON	MULLARD	CR25	2
R86	000220	22R 5% 1/4W CARBON	MULLARD	CR25	2
R87	018870	887R 1% 1/8W 50ppm M.F.	HOLCO	H8C	2
R88	018870	887R 1% 1/8W 50ppm M.F.	HOLCO	H8C	—
R89	000393	39k 5% 1/4W CARBON	MULLARD	CR25	—
R90	000273	27k 5% 1/4W CARBON	MULLARD	CR25	2
R91	000273	27k 5% 1/4W CARBON	MULLARD	CR25	—
R92	000222	2k2 5% 1/4W CARBON	MULLARD	CR25	—

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DRAWING NUMBER 400449 SHEET 5 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R93	000681	680R 5% 1/4W CARBON	MULLARD	CR25	3
R94	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R95	000681	680R 5% 1/4W CARBON	MULLARD	CR25	—
R96	012802	28k 1% 1/8W 50ppm M.F.	HOLCO	H8C	1
R97	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—
R98	000153	15k 5% 1/4W CARBON	MULLARD	CR25	2
R99	000220	22R 5% 1/4W CARBON	MULLARD	CR25	—
R100	000478	4R7 5% 1/4W CARBON	MULLARD	CR25	—
R101	000470	47R 5% 1/4W CARBON	MULLARD	CR25	—
R102	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R103	000470	47R 5% 1/4W CARBON	MULLARD	CR25	—
R104	000390	39R 5% 1/4W CARBON	MULLARD	CR25	2
R105	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R106	000221	220R 5% 1/4W CARBON	MULLARD	CR25	—
R107	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R108	000390	39R 5% 1/4W CARBON	MULLARD	CR25	—
R109	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R110	000223	22k 5% 1/4W CARBON	MULLARD	CR25	—
R111	000471	470R 5% 1/4W CARBON	MULLARD	CR25	—
R112	000121	120R 5% 1/4W CARBON	MULLARD	CR25	—
R113	000121	120R 5% 1/4W CARBON	MULLARD	CR25	—
R114	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R115	008036	3R3 5% 2½W WIREWOUND	WELWYN	W21	1

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 6 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R116	000223	22k 5% 1/4W CARBON	MULLARD	CR25	—
R117	000102	1k 5% 1/4W CARBON	MULLARD	CR25	—
R118	000223	22k 5% 1/4W CARBON	MULLARD	CR25	—
R119	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R120	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R121	000223	22k 5% 1/4W CARBON	MULLARD	CR25	—
R122	000473	47k 5% 1/4W CARBON	MULLARD	CR25	3
R123	000472	4k7 5% 1/4W CARBON	MULLARD	CR25	—
R124	000105	1M 5% 1/4W CARBON	MULLARD	CR25	3
R125	000105	1M 5% 1/4W CARBON	MULLARD	CR25	—
R126	000105	1M 5% 1/4W CARBON	MULLARD	CR25	—
R127	000221	220R 5% 1/4W CARBON	MULLARD	CR25	—
R128	008032	270R 5% 2½W WIREWOUND	WELWYN	W21	1
R129	008029	18R 2% 1/2W MET-GLAZE	NEOHM	RGP 0207	2
R130	008029	18R 2% 1/2W MET-GLAZE	NEOHM	RGP 0207	—
R131	000473	47k 5% 1/4W CARBON	MULLARD	CR25	—
R132	000394	390k 5% 1/4W CARBON	MULLARD	CR25	1
R133	000473	47k 5% 1/4W CARBON	MULLARD	CR25	—
R134	000363	36k 5% 1/4W CARBON	MULLARD	CR25	1
R135	000154	150k 5% 1/4W CARBON	MULLARD	CR25	1
R136	000100	10R 5% 1/4W CARBON	MULLARD	CR25	1
R137	000153	15k 5% 1/4W CARBON	MULLARD	CR25	—
R138	000104	100k 5% 1/4W CARBON	MULLARD	CR25	—

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TITLE 4000. POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 7 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R139	000822	8k2 5% 1/4W CARBON	MULLARD	CR25	—
R140	000681	680R 5% 1/4W CARBON	MULLARD	CR25	—
R141	000181	180R 5% 1/4W CARBON	MULLARD	CR25	—
R142	000560	56R 5% 1/4W CARBON	MULLARD	CR25	—
R143	001151	150R 5% 1/2W CARBON	MULLARD	CR37	1
R144	000103	10k 5% 1/4W CARBON	MULLARD	CR25	—
R145	008038	1k2 5% 2½W WIREWOUND	WELWYN	W21	2
R146	008038	1k2 5% 2½W WIREWOUND	WELWYN	W21	—
R147	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—
R148	000101	100R 5% 1/4W CARBON	MULLARD	CR25	—

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TITLE 4000. POWER AMP (DC) PCB ASSY.
DRAWING NUMBER 400449 SHEET 8 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	3
C2	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	—
C3	180039	470µF 63V AL. ELECT.	STEATITE	EKR 00KJ 347J	4
C4		NOT USED			—
C5	104026	47nF +50% −20% 50V CER DISC	SIEMENS	B37449	11
C6	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	K1R0E35	2
C7	180040	10µF 63V AL. ELECT	STEATITE	EKR 00CC 210J	2
C8	110013	100nF 20% 250V POLYESTER	MULLARD	C280 AEP 100K	8
C9		NOT USED			—
C10	180039	470µF 63V AL. ELECT.	STEATITE	EKR 00KJ 347J	—
C11	101103	10nF 25% 250V CER DISC	ITT	CD10	2
C12	101103	10nF 25% 250V CER DISC	ITT	CD10	—
C13	180040	10µF 63V AL. ELECT	STEATITE	EKR 00CC 210J	—
C14	110013	100nF 20% 250V POLYESTER	MULLARD	C280 AEP 100K	—
C15	180039	470µF 63V AL. ELECT.	STEATITE	EKR 00KJ 347J	—
C16	104026	47nF +50% −20% 50V CER DISC	SIEMENS	B37449	—
C17	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	K1R0E35	—
C18	110013	100nF 20% 250V POLYESTER	MULLARD	C280 AEP 100K	—
C19	150003	47µF 20% 6V3 DIP TANT	UNION CARBIDE	K47E6V3	2
C20	102332	3n3F 20% 500V CER DISC	ITT	CD10	3
C21	150004	100µF 20% 6V3 DIP TANT	UNION CARBIDE	K100E6V3	3
C22	150004	100µF 20% 6V3 DIP TANT	UNION CARBIDE	K100E6V3	—
C23	102332	3n3F 20% 500V CER DISC	ITT	CD10	—

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TITLE 4000 POWER AMP (DC) PCB ASSY
DRAWING NUMBER 400449 SHEET 9 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C24	150003	47µF 20% 6V3 DIP TANT	UNION CARBIDE	K47E6V3	—
C25	180039	470µF 63V AL ELECT	STEATITE	EKR 00KJ 347J	—
C26	110013	100nF 20% 250V POLYESTER	MULLARD	C280AEP100K	—
C27	110029	1n5F 20% 100V POLYESTER	WIMA	FKS2MIN	1
C28	180044	220µF 40V AL. ELECT	STEATITE	EKM 00DE 322G	1
C29	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	—
C30	102470	47pF 5% 500V CER DISC	ITT	CD10	2
C31	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C32	110005	10nF 20% 250V POLYESTER	MULLARD	C280AE P10K	1
C33	102470	47pF 5% 500V CER DISC	ITT	CD10	—
C34	180041	100µF 40V AL. ELECT	STEATITE	EKM 00FD 310G	1
C35		NOT USED			—
C36	110035	220nF 20% 63V POLYESTER	WIMA	MKS2 MIN	1
C37	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C38	102331	330pF 10% 500V CER DISC	ITT	CD10	1
C39	102152	1n5F 10% 500V CER DISC	ITT	CD10	1
C40	110013	100nF 20% 250V POLYESTER	MULLARD	C280AE P100K	—
C41	120028	4n7F 20% 100V POLYCARB	WIMA	FKC2MIN	1
C42	102121	120pF 10% 500V CER DISC	ITT	CD10	1
C43	150004	100µF 20% 6V3 DIP TANT	UNION CARBIDE	K100E6V3	—
C44	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C45	102680	68pF 5% 500V CER DISC	ITT	CD10	1
C46	150015	10µF 20% 35V DIP TANT	UNION CARBIDE	K10E35	1

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 10 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C47	110013	100nF 20% 250V POLYESTER	MULLARD	C280 AE P100K	—
C48	120021	470nF 10% 63V POLYCARB	ASHCROFT	A2B4711B	1
C49	150017	100µF 20% 16V DIP TANT	UNION CARBIDE	K100E16	2
C50	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C51	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C52	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C53	180043	470µF 25V AL ELECT	STEATITE	EKM 00FE 347E	2
C54	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C55	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C56	180043	470µF 25V AL ELECT	STEATITE	EKM 00FE 347E	—
C57	104026	47nF +50/-20% 50V CER DISC	SIEMENS	B37449	—
C58	140047	33nF 10% 1k5V POLYPROP	STEATITE	MKP 1841	3
C59	140047	33nF 10% 1k5V POLYPROP	STEATITE	MKP 1841	—
C60	110013	100nF 20% 250V POLYESTER	MULLARD	C280AE P100K	—
C61	110013	100nF 20% 250V POLYESTER	MULLARD	C280AE P100K	—
C62	102102	1nF 10% 500V CER DISC	ITT	CD10	1
C63	102221	220pF 10% 500V CER DISC	ITT	CD10	1
C64	102821	820pF 10% 500V CER DISC	ITT	CD10	1
C65	102332	3n3F 20% 500V CER DISC	ITT	CD10	—
C66	140048	47nF 10% 1k5V POLYPROP	STEATITE	MKP1841	1
C67	140047	33nF 10% 1k5V POLYPROP	STEATITE	MKP1841	—
C68	150022	2µ2F 20% 35V DIP TANT	UNION CARBIDE	K2R2E35	1
C69		NOT USED			—

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 11 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C70	150025	3µ3F 20% 35V DIP TANT	UNION CARBIDE	K3R3E35	1
C71	150017	100µF 20% 16V DIP TANT	UNION CARBIDE	K100E16	—
C72	102471	470pF 10% 500V CER DISC	ITT	CD10	2
C73	102471	470pF 10% 500V CER DISC	ITT	CD10	—
D1	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	4
D2	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	—
D3	210100	10V 400mW ZENER	MULLARD	BZY88C10	4
D4	210150	15V 400mW ZENER	MULLARD	BZY88C15	3
D5	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	25
D6	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D7		NOT USED			—
D8		NOT USED			—
D9	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 12 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D10	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D11	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D12	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	—
D13	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	—
D14	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D15	214012	2V45 30ppm ZENER	FERRANTI	ZN458	2
D16	214012	2V45 30ppm ZENER	FERRANTI	ZN458	—
D17	200006	1A 600V GP Si DIODE	FAIRCHILD	IN4005	6
D18	200006	1A 600V GP Si DIODE	FAIRCHILD	IN4005	—
D19	200006	1A 600V GP Si DIODE	FAIRCHILD	IN4005	—
D20	200006	1A 600V GP Si DIODE	FAIRCHILD	IN4005	—
D21	210150	15V 400mW ZENER	MULLARD	BZY88C15	—
D22	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D23	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D24	210150	15V 400mW ZENER	MULLARD	BZY88C15	—
D25	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D26	210056	5V6 400mW ZENER	MULLARD	BZY88C5V6	2
D27	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D28	210056	5V6 400mW ZENER	MULLARD	BZY88C5V6	—
D29	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D30	213011	1V5 250mW ZENER	MULLARD	BZV46-1V5	3
D31	213011	1V5 250mW ZENER	MULLARD	BZV46-1V5	—
D32	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 13 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D33	200001	75mA 75v GP Si DIODE	FAIRCHILD	IN4148	—
D34	213011	IV5 250mW ZENER	MULLARD	BZV46-IV5	—
D35	213012	2V0 250mW ZENER	MULLARD	BZV46-2V0	1
D36 *	214013 BLZ	6V2 ZENER SELECTED	DATRON	SEE DRG	1
D37	220008	LED RED	PYE-TMC	521-9165	1
D38	200006	1A 600V GP Si DIODE	FAIRCHILD	IN4005	—
D39	200006	1A 600V GP Si DIODE	FAIRCHILD	IN4005	—
D40	220010	Si HOT CARRIER DIODE	HP	HSCH1001/IN6263	1
D41	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D42	210033	3V3 400mW ZENER	MULLARD	BZY88C3V3	1
D43	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D44	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	1
D45	210240	24V 400mW ZENER	MULLARD	BZY88C24	1
D46	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D47	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D48	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D49	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D50	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D51	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D52	210100	10V 400mW ZENER	MULLARD	BZY88C10	—
D53	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D54	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D55	213009	15V 5W ZENER	UNITRODE	TVS 515	1

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 — SHEET 14 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D56	200020	1A 1k5V FR Si DIODE	MOTOROLA	BY339	8
D57	200020	1A 1k5V FR Si DIODE	MOTOROLA	BY339	—
D58	200020	1A 1k5V FR Si DIODE	MOTOROLA	BY339	—
D59	200020	1A 1k5V FR Si DIODE	MOTOROLA	BY339	—
D60	200020	1A 1k5V FR Si DIODE	MOTOROLA	BY339	—
D61	200020	1A 1k5V FR Si DIODE	MOTOROLA	BY339	—
D62	200020	1A 1k5V FR Si DIODE	MOTOROLA	BY339	—
D63	200020	1A 1k5V FR Si DIODE	MOTOROLA	BY339	—
D64	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D65	200001	75mA 75V GP Si DIODE	FAIRCHILD	IN4148	—
D66	210100	10V 400mW ZENER	MULLARD	BZY88C10	—
D67	210100	10V 400mW ZENER	MULLARD	BZY88C10	—
D68	213006	5V 5W ZENER	UNITRODE	TVS505	2
D69	213006	5V 5W ZENER	UNITRODE	TVS505	—

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 — SHEET 15 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q1	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	7
Q2	250009	Si PNP TRANSISTOR	NATIONAL	2N5401 / TO18	6
Q3	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	–
Q4	230039	P-CHAN JFET	SILICONIX	J175	1
Q5	230035	N-CHAN JFET	TELEDYNE	U1897 JF	3
Q6	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	–
Q7	240006	Si NPN TRANSISTOR	NATIONAL	2N3904 / TO18	1
Q8	250009	Si PNP TRANSISTOR	NATIONAL	2N5401 / TO18	–
Q9	250009	Si PNP TRANSISTOR	NATIONAL	2N5401 / TO18	–
Q10	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	–
Q11	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	–
Q12	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	–
Q13	250009	Si PNP TRANSISTOR	NATIONAL	2N5401 / TO18	–
Q14	250009	Si PNP TRANSISTOR	NATIONAL	2N5401 / TO18	–
Q15	250001	Si PNP TRANSISTOR	NATIONAL	BC214 / TO18	2
Q16	240001	Si NPN TRANSISTOR	NATIONAL	BC184 / TO18	1
Q17	230042	N-CHAN I LIM 3·0mA	TELEDYNE	TCR510	2
Q18	230042	N-CHAN I LIM 3·0mA	TELEDYNE	TCR510	–
Q19	250009	Si PNP TRANSISTOR	NATIONAL	2N5401 / TO18	–
Q20	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	–
Q21	240031	Si NPN TRANSISTOR	MOTOROLA	BD139	1
Q22	250020	Si PNP TRANSISTOR	MOTOROLA	TIP 32C	2
Q23	240034	Si NPN TRANSISTOR	MOTOROLA	TIP31C	2

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DRAWING NUMBER 400449
SHEET 16 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q24	250020	Si PNP TRANSISTOR	MOTOROLA	TIP32C	–
Q25	240034	Si NPN TRANSISTOR	MOTOROLA	TIP31C	–
Q26	239051-2	N-CHAN J-FET KIT	DATRON	U1897JF (COLOUR)+RES (R66)	1
Q27	230035	N-CHAN J-FET	TELEDYNE	U1897JF	–
Q28	230050	N-CHAN I LIM 2·5mA	TELEDYNE	TCR 509	1
Q29	250011	Si PNP TRANSISTOR	NATIONAL	BC327 / TO18	1
Q30	240014	Si NPN TRANSISTOR	NATIONAL	BC337 / TO18	1
Q31	240029	Si NPN TRANSISTOR	MOTOROLA	BC546 / TO18	4
Q32	250018	Si PNP TRANSISTOR	MOTOROLA	BC556 / TO18	2
Q33	230036	N-CHAN J FET	SILICONIX	J108	1
Q34	230035	N-CHAN J FET	TELEDYNE	U1897 JF	–
Q35	240029	Si NPN TRANSISTOR	MOTOROLA	BC546 / TO18	–
Q36	240028	Si NPN TRANSISTOR	MOTOROLA	BC414 / TO18	2
Q37	240029	Si NPN TRANSISTOR	MOTOROLA	BC546 / TO18	–
Q38	240028	Si NPN TRANSISTOR	MOTOROLA	BC414 / TO18	–
Q39	250018	Si PNP TRANSISTOR	MOTOROLA	BC 556 / TO18	–
Q40	240029	Si NPN TRANSISTOR	MOTOROLA	BC 546 / TO18	–
Q41	240030	Si NPN TRANSISTOR	MOTOROLA	BD389	1
Q42	250019	Si PNP TRANSISTOR	MOTOROLA	BD390	1
Q43	250001	Si PNP TRANSISTOR	NATIONAL	BC214 / TO18	–
Q44	250008	Si PNP TRANSISTOR	NATIONAL	BC214C / TO18	1

NOTES.

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DATE												
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DATE 23.3.82
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datron ELECTRONICS LTD
TITLE 4000 POWER AMP (DC) PCB ASSY
DRAWING NUMBER 400449
SHEET 17 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
M1	260043	358 DUAL OP AMP	NATIONAL	LM358N	1
M2	260050	412 DUAL FET I/P OP AMP	NATIONAL	LF412N	2
M3	260057	5534 OP AMP	SIGNETICS	NE5534N	2
M4	260057	5534 OP AMP	SIGNETICS	NE5534N.	–
M5	260050	412 DUAL FET I/P OP AMP	NATIONAL	LF412N	–
M6	260027	714 OP AMP	FAIRCHILD	µA714 HC	1
M7	290090	7 x DARLINGTON DRIVER	SPRAGUE/EXAR	ULN2002A/XR2202 CP	1
M8	280037	HEX BUFFER	MOTOROLA	MC14050BCP	1
M9	220015	5kV OPTO ISOLATOR	FAIRCHILD	FCD820C	1
M10	280011	DUAL D FLIP-FLOP	MOTOROLA	MC 14013 BCP	1
M11	220033	INTERFACE OPTO ISOLATOR	HP	HCPL-3700	1
RL1	330020-1	RELAY 2P2W 5A	PYE	GW 265/24/3	2
RL2	330020-1	RELAY 2P2W 5A	PYE	GW 265/24/3	–
RL3	330005	RELAY 2P2W 5AMP	P+B	R10-E1-X2-S3.2k (25209)	1

NOTES.

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 18 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
L1	370013	4µH 6A RF CHOKE	ERO	F1756-004-601	3
L2	370013	4µH 6A RF CHOKE	ERO	F1756-004-601	–
L3	370013	4µH 6A RF CHOKE	ERO	F1756-004-601	–
L4	370001	10µH 0.85Ω RF CHOKE	PLESSEY	58/10/0011/10	4
L5	370001	10µH 0.85Ω RF CHOKE	PLESSEY	58/10/0011/10	–
L6	370009	1µH 3A RF CHOKE	ERO	F1756-001-301	1
L7	370018	10mH 137Ω RF CHOKE	SIGMA	SC60	1
L8	370007-1	40mH CHOKE	SIGA	SEE DRG	1
L9	370015-1	26m5H CHOKE	SIGA	SEE DRG	1
L10	370016-1	24m1H CHOKE	SIGA	SEE DRG	1
L11	370001	10µH 0.85Ω RF CHOKE	PLESSEY	58/10/0011/10	–
L12	370001	10µH 0.85Ω RF CHOKE	PLESSEY	58/10/0011/10	–
F1	920128	FUSE 4A 250V 20mm SLO-B	BELLING LEE	L2080A/4	3
F2	920128	FUSE 4A 250V 20mm SLO-B	BELLING LEE	L2080A/4	–
F3	920128	FUSE 4A 250V 20mm SLO-B	BELLING LEE	L2080A/4	–
S1	700070	SWITCH 2P2W SLIDE	APR	25446H6A	1
	400472	CONSTANT I PCB ASSY.	DATRON		1

NOTES.

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 19 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	410203-4A	PCB			1
	459112-2	RELAY BRACKET			1
	590004	SLEEVE - PTFE	HELLERMANN ELECTRIC	FE10	A/R
	540008	7/·2 PTFE INSULATED (WHITE) WIRE			1260 mm
	540002	22 SWG B.T.C. WIRE			A/R
	590001	SLEEVE. MAX.CABLE ∅ 3·0	HELLERMAN ELECTRIC	H15 x 20mm. BLK HELSYN	11
	590007	LACING CORD (BLACK)	HELLERMANN ELECTRIC	MW/062	A/R
J1- J6	604042	4 WAY ·156" PLUG GD/PL	MOLEX	09-72-2041	12
	605059/A	8 WAY DIL SOCKET			6
	605060/A	14 WAY DIL SOCKET			1
	605061/A	16 WAY DIL SOCKET			2
	605066/A	6 WAY DIL SOCKET			1
	613014	M2·5 INT SHAKEPROOF			1
	611016	M3x8mm POZIPAN STEEL	ZN PL		7
	613005	M3 INT. SHAKEPROOF			7
	613007	M3 WASHER STEEL ZN PL			4
	615002	M3 FULL NUT STEEL ZN PL			7
	615005	3-48UNC FULL NUT STEEL	ZN PL		1
	618004	MOUNTING PAD TO18	JERMYN	TO18-008D	2

NOTES.

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 20 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	620003	SOLDER PIN	HARWIN	H2105 A01	15
	630024	STEATITE BEAD 16 SWG	PARK ROYAL PORCELAIN	No 2	10
	630036	STEATITE BEAD 18 SWG	PARK ROYAL PORCELAIN	No 1	5
	630123	PCB EJECTOR VIOLET	RICHCO	CBE	2
	620007	TEST POINT TERMINAL	MICROVAR	C30	30
	920091-1	HEATSINK TO-220	SEE DRG		4
	920126	FUSE HOLDER 20mm PCB	BELLING LEE	L1426	3
	920105-1	HEATSINK TO-202	SEE DRG		2
	900003	HEATSINK COMPOUND	RS	554-311	A/R

NOTES.

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TITLE 4000 POWER AMP (DC) PCB ASSY

DRAWING NUMBER 400449 SHEET 21 OF 21

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000102	1k 5% 1/4W CARBON	MULLARD	CR25	2
R2	011502	15k 1% 1/8W 50ppm M.F.	HOLCO	H8C	1
R3	000338	3R3 5% 1/4W CARBON	MULLARD	CR25	1
R4	000682	6k8 5% 1/4W CARBON	MULLARD	CR25	1
R5	011101	1k10 1% 1/8W 50ppm M.F.	HOLCO	H8C	1
R6	000102	1k 5% 1/4W CARBON	MULLARD	CR25	–
R7	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	2
R8	000272	2k7 5% 1/4W CARBON	MULLARD	CR25	–
C1	180042	3300µF 25V AL. ELECT.	STEATITE	EG 00MG 433E	2
C2	180042	3300µF 25V AL. ELECT.	STEATITE	EG 00MG 433E	–
C3	180025	1000µF 35V AL. ELECT.	WIMA	PRINTILYT 1	3
C4	180025	1000µF 35V AL. ELECT.	WIMA	PRINTILYT 1	–
C5	104026	47nF +50 -20 % 50V CER DISC	SIEMENS	B37449	5
C6	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	4
C7	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	–
C8	150001	22µF 20% 16V DIP TANT	UNION CARBIDE	K22E16	4
C9	150001	22µF 20% 16V DIP TANT	UNION CARBIDE	K22E16	–
C10	104026	47nF +50 -20 % 50V CER DISC	SIEMENS	B37449	–
C11	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	–
C12	104026	47nF +50 -20 % 50V CER DISC	SIEMENS	B37449	–

NOTES.

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ISS.	1	2	3
E.C.O.	RELEASED	1325	1529
DATE	9.3.82	13.5.82	15.9.83
CHKD.	MD	MD	MD

DATE 19.11.81 — datron ELECTRONICS LTD
DRAWN JL
CHECKED
APPROVED
DATE 9.3.82.
TITLE 4000. IN-GUARD POWER SUPPLY PCB. ASSY.
DRAWING NUMBER 400451 — SHEET 2 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C13	150021	22µF 20% 25V DIP TANT	UNION CARBIDE	K22E25	–
C14	180024	10µF 63V AL. ELECT.	MULLARD	016 18109	1
C15	102102	1nF 10% 500V CER DISC	ITT	CD10	1
C16	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	K1R0E35	1
C17	104026	47nF +50 -20 50V CER DISC	SIEMENS	B37449	–
C18	150001	22µF 20% 16V DIP TANT	UNION CARBIDE	K22E16	–
C19	150001	22µF 20% 16V DIP TANT	UNION CARBIDE	K22E16	–
C20	104026	47nF +50 -20 % 50V CER DISC	SIEMENS	B37449	–
C21	180038	1000µF 63V AL. ELECT	STEATITE	EG00MG410J	1
C22	180025	1000µF 35V AL. ELECT	WIMA	PRINTILYT 1	–
C23	180005	1000µF 25V AL. ELECT	WIMA	PRINTILYT 1	2
C24	180005	1000µF 25V AL. ELECT	WIMA	PRINTILYT 1	–
D1	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	4
D2	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	–
D3	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	–
D4	200022	3A 400V GP Si DIODE	MOTOROLA	BY252	–
D5	210150	15V 400mW ZENER	MULLARD	BZY88C15	1

NOTES.

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TITLE 4000. IN-GUARD POWER SUPPLY PCB. ASSY.
DRAWING NUMBER 400451 — SHEET 3 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
D6	211150	15V 1·3W ZENER	MOTOROLA	BZX61C15	1
D7	214012	2V45 30ppm ZENER	FERRANTI	ZN458	1
W1 - W4	209003	1A5 100V BRIDGE RECTIFIER	MICRO-ELECTRONICS	W001	4
Q1	240009	Si NPN TRANSISTOR	NATIONAL	MPSL01 / TO18	1
Q2	240014	Si NPN TRANSISTOR	NATIONAL	BC337 / TO18	1
Q3	230047	N-CHAN CURRENT LIM	TELEDYNE	TCR 513	1
Q4	240024	Si NPN TRANSISTOR	NATIONAL	TIP31A	1
M1	260051	-15V 1A REGULATOR	MOTOROLA	MC7915CT	2
M2	260006	15V 1A REGULATOR	MOTOROLA	MC7815CP	1
M3	260045	-8V ½A REGULATOR	MOTOROLA	MC79M08CT	2
M4	260044	8V ½A REGULATOR	MOTOROLA	MC78M08CT	2
M5	260026	212 OP AMP	NATIONAL	LM212H	1
M6	260005	5V 1A REGULATOR	MOTOROLA	MC7805CP	1
M7	260051	-15V 1A REGULATOR	MOTOROLA	MC7915CT	–
M8	260045	-8V ½A REGULATOR	MOTOROLA	MC79M08CT	–
M9	260044	8V ½A REGULATOR	MOTOROLA	MC78M08CT	–

NOTES.

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TITLE 4000. IN-GUARD POWER SUPPLY PCB. ASSY

DRAWING NUMBER 400451 SHEET 4 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
L1 - L3	370013	4µH 6A RF CHOKE	ERO	F1756-004-601	3
L4 - L9	370014	8µH 3A RF CHOKE	ERO	F1756-008-301	6
L10	370019 - 1	P.S. COMMON MODE CHOKE	SIGA	SEE DRG.	1
	410160-6A	PCB			1
	540002	22 SWG B.T.C. WIRE	RS.		A/R
J1 - J3	604042	4WAY PLUG WITH LOCKING RAMP	MOLEX	09-72-2041	5
	611016	SCREW M3x8mm POZI PAN STEEL	ZN/PLATED GKN		12
	613005	WASHER M3 SHAKEPROOF	ZN/PLATED GKN		12
	620007	TEST POINT TERMINAL	MICROVAR	C30	6
	615002	NUT M3 HEX FULL STEEL	ZN/PLATED GKN		12
	900004	SILICONE RUBBER COMPOUND	RS	555-588	A/R
	920089-1	HEATSINK TO220	SEE DRG.		4
	920090-1	HEATSINK 2x TO220	SEE DRG.		3
F1. F2	920128	FUSE 4 A SLO-BLOW	BELLING LEE	L2080A/4	2
	920126	FUSE HOLDER	BELLING LEE	L1426	4
F3. F4	920127	FUSE 2 A SLO-BLOW	BELLING LEE	L2080A/2	2
	900003	HEATSINK COMPOUND	RS	554-311	A/R

NOTES.

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E.C.O.												
DATE												
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TITLE 4000. IN-GUARD POWER SUPPLY PCB. ASSY

DRAWING NUMBER 400451 SHEET 5 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	090014-2	50K ·02%R 2ppmR W.W.	MANN	AX175B	} 1 SET
R2	090014-2	9K995 ·02%R 2ppmR W.W	MANN	AX175B	
R3		PART OF KIT DI-4 DG-9	MANN	AX175B	-
R4		PART OF KIT DI-4 DG-9	MANN	AX175B	-
R5	018251	8K25 1% 1/8W 50ppm MF	HOLCO	H8C	1
R6	000470	47R 5% 1/4W CARBON	MULLARD	CR25	2
R7	070152	68R ·1% 10ppm W.W	MANN	MX125	2
R8	070152	68R ·1% 10ppm W.W	MANN	MX125	-
R9	070153	34R ·1% 10ppm W.W.	MANN	MX125	2
R10	070153	34R ·1% 10ppm W.W.	MANN	MX125	-
R11	011698	16R9 1% 1/8W 50ppm MF	HOLCO	H8C	2
R12	011698	16R9 1% 1/8W 50ppm MF	HOLCO	H8C	-
R13	050056	10R ·25% 1/8W 50ppm MF	HOLCO	H8C	2
R14	050056	10R ·25% 1/8W 50ppm MF	HOLCO	H8C	-
R15	000438	4R3 5% 1/4W CARBON	MULLARD	CR25	2
R16	000438	4R3 5% 1/4W CARBON	MULLARD	CR25	-
R17	018459	8R45 1% 1/8W 50ppm MF	HOLCO	H8C	2
R18	018459	8R45 1% 1/8W 50ppm MF	HOLCO	H8C	-
R19	090081	2K NTC THERMISTOR	RHOPOINT	MSB 202K	1
R20	008751	750R 2% 1W MET-OX	ELECTROSIL	FP1	1
R21	000470	47R 5% 1/4W CARBON	MULLARD	CR25	-
R22	000222	2K2 5% 1/4W CARBON	MULLARD	CR25	1
R23	015231	5K23 1% 1/8W 50ppm MF	HOLCO	H8C	2

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	1	2	3	4	5
E.C.O.	RELEASED	1367	1432	1445	1492
DATE	22.5.82	23-8-82	15-12-82	15-2-83	7.6.83
CHKD.	MJD.	MJD.	MJD.	MD	KO

DATE 15th FEB 83 — DRAWN B. JACKSON — CHECKED MD — APPROVED — DATE 21.2.83.

datron ELECTRONICS LTD

TITLE 4000/4000A REFERENCE PCB ASSY

DRAWING NUMBER 400452 400452A — SHEET 2 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R24	090099-3	25K } ATTEN SET	MANN	SEE DRG A4	} 1 SET
R25	090099-3	10K			
R26	090099-3	10K			
R27	000125	1M2 5% 1/4W CARBON	MULLARD	CR25	1
R28	012263	226K 1% 1/8W 50ppm MF	HOLCO	H8C	2
R29	063104	100K POT 3/8" SQ CERMET	BECKMAN	72P	1
R30	012003	200K 1% 1/8W 50ppm MF	HOLCO	H8C	1
R31	015231	5K23 1% 1/8W 50ppm MF	HOLCO	H8C	-
R32	012263	226K 1% 1/8W 50ppm MF	HOLCO	H8C	-

NOTES.

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TITLE 4000/4000A REFERENCE PCB ASSY

DRAWING NUMBER 400452 400452A — SHEET 3 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1	102470	47pF 5% 500V CER DISC	ITT	CD10	1
C2	102221	220pF 10% 500V CER DISC	ITT	CD10	1
C3	104026	47nF $^{+50\%}_{-20\%}$ 500V CER DISC	SIEMENS	B37449	1
D1,2,3,4,6,7,8,9.	219015-2	6V2 X 8 ZENER + RESISTOR X 2	DATRON	IN829AX8 + AX1758X 2.	1 KIT
D5	200008	200mA 125V LL Si DIODE	FAIRCHILD	IN458A	1
Q1	240006	Si NPN TRANSISTOR	NATIONAL	2N3904 / TO18	2
Q2	240006	Si NPN TRANSISTOR	NATIONAL	2N3904 / TO18	-
M1	260025	101 OP AMP	NATIONAL	LM 101 AH	1
M2	260027	714 OP AMP	FAIRCHILD	μA714HC	1

NOTES.

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TITLE 4000/4000A REFERENCE PCB ASSY.

DRAWING NUMBER 400452 400452A

SHEET 4 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
TP1-4	604056	4 WAY ·1" PCB PLUG GD PL	MOLEX	22-10-2041	1
J1	605085	4 WAY PCB SOCKET	MOLEX	22-17-2042	2
J2	605085	4 WAY PCB SOCKET	MOLEX	22-17-2042	-
	410162-6	PRINTED CIRCUIT BOARD			1
	450372-3	HEATSINK BLOCK			1
	450373-2	HEATSINK PLATE			1
	540002	22 SWG TINNED COPPER WIRE			A/R
	611004	M3X6mm POZIPAN STEEL	ZN PL		2
	611007	M3X6mm POZI-CSK STEEL	ZN PL		2
	613029	M3 CRINKLE WASHER SS			2
	900003	HEATSINK COMPOUND	RS	554-311	A/R

NOTES.

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TITLE 4000/4000A REFERENCE PCB ASSY

DRAWING NUMBER 400452 400452A

SHEET 5 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	008021	OR47 2½w 5% W/W	WELWYN	W 21	3
R2	008021	OR47 2½w 5% W/W	"	"	—
R3	090098	TS485 THERMAL SENSOR	MICROTHERM	TS485	1
R4	008021	OR47 2½w 5% W/W	WELWYN	W 21	—
Q1	240027	SI NPN TRANSISTOR	MOTOROLA	MJ15001	3
Q2	240027	SI NPN TRANSISTOR	"	MJ15001	—
Q3	240027	SI NPN TRANSISTOR	"	MJ15001	—
Q4	NOT USED.				
Q5	240014	SI NPN TRANSISTOR	NATIONAL	BC 337/ TO 18	1
	590004	SLEEVE · PTFE	HELLERMANN ELECTRIC	FEIO	A/R
	590001	SLEEVE MAX CABLE ϕ 3·0	HELLERMANN ELECTRIC	H15 X 20mm BLACK HELSYN	4
	920087-1	TRANSISTOR HEATSINK	SEE DRG.		1
	410166-4	HEATSINK P.C.B			1
	450279-1	HEATSINK			1

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	C	1
E.C.O.	—	RELEASED
DATE	5-8-81	19-4-82
CHKD.	—	AD

DATE 14-7-81
DRAWN JK
CHECKED MJD
APPROVED
DATE 23.7.82

datron ELECTRONICS LTD

TITLE 4000 POWER AMPLIFIER POSITIVE HEATSINK ASSY

DRAWING NUMBER 400454 SHEET 2 OF 3

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	540002	22 SWG TINNED CU WIRE			A/R
	530000	24/·2 WIRE BLACK			170mm
	530222	" RED			150mm
	530444	" YELLOW			170mm
	530555	" GREEN			195mm
	900003	HEATSINK COMPOUND	RS	554-311	A/R
	530777	24/0·2 WIRE VIOLET			195mm
	530888	" GREY			195mm
	530999	" WHITE			330mm
	605101	13 WAY CRIMP TERMINAL	HOUSING + LOCKING RAMP	09-91-1301	1
	605077	GOLD CRIMP	MOLEX	2478 GL	8
	611017	M3 X 16 POZIPAN SCREW	GKN	ZINC PLATED	5
	611027	M3 X 20 POZIPAN SCREW	"	" "	2
	612004	M3 X 4 STANDOFF	HARWIN	CS 2116/B	6
	612022	M3 X 3 STANDOFF	SEE DRG.		2
	613005	M3 INT SHAKEPROOF ST	GKN DISTRIBUTORS	ZINC PLATED	8
	613007	M3 FLAT STEEL WASHER	" "	"	10
	615002	M3 HEX NUT STEEL	" "	"	3
	618008	INSULATING BUSH	ASSMANN / MULLARD	105 358 / 56201 C	2
	611006	M3 X 10mm POZI·PAN SCREW	GKN	ZINC PLATED	1
	620003	SOLDER PIN	HARWIN	H2105A	8
	630126	CABLE CLIPS 7·9 DIA	RICHCO	N5	1

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	
E.C.O.	
DATE	
CHKD.	

DATE 14-7-81
DRAWN JK
CHECKED
APPROVED
DATE

datron ELECTRONICS LTD

TITLE 4000 POWER AMPLIFIER POSITIVE HEATSINK ASSY

DRAWING NUMBER 400454 SHEET 3 OF 3

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	000101	100R 5% 1/4W CARBON	MULLARD	CR25	2
R2	008037	0R18 10% 2½W WIREWOUND	WELWYN	W21	2
R3	008037	0R18 " " "	"	"	-
R4	000101	100R 5% 1/4W CARBON	MULLARD	CR25	-
R5	090098	NTC THERMISTOR (85°C)	MICROTHERM	TS485	1
R6	000102	1K0 5% 1/4W CARBON	MULLARD	CR25	1
R7	000220	22R " " "	"	"	1
C1	104025	100nF $^{+80}_{-20}$% 50V CER DISC	ITT	DD2	1
C2	180045	47µF 63V AL. ELECT.	MULLARD	031-38479	1
C3	104026	47nF $^{+50}_{-20}$% 50V CER DISC	SIEMENS	B37449	2
C4	104026	47nF " " " "	"	"	-
Q1	240036	Si NPN DARL. TRANSISTOR	MOTOROLA	MJ1000	1
Q2	250024	Si PNP DARL. TRANSISTOR	"	MJ900	1
Q3	240035	Si NPN DARL. TRANSISTOR	"	MJ11016	1
Q4	250023	Si PNP DARL. TRANSISTOR	"	MJ11015	1
Q5	240001	Si NPN TRANSISTOR	NATIONAL	BC184/TO18	2
Q6	250001	Si PNP TRANSISTOR	NATIONAL	BC214/TO18	1
Q7	240001	Si NPN TRANSISTOR	NATIONAL	BC184/TO18	-

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	C	1
E.C.O.	-	RELEASED
DATE	5-8-81	19-4-82
CHKD.	-	MD

DATE 19-4-82
DRAWN B JACKSON
CHECKED MJD
APPROVED B [signature]
DATE 23.4.82

datron ELECTRONICS LTD

TITLE 4000 POWER SUPPLY / CURRENT HEATSINK ASSY

DRAWING NUMBER 400455 SHEET 2 OF 4

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	530000	24\2 WIRE BLACK			355 mm
	530111	" BROWN			865 mm
	530222	" RED			860 mm
	530333	" ORANGE			305 mm
	530444	" YELLOW			375 mm
	530555	" GREEN			170 mm
	530666	" BLUE			125 mm
	530777	" VIOLET			170 mm
	530888	" GREY			170 mm
	530999	" WHITE			290 mm
	605099	5 WAY 0·156 CRIMP TERMINAL HOUSING + RAMP		09 91 0501	1
	605100	9 WAY 0·156 CRIMP TERMINAL HOUSING + RAMP		09 91 0901	2
	605077	GOLD CRIMP	MOLEX	2478-GL	16
	612022	M3X3 STANDOFF	SEE DRG.		8
	611017	M3X16 POZIPAN SCREW	GKN DISTRIBUTORS	ZINC PLATED	4
	611027	M3X20 POZIPAN "	" "	" "	4
	613005	M3 INT SHAKEPROOF ST	GKN DISTRIBUTORS	ZINC PLATED	8
	613007	M3 FLAT STEEL	" "	" "	10
	615002	M3 HEX NUT STEEL	" "	" "	4
	618008	INSULATING BUSH	ASSMANN / MULLARD	105 358 / 56201C	8
	618009	TO3 SIL PAD	WARTH INTERNATIONAL.	3223-07FR-06	4
	620003	SOLDER PIN	HARWIN	H2105A	16
	630126	CABLE CLIP 7·9 DIA	RICHCO	N5	2

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	
E.C.O.	
DATE	
CHKD.	

DATE 15-7-81
DRAWN JK
CHECKED
APPROVED
DATE

datron ELECTRONICS LTD

TITLE 4000 POWER SUPPLY / CURRENT HEATSINK ASSY

DRAWING NUMBER 400455 SHEET 3 OF 4

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	920087-1	TRANSISTOR HEATSINK	SEE DRG.		1
	590028	HEATSHRINK PVC SLEEVE	HELLERMANN	EHN 105	500mm
	590001	SLEEVE MAX CABLE ϕ 3·0	HELLERMANN ELECTRIC	H15x20mm BLK HELSYN	8
	606010	POLARISING KEY	MOLEX	15-04-0219	1
	410166-4	HEATSINK PCB			1
	450279-1	HEATSINK			1

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.												
E.C.O.												
DATE												
CHKD.												

DATE 15-7-81
DRAWN OK
CHECKED
APPROVED
DATE

datron ELECTRONICS LTD

TITLE 4000 POWER SUPPLY/ CURRENT HEATSINK ASSY

DRAWING NUMBER 400455

SHEET 4 OF 4

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1, R2	008021	0R47 2½W 5% W/W	WELWYN	W 21	3
R3	090098	TS485 THERMAL SENSOR	MICROTHERM	TS485	1
R4	008021	0R47 2½W 5% W/W	WELWYN	W21	–
Q1	250017	SI PNP TRANSISTOR	MOTOROLA	MJ 15002	3
Q2	250017	SI PNP TRANSISTOR	MOTOROLA	MJ 15002	–
Q3	250017	SI PNP TRANSISTOR	MOTOROLA	MJ 15002	–
	410166-4	HEATSINK P.C.B			1
	450279-1	HEATSINK			1
	530000	24/·2 WIRE BLACK			170 mm
	530222	" RED			150 mm

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	C	1
E.C.O.	–	RELEASED
DATE	5-8-81	19-4-82
CHKD.	–	AD

DATE 14-7-81	datron ELECTRONICS LTD
DRAWN JK	TITLE 4000 POWER AMPLIFIER NEGATIVE HEATSINK ASSY
CHECKED MJD	
APPROVED [signature]	DRAWING NUMBER 400461
DATE 23.4.82	SHEET 2 OF 3

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	530444	24/·2 WIRE YELLOW			170 mm
	530999	24/·2 WIRE WHITE			330 mm
	605100	9 WAY 0·156 CRIMP TERMINAL HOUSING + RAMP		09-91-0901	1
	605077	GOLD CRIMP	MOLEX	2478 GL	5
	611017	M3X16 POZIPAN SCREW	GKN	ZINC PLATED	6
	611027	M3X20 POZIPAN SCREW	"	" "	1
	612004	M3X4 STANDOFF 1/16" PCB	HARWIN	CS211G / B	6
	612022	M3X3 STANDOFF 1/16" PCB	SEE DRG.		2
	613005	M3 INT SHAKEPROOF ST	GKN DISTRIBUTORS	ZINC PLATED	8
	613007	M3 FLAT STEEL WASHER	" "	"	10
	618008	INSULATING BUSH	ASSMANN / MULLARD	105 358 / 56201C	2
	611006	M3X10mm POZIPAN SCREW	GKN	ZINC PLATED	1
	620003	SOLDER PIN	HARWIN	H2105A	5
	630004	CABLE CLIP 6·4 DIA	RICHCO	N4	1
	540002	22SWG TINNED CU WIRE			A/R
	615002	NUT M3 FULL HEX STEEL		ZINC PLATED.	2
	590001	SLEEVE MAX CABLE ϕ 3·0	HELLERMAN ELECTRIC	H15 X 20mm BLK HELSYN	3
	590004	SLEEVE - PTFE	" "	FE 10	A/R
	900003	HEATSINK COMPOUND	RS	554-311	A/R

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	
E.C.O.	
DATE	
CHKD.	

DATE 14-7-81	datron ELECTRONICS LTD
DRAWN JK	TITLE 4000 POWER AMPLIFIER NEGATIVE HEATSINK ASSY
CHECKED	
APPROVED	DRAWING NUMBER 400461
DATE	SHEET 3 OF 3

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
R1	008024	0R27 10% 2½W WW	WELWYN	W21	1
R2	000330	33R 5% ¼W CARBON	MULLARD	CR25	1
R3	000102	1K0 5% ¼W CARBON	MULLARD	CR25	3
R4	000182	1K8 5% ¼W CARBON	MULLARD	CR25	1
R5	013922	39K2 1% ⅛W 50 ppm MF	HOLCO	H8C	1
R6	013742	37K4 1% ⅛W 50 ppm MF	HOLCO	H8C	1
R7	090001	PTC THERMISTOR	MULLARD	VA8650	1
R8	000470	47R 5% ¼W CARBON	MULLARD	CR25	2
R9	000470	47R 5% ¼W CARBON	MULLARD	CR25	—
R10	011003	100k 1% ⅛W 50ppm MF	HOLCO	H8C	2
R11	011003	100k 1% ⅛W 50ppm MF	HOLCO	H8C	—
R12	066205	2M POT ⅜ SQ VERT CERMET	BECKMAN	72XW	1
R13	001184	180K 5% ½W CARBON	MULLARD	CR37	1
R14	000102	1K0 5% ¼W CARBON	MULLARD	CR25	—
R15	000102	1K0 5% ¼W CARBON	MULLARD	CR25	—
R16	000221	220R 5% ¼W CARBON	MULLARD	CR25	1
R17	008022	0R27 10% ½W MF	RS	147-525	2
R18	008022	0R27 10% ½W MF	RS	147-525	—
R19	000104	100K 5% ¼W CARBON	MULLARD	CR25	1
R20	000221	220R 5% ¼W CARBON	MULLARD	CR25	1

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.	1	2	3	4	5	6
E.C.O.	RELEASED	1314.1324	1447	1468/1476	1504	1529
DATE	17.3.82	13.5.82	14-3-83	8-4-83	12-8-83	15.9.83
CHKD.	MJD	MD	MD	MD	MD	MD

DATE 16-11-81	datron ELECTRONICS LTD
DRAWN JK	TITLE 4000 OUT GUARD POWER SUPPLY ASSY
CHECKED MJD	
APPROVED BY	DRAWING NUMBER 400470
DATE 17.3.82	SHEET 2 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
C1		NOT USED			
C2	150016	1µF 20% 35V DIP TANT	UNION CARBIDE	KIROE35	1
C3		NOT USED			
C4	150017	100µF 20% 16V DIP TANT	UNION CARBIDE	K100E16	1
C5	180004	4700µF 16V AL. ELECT.	WIMA	PRINTILYT I	1
C6	101103	10nF 25% 250V CER DISC	ITT	CD10	1
C7	180026	10µF 350V AL. ELECT.	ITT	EN12.12 10/350	1
C8	104030	100pF 10% 4KV CERDISC	ITT	HD16	1
C9	120032	100nF 10% 160V POLYCARB	ASHCROFT	A2B3321B	1
C10	110004	47nF 20% 250V POLYESTER	MULLARD	C280AEP47K	1
D1	200022	3A 400V GP SI DIODE	MOTOROLA	BY252	2
D2	200022	3A 400V GP SI DIODE	MOTOROLA	BY252	—
D3	210027	2V7 400mW ZENER	MULLARD	BZY88C2V7	1
D4	214012	2V45 30ppm ZENER	FERRANTI	ZN458	1
D5	213006	5V 5W ZENER	UNITRODE	TVS505	1
D6	210068	6V8 400mW ZENER	MULLARD	BZY88C6V8	1
D7	213004	180V ½W ZENER	MOTOROLA	IN5279B	1

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.						
E.C.O.						
DATE						
CHKD.						

DATE 16-11-81	datron ELECTRONICS LTD
DRAWN JK	TITLE 4000 OUT GUARD POWER SUPPLY ASSY
CHECKED	
APPROVED	DRAWING NUMBER 400470
DATE	SHEET 3 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
Q1	250011	Si PNP TRANSISTOR	NATIONAL	BC327/TO18	1
Q2	240024	Si NPN TRANSISTOR	NATIONAL	TIP31A	1
Q3	240018	Si NPN TRANSISTOR	MOTOROLA	MJE340	2
Q4	240018	Si NPN TRANSISTOR	MOTOROLA	MJE340	—
Q5	250016	Si PNP TRANSISTOR	MOTOROLA	MJ2955	2
Q6	250016	Si PNP TRANSISTOR	MOTOROLA	MJ2955	—
M1	260061	3140 OP AMP	RCA	CA3140E	1
W1	209013	1A5 600v BRIDGE RECT	MICRO-ELECTRONICS	W006	1
F1	920128	4A FUSE 20mm SLO-B	BELLING LEE	L2080A/4	1
	410179-3A	P.C.B			1
	540002	22 SWG TINNED CU WIRE			A/R
	604042	4 WAY ·156" LOCKING RAMP GOLD	MOLEX	09-72-2041	2
	605059	8 WAY DIL SOCKET			1
	611006	M3X10mm POZIPAN SCREW	GKN		6
	611004	M3X6mm POZIPAN SCREW	GKN		3

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.												
E.C.O.												
DATE												
CHKD.												

DATE 16-11-81

DRAWN JR

CHECKED

APPROVED

DATE

datron ELECTRONICS LTD

TITLE 4000 OUT GUARD POWER SUPPLY ASSY

DRAWING NUMBER 400470 SHEET 4 OF 5

J.W. 1164

DESIGNATOR	DATRON PART No.	DESCRIPTION	PRINCIPAL MANUFACTURER	MANUFACTURER'S PART No.	No. USED Per Assy.
	613005	M3 SHAKEPROOF WASHER	GKN		9
	613007	M3 FLAT STEEL WASHER	GKN		3
	615002	M3 STEEL HEX NUT	GKN		9
	630024	STEATITE BEAD 16SWG	PARK ROYAL PORCELAIN	N°2	6
	900003	HEAT SINK COMPOUND	RS	554-311	A/R
	920088-1	TO-3 HEATSINK	SEE DRG		2
	920090-1	2X TO220 HEATSINK	SEE DRG		2
	920126	FUSE HOLDER PCB MT	BELLING LEE	L1426	1
	900004	SILICONE RUBBER COMPOUND	RS	555-588	A/R
	590004	PTFE SLEEVE	HELLERMANN ELECTRIC	FE10	A/R
	620007	TEST POINT TERMINAL	MICROVAR	C30	7

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

ISS.												
E.C.O.												
DATE												
CHKD.												

DATE 16-11-81

DRAWN JR

CHECKED

APPROVED

DATE

datron ELECTRONICS LTD

TITLE 4000 OUT GUARD POWER SUPPLY ASSY

DRAWING NUMBER 400470 SHEET 5 OF 5

J.W. 1164

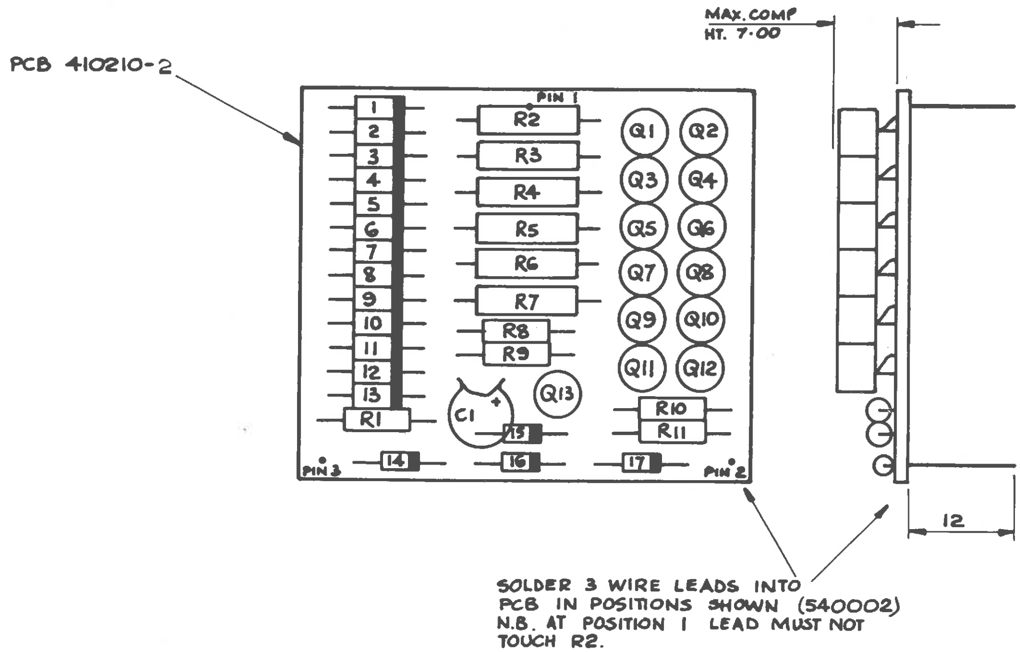
400472

THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH B.S. 308

ALL BURRS TO BE REMOVED

ISS.	CHANGES
1	RELEASED 16.4.82

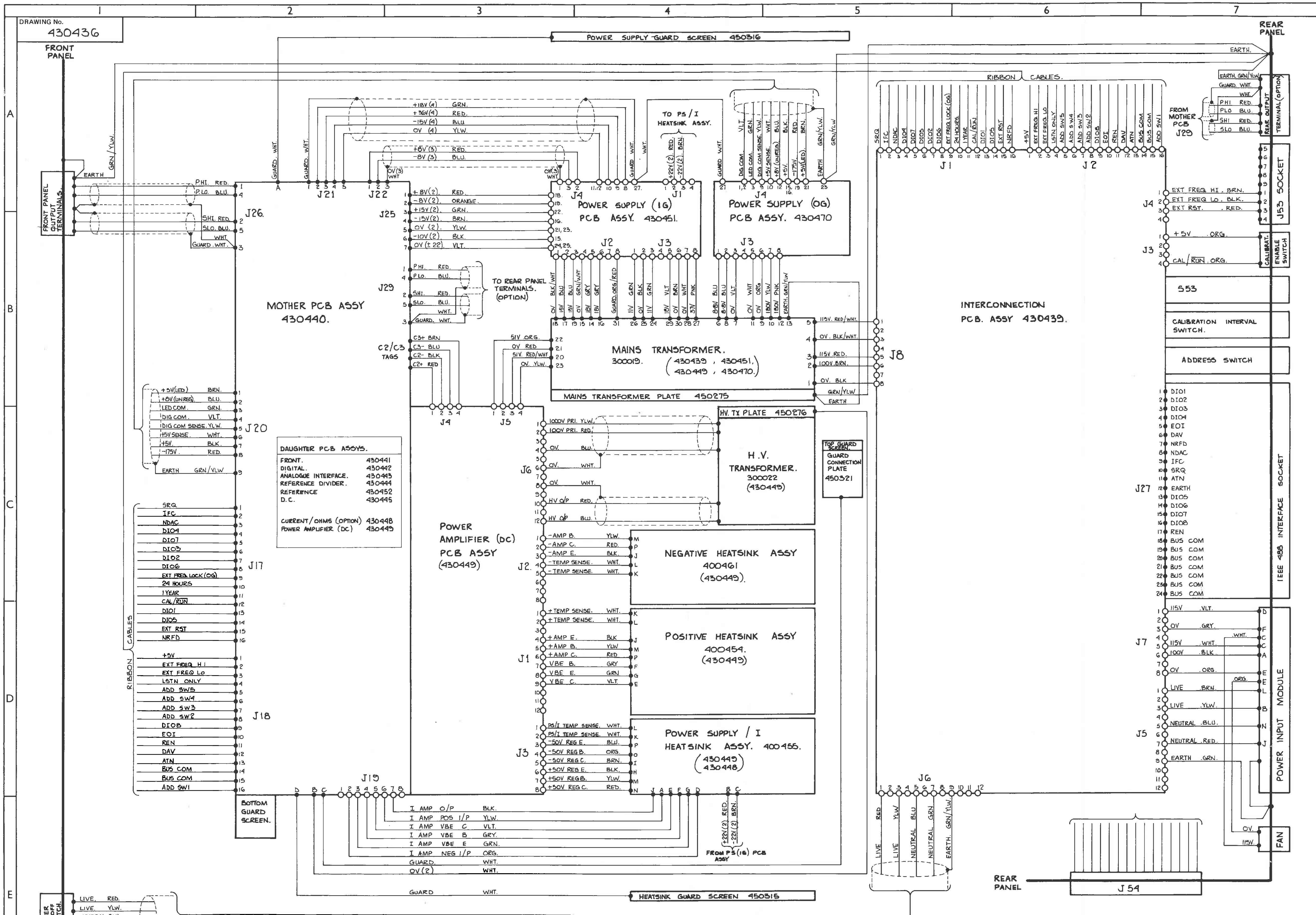


DRAWN	DATE 5.4.82	DIMENSIONS IN MILLIMETRES	TOLERANCES ANGULAR ± ½° DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm UNLESS OTHERWISE STATED	MATERIAL ———	datron ELECTRONICS LTD. NORWICH	DRAWING SIZE A4
CHKD	DATE 16.4.82	SCALE 2:1		FINISH ———	TITLE 4000 CONSTANT CURRENT ASSY.	DRAWING No. 400472 / SHEET 1 OF 4
APPD.	DATE 23.4.82	NOT TO BE SCALED				

J.W. 1786

4961HT

DRAWING No. 430436



ISS.	CHANGES
A	17th MAY 82
1	RELEASED 25-5-82

DRAWN B. JACKSON	DATE 17th MAY 82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL
CHECKED	DATE 25.5.82.	SCALE —	UNLESS OTHERWISE STATED	FINISH
APPR.	DATE 4.6.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION	

ASSY DRG & PARTS LIST: 400436.
CIRCUIT DIAGRAM: —
CHECK PROCEDURE: 460436
CHECK LIST: 470436

TITLE: 4000 INTERCONNECTION DIAGRAM.

datron ELECTRONICS LIMITED NORWICH

DRAWING No. 430436

SHEET 1 OF 1

DRAWING No. 400439

FIRST USED ON 4000

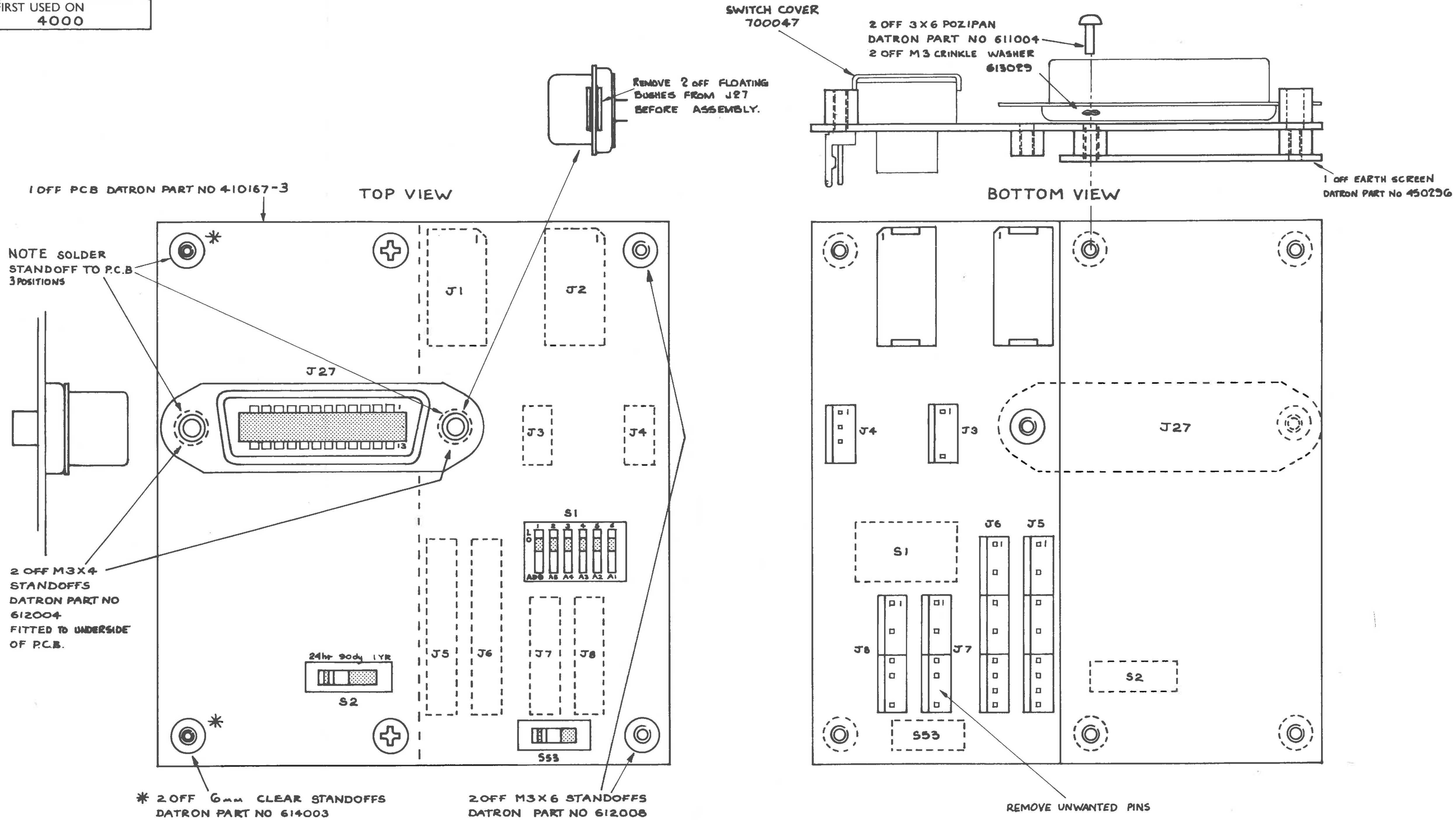
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

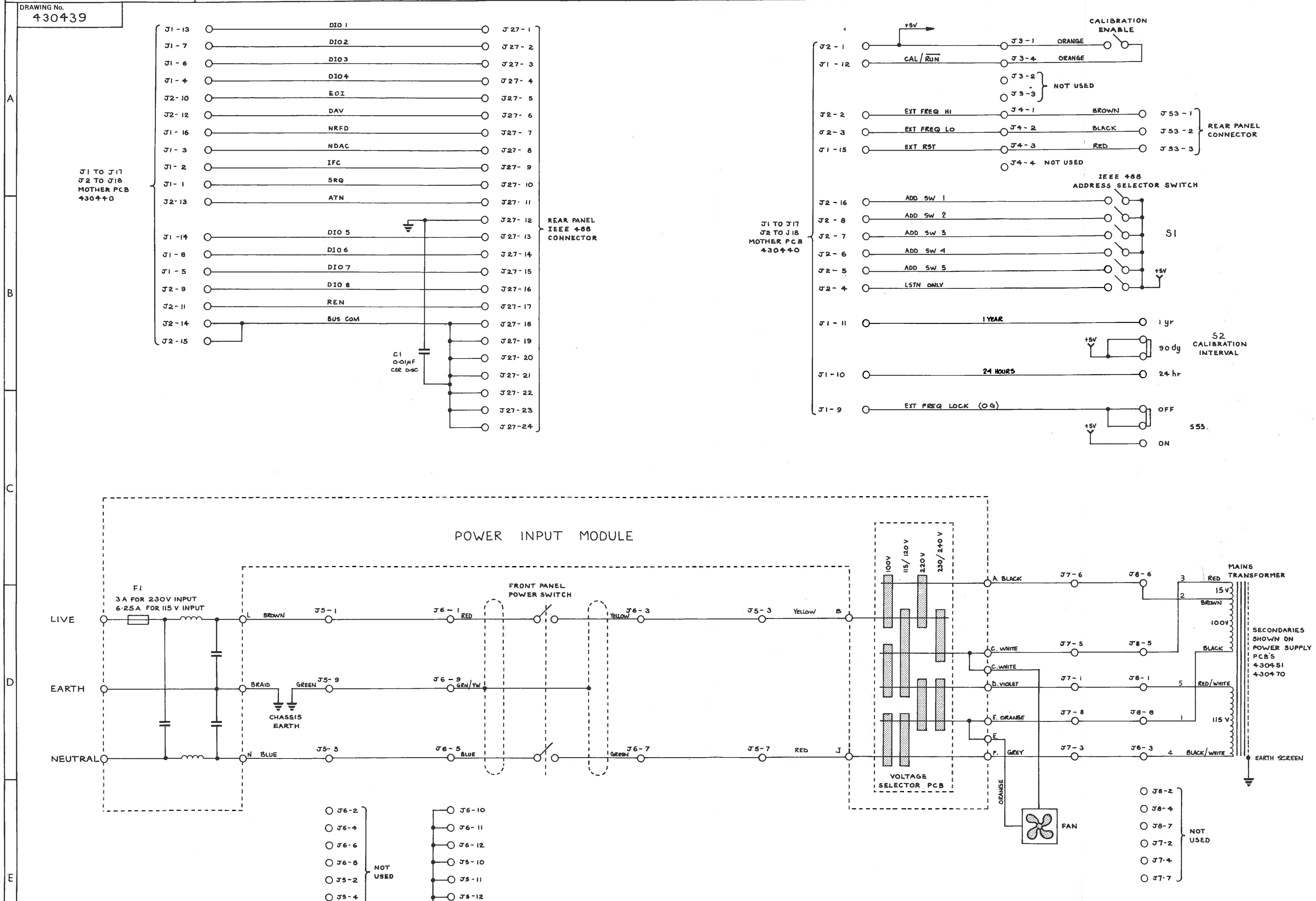
ISS.	CHANGES
B	5-8-81.
1	29th MAR 82 RELEASED



datron ELECTRONICS LIMITED NORWICH

DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST 400439	TITLE	DRAWING No.
J.R.	24.7.81.		DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR ± ½°	——	CIRCUIT DIAGRAM 430439	4000 INTERCONNECTION PCB ASSY	400439
CHECKED	DATE 29.3.82	SCALE 2:1		FINISH ——	CHECK PROCEDURE 460439		
APPR.	DATE 2.4.82	NOT TO BE SCALED	UNLESS OTHERWISE STATED THIRD ANGLE PROJECTION		CHECK LIST 470439		SHEET 1 OF 2

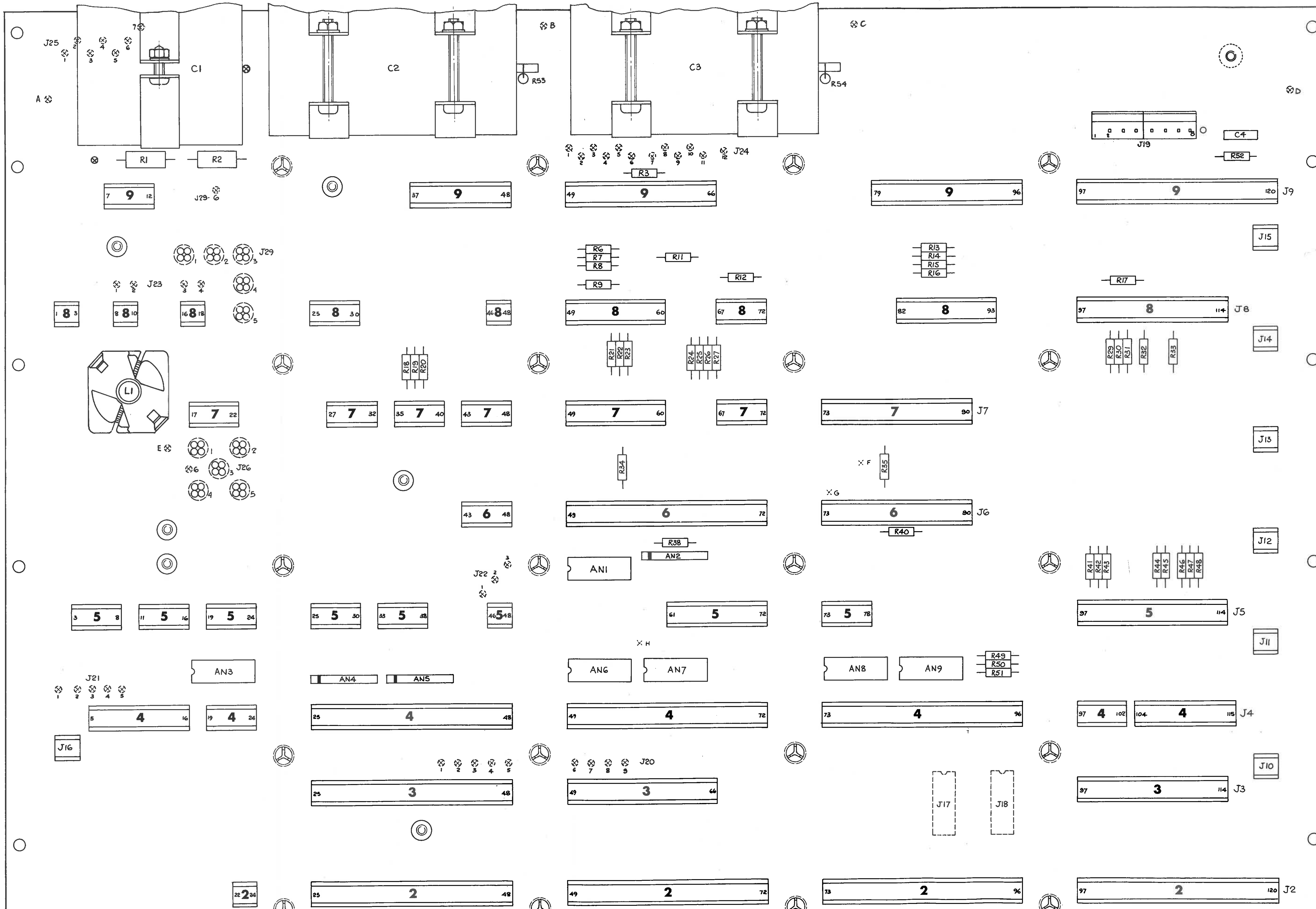
4951MT



DRAWN	DATE 30.7.81	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ±·1mm DECIMAL TO 1 PLACE ±·2mm WHOLE DIMENSIONS ±·4mm ANGULAR ±½°	MATERIAL	ASSY DRG & PARTS LIST 400439	TITLE 4000 INTERCONNECTION PCB	DRAWING No. 430439
CHECKED	DATE 2.4.82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM		
APPR. B Hume	DATE 2.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460439 CHECK LIST 470439		SHEET 1 OF 1

ISS.	CHANGES
B	5-8-81
1	29th MAR 82 RELEASED. BJ.
2	C1 ADDED. ECO 1466 BJ. 11th APRIL 83.

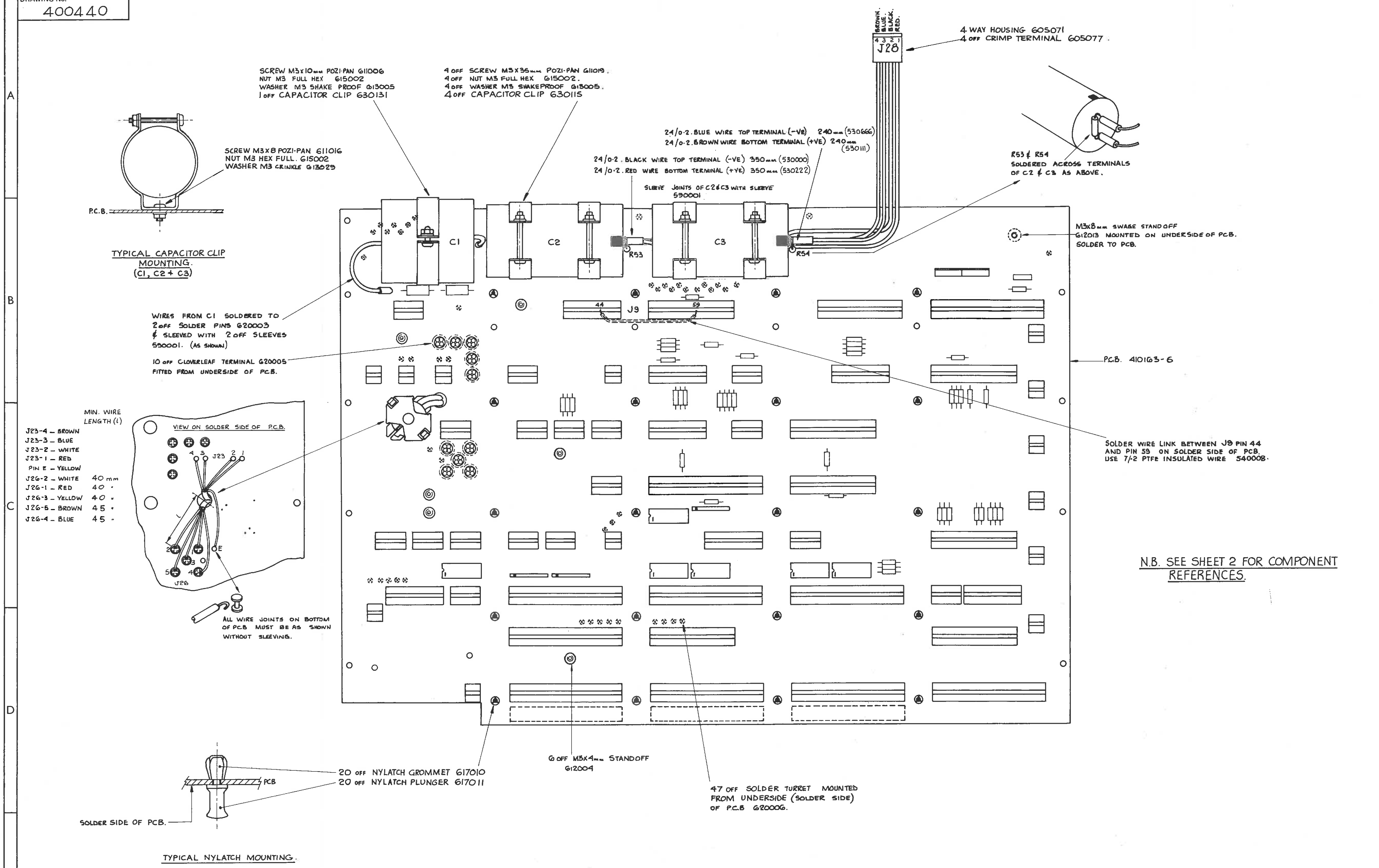
datron ELECTRONICS LIMITED NORWICH



ISS.	1	2	3	4	5				
E.C.O.	RELEASED	1330.34	1387	1397	1511				
DATE.	29-3-82	24-5-82	24-8-82	9.9.82	13.7.83				
CHKD.	MD	MD	MD	MD	MD				

400440 SH 2

DRAWING No. 400440



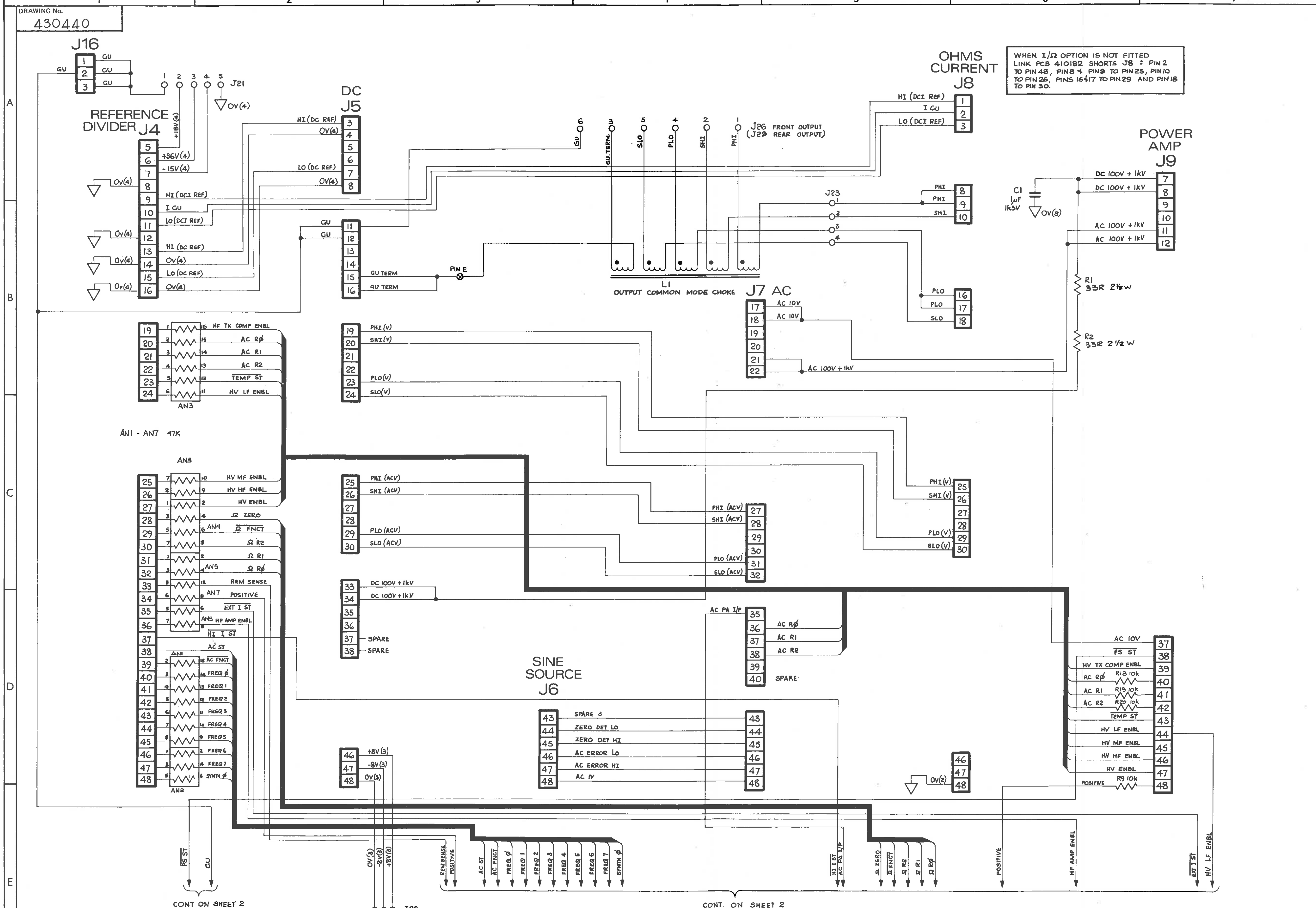
ISS.	CHANGES
C	
1	RELEASED 29-3-82
2	ECO 1330.1334 J27 (4 HARWIN PINS) DELETED. J8 WAS 24 WAY CONNECTOR. CABLE DELETED + SOLDER TURRETS F.G.+H. JR 24.5.82
3	ECO 1387 J1 PINS 115 TO 117 DELETED. J1 WAS 6 OFF 12 WAY MOLEX PCB WAS ISS 5. JR 24·8·82
4	ECO.1397 R4.R5. R36 + R37 DELETED IL 9.9.82
5	ECO.1511 R10 DELETED. LINK BETWEEN J9 PIN 44 AND 59 ADDED. IL 12.7.83

datron ELECTRONICS LIMITED NORWICH

DRAWN IL	DATE 19.11.81	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ±·1mm; DECIMAL TO 1 PLACE ±·2mm; WHOLE DIMENSIONS ±·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400440	TITLE 4000 MOTHER PCB ASSY.
CHECKED	DATE 2.4.82	SCALE 1:1	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430440	DRAWING No. 400440
APPR. B Hume	DATE 6.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460440; CHECK LIST 470440	SHEET 1 OF 8

4951MT

DRAWING No. 430440

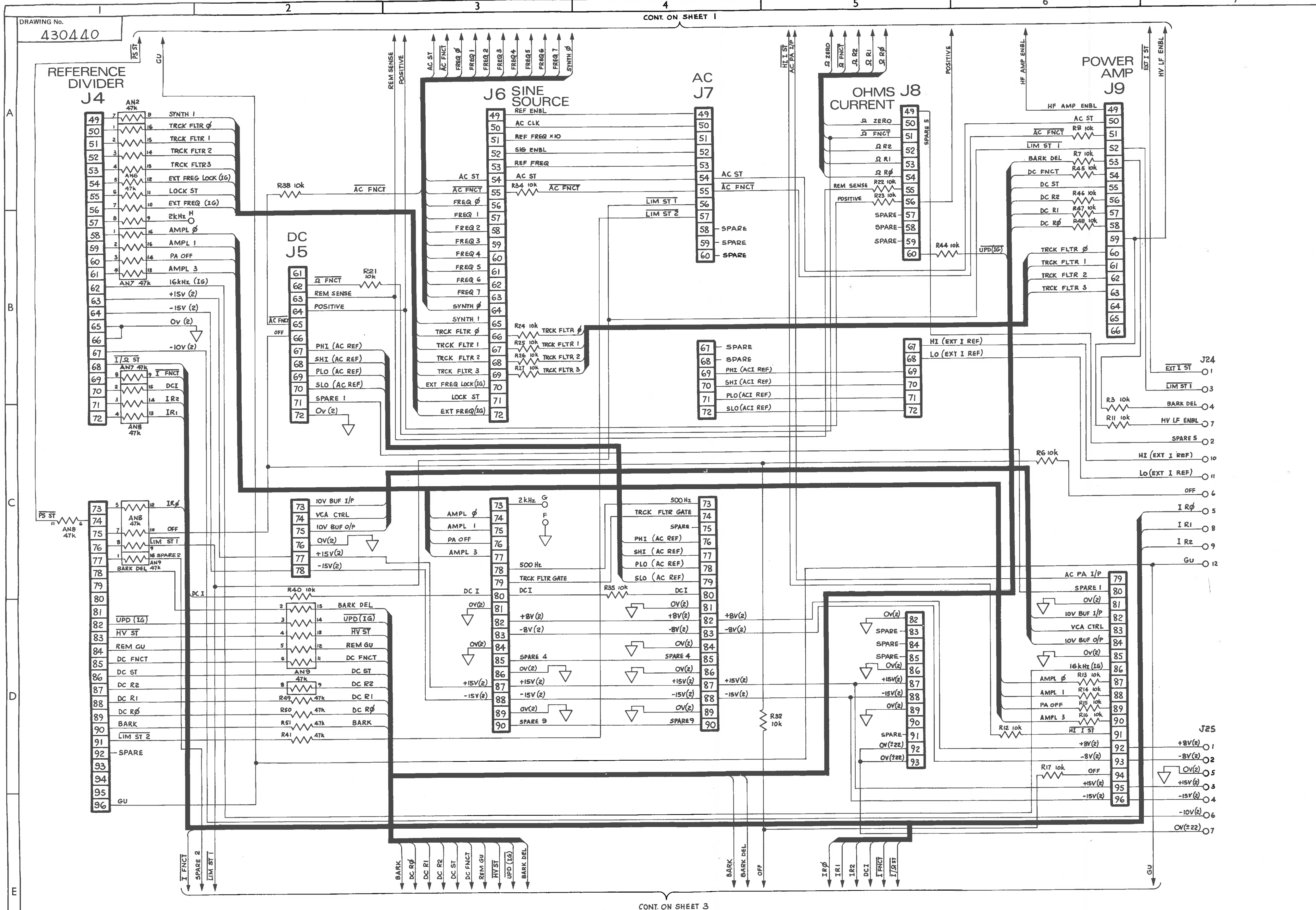


ISS.	CHANGES
F	
1	RELEASED 29.3.82.
2	ECO 1330, 1334 SEE SHEETS 2+4 JR 13.5.82
3	SEE SHEET 4
4	ECO. 1397 R4, R5, R36 AND R37 DELETED IL 9.9.82
5	ECO. 1511 SIGNAL LINE 'HV LF ENBL' FROM J9-44 TO J9-59 (SHT. 2) ADDED IL 13.7.83

datron ELECTRONICS LIMITED NORWICH

DRAWN IL	DATE 18.1.82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ±·1mm DECIMAL TO 1 PLACE ±·2mm WHOLE DIMENSIONS ±·4mm ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400440	TITLE 4000 MOTHER P.C.B.
CHECKED R.K. COGGAN	DATE 5.4.82	SCALE		FINISH	CIRCUIT DIAGRAM	DRAWING No. 430440
APPD	DATE 6.4.82	NOT TO BE SCALED	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION		CHECK PROCEDURE 460440 CHECK LIST 470440	SHEET 1 OF 4

DRAWING No. 430440



ISS.	CHANGES
	SEE SHEET 1
1	RELEASED 29-3-82
2	ECO 1330.1334 CABLE FROM J6-73 TO AN7-16 DELETED. JR 13.5.82
3	SEE SHEET 4
4	SEE SHEET. 1
5	ECO J511 R10 DELETED SIGNAL LINE 'HV LF ENBL' FROM J9-59 TO J9-44 (SHT.1) ADDED. SIGNAL LINE 'BARK' FROM J9-59 TO J8-107 DELETED. 13.7.83

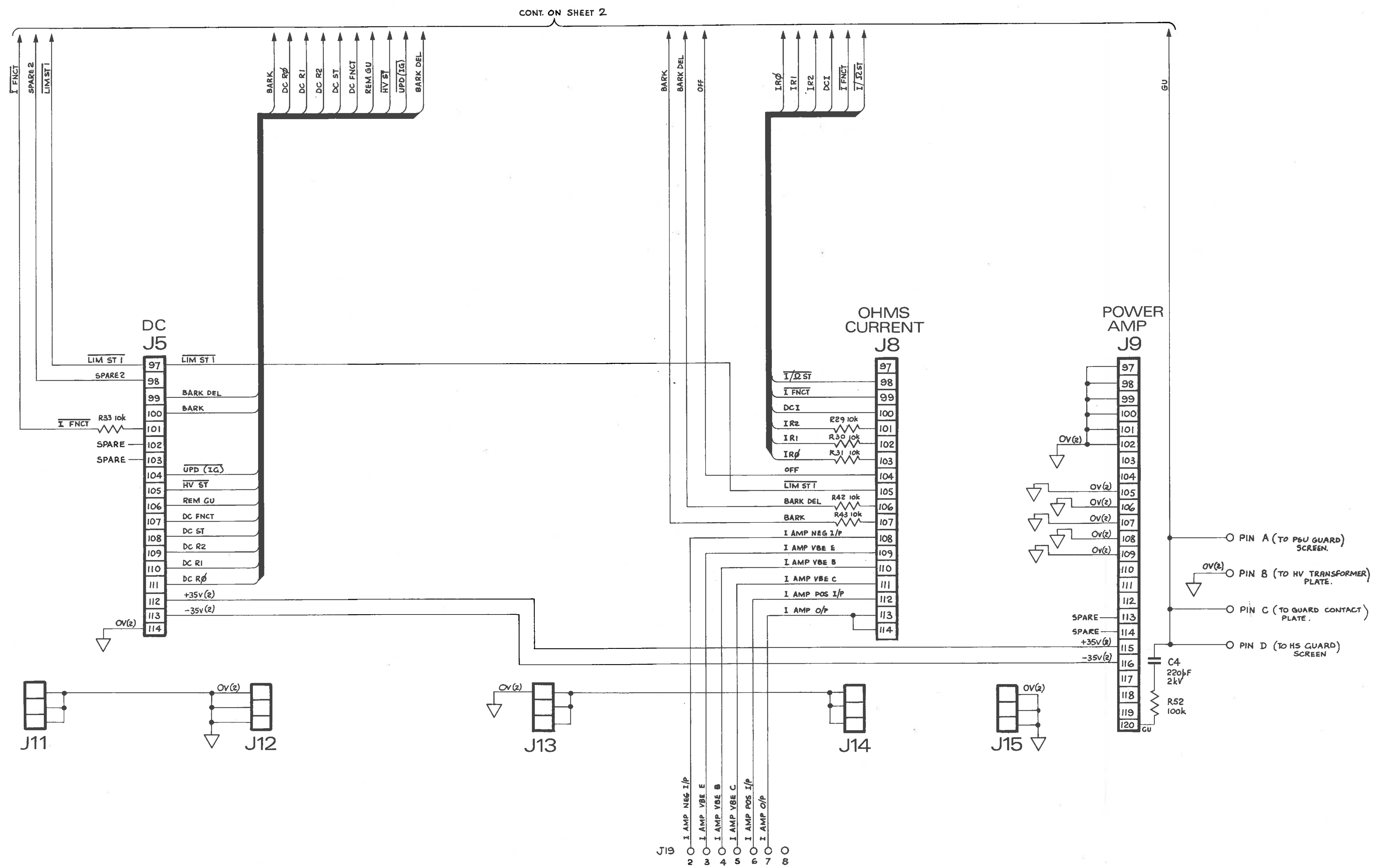
datron ELECTRONICS LIMITED NORWICH

DRAWN	DATE 18.1.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400440	TITLE 4000 MOTHER P.C.B.
CHECKED R.K. COGGAN	DATE 5.4.82	SCALE		FINISH	CIRCUIT DIAGRAM	
APPR.	DATE 6.4.82	NOT TO BE SCALED	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION		CHECK PROCEDURE 460440; CHECK LIST 470440	

DRAWING No. 430440

SHEET 2 OF 4

DRAWING No. 430440

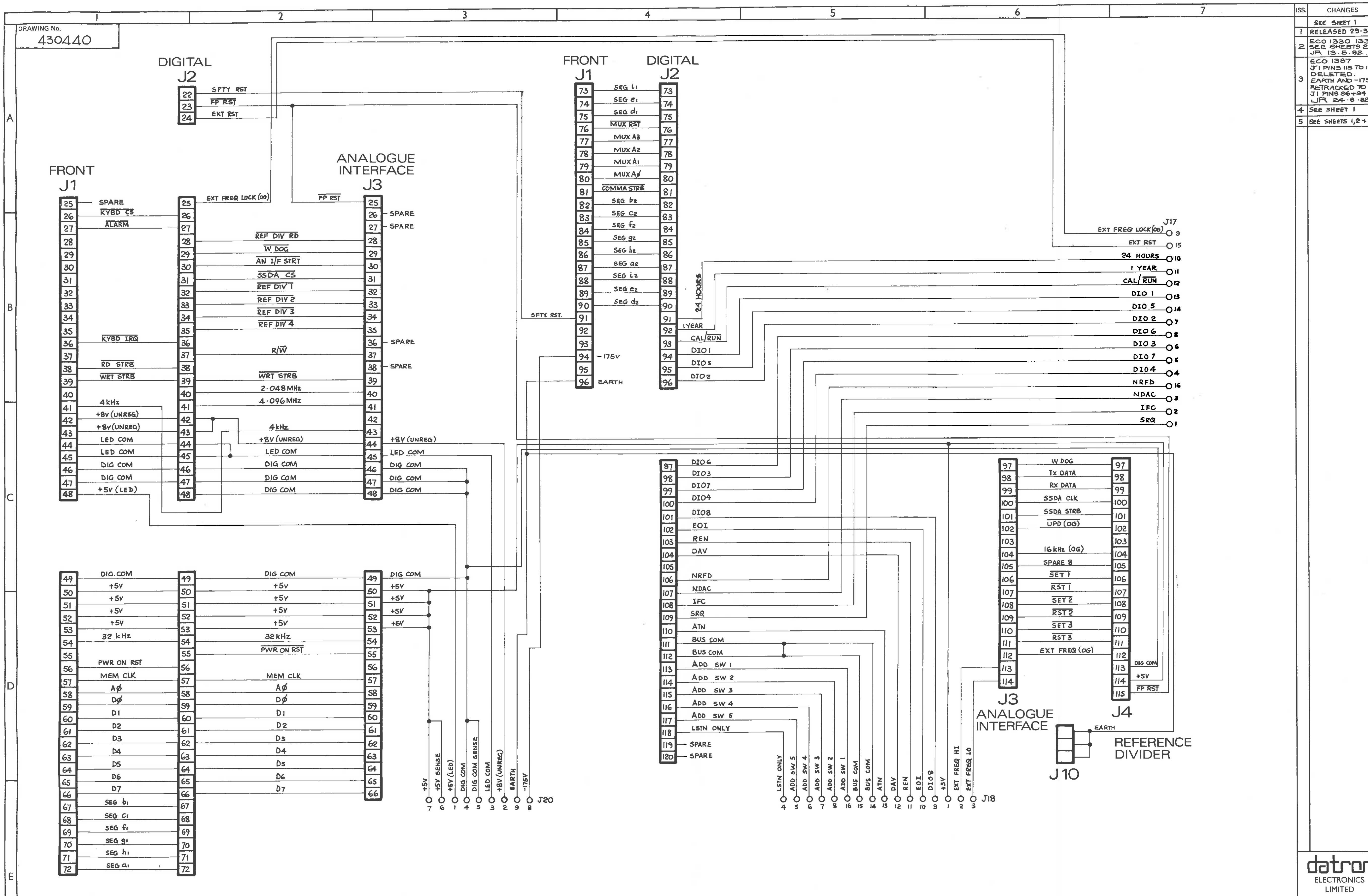


ISS.	CHANGES
	SEE SHEET 1
1	RELEASED 29-3-82
2	ECO 1330,1334 J27 DELETED J8 PINS 115 TO 120 ALSO DELETED. JR 13.5.82
3	SEE SHEET 4.
4	SEE SHEET 1
5	ECO. 1511 SIGNAL LINE 'BARK' FROM J8-107 TO J9-59 DELETED. 13.7.83

datron ELECTRONICS LIMITED NORWICH

DRAWN	DATE 18.1.82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR + ½°	MATERIAL ———	ASSY DRG & PARTS LIST 400440	TITLE 4000 MOTHER P.C.B.	DRAWING No. 430440
CHECKED R.K. COGGAN	DATE 5.4.82	SCALE ———	UNLESS OTHERWISE STATED	FINISH ———	CIRCUIT DIAGRAM		
APPR. B	DATE 6.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460440		SHEET 3 OF 4
					CHECK LIST 470440		

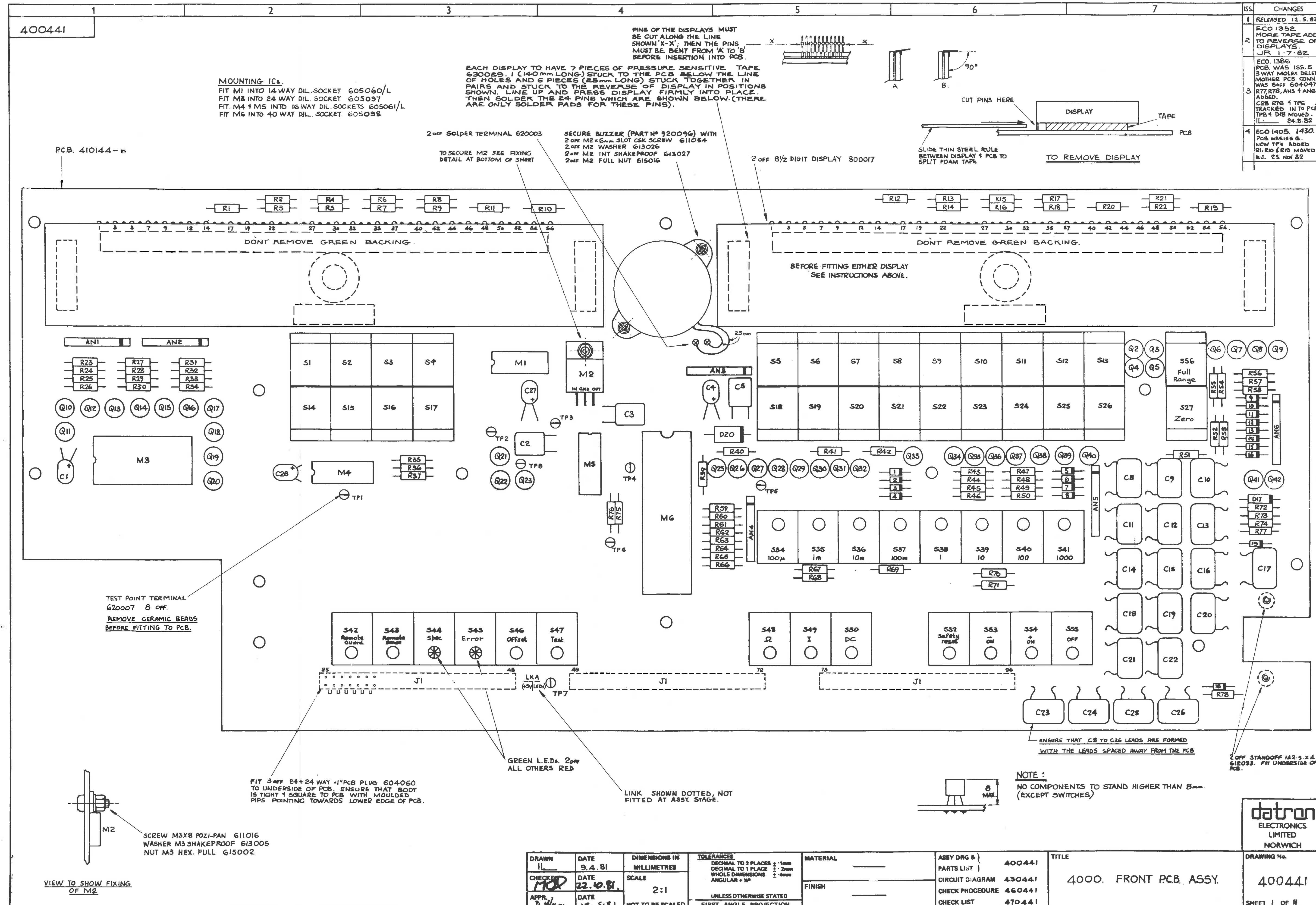
4951MT

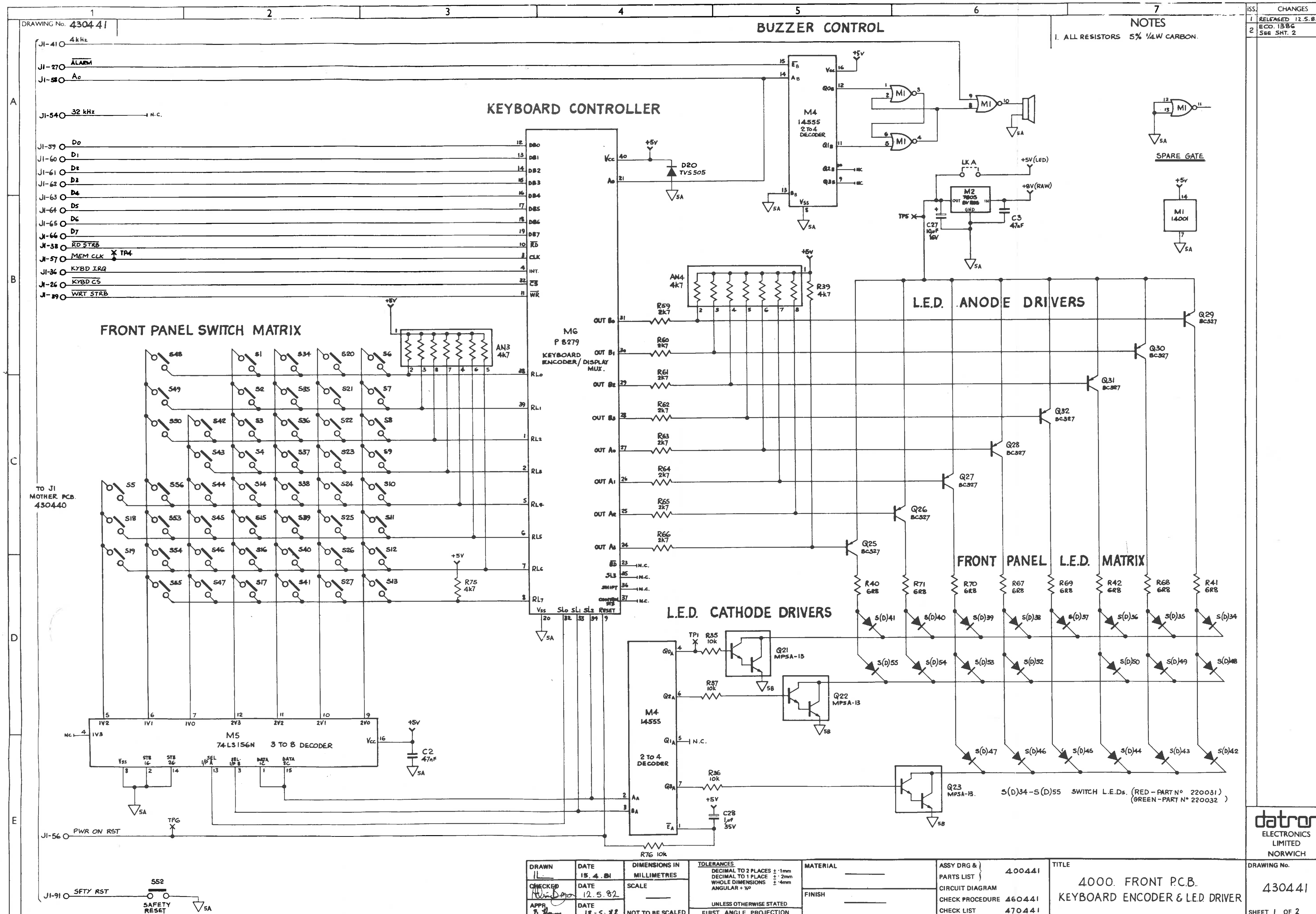


ISS.	CHANGES
	SEE SHEET 1
1	RELEASED 29-3-82
2	ECO 1330 1334 SEE SHEETS 2+4 JR 13.5.82.
3	ECO 1387 J1 PINS 115 TO 117 DELETED. EARTH AND -175V RETRACKED TO J1 PINS 96+94. JR 24.8.82
4	SEE SHEET 1
5	SEE SHEETS 1,2+3

datron ELECTRONICS LIMITED NORWICH

DRAWN JL	DATE 18.1.82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm, DECIMAL TO 1 PLACE ± ·2mm, WHOLE DIMENSIONS ± ·4mm, ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400440	TITLE 4000 MOTHER P.C.B.
CHECKED R.K.COGGAN	DATE 5-4-82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM	DRAWING No. 430440
APPR.	DATE 6.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460440	
					CHECK LIST 470440	SHEET 4 OF 4


400441
MOUNTING ICs.
FIT M1 INTO 14 WAY DIL. SOCKET 605060/L
FIT M3 INTO 24 WAY DIL. SOCKET 605097
FIT M4 & M5 INTO 16 WAY DIL. SOCKETS 605061/L
FIT M6 INTO 40 WAY DIL. SOCKET 605098
PINS OF THE DISPLAYS MUST BE CUT ALONG THE LINE SHOWN 'X-X'; THEN THE PINS MUST BE BENT FROM 'A' TO 'B' BEFORE INSERTION INTO PCB.
EACH DISPLAY TO HAVE 7 PIECES OF PRESSURE SENSITIVE TAPE 630029. 1 (140mm LONG) STUCK TO THE PCB BELOW THE LINE OF HOLES AND 6 PIECES (25mm LONG) STUCK TOGETHER IN PAIRS AND STUCK TO THE REVERSE OF DISPLAY IN POSITIONS SHOWN. LINE UP AND PRESS DISPLAY FIRMLY INTO PLACE. THEN SOLDER THE 24 PINS WHICH ARE SHOWN BELOW. (THERE ARE ONLY SOLDER PADS FOR THESE PINS).
CUT PINS HERE
DISPLAY
TAPE
PCB
SLIDE THIN STEEL RULE BETWEEN DISPLAY & PCB TO SPLIT FOAM TAPE
TO REMOVE DISPLAY
P.C.B. 410144-6
2 off SOLDER TERMINAL 620003
TO SECURE M2 SEE FIXING DETAIL AT BOTTOM OF SHEET
SECURE BUZZER (PART Nº 920096) WITH
2 off M2×6mm SLOT CSK SCREW 611054
2 off M2 WASHER 613026
2 off M2 INT SHAKEPROOF 613027
2 off M2 FULL NUT 615016
2 off 8½ DIGIT DISPLAY 800017
DONT REMOVE GREEN BACKING.
BEFORE FITTING EITHER DISPLAY SEE INSTRUCTIONS ABOVE.
S34 100µ
S35 1m
S36 10m
S37 100m
S38 1
S39 10
S40 100
S41 1000
S56 Full Range
S27 Zero
S42 Remote Guard
S43 Remote Sense
S44 Spec
S45 Error
S46 Offset
S47 Test
S48 Ω
S49 I
S50 DC
S52 Safety reset
S53 ON
S54 ON
S55 OFF
TEST POINT TERMINAL 620007 8 off.
REMOVE CERAMIC BEADS BEFORE FITTING TO PCB.
ENSURE THAT C8 TO C26 LEADS ARE FORMED WITH THE LEADS SPACED AWAY FROM THE PCB
2 off STANDOFF M2.5 x 4mm 612023. FIT UNDERSIDE OF PCB.
GREEN L.E.Ds. 2 off ALL OTHERS RED
FIT 3 off 24+24 WAY ·1" PCB PLUG 604060 TO UNDERSIDE OF PCB. ENSURE THAT BODY IS TIGHT & SQUARE TO PCB WITH MOULDED PIPS POINTING TOWARDS LOWER EDGE OF PCB.
LINK SHOWN DOTTED, NOT FITTED AT ASSY. STAGE.
NOTE: NO COMPONENTS TO STAND HIGHER THAN 8mm. (EXCEPT SWITCHES)
SCREW M3X8 POZI-PAN 611016
WASHER M3 SHAKEPROOF 613005
NUT M3 HEX. FULL 615002
VIEW TO SHOW FIXING OF M2
ISS. CHANGES
1 RELEASED 12.5.82
2 ECO 1352 MORE TAPE ADDED TO REVERSE OF DISPLAYS. JR 1.7.82
3 ECO. 1386 PCB. WAS ISS.5 3 WAY MOLEX DELETED MOTHER PCB CONN WAS 6off 604047 R77, R78, AN5 & AN6 ADDED. C28 R76 & TP8 TRACKED IN TO PCB. TP5 & D18 MOVED. IL 24.8.82
4 ECO 1405. 1430. PCB WAS ISS 6. NEW TP's ADDED R1, R10 & R19 MOVED BJ. 25 NOV 82
DRAWN IL DATE 9.4.81
CHECKED DATE 22.10.81
APPR. DATE 18.5.81
DIMENSIONS IN MILLIMETRES
SCALE 2:1
NOT TO BE SCALED
TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR ± ½°
UNLESS OTHERWISE STATED
FIRST ANGLE PROJECTION
MATERIAL
FINISH
ASSY DRG & PARTS LIST 400441
CIRCUIT DIAGRAM 430441
CHECK PROCEDURE 460441
CHECK LIST 470441
TITLE 4000. FRONT PCB. ASSY.
datron ELECTRONICS LIMITED NORWICH
DRAWING No. 400441
SHEET 1 OF 11



DRAWING No. 430441
BUZZER CONTROL
NOTES
1. ALL RESISTORS 5% 1/4W CARBON.
ISS. CHANGES
1 RELEASED 12.5.82.
2 ECO. 1386 SEE SHT. 2
KEYBOARD CONTROLLER
M4 14555 2 TO 4 DECODER
M6 P 8279 KEYBOARD ENCODER/DISPLAY MUX.
D20 TVS505
LK A
+5V (LED)
+8V (RAW)
M2 7805 5V REG
C3 47nF
C27 10µF 16V
SPARE GATE
M1 14001
AN4 4k7
R39 4k7
L.E.D. ANODE DRIVERS
FRONT PANEL SWITCH MATRIX
AN3 4k7
TO J1 MOTHER PCB. 430440
FRONT PANEL L.E.D. MATRIX
L.E.D. CATHODE DRIVERS
Q21 MPSA-13
Q22 MPSA-13
Q23 MPSA-13.
M4 14555 2 TO 4 DECODER
M5 74LS156N 3 TO 8 DECODER
C2 47nF
C28 1µF 35V
R76 10k
S(D)34 - S(D)55 SWITCH L.E.Ds. (RED - PART No 220031) (GREEN - PART No 220032)
J1-56 PWR ON RST
J1-91 SFTY RST
S52 SAFETY RESET
DRAWN 15.4.81
CHECKED 12.5.82
APPR. 18-5-82
DIMENSIONS IN MILLIMETRES
NOT TO BE SCALED
FIRST ANGLE PROJECTION
MATERIAL
FINISH
ASSY DRG & PARTS LIST 400441
CIRCUIT DIAGRAM
CHECK PROCEDURE 460441
CHECK LIST 470441
TITLE
4000. FRONT P.C.B. KEYBOARD ENCODER & L.E.D. DRIVER
DRAWING No. 430441
SHEET 1 OF 2
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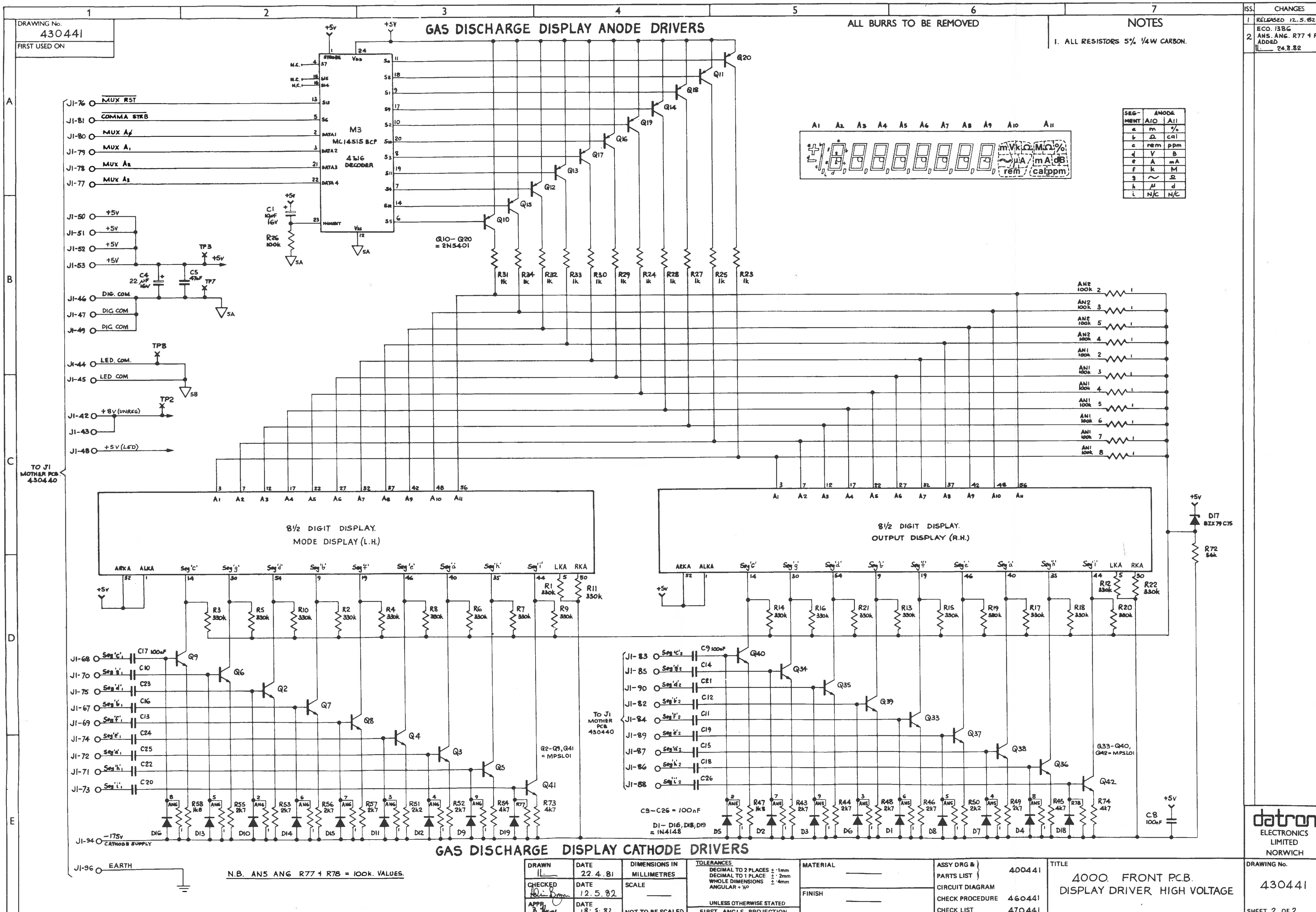

GAS DISCHARGE DISPLAY ANODE DRIVERS
ALL BURRS TO BE REMOVED
NOTES
1. ALL RESISTORS 5% 1/4W CARBON.
DRAWING No. 430441
FIRST USED ON
CHANGES
1 RELEASED 12.5.82.
2 ECO. 1386 ANS. ANG. R77 + R78 ADDED 24.8.82
M3 MC14515BCP 4-16 DECODER
Q10–Q20 = 2N5401
8½ DIGIT DISPLAY. MODE DISPLAY (L.H.)
8½ DIGIT DISPLAY. OUTPUT DISPLAY (R.H.)
TO J1 MOTHER PCB 430440
Q2–Q9, Q41 = MPSL01
Q33–Q40, Q42 = MPSL01
C9–C26 = 100nF
D1–D16, D18, D19 = 1N4148
D17 BZX79 C75
GAS DISCHARGE DISPLAY CATHODE DRIVERS
N.B. AN5 AN6 R77 + R78 = 100k. VALUES.
J1-96 EARTH
J1-94 –175v CATHODE SUPPLY
DRAWN 22.4.81
CHECKED 12.5.82
APPD. 18.5.82
DIMENSIONS IN MILLIMETRES
NOT TO BE SCALED
FIRST ANGLE PROJECTION
ASSY DRG & PARTS LIST 400441
CIRCUIT DIAGRAM
CHECK PROCEDURE 460441
CHECK LIST 470441
TITLE 4000 FRONT P.C.B. DISPLAY DRIVER HIGH VOLTAGE
datron ELECTRONICS LIMITED NORWICH
DRAWING No. 430441
SHEET 2 OF 2

DRAWING No. 400442. 400442A
FIRST USED ON

THIRD ANGLE PROJECTION

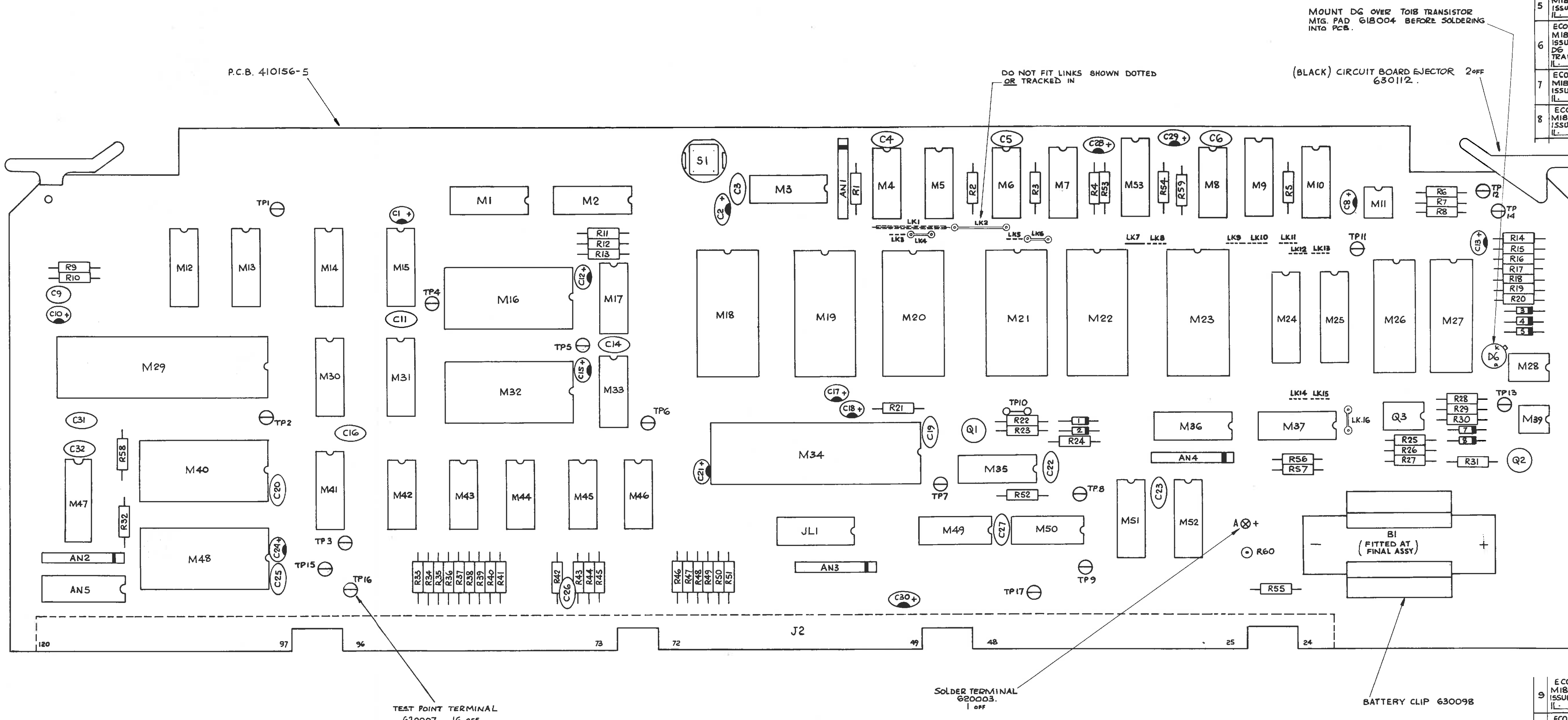
DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

ISS.	CHANGES
1	RELEASED 13.5.82
2	ECO 1339,1346 C7 DELETED + R26 AND R29 WERE 10M. JR 30·6·82
3	ECO. 1349 TO 1353 SOFTWARE UPDATE – PARTS LIST CHANGE ONLY. IL 23.8.82
4	ECO. 1379 M18-M22 WERE TO ISSUE 3 SOFTWARE. IL 14.9.82
5	ECO. 1401 M18-M22 WERE TO ISSUE 4 SOFTWARE IL 14.9.82
6	ECO. 1404. 1408. 1418. M18-M22 WERE TO ISSUE 5 SOFTWARE D6 NOW STOOD ON TRANSISTOR MTG. PAD IL 24.11.82
7	ECO. 1443. 1453. M18-M22 WERE TO ISSUE 6/7 SOFTWARE IL 22.2.83
8	ECO. 1456 M18-M22 WERE TO ISSUE 8 SOFTWARE IL 11.4.83

CONT...



ISS.	CHANGES
9	ECO 1488 M18-M22 WERE TO ISSUE 8A SOFTWARE IL 6.6.83
10	ECO. 1511 M18-M22 WERE TO ISSUE 9 SOFTWARE IL 12.7.83
11	ECO. 1533 M18-M22 WERE TO ISSUE 10 SOFTWARE IL 29.9.83.

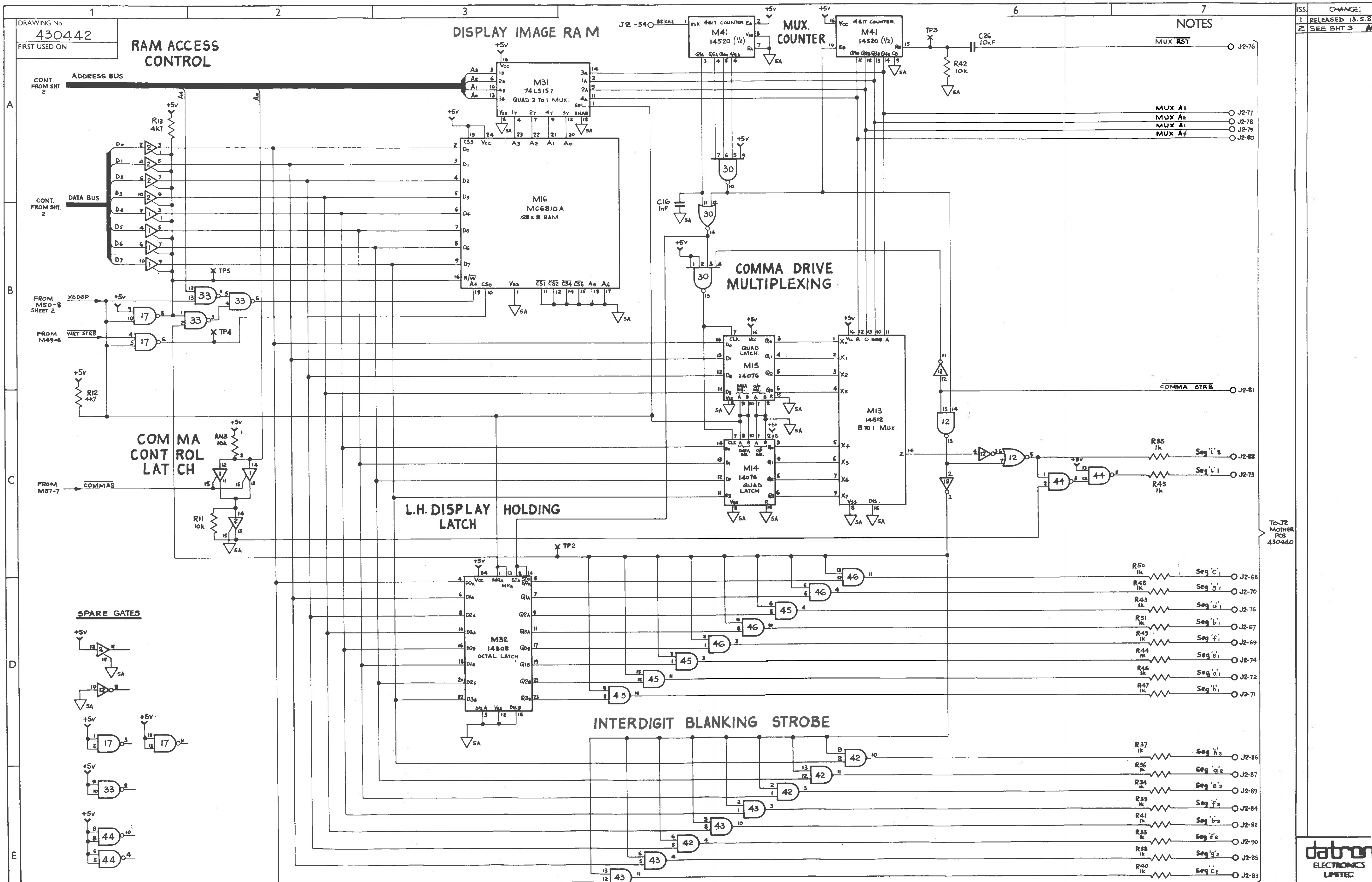
MOUNTING I.Cs.

FIT M11 + M39 INTO 6-WAY DIL. SOCKET 605066 2 OFF
FIT M28 + Q3 INTO 8-WAY DIL SOCKET 605059 2 OFF
FIT M4-M8, M10, M17, M33, M42-M46, M49 + M50 INTO 14-WAY DIL SOCKET 605060. 15 OFF
FIT M1-M3, M9, M12-M15, M30, M31, M35-M37, M41, JL1, M47, M51–M53 INTO 16-WAY DIL SOCKET 605061. 19 OFF
FIT M24 + M25 INTO 18-WAY DIL SOCKET 605062. 2 OFF
FIT M26 + M27 INTO 22-WAY DIL SOCKET 605063 2 OFF
FIT M16, M18-M23, M32, M40 + M48 INTO 24-WAY DIL SOCKET 605064. 10 OFF
FIT M29 + M34 INTO 40-WAY DIL SOCKET 605050 2 OFF

datron ELECTRONICS LIMITED NORWICH

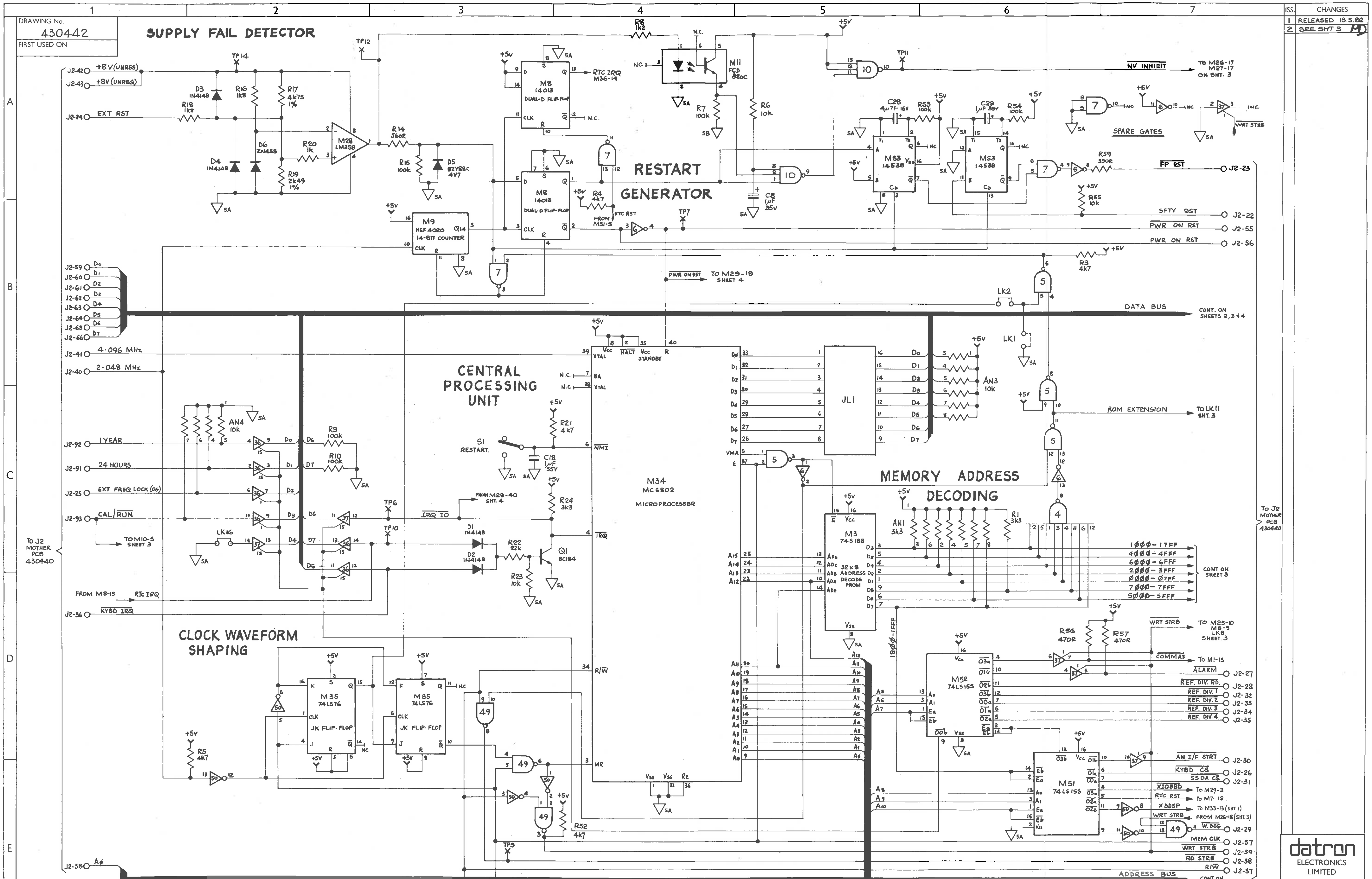
DRAWN IL	DATE 20.5.81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½° UNLESS OTHERWISE STATED	MATERIAL ______	ASSY DRG & PARTS LIST 400442(A)	TITLE	DRAWING No. 400442 400442A
CHECKED	DATE 6.6.82	SCALE 2:1		FINISH ______	CIRCUIT DIAGRAM 430442(A)	4000. DIGITAL P.C.B. ASSY.	
APPR.	DATE 17.5.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460442(A); CHECK LIST 470442(A)		SHEET 1 OF 11

4951MT



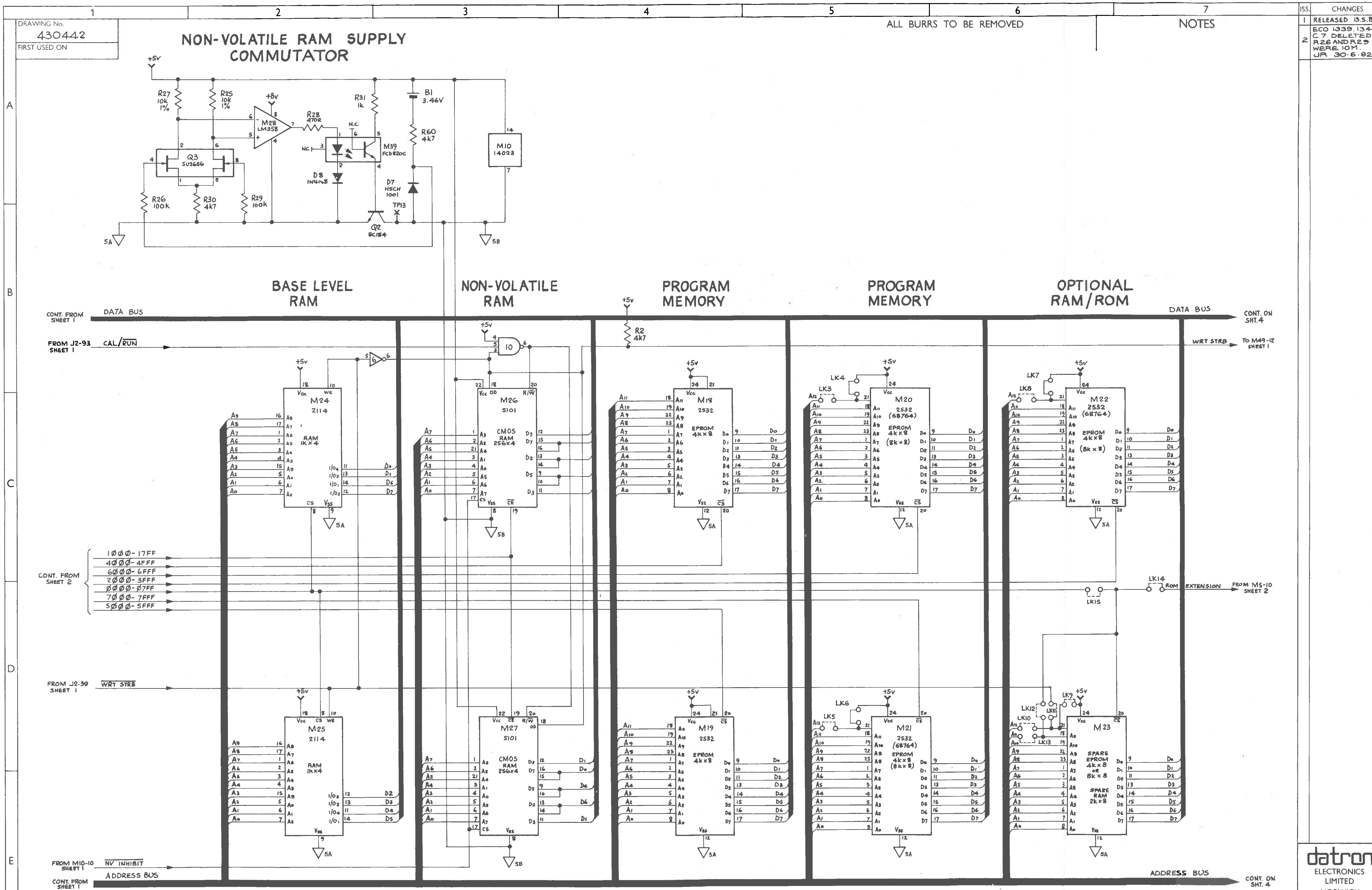
DRAWN	DATE 11.5.81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400442	TITLE 4000. DIGITAL P.C.B. DISPLAY MULTIPLEXING LOGIC	DRAWING No. 430442
CHECKED	DATE 6.6.82	SCALE —	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM; CHECK PROCEDURE 460442		
APPR.	DATE 17.5.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST 470442		SHEET 1 OF 5

datron ELECTRONICS LIMITED NORWICH



DRAWN	DATE 7.7.81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400442	TITLE 4000 DIGITAL P.C.B. MICROPROCESSOR	DRAWING No. 430442
CHECKED	DATE 6.6.82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM		
APPR. B Hume	DATE 17.5.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460442; CHECK LIST 470442		SHEET 2 OF 5

datron ELECTRONICS LIMITED NORWICH



DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400442	TITLE	DRAWING No.
JL	7.7.81		DECIMAL TO 2 PLACES ± .1mm; DECIMAL TO 1 PLACE ± .2mm; WHOLE DIMENSIONS ± .4mm; ANGULAR ± ½°		CIRCUIT DIAGRAM		4000 DIGITAL P.C.B. MEMORY & BATTERY BACK-UP	430442
CHECKED	DATE 6.6.82	SCALE	UNLESS OTHERWISE STATED	FINISH	CHECK PROCEDURE	460442		
APPR.	DATE 17.5.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST	470442		SHEET 3 OF 5

DRAWING No. 430442

FIRST USED ON

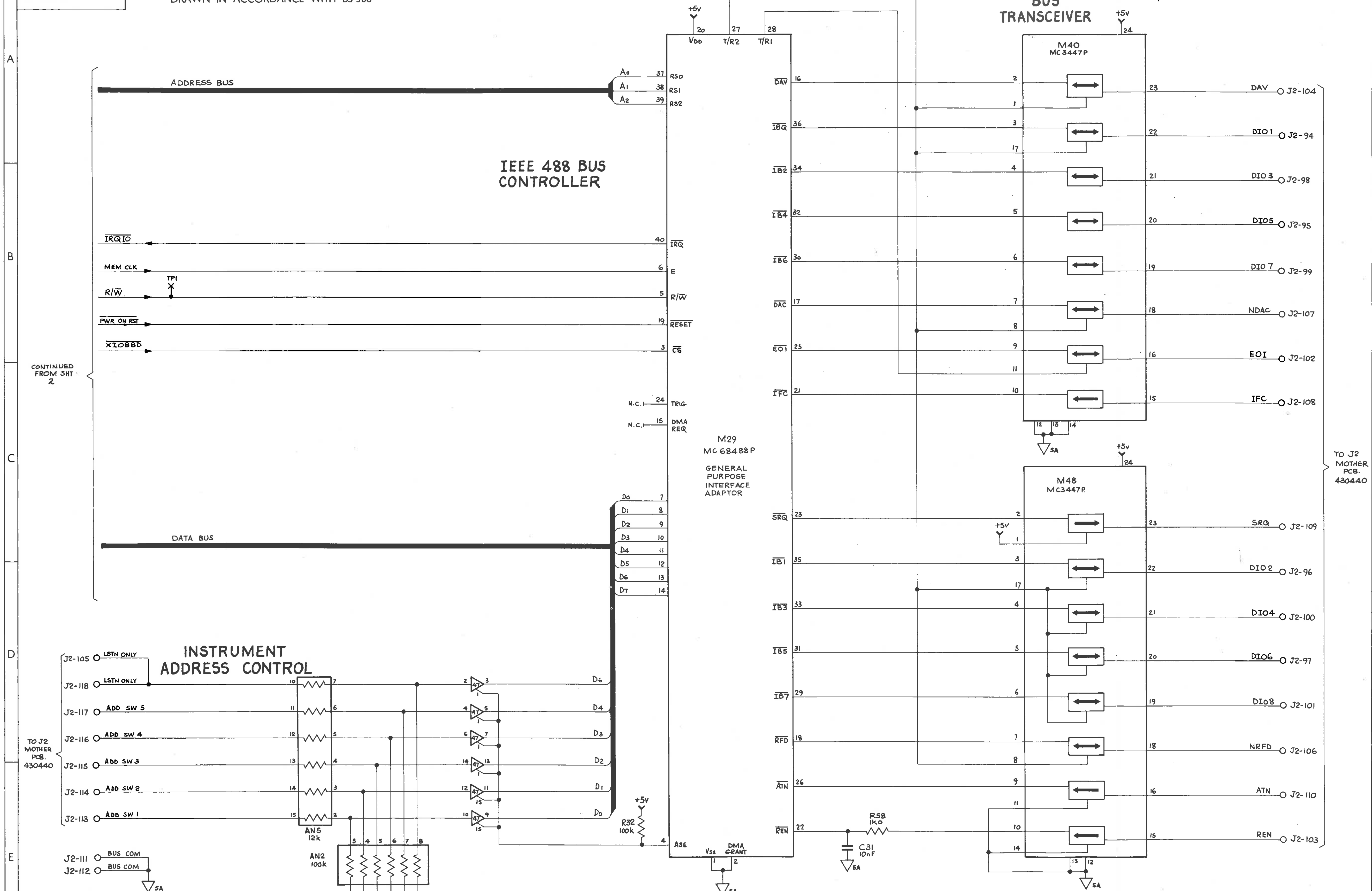
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

ISS.	CHANGES
1	RELEASED 13.5.82
2	SEE SHT 3



DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400442	TITLE
IL			DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°		CIRCUIT DIAGRAM		4000 DIGITAL PCB. I.E.E.E. 488 INTERFACE.
CHECKED	DATE 6.6.82	SCALE		FINISH	CHECK PROCEDURE	460442	
APPR.	DATE 17.5.82	NOT TO BE SCALED	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION		CHECK LIST	470442	

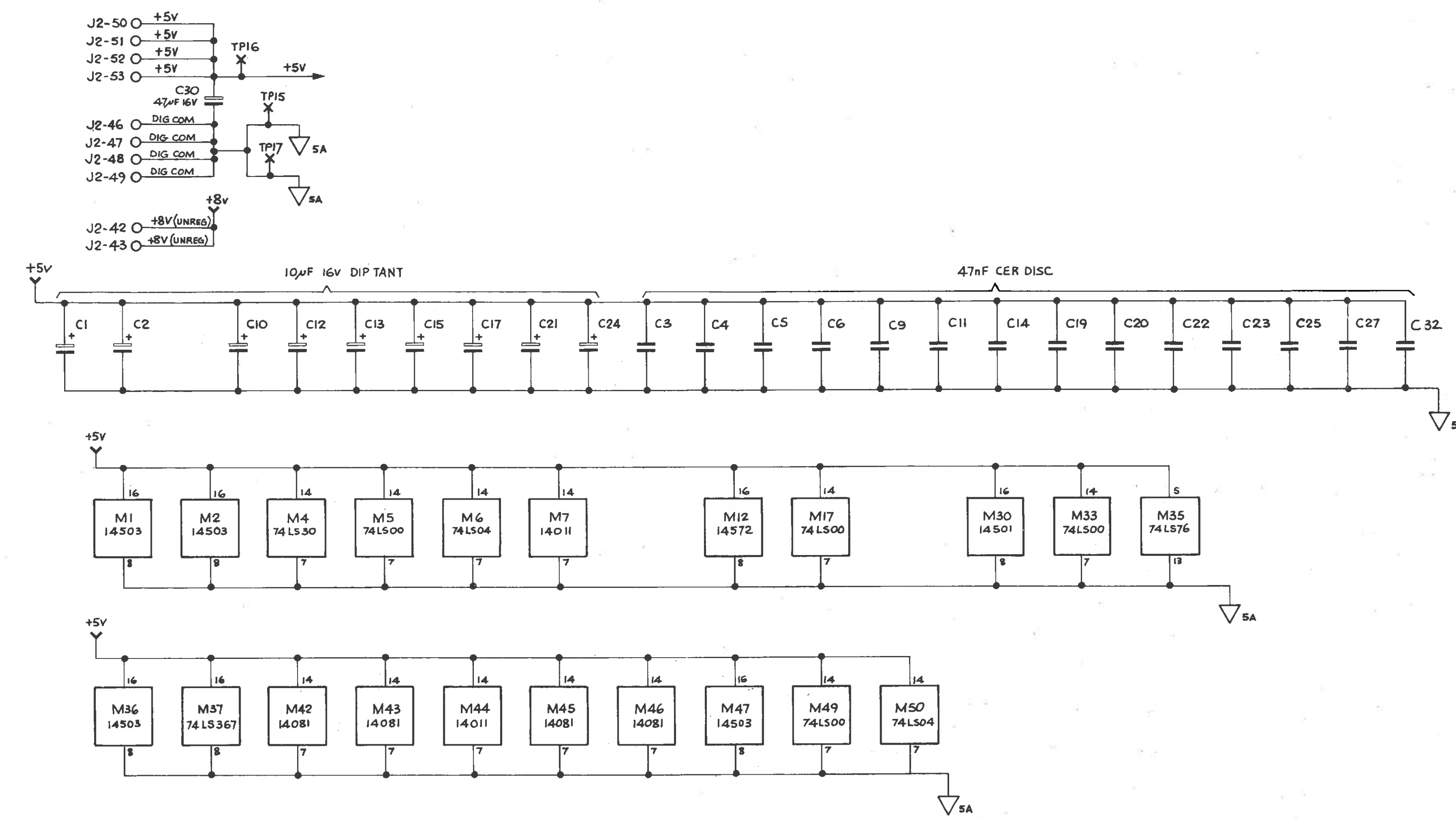
datron ELECTRONICS LIMITED NORWICH

DRAWING No. 430442

SHEET 4 OF 5

DRAWING No. 430442

ISS.	CHANGES
1	RELEASED 13.5.82
2	SEE SHT 3.

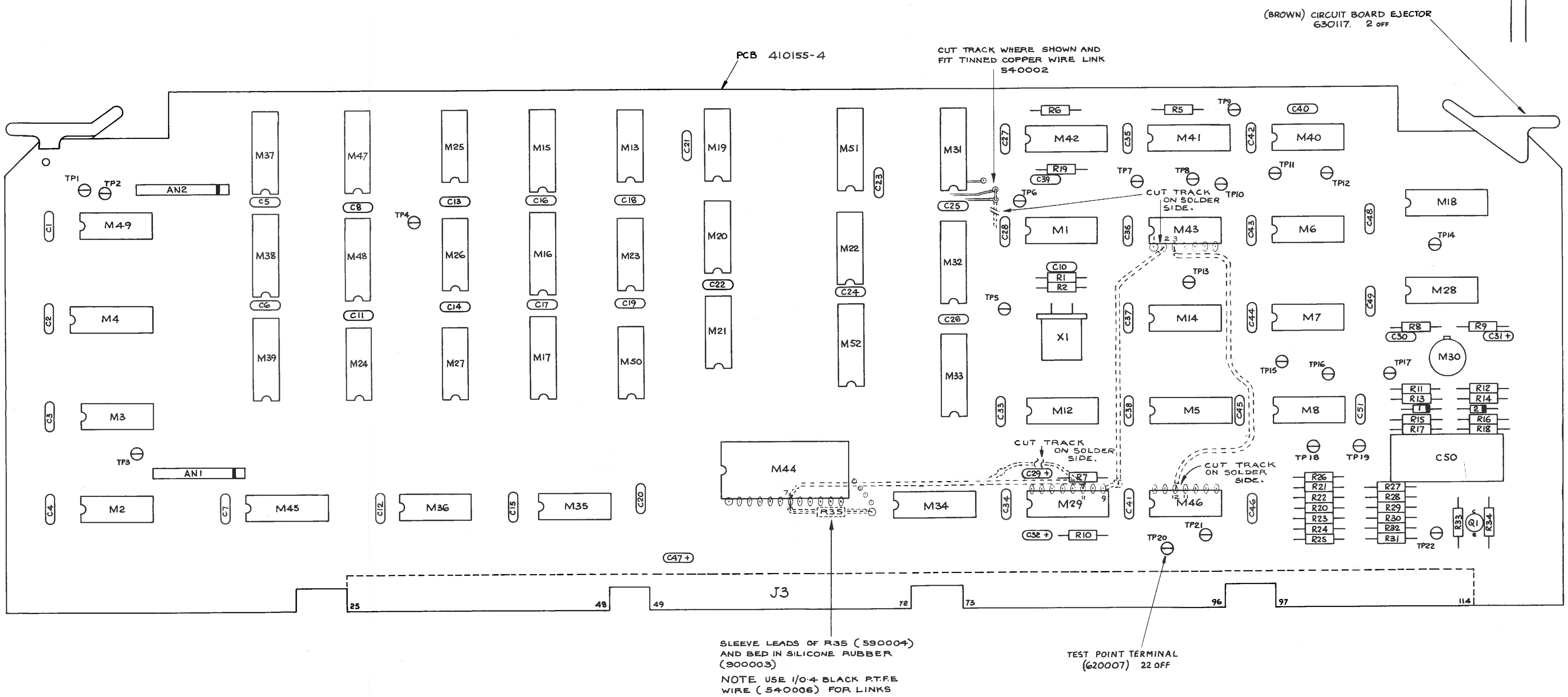


DRAWN	DATE 7.7.81	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400442	TITLE 4000 DIGITAL P.C.B. I.C. POWER SUPPLIES	DRAWING No. 430442
CHECKED	DATE 6.6.82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430442		
APPR.	DATE 17.5.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460442		
					CHECK LIST 470442		SHEET 5 OF 5

datron ELECTRONICS LIMITED NORWICH

DRAWING No. 400443

ISS.	CHANGES
D	
1	RELEASED 3.3.82.
2	ECO 1315, 1323 C29 WAS 100nF C47 WAS 10µF R35 ADDED. 3 TRACKS CUT 3 LINKS ADDED. JR 14.5.82
3	ECO 1435 1 TRACK CUT AND 1 LINK ADDED. JR 16 12 82

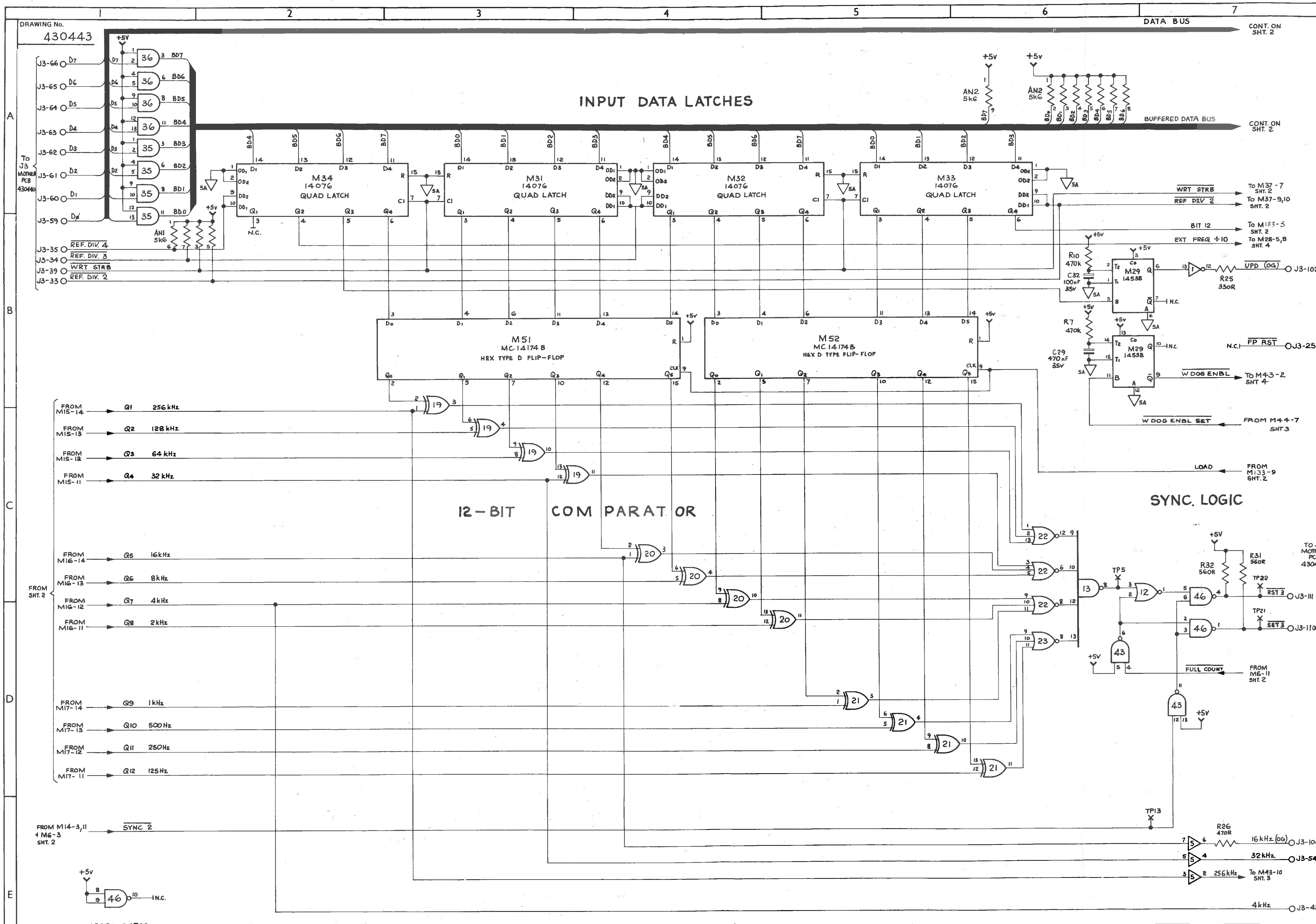


MOUNTING IC's.			
Nº WAYS	PART Nº	USED TO MOUNT	Nº OFF
14	605060/A	1-3, 6-8, 12-14, 19-28, 35, 36, 40, 43, 46, 49 + 50	26
16	605061/A	4-5, 15-18, 29, 31-34, 37-39, 41, 42, 45, 47, 48, 51, 52	21
24	605064/A	44	1

M9 - M11 NOT USED.

datron ELECTRONICS LIMITED NORWICH

DRAWN	DATE 12.2.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400443	TITLE 4000. ANALOGUE INTERFACE PCB. ASSY.	DRAWING No. 400443
CHECKED	DATE 9.3.82	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430443		
APPR.	DATE	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460443		
					CHECK LIST 470443		SHEET 1 OF 9



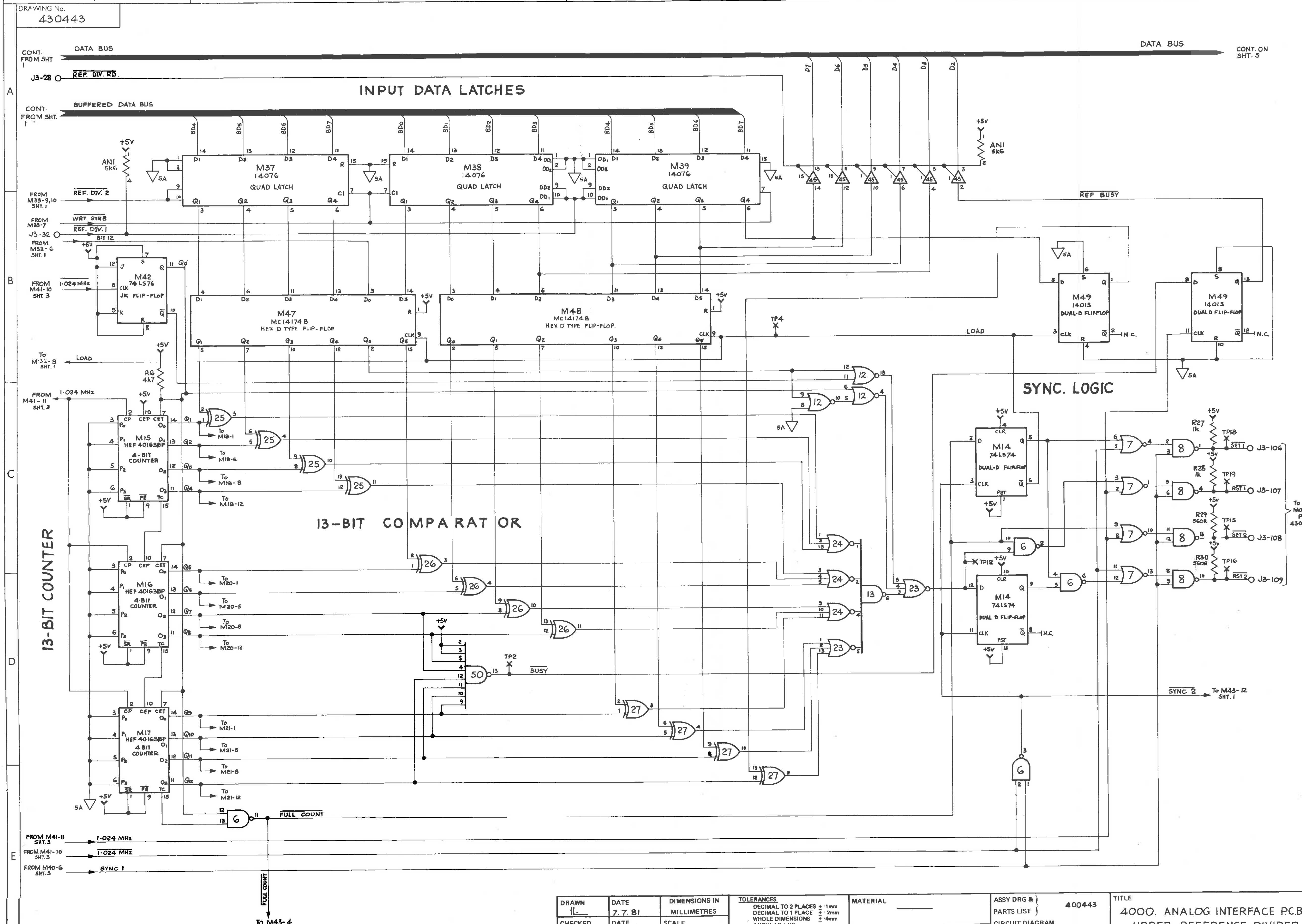
ISS.	CHANGES
1	RELEASED 3.3.82
2	ECO 1315.1323. M34-3 WENT TO M29-11. M29-9 WAS N.C. M43(1, 2, 3) HAD SPARE GATE. C29 WAS 100nF. JR 17·5·82
3	ECO 1435 SEE SHT 2. JR 16·12·82

datron ELECTRONICS LIMITED NORWICH

DRAWN IL	DATE 1.7.81	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR + ½° UNLESS OTHERWISE STATED	MATERIAL	ASSY DRG & PARTS LIST 400443	TITLE 4000. ANALOG INTERFACE P.C.B. LOWER REFERENCE DIVIDER COUNTER.
CHECKED A.K.B.	DATE 18/1/82	SCALE		FINISH	CIRCUIT DIAGRAM	DRAWING No. 430443
APPR.	DATE	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460443 CHECK LIST 470443	SHEET 1 OF 4

4951MT

DRAWING No. 430443



ISS.	CHANGES
1	RELEASED 3.3.82
2	ECO 1315, 1323. SEE SHEETS 1, 3 AND 4 JR 17.5.82
3	ECO 1435 M49 PIN 11 WENT TO M43 PIN 12. JR 16.12.82

DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400443
IL	7.7.81		DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°		CIRCUIT DIAGRAM	
CHECKED	DATE	SCALE		FINISH	CHECK PROCEDURE	460443
A.K.B	18/1/82				CHECK LIST	470443
APPR.	DATE	NOT TO BE SCALED	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION			

TITLE: 4000. ANALOG INTERFACE P.C.B. UPPER REFERENCE DIVIDER COUNTER.

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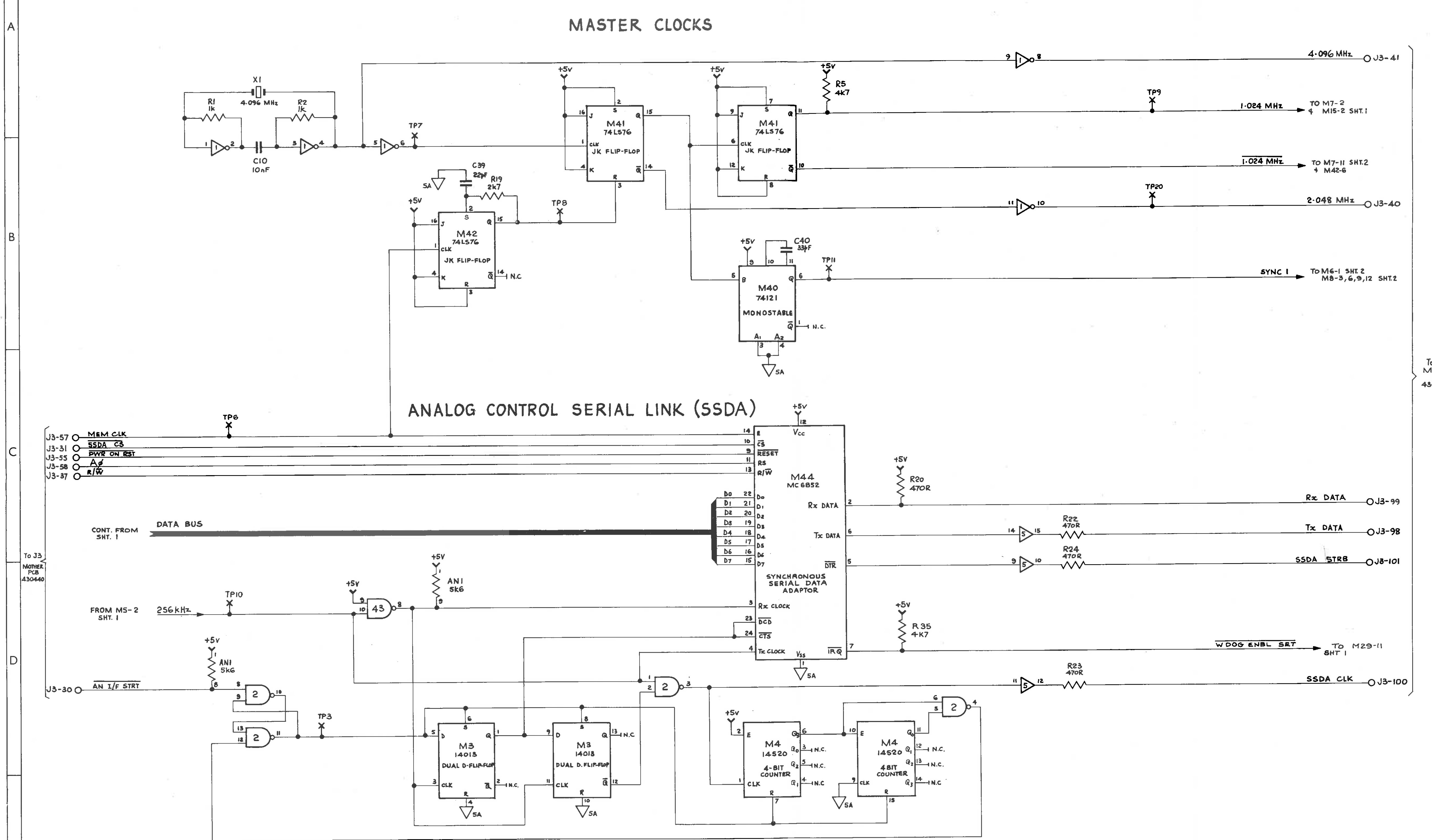
DRAWING No. 430443

SHEET 2 OF 4

DRAWING No. 430443

ISS.	CHANGES
1	RELEASED 3.3.82
2	ECO 1315, 1323. M44-7 WAS N.C. R35 ADDED. JR 17.5.82
3	ECO 1435 SEE SHT 2. JR 16.12.82



DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400443
IL	7.7.81	SCALE	DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	FINISH	CIRCUIT DIAGRAM	
CHECKED A.K.8	DATE 18/1/82		UNLESS OTHERWISE STATED		CHECK PROCEDURE	460443
APPR.	DATE	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST	470443

TITLE: 4000 ANALOG INTERFACE P.C.B. MASTER CLOCKS & ANALOG CONTROL SERIAL LINK.

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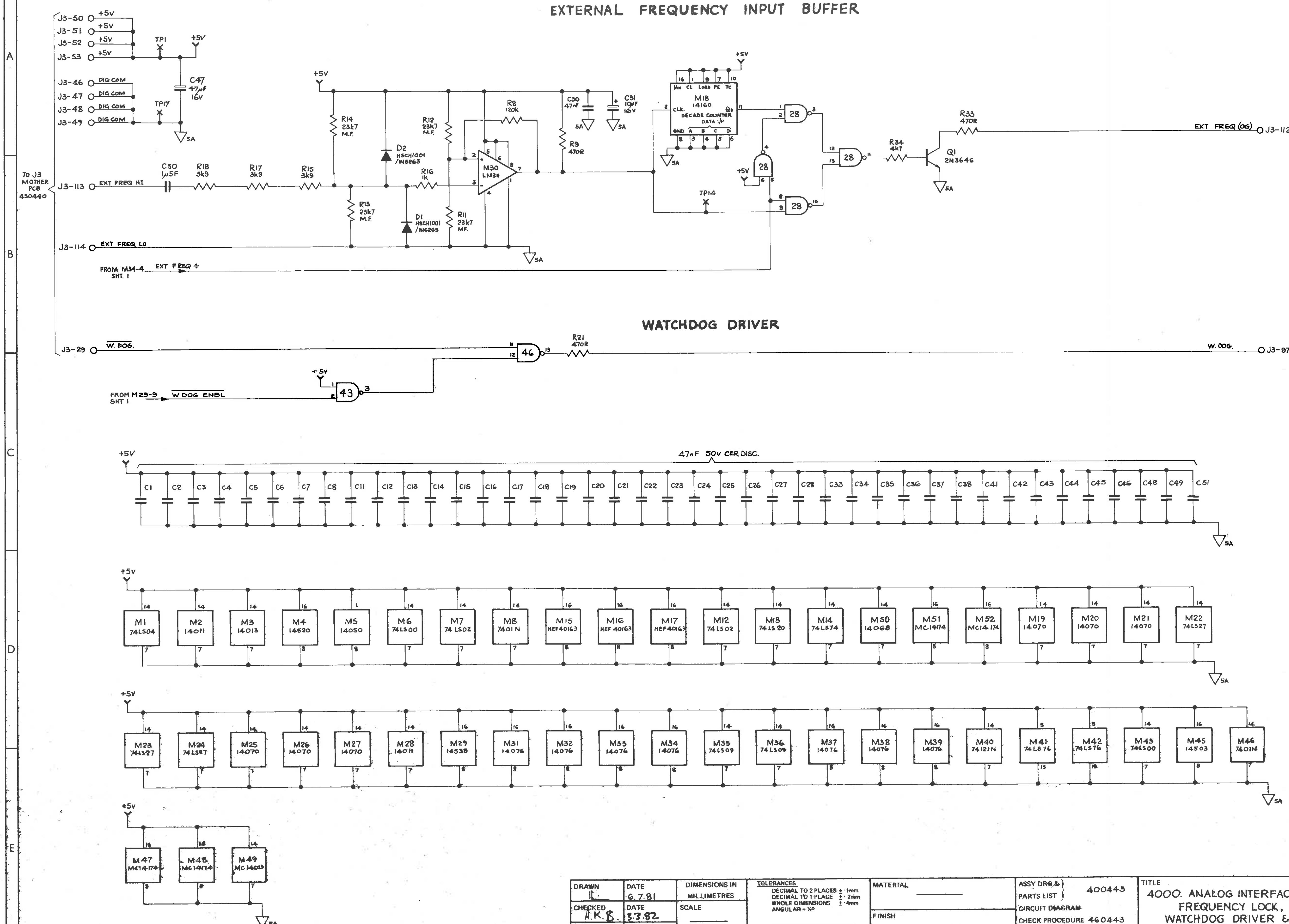
DRAWING No. 430443

SHEET 3 OF 4

DRAWING No. 430443



ISS.	CHANGES
1	RELEASED 3.3.82
2	ECO 1315.1323 M46-12 WAS CONNECTED TO M46-11 C47 WAS 10µF JR 17.5.82
3	ECO 1435 SEE SHT 2 JR 16.12.82

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DRAWN	DATE 6.7.81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°
CHECKED A.K.B.	DATE 3.3.82	SCALE	UNLESS OTHERWISE STATED
APPR.	DATE	NOT TO BE SCALED	FIRST ANGLE PROJECTION

MATERIAL
FINISH

ASSY DRG & PARTS LIST 400443
CIRCUIT DIAGRAM
CHECK PROCEDURE 460443
CHECK LIST 470443

TITLE: 4000 ANALOG INTERFACE P.C.B. FREQUENCY LOCK, WATCHDOG DRIVER & I.C. POWER SUPPLIES.

DRAWING No. 430443

SHEET 4 OF 4

DRAWING No. 400444 / 400444A

ISS.	CHANGES
1	RELEASED 7.5.82
2	ECO 1354 M32 AND M35 WERE FITTED IN SOCKETS. R33 NOW IN F.S.V. Q48 AND Q49 NOW DRAWN CORRECTLY. JR 1.7.82
3	ECO. 1380.1383 R18 WAS 866R R23 WAS 3K83 R29. R33. R48 & R53 WERE 110R. IL 24.8.82
4	ECO 1439. C65 & R124 ADDED. BJ. 11-FEB 83
5	ECO 1501 & 1502 R125 WAS Q38. R126 " Q39. D19 " R82 D20 " R83 R85 WAS 18K2 Q33 & Q36 WERE 239040-1 CONT. BELOW
5	ECO. 1511 R88 R89 + LKF DELETED. TRACK UNDER M24 CUT. WIRE LINKS FROM M13 + M24 ADDED. IL 14.7.83

LINK TO M24 PIN 10 USING 7/2 PTFE INSUL. WIRE 540008.

CUT TRACK ON COMPONENT SIDE OF PCB.

LINK ACROSS PADS ON UNDERSIDE OF PCB USING 22 SWG BTC WIRE 540002.

SOLDER WIRE LINK BETWEEN REF PLUG-IN PCB AND REF DIVIDER PCB IN POSITION SHOWN. (540002)

TO SECURE Q50 TO BOARD USE M3 x 8mm POZI-PAN SCREW 611016 M3 NUT 615002 M3 SHAKEPROOF 613005

PCB 410157-5

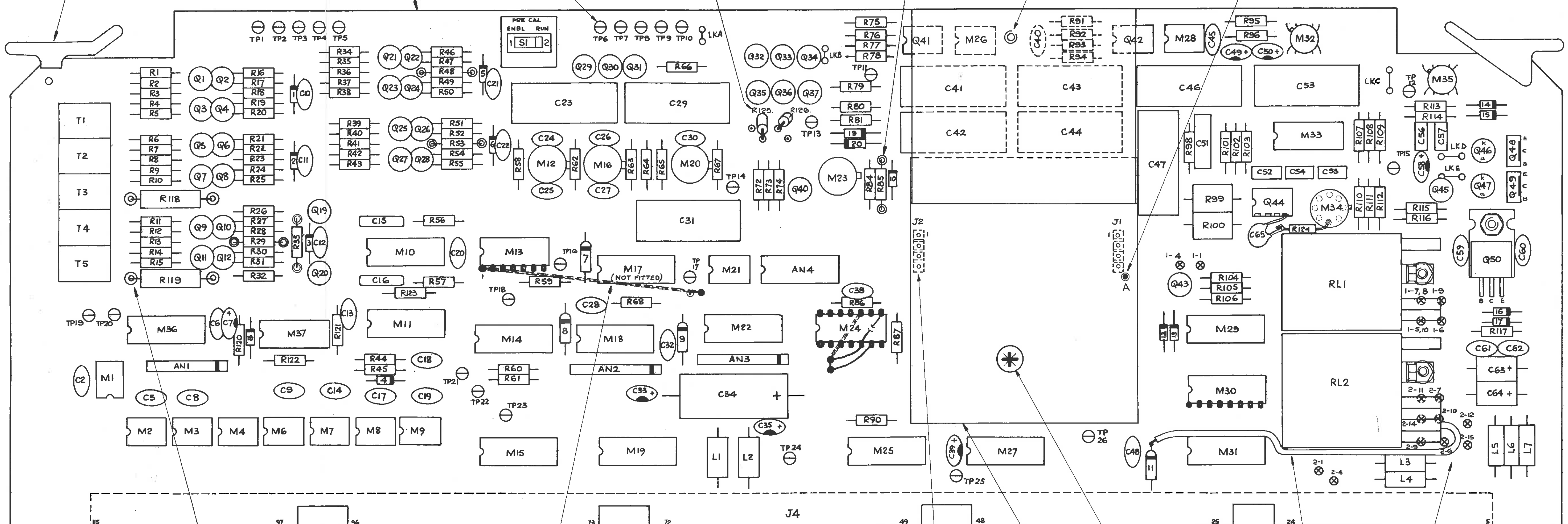
(RED) CIRCUIT BOARD EJECTOR 2 OFF 630118

TEST POINT TERMINAL 620007 26 OFF.

R125 & R126 MUST BE MOUNTED AS SHOWN.

FSV TERMINAL 602001 10 OFF (R29, R48, R53, R33. AND R85)

FIT M3X8 POZI-PAN SCREW 611016 + M3 CRINKLE WASHER 613029 FROM UNDERSIDE OF MAIN PCB.



MOUNT R118 AND R119 ON CERAMIC INSULATING BEAD (1 PER LEAD) 630024 4 OFF

3-48 UNC NUT 615005 2 OFF M2.5 WASHER 613014 2 OFF

LINK M13 PIN 1 AND PAD SHOWN USE 7/2 PTFE INSUL. WIRE 540008.

4 WAY .1" PCB PLUG 604053 2 OFF SOLDERED INTO MAIN PCB. N.B. SOCKETS ON REF PCB ASSY TO PLUG BOARD ONTO PINS, NOT SHOWN.

REFERENCE PCB ASSY 400452 (4000) 400452A (4000A)

M3 x 4mm SWAGED STANDOFF 612004 SECURED TO REV. DIV. PCB ON COMP. SIDE M3 X 8 POZI-PAN SCREW 611016 M3 CRINKLE WASHER 613029.

SOLDER TERMINAL 16 OFF 620003

WIRE LEAD 7/2 PTFE INSULATED WIRE 540008 120mm LONG TO CONNECT RL2-8 TO D11 CATHODE

MOUNTING I.C.s.

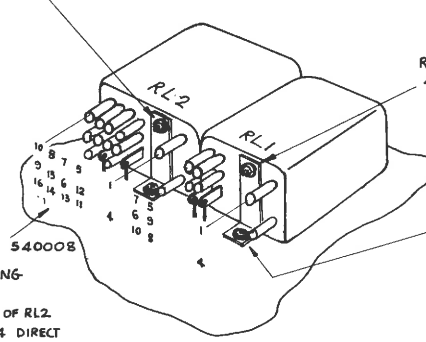
FIT M1-M4, M6-M9, M21, M26, M28, Q41, Q42, Q44 ON 8 WAY D.I.L. SOCKET 605059 14 OFF

FIT M13, M24, M33, M37 ON 14 WAY DIL SOCKET 605060 4 OFF

FIT M10, M11, M14, M15, , M18, M19, M22, M25, M27 M29, M30, M31, M36 ON 16 WAY DIL SOCKET 605061 13 OFF

RELAY BRACKET 459112 2 OFF.

M3X8 POZI-PAN SCREW 611016 2 OFF M3 NUT 615002 2 OFF M3 SHAKEPROOF 613005 2 OFF



1. USE 7/.2 PTFE INSULATED (WHITE) WIRE 540008 TO MAKE CONNECTIONS TO RELAYS/ SOLDER PINS AND SLEEVE JOINTS USING 1/2 X PART No 590001 15 OFF
2. SLEEVE UNCONNECTED PINS 13 & 16 OF RL2.
3. CONNECT RL1-8, 10 AND RL2-11, 14 DIRECT TO SOLDER PINS (DO NOT SLEEVE)

VIEW TO RELAY PIN LAYOUTS

RELAY WIRING

FROM	TO	LENGTH (mm)
RL1-1	PIN 1-1	100
-4	" 1-4	100
-5	" 1-5,10	30
-6	" 1-6	25
-7	" 1-7,8	30
-9	" 1-9	25
RL2-1	PIN 2-1	90
-4	" 2-4	80
-5	RL2-8	30
-6	PIN 2-2,6	25
-7	" 2-7	30
-9	" 2-2,9	25
-10	" 2-10	30
-12	" 2-12	25
-15	" 2-15	25

N.B. M30 PIN 5 MUST BE CLIPPED OFF BEFORE SOLDERING DEVICE INTO SOCKET.

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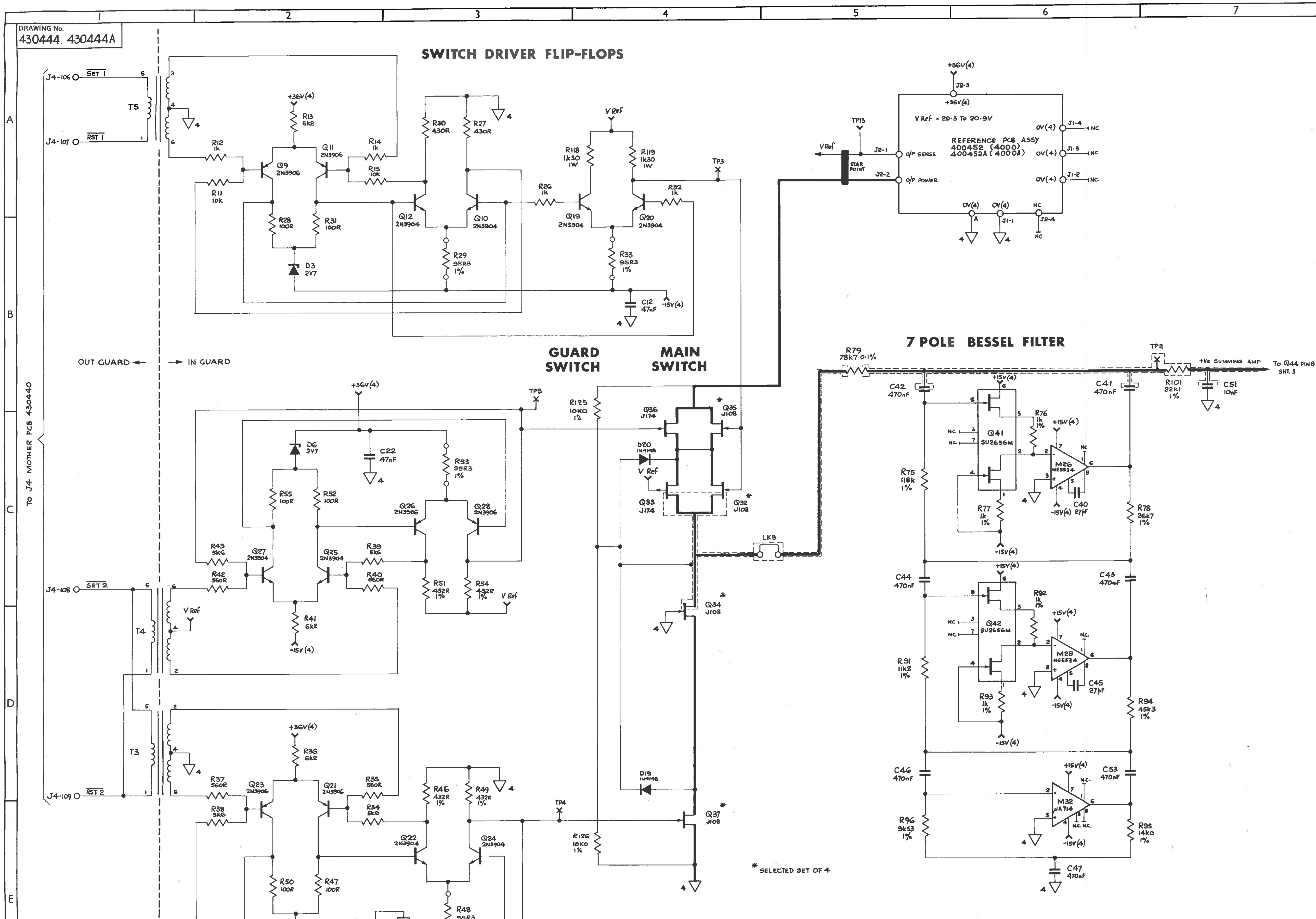
DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400444(A)	TITLE
IL	18.9.81	SCALE 2:1	DECIMAL TO 2 PLACES ± .1mm; DECIMAL TO 1 PLACE ± .2mm; WHOLE DIMENSIONS ± .4mm; ANGULAR + 1/2°	FINISH	CIRCUIT DIAGRAM	430444(A)	4000 / 4000A REFERENCE DIVIDER PCB. ASSY.
CHECKED MS	DATE 13.5.82.	NOT TO BE SCALED	UNLESS OTHERWISE STATED THIRD ANGLE PROJECTION		CHECK PROCEDURE	460444(A)	
APPR. B Hare	DATE 19-5-82				CHECK LIST	470444(A)	

DRAWING No. 400444 400444A

SHEET 1 OF 17



ISS.	CHANGES
1	RELEASED 7.5.82
2	ECO 1354 R 29, 33, 48, 53 NOW FITTED IN F.S.V.S JR 1·7·82
3	ECO. 1383 R29, R33, R48 & R53 WERE 110R 24.8.82
4	SEE SHEET 3
5	ECO 1501, 1502 R82 & R83 NOW D19 & D20. R125 WAS Q38. R126 " Q39. BJ. 4-7-83.
6	ECO. 1511 DETAILS INDICATED ON SHTS 4 & 5. 14.7.83

DRAWING No. 430444. 430444A

DRAWN	DATE 20.4.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400444/A	TITLE 4000/4000A REFERENCE DIVIDER PCB. MOST SIGNIFICANT SWITCH & FILTER
CHECKED R.K. COEGAN	DATE 18/5/82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM	
APPR.	DATE 21·5·82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460444/A; CHECK LIST 470444/A	

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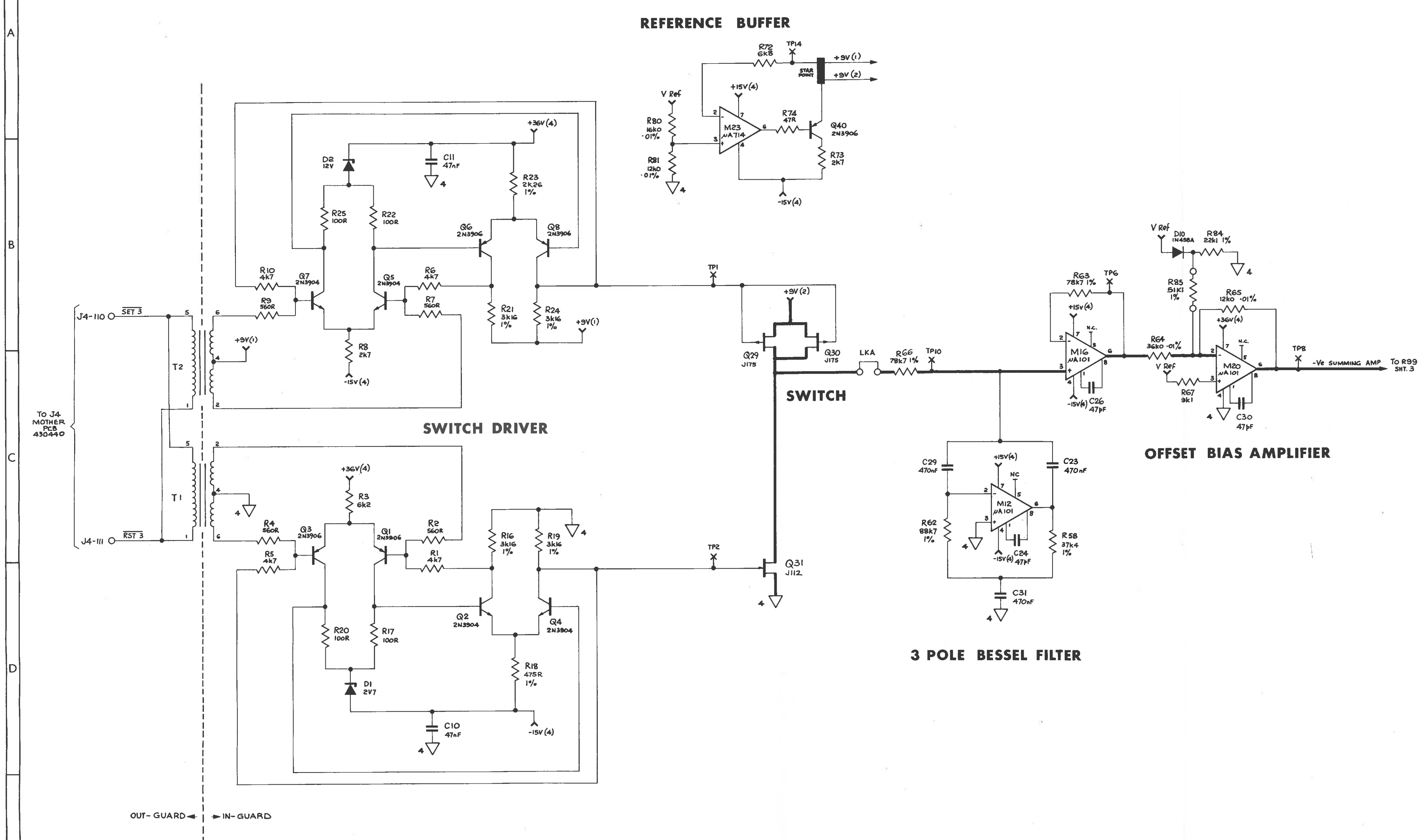
DRAWING No. 430444 430444A

SHEET 1 OF 6

DRAWING No. 430444. 430444A

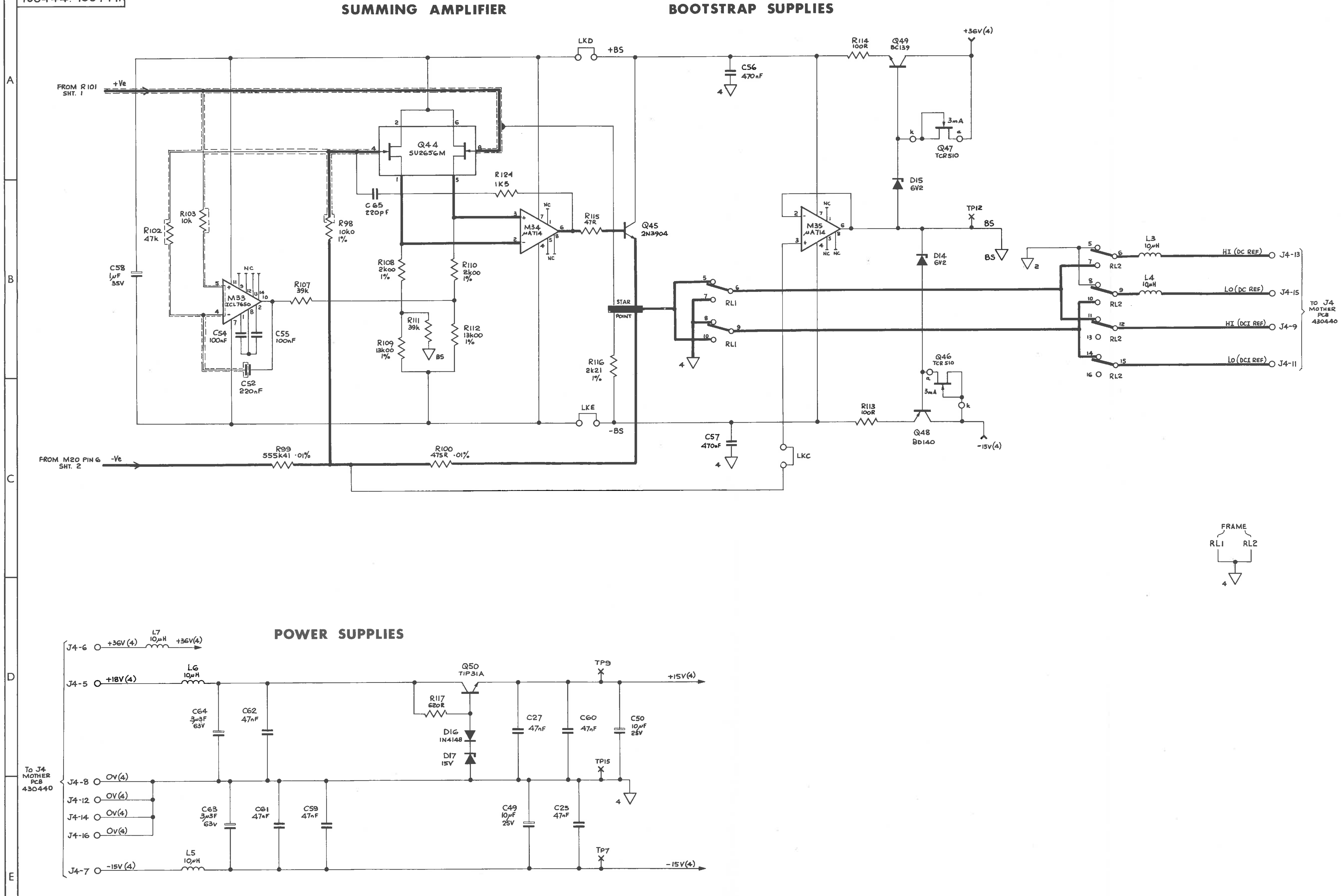
ISS.	CHANGES
1	RELEASED 7.5.82
2	SEE SHT 1
3	ECO. 1383. 1380 R18 WAS 866R R23 WAS 3K83 R85 WAS 22k1 IL 24.8.82
4	SEE SHEET 3
5	R85 WAS 18K2. ECO 1501 & 1502 4.7.83. BJ
6	SEE SHTS 4 + 5



DRAWN IL	DATE 20. 4. 82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400444(A)	TITLE 4000/4000A REFERENCE DIVIDER PCB LEAST SIGNIFICANT SWITCH AND FILTER	DRAWING No. 430444 430444A
CHECKED A.K.COGGAN	DATE 18/5/82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM		
APPR.	DATE 21. 5. 82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460444(A) CHECK LIST 470444(A)		SHEET 2 OF 6

datron ELECTRONICS LIMITED NORWICH

DRAWING No. 430444. 430444A



ISS.	CHANGES
1	RELEASED 7.5.82.
2	SEE SHT 1
3	SEE SHTS 1 AND 2
4	ECO 1439. 11-2-83 R124 & C65 ADDED.
5	SEE SHTS 1 & 2
6	SEE SHTS 4 + 5

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DRAWN	DATE 20.4.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°
CHECKED R.K. COGGAN	DATE 18/5/82	SCALE —	UNLESS OTHERWISE STATED
APPR.	DATE 21.5.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION

MATERIAL —

FINISH —

ASSY DRG & PARTS LIST	400444(A)
CIRCUIT DIAGRAM	
CHECK PROCEDURE	460444(A)
CHECK LIST	470444(A)

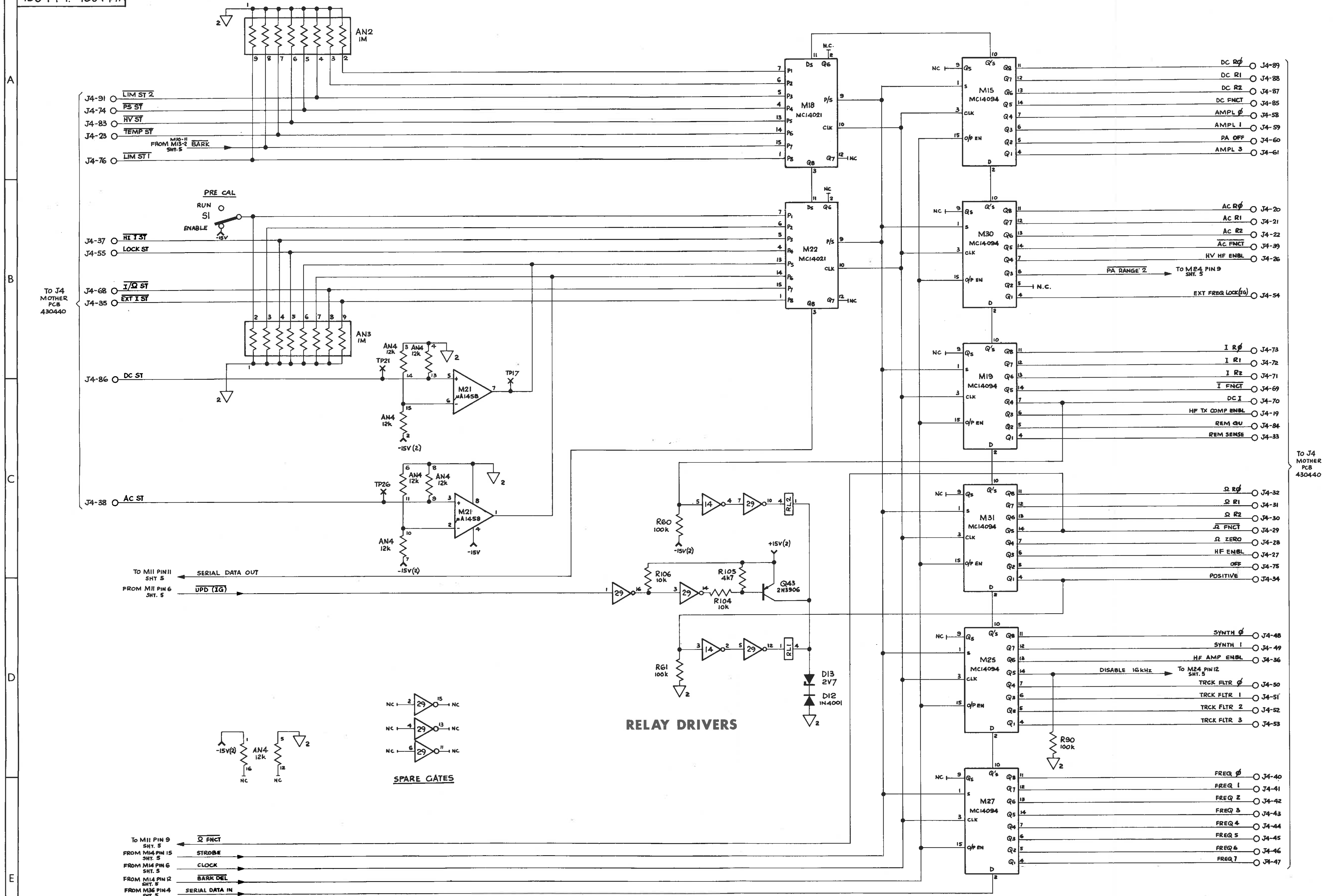
TITLE: 4000/4000A REFERENCE DIVIDER PCB. SUMMING AMPLIFIER AND COMMON 4 SUPPLIES.

DRAWING No. 430444 430444A

SHEET 3 OF 6

DRAWING No. 430444. 430444A

ISS.	CHANGES
1	RELEASED 7.5.82
2	SEE SHT 1
3	SEE SHTS 1 AND 2
4	SEE SHT 3
5	SEE SHEETS 1 & 2
6	LINE FROM M30-5 NOT USED



DRAWN	DATE 22.4.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL
CHECKED R.K. COGGAN	DATE 18/5/82	SCALE	UNLESS OTHERWISE STATED	FINISH
APPR.	DATE 21.5.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION	

ASSY DRG & PARTS LIST	400444(A)
CIRCUIT DIAGRAM	
CHECK PROCEDURE	460444(A)
CHECK LIST	470444(A)

TITLE 4000/4000A REFERENCE DIVIDER PCB SERIAL/PARALLEL DATA CONVERTER

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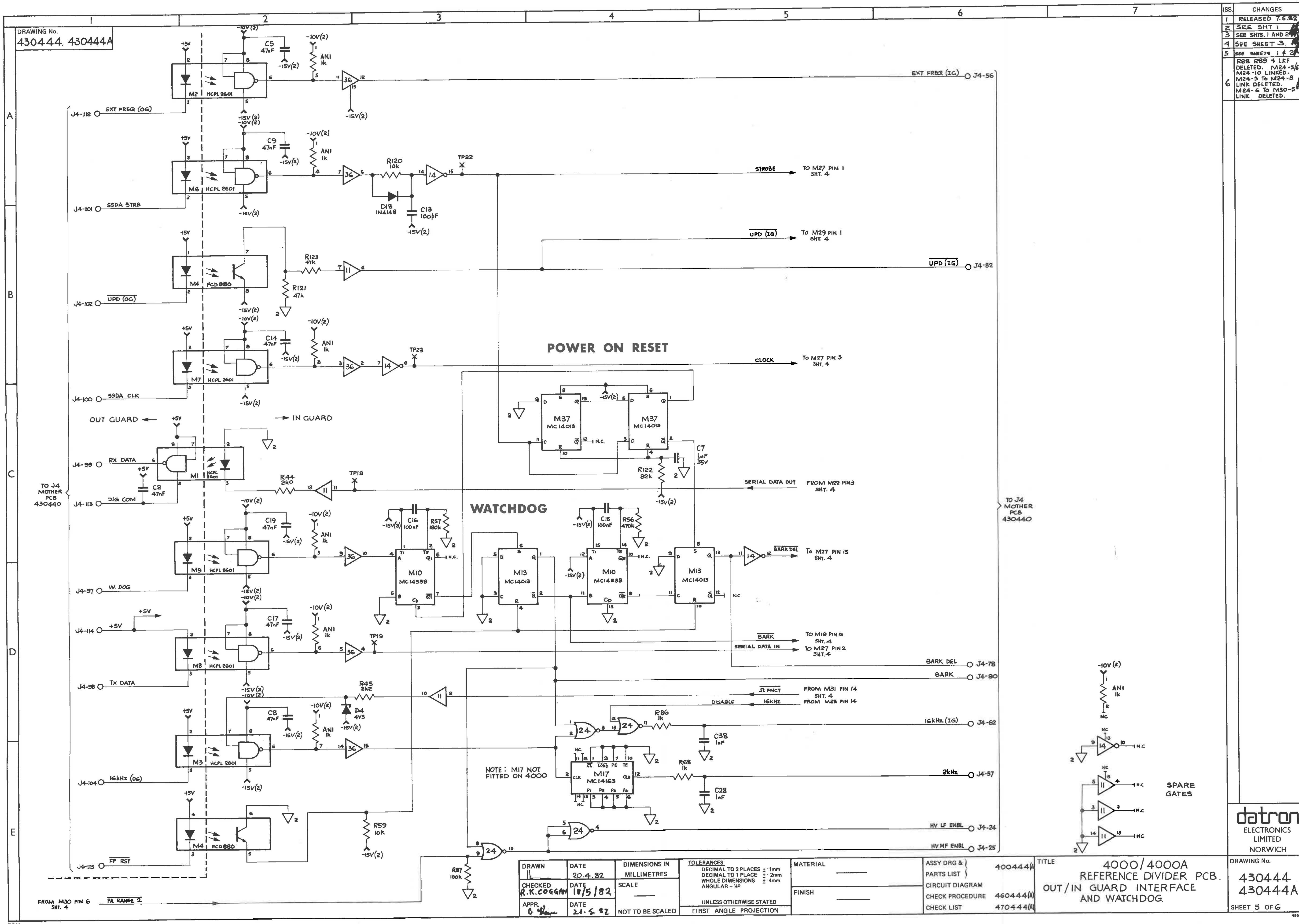
DRAWING No. 430444 430444A

SHEET 4 OF 6



DRAWING No. 430444. 430444A
POWER ON RESET
WATCHDOG
OUT GUARD
IN GUARD
TO J4 MOTHER PCB 430440
EXT FREQ (OG)
EXT FREQ (IG)
SSDA STRB
STROBE
TO M27 PIN 1 SHT. 4
UPD (OG)
UPD (IG)
TO M29 PIN 1 SHT. 4
SSDA CLK
CLOCK
TO M27 PIN 3 SHT. 4
RX DATA
DIG COM
SERIAL DATA OUT
FROM M22 PIN 3 SHT. 4
W. DOG
BARK DEL
TO M27 PIN 15 SHT. 4
TX DATA
BARK
TO M18 PIN 15 SHT. 4
SERIAL DATA IN
TO M27 PIN 2 SHT. 4
16kHz (OG)
16kHz (IG)
FROM M31 PIN 14 SHT. 4
DISABLE
FROM M25 PIN 14
2kHz
FP RST
HV LF ENBL
HV MF ENBL
FROM M30 PIN 6 SHT. 4
PA RANGE 2
NOTE: M17 NOT FITTED ON 4000
SPARE GATES
CHANGES
1 RELEASED 7.5.82
2 SEE SHT 1
3 SEE SHTS. 1 AND 2
4 SEE SHEET 3.
5 SEE SHEETS 1 & 2
6 R88 R89 & LKF DELETED. M24-5/6 M24-10 LINKED. M24-5 To M24-8 LINK DELETED. M24-6 To M30-5 LINK DELETED.
DRAWN 20.4.82
CHECKED R.K.COGGAN 18/5/82
APPR. 21.5.82
DIMENSIONS IN MILLIMETRES
NOT TO BE SCALED
TOLERANCES DECIMAL TO 2 PLACES ±·1mm DECIMAL TO 1 PLACE ±·2mm WHOLE DIMENSIONS ±·4mm ANGULAR ± ½°
UNLESS OTHERWISE STATED
FIRST ANGLE PROJECTION
ASSY DRG & PARTS LIST 400444(A)
CHECK PROCEDURE 460444(A)
CHECK LIST 470444(A)
TITLE 4000/4000A REFERENCE DIVIDER PCB. OUT/IN GUARD INTERFACE AND WATCHDOG.
datron ELECTRONICS LIMITED NORWICH
DRAWING No. 430444 430444A
SHEET 5 OF 6

DRAWING No.
430444. 430444A
FIRST USED ON

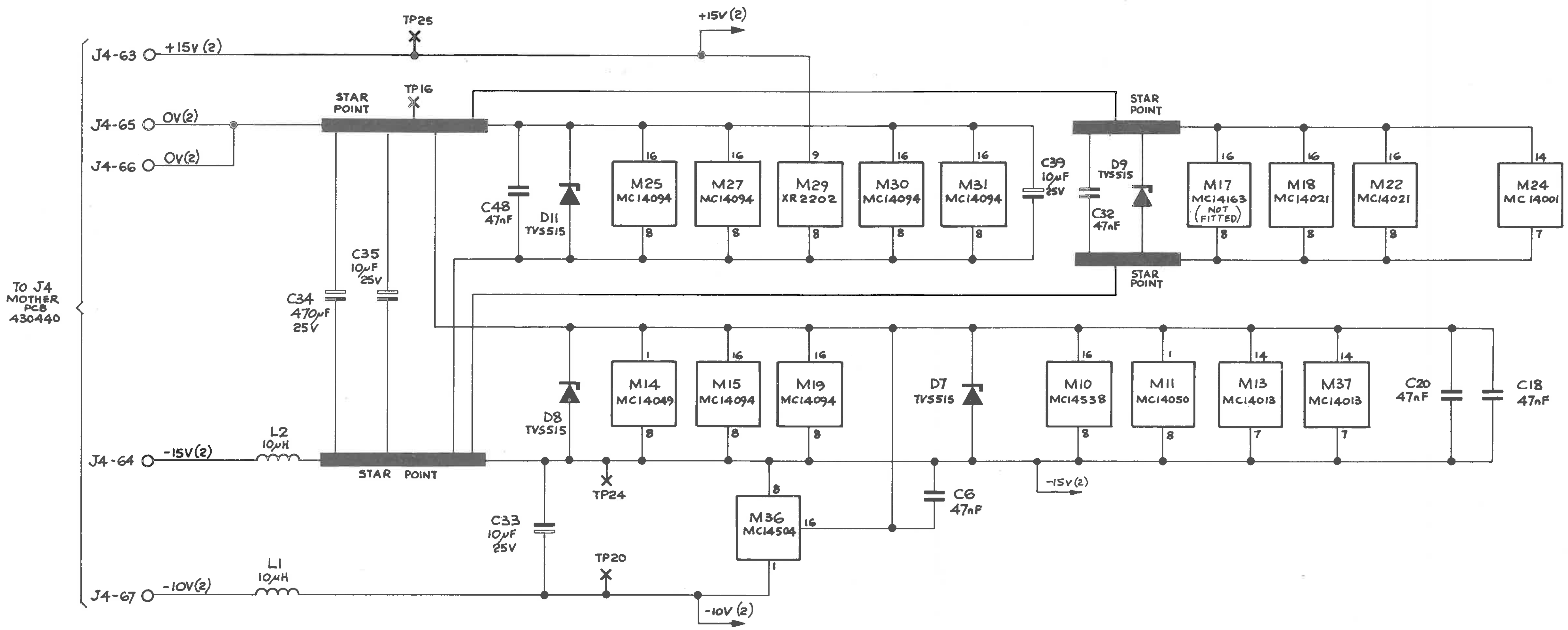
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

ISS.	CHANGES
1	RELEASED 7.5.82
2	SEE SHT 1
3	SEE SHTS 1 AND 2
4	SEE SHT 3.
5	SEE SHTS. 2 & 1
6	SEE SHTS 4 + 5



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DRAWN	DATE 29. 4. 82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400444(A)	TITLE 4000/4000A REFERENCE DIVIDER PCB COMMON 2 POWER SUPPLIES	DRAWING No. 430444 430444A
CHECKED R.K. COGGAN	DATE 18/5/82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM		
APPR.	DATE 21.5.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460444(A)		
					CHECK LIST 470444(A)		SHEET 6 OF 6

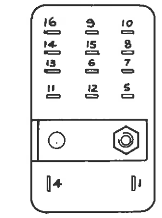
4951MT

DRAWING No. 400445 / 400445A

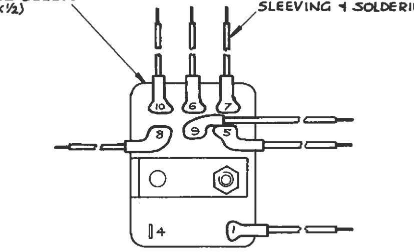
RELAY WIRING SCHEDULE											
RELAY	PINS LINKED ON RELAY (540002)	WIRE LINKS TO PCB (540002)	WIRE LEAD CONNECTIONS TO PCB (540008) 25mm	35mm	50mm	70mm	90mm	120mm	270mm	40mm	130mm
RL1	6-9	4,10	1			7					
RL2	6-9	4,10	1		7						
RL3	9-15 ; 6-12	4,13,16	1						7, 10		
RL4		4,10	1,5,6,9								
RL5		4,8,10	1,5,6,7,9								
RL6	6-9	4,10	1,7								
RL7	9-15 ; 6-12	4,13,16	1,7,10								
RL8		4,13,14,16	1,6, 8,10,12,15					7,9			
RL9		4,13	1,8,9,12			*14	15,16				
RL10	6-9	4	1,5,8,(6+9)								
RL11		4	1,8			*9	10				
RL12	6-9	4,8	5,(6+9)		1						
RL13	9-15 ; 6-12	4	1,16	7	10					13	
RL14	9-15 ; 6-12	4	10	7		13,16	1				
RL15		4	1,9								8

* N.B. IN ADDITION TO THE ABOVE A WIRE CONNECTION MUST ALSO BE MADE BETWEEN RL9-14 + RL11-9 70mm LONG.

MOUNTING IC's			
Nº WAYS	PART Nº	Nº OFF	USED TO MOUNT
8	605059	7	M9, M10, M11, M12, M14. Q6 + Q11
14	605060	6	M3, M5, M6, M8, M16, M20.
16	605061	4	M1, M2, M4, M7



4 POLE RELAY 330019 PIN LAYOUT



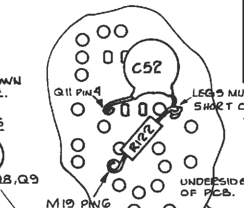
2 POLE RELAY 330018 PIN LAYOUT.

SLEEVE ALL WIRE BEFORE SOLDERING CONNECTIONS (INCL. SOLDER PIN CONNS ON PCB) USING SLEEVE 590001 (x½)

ALL RELAY LEADS MADE FROM 7/0·2 PTFE INSULATED (WHITE) WIRE ; CUT + STRIP EACH END 5mm BEFORE SLEEVING + SOLDERING.

ISS.	CHANGES
1	RELEASED 25.6.82
2	ECO 1376,1385 P.C.B WAS ISS4 R28, R91, R49, R50 R67 R68 R90 DELETED. R29 WAS 10M R22 WAS 1M50 F6 WAS 62mA Q7 WAS BD140 Q10 WAS BD139 R119 + R120 ADDED 2 CERAMIC BEADS ADDED, 1 HARWIN PIN DELETED. JR 25.8.82
3	ECO 1432 RESISTOR SETS 090057,58,59 WERE ISS 1 JR 15·12 82.
4	ECO 1440 & 1444 C49,50,51,52, R121 & R122 ADDED. BJ. 9-2-83.
5	ECO 1478. 1483 R69-R73 R76 R99 DELETED. PART Nº CHANGES To R10 R27 R48 R66 R89 R96 R74 + R75. Nº OF CERAMIC BEADS WAS (630024) 44. R88/R95 WAS 7M15 R98 WAS 1M62. TOTAL LENGTH OF PTFE WIRE REQD WAS 2475mm. No OF SOLDER PINS WAS 57. JL 6.6.83

NOTE : FIT TCR50G AS SHOWN ON DRG. FIT E50G AS SHOWN WITH FLAT ON THE CORNER.

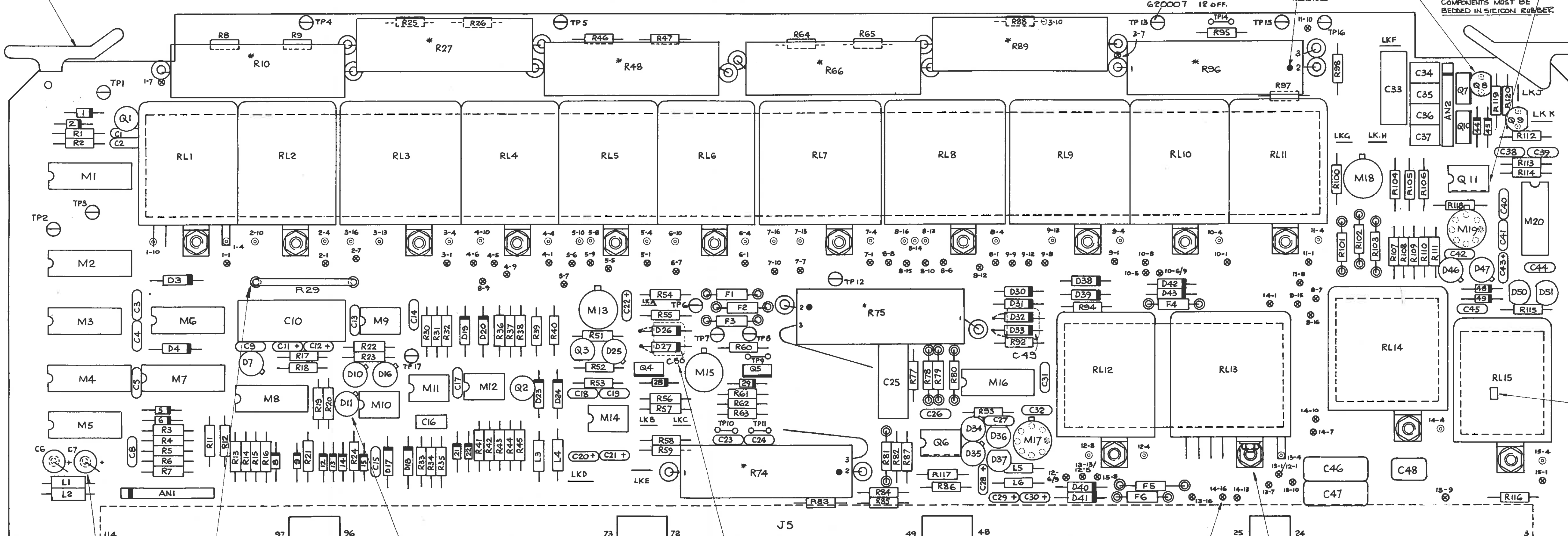


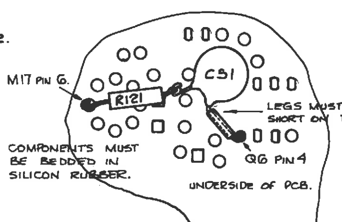
LINKS / TEST POINT LOOPS MADE FROM 22SWG BTC WIRE 540002

TEST POINT TERMINAL 620007 12 OFF.

ON R74 R75 + R96 PIN 2 INDICATED BY ● ON MANN RESISTORS

(ORANGE) CIRCUIT BOARD EJECTOR 2 OFF 630119





SLEEVE LEADS OF C6 + C7 USING SLEEVE 590001 2 OFF (CUT LENGTH TO APPROX 15mm) AND STAND COMPONENT ON A CERAMIC BEAD 630036 2 OFF

MOUNT R29 ON CERAMIC BEADS 2OFF 630036.

MOUNT D7 D10 D11 D16 + D25 ON MOUNTING PAD 618004 5 OFF.

PCB 410159-6

C49 & C50 MOUNTED ON UNDERSIDE OF PCB AND BEDDED IN SILICON RUBBER.

MOUNT F1-F6, R78-R81, R101-R103 ON CERAMIC BEADS 630036 (1 PER LEAD) 26 OFF

MOUNT R10, R27, R48, R66, R89, R96, R74, R75 ON CERAMIC BEAD 630024. (2 PER LEAD ON COMPONENTS MARKED THUS *) 34 OFF

SOLDER TERMINAL 56 OFF 620003

RELAY BRACKET 459112 15 OFF (RL1-RL15)
3-48 UNC NUT 615005 15 OFF
M2·5 WASHER 613014 15 OFF
M3x8 POZI-PAN SCREW 611016 15 OFF
M3 NUT 615002 15 OFF
M3 SHAKEPROOF 613005 15 OFF

N.B. BEFORE MOUNTING RL1-RL15 TO PCB USE STRIP OF POLYAMIDE TAPE (630132) TO ISOLATE RELAY 'SPIGOT' FROM PCB RL15 IS TYPICAL.

POSITION OF RELAY SPIGOT

DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400445 (A)	TITLE
JL	18.5.82		DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°				4000 / 4000A DC PCB ASSY.
CHECKED	DATE	SCALE		FINISH	CIRCUIT DIAGRAM	430445 (A)	
B. JACKSON.	25-6-82	2:1	UNLESS OTHERWISE STATED		CHECK PROCEDURE	460445 (A)	
APPR.	DATE	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST	470445 (A)	
[illegible]	2.7.82						

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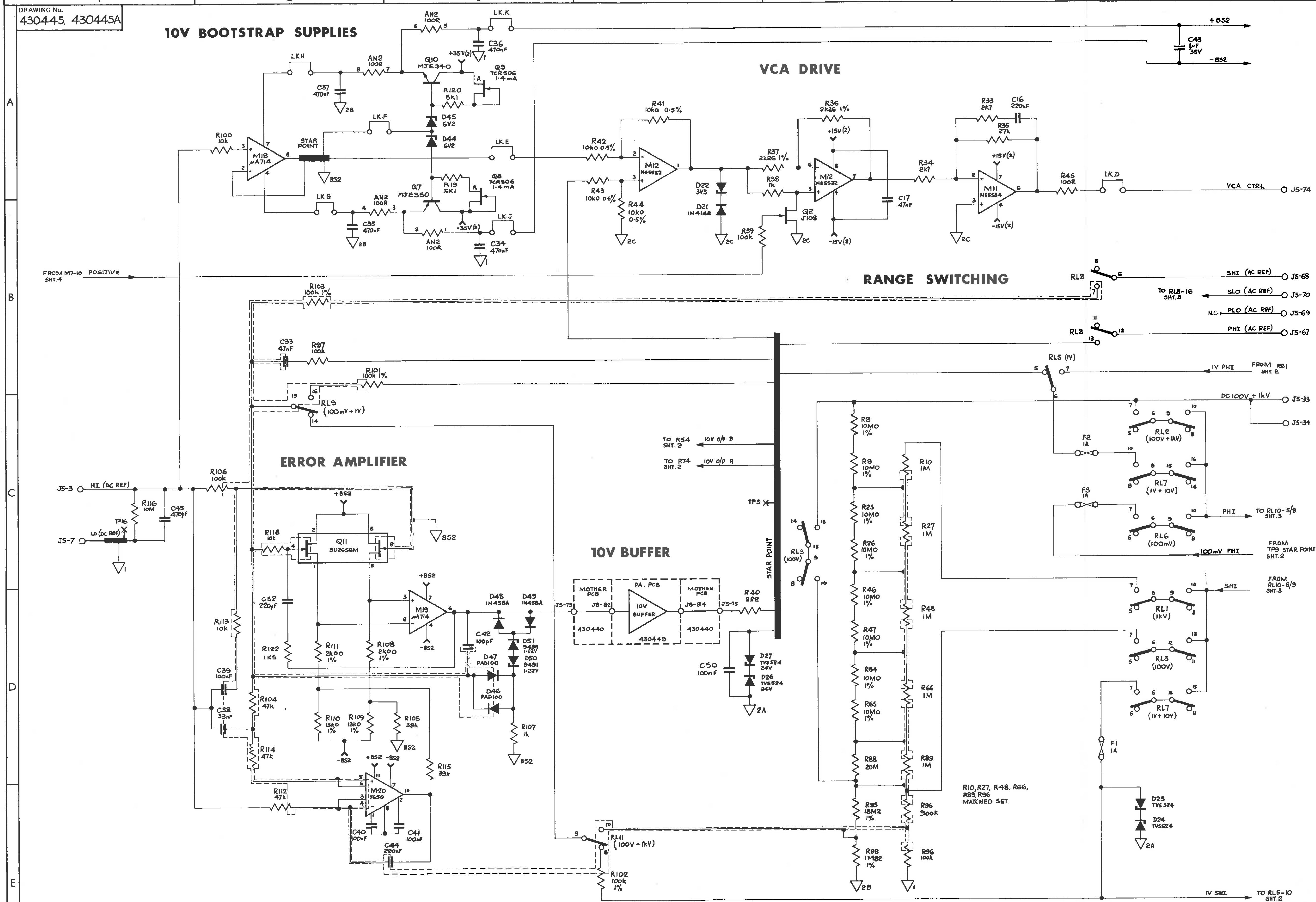
DRAWING No. 400445 / 400445A

SHEET 1 OF 16

DRAWING No. 430445, 430445A



ISS.	CHANGES
1	RELEASED 25.6.82.
2	ECO 1376, 1385 Q7 WAS BD140 Q10 WAS BD139 R119 AND R120 ADDED. JR 25·8·82
3	ECO 1440 & 1444 C50, C52 & R122 ADDED. BJ. 11-2-83.
4	ECO 1478, 1483 R10, R27, R48, R66, WERE 1M25. R89, R96 WERE 450k. R99 DELETED. R88 WAS 7M15 1% R95 WAS 7M15 1% R98 WAS 1M62 1% IL 6.6.83

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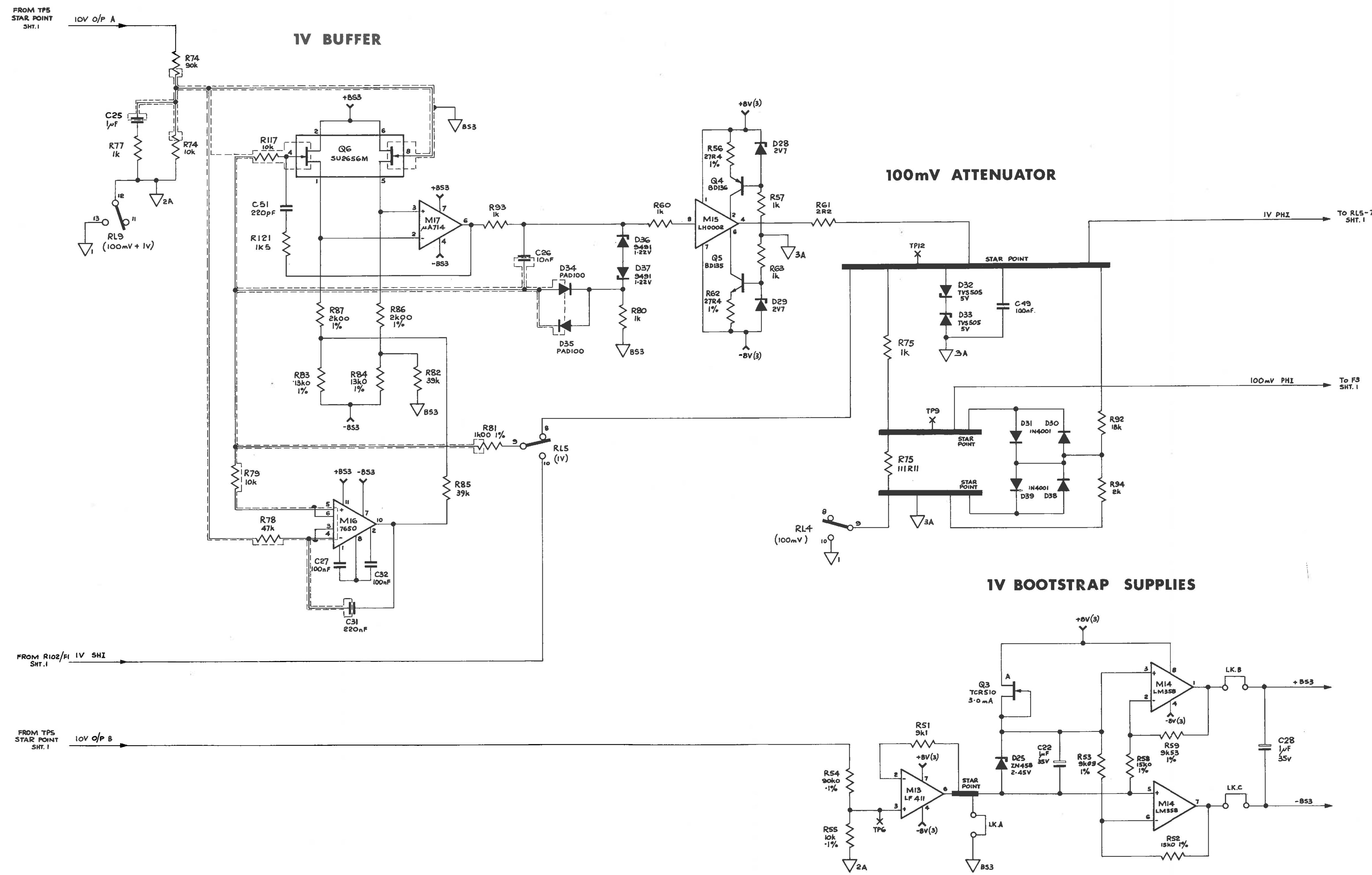
DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400445(A)	TITLE
IL	9.6.82		DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°		CIRCUIT DIAGRAM		4000/4000A DC PCB 10V/100V/1000V OUTPUTS
CHECKED R.K. COGGAN	DATE 25/6/82	SCALE	UNLESS OTHERWISE STATED	FINISH	CHECK PROCEDURE	460445(A)	
APPR.	DATE 2-7-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST	470445(A)	

DRAWING No. 430445 430445A

SHEET 1 OF 4

DRAWING No. 430445, 430445A

ISS.	CHANGES
1	RELEASED 25.6.82.
2	SEE SHT 1 AND 3.
3	ECO 1440 & 1444 C49, C51 & R121 ADDED. BJ. 11-2-83
4	ECO 1478 R69-R73, R76 DELETED R75 WAS 30R. IL C.G.83



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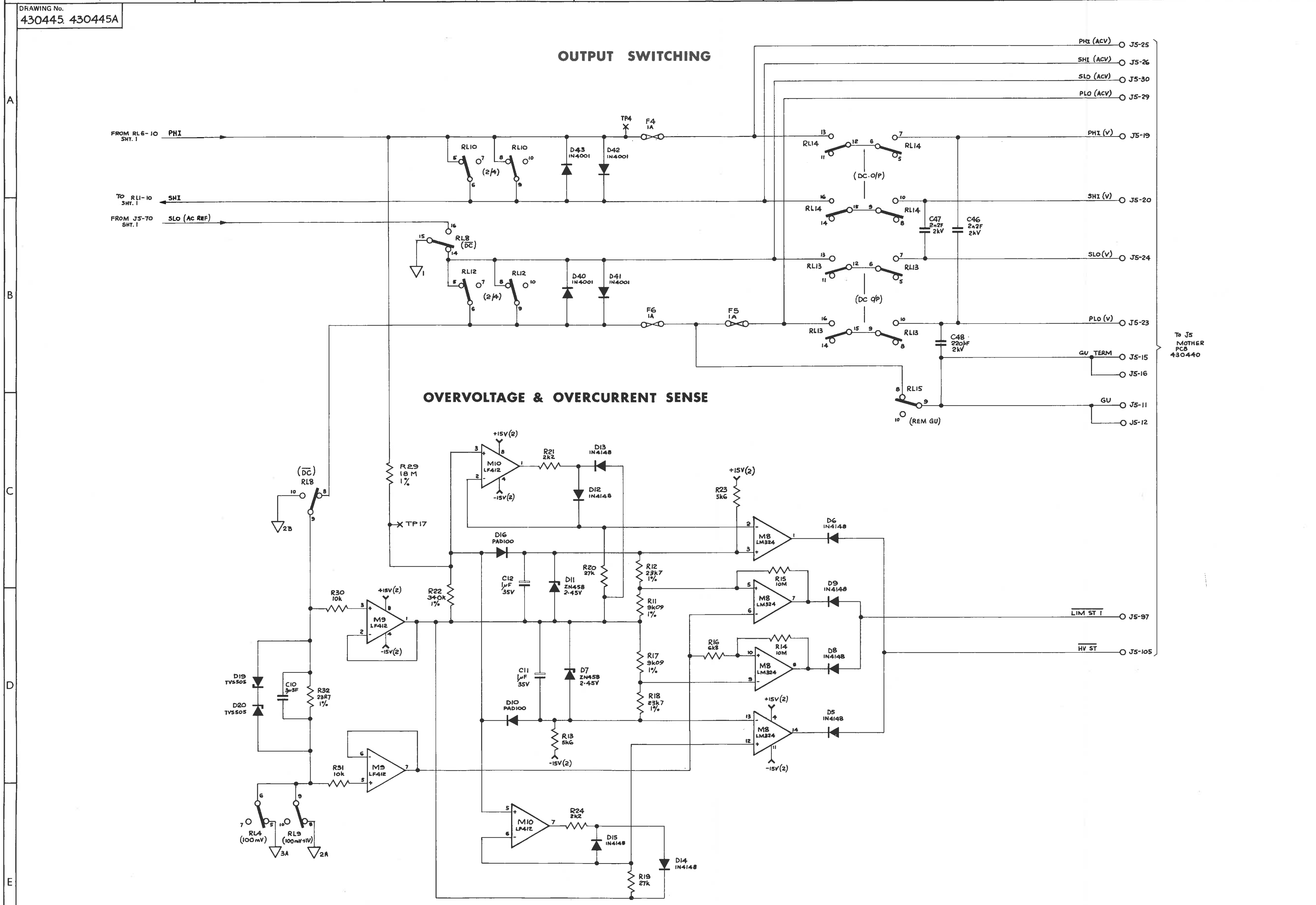
DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400445(A)	TITLE
IL	9.6.82	SCALE	DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°		CIRCUIT DIAGRAM		4000/4000A DC. PCB 1V & 100mV OUTPUTS
CHECKED R.K. COGGAN	DATE 25/6/82		UNLESS OTHERWISE STATED	FINISH	CHECK PROCEDURE	460445(A)	
APPR. B Hume	DATE 2-7-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST	470445(A)	

DRAWING No. 430445 430445A

SHEET 2 OF 4

DRAWING No. 430445. 430445A



ISS.	CHANGES
1	RELEASED 25.6.82
2	ECO 1376 R28, R49, R50, R67, R68, R90 + R91 DELETED R22 WAS 1M50 F6 WAS 62mA RL15-8 WENT TO V28 R25 WAS 10M. F5+F6 MOVED. TP17 ADDED. JR 25.8.82.
3	SEE SHEET 1 & 2
4	SEE SHEET 1 & 2

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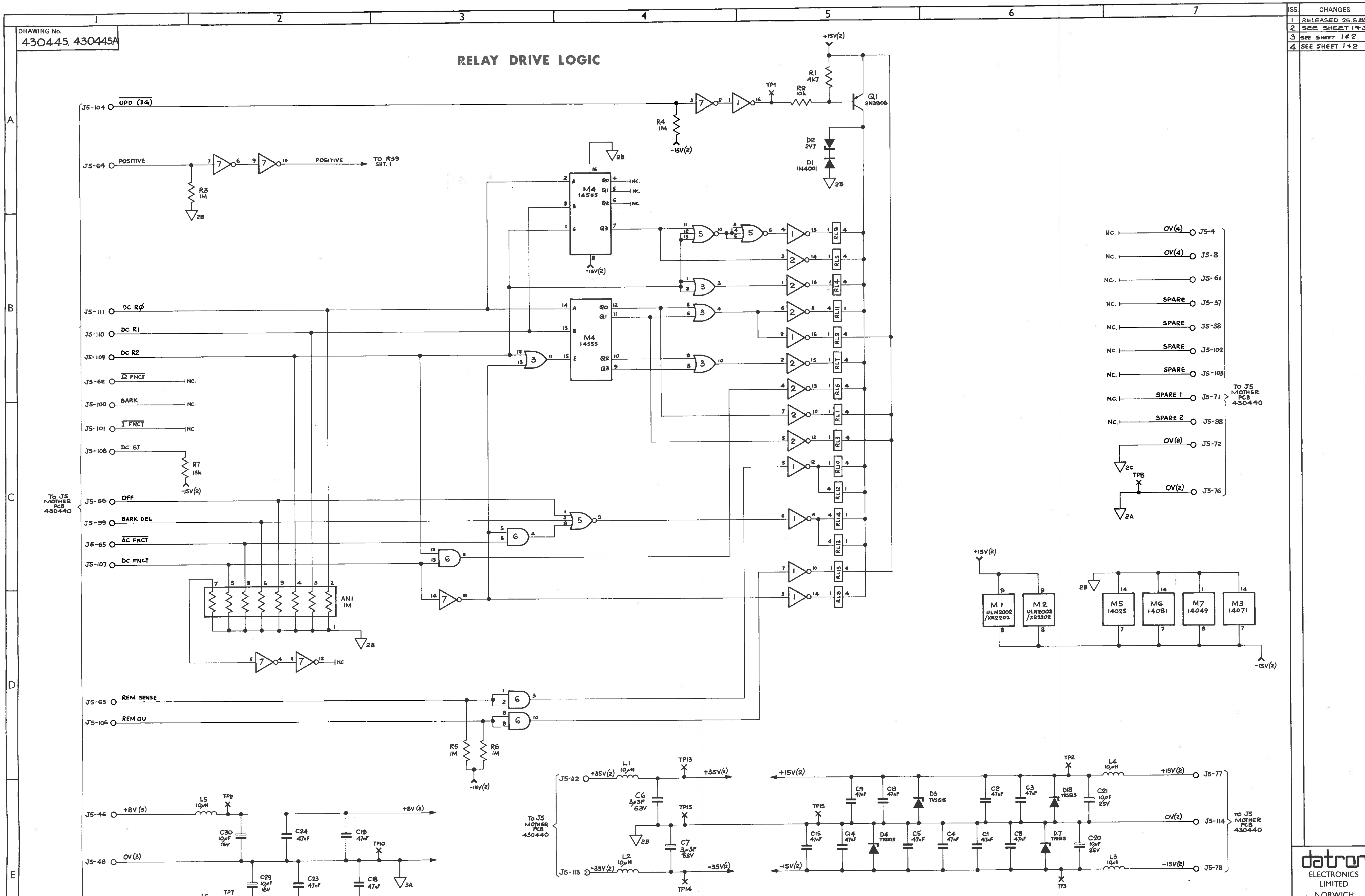
DRAWN IL	DATE 9.6.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ±·1mm; DECIMAL TO 1 PLACE ±·2mm; WHOLE DIMENSIONS ±·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400445(A)	TITLE 4000/4000A D.C. PCB OUTPUT SWITCHING AND OVERLOAD SENSE
CHECKED R.K. COGGAN	DATE 25/6/82	SCALE —	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM	DRAWING No. 430445 430445A
APPR.	DATE 2-7-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460445(A); CHECK LIST 470445(A)	SHEET 3 OF 4



DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400445(A)	TITLE
IL	9.6.82		DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°		CIRCUIT DIAGRAM		4000/4000A DC. PCB. RELAY DRIVE LOGIC + POWER SUPPLIES
CHECKED R.K.COGGAN	DATE 25/6/82	SCALE	UNLESS OTHERWISE STATED	FINISH	CHECK PROCEDURE	460445(A)	
APPR. B. Hume	DATE 2.7.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST	470445(A)	

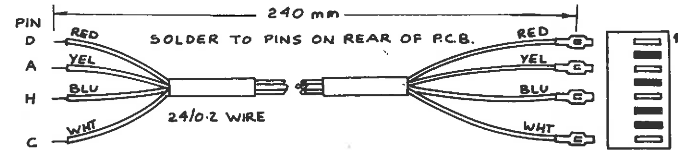
DRAWING No. 430445 430445A

SHEET 4 OF 4

DRAWING No. 400448

ISS.	CHANGES
4	ECO1481 NEW PCB LAYOUT. IL. 10.5.83
5	ECO. 1490. 1491 PARTS LIST CHANGES TO RESISTOR SET' ISSUES IL. 7.6.83
6	ECO 1529 D16 AND D17 WERE 200010. P.C.B WAS ISSUE 2A. UP. 15.9.83
7	ECO. 1537 TRACK TO M20-7 IS CUT. M19-1 & M20-7 LINKED. IL. 29.9.83

4 OFF CRIMPS 605077
1 OFF HOUSING 605072
2 OFF SLEEVE 590002



MOUNTING I.C.s.			
Nº OF WAYS	PART Nº	Nº OFF	
14	605060	8	M3. M5. M9. M10. M15 M16. M17. M19.
16	605061	6	M6. M12. M13 M14. M18. M20.

NO COMPONENTS WITHIN THIS AREA DEFINED BY DOTTED LINE, SHOULD BE NO HIGHER THAN 7mm.

MOUNT R2, R3, R4, R35 & F1-F3 ON SMALL CERAMIC BEAD 630036 14 OFF

ALL TEST LINKS & LINKS USE 22 SWG BTC WIRE 540002. WHEN SLEEVING REQ'D USE SLEEVE 590004.

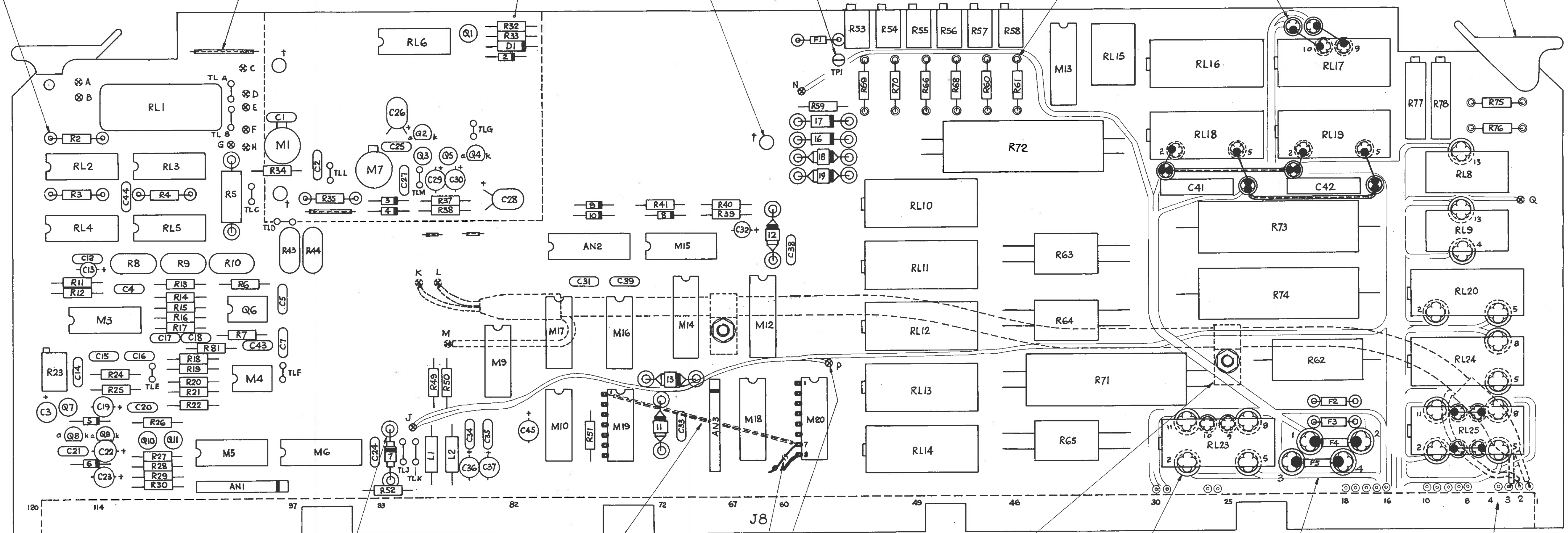
† FIXING HOLE FOR MOUNTING ALTERNATIVE RES/HEATSINK ASSYS - SEE SHT 2.

1 OFF TEST POINT TERMINAL 620007

MOUNT R60, R61, R66, R68, R69, R70 R75, R76 ON FSV TERMINAL. 602001 16 OFF.

18 OFF SMALL CLOVERLEAF TERMINAL 620001

2 OFF CIRCUIT BOARD EJECTOR 630122 (BLUE)



410262-2B

MOUNT R5, D7, D11, D12, D13, D16-D19 ON LARGE CERAMIC BEAD 630024 18 OFF

LINK M19 PIN 1 TO M20 PIN 7 USING WIRE LINK (540006) SOLDER TO PCB ON SOLDER SIDE OF BOARD.

CUT TRACK ON COMP. SIDE OF PCB.

15 OFF SOLDER TERMINAL 620003. MOUNT A, C, D, H, K, L & M UNDERSIDE OF BOARD.

N.B. ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED, USE SLEEVE 590001 (X6), EXCEPT THOSE ON UNDERSIDE.

2 OFF 'P' CLIP 630003
2 OFF SCREW M3 x 10 POZI-PAN 611006
2 OFF NUT M3 HEX FULL 615002
2 OFF M3 CRINKLE WASHER 613029
2 OFF M3 PLAIN WASHER 613007

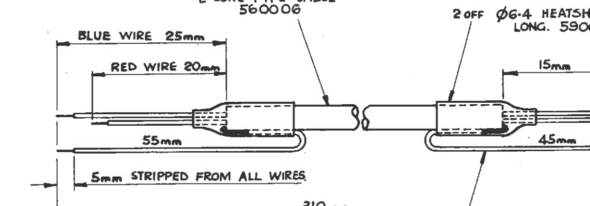
19 OFF LARGE CLOVERLEAF TERMINAL 620005

EASE WIRES INTO PATHS BETWEEN COMPONENTS AS NEATLY AS POSSIBLE. SEE SHEET 2 FOR POINT TO POINT WIRING SCHEDULE.

RED WIRE TO PIN.1 & PIN L
WHITE WIRE TO PIN.2 & PIN M
BLUE WIRE TO PIN 3 & PIN K

2 CORE PTFE CABLE 560006

2 OFF Ø6.4 HEATSHRINK 20mm LONG. 590003



2 OFF WHITE WIRES 7/0.2 PTFE 540008 SOLDERED TO SCREEN AS ABOVE

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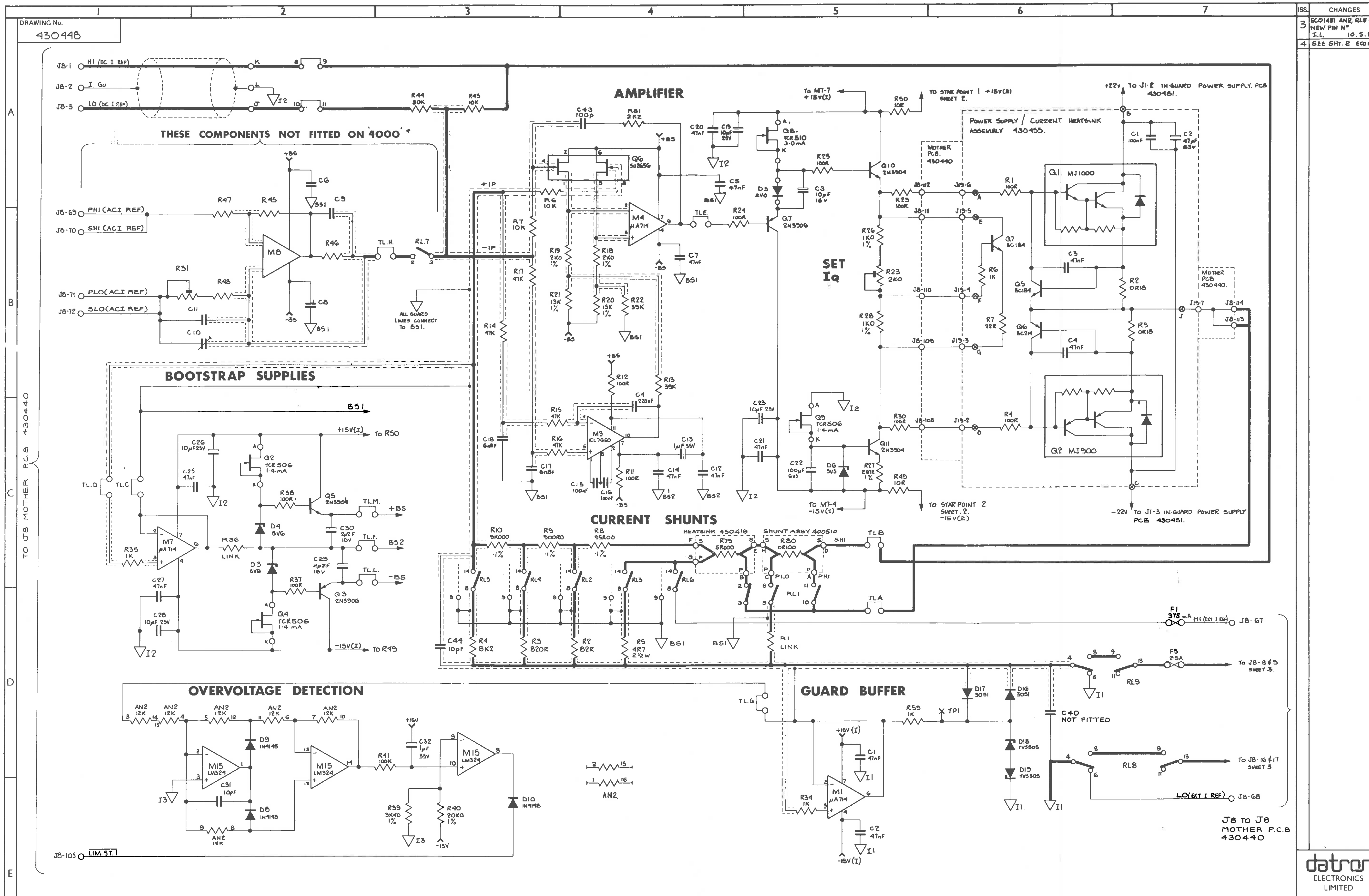
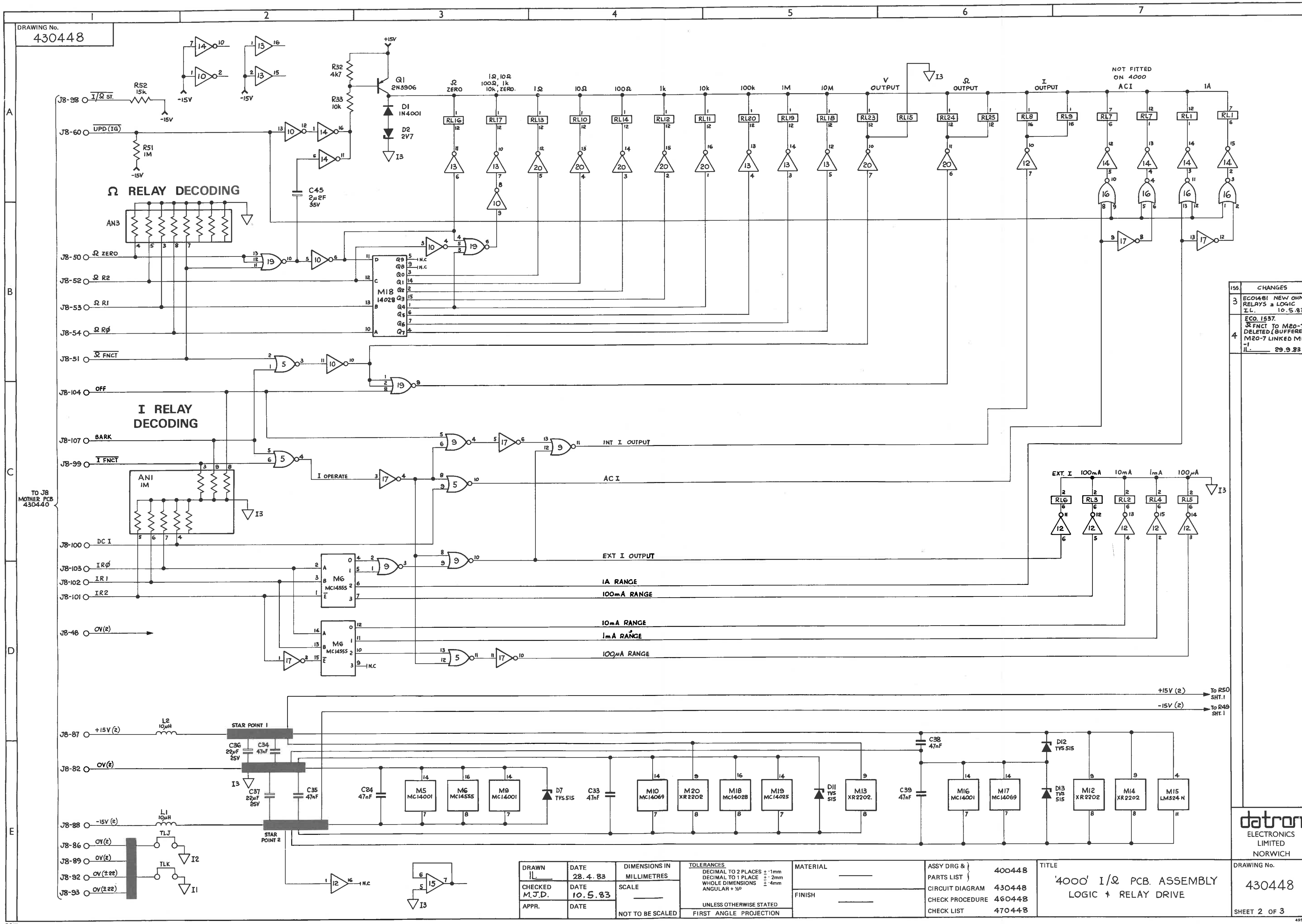
DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400448	TITLE	DRAWING No.
IL	22.4.83	SCALE 2:1	DECIMAL TO 2 PLACES ± .1mm; DECIMAL TO 1 PLACE ± .2mm; WHOLE DIMENSIONS ± .4mm; ANGULAR ± ½°	FINISH	CIRCUIT DIAGRAM	430448	4000 I/Ω PCB ASSEMBLY	400448
CHECKED M.J.D.	DATE 10.5.83	NOT TO BE SCALED	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION		CHECK PROCEDURE	460448		SHEET 1 OF 15
APPR.	DATE				CHECK LIST	470448		



DRAWN	IL	DATE	26.4.83	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	—	ASSY DRG & PARTS LIST	400448	TITLE	'4000' I/Ω PCB ASSEMBLY. VOLTAGE TO CURRENT CONVERTER
CHECKED	M.J.D.	DATE	10.5.83	SCALE —	UNLESS OTHERWISE STATED	FINISH	—	CIRCUIT DIAGRAM	430448	DRAWING No.	430448
APPR.		DATE		NOT TO BE SCALED	FIRST ANGLE PROJECTION			CHECK PROCEDURE	460448	SHEET	1 OF 3
								CHECK LIST	470448		



DRAWING No. 430448
Ω RELAY DECODING
I RELAY DECODING
TO J8 MOTHER PCB 430440
J8-98 I/Ω ST.
J8-60 UPD (IG)
J8-50 Ω ZERO
J8-52 Ω R2
J8-53 Ω R1
J8-54 Ω RØ
J8-51 Ω FNCT
J8-104 OFF
J8-107 BARK
J8-99 I FNCT
J8-100 DC I
J8-103 IRØ
J8-102 IR1
J8-101 IR2
J8-48 OV(2)
J8-87 +15V (2)
J8-82 OV(2)
J8-88 -15V (2)
J8-86 OV(2)
J8-89 OV(2)
J8-92 OV(2 2)
J8-93 OV(2 2)
INT I OUTPUT
AC I
EXT I OUTPUT
1A RANGE
100mA RANGE
10mA RANGE
1mA RANGE
100μA RANGE
I OPERATE
V OUTPUT
Ω OUTPUT
I OUTPUT
NOT FITTED ON 4000
ACI
1A
EXT. I
STAR POINT 1
STAR POINT 2
+15V (2) To R50 SHT. 1
-15V (2) To R49 SHT. 1
CHANGES
3 ECO1481 NEW OHMS RELAYS & LOGIC I.L. 10.5.83
4 ECO. 1537. Ω FNCT TO M20-7 DELETED (BUFFERED) M20-7 LINKED M19-1 IL. 29.9.83
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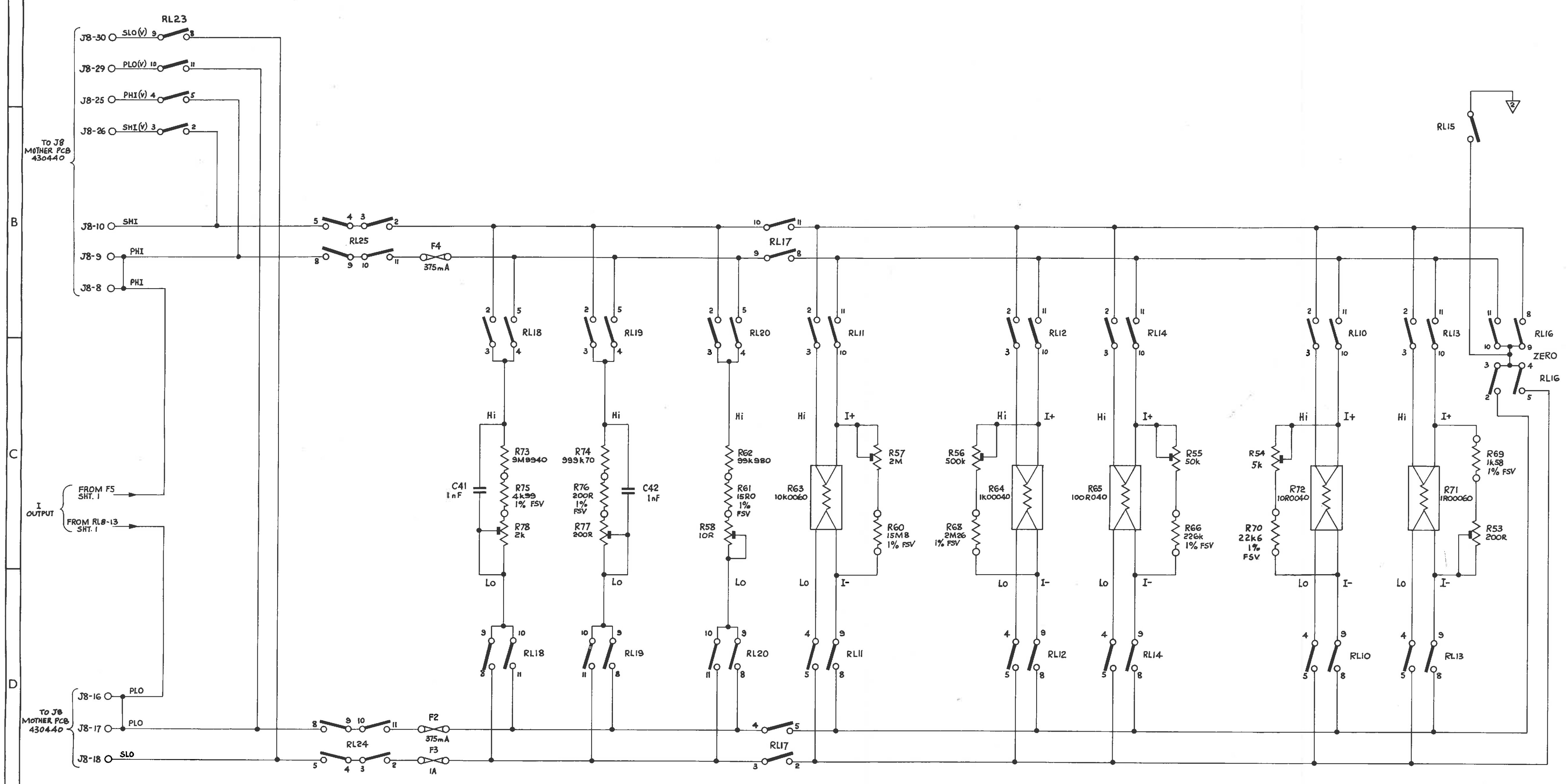
DRAWN IL DATE 28.4.83
CHECKED M.J.D. DATE 10.5.83
APPR. DATE
DIMENSIONS IN MILLIMETRES
SCALE
NOT TO BE SCALED
TOLERANCES
UNLESS OTHERWISE STATED
FIRST ANGLE PROJECTION
MATERIAL
FINISH
ASSY DRG & PARTS LIST 400448
CIRCUIT DIAGRAM 430448
CHECK PROCEDURE 460448
CHECK LIST 470448
TITLE '4000' I/Ω PCB. ASSEMBLY LOGIC + RELAY DRIVE
DRAWING No. 430448
SHEET 2 OF 3

DRAWING No. 430448

ISS.	CHANGES
3	ECO1481 NEW RELAY SWITCHING. C41&42 WERE 10nF I.L. 10.5.83
4	SEE SHT. 2



DRAWN	DATE 26.4.83	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½° UNLESS OTHERWISE STATED	MATERIAL	ASSY DRG & PARTS LIST 400448
CHECKED MJD	DATE 10.5.83	SCALE		FINISH	CIRCUIT DIAGRAM 430448
APPR.	DATE	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460448
					CHECK LIST 470448

TITLE: 4000 I Ω PCB ASSY STANDARD RESISTORS + SWITCHING.

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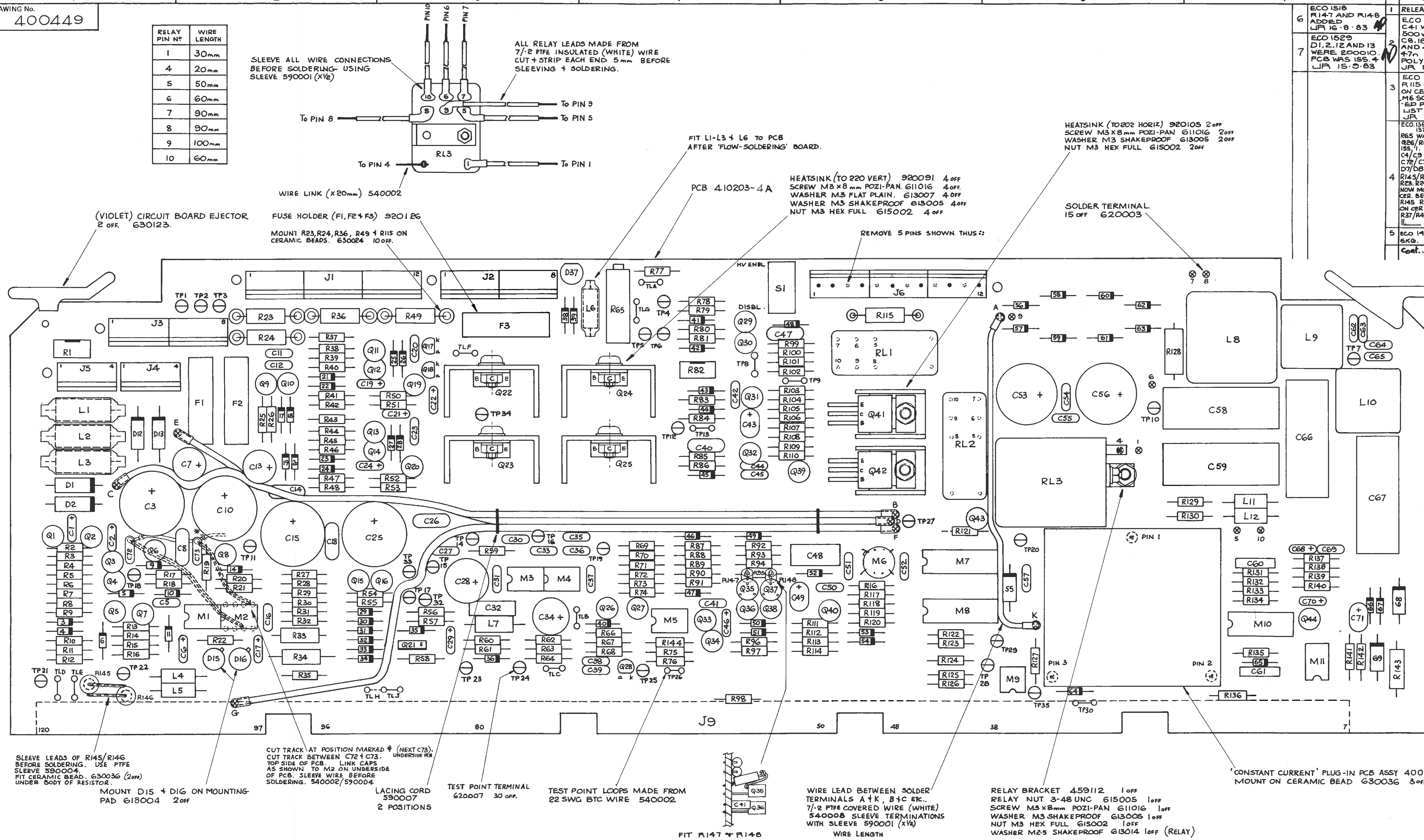
DRAWING No. 430448

SHEET 3 OF 3

DRAWING No. 400449

RELAY PIN Nº	WIRE LENGTH
1	30mm
4	20mm
5	50mm
6	60mm
7	90mm
8	90mm
9	100mm
10	60mm



NOTE: USE HEATSINK COMPOUND BETWEEN MATING SURFACES OF Q22, Q23, Q24, Q25, Q41 + Q42 AND THE RESPECTIVE HEATSINKS 900003 A TORQUE OF 0·5 Nm. SHOULD BE APPLIED TO TIGHTEN COMPONENT FIXING.

I.C. MOUNTING

Nº WAYS	PART Nº	Nº OFF	USED TO MOUNT
8	605059/A	6	M1-M5, M11
14	605060/A	1	M10
16	605061/A	2	M7, M8
6	605066/A	1	M9

ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 C41 WAS 4n7 500V CER. DISC. C8, 18, 14, 26, 40 AND 47 WERE 47n 63V POLYESTER. JR 17.5.82.
3	ECO 1353, 1356. R115 NOW MOUNTED ON CERAMIC BEADS. M6 SOCKET REMOVED PLUS PARTS LIST CHANGE. JR 5·7·82
4	ECO. 1364. 1366. 1368 1375. 1381. 1388 R65 WAS 20k POT. Q26/R66 KIT WAS ISS. 1. C4/C9 DELETED. C72/C73 ADDED. D7/D8 DELETED R145/R146 ADDED R23. R24. R36 + R49 NOW MOUNTED ON CER. BEADS 630024. R145 R146 MOUNTED ON CER. BEAD 630036. R37/R43 WERE 22k. IL 23.8.82
5	ECO 1458. R6 WAS 5K6. 8-4-83. BJ.
	Cont....
6	ECO 1518 R147 AND R148 ADDED JR 16·8·83
7	ECO 1529 D1, 2, 12 AND 13 WERE 200010. PCB WAS ISS. 4 JR 15·9·83

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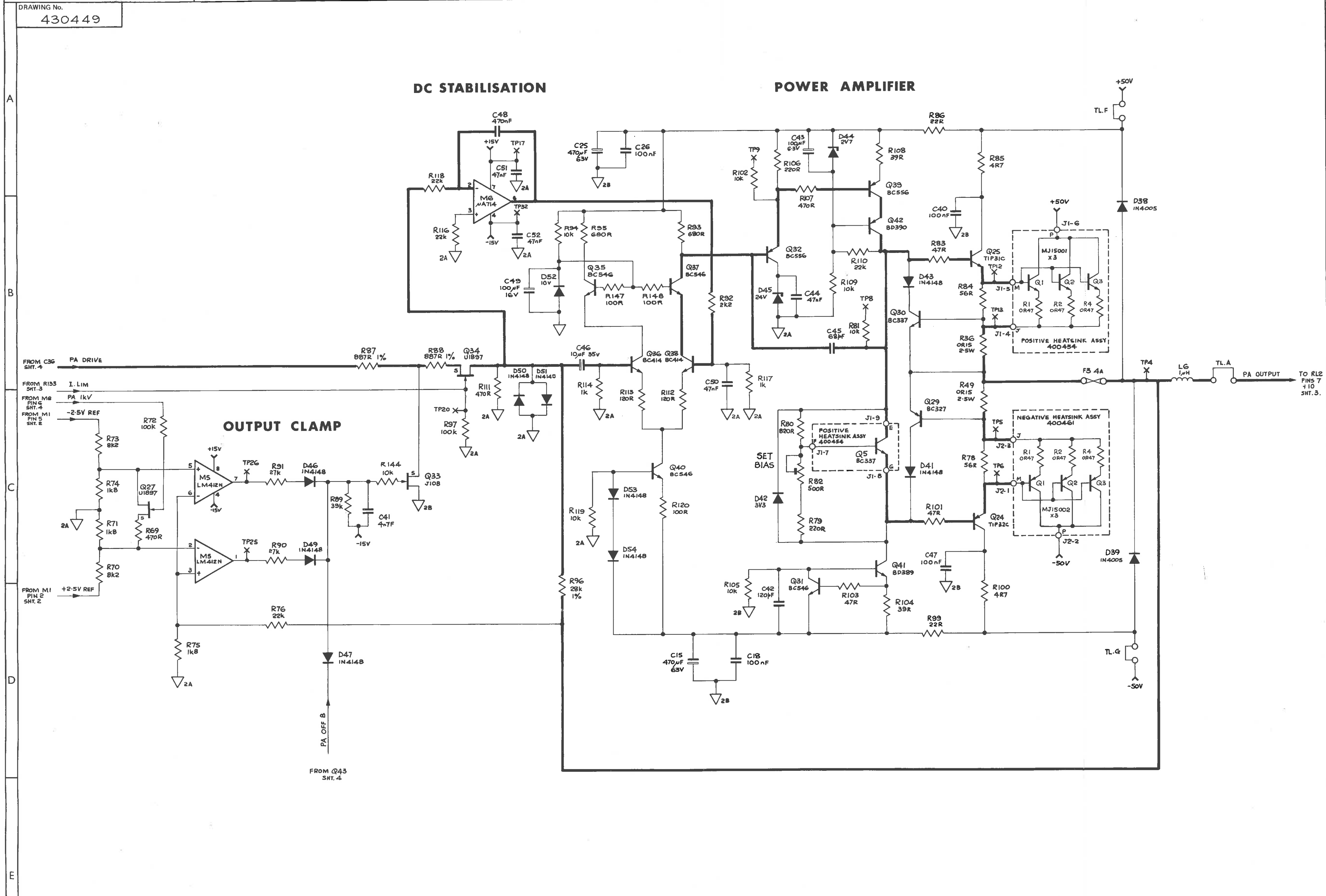
DRAWN IL	DATE 1.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR + ½°	MATERIAL	ASSY DRG & PARTS LIST 400449	TITLE 4000. POWER AMP (D.C) PCB. ASSY.
CHECKED MJD	DATE 16.4.82	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430449	DRAWING No. 400449
APPR. B Hume	DATE 23.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460449 CHECK LIST 470449	SHEET 1 OF 21

4951MT

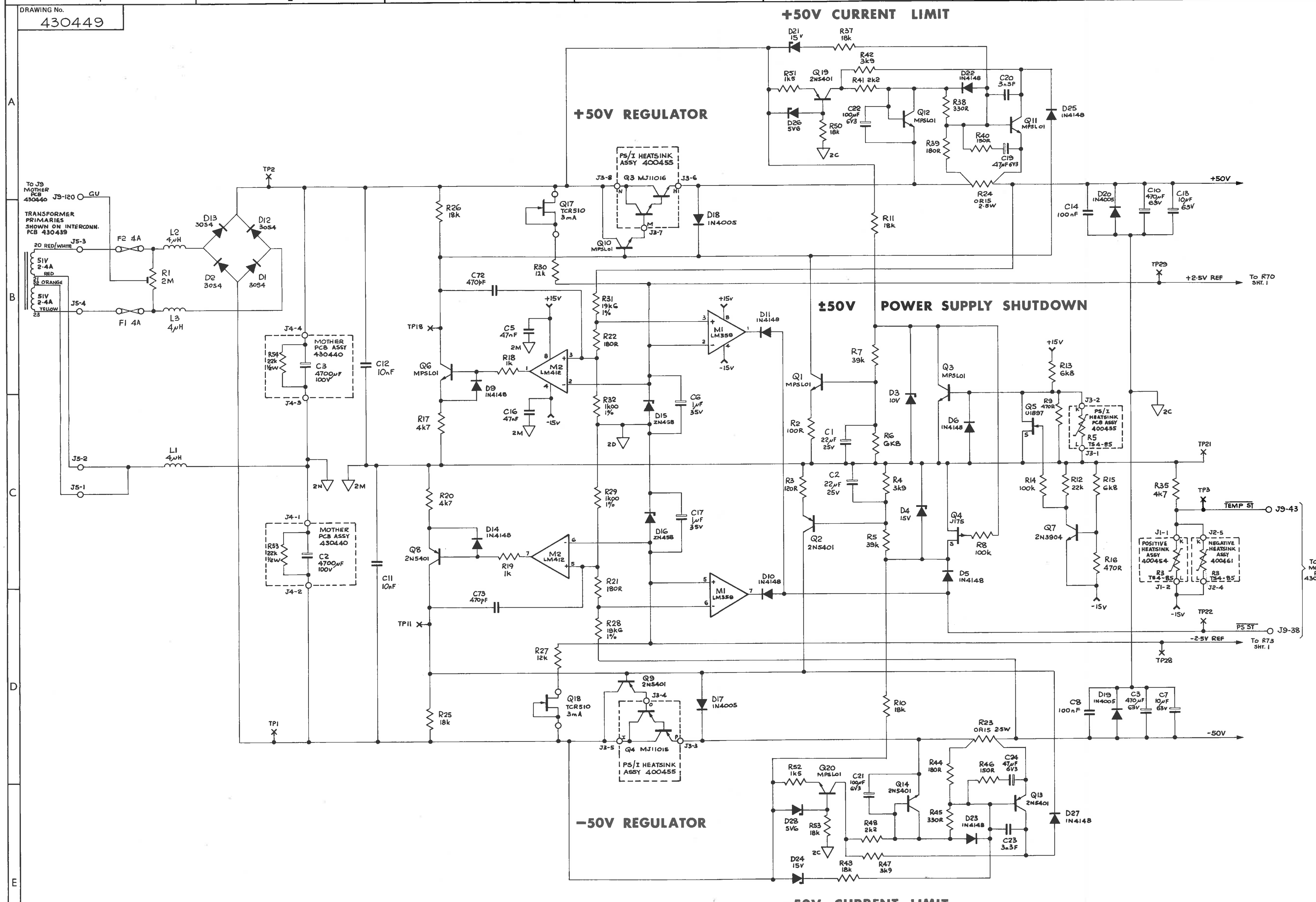
DRAWING No. 430449

ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 SEE SHT 5.
3	SEE SHT 2.
4	SEE SHTS. 2 4 + 5
5	SEE SHEET. 2.
6	ECO 1518 R147 AND R148 ADDED. JR 12.8.83



DRAWN	DATE 17.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400449	TITLE 4000. POWER AMP (D.C.) D.C. POWER AMPLIFIER	datron ELECTRONICS LIMITED NORWICH
CHECKED J.B.S.	DATE 23.4.82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM		DRAWING No. 430449
APPR.	DATE 23.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460449		
					CHECK LIST 470449		SHEET 1 OF 5

DRAWING No. 430449



ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 SEE SHT S.
3	ECO 1356 R37 AND R43 WERE 12K. D21 AND D24 WERE 30V. JR 5.7.82.
4	ECO 1368 C4/C9 DELETED C72/C73 ADDED R37 R43 WERE 22k IL 23.8.82
5	ECO 1458 R6 WAS 5K6. 8-4-83
6	ECO 1518 SEE SHEET 1.

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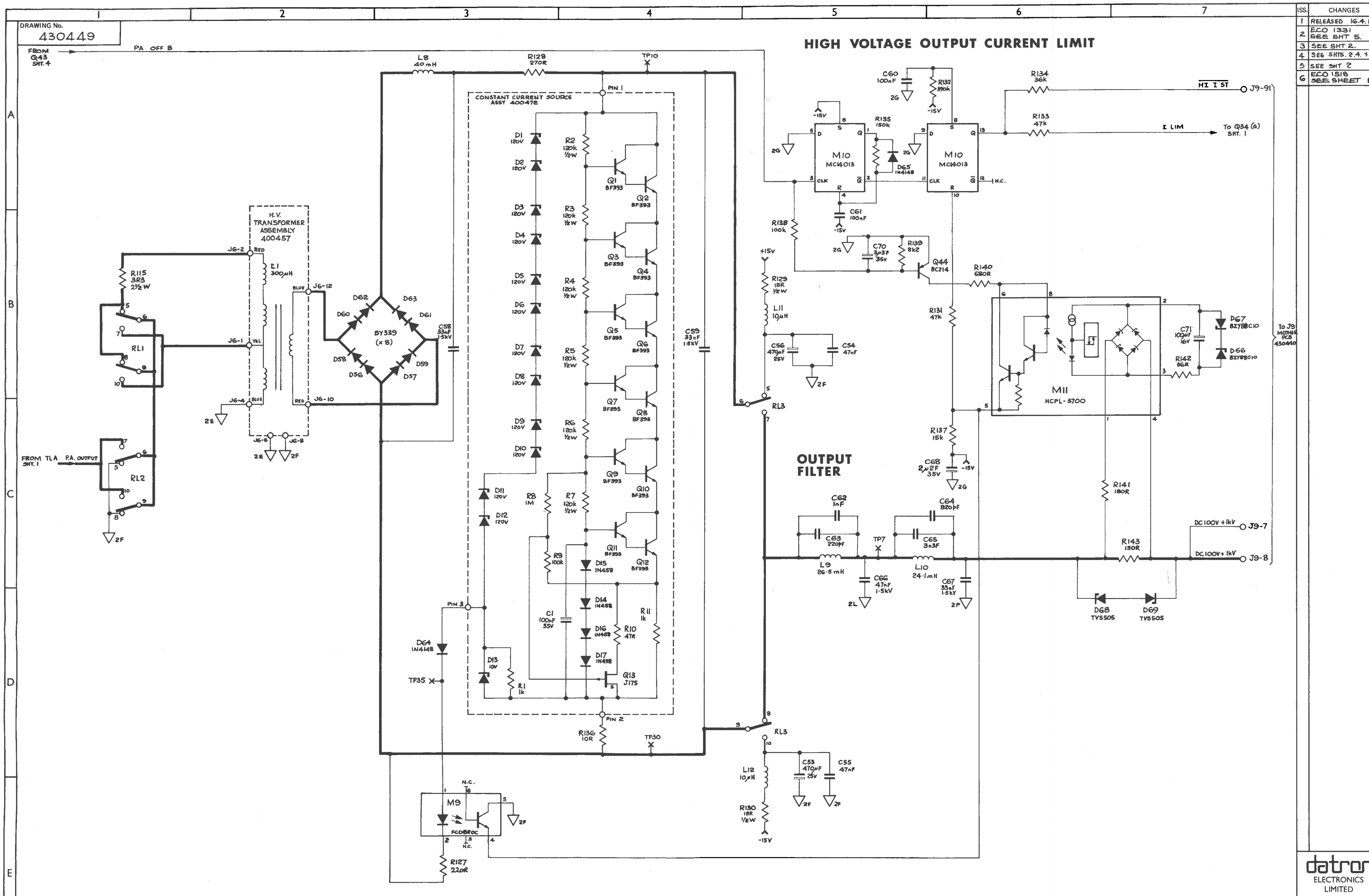
DRAWN IL	DATE 17.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400449
CHECKED G.S.S.	DATE 23.4.82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM
APPR.	DATE 23.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460449
					CHECK LIST 470449

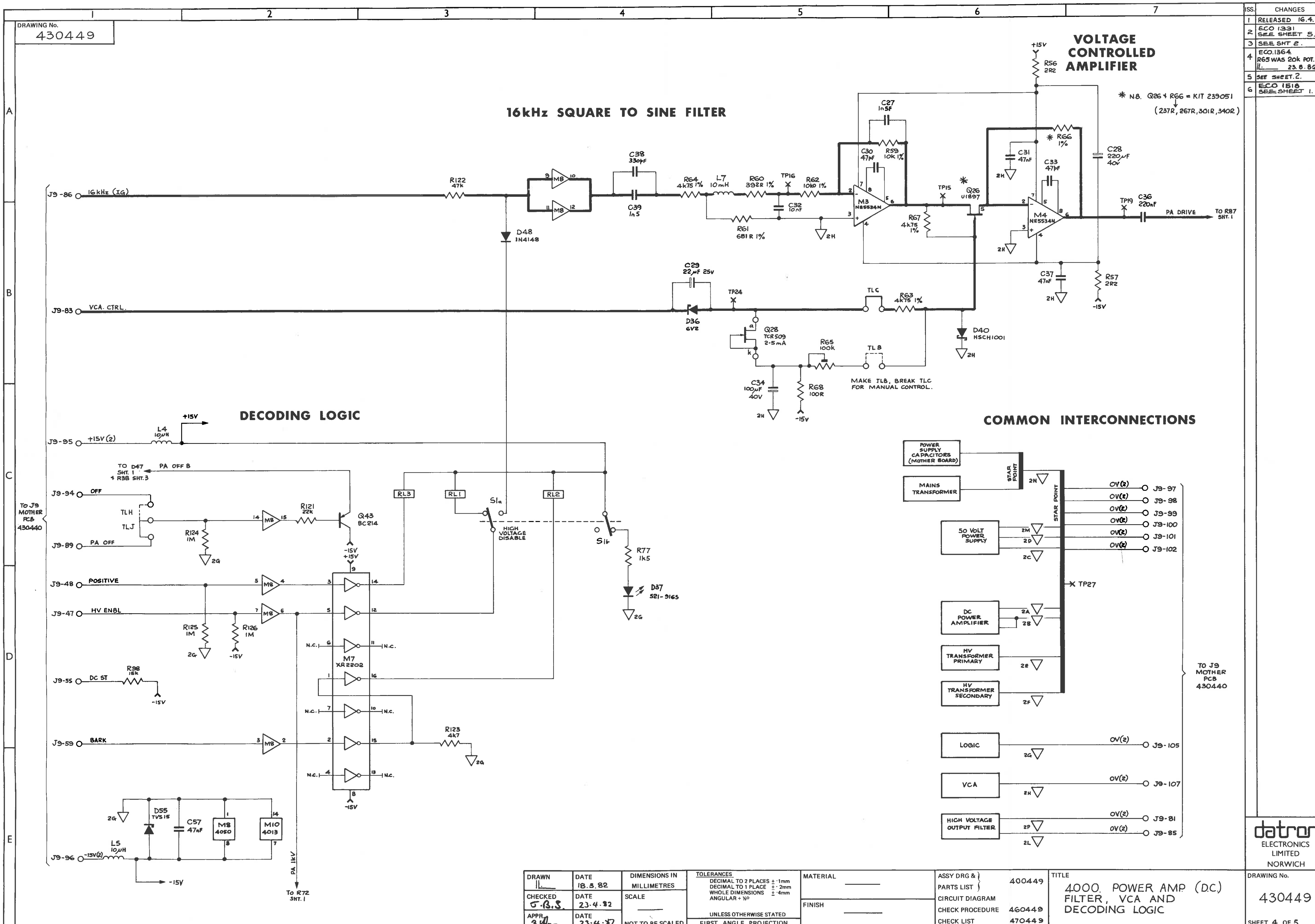
TITLE: 4000 POWER AMP (DC) ±50V POWER SUPPLY

DRAWING No. 430449

SHEET 2 OF 5



DRAWN	DATE 17.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400449	TITLE 4000. POWER AMP (DC) HIGH VOLTAGE OUTPUT.	DRAWING No. 430449
CHECKED	DATE 23.4.82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM		
APPR.	DATE 27.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460449		
					CHECK LIST 470449		SHEET 3 OF 5



DRAWING No. 430449
VOLTAGE CONTROLLED AMPLIFIER
16kHz SQUARE TO SINE FILTER
DECODING LOGIC
COMMON INTERCONNECTIONS
* N.B. Q26 + R66 = KIT 239051 (237R, 267R, 301R, 340R)
MAKE TLB, BREAK TLC FOR MANUAL CONTROL.
J9-86 16kHz (IG)
J9-83 VCA. CTRL.
J9-95 +15V (2)
J9-94 OFF
J9-89 PA OFF
J9-48 POSITIVE
J9-47 HV ENBL
J9-55 DC ST
J9-59 BARK
J9-96 -15V(2)
TO D47 SHT. 1 + R38 SHT. 3
PA OFF B
PA DRIVE
TO R87 SHT. 1
To J9 MOTHER PCB 430440
HIGH VOLTAGE DISABLE
PA 1kV
To R72 SHT. 1
POWER SUPPLY CAPACITORS (MOTHER BOARD)
MAINS TRANSFORMER
STAR POINT
50 VOLT POWER SUPPLY
DC POWER AMPLIFIER
HV TRANSFORMER PRIMARY
HV TRANSFORMER SECONDARY
LOGIC
VCA
HIGH VOLTAGE OUTPUT FILTER
J9-97
J9-98
J9-99
J9-100
J9-101
J9-102
J9-105
J9-107
J9-81
J9-85
TO J9 MOTHER PCB 430440
ISS. CHANGES
1 RELEASED 16.4.82
2 ECO 1331 SEE SHEET 5.
3 SEE SHT 2.
4 ECO.1364 R65 WAS 20k POT. 23.8.82
5 SEE SHEET.2.
6 ECO 1518 SEE SHEET 1.
DRAWN
DATE 18.3.82
CHECKED
DATE 23.4.82
APPR.
DATE 23.4.82
DIMENSIONS IN MILLIMETRES
SCALE
NOT TO BE SCALED
TOLERANCES
DECIMAL TO 2 PLACES ± ·1mm
DECIMAL TO 1 PLACE ± ·2mm
WHOLE DIMENSIONS ± ·4mm
ANGULAR ± ½°
UNLESS OTHERWISE STATED
FIRST ANGLE PROJECTION
MATERIAL
FINISH
ASSY DRG & PARTS LIST 400449
CIRCUIT DIAGRAM
CHECK PROCEDURE 460449
CHECK LIST 470449
TITLE
4000 POWER AMP (D.C.) FILTER, VCA AND DECODING LOGIC
datron ELECTRONICS LIMITED NORWICH
DRAWING No. 430449
SHEET 4 OF 5

DRAWING No. 430449

FIRST USED ON

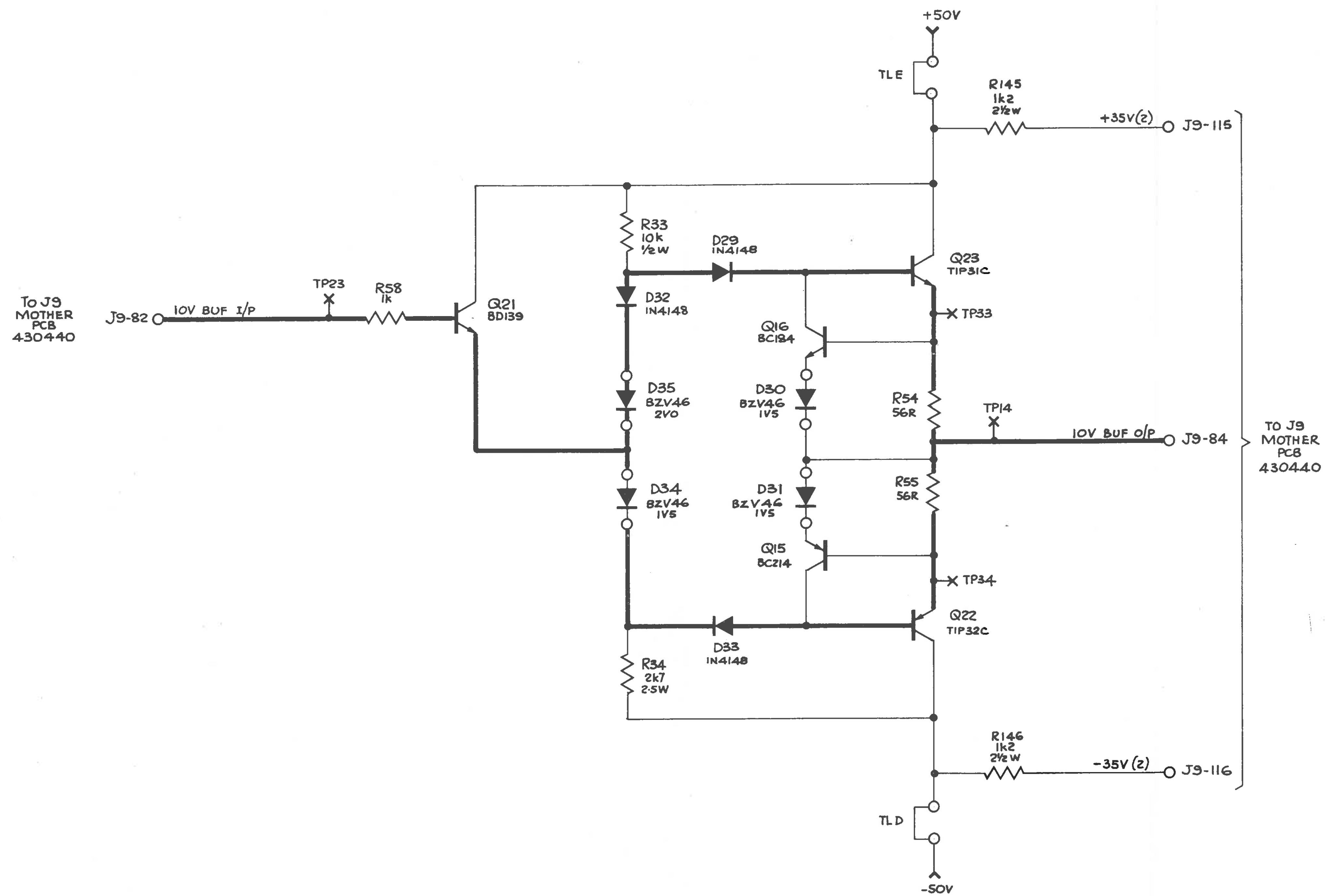
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 D7 AND D8 WERE BZY88C-15V JR 17.5.82
3	SEE SHT 2
4	ECO. 1375 D7/D8 DELETED R145/R146 ADDED IL 23.8.82
5	SEE SHEET 2.
6	ECO 1518 SEE SHEET 1



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DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400449	TITLE	DRAWING No.
IL	18.3.82		DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	———	CIRCUIT DIAGRAM		4000. POWER AMP (DC) 10V DC BUFFER AMP	430449
CHECKED J.BS.	DATE 23.4.82	SCALE ———		FINISH ———	CHECK PROCEDURE	460449		
APPR. B Hume	DATE 23.4.82	NOT TO BE SCALED	UNLESS OTHERWISE STATED; FIRST ANGLE PROJECTION		CHECK LIST	470449		SHEET 5 OF 5

4951MT

DRAWING No. 400451

ISS.	CHANGES
1	RELEASED 9-3-82
2	ECO 1325 D6 WAS 18V JR 13.5.82.
3	ECO 1525 D1, D2, D3 AND D4 WERE 200010 P.C.B WAS ISS 6. JR 15.9.83

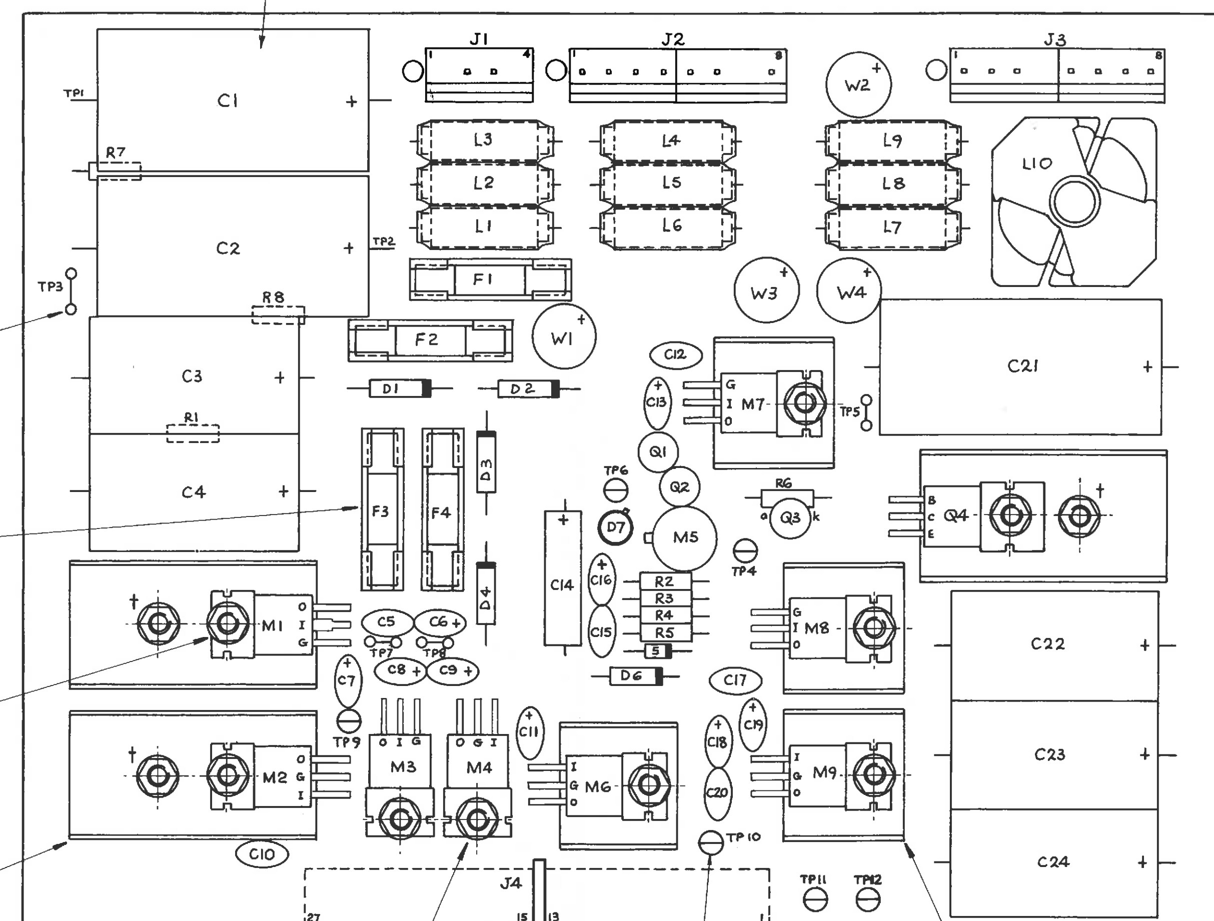
BED C1 TO C4 AND C21 TO C24 IN SILICONE RUBBER (900004)

MAKE ALL TEST POINT LOOPS FROM 22 SWG BTC WIRE 540002

4 OFF FUSE HOLDER 920126
2 OFF FUSE (4A S/B) 920128 – F1, F2
2 OFF FUSE (2A S/B) 920127 – F3, F4

M1, M2 & Q4 FIXINGS
3 OFF SCREW M3X 8 mm POZIPAN 611016
3 OFF NUT M3 FULL HEX 615002
3 OFF WASHER M3 SHAKEPROOF 613005

HEATSINK – PCB FIXING
† 3 OFF HEATSINK (TO 220×2) 920090
3 OFF SCREW M3×8mm POZIPAN 611016
3 OFF NUT M3 FULL HEX 615002
3 OFF WASHER M3 SHAKEPROOF 613005



PCB 410160-6A

NOTE: USE HEATSINK COMPOUND (900003) BETWEEN MATING SURFACES OF Q4, M1-M2, M6-M9 AND THE RESPECTIVE HEATSINKS. A TORQUE OF 0.5Nm SHOULD BE APPLIED TO TIGHTEN COMPONENT FIXINGS.

2 OFF SCREW M3x8mm POZIPAN 611016
2 OFF NUT M3 FULL HEX 615002
2 OFF WASHER M3 SHAKEPROOF 613005

TEST POINT TERMINAL 620007 6 OFF.

4 OFF HEATSINK (TO 220) 920089
4 OFF SCREW M3 × 8 POZI PAN 611016
4 OFF NUT M3 FULL HEX 615002
4 OFF WASHER M3 SHAKEPROOF 613005.

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DRAWN JL	DATE 3.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400451
CHECKED MJD	DATE 9.3.82	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430451
APPR. B Blume	DATE 17-3-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460451
					CHECK LIST 470451

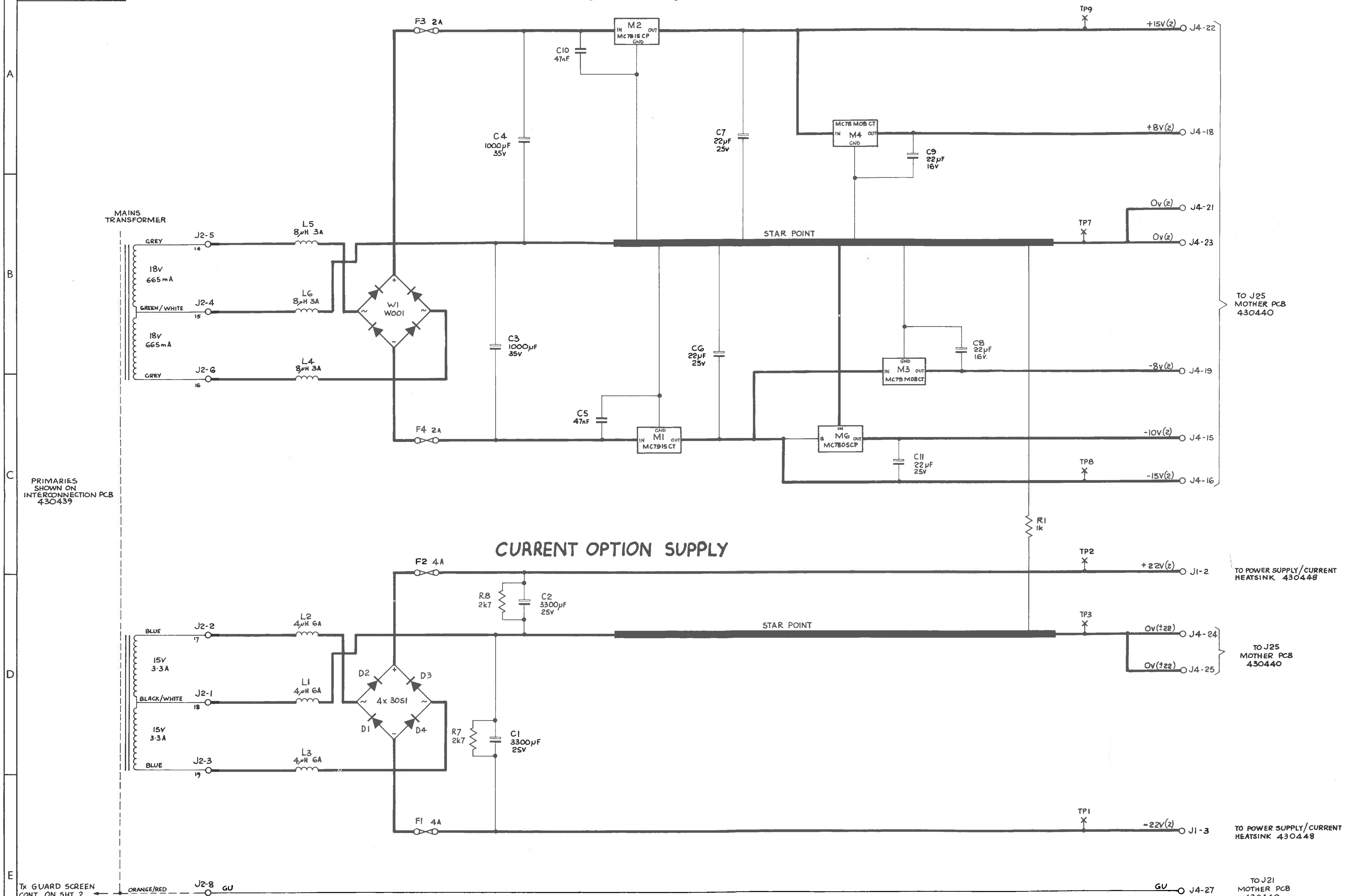
TITLE 4000. IN-GUARD POWER SUPPLY P.C.B. ASSY.

DRAWING No. 400451

SHEET 1 OF 5

DRAWING No. 430451

IN GUARD COMMON 2 SUPPLIES



ISS.	CHANGES
1	RELEASED 9-3-82
2	E.C.O 1325 D6 WAS 18V JR 13.5.82

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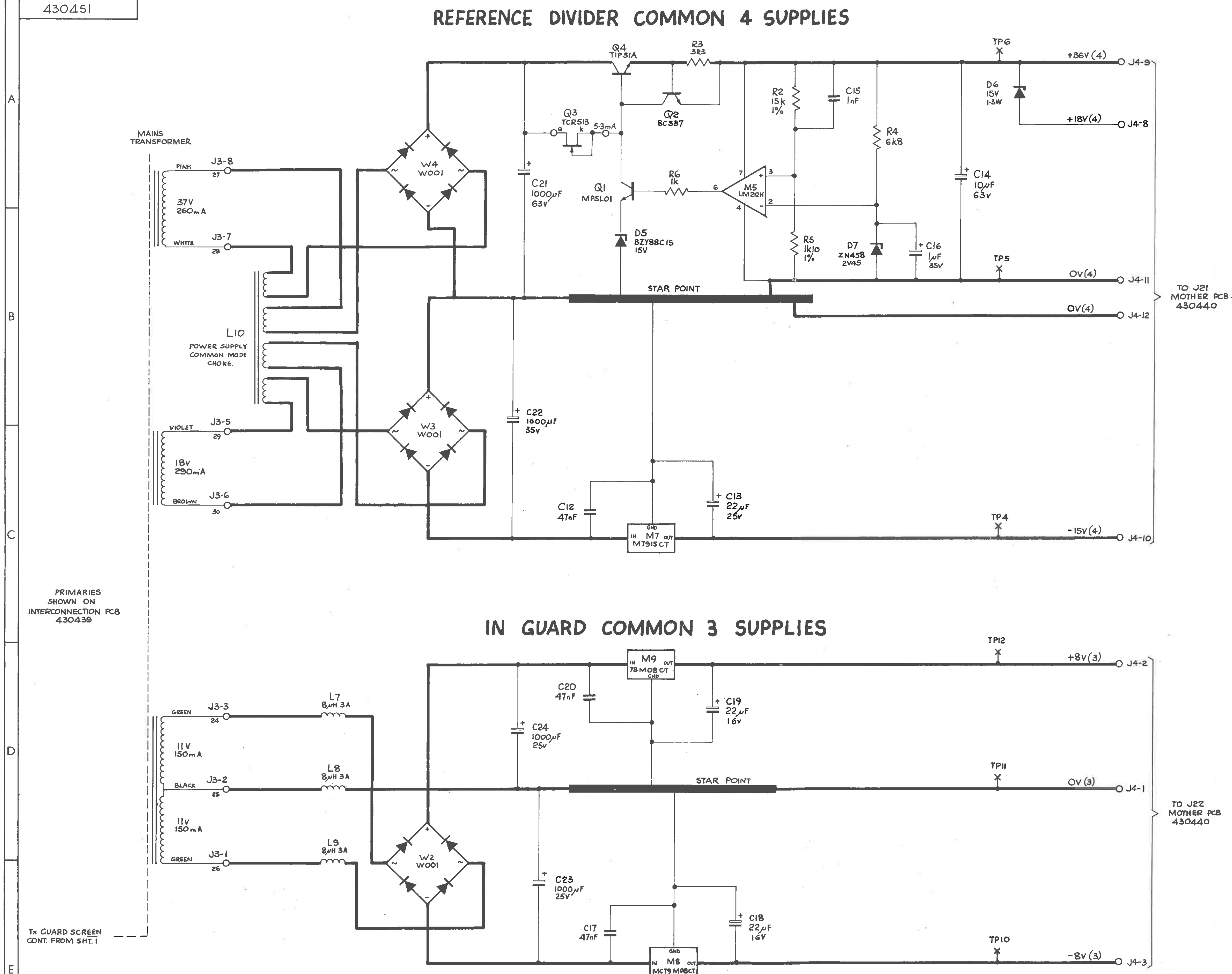
DRAWN	DATE 3.3.82.	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm, DECIMAL TO 1 PLACE ± ·2mm, WHOLE DIMENSIONS ± ·4mm, ANGULAR ± ½° UNLESS OTHERWISE STATED	MATERIAL	ASSY DRG & PARTS LIST 400451	TITLE 4000 POWER SUPPLY IN-GUARD	DRAWING No. 430451
CHECKED R.K. COGGAN	DATE 9-3-82	SCALE		FINISH	CIRCUIT DIAGRAM 430451		
APPR. B. Hume	DATE 17-3-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460451		
					CHECK LIST 470451		SHEET 1 OF 2

DRAWING No. 430451

ISS.	CHANGES
1	RELEASED 9-3-82
2	ECO 1325 D6 WAS 18 V JR 13.5.82



DRAWN JL	DATE 3.3.82.	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm, DECIMAL TO 1 PLACE ± ·2mm, WHOLE DIMENSIONS ± ·4mm, ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400451	TITLE 4000 POWER SUPPLY IN-GUARD	DRAWING No. 430451
CHECKED R.K. COGGAN	DATE 9-3-82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430451		SHEET 2 OF 2
APPR. B Vane	DATE 17-3-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460451		
					CHECK LIST 470451		

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1	2	3	4	5	6

DRAWING No. 400452 / 400452A

FIRST USED ON 4000/4000A

THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

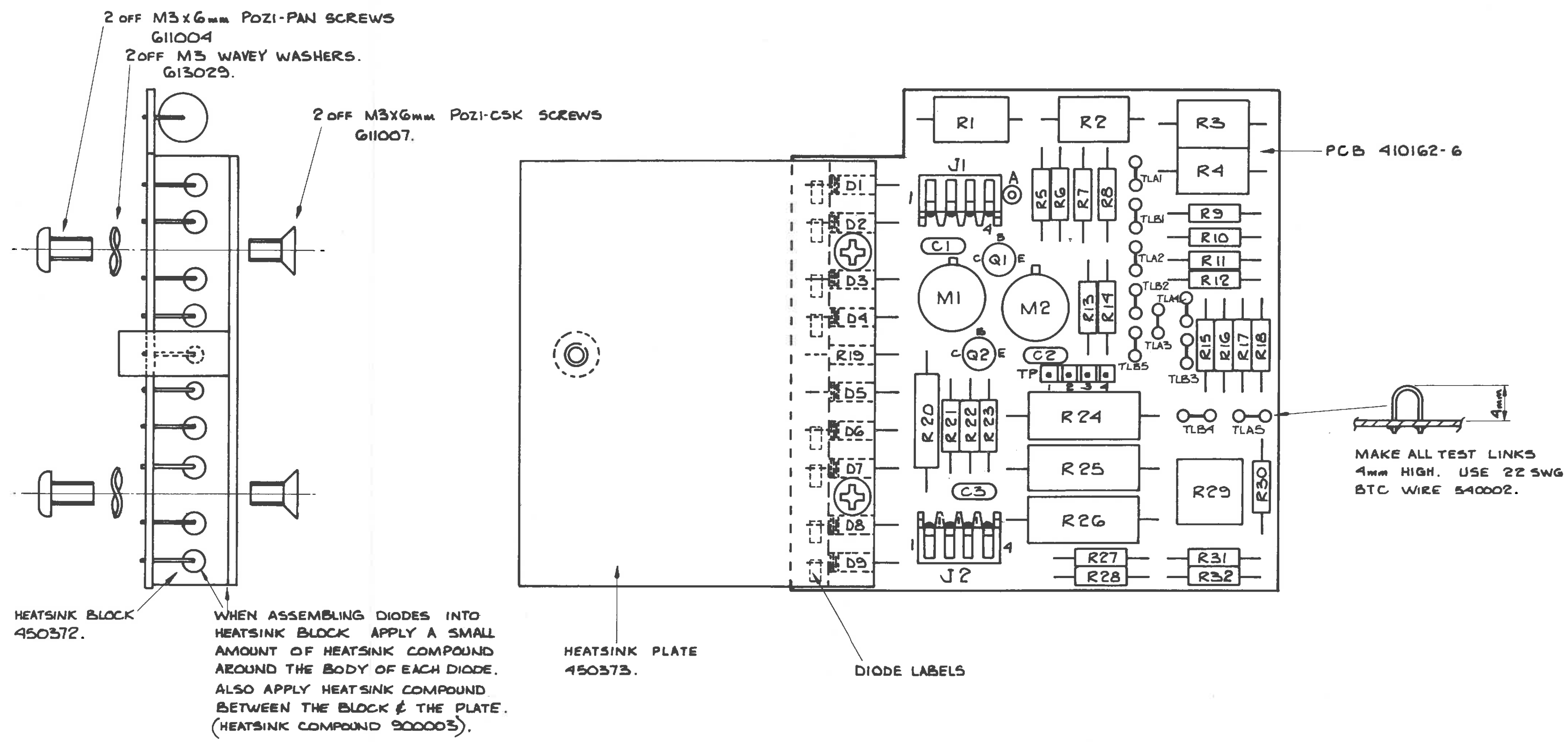
ISS.	CHANGES
4	ECO 1445. BJ ISS-6 PCB. RE-DRAWN. 14-2-83
5	ECO 1492 ATT'N SET 090099 WAS ISSUE 2 IL 7.6.83

NOTES

ZENER DIODE KIT 219015 FITTING INSTRUCTIONS.

CARE MUST BE TAKEN THAT EACH DIODE IS FITTED TO ITS CORRECT POSITION ON THE BLOCK. DO NOT REMOVE DIODE SERIAL Nº LABELS. FIT DIODES TO THE CORRECT POSITION AS INDICATED ON THE RECORD SHEET. IF ANY COMPONENT IS LOST OR DAMAGED REFER TO QA.

1. FIT CONTENTS OF BAG 'A' TO D2, D4, D7, D9 & R3.
2. FIT CONTENTS OF BAG 'B' TO D1, D3, D6, D8 & R4.
3. FILL IN REFERENCE RECORD SHEET :-
   - (I). ASSEMBLY SERIAL No.
   - (II). ASSEMBLY ISSUE NO.
   - (III). ASSEMBLY DATE.
4. CUT TEST LINKS INDICATED ON THE RECORD SHEET.
5. THE RECORD SHEET MUST ACCOMPANY THE FINISHED ASSEMBLY.



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DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400452 (A)	TITLE	DRAWING No.
B. JACKSON	15th FEB 83		DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°		CIRCUIT DIAGRAM	430452 (A)	4000. REFERENCE PCB ASSEMBLY. 4000A	400452 400452A
CHECKED	DATE 21.2.83	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH	CHECK PROCEDURE	460452 (A)		
APPR.	DATE	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST	470452 (A)		SHEET 1 OF 5

4951MT

DRAWING No. 430452

FIRST USED ON 4000

THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

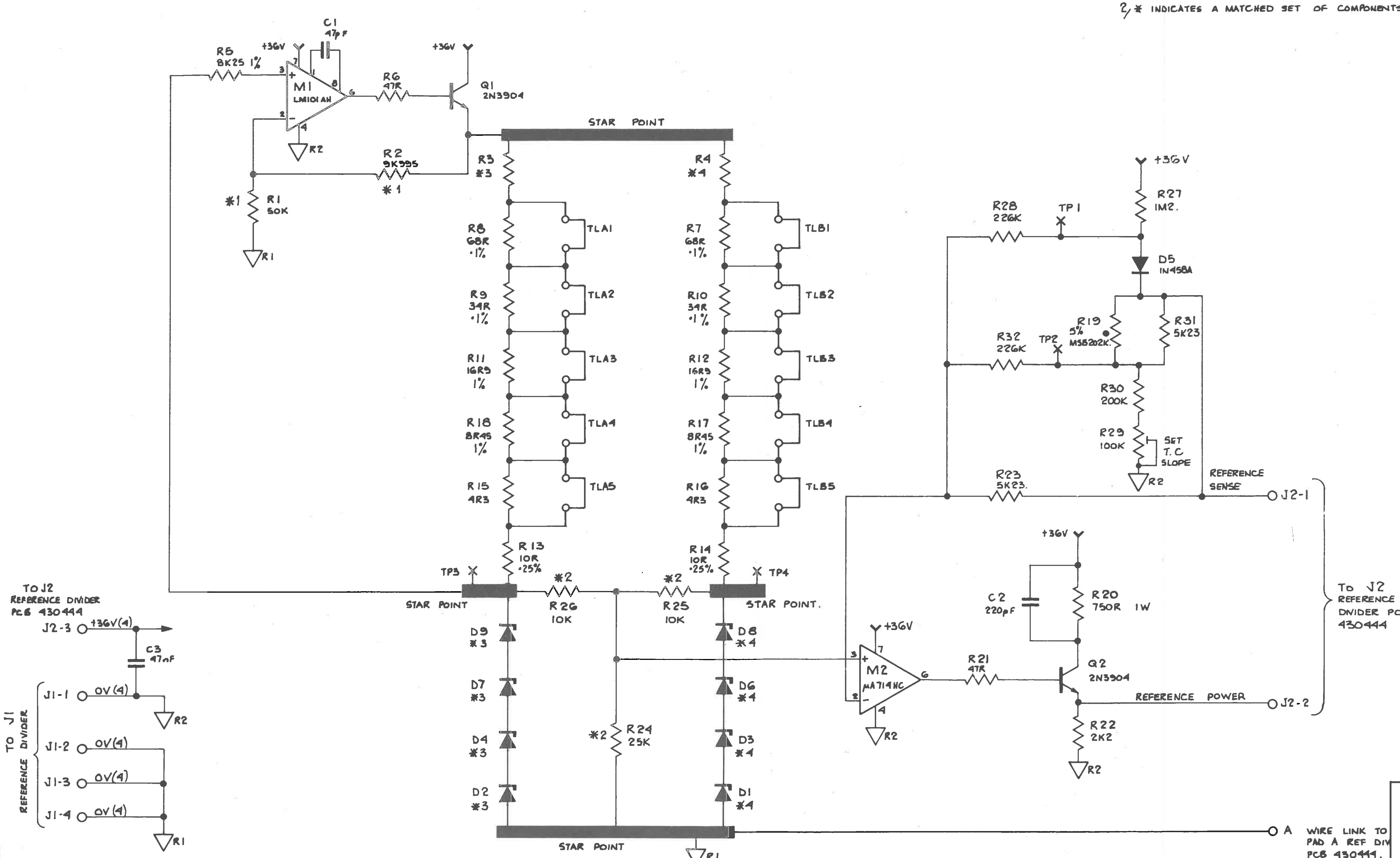
ALL BURRS TO BE REMOVED

ISS.	CHANGES
1	RELEASED BJ 22-MAR 82.
2	ECO 1445 BJ PCB ISSUE-G R23 WAS 5K1 R19, R27, R28, R29, R30, R31, R32 & D5. ADDED. 15-2-83 DESIGNATORS CHANGED FOR NEW PCB.

NOTES

1/ R3 & R4 ARE SELECTED WITH THEIR DIODE SETS. PART OF KIT 219015. VALUES ARE :- 475, 611, 747 & 883 Ω SEE DRAWING Nº 219015.

2/ * INDICATES A MATCHED SET OF COMPONENTS.



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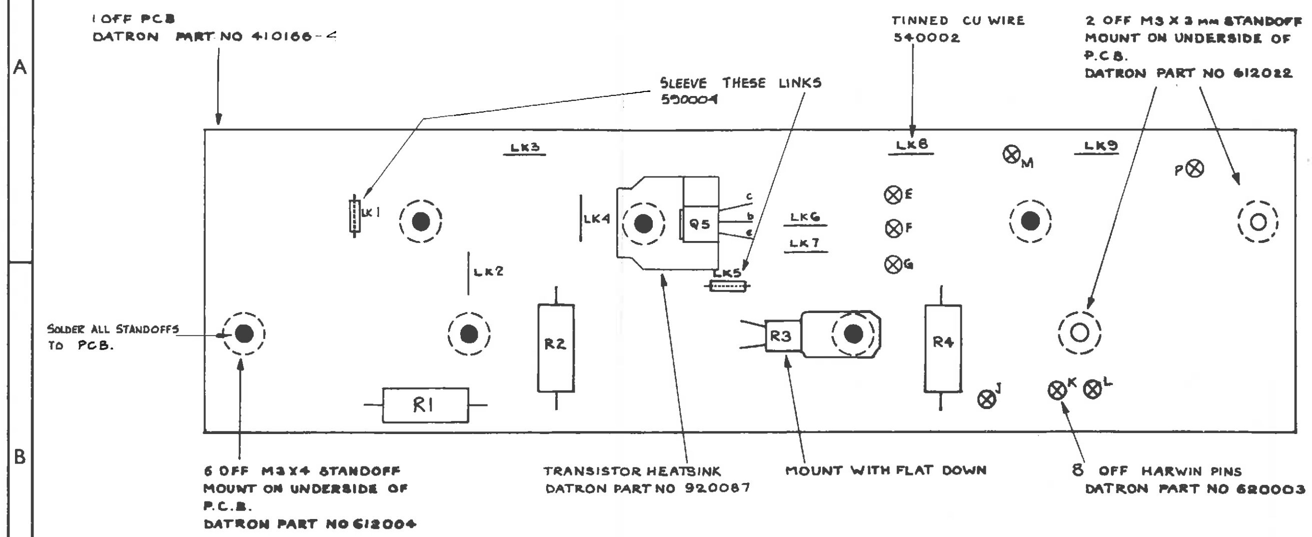
DRAWN B.JACKSON	DATE 19th MAR 82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400452	TITLE 4000 REFERENCE PCB	DRAWING No. 430452
CHECKED R.K.COGGAN	DATE 23rd MAR 82	SCALE		FINISH	CIRCUIT DIAGRAM 430452		
APPR. B Hume	DATE 24th MAR 82	NOT TO BE SCALED	UNLESS OTHERWISE STATED THIRD ANGLE PROJECTION		CHECK PROCEDURE 460452 CHECK LIST 470452		SHEET 1 OF 1

4951MT

ISS.	CHANGES
C	13-8-81
1	RELEASED 19-APR 82

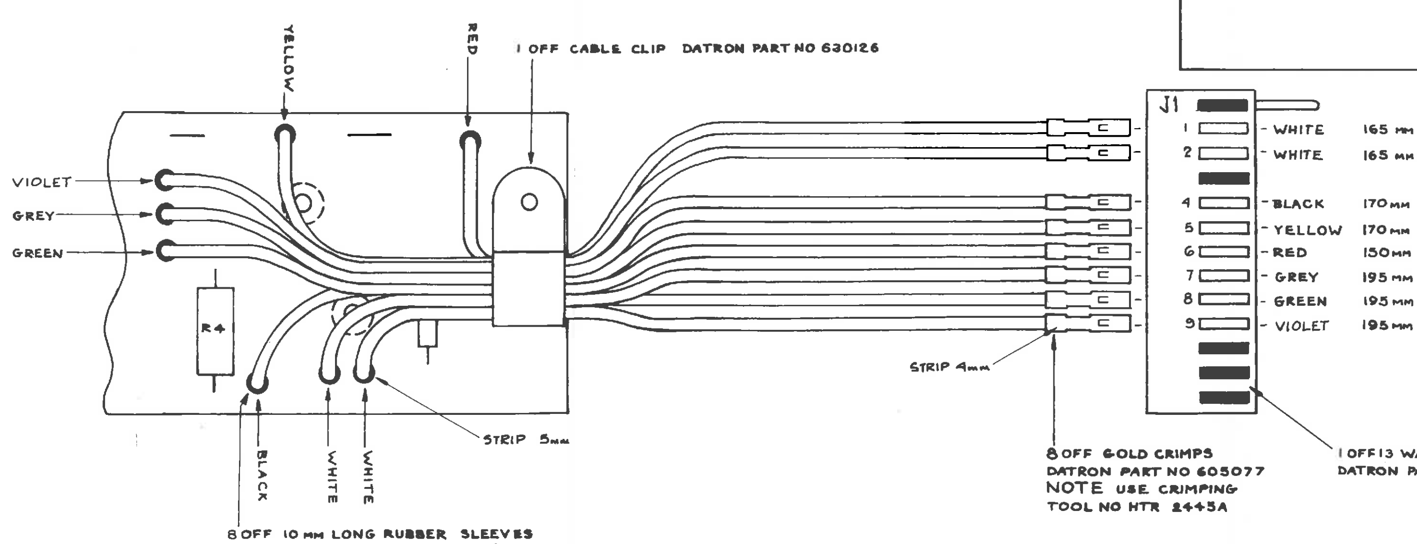
DRAWING No. 400454



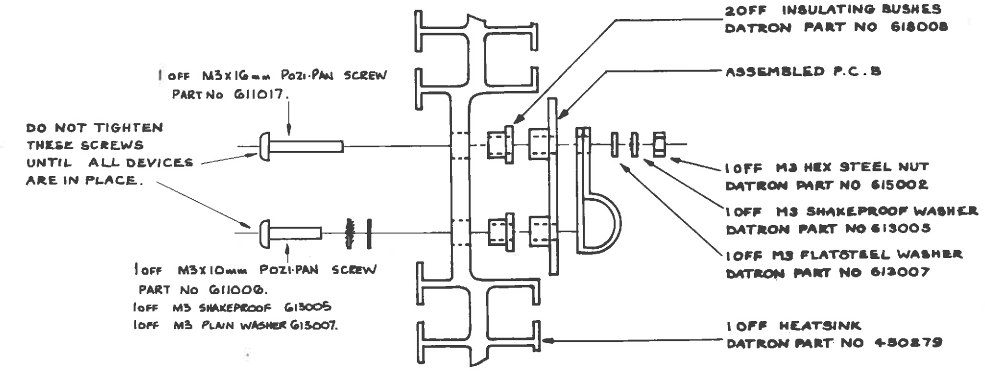
PROCEDURE

1) ASSEMBLE BOARD
ALIGN THE HOLES IN R3 & Q5 HEATSINK, WITH THE STANDOFFS.

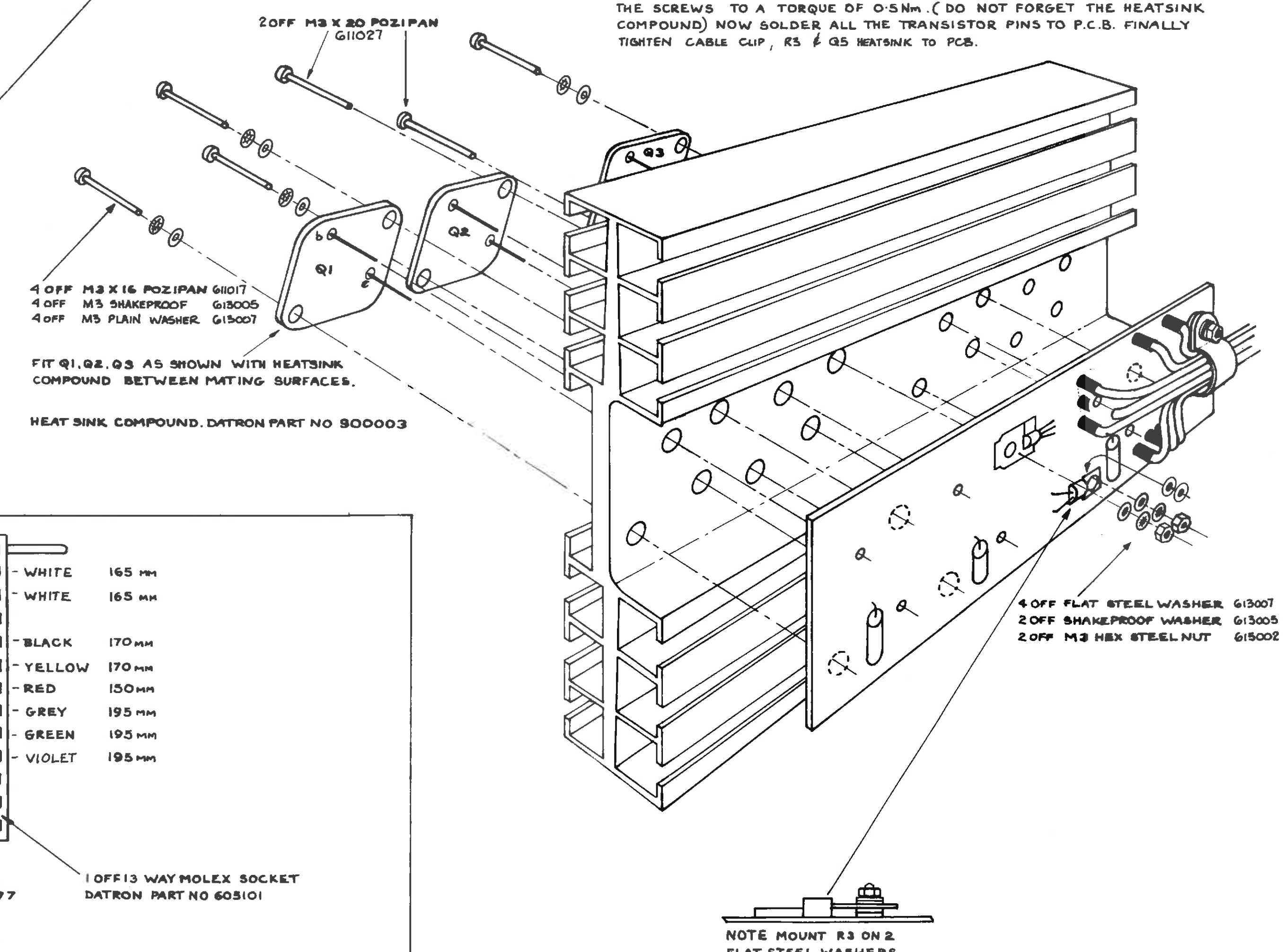
2) WIRE CABLE AS SHOWN



3) PLACE PCB IN RECESS OF HEATSINK WITH CUT AWAY FLANGES. WITH BOARD FACING AS IN PROCEDURE 1). START AT RIGHTHAND END AND FIT 2 OFF SCREWS AS SHOWN BELOW.



4) NOW THAT THE PCB IS HELD IN POSITION INSERT TRANSISTORS Q1, Q2 & Q3 AS SHOWN, THEN USING A TORQUE SCREW DRIVER, TIGHTEN THE SCREWS TO A TORQUE OF 0.5Nm. (DO NOT FORGET THE HEATSINK COMPOUND) NOW SOLDER ALL THE TRANSISTOR PINS TO P.C.B. FINALLY TIGHTEN CABLE CLIP, R3 & Q5 HEATSINK TO PCB.



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ELECTRONICS
LIMITED
NORWICH

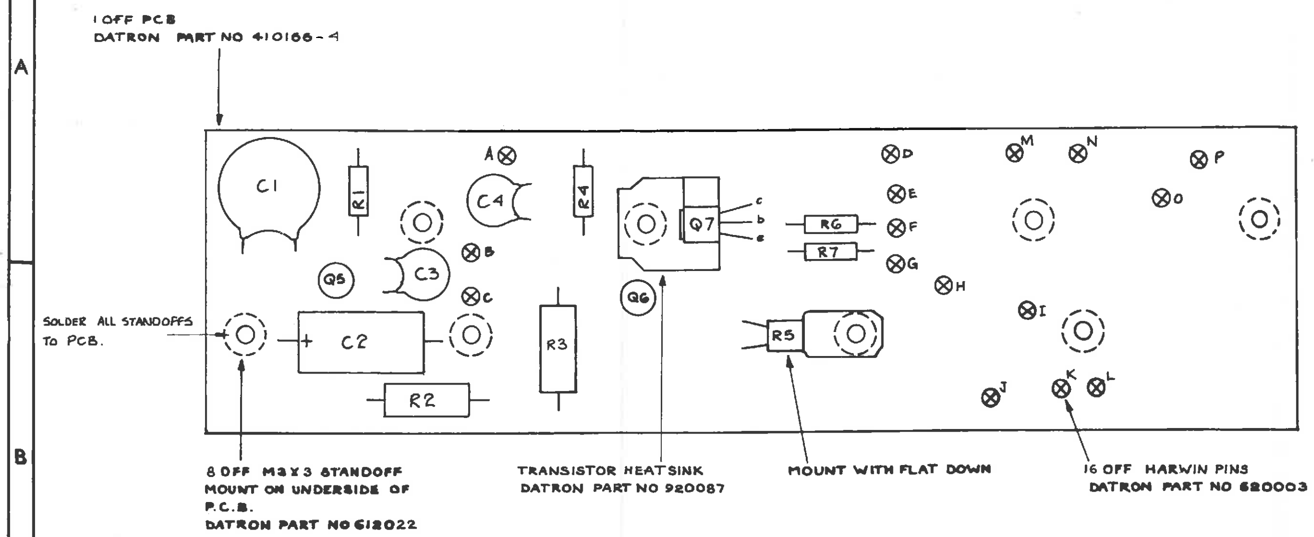
DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	TITLE	DRAWING No.
JK	7-7-81		DECIMAL TO 2 PLACES ± ·1mm DECIMAL TO 1 PLACE ± ·2mm WHOLE DIMENSIONS ± ·4mm ANGULAR ± ½°		400454	4000 POWER AMPLIFIER POSITIVE HEATSINK ASSY	400454
CHECKED MJD	DATE 23.4.82	SCALE		FINISH	CIRCUIT DIAGRAM 430449		
					CHECK PROCEDURE 460454		
APPR. B Hume	DATE 29.4.82	NOT TO BE SCALED	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION		CHECK LIST 470454		SHEET 1 OF 3

DRAWING No. 400455

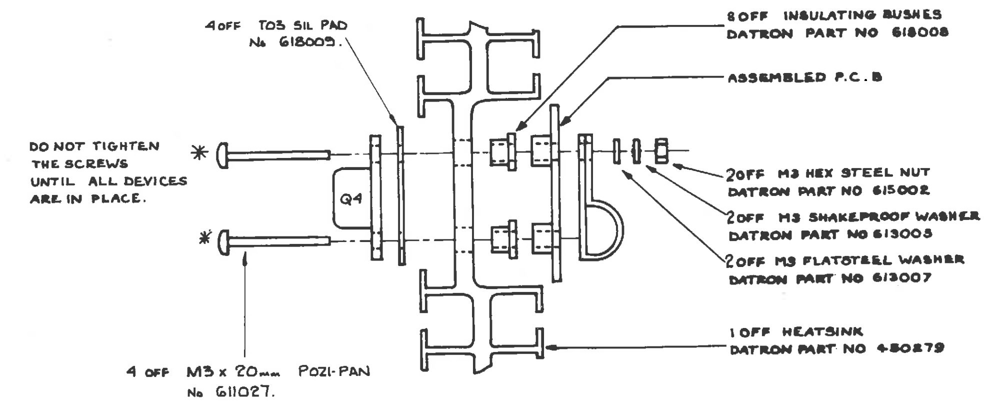
ISS.	CHANGES
C	13-8-81
1	RELEASED 19th APR. 82

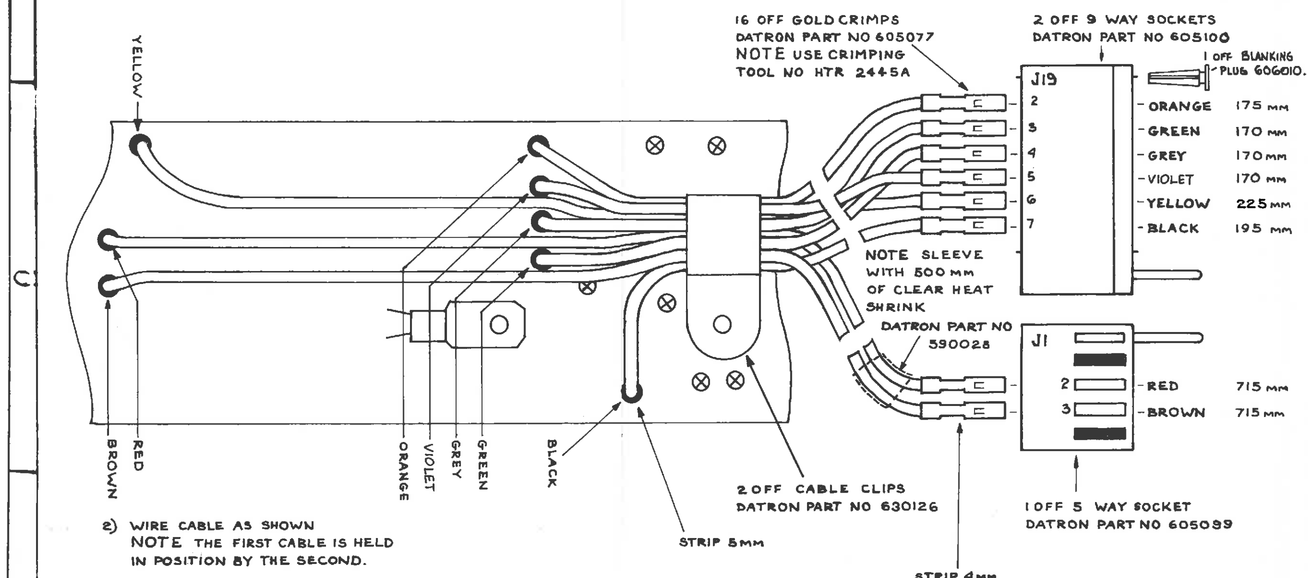
PROCEDURE

1) ASSEMBLE BOARD
ALIGN THE HOLES IN R5 AND Q7 HEATSINK WITH THE STANDOFFS CENTRES.

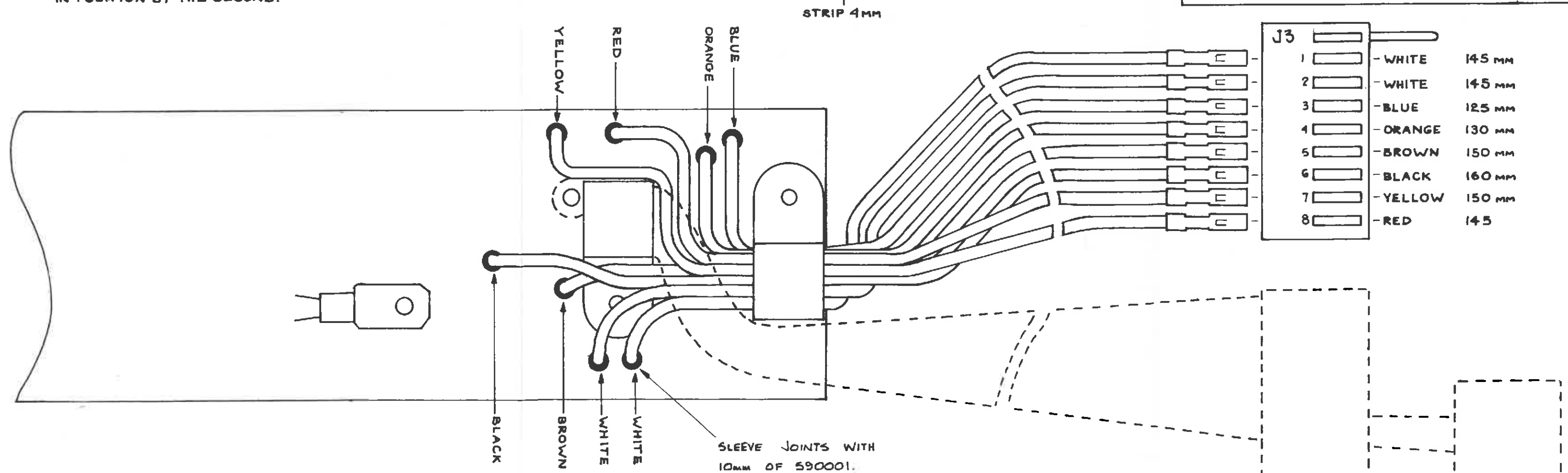


3) POSITION ALL INSULATING BUSHES IN RESPECTIVE HOLES IN HEATSINK. THEN PLACE PCB IN RECESS OF HEATSINK WITH CUT AWAY FLANGES. WITH BOARD FACING AS PROCEDURE 1). START AT RIGHTHAND END AND FIT Q4 TO REVERSE SIDE OF HEATSINK WITH SIL PAD AS SHOWN.
DON'T SOLDER Q4 IN PLACE YET.

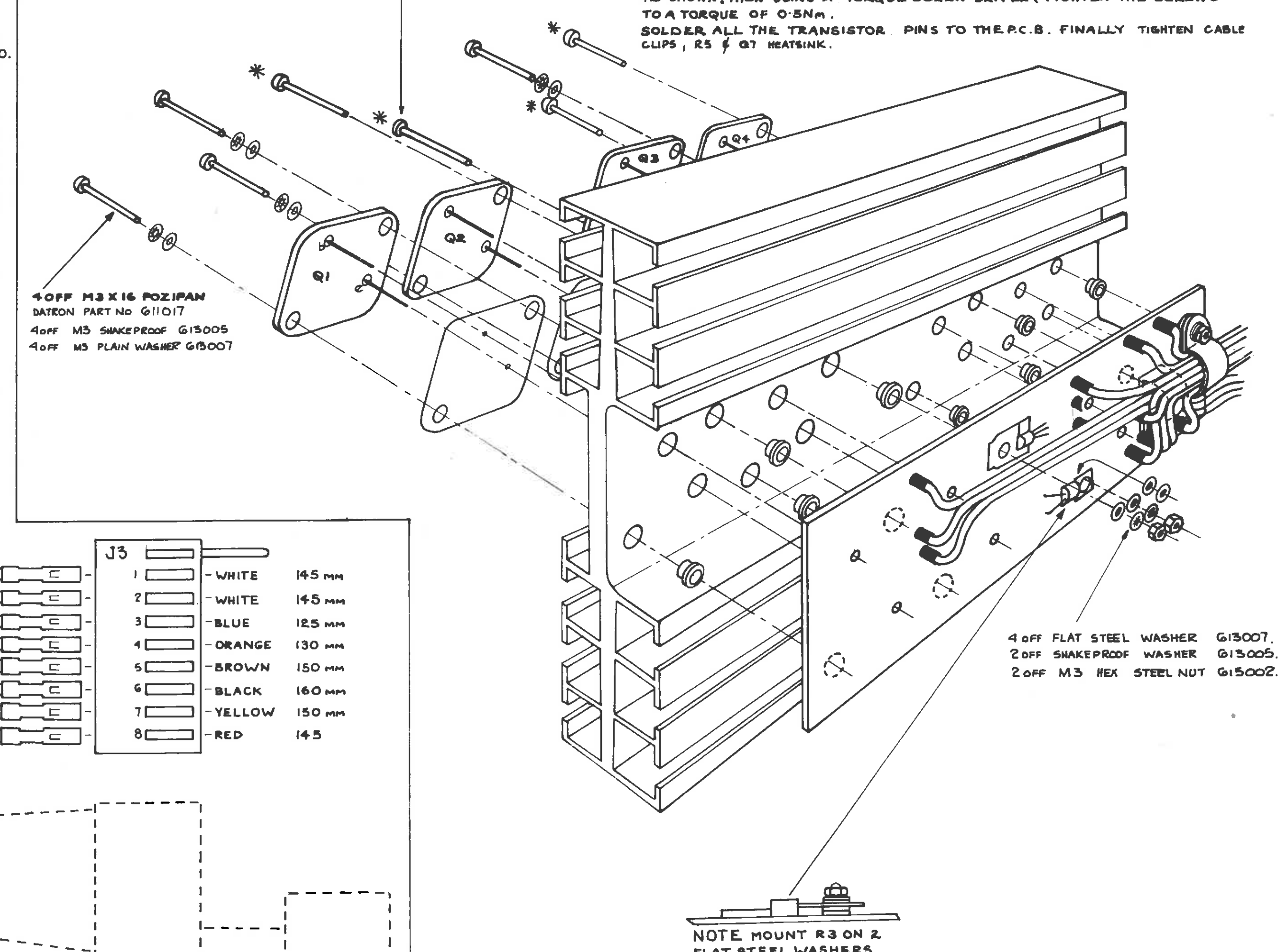




2) WIRE CABLE AS SHOWN
NOTE THE FIRST CABLE IS HELD IN POSITION BY THE SECOND.



4) WITH Q4 HOLDING THE BOARD IN POSITION, INSERT THE OTHER TRANSISTORS AS SHOWN, THEN USING A TORQUE SCREW DRIVER, TIGHTEN THE SCREWS TO A TORQUE OF 0·5Nm.
SOLDER ALL THE TRANSISTOR PINS TO THE P.C.B. FINALLY TIGHTEN CABLE CLIPS, R5 & Q7 HEATSINK.



DRAWN	DATE 7-7-81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400455	TITLE 4000 POWER SUPPLY/ CURRENT HEATSINK ASSY
CHECKED	DATE 23.4.82.	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430449. 430448.	
APPR.	DATE 29.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460455	
					CHECK LIST 470455	

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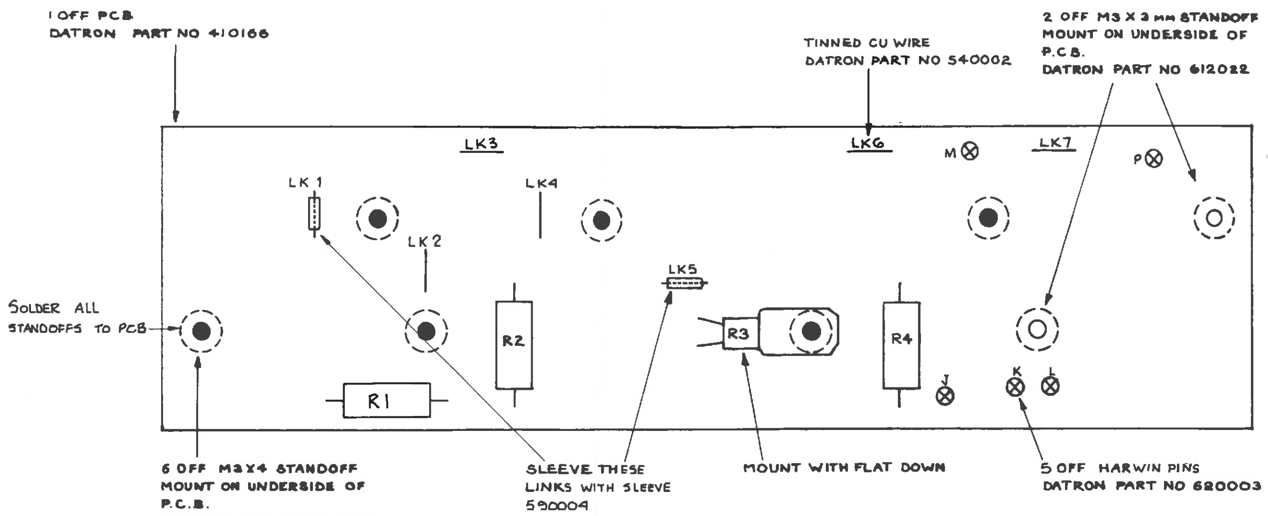
DRAWING No. 400455

SHEET 1 OF 4

ISS.	CHANGES
C	7-7-81
1	RELEASED 19-APR-82

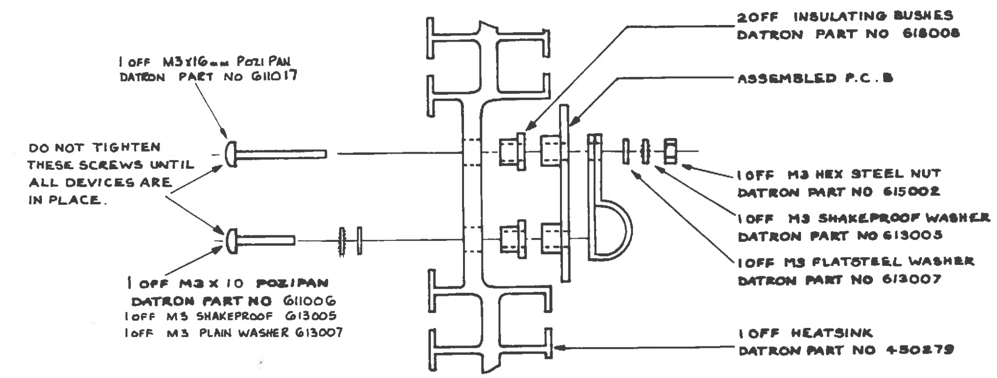
DRAWING No. 400461



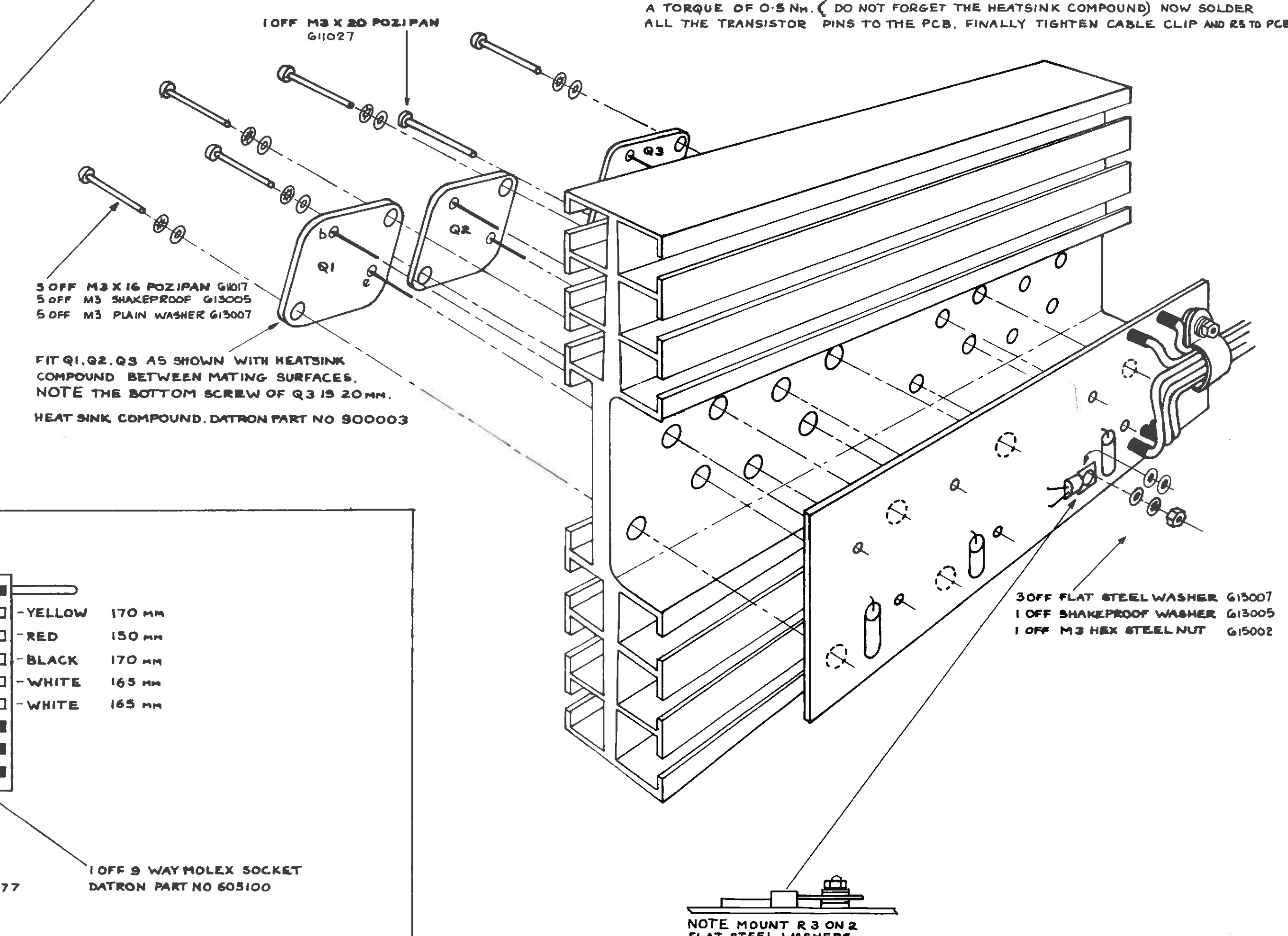
PROCEDURE

1) ASSEMBLE BOARD
ALIGN THE HOLE IN R3 WITH THE STANDOFF

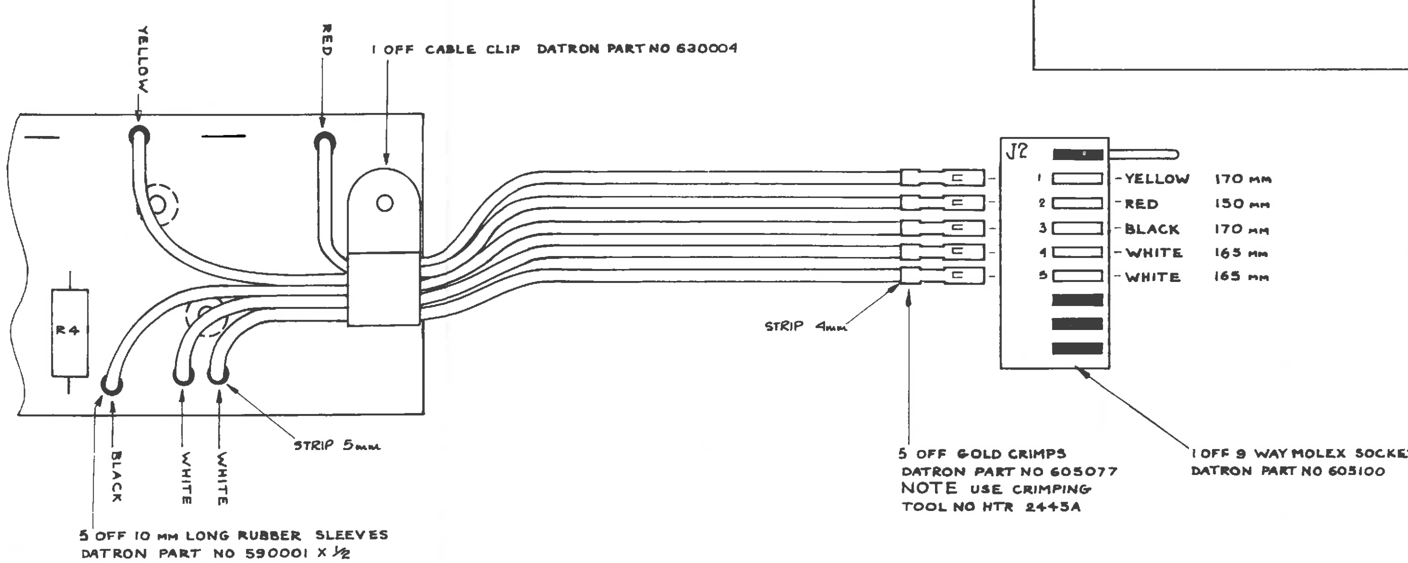
3) PLACE PCB IN RECESS OF HEATSINK WITH CUT AWAY FLANGES. WITH BOARD FACING AS IN PROCEDURE 1). START AT RIGHTHAND END AND FIT 2 OFF SCREWS AS SHOWN BELOW.



4) NOW THAT THE PCB IS HELD IN POSITION INSERT TRANSISTOR Q1 Q2 & Q3 AS SHOWN, THEN USING A TORQUE SCREW DRIVER TIGHTEN THE SCREWS TO A TORQUE OF 0.5 Nm. (DO NOT FORGET THE HEATSINK COMPOUND) NOW SOLDER ALL THE TRANSISTOR PINS TO THE PCB. FINALLY TIGHTEN CABLE CLIP AND R3 TO PCB.



2) WIRE CABLE AS SHOWN



DRAWN	DATE 7-7-81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400461	TITLE: 4000 POWER AMPLIFIER NEGATIVE HEATSINK ASSY
CHECKED	DATE 23.4.82	SCALE		FINISH	CIRCUIT DIAGRAM 430449	
APPR.	DATE 29.4.82	NOT TO BE SCALED	UNLESS OTHERWISE STATED; FIRST ANGLE PROJECTION		CHECK PROCEDURE 460461; CHECK LIST 470461	

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DRAWING No. 400461

SHEET 1 OF 3

DRAWING No. 400470

ISS.	CHANGES
1	RELEASED 17.3.82
2	ECO 1314, 1324 C1 DELETED R5 AND R6 CHANGE VALUE. R20, C8 AND C10 ADDED. JR 14.5.82
3	ECO 1447. BJ TP8 & TP9 ADDED. 14th FEB 83.
4	ECO 1468. D5 MOUNTED ON CERAMIC BEADS. BJ. 8-4-83. ECO 1476. C9 VALUE CHANGE WAS 110013.
5	ECO 1504 R13 WAS CR25. JR 12-8-83.
6	ECO 1529 D1 AND D2 WERE 200010. PCB WAS ISSUE 3. JR 15.9.83

BED C5 & C7 ON P.C.B WITH SILICONE RUBBER COMPOUND 900004.

LINKS TO BE MADE FROM TINNED COPPER WIRE SLEEVED WITH P.T.F.E SLEEVING 580004

2 OFF 4 WAY ·156" LOCKING RAMP 604042 MOUNT ON UNDERSIDE.

2 OFF 2 X TO220 HEATSINKS 920090
2 OFF M3 X 6mm POZIPAN SCREW 611004
2 OFF M3 X 10mm POZIPAN SCREW 611006
4 OFF M3 SHAKEPROOF WASHER 613005
4 OFF M3 HEX NUT 615002
2 OFF M3 FLAT STEEL WASHER 613007
USE M3 X 10mm ON Q3 AND Q4 WITH A FLAT AND SHAKEPROOF WASHER UNDER NUT

TEST POINTS TO BE MADE FROM 22 SWG TINNED COPPER WIRE 540002 (TP5 & TP6).

TEST POINT TERMINAL 620007 7 OFF.

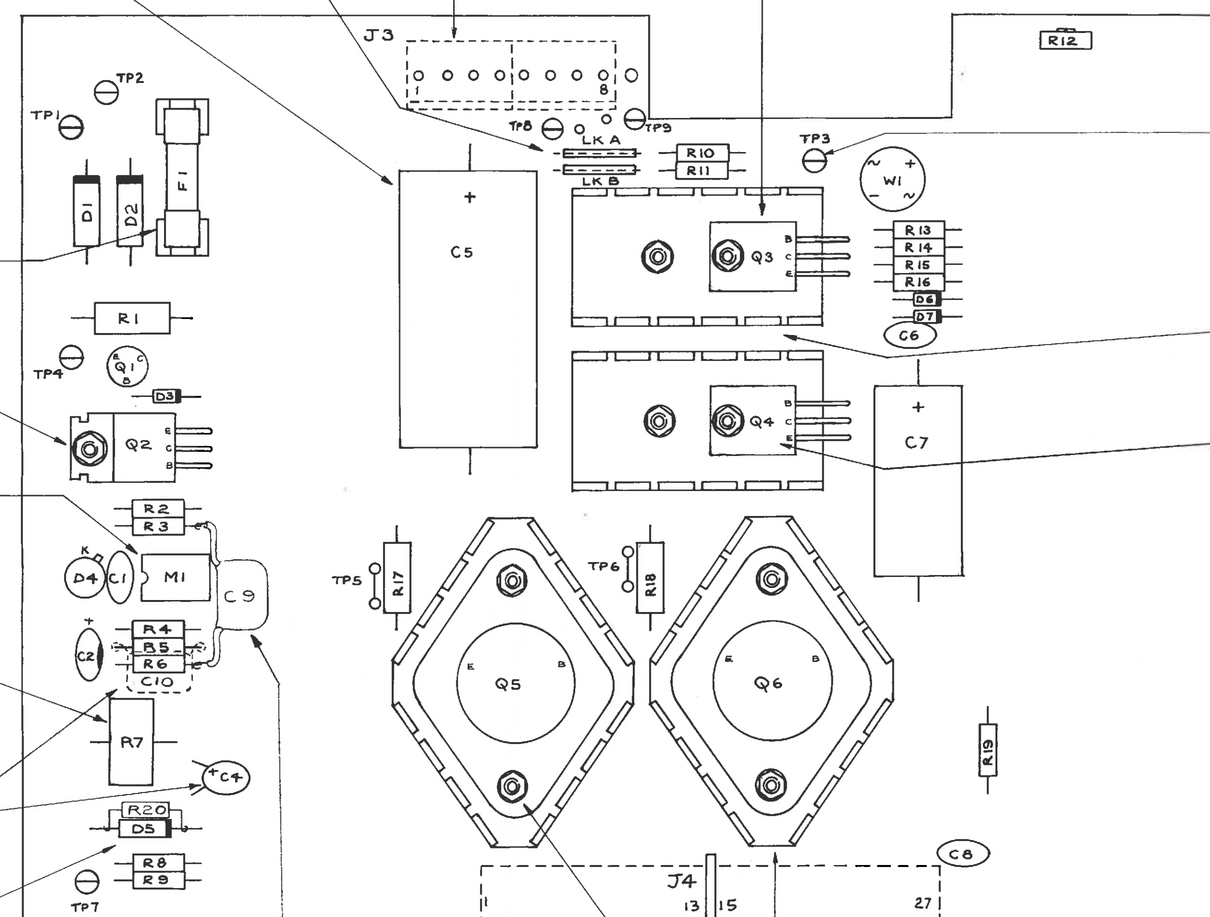
1 OFF 4A FUSE 20mm 920128
1 OFF P.C.B MT FUSE HOLDER 920126

ENSURE THAT THERE IS A GAP OF AT LEAST 5mm BETWEEN HEATSINKS.

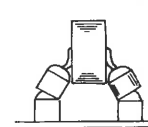
1 OFF M3 X 6mm POZIPAN SCREW 611004
1 OFF M3 SHAKEPROOF WASHER 613005
1 OFF M3 HEX NUT 615002

FIT Q3 AND Q4 WITH GOLD SIDE TO HEATSINK

1 OFF 8 WAY DIL SOCKET 605059

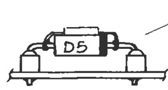


MOUNT R7 ON STEATITE BEADS 630024 4 OFF



MOUNT C4 FLAT TO THE P.C.B AS SHOWN.

MOUNT C10 ON THE BACK OF THE PCB ACROSS R5, BED IN SILICONE RUBBER (900004)



MOUNT D5 ON STEATITE BEADS 630024 2 OFF.

PCB 410179-3A

SLEEVE LEADS OF C9 (590004) AND BED IN SILICONE RUBBER (900004)

NOTE USE HEATSINK COMPOUND BETWEEN MATING SURACES OF Q3,4,5 & 6 AND THE HEATSINKS, THEN USING A TORQUE SCREW DRIVER TIGHTEN TO TORQUE OF 0·5 Nm. (HEATSINK COMPOUND 920003)

2 OFF TO3 HEATSINK 920088
4 OFF M3 X 10mm POZIPAN SCREW 611006
4 OFF M3 SHAKEPROOF WASHER 613005
4 OFF M3 HEX NUT 615002
1 OFF M3 FLAT STEEL WASHER 613007
USE FLAT STEEL WASHER UNDER SCREW HEAD ON BACK OF PCB.

DRAWN	DATE	DIMENSIONS IN MILLIMETRES	TOLERANCES	MATERIAL	ASSY DRG & PARTS LIST	400470	TITLE
JR	13-11-81		DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	—	CIRCUIT DIAGRAM	430470	4000 OUT GUARD POWER SUPPLY ASSY
CHECKED MJD	DATE 18.3.82	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH —	CHECK PROCEDURE	460470	
APPR. B. Hare	DATE 22.3.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK LIST	470470	

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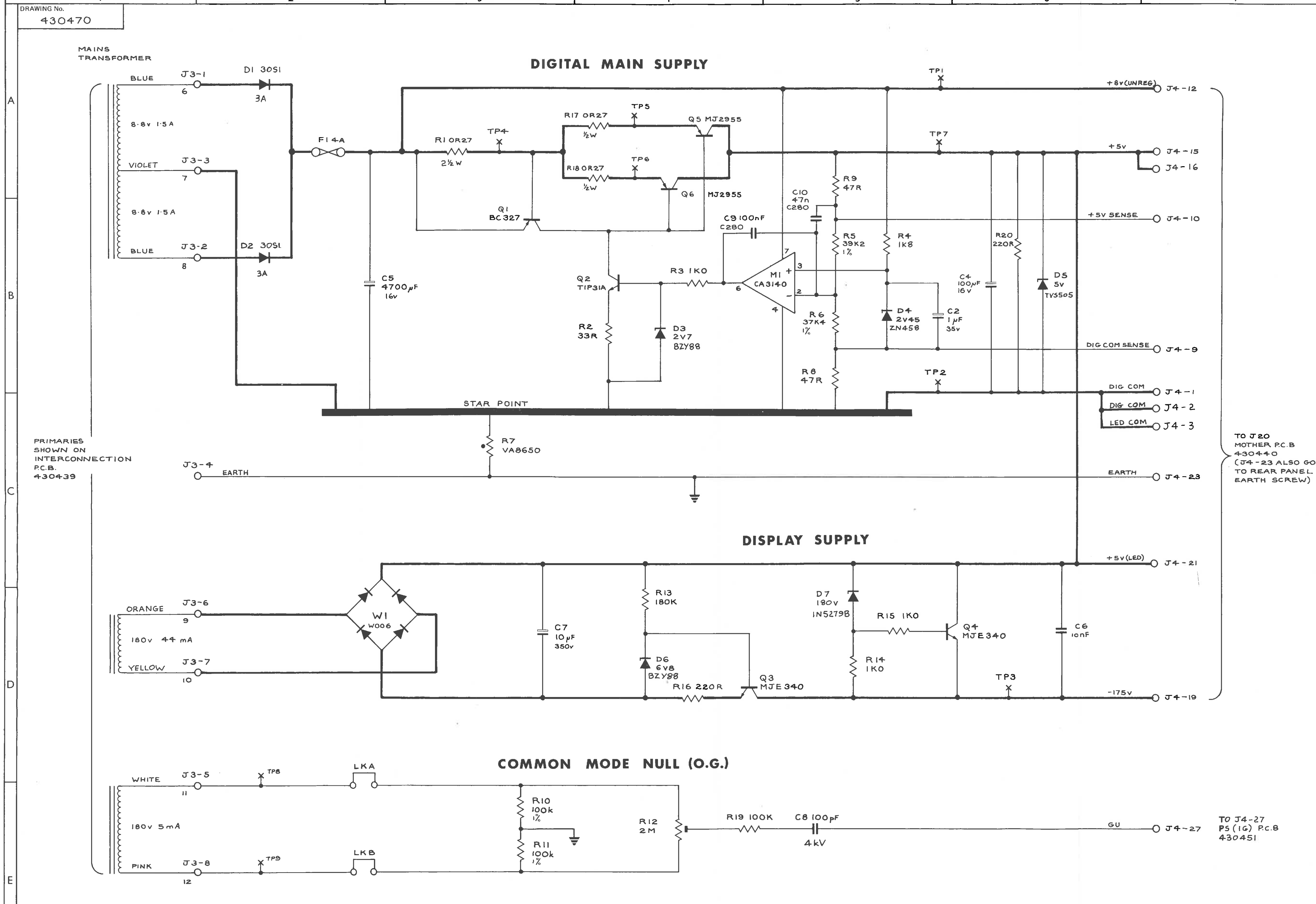
DRAWING No. 400470

SHEET 1 OF 5

DRAWING No. 430470

ISS.	CHANGES
1	RELEASED 17.3.82
2	ECO 1314, 1324 C1 DELETED R5 WAS 1K24 R6 WAS 1K18 R20, C9 AND C10 ADDED. JR 14.5.82
3	ECO 1447. 14-3-83. TP8 & TP9 ADDED.



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DRAWN	DATE 7·12·81	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ±·1mm DECIMAL TO 1 PLACE ±·2mm WHOLE DIMENSIONS ±·4mm ANGULAR ±½°	MATERIAL —	ASSY DRG & PARTS LIST 400470	TITLE 4000 POWER SUPPLY OUT GUARD	DRAWING No. 430470
CHECKED R.K. COGGAN	DATE 18-3-82	SCALE —		FINISH —	CIRCUIT DIAGRAM 430470		
APPR. B. Thomas	DATE 22.3.82	NOT TO BE SCALED	UNLESS OTHERWISE STATED FIRST ANGLE PROJECTION		CHECK PROCEDURE 460470		
					CHECK LIST 470470		SHEET 1 OF 1

DATRON INSTRUMENT FAILURE REPORT

(This form must accompany all warranty claims.)

Date.................................

Submitted by (Name)...

Name of Company...

Address...

....

Datron Instrument Model No. ....

Datron Instrument Serial No. ....

Date of purchase (if known)..

Customer Order Number...

Datron Sales/Service Center...

Symptoms of Failure

Please describe the symptoms of failure, including any relevant diagrams (use a separate sheet if necessary).

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TERMS AND CONDITIONS OF SALE

1. GENERAL
The acceptance of a quotation, of any goods supplied, advice given or service rendered includes the acceptance of the following terms and conditions and no variation of or addition to the same shall be binding upon us unless expressly agreed in writing by us. Any order shall be subject to our written acceptance.

2. QUOTATION
Unless previously withdrawn our quotation is open to acceptance in writing within the period stated or where no period is stated within thirty (30) days after its date. We reserve the right to correct any errors or omissions in our quotation. Unless otherwise stated all quotations are firm and fixed. The prices quoted are based on manufacture of the quantity and type ordered and are subject to revision when interruptions, engineering changes or changes in quantity are caused or requested by the customer.

3. LIABILITY FOR DELAY
Any delivery times quoted are from the date of our written acceptance of any order and on receipt of all information and drawings to enable us to put the work in hand. Where delivery is to take place by instalments each such instalment shall constitute a separate contract. We will use our best endeavours to complete delivery of the goods or services in the period stated but accept no liability in damages or otherwise for failure to do so for any cause whatsoever. In all cases of delay the delivery time shall be extended by reasonable period having regard to the cause of delay.

4. PAYMENT
Payment shall be made net cash within thirty (30) days of delivery or in accordance with the payment terms set out in the quotation. Unless specifically stated to the contrary payment shall be in pounds sterling. In the event of any payment to us being overdue we may without prejudice to any other right suspend delivery to you or terminate the contract and/or charge you simple interest on overdue amounts at the rate of 2.5% above the ruling Bank of England Minimum Lending Rate. No payment to us shall in any circumstance be offset against any sum owing by us to you whether in respect of the present transaction or otherwise.

5. INSPECTION & TEST
All goods are fully inspected at our works and where practicable subjected to our standard tests before despatch. If tests are required to be witnessed by your representative notice of this must be given at the time of placing the order and notice of readiness will then be given to you seven (7) days in advance of such tests being carried out. In the event of of any delay on your part in attending such tests or in carrying out inspection by you after seven (7) days notice of readiness the tests will proceed in your absence and shall be deemed to have been made in your presence and the inspection deemed to have benn made by you. In any event you shall be required promptly after witnessing a test or receiving test results of witnessed or unwitnessed tests to notify us in writing of any claimed defects in the goods or of any respect in which it is claimed that the goods do not conform with the contract. Before you become entitled to reject any goods we are to be given reasonable time and opportunity to rectify them. You assume the responsibility that the goods stipulated by you are sufficient and suitable for your purpose and take all steps to ensure that the goods will be safe and without risk to health when properly used. Any additional certification demanded may incur extra cost for which a special quotation will be issued.

6. DELIVERY AND PACKING
All shipments are, unless otherwise specifically provided, Ex-works which is the address given on the invoice. An additional charge will be made for carriage and insurance as necessary with the provision that all shipments shall be insured and this insurance expense shall be paid by the purchaser. Where special domestic or export packing is specified a charge will be made to cover the extra expense involved.

7. DAMAGE IN TRANSIT
Claims for damage in transit or loss in delivery of the goods will only be considered if the carriers and ourselves receive notice of such damage within seven (7) days of delivery or in the event of loss of goods in transit within fourteen (14) days of consignment.

8. TRANSFER OF PROPERTY & RISK
Title and property of the goods shall pass when full payment has been received of all sums due to us whether in respect of the present transaction or not. The risk in the goods shall be deemed to have passed on delivery.

9. WARRANTY
We agree to correct, either by repair, or at our election, by replacement, any defects of material or workmanship which develop within the warranty period specified in the sales literature or quotation after delivery to the original purchaser. All items claimed defective must be promptly returned to us carriage paid unless otherwise arranged and will be returned to you free of charge. Unless otherwise agreed no warranty is made concerning components or accessories not manufactured by us. We will be released from all obligations under warranty in the event of repairs or modifications made by persons other than our own authorised service personnel unless such repairs are made with our prior written consent.

10. PATENTS
We will indemnify you against any claim of infringement of Letters Patent, Registered Design, Trade Mark or Copyright (published at the date of the contract) by the use or sale of any goods supplied or service rendered by us to you and against all costs and damages which you may incur and for which you may become liable in any action for such infringement. Provided always that this indemnity shall not apply to any infringement which is due to our having followed a design or instruction furnished or given by you or to the use of such goods or service in association or combination with any other article, material or service not supplied by us. This indemnity is conditional on your giving to us the earliest possible notice in writing of any claim being made or action threatened or brought against you and on your permitting us at our own expense to conduct litigation that may ensue and all negotiations for a settlement of the claim or action. You on your part warrant that any design or instruction furnished or given by you shall not cause us toinfringe any Letter Patent, Registered Design, Trade Mark or Copyright in the execution of your order.

11. DOCUMENTATION
All drawings, plans, designs, software specifications, manuals and technical documents and information supplied by us for your use or information shall remain at all times our exclusive property and must not be copied, reproduced, transmitted or communicated to a third party without our prior written consent.

12. FRUSTRATION
If any contract or any part of it shall become impossible of performance or otherwise frustrated we shall be entitled to a fair and reasonable proportion of the price in respect of the work done up to the date thereof. For this purpose any monies previously paid by you shall be retained against the sum due to us under this provision. We may dispose of the goods as we think fit due allowance being made to you for the net proceeds thereof.

13. BANKRUPTCY
If the purchaser shall become bancrupt or insolvent, or being a Limited Company commence to be wound up or suffer a Receiver to be appointed, we shall be at liberty to treat the contract as terminated and be relieved of further obligations. This shall be without prejudice to our right to claim for damages for breach of contract.

14. LEGAL INTERPRETATION
Any contract will be deemed to be made in England and shall be governed and construed for all purposes and in all respects in accordance with English Law and only the Courts of England shall have jurisdiction.

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SALES AND SERVICE REPRESENTATIVES WORLDWIDE

COUNTRY	AND REPRESENTATIVE	Telephone	Telex
AUSTRALIA	**Scientific Devices (Australia) Pty. Ltd.,** 2 Jacks Road, South Oakleigh, Victoria 3167	(579)3622	32742
AUSTRIA	**Kontron GmbH & Co, Electronics Department** Eisgrubengasse 2, A-2334 Voesendorf B. Wien	(222)692531	131699
BELGIUM	**Air-Parts International B.V.** Avenue Huart-Hamoir 1-Box 19, 1030 Brussels	0103222416460	25146
BRAZIL	**Comercial Goncalves** Rua Deocleciana, 77, Ponte Pequena Sao Paulo SP, Cep 01106	(11)2294044	22104
CHINA	**Tianjin First Radio Factory** No. 5 Zhao Jia Chang Street, Hong Qiao Section, Tianjin	Tianjin 251941	-
DENMARK	**Instrutek A/S,** Head Office: Christiansholmsgade DK-8700 Horsens	(5)611100	61656
EASTERN EUROPE	**Amtest Associates Ltd.,** Amtest Hse, 75-79 Guilford St, Chertsey, Surrey KT16 9AS, England	0932568355	928855
EGYPT & MIDDLE EAST	**EPIC** 20 Ashmoun St, PO Box 2682, Horria, Heliopolis	(2)661767	23315
FINLAND	T.B.A.	-	-
FRANCE	**JOD Instrumentation** 37-41 rue des Artisans, 78760 Jouars Pontchartrain, Paris	(1)34891174	698485
GERMANY	**Wavetek Electronics GmbH** Hans-Pinsel Strasse 9-10, 8013 Haar b. Munchen, W.Germany	(89)461090	5212996
GREECE	**American Technical Enterprises** PO Box 156, 48 Patission Street, Athens 147	(1)8219470	216046
HONG KONG	**Eurotherm (Far East) Ltd.,** 21/F Kai Tak Commercial Building, 317-321 Des Voeux Road, Central, Hong Kong	(5)411268	72449
INDIA	**Technical Trade Links** 42, Navketan Estate, Mahakali Caves Road, Andheri (East), Post Box No. 9447, Bombay 400 093	(22)4133341	1171071
INDONESIA	**PT & PD Bah Bolon Trading Co.,** D1/Arena Pekan Raya Jakarta. P. O. Box 2157, Jakarta 10000	(21)377008	46164
IRELAND	**Euro Instruments & Electronics** Euro House, Swords Road, Santry, Dublin 9	01-425-000	318121
ISRAEL	**Racom Electronics Co. Ltd.,** 7 Kehilat Saloniki St., P. O. Box 21120, Tel-Aviv 61210	(3)491922	33808

COUNTRY AND REPRESENTATIVE		Telephone	Telex
ITALY(1)	**Telav International** Via Salaria 1313, 00138 Roma	(6)691-9312/ 9376/7058	614381
ITALY(2)	**Telav International SRL** Viale Leonardo da Vinci 43, 20090 Trezzano sul Naviglio, Milano	(2)4455741	312827
JAPAN	**G & G Japan Inc.,** No. 406, 12-14, 4-Chome, Hongoh, Bunkyo-ku, Tokyo	(3)8130971	2722884
KOREA	**Sama Trading Corporation** CPO Box 2447, Seoul	(2)733 8336	26375
MALAYSIA	**TME Systems Pte Ltd.,** 21 Moonstone Lane, No. 06-01, Poh Leng Building, Singapore 1232	(286)4608	37545
NETHERLANDS	**Air Parts International BV** PO Box 255, 12 Kalkovenweg, 2400 AG Alphen a.d. Rijn	(72)43221	39564
NEW ZEALAND	**G.T.S. Engineering Ltd.,** 52 Broadway, Newmarket, AUCKLAND Box 9613	(9)546 745	60430
NORWAY	**Norsk Marconi A/S** Ryensvingen 5, PO Box 50, Manglerud, N-0612, Oslo 6	(2)680480	77140
PAKISTAN	**CMC** 22 Fareed Chambers, Abdullah Haroon Road, Karachi-3	(21)516134	24791
PORTUGAL	**Omnitecnica SARL** Estrada de Alfragide, 2700 Amadora	(19)905517	13433
SINGAPORE	**Mecomb Singapore Ltd.,** Sime Darby Centre, 896 Dunearn Road, 04-2 Singapore 2158	(469)8833	23178
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SWEDEN	**Ferner Electronics AB** Snormakarvagen 35, Box 125, 16126 BROMMA	(8)802540	10312
SWITZERLAND	**Kontron Electronic AG** Bemerstrasse-Sued 169, 8048 Zurich	0104114354111	822195
TAIWAN	**Evergo Corporation** Room A, 9Fl., 305 Section, 3 Nan King East Road, P. O. Box 94-546, Taipei	(2)7150283	27027
UNITED KINGDOM	**Datron Instruments** Hurricane Way, Norwich, Norfolk, England	(0603)404824	975173
UNITED STATES & CANADA	**Wavetek Indiana Inc.,** 5808 Churchman, Box190, Beech Grove, IN 46107	(317)787-3332	TWX8103413226

For customers in countries not listed please contact DATRON INSTRUMENTS in the United Kingdom