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DIGITAL MULTIMETER APPLICATIONS (4)

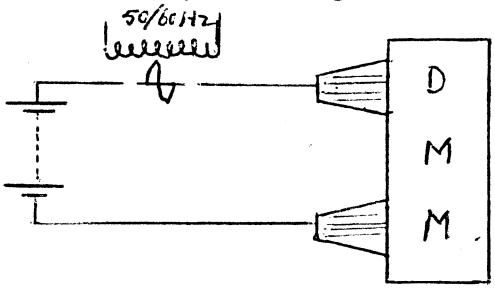
SERIES MODE REJECTION, LINE LOCKING,DIGITAL FILTERING,AVERAGING & ANALOGUE FILTERING

Not often highlighted, but arguably one the most significant factors in determining the actual quality of a precision Digital Multimeter's (DMMs) DCV measurement capability, is its Series Mode Rejection (SMR). If the SMR is not good, then claims of high accuracy are meaningless, and 6.5 to 8.5 digit resolution becomes unusable.

SERIES MODE REJECTION RATIO: *Expressed in dBs (see formula below), the Series Mode Rejection Ratio (SMRR), or Normal Mode (ACNMR) in the US, is a measure of a DMMs ability, when measuring DCV (or DCI & Ohms)), to reject any AC component in series with its input. That is the DMMs ability to accurately measure a (required) DC Voltage in the presence of an interfering (unwanted) AC Voltage.*

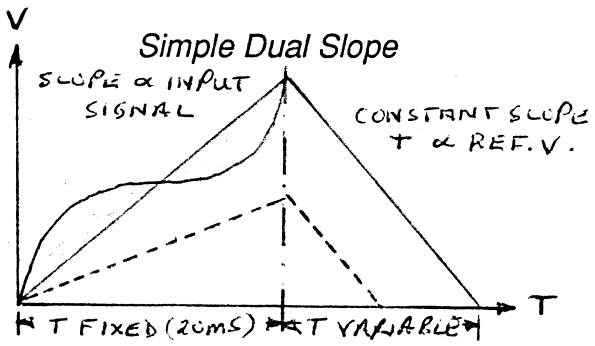
SMRR =

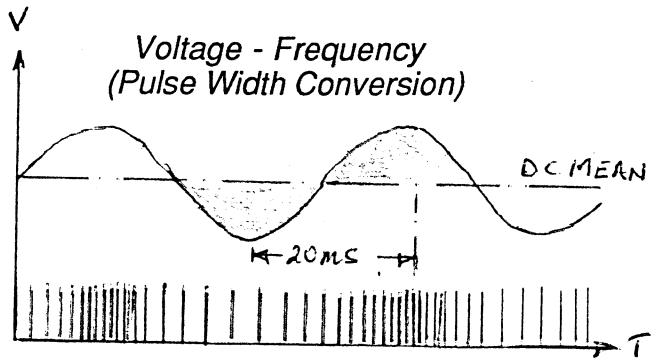
20 log (Pk - Pk series mode voltage) / (Pk - Pk voltage noise observed)



The most significant source of AC interference is the frequency of the utility supply, 50Hz in Europe and 60Hz in the USA and much of the Far East.

A-D CONVERSION TECHNIQUES: *Most DMMs today are caused to reject this AC component by timing the integration period of their A-D conversion to be coincidental with, or some multiple of, the line frequency (line-f). Examples of these A-D techniques are dual slope, quard slope (Autocal), multi slope (Selfcal) and voltage to frequency and associated techniques.*

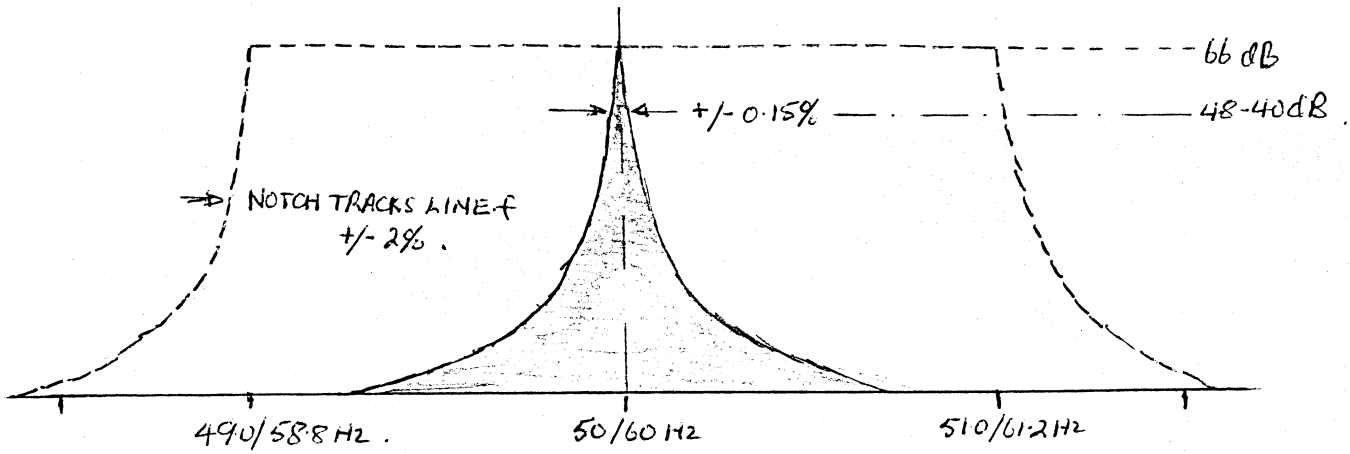




In these techniques the areas under the curve of the AC component cancel out, resulting in the measurement of the MEAN or DC level only.

Due to the inherent instability of the line-f, a simple Dual Slope technique, a timed 20ms (@ 50 Hz) integration period, will only provide a rejection "Notch" in the order of 48 dBs (suitable up to 4.5 Digits).

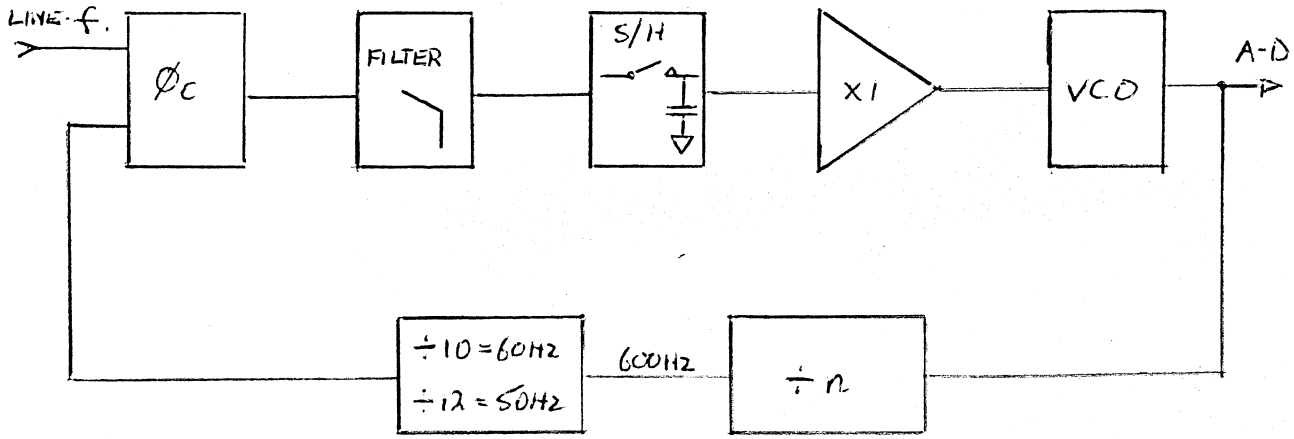
LINE LOCKING: *The next step in improving this performance is to provide line locking, that is locking the integrating period to line-f. This technique in theory can provide for infinite rejection, in practice due to the effects of cycle to cycle jitter, the rejection is in the order of 60 to 70 dBs (suitable up to 6.5 digits).*



The effectiveness of this rejection Notch is very much qualified by the ability of the DMM's line locking circuit to track (hold lock on) small shifts in line frequency. Utility authorities generally specify frequency stabilities in the order of +/- 1%.

Datrons 1271, 1061A, 1062 can maintain full line locking over a line-f drift of +/- 2%. Unless compensated for by a longer integration time (2s to 20s), most of our significant competition can only maintain full SMRR (60dB) for shifts in line-f of +/- 0.1%, beyond this shift their SMRR falls dramatically to about 40dB.

Datron's 1271 employs a traditional phase locked loop to lock its internal clock to line-f. In order to provide for a better long term stability the 1281 (as did the Autocal 1081 & 1071) locks its clock to an internal crystal.

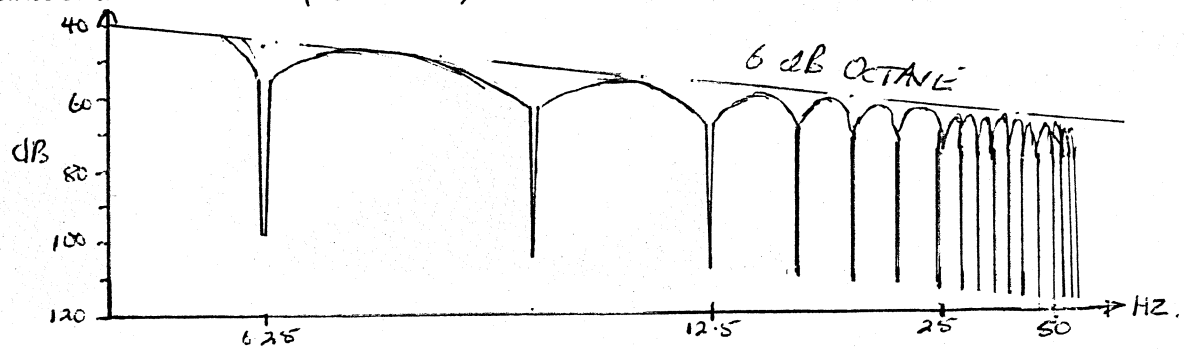


DIGITAL FILTERING: *Improvement on the basic 60 to 70dB SMRR obtained from an integration over one power line cycle (PLC) can be achieved by integrating over a number of PLCs, thereby averaging out the effects of line-f "jitter".*

Other manufacturers tend to require the user to select a specific integration time, Solartron in seconds, Hewlett Packard in PLCs, and Fluke an exponent value which defines the number of samples. The A-D in Fluke's 8506A/05A is not based on dual slope, but rather on a modified "successive approximation" technique.

In order to optimise for the best possible measurement configuration, the integration time in Datron's Selfcals is defined by the selection of "Fast" or "Normal" filter and by the scale length selected (please see page 5-71 of the Users Handbook).

Extending the integration time provides for a "COMB" of notches, the number being proportional to the number of PLCs. That is with a Selfcal DMM in a 6.5 digit "Normal" mode, the fouth notch coincides with line-f in the 1271 (4 x PLCs), and the sixteenth in the 1281 (16 x PLCs)



AVERAGING: *Another technique employed to improve the SMRR, and to give a quieter display, is post A-D averaging, where the user can choose to average over a number of readings. The Selfcal DMMs provide for both "Block" and "Rolling" average.*

ANALOGUE FILTERING: *A significant problem with these "digital" only techniques is that the rejection notches are only applied at line-f, or multiples of line-f. Unfortunately although line-f is the most significant contributor to AC interference, in the typical laboratory, ATE or other workplace, many other frequencies are present, emanating from adjacent instruments, fluorescent tubes, machine tools and other electrical equipment.*

Datron is unique in offering a solution. The Analogue filter available in all Datron's DMMs provides for an additional 12dB (Selfcal) or 18dB (Autocal) per octave of noise rejection, from approximately 6Hz upwards.

In addition to the general enhancement of measurement ability, this combination of digital and analogue filtering provides for a faster read-rate at higher levels of SMRR. eg the 1281 can provide for a 110 dBs SMRR at 1 reading/second in the 6.5 digit, Fast, Filter-In mode (Default Delay-faster with small step changes). Solartron's 7081 requires 10 Secs to achieve 90 dB, and the HP 3458A 20 Secs (1000 PLCs) to guarantee 80 dB.

SUMMARY: *In summary, two of a number of features in a Datron SELFCAL DMM which offer significant benefits to a prospective user, and advantage over the competition, are therefore ANALOGUE FILTERING (1281 &1271) and better LINE LOCKING (1271). The benefit to the prospective customer are:*

1. ***Significantly better measurement integrity in the typical (noisy) industrial environment.***

2. ***A unique combination of a fast read-rate, and good noise rejection.***

3. ***An ability to maintain the full Series Mode Rejection specification from the typical utility supply.***

NOTE: *In any test to prove the SMR performance of a DMM, it is essential that the AC Voltage source used to prove the SMRR is derived from the same supply that powers the unit.*

Ted Foster (Divisional Sales Support Manager) Norwich, England.