2-12. Wideband AC V Functional Description (Option -03)

The Wideband AC Voltage module (Option -03) consists of the Wideband Oscillator assembly (A6) and the Wideband Output assembly (A5). There are two wideband frequency ranges:

- o 10 Hz to 1.1 MHz
- o 1.2 MHz to 30 MHz

During operation between 10 Hz and 1.1 MHz, output from the Oscillator Output assembly is routed to the Wideband Output assembly where it is amplified and attenuated to achieve the specified amplitude range. The output is connected to the 5700A front panel WIDEBAND connector. Operation between 1.2 MHz and 30 MHz works the same way, except the input to the Wideband Output assembly is the ac signal from the Wideband Oscillator assembly.

2-13. DC Current Functional Description

DC current is generated in five ranges:

- o 20 uA - 220 uA
- o 220 uA - 2.2 mA
- o 2.2 mA - 22 mA
- o 22 mA - 220 mA
- o 2.2A

All current ranges except 2.2A are generated by the current portion of the Current/Hi-Res assembly. These currents are created by connecting the output of the DAC assembly, set to the 22V range, to the input of the Current assembly. The Current assembly uses this dc voltage to create the output current. The current output can be connected to the AUX CURRENT OUTPUT binding post by relays on the Current assembly, to the OUTPUT HI binding post by relays on the Current, Switch Matrix, and Analog Motherboard assemblies, or to the 5725A via the B-CUR line by relays on the Analog Motherboard assembly and Rear Panel assembly.

The 2.2A range is an extension of the 22 mA range. The 22 mA range output from the Current assembly is amplified by a gain of 100 by the High Voltage/High Current assembly operating in conjunction with the Power Amp assembly and the High Voltage Control assembly. The 2.2A current range is routed back to the Current assembly where it is connected to either the AUX CURRENT OUTPUT binding post, the OUTPUT HI binding post, or the 5725A in the same manner as the lower current ranges.

2-14. AC Current Functional Description

AC current is created in the same manner as dc current, except the input to the Current assembly is the ac voltage from the Oscillator Output assembly set to the 22V range. The switching between ac and dc is carried out on the Switch Matrix, Oscillator Control, Oscillator Output, and DAC assemblies.

2-15. Ohms Functional Description

Two assemblies function as one to supply the fixed values of resistance:

- o Ohms Main assembly (A10)
- o Ohms Cal assembly (A9)

All of the resistance values except the 1 ohm, 1.9 ohm, and short are physically located on the Ohms Main assembly. The 1 ohm, 1.9 ohm, and short are physically located on the Ohms Cal assembly. The desired resistance is selected by relays on these Ohms assemblies and is connected to the 5700A binding posts by relays on the Analog Motherboard. The Ohms Cal assembly also contains the appropriate circuitry to enable the 5700A to perform resistance calibration. Once calibrated, the 5700A output display shows the true value of the resistance selected, not the nominal (e.g., 10.00031 kilohm, not 10 kilohm).

Four ohms measurement modes are available:

- o For the two-wire configuration, measurement with or without lead-drop compensation sensed at the binding posts of the UUT (using the SENSE binding posts and another set of leads), or at the ends of its test leads is available for 19 kilohms and below.
- o Four-wire configuration is available for all but the 100 megohm value.

2-16. SYSTEM INTERCONNECT DETAILED CIRCUIT DESCRIPTION

The Motherboard assembly contains the Digital Motherboard assembly (A4), and the Analog Motherboard assembly (A3). These two Motherboards are mechanically fastened together with screws. They are electrically connected by connectors P81 and P82 on the Digital Motherboard and connectors J81 and J82 on the Analog Motherboard. AC voltage taps from the Transformer assembly (A22) are connected to the Analog Motherboard through these connectors. Refer to Figure 2-4 for an overview of system interconnections. Figure 2-4 continues on the reverse side, showing system grounds.

2-17. Digital Motherboard Assembly (A4)

The Digital Motherboard contains the line-select switches, line fuse, power switch, a fiber-optic transmitter (J73), and a fiber-optic receiver (J74). It also contains connectors for the Transformer assembly (A22), Digital Power Supply assembly (A19), CPU assembly (A20), Front Panel assembly (A2), Rear Panel assembly (A21), and the two 24V dc fans mounted in the chassis.

The fiber-optic receiver and transmitter provide the serial communication link between the CPU on the unguarded Digital Motherboard and the Regulator/Guard Crossing on the guarded Analog Motherboard.

2-18. Transformer Assembly (A22)

The Transformer assembly receives ac line inputs routed through the A4 Digital Motherboard. This assembly supplies outputs throughout the 5700A, all of which are routed through the A4 Digital Motherboard.

The Transformer assembly, the filter portion of the Filter/PA Supply assembly (A18), and the regulator portion of the Regulator/Guard Crossing assembly (A17) create the system power supply for all analog assemblies. The Transformer assembly also supplies ac voltages to the Digital Power Supply assembly which generates five regulated dc voltages for use by the CPU, Front Panel assembly, Rear Panel assembly, and the cooling fans.

2-19. Analog Motherboard Assembly (A3)

The Analog Motherboard contains the connectors for all assemblies in the guarded section of the calibrator. The Analog Motherboard also contains 13 relays, a fiber-optic transmitter, a fiber-optic receiver, a cable for binding post connections, and two cables for the interface to the Rear Panel assembly.

Table 2-1 lists Analog Motherboard connectors.

Table 2-1. Analog Motherboard Connectors

MOTHERBOARD CONNECTOR	CONNECTED TO ASSEMBLY
J101	Wideband Oscillator assembly (A6)
J111	Wideband Output assembly (A5)
J201 and J202	Switch Matrix assembly (A8)
J211 and J212	Current/Hi-Res assembly (A7)
J301 and J302	Ohms Main assembly (A10)
J311 and J312	Ohms Cal assembly (A9)
J401 and J402	DAC assembly (A11)
J501 and J502	Oscillator Control assembly (A12)
J511 and J512	Oscillator Output assembly (A13)
J601 and J602	High Voltage/High Current assembly (A15)
J611 and J612	High Voltage Control assembly (A14)
J701 and J702	Power Amplifier assembly (A16)
J801 and J802	Regulator/Guard Crossing assembly (A17)
J901 and J902	Filter/PA Supply assembly (A18)

The fiber-optic transmitter (J72) and the fiber-optic receiver (J71) provide the serial communication link between the Regulator/Guard Crossing assembly and the CPU assembly on the unguarded Digital Motherboard.

Control lines for relays K1-K10 and K13 on the Analog Motherboard assembly are generated on the Switch Matrix (A8) assembly. Control line RLY11*, which controls relay K11, is generated on the Current/Hi-Res assembly (A7). Control line RLY12*, which controls relay K12, is generated on the the Rear Panel assembly (A21).

Line INT OUT HI is the calibrator output for ac voltage operation in the 22V range and below, dc voltage operation in the 220V range and below, all resistance functions, and all ac/dc current ranges. Relays on the Current assembly route the current output to the AUX CURRENT OUTPUT binding post via the I OUT line if so selected by the operator. INT SENSE HI is the sense high path during these modes of operation. INT OUT HI is connected to the OUTPUT HI binding post through relay K1. INT SENSE HI is connected to the SENSE HI or OUTPUT HI binding post through relays K2 and K3.

Line HV OUT is the calibrator output for dc voltage operation in the 1100V range, and ac voltage operation in the 220V and 1100V ranges. Line HV SENSE is the sense high path during these modes of operation. HV OUT is connected to the OUT HI binding post through relays K9 and K1. HV SENSE is connected to the SENSE HI or OUTPUT HI binding post through relays K10, K2, and K3.

The 5725A Amplifier output is B OUT HI and the sense high path is B SNS HI. When the 5725A is active, B OUT HI is connected to the OUT HI binding post through relays K4 and K1. When the 5725A Amplifier is inactive, B OUT HI is connected to GUARD CHASSIS by relay K12. Line B SNS HI is tied to B OUT HI through diode clamps CR1 and CR2 and is connected to the SENSE HI or OUTPUT HI binding post through relays K5, K2, and K3.

The cable from the Motherboard to the binding posts consists of six insulated wires and six shields, each with its own drain wire. The OUT HI line, SENSE HI line, OUT/SENSE HI line and AUX CURRENT line each connect to an insulated wire and each has a shield around the wire. These shields are connected to OUT LO, SENSE LO, OUT/SENSE LO, and I/V GUARD, respectively. The I/V GUARD line is connected to I GUARD during operation in the current mode or V GUARD during operation in the voltage mode. This selection is done by relay K11.

When the 5700A is in standby, all binding posts are open-circuited except the GROUND binding post. In addition, GUARD CHASSIS is connected to S COM by K6. When in the operate condition, this connection is broken (K6 energized) and GUARD CHASSIS is connected to V GUARD via K7, which goes to the GUARD binding post, and to OUT LO via K8. GUARD CHASSIS is also connected to OSC LO GD by K13 except during ac or dc millivolt operation, when instead OSC LO GD is connected to S COM.

2-20. Front/Rear Binding Posts

An internal cable can be configured to enable either the front panel or rear panel binding posts. When compared to front panel binding posts, the rear panel provides the same OUTPUT HI, OUTPUT LO, SENSE HI, SENSE LO, AND V GUARD functions. Also, the rear panel provides an I GUARD (current guard) connection for use when the 5700A is supplying low-level ac current through a long cable. Use of the I GUARD connection removes errors introduced by leakage through such cables. The rear panel binding posts do not provide an AUX CURRENT OUTPUT connection. The procedure to disable the front panel binding posts and enable the rear panel binding posts is to be done at Service Centers, although it is described in this manual in Section 4.

2-21. Rear Panel

The Rear Panel assembly provides physical and electrical connections for the auxiliary amplifiers, along with RS-232-C and IEEE-488 interface connections. Relays on the Rear Panel assembly are used as the interfaces for the 5205A, 5215A, 5220A, or 5725A amplifiers, or for switching the PHASE LOCK IN and VARIABLE PHASE OUT signals.

Three Auxiliary Amplifiers can be physically connected to the Rear Panel assembly of the 5700A: the 5725A at J7, the 5220A at J4, and either 5205A or 5215A at J3. Only one amplifier can be in use at one time.

- The Rear Panel assembly provides relay switching for 5725A signals. Voltage outputs from the 5725A are routed to the binding posts on the 5700A. Current outputs are sourced at the 5725A OUTPUT binding posts. An alternate configuration is also available, allowing for routing of 5700A current outputs to the 5725A OUTPUT binding posts.

- When the 5220A (current output) is selected via the front panel, the output of the 5700A is routed to connector J4 on the rear panel, which is the interface to the 5220A.

- When the 5205A (ac and dc volts) or 5215A (ac volts only) function is selected via the calibrator keyboard, the output of the calibrator is routed to connector J3 (pins 1, 9, 2, and 10) on the Rear Panel assembly.

2-22. Power Supply

The Filter/PA Supply assembly (A18) incorporates two sections. The first section contains filters and regulators for some of the in-guard low-voltage supplies, and the second contains the power supply for the Power Amplifier output. Theory for each section is discussed separately.

2-23. DIGITAL SECTION DETAILED CIRCUIT DESCRIPTION

Detailed descriptions of each assembly in the digital section are provided here. Simplified schematics and block diagrams are provided to supplement the text.

2-24. Digital Power Supply (A19)

The Digital Power Supply assembly receives ac voltages from the transformer and provides five regulated dc voltages for use by the CPU, Front Panel assembly, Rear Panel assembly, and the cooling fans. All power supply voltages are referenced to COMMON, which is the transformer center tap for the ± 12V supplies. Test points at the top of the assembly can be used to check unregulated input voltages, and regulated dc output voltages.

Table 2-2 lists the supplies generated by the Digital Power Supply.

Table 2-2. Supplies Generated by the Digital Power Supply

SIGNAL NAME	TEST POINT	NOMINAL OUTPUT	TOLERANCE	CURRENT LIMIT	RATED OUTPUT
+75V OUT	TP2	73V	8%	121 mA	100 mA
+35V OUT	TP5	35V	7%	52 mA	40 mA
+12 VOLTS	TP8	12V	5%	1.5A	700 mA
-12 VOLTS	TP10	12V	5%	1.5A	450 mA
+5V	TP12	5.2V	5%	2.4A	2.0A
COMMON	TP13				

2-25. +5V POWER SUPPLY

The unregulated +5V supply uses CR25-CR28 in a full-wave rectifier configuration with filter capacitors C12, C13, and C14. Capacitors C20 and C21 filter out high-frequency noise. Inductor L8 is a common-mode choke and C11 is a bypass capacitor. The regulator is fused by 3.15A slow-blow fuse F5.

The regulated +5V is generated by three-terminal low-dropout +5V regulator U3 with heat sink. The regulator's output voltage is increased about 0.2V by CR35, a germanium diode connected between the regulator's ground pin and COMMON. Capacitor C14 is for bypass. Capacitor C23 filters out high-frequency noise. Diode CR29 protects the regulator against input shorts, and diode CR30 protects the regulator from reverse voltage. Inductor L7 and C16 further filter the output to P41.

2-26. ± 12V POWER SUPPLIES

A full-wave rectifier made of diodes CR17-CR20 and filter capacitors C6 and C7 generate the unregulated +12V and -12V supplies. AC inputs are fused by F3 and F4, both 2A slow blow.

The regulated +12V supply is generated by a three-terminal +12V regulator U1 with heat sink. Capacitors C5 and C9 are for bypass. Diode CR21 protects the regulator from input shorts, and diode CR23 protects the regulator from reverse voltage. Capacitor C22 filters out high frequency noise.

Three-terminal -12V regulator U2 with heat sink generates the regulated -12V supply. Capacitors C8, C10, and C19 are for bypass. Diode CR22 protects the regulator from input shorts, and diode CR24 protects the regulator from reverse voltage.

Inductors L3-L6 filter the regulated outputs. R7 further isolates the ±12V FAN lines from the ±12V power lines. The +12V FAN and -12V FAN lines power the two 24V dc fans inside the calibrator.

2-27. +35V POWER SUPPLY

The +35V power supply powers the grid drivers and anode drivers on the front panel output display circuitry.

A full-wave rectifier made of diodes CR9-CR12 and filter capacitor C3 generate the unregulated +35V supply. Its input is fused by F2, a 0.125A slow-blow. Capacitor C18 is for bypass. Capacitor C25 filters out high frequency noise.

Zener diodes VR14, VR15 and transistor Q5 generate the +35V regulated output. Zener diodes VR14 and VR15 (both 18V) make up the control element which sets the output voltage. Transistor Q5 is used as an emitter follower. CR13 is the constant current source supplying current to the zener diodes and the base of Q5. Components R5 and Q6 make up the current-limiting circuit. During an over-current condition, the voltage drop across R5 turns Q6 on, thus drawing current away from the base of Q5 and limiting current flow to the output. Diode CR16 protects this circuit from reverse voltage and C4 is a bypass capacitor. Inductor L2 filters the regulated output. Resistor R13 is a bleed-off resistor for C3.

2-28. +75V POWER SUPPLY

The +75V power supply powers the grid drivers and anode drivers on the front panel control display circuitry.

A full-wave rectifier made of diodes CR1-CR4 and filter capacitor C1 generate the unregulated +75V supply. Its input is fused by F1, a 0.315A slow-blow. Capacitor C17 is for bypass. Capacitor C24 filters out high frequency noise.

The +75V regulated output is generated by 36V zener diode VR6, 39V zener diode VR7, and transistors Q1 and Q3. Zener diodes VR6 and VR7 set the output voltage. Transistors Q1 and Q3, in a Darlington configuration for current gain, are used as an emitter follower. Transistor Q4, zener diode VR5, and resistors R2 and R3 make up the constant current source supplying current to the zener diodes and the base of Q3. Current limiting is performed by R1 and Q2 in the same manner as in the +35V supply. Diode CR8 protects the circuit from reverse voltage and C2 is a bypass capacitor. Inductor L1 filters the regulated output. Resistor R6 is a bleed-off resistor for C1.

2-29. +35V AND +75V SHUT-DOWN CIRCUIT

The +35V and +75V high voltage supplies are shut down when a fault occurs in the control display refresh circuitry. This shut-down circuit prevents the Control Display and Output Display from burning out, and also verifies that the master clock is generating control signals for both displays.

During normal operation, 75VSD is low, turning Q10 off. Line RESETL pulls the base of Q9 high through R9, turning Q9 on. This action in turn pulls the junctions of CR31-CR32 and CR33-CR34 low, turning Q7 and Q8 off. The +75V and +35V constant-current sources can then supply the appropriate zener diodes and drive the bases of the respective emitter followers.

When a display refresh fault occurs, the 75VSD line on P41 pin 5C, coming from the Front Panel assembly, goes high. this signal, pulled up by R4, drives the base of Q10 through base resistor R11. Transistor Q10 then saturates, pulling the base of Q9 near ground, turning Q9 off. On power-up or during a CPU reset, the RESETL signal is low, pulling the base of Q9 near ground through R9, also turning Q9 off. Resistor R12 is a turn-off resistor for Q9. Diodes CR31 and CR33 are in a wired-OR configuration. When Q9 is saturated (on), CR31 and CR33 pull their respective junctions to CR32 and CR34 near ground, turning Q7 and Q8 off. When Q9 is off, the junctions are pulled high through R8 and R10, saturating Q7 and Q8 (on). When on, Q7 removes the base drive from Q3, shutting down the +75V supply. Similarly, Q8 removes the base drive from Q5, shutting down the +35V supply.

Diodes CR32 and CR34 simply insure that Q7 and Q8 are off when Q9 is on. Resistor R8 guarantees that Q7 will hold the +75V supply off until it drops below 15.6V, and R10 holds the +35V supply off to 7.8V.

2-30. CPU (Central Processing Unit, A20)

The CPU (Central Processing Unit) for the 5700A is a single-board computer based on a 68HC000 microprocessor. The CPU assembly communicates with the Guarded Digital section, the Front Panel assembly, and the Rear Panel assembly. The board can be divided into three primary areas:

- o The microprocessor and its support circuitry
- o Memory
- o Peripheral chips and I/O interfaces

Microprocessor support circuitry consists of a power-up and reset circuit, clock generation, a watchdog timer, address decoders and dtack generator, bus error timeout, and interrupt controller.

Figure 2-5 is a block diagram of the CPU assembly. Table 2-3 is a glossary of the acronyms used in the text and schematic for the CPU assembly.

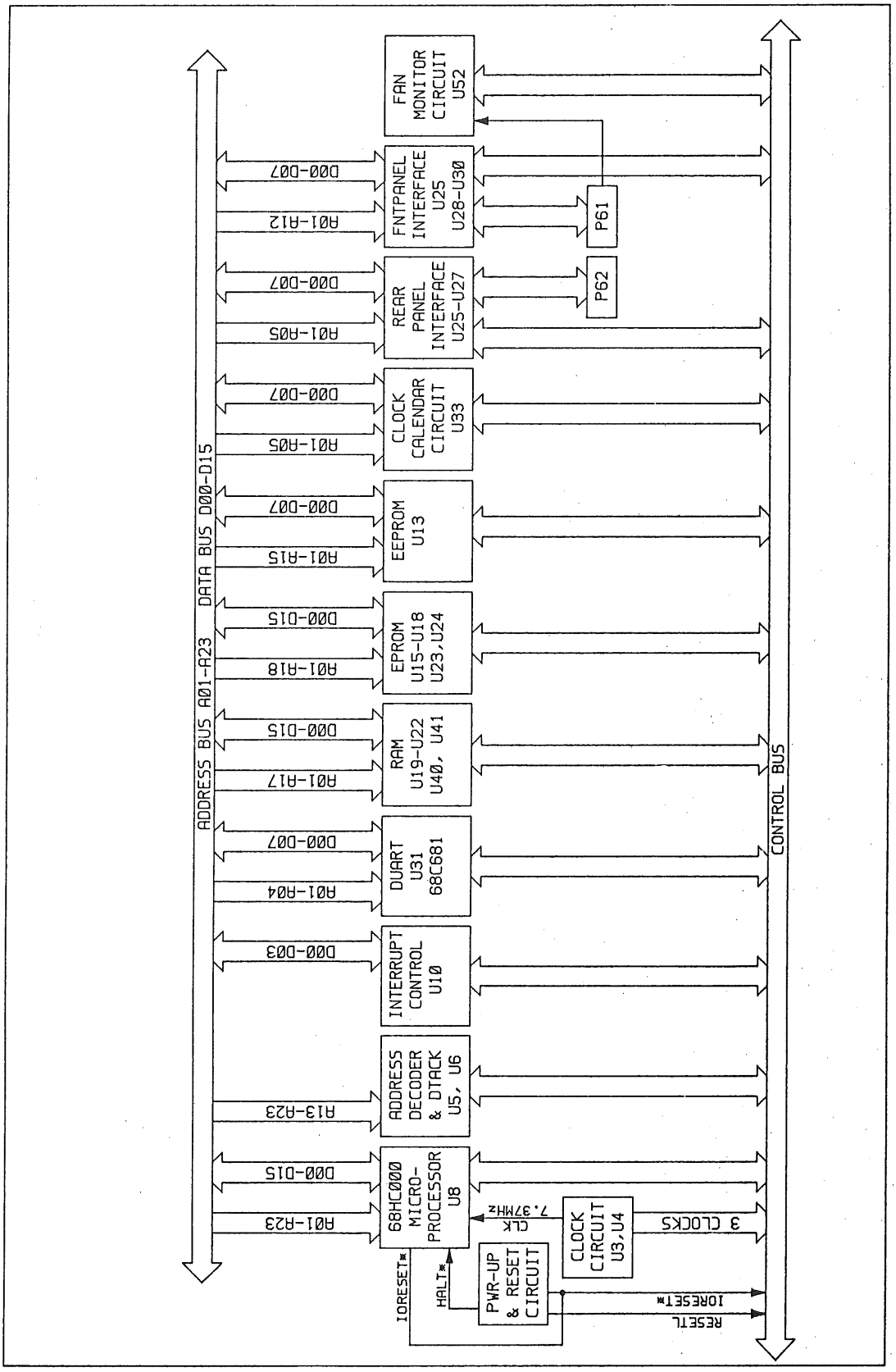


Figure 2-5. CPU Assembly Block Diagram

Table 2-3. CPU Acronym Glossary

A01-A23	Address lines
ADCLKCS*	Clock/calendar (U33) chip select
AS*	Address strobe
BERR*	Bus error
BGACK*	Bus grant acknowledge
BR*	Bus request
BRPDRTINT*	Rear panel DUART interrupt
BRPDTK*	Rear panel data transfer acknowledge
BRPIEEEINT*	Rear panel IEEE-488 interrupt
CLKCALINT*	Clock/calendar interrupt
D00-D15	Data lines
DOGCLR	Dog clear (clears watchdog timer)
DOGINTH	Dog interrupt (interrupt from watchdog timer)
DRTDTK*	DUART data transfer acknowledge
DTACK*	Data transfer acknowledge
E	Enable for 6800 family devices (737.28 kHz clock)
EXDUARTINT*	External DUART Interrupt
FAN1	Signal monitoring fan 1
FAN2	Signal monitoring fan 2
FANINT*	Fan monitor interrupt
FC0	Function code output 0
FC1	Function code output 1
FC2	Function code output 2
FPDTK*	Front panel data transfer acknowledge
FRNTPNLCS*	Front panel chip select
FRNTPNLEN*	Front panel enable
GCDRTCS*	Guard crossing DUART chip select
GCDUARTINT*	Guard crossing DUART interrupt
INTRCNTL1	Interrupt control 1
INTRCNTL2	Interrupt control 2
IPL0*	Interrupt priority level 0
IPL1*	Interrupt priority level 1
IPL2*	Interrupt priority level 2
KEYBRDINT*	Keyboard interrupt
LDS*	Lower data strobe
MISCCS*	Miscellaneous chip select enable (upper address bits decoder)
NVMCS*	Nonvolatile memory chip select
NVMOE*	Nonvolatile memory output enable
PROM0CS*	PROM 0 chip select (U15 and U16)
PROM1CS*	PROM 1 chip select (U17 and U18)
PROM2CS*	PROM 2 chip select (U23 and U24)
PSFAILINT*	Power supply fail interrupt
RAM0CS*	RAM chip select (U19 and U20)
RAM1CS*	RAM chip select (U21 and U22)
RAM2CS*	RAM chip select (U40 and U41)
R/WR*	Read/write
RDINT*	Read interrupt
RDL*	Read data lower
RDU*	Read data upper
RDY/BSYL	Ready/busy

Table 2-3. CPU Acronym Glossary (cont)

RPSEL*	Rear panel chip select
RRPNLEN*	Rear panel enable
RXDA	Receive Data Port A
RXDB	Receive Data Port B
SCLK	Serial clock
TXDA	Transmit Data Port A
TXDB	Transmit Data Port B
UDS*	Upper data strobe
WRL*	Write lower
WRU*	Write upper
XDUARTCS*	External DUART chip select

2-31. POWER-UP AND RESET CIRCUIT

The power-up and reset circuitry consists of line monitor chip U1, C5, C6, CR1, R3, Z3, switch SW1, and inverters on U2. This circuit provides a 195 ms reset pulse at power-up or upon pressing and releasing SW1, placing the CPU assembly in a known safe condition. If the power supply glitches or falls below 4.55V $\pm$0.05V, U1 resets the 5700A. The reset pulse duration is determined by C5. Note that SW1 performs a different function than the front panel RESET button. SW1 is a hardware reset that is hard-wired to and directly read by the microprocessor. The front panel RESET button is a software reset; it tells the system software to restore the 5700A configuration to a default condition.

The heart of this circuit is the line monitor chip U1. On power-up or when SW1 is pushed, U1 forces an active-low reset pulse on RESETL and an active-high pulse on RESET. RESETL helps to prevent accidental writes to EEPROM and drives an inverter in U2 to turn off LED CR1. CR1 indicates that the +5V supply is on and that the CPU is operating, i.e. not reset. RESETL also resets the rear panel assembly. The other output, RESET, drives two inverters in U2. One of these inverters provides HALT*. The other generates IORESET*, which drives the processor's RESET, and provides a reset for the front panel interface and DUARTs (dual universal asynchronous receiver/transmitter) circuitry.

2-32. CLOCK GENERATION

The clock generation circuit uses components Y1, Y2, U3, U4, R4, R5, C8, C9, and E5. The crystal Y1, along with the resistors, capacitors, and an inverter in U3 generates the 7.3728 MHz primary system clock CLK. This system clock is used by the processor and is divided down by a binary counter (U4) for clocks of 3.6864 MHz, 28.8 kHz, and 450 Hz. The 450 Hz clock is used by the watchdog timer, the 28.8 kHz is used by U6 in the decoding circuit, and the 3.6864 MHz is used by the DUARTs, and the clock filter circuit. Jumper E5 allows for selection of the alternate oscillator (Y2) as the system clock.

2-33. WATCHDOG TIMER

The watchdog timer circuitry uses a 74HC4020 binary counter (U11) to divide the 450 Hz from the clock generation circuit to produce interrupt DOGINTH, signifying that the system may be locked up. This interrupt is generated 1.14 seconds after the last DOGCLR2 signal from interrupt controller U10. Therefore, DOGCLR2 must occur more often then every 1.14 seconds to clear U11 and prevent the watchdog interrupt. Generation of DOGCLR2 is under software control. The watchdog timer can be disabled by cutting jumper E1.

2-34. ADDRESS DECODING AND DTACK

Two Programmable Logic Devices (PLDs) accomplish address decoding and dtack (data acknowledge) generation. ICs U5 and U6 provide chip selects and generate acknowledgement signals for those devices without data acknowledge lines. IC U5 receives dtack signals from the asynchronous devices and ORs these signals together to form DTACK*. Table 2-4 is the memory map for the system. It shows the chip select, address range, and notes whether AS* (address strobe) or LDS* (lower data strobe) is required.

Table 2-4. CPU Memory Map

CHIP SELECT	READ/WRITE	ADDRESS RANGE	AS* OR LDS* REQUIRED?
PROM0CS*	R	0 - 3FFFF	no
PROM1CS*	R	40000 - 7FFFF	no
PROM2CS*	R	80000 - BFFFF	no
RAM0CS*		600000 - 60FFFF	no
RAM1CS*		610000 - 61FFFF	no
RAM2CS*		620000 - 623FFF	no
NVMCS*	R/W	C00000 - CFFFFF	no
MISCCS*	R/W	D00000 - DFFFFF	no
RPSEL*	R/W	D00000 - D01FFF	LDS*
RPDUARTCS*	R/W	D00000 - D0001F	LDS*
RPIEEECS*	R/W	D00020 - D0002F	LDS*
Y52XXRD*	R	D00030 - D00031	LDS*
Y5205WR*	W	D00032 - D00033	LDS*
Y5220WR*	W	D00034 - D00035	LDS*
FRNTPNLCS*	R/W	D02000 - D03FFF	AS*
OTDCS*	R/W	D02000 - D027FF	AS*
DMDCS*	R/W	D02800 - D02FFF	AS*
ENCODERCS*	R	D03000 - D033FF	AS*
ENCODERRESET*	W	D03000 - D033FF	AS*
LED_OUTPUT_CNTRL	R	D03400 - D037FF	AS*
LED_LATCH_EN	W	D03400 - D037FF	AS*
KEYBOARDCS*	R/W	D03800 - D038FF	AS*
GCDRTCS*	R/W	D04000 - D05FFF	LDS*
XDUARTCS*		D06000 - D07FFF	LDS*
RDINT*	R/W	D08000 - D09FFF	AS*
DOGCLR	W	D08000 - D09FFF	even only, AS*
ADCLKCS*		E00000 - EFFFFF	AS*

2-35. INTERRUPT CONTROLLER

PLD U10 is the priority interrupt controller. The interrupt controller reads incoming interrupts and interrupt control lines, then encodes the highest priority interrupt into the interrupt level for the 68HC000. When the 68HC000 responds to an interrupt request, it asks the interrupt controller for an 8-bit vector that corresponds to the pending interrupt of highest priority. The interrupt controller responds with the 4 LSB's of the vector according to how it is programmed. The 4 MSB's are pulled up on resistor network Z1. Table 2-5 shows the interrupts, their priority levels, and vectors.

Table 2-5. CPU Interrupts, Priorities, and Vectors

INTERRUPT	PRIORITY LEVEL	VECTOR (HEX)	
NMI	7	-	(not used)
DOGINTH	6	F4	
BRPDRTINT*	5	F6	
GCDUARTINT*	5	F7	
EXDUARTINT*	5	F8	
CLKCALINT*	4	F5	
BRPIEEEINT*	4	F9	
KEYBRDINT*	3	FA	
BPSFAILINT*	2	FB	
FANINT*	0	FF	(not used)
RDY/BSYL	0	FF	(not used)
No interrupt	0	FF	

2-36. GLUE LOGIC

ICs U2, U3, and U9 form the glue logic circuit, which keeps various CPU functions running properly. The four OR gates in U9 and an inverter in U3 use control signals UDS*, LDS*, and R/WR* from the microprocessor to generate control signals WRU*, WRL*, RDL*, and RDU*.

2-37. RAM (RANDOM-ACCESS MEMORY)

Random-access memory is contained in three pairs of sockets, U19 and U20, U21 and U22, and U40 and U41. These sockets accommodate either 32K x 8 or 128K x 8 static CMOS RAM modules (32KB or 128 KB each). The 5700A is shipped with U19-U22 installed, using 32K x 8 parts and providing 128 KB of static RAM.

2-38. ROM (READ-ONLY MEMORY)

Read-only memory is contained in three pairs of sockets, U15-U16, U17-U18, and U23-U24. These sockets accommodate 27010 EPROMS, 128K x 8 devices (128 KB each). Jumpers allow 256 KB devices to be used in their place. The 5700A is shipped with U15-U18 installed, providing 512 KB of EPROM.

2-39. ELECTRICALLY-ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)

IC U13 is an EEPROM. The socket accommodates a 32K x 8 device (32 KB of storage.) A jumper is provided to allow an 8K x 8 (8 KB) device to be used in place of the 32 KB device. The 5700A is shipped with a 32KB EEPROM installed.

The EEPROM requires protection against inadvertent writes during power-up and power-down sequences, which could corrupt calibration constants stored there by the 68HC000. The 32 KB EEPROM provides for software-controlled protection against accidental writes.

Hardware is also used to further ensure data integrity. The EEPROMs are designed so that writes to the device are prevented by holding the output enable line (NVMOE*) low. Diodes CR5, CR6 and CR8, together with resistor R6, perform a wired-OR function for three signals that control NVMOE*. Components R6, CR6 and C17 hold NVMOE* to a valid logic low for typically 37.3 ms during power-up; 26.8 ms minimum, 49.6 ms maximum. Diode CR7 provides a discharge path for C17 on power-down, allowing the operator to quickly turn the 5700A off then on again, without interfering with the power-up charge time of the capacitor. Diode CR8 allows the normal microprocessor read of the device to take place. And diode CR5 allows power monitoring IC U1 to hold NVMOE* low when the +5V power supply drops below 4.5V on power-down or during power glitches.

2-40. DUART (DUAL UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER) CIRCUIT

The 68C681 DUART (U31) has several functions. Its primary function is to provide the asynchronous serial lines that communicate with the Guarded Digital Controller over the fiber-optic path off the Digital Motherboard. A 75451 driver chip (U32) drives the fiber-optic transmitter on the digital Motherboard.

The DUART has 8 output lines that perform various functions. INTRCNTL1 and INTRCNTL2 go to the interrupt controller and are fed back to the DUART inputs. These are used by the interrupt controller to enable certain interrupts. Line SCLK is a test output of the channel A serial clock.

The DUART monitors the EEPROM ready signal and the FANINT* signal. It also has a spare serial channel that goes to connector J5. Components U44 and U43 convert the TTL-level signals at the DUART to RS-232-C-level signals at J5.

The DUART generates its own dtack signal, DRTDTK*, which is used by U5 to generate system dtack, DTACK*. A second DUART, U42, with associated RS-232-C drivers and receivers is used only for test purposes. It generates its own dtack, wire-ORed to DRTDTK*.

2-41. CLOCK/CALENDAR CIRCUIT

Time and date information is stored in a battery-backed clock/calendar circuit consisting of 32.768 kHz crystal Y3, 3V lithium battery BT1, clock/calendar IC U33, and capacitors C10 and C11. The clock/calendar IC has the necessary circuitry internally to switch operation from the power supply to battery BT1. Pull-up resistors in Z5 off U33 are to ensure low power operation when the +5V supply is off. U33 generates CLKCALINT* under software control.

2-42. CLOCK FILTER CIRCUIT

The clock filter circuit generates a 3.6864 MHz 200 mV sine wave for the Rear Panel and Front Panel assemblies. This circuit buffers the 3.6864 MHz Clock with an inverter in U3. The circuit contains dc-blocking capacitor C80 which forms a high-pass filter with R81, two stages of a low pass LC filter (L80 and C81, L81 and C82), load resistor R81, transformer T51, and termination resistor R82.

2-43. CPU TO REAR PANEL INTERFACE

Components U25, U26, U27, and connector P62 interface the CPU to the rear panel. Bi-directional bus transceiver U26 buffers the data lines. Control signal R/WR* controls the transmission direction of the data lines, and RRPNLEN* is the chip enable. IC U25 buffers control lines BRPDRTINT*, BRPIEEEINT*, and BRPDTK*. U27, enabled by RRPNLEN*, buffers address line A01-A05 and control lines WRL* and R/WR*. Control lines RESETL, RPSEL*, TXDB, RXDB, and XMT go directly to connector P62.

2-44. CPU TO FRONT PANEL INTERFACE

Components U25, U28, U29, U30 and connector P61 interface the front panel to the CPU. Bi-directional bus transceiver U30 buffers the data lines. Control signal R/WR* controls the transmission direction of the data lines, and FRNTPNLEN* is the chip enable. IC U28, enabled by FRNTPNLEN*, buffers address lines A05-A12. IC U29, also enabled by FRNTPNLEN*, buffers address lines A01-A04 and control line R/WR*. Two sections of U25 in parallel buffer IORESET*, providing twice the drive current of a single section, generating BRESET*. Three other sections of U25 buffer FPINT*, FPDTK*, and PSFAILINT*. Control line FRNTPNLCS* goes directly to connector P61.

2-45. FAN MONITOR

The fan monitor circuit detects whether one of the two fans is fully or partially shorted, open-circuited, or drawing excessive current. Current-sense resistors on the Digital Motherboard send analog signals FAN1 and FAN2 to the CPU through P61. FAN1 is subtracted from FAN2 in U52D, and the difference is amplified before being sent to a window comparator made up of U52B and U52C (plus associated resistors). Capacitors C12 and C13 act as low-pass filters for the two signals, preventing spurious noise from interfering with detection circuitry.

When the output of U52D is greater than +5V, the output of U52B goes low (to about -11V); otherwise the output is high (about +11V). U52A takes the +5V and generates a -5V reference for comparator U52C. When the output of U52D is more negative than -5V, the output of U52C goes low (to about -11V); otherwise the output is high (about +11V). The outputs of U52B and U52C are wire-ORed through CR2 and CR3, using R52 and R53 to limit current sunk by the comparators when their respective outputs are low. Schottky barrier diode CR4 converts the -11V outputs of the comparators, when either is low, to a TTL-level logic low, which is the active (true) level of FANINT*.

When both fans are functioning properly, diodes CR2 and CR3 are reverse-biased, effectively taking the comparators out of the circuit. At this point, R51 pulls FANINT* to a valid TTL-level logic high, the inactive state of FANINT*. R51 and CR4 level-shift the $\pm$11V signal to valid TTL levels.

Signal FANINT* goes to DUART U31 and to the interrupt controller U10 for further processing. System software monitors FANINT* through U31, and can program the DUART to generate a GCDUARTINT* interrupt signal on FANINT* going low.

2-46. Front Panel Assembly (A2)

The Front Panel assembly, operating in conjunction with the Keyboard assembly (linked by a cable), is the operator interface to the 5700A. This assembly contains two separate vacuum-fluorescent displays: the Control Display and the Output Display. Each display has its own control, high voltage drive, and filament-switching circuits. This assembly also contains clock regeneration, refresh failure detect, keyboard scanner, rotary knob encoder, LED drive, and decoding and timing circuitry.

Connector J2 connects this assembly with the Keyboard/Encoder. Connector J1 interfaces with the CPU assembly and the Digital Power Supply assembly via the Digital Motherboard.

2-47. CLOCK REGENERATION CIRCUITRY

To minimize EMI (electro-magnetic interference), the Front Panel assembly accepts a low-level sine-wave (approximately 200 mV p-p) 3.6864 MHz clock from the CPU assembly and converts it to a TTL-acceptable level. This is done by high-speed differential comparator (U7A), operating on incoming signals 3.6864MHZCLK and 3.6864MHZCLK*. The output of U7A is the input to U8 and is also inverted by U11B to create the 3.6864 MHz clock signal CLOCK. Twelve-stage binary counter U8 divides the 3.6864 MHz clock by eight and U11A inverts the signal to create 460.8 kHz. The master clock is further divided by U8, which outputs a 900 Hz signal on pin 1. These clocks provide system timing for the other ICs on the assembly. A -5.2V supply for U7 is provided by VR5, with C64 acting as the supply bypass.

2-48. REFRESH FAILURE DETECT CIRCUITRY

If a clock failure were to occur, the refresh cycles of the vacuum-fluorescent displays would be interrupted. This condition could damage the tubes if not immediately detected. Refresh failure detect circuitry monitors the GRIDDATA output from the last high voltage driver (U23) for the Control Display. This output (REFRESH) is used to clear a watchdog timer (U6) every refresh cycle. If the refresh is interrupted and GRIDDATA does not occur, the watchdog timer times out and latches U12. Flip-flop U12 generates control lines 75VSD and PSFAILINTR*. Control line 75VSD is routed to the Digital Power Supply assembly to shut down the +35V and +75V power supplies, thus preventing damage to the vacuum-fluorescent displays. Interrupt line PSFAILINTR* is used by PLD U3 to properly blank the Control Display and Output Display through DMDBLANK and OTDBLANK, and alerts the CPU that this failure has occurred.

2-49. DECODING AND TIMING CIRCUITRY

Main decoding and master timing functions for the front panel is accomplished by an EP900 PLD (Programmable Logic Device), U3. Two state machines control display refresh and filament switching. Filament switching is handled by two non-overlapping 57.6 kHz signals.

Signals GSTRBE and STROBE are master timing and synchronization signals used by the other ICs. Signal DMDBLANK controls the Control Display grid drivers, ABCLK and CDCLK control the Control Display anode drivers, and OTDBLANK controls the Output Display grid and anode drivers. Front panel DTACK and interrupt functions, and generation of the various chip select and reset signals are also provided by U3.

Table 2-6 is a memory map for the front panel.

Table 2-6. Front Panel Memory Map

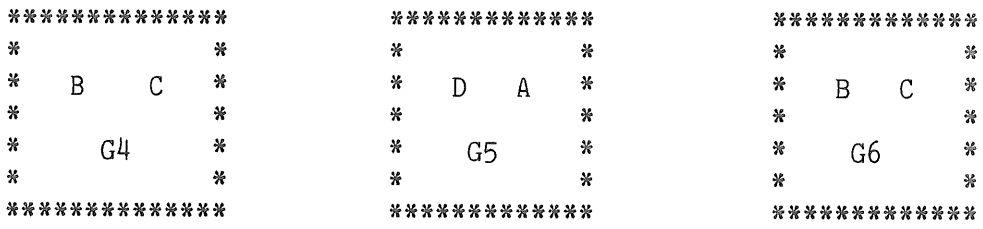
NAME	READ/WRITE	ADDRESS
OTDCS*	R/W	D02000-D027FF
DMDCS*	R/W	D02800-D02FFF
ENCODERCS*	R	D03000-D033FF
ENCODERRESET*	W	D03000-D033FF
LED_OUTPUT_CNTRL	R	D03400-D037FF
LED_LATCH_EN	W	D03400-D037FF
KEYBOARDCS*	R/W	D03800-D03BFF

2-50. CONTROL DISPLAY CIRCUITRY

Control display circuitry consists of a 26-row by 256-column vacuum-fluorescent dot matrix display under the control of PLD U4, four high voltage grid drivers (U20-U23), four high voltage anode drivers (U16-U19), a filament switching circuit, and 1K x 8 (1 KB) dual-port RAM U1.

This display is divided into 129 grids; alternate grids contain two anode columns lettered B C or D A. Grid G129 and column C in grid G128 are not used. Each column contains 26 individual anodes.

IC U4 is an EP900 Programmable Logic Device (PLD). It provides the timing and control signals for control display circuitry. Display data written by the microprocessor into the Control Display's dual port RAM (U1) is read by U4 and sent serially to the high voltage anode drivers. Both the anode and grid drivers are serial TTL-level input, 32-bit parallel high voltage output devices. IC U4 also controls the grid timing and display refresh.



Adjacent columns in adjacent grids are driven, while the opposite columns are turned off. For instance, grid G4 contains columns B and C, and grid G5 contains columns D and A. G4 and G5 are driven simultaneously while anode columns G4-C and G5-D are activated, and G4-B and G5-A are driven off. Next, grids G5 and G6 are driven simultaneously, while columns G5-A and G6-B are activated, and G5-D and G6-C are driven off. This pattern is repeated for all 128 grids at a refresh rate of about 75 Hz.

This particular scheme was selected because of the way the anode drivers are loaded with display data. Both the A and C (U16 and U18), and B and D (U17 and U19) anode drivers' input registers are latched with the same data, while the output drivers are appropriately enabled and displaying the data previously strobed to the driver outputs from the input registers. The input register data is strobed to the output drivers while all of the drivers are disabled, or blanked. Following this, either the A and B drivers are enabled to display the A-B data, when the C and D drivers, latched with A-B data, are disabled, or the C and D drivers are enabled to display the C-D data, when the A and B drivers, latched with C-D data, are disabled.

Control display filament driver circuitry consists of transistors Q1 through Q6 and zener diodes VR1 and VR2, with associated resistors. The transistors are driven by 7406 open collector drivers U13B and U13A. These drivers are controlled by AOUT and BOUT. AOUT and BOUT are synchronous, non-overlapping, three-eighths duty cycle, 57.6 kHz timing signals generated by U3. Each signal is alternately active high for 6.51 us, with a dead time between active signals of about 2.17 us to allow for turn-off times of the drive transistors. When AOUT is high, U13B turns Q2 and Q4 on. Q4 turns Q6 on, providing a path for the filament current through Q2 and Q6. Zener diode VR2 provides the dc voltage offset necessary for proper filament operation. Then when BOUT is high, U13A turns Q1 and Q3 on. Q1 turns Q5 on, providing a path for the

filament current through Q3 and Q5, effectively reversing the direction of the voltage driving the filament. Zener diode VR1 provides the dc voltage offset necessary for proper filament operation.

PLD U4 also generates the 225 Hz square-wave SCAN signal used by PLD U9 to control front panel keypad scanning and key debounce.

Dual-port RAM U1 contains all the Control Display data written by the 68HC000 microprocessor on the CPU board. PLD U4 contains a 10-bit address counter which is used by U4 to read the contents of U1. U1 provides a BUSYD signal to U3, which is active low whenever the CPU and U4 try to access the same RAM location at the same time. If the microprocessor attempts to write to the RAM location that U4 is reading (as it refreshes the DMD), U3 uses BUSYD to hold off DTACK to the microprocessor. This prevents the written data from being lost. The other busy signal, generated when U4 attempts to read from a location being written to by the microprocessor, is ignored. Losing display data for one refresh cycle is insignificant.

2-51. OUTPUT DISPLAY CIRCUITRY

Output display circuitry consists of a custom 2-row, 22-character vacuum-fluorescent display under the control of PLD U5. The circuit contains high voltage grid driver U15, high voltage anode driver U14, a filament switching circuit, and a 1K x 8 (1 KB) dual-port RAM, U2.

The custom display is divided into 24 grids. The 22 characters are made up of fourteen seven-segment digits and eight 14-segment characters.

IC U5 is an EP900 PLD, programmed to provide the timing and control signals for the output display circuitry. Display data written by the microprocessor into the Output Display's dual-port RAM U2, is read by U5 and sent serially to the high voltage anode driver. Both the anode and grid drivers are serial TTL-level input, 32-bit parallel high voltage output devices. Only 31 anode driver outputs and 24 grid driver outputs are used, the remaining high voltage outputs are left unconnected. IC U5 also controls grid timing and display refresh.

A special refresh scheme is used by the Output Display to intensify a specific digit to be displayed. This feature is used by the 5700A when in Error Mode, while editing a value displayed on the Output Display. The digit selected for editing is brighter than the other digits. To accomplish this, U5 monitors data it reads from the dual-port RAM. Following the entry of the fourth data byte to the input registers of the anode driver, the registers are strobed to the high voltage output drivers, then the drivers are enabled. If data bit D7 of the fourth byte is low, the state machine in U5 simply goes on to refresh the next digit at the normal rate of approximately 200 Hz. If, however, bit D7 of the fourth byte is high, the state machine enters a delay routine that adds about 625 us to the normal 5 ms anode and grid on-time, thereby intensifying the digit. Unlike the Control Display, only one grid at a time is turned on.

Output display filament driver circuitry consists of transistors Q7-Q12 and zener diodes VR3 and VR4, plus associated resistors. The transistors are driven by 7406 open-collector drivers U13C and U13D. These drivers are controlled by AOUT and BOUT as in the Control Display. When AOUT is high, U13C turns Q8 and Q10 on. Q10 turns Q12 on, providing a path for the filament current through Q8 and Q12. Zener diode VR4 provides the dc voltage offset necessary for proper filament operation. Then when BOUT is high, U13D turns Q7 and Q9 on. Q7 turns Q11 on, providing a path for the filament current through Q9 and Q11, effectively reversing the direction of the voltage driving the filament. Zener diode VR3 provides the dc voltage offset necessary for proper filament operation.

Dual-port RAM U2 contains all the Output Display data written by the 68HC000 microprocessor on the CPU board. U5 contains a 7-bit address counter which U5 uses to read the contents of U2. U2 provides a BUSY0 signal to U3, which is active low whenever the CPU and U5 try to access the same RAM location at the same time. If the microprocessor attempts to write to the same RAM location U5 is reading as it refreshes the Control Display, U3 uses BUSY0 to hold off DTACK to the microprocessor. This prevents written data from being lost. The other busy signal, generated when U5 attempts to read from a location being written to by the microprocessor, is ignored. Losing display data for one refresh cycle is insignificant.

IC U5 also generates the FPINTR* (front panel interrupt, active low) signal sent to the 68HC000 microprocessor, telling it there is an encoder or keyboard interrupt. The interrupt inputs to U5, ENCODERINTR (encoder interrupt, active high) and KEYBOARDINTR (keyboard interrupt, active high), are generated by PLDs U24 and U9 respectively.

2-52. KEYBOARD SCANNER CIRCUITRY

The key matrix is scanned by PLD U9. It sequentially drives one of the eight columns for about 2.2 ms, then reads all six rows of the matrix on each column scan. When a key is pressed and the column associated with that key is scanned, the row associated with that key goes low. If the key is still pressed after a 6.6 ms debounce period, U9 generates signal KEYBOARDINTR. This signal goes to U5 where it generates FPINTR*, which interrupts the 68HC000 microprocessor. The microprocessor generates KEYBOARDCS* through PLD U3, causing U9 to output encoded row and column data on the data bus for the microprocessor to read. This also resets the keyboard interrupt.

The microprocessor controls the speaker, also referred to as the beeper. Writing a logic high on data line D6 to U9 enables the speaker, writing a logic low on D6 disables the speaker. When enabled, a 900 Hz square-wave signal generated by U8 is gated out to the speaker through U9.

2-53. KNOB ENCODER CIRCUITRY

Knob encoder circuitry consists of PLD U24 and resistors R22, R23, R26, and R27. The resistors configure the U24 knob inputs as Schmitt trigger inputs, with approximately 400 mV of hysteresis. The Schmitt inputs receive the two quadrature signals from the optical shaft encoders at the knob, and remove digital bounce that can result from slowly rotating the knob. The state machine inside U24 uses these signals to determine direction and amount of rotation.

A feature was incorporated to allow the operator to quickly spin the knob and allow the 5700A to properly track it in spite of the inherent delay servicing the interrupt. Every time the operator moves the knob through a 180° rotation of a single detent, U24 generates ENCODERINTR which is sent to U5. IC U5 then generates FPINTR*, interrupting the 68HC000 microprocessor. The microprocessor services the encoder interrupt by reading U24. On a read, indicated by a logic low on ENCODERCS*, U24 places the contents of a seven-bit up/down counter on the data bus. The counter keeps track of the number of 180° rotations that have occurred between the time the interrupt was first initiated and the counter is read. The counter is incremented or decremented depending on the direction of rotation. Signal ENCODERRESET*, generated by U3 on a write to the front panel encoder address space, clears the encoder interrupt.

2-54. LED CIRCUITRY

The LED circuit controls the four light-emitting diodes mounted on the keyboard assembly. It includes a 74LS373 8-bit latch (U10), and four resistors (R16-R19). The respective LEDs light when the following states are active: external sense (EX SNS), external guard (EX GRD), the wideband module is active (WBND), or when an attached 5725A Amplifier is active (BOOST).

Latch (U10) is controlled by the LED_LATCH_EN signal from the decoding PLD U3. Signal LED_LATCH_EN latches the CPU data bus into the internal latches of U10 on a write to the front panel LED memory space. This data appears at the output when control line LEDENABLE* goes low. Control line LED_OUTPUT_CNTRL from U3 is inverted by U11C to create LEDENABLE*. Table 2-7 shows which line activates each LED.

Table 2-7. Control Lines for the Keyboard LEDs

KEYBOARD LED	CONTROL LINES
EX SNS	LED1A
EX GRD	LED2A
W BND	LED2B
BOOST	LED1B

2-55. Keyboard Assembly (A1)

The Keyboard assembly provides the operator with front panel control of the 5700A Calibrator. It connects to the Front Panel assembly (A2) through a cable, and includes an elastomeric keypad, four LEDs, and a rotary encoder (output adjustment) knob.

The elastomeric keypad and the printed circuit board form a 45-switch keyboard arranged in eight columns and six rows. The keyboard scanner circuit on the Front Panel assembly sequentially drives columns one through eight. When a key is pressed, a low appears on the corresponding row as the key's column is scanned. The keyboard scanner circuit encodes the key's row and column location, then takes appropriate action.

The four LEDs (CR1-CR4) are controlled by the LED driver circuit on the Front Panel assembly. LED CR1 is turned on by LED1A when external sensing is selected. LED CR2 is turned on by LED2A when external guard is selected. LED CR3 is turned on by LED2B when the wideband module is active. LED CR4 is turned on by LED1B when an attached 5725A Amplifier is active.

The rotary output adjustment knob activates UUT "Error Mode", allowing the operator to adjust the 5700A output. It can also control the phase shift for variable phase output. The knob assembly consists of two optocouplers (DT1 and DT2) and a magnetically-detented rotary knob. As the knob is turned, optocoupler DT1 generates a pulse signal on ENCODERA and optocoupler DT2 generates a pulse signal on ENCODERB. These signals are routed to the Front Panel assembly where knob encoder circuitry interprets these signals and takes appropriate action. The current-limiting resistor for LEDs within DT1 and DT2 is located on the Front Panel assembly.

2-56. ANALOG SECTION DETAILED CIRCUIT DESCRIPTION

Detailed descriptions of each assembly in the analog section are provided here. Simplified schematics are provided to supplement the text.

2-57. Filter/PA Supply (A18), Low-Voltage Filter/Regulator Section

The Filter assembly receives various ac inputs from the main power transformer and provides unregulated dc to the Regulator/Guard Crossing assembly (A17), and regulated dc supplies +5FR1, -18FR1, and -5FR2 to the DAC assembly. The unregulated supplies are listed in Table 2-8 and the regulated supplies are listed in Table 2-9.

Table 2-8. Unregulated Supplies from the Filter Assembly

SIGNAL NAME	NOMINAL OUTPUT	TOLERANCE	MAX. P-P RIPPLE	RATED OUTPUT	TEST POINT
+15 OSCR	27V	±8V	2V	200 mA	TP2
-15 OSCR	27V	±8V	2V	200 mA	TP5
OSC COM	RETURN				TP4
+5 LHR	12V	±4V	3V	3.5A	TP1
-5 LHR	12V	±4V	2V	400 mA	TP6
LH COM	RETURN				TP3
+44 SR	60V	±15V	3V	155 mA	TP7
-44 SR	60V	±15V	3V	460 mA	TP9
44 S COM	RETURN		SEE NOTE BELOW		TP22
+17 SR	27V	±8V	3V	1.3A	TP10
-17 SR	27V	±8V	3V	1.3A	TP14
17 S COM	RETURN				TP12
+5 FR1R	12V	±4V	2V	400 mA	TP17
-18 FR1R	27V	±8V	2V	50 mA	TP20
FR1 COM	RETURN				TP19
+30 FR1R	50V	±15V	3V	85 mA	TP15
FR1R COM	RETURN				TP16
+30 FR2R		±15V	3V	85 mA	TP8
FR2 COM	RETURN				TP11

NOTE: 44 S COM and 17 S COM are tied together on the Regulator/Guard Crossing assembly (A17).

Table 2-9. Regulated Supplies from the Filter/PA Supply

Signal Name	Nominal Output	Tolerance	Current Limit	Rated Output	Test Point
-5 FR2	-5V	±0.3V	0.15A	0.03A	TP13
FR2 COM	RETURN				TP11
+5 FR1	+5V	±0.3V	2A	0.1A	TP18
-18 FR1	-18V	±0.9V	2A	0.05A	TP21
FR1 COM	RETURN				TP19

2-58. UNREGULATED OSC SUPPLIES

Line OSC COM is the return path for the +15 OSCR and -15 OSCR supplies. These supplies use a full-wave center-tapped configuration. They consist of bridge rectifier CR3 and two filter capacitors, C4 and C6, for +15 OSCR and -15 OSCR, respectively. Inputs are fused with 1.6A slow-blow fuses F1 and F2.

2-59. UNREGULATED LH SUPPLIES

Line 5 LH COM is the return path for the +5 LHR and -5 LHR supplies. These supplies use a full-wave center-tapped configuration, and consist of four diodes (CR1, CR2, CR4, CR5) configured as a bridge rectifier.

Capacitors C2 and C3 filter +5 LHR, and C5 filters -5 LHR. Capacitor C1 reduces the level of generated transients.

2-60. UNREGULATED S SUPPLIES

The ±44 SR supplies use full-wave center-tapped rectifiers. Bridge rectifier CR6 is followed by two filter capacitors C7 and C8 for the +44 SR and -44 SR supplies, respectively. Inputs are fused by 0.5A slow blow fuses, F3 and F5. The ±17 SR supplies also are full-wave center-tapped, consisting of four diodes (CR8, CR10, CR12, CR13) configured as a bridge rectifier. Capacitors C13 and C14 filter the +17 SR supply, while C15 and C16 filter the -17 SR supply.

2-61. TRIAC CIRCUIT

The triac circuit protects the 5700A if it is inadvertently plugged into an excessively high line voltage. For example, it protects the 5700A if it is plugged into a 230V line when the rear panel line voltage select switches are set for 115V operation.

This circuit contains triac CR19, zener diodes VR20, VR21, resistor R1, and capacitor C23. The zener diodes set a trip voltage of 82V. If the ac voltage across the main transformer secondary for the ±17V supply exceeds 82V, the triac fires, shorting out the winding, which causes the main transformer primary fuse to blow.

2-62. FR1 SUPPLIES

Line FR1 COM is the return path for the unregulated +5 FR1R raw supply and the regulated +5 FR1, and -18 FR1 supplies. Each supply uses a full-wave bridge configuration.

The unregulated +5 FR1R supply consists of bridge rectifier CR15 and filter capacitor C19. The input is fused with 1.6A slow-blow fuse F8. The regulated +5 FR1 supply uses the unregulated +5 FR1R supply and contains regulator U2, filter capacitor C20, and protection diode CR16.

The -18 FR1 supply consists of bridge rectifier CR17 and filter capacitor C21. Its input is fused with 0.5A slow-blow fuse F9. The regulated -18 FR1 supply uses the unregulated -18 FR1 supply and contains regulator U3, filter capacitor C22, and protection diode CR18.

2-63. UNREGULATED FR1 SUPPLY

FR1R COM is the return path for the unregulated +30 FR1 supply. This supply uses full-wave bridge rectifier CR14 and filter capacitor C18. Its input is fused with 0.5A slow-blow fuse F7.

2-64. FR2 SUPPLIES

FR2 COM is the return path for unregulated +30 FR2R supply and regulated -5 FR2 supply. Each supply uses a full-wave, bridge configuration. The unregulated +30 FR2R supply consists of bridge rectifier CR7 and filter capacitor C9. Its input is fused with 0.5A slow-blow fuse F4. The -5 FR2 supply consists of bridge rectifier CR11, filter capacitor C11, regulator U1, bypass capacitor C12, and protection diode CR9. The input is fused with 315 mA slow-blow fuse F6.

2-65. Filter/PA Supply (A18), Power Amplifier Output Supply Section

The power amplifier output power supply section of the Filter/PA Supply assembly (A18) receives ac voltage from the main power transformer to generate power supplies +PA and -PA for the output stage of the Power Amplifier assembly (A16). These two power supplies can be switched between the following three modes of operation, depending on the needs of the Power Amplifier.

- o +PA and -PA to ±185V respectively.
- o +PA and -PA to ±365V respectively.
- o +PA and -PA are both turned off.

Figure 2-6 is a simplified schematic for the Power Amplifier Supply section of this assembly.

2-66. ±PA SUPPLIES DIGITAL CONTROL

Circuitry to control the three modes of operation of the +PA and -PA supplies is located on the Power Amplifier Digital Control SIP assembly (A16A1). This SIP assembly is mounted on the main Power Amplifier assembly (A16). Not on the assembly is the quad comparator U201.

The main Power Amplifier assembly generates four control lines:

- o +HI/LO V
- o LO/HI I
- o +ON/OFF
- o H/LV S

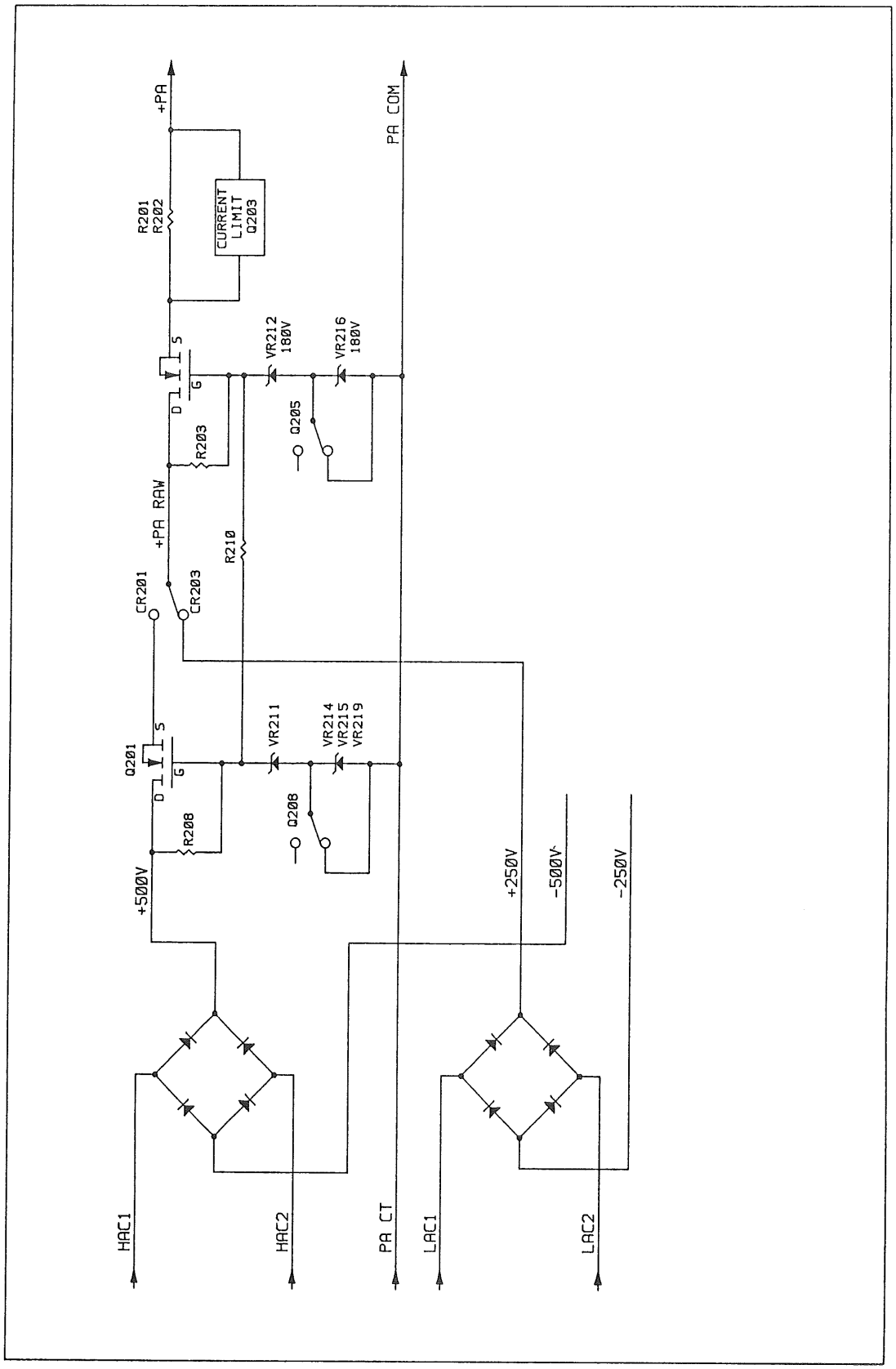


Figure 2-6. Power Amplifier Supply Simplified Schematic

Component Z201 pulls these signals up. At calibrator power up, the ±PA supply is off. The Power Amplifier Digital Control SIP (A16A1) selectively pulls these control lines low to achieve the two modes of operation. Pulling control lines +HI/LO V and +ON/OFF low sets the +PA supply to +365V. Releasing +HI/LO V changes the +PA supply to 185V.

The comparator (U201) provides level shifting to control the PMOSFETS in the -PA circuit in a similar way. Signal -ON/OFF is generated from +ON/OFF, and -HI/LO V from -H/LV. Control line +LO/HI I switches transistor Q217 which controls relay K201. Relay K201 selects the current limit for both +PA and -PA supplies.

2-67. ±250V AND ±500V SUPPLIES

Input signals PA CT, PA HAC1, PA HAC2, PA LAC1, and PA LAC2 come from the main transformer.

- o PA CT is the center tap.
- o PA HAC1 and PA HAC2 are high voltage taps with approximately 400V rms and are fused by F201 and F204 respectively.
- o PA LAC1 and PA LAC2 are lower voltage taps with approximately 200V rms and are fused by F202 and F203 respectively.
- o PA LAC1 and PA LAC2 and bridge rectifier CR222 generate the unregulated ±250V supplies.
- o PA HAC1 and PA HAC2 and diodes CR217, CR218, CR220, CR221, CR223, CR224, CR227, and CR228 are in a bridge rectifier configuration to generate the unregulated ±500V supplies.

When the PA supply outputs ±185V, current is drawn only from the lower voltage taps LAC1 and LAC2.

2-68. +PA AND -PA SUPPLIES

Unregulated voltage for +PA is selected between the +250V and +500V unregulated supplies by control line +HI/LO V and diodes CR201, CR203, CR208, and CR210.

Transistor Q204 is a current source that biases VR212 and VR216.

Supply +PA is +185V when the +HI/LO V signal is above 3V. (Transistors Q205 and Q208 are turned on.) Transistor Q205 shorts VR216, while Q208 places a short across VR214, VR215, and VR219. A voltage of +185V appears at the gate of Q202 because of VR212. Approximately 140V appears at the gate of Q201. This 140V and about 250V at the anode of CR208 reverse biases CR201 and CR210, thereby shutting off Q201. Current flows out of the 250V unregulated supply through CR203 and Q202. Regulated supply voltage +PA is determined by the gate voltage of Q202, which is about 190V when +HI/LO V is above 3V.

When +HI/LO V is close to 0V, both Q208 and Q205 are turned off, and over 400V appears at the gate of Q201. CR203 and CR208 are reverse biased, and the supply current flows from the +500V unregulated supply through Q201, CR201, and Q202. The gate voltage of Q202 is approximately 370V, nearly the same as +PA.

The -PA side works exactly like the +PA side except -PA is switched between -185V and -365V by control line -HI/LO V.

The ±PA supplies can be replaced by the ±44SR unregulated supplies by moving switch S201 switched towards the top edge of the board. This feature provides the means to troubleshoot the Power Amplifier using reduced voltages.

NOTE

Make sure S201 is returned to the ±PA position before resuming normal operation.

2-69. ±PA SUPPLY CURRENT LIMIT

The current limit for both the +PA and -PA supplies is set to either about 90 mA (K201 de-energized) or 150 mA (K201 energized) by K201. Control line +LO/HI I controls relay K201. The high-current mode (150 mA) is used during operation in the 1100V dc range and the 2.2A range.

Output current on the +PA side is sensed between the emitter and base of Q203 by R202 and/or R201. Supply +PA shuts off to near 0V when enough current is flowing through +PA to forward-bias Q203. Then, current though Q203 charges capacitor C209 through R214 to a voltage above the threshold voltage at the inverting input of comparator U201C. The overcurrent condition must persist for about 75 ms for C209 to charge above the threshold. The output of U201 goes high, turning on Q207. This forces the zener diode bias current to flow through Q207 instead of VR212 or VR216, leaving only a few volts at the gate of Q202, thus shutting +PA off. The output of U201C also saturates Q218 and reduces the comparator threshold voltage to near 0V. This provides the comparator with hysteresis; C209 has to discharge close to 0V before +PA can turn on again. The +PA supply cycles on and off as long as the overcurrent condition exists.

Transistor Q206 provides another current limit. While otherwise similar to the Q203 limit, the Q206 current limit turns on at 0.5A and turns off immediately without any delay. The Q206 limit thereby protects the supply under short circuit conditions.

Current limiting on the -PA side works similarly to the +PA side with one difference. That is that shutoff of -PA can happen under two circumstances:

- o -PA is loaded beyond its current limit.
- o +PA is shut off. (Shut off of -PA is slaved to shut off of +PA.)

2-70. Regulator/Guard Crossing Assembly (A17)

The Regulator/Guard Crossing assembly (A17) provides two separate functions: voltage regulation for the analog power supplies, and digital control of the guard crossing. The voltage regulation portion is described first followed by the digital control portion. Refer to the schematic diagrams for the Regulator/Guard Crossing Assembly for this discussion.

2-71. VOLTAGE REGULATOR CIRCUITRY

The regulator circuit receives unregulated dc from the regulator filter circuit on the Filter/PA Supply assembly (A18) and provides 13 regulated dc outputs and 1 unregulated dc output for the various analog assemblies. Table 2-10 lists the regulated supplies from the Regulator/Guard Crossing Assembly.

Table 2-10. Regulated Outputs from the Regulator/Guard Crossing Assembly

SIGNAL NAME	NOMINAL OUTPUT	TOLERANCE	CURRENT LIMIT	RATED OUTPUT	TEST POINT
+15 OSC	+15V	±800 mV	2A	200 mA	TP3
-15 OSC	-15V	±800 mV	2A	200 mA	TP5
+5RLH	+5.975V	±425 mV	2A	600 mA	TP14
+5LH	+5.1V	±300 mV	2A	600 mA	TP11
-5LH	-5V	±300 mV	2A	400 mA	TP15
+44S	+44.15V	±2.03V	0.5A	140 mA	TP13
-44S	-44.15V	±2.03V	0.5A	140 mA	TP16
+17S	+17.475V	±475 mV	4A	1.0A	TP8
-17S	-17.865V	±835 mV	6A	1.0A	TP12
+15S	+15V	±800 mV	2A	300 mA	TP18
-15S	-15V	±800 mV	2A	300 mA	TP19
+30FR1	+30.96V	±1.7V	1A	85 mA	TP2
+30FR2	+30.96V	±1.7V	1A	85 mA	TP7

2-72. REGULATED OSC SUPPLIES

The +15 OSC and -15 OSC supplies are used exclusively by the Oscillator Output (A12) and Oscillator Control (A13) assemblies. OSC COM is the return path for these supplies. The +15 OSC uses the unregulated +15 OSCR from the Filter assembly and consists of three-terminal TO-220 regulator U2 with heat sink, bypass capacitors C1 and C2, and protection diodes CR2 and CR3. The -15 OSC uses the unregulated -15 OSCR from the Filter assembly and consists of three-terminal TO-220 regulator U3 with heat sink, bypass capacitors C4 and C5, and protection diodes CR5 and CR7. Capacitors C2 and C5 improve the stability of U2 and U3 respectively. Diodes CR3 and CR5 protect U2 and U3 from reverse voltages. Diodes CR2 and CR7 protect U2 and U3 from input shorts.

2-73. REGULATED LH SUPPLIES

LH COM is the return path for the +5RLH, +5LH, -5LH and +8RLH supplies. The +5RLH, +8RLH, and +5LH supplies use the unregulated +5LHR supply from the Filter assembly. The +5RLH supply uses three-terminal TO-3 regulator U11 with heat sink, bypass capacitors C20 and C21, protection diodes CR17 and CR20, and the diode combination of CR34 and CR35. The +5LH supply uses three-terminal TO-3 regulator U8 with heat sink, bypass capacitor C16, protection diodes CR14 and CR16, and resistor R13. The -5LH supply uses the unregulated -5LHR from the Filter assembly and consists of three-terminal TO-220 regulator U12 with heat sink, bypass capacitors C23 and C24, and protection diodes CR21 and CR24. Capacitors C16, C21, and C24 improve the stability of U8, U11, and U12 respectively. Diodes CR14, CR17, and CR24 protect the regulators from input shorts. Diodes CR16, CR20, and CR21 protect the regulators from reverse voltage. Resistor R13 and diodes CR34 and CR35 increase the output of regulators U8 and U11. The unregulated +8RLH supply is generated by fusing the unregulated +5LHR supply from the Filter assembly with 3.15A slow-blow fuse F1.

2-74. REGULATED S SUPPLIES

Line S COM is the return path for the +44S, -44S, +17S, -17S, +15S and -15S supplies. Line S COM is also connected to LH COM. The +44S supply uses the unregulated +44SR from the Filter assembly. This supply uses three-terminal TO-39 regulator U10, Q2, VR3, VR4, VR5, R20, R14, R15, CR18, CR19, CR25, C17, C18, C19, C65, PTC resistor R60. The regulator IC (U10) provides the current and thermal limiting. Its regulated output voltage is set by R14 and R15, yielding a nominal output of +44.15V. Components Q2, R20, VR3 and VR4 act as an emitter follower to protect the regulator against a potentially excessive input-output voltage differential in the event of a short circuit. Capacitor C65 filters this voltage to the regulator. Diodes CR19 and CR25 protect the regulator against shorts at the input, while CR18 protects the regulated output from reverse voltage. Capacitors C17 and C18 are for bypass. Capacitor C19 improves rejection of input variations. Components U10 and Q2 have heat sinks to provide thermal protection for both normal and short-circuit conditions. The regulator is shunted by R60 and VR5, which normally pass 28 mA of current to remove the power from the regulator.

In an output short condition, the value of the PTC increases, limiting current through the device to less than 17 mA at 25oC.

The -44S supply uses the unregulated -44SR supply from the Filter assembly. This supply uses three-terminal TO-39 regulator U13, Q1, VR1, VR2, VR6, R17, R18, R19, PTC Resistor R61, CR22, CR23, CR32, CR33, C22, C25, C26, and C66. The regulator IC, U13, provides the current and thermal limiting. Its regulated output voltage is set by R17 and R18, yielding a nominal output of -44.15V. Components Q1, R19, VR1, VR2 and CR32 act as an emitter follower and protect the regulator against a potentially excessive input-output voltage differential if a short circuit occurs. Capacitor C66 filters the voltage to the regulator. The regulator is shunted by R61 and VR6, which pass 28 mA. In an output short condition, the value of the PTC increases, limiting current through the device to less than 17 mA at 25°C.

Diode CR32 removes VR2 from the circuit in a shorted condition to meet U13's input-output differential specifications. Diodes CR22 and CR33 protect the regulator against shorts at the output, while CR23 protects the regulated output from reverse voltage. Capacitors C25 and C26 are for bypass. Capacitor C22 improves rejection of any input variations. The heat sink on regulator U13 guarantees thermal protection for both normal and short-circuit operating conditions.

The +17S supply uses the unregulated +17SR supply from the Filter assembly. This supply uses three-terminal TO-3 regulator U6 with heat sink, and R5 and R6. The output voltage is set by resistors R5 and R6 in the same manner as the +44S supply. Capacitors C8 and C9 are for bypass. Capacitor C11 improves ripple rejection. Diodes CR8 and CR26 protect the regulator against shorts at the input, while CR11 protects the regulated output from reverse voltage.

The -17S supply uses the unregulated -17SR supply from the Filter assembly. It uses three-terminal TO-3 regulator U7 and R10 and R11. The output voltage is set by resistors R10 and R11 in the same manner as the -44S supply. Capacitors C13 and C15 are for bypass. Capacitor C14 improves ripple rejection. Diodes CR15 and CR27 protect the regulator against shorts at the input, while CR13 protects the regulated output from reverse voltage.

The +15S supply uses the unregulated +17SR supply from the Filter assembly. It consists of +15V three-terminal TO-220 regulator U4. Capacitor C27 is required for the stability of U4. Diode CR28 protects the regulator against shorts at the input, while CR29 protects the regulated output from reverse voltage.

The -15S supply uses the unregulated -17SR supply from the Filter assembly. It consists of -15V three-terminal TO-220 regulator U9. Capacitor C29 stabilizes U9. Diode CR31 protects the regulator against shorts at the output, while CR30 protects the regulated output from reverse voltage.

2-75. FR1 SUPPLY

FR1 COM is the return path for the +30FR1 supply. This supply uses the unregulated +30FR1R supply from the Filter assembly and consists of three-terminal TO-39 regulator U1 with heat sink, bypass capacitors C3 and C6 and protection diodes CR1, CR4, and CR6. Resistors R1 and R2 set the output voltage in the same manner as the +44S supply. Capacitor C7 improves ripple rejection. Diodes CR1 and CR4 protect U1 against input shorts, while CR6 protects against reverse voltage.

2-76. FR2 SUPPLY

FR2 COM is the return path for the +30FR2 supply. This supply uses the unregulated +30FR2R supply from the filter assembly and consists of three-terminal TO-39 regulator U5 with heat sink, bypass capacitors C10 and C28, and protection diodes CR9, CR10, and CR12. Resistors R4 and R8 set the output voltage in the same manner as the +44S supply. Capacitor C12 improves ripple rejection. Diodes CR9 and CR10 protect U5 against input shorts, while CR12 protects against reverse voltage.

2-77. GUARDED DIGITAL CONTROL CIRCUITRY

The Inguard CPU controls all the analog assemblies. It communicates with the Unguarded CPU assembly (A20) through a serial fiber-optic link. The Inguard CPU is a Hitachi 637A01Y0 CMOS microcontroller (U56) with 16K x 8 bit (16 KB, or 16 kilobyte) internal CMOS EPROM. Support circuitry includes 8K x 8 bits (8 KB) of external CMOS static RAM, watchdog timer circuitry, reset and power glitch detect circuitry, test switches, a serial fiber-optic link to the unguarded CPU, and decoders and buffers to interface to the guarded digital bus. The assembly also generates an 8 MHz sine wave for use by some of the analog assemblies.

2-78. Inguard CPU Memory Map

Table 2-11 shows the memory map of the Inguard processor.

2-79. Inguard Memory Configuration

The microcontroller (U56) has 16 KB (kilobytes) of internal EPROM program memory. IC U62 provides 8 KB of external static CMOS RAM, with a jumper option for a plug-in replacement with a 2 KB device.

2-80. Inguard Clock Circuit

This circuit uses 8 MHz crystal Y52 and step-down transformer T51 to generate a low-level (200 mV p-p) 8 MHz clock used by other guarded assemblies throughout the calibrator. Transformer (T51) has a center-tapped secondary, and provides CLK COM, CLK and CLK*. The CLK and CLK* sine-wave signals are sent to certain analog assemblies where they are converted into square wave clock signals for timing purposes.

Table 2-11. Inguard CPU Memory Map

ADDRESS SPACE (HEX)	NAME	USE
0000 - 0027		Internal Registers on the 6301
0028 - 003F		Unused memory space
0040 - 013F		Internal RAM 256 Bytes
0140 - 3FFF		Unused memory space
4000 - 4007	CS0*	Wideband Output (A5)
4008 - 400F	CS1*	Current/Hi-Res (A7)
4010 - 4017	CS2*	Switch Matrix (A8)
4018 - 401F	CS3*	Ohms Cal (A9)
4020 - 4027	CS4*	Unused
4028 - 402F	CS5*	DAC (A11)
4030 - 4037	CS6*	DAC (A11)
4038 - 403F	CS7*	Current/Hi-Res (A7)
4040 - 4047	CS8*	Oscillator Control (A12)
4048 - 404F	CS9*	Oscillator Output (A13)
4050 - 4057	CS10*	High Voltage Control (A14)
4058 - 405F	CS11*	Power Amplifier (A16)
4060 - 4067	CS12*	Rear Panel (A21) Boost
4068 - 406F	CS13*	Current/Hi-Res (A7)
4070 - 4077	CS14*	Wideband Oscillator (A6)
4078 - 407F	CS15*	Unused
4080 - 5FFF		Unused(memory overlay of 4000-407F)
6000 - 9FFF		Unused
A000 - BFFF		External RAM
C000 - FFFF		Internal ROM or EPROM

2-81. Inguard Watchdog Timer

The watchdog timer circuit uses a 74HC4020 (U59) and part of Programmable Logic Device (PLD) U58. The microcontroller (U56) generates a 19.2 kHz square wave (SCLK) on pin 11. The frequency of this clock is the same as the baud rate of the serial interface. Once the clock frequency is initialized, it runs without software supervision. This clock drives U59, which divides by 16384 to obtain a logic low interval of 427 ms followed by a logic high interval of 427 ms. The output of the U59, POPIN, goes to the PLD, which asserts POP to the analog hardware and NMIPOP* to the processor if U59 is not reset every 427 ms. The PLD also asserts POP on power-up and on any hardware reset. In order to prevent POP and NMIPOP*, the watchdog counter must be reset by reading or writing any analog hardware, or by toggling the POPCLRL line. The POPCLRL line is also used to disable the watchdog by going low.

2-82. Power-Up and Reset Circuitry

This circuit consists of U60, SW51, C55, C56, R52, and Z51. The line monitor chip (U60) detects three events: the power supply falling below 4.5V, reset being initiated by closure of momentary contact switch SW51, or BREAK being asserted from the break detection circuitry. If any of these conditions occurs, U60 resets the board for 130 ms. Pin 5 of U60 is an open-collector output, pulled high by pin 12 of Z51.

2-83. Break Detection

The break-detect circuit acts as a serial communications break detector enabling the CPU assembly (A20) to reset U56 and U58 via the power-up and reset circuitry. This break-detect circuit uses a 74HC4020 binary counter (U63) and an inverter U51C. The microcontroller (U56) outputs the 1.2288 MHz ECLK clock on pin 64. This signal clocks U63, which in turn divides the signal by 16,384 to produce successive logic low and high intervals (each of 6.67 ms) at the BREAK output (U63, pin 3). Under normal conditions the RCV (receive) line is high to hold U63 clear. The main 68HC000 CPU can force a reset of the Guard Crossing over the fiber-optic link by holding RCV low for more than 6.67 ms, which causes BREAK to go high. BREAK, inverted by U51C, is used by the reset circuitry to force a Guard Crossing reset via RESET*.

2-84. Fiber-Optic Link to CPU

Guarded digital and analog circuits are isolated from the unguarded CPU assembly (A20) by a fiber-optic link that asynchronously transmits serial data. On the transmit side, the microcontroller transmit output (XMT) controls a 75451 (U57) which drives fiber-optic transmitter J72 mounted on the Analog Motherboard. Receive signal RCV comes from fiber-optic receiver J71 also mounted on the Analog Motherboard. The receiver converts the light signal to TTL levels that become the RCV signal at the microcontroller. A fiber-optic cable links the fiber-optic transmitter on the Analog Motherboard to the fiber-optic receiver on the Digital Motherboard. Another fiber-optic cable links the other receiver/transmitter pair on the motherboards.

2-85. Interface to Guarded Digital Bus

The interface to the guarded digital bus consists of a 74HCT245 (U55), a 74HCT244 (U52), two 74HC137s (U53 and U54), inverters U51B and U51D, resistor packs Z52, Z53, and Z54, and the POP line from U58. U52A and U52B buffer various control and address lines. Resistors from Z52 pull the lines of U52A to desired inactive states when BUSEN* is at a logic high, disabling the bus. U55 is a bi-directional data bus buffer (D0-D7). Resistor packs Z53 and Z54 match the lines of the buffered data bus, reducing reflected noise. ICs U53, U54, and U51D perform a 4-to-16 decode of address lines A3-A6, generating 16 chip-select lines (CS0*-CS15*) on the guarded digital bus. These 16 signals select the various assemblies on the Analog Motherboard. U51B buffers and inverts the INT interrupt signal from the DAC assembly. The POP signal from U58 is a reset line sent to the analog assemblies.

2-86. Inguard CPU Interrupts

The Inguard CPU microprocessor handles many different interrupts. These are listed in Table 2-12 in order of priority with the highest priority interrupts first.

Table 2-12. Inguard CPU Interrupts

VECTOR MSB	VECTOR LSB	INTERRUPT	DESCRIPTION
FFFE	FFFF	*RES	Power Up Reset
FFEE	FFEF	TRAP	Address error or op code error
FFFC	FFFD	!NMI	Non maskable interrupt (NMIPOPL)
FFFA	FFFB	SWI	UNUSED
FFF8	FFF9	!IRQ1	!IRQ1,ISF (A/DINTL)
FFF6	FFF7	ICI	Timer 1 input capture (unused)
FFF4	FFF5	OCI	Timer 1 output compare 1,2 (unused)
FFF2	FFF3	TOI	Timer 1 overflow (unused)
FFEC	FFED	CMI	Timer 2 counter match
FFEA	FFEB	!IRQ2	UNUSED
FFF0	FFF1	SIO	RDRF + ORFE + TDRE + PER

RDRF - Receive Data Register Full
ORFE - Overrun Framing Error
TDRE - Transmit Data Register Empty
PER - Parity Error

2-87. Switch Matrix Assembly (A8)

The Switch Matrix Assembly does the following tasks:

- Coordinates the flow of signals from each analog assembly (excepting the Wideband AC Module (Option -03)) to the calibrator's binding posts. This communication determines the calibrator's range.
- Coordinates the connection of various analog and digital common lines during operate, standby, and calibration modes.
- Controls such binding post functions as operate/standby, internal/external sense, and internal/external guard.
- Provides an internal cal zero amplifier used in the calibration of offsets for all dcv ranges (except the 1100V range).

The Switch Matrix Assembly consists of 33 latching type, two- and four-pole relays. The relays are driven by special driver chips, which are controlled by the assembly's 24-output 82C55 chip. The Switch Matrix also contains the 5700A-4HR1 Temperature-Controlled Precision DC Amplifier Hybrid and RNET assembly, which is used when the calibrator is in the dc 2.2V or 220 mV range. The resistor network also is used to create resistive dividers to generate the ac or dc 220 mV, ac 22 mV, and ac 2 mV ranges. Additional analog circuitry in the Switch Matrix Assembly includes the dc 2.2V range output stage, the internal cal zero amplifier, FETs to support assembly calibration, assembly diagnostics, and circuitry to control some of the motherboard relays.

2-88. SWITCH MATRIX DIGITAL CONTROL

Refer to sheet four of the 5700A-1020 schematic diagram during the following discussion. The heart of the Switch Matrix digital control circuitry is an 82C55 Programmable Peripheral Interface IC (U1) under software control via the guarded digital bus. This IC has three ports that generate 24 outputs. These outputs are used to control eight UCN5801 Latching Driver ICs (U5-U12) controlling all Switch Matrix latching relays, one UCN5801 Latching Driver (U13) controlling the 10 non-latching relays on the Motherboard, a 4028 decoder (U2), five FET switches (Q6-Q7, Q9-Q11), and an analog multiplexer (U4) for self diagnostics.

Eight UCN5801 latching driver ICs (U5-U12) drive Switch Matrix latching relays. Port A (PA0-PA7) from U1 provides a common input bus. Each driver chip has a separate strobe line. A 4028 decoder (U2) generates strobe lines U5STB-U13STB for strobing U5-U13 respectively. These individual strobe lines are decoded from PB0-PB3 of U1. When a strobe line is selected, the data on the bus is strobed in the respective driver chip. The output enables are controlled directly by PC0-PC3 of U1. One bit of port C enables two drivers. PC0 enables U5 and U6, PC1 enables U7 and U8, PC2 enables U9 and U10, and PC3 enables U11 and U12. By enabling only two driver ICs at a time, excessive power supply current draw is prevented. To insure that the relays are latched properly, the driver chips must be enabled for 10 ms. As an example, the following steps are taken to set up relays in the first bank:

1. Write the proper data for the relays associated with driver U5 (K2, K9, K11, and K15) to port A of the 82C55.

2. Write 0 hex to PB0-PB3 to make U5STB go high. Now write 9 hex to PB0-PB3 to make all strobe lines go low. The data has now been strobed into U5.

3. Write the proper data for the relays associated with U6 (K3, K4, K5, and K24) to port A of the 82C55.

4. Write 1 hex to PB0-PB3 to make U6STB go high. Now write 9 hex to PB0-PB3 to make all strobe lines go low. The data has now been strobed into U6.

5. Write FE hex to port C (PC0 is low), wait 10 ms and write FF hex to port C. This takes the outputs of U5 and U6 out of tri-state and allows the proper relay coils to be energized for 10 ms.

A UCN5801 driver (U13) drives non-latching relays on the Motherboard. The Motherboard non-latching relay supply circuit, as outlined in sections A6 through A8 of the schematic diagram, contains U17, Q1, Q2, CR1, CR2, CR10, and R6-R12. Port A of U1 provides data for this driver (PA0-PA7), and decoder U2 provides the strobe signal. Since this driver controls non-latching relays, the enable is tied to LH COM.

The non-latching relay supply circuit provides approximately 7V to the relays on the Motherboard during pull-in, and approximately 3.5V during normal operation. This voltage is routed to the Motherboard on the RLY+V line. The 7V is needed to insure pull-in while the 3.5V is sufficient to prevent drop out. This cuts relay heating and thermal EMFs. PC5 controls the non-inverting amplifier U17. This amplifier is the control element for Transistor Q1. When PC5 is low, the output is 3.5V, and when PB5 is high, the output is 7V. Components CR1, Q2 and R10-12 form a foldback current limit for the supply. The following steps are taken to select a particular state for Motherboard relays RLY1-RLY10:

1. Write the data corresponding to the desired state to port A (PA0-PA7) of the 82C55 (U1).

2. Strobe the data into U13 by writing 8 hex to PB0-PB3 to make U13STB go high, then a 9 hex to make it go low.

3. Apply 7V to the relay coils by setting PC5 high.

4. Wait approximately 20 ms for the relays to pull in, then reduce the coil voltage to 3.5V by setting PC5 low.

There are five FETs on the Switch Matrix. Q9 and Q10 (sheet 3, C7), which are N-channel JFETs controlled by port B (PB5) of U1, are driven by an LM393 open-collector comparator (U15A) to provide the proper level shifting. DMOS enhancement FETs are used for the remaining three FETs (Q6, Q7, and Q11). Refer to sheet 1, B5 of the schematic diagram. FETs Q6 and Q7 are driven by U1, port B, with a high on PB4 turning on Q6, and a logic high on PB7 turning on Q7. FET Q11 is driven on by a logic high from U1, port C (PC4).

The diagnostic circuit (sheet 4, B7) enables the calibrator to monitor +8RLH, the 2.2V range output voltage, +5RLH, -5LH, +17S, -17S, the assembly temperature (U3), and the OVEN TEMP line from the heated hybrid. OVEN TEMP, +5RLH, -5LH, and +8RLH are divided down by a factor of ten by Z5 and Z6. A 4051 analog multiplexer (U4) is controlled by PA0-PA2 and PC6 from U1. This multiplexer selects which one of these eight voltages is applied to the SDL line, where it is measured by the adc circuit on the DAC assembly (A11).

2-89. SWITCH MATRIX OPERATION: 11V DC AND 22V DC RANGES

Refer to Figure 2-7 for the following discussion. DC 11V and 22V ranges are generated by the DAC assembly and routed directly to the front panel binding posts through relays on the Switch Matrix and Motherboard.

Line DAC HI is connected to INT OUT HI through relays K18B, K27, and K30. INT OUT HI is connected to the OUTPUT HI binding post through relay K1 on the Motherboard. Line DAC SENSE HI is connected to INT SENSE HI through relays K18A, K25, and K26. Motherboard relays K2 and K3 switch INT SENSE HI to the SENSE HI binding post during external sensing, or OUTPUT/SENSE HI during internal sensing.

Lines PA COM and DAC LO are connected by relays K11 and K12, and connected to the OUTPUT LO binding post by relay K10. Switch Matrix relays K14 and K15 connect R COM to the SENSE LO binding post during external sensing, or to OUTPUT/SENSE LO during internal sensing.

2-90. SWITCH MATRIX OPERATION: 2.2V AC AND 22V AC RANGES

Refer to Figure 2-8 for the following discussion. AC 2.2V and 22V ranges are generated by the Oscillator assemblies and routed directly to the front panel binding posts through relays located on the Switch Matrix and Motherboard.

Line OSC OUT is connected to INT OUT HI through relays K19A, K18B, K27, and K30. INT OUT HI is connected to the OUTPUT HI binding post through relay K1 on the Motherboard. Line OSC SENSE is connected to INT SENSE HI through relays K19B, K18A, K25, and K26. Motherboard relays K2 and K3 switch INT SENSE HI to the SENSE HI binding post during external sensing, or OUTPUT/SENSE HI during internal sensing.

Line OSC COM is connected to the OUTPUT LO binding post through relays K11 and K10 on the Switch Matrix. Switch Matrix relays K13 and K15 connect OSC SENSE LO to the SENSE LO binding post during external sensing, or OUTPUT/SENSE LO during internal sensing.

2-91. SWITCH MATRIX OPERATION: 220V AC AND DC RANGES

Refer to Figure 2-9 for the following discussion. In the dc 220V range, PA OUT HI from the Power Amplifier assembly (A16) is routed to the High Voltage Control assembly (A14), where it goes through relay K10 and becomes PA OUT DC. Line PA OUT DC is routed to the Switch Matrix and connected to INT OUT HI through relays K20, K19A, K18B, K27 and K30. Relay K1 on the Motherboard connects INT OUT HI to the OUTPUT HI binding post.

Line PA SENSE DC is connected to INT SENSE HI through relays K20, K19B, K18A, K25, and K26. Motherboard relays K2 and K3 switch INT SENSE HI to the SENSE HI binding post during external sensing, or OUT/SENSE HI during internal sensing. PA COM and DAC LO are connected by relays K11 and K12, and connected to the OUTPUT LO binding post by relay K10. Switch Matrix relays K14 and K15 connect R COM to the SENSE LO binding post during external sensing, or OUTPUT/SENSE LO during internal sensing.

In the ac 220V range, Power Amplifier outputs PA OUT HI and PA SNS AC are routed to the High Voltage Control assembly (A14) where relays K10, K3, and K13 connect them to HV OUT and HV SNS respectively. HV OUT is connected to the OUTPUT HI binding post through relays K9 and K1 on the Motherboard. Motherboard relays K10, K2, and K3 connect HV SNS to the SENSE HI binding post during external sensing, or to OUTPUT/SENSE HI during internal sensing. Connection to the OUTPUT LO and SENSE LO binding posts is done with relays on the Switch Matrix. PA COM is connected to the OUTPUT LO binding post through relays K11 and K10. Switch Matrix Relays K13 and K15 connected OSC SENSE LO to the SENSE LO binding post during external sensing, or OUTPUT/SENSE LO during internal sensing.

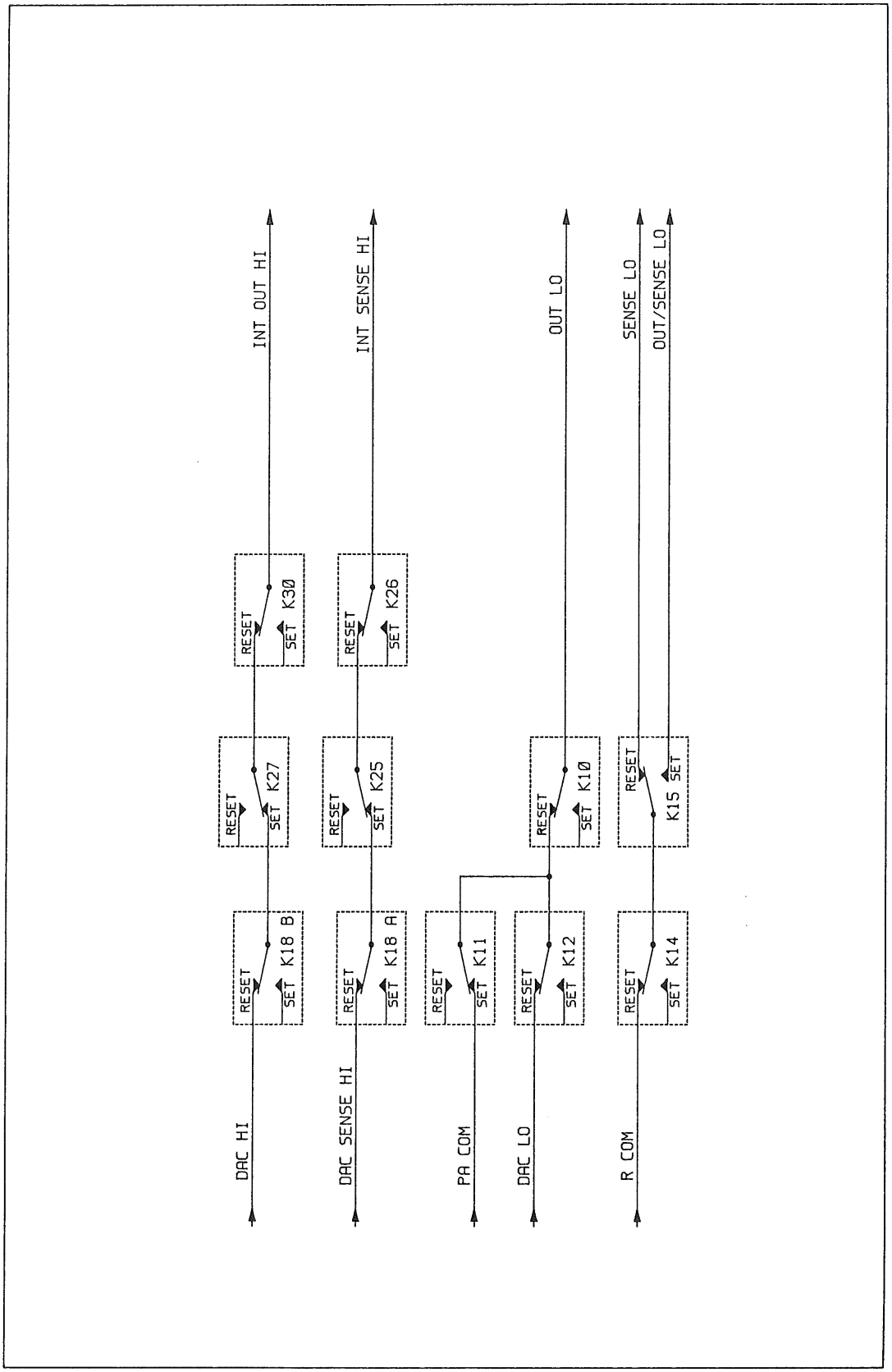


Figure 2-7. Switch Matrix Configuration for 11V dc and 22V dc Ranges

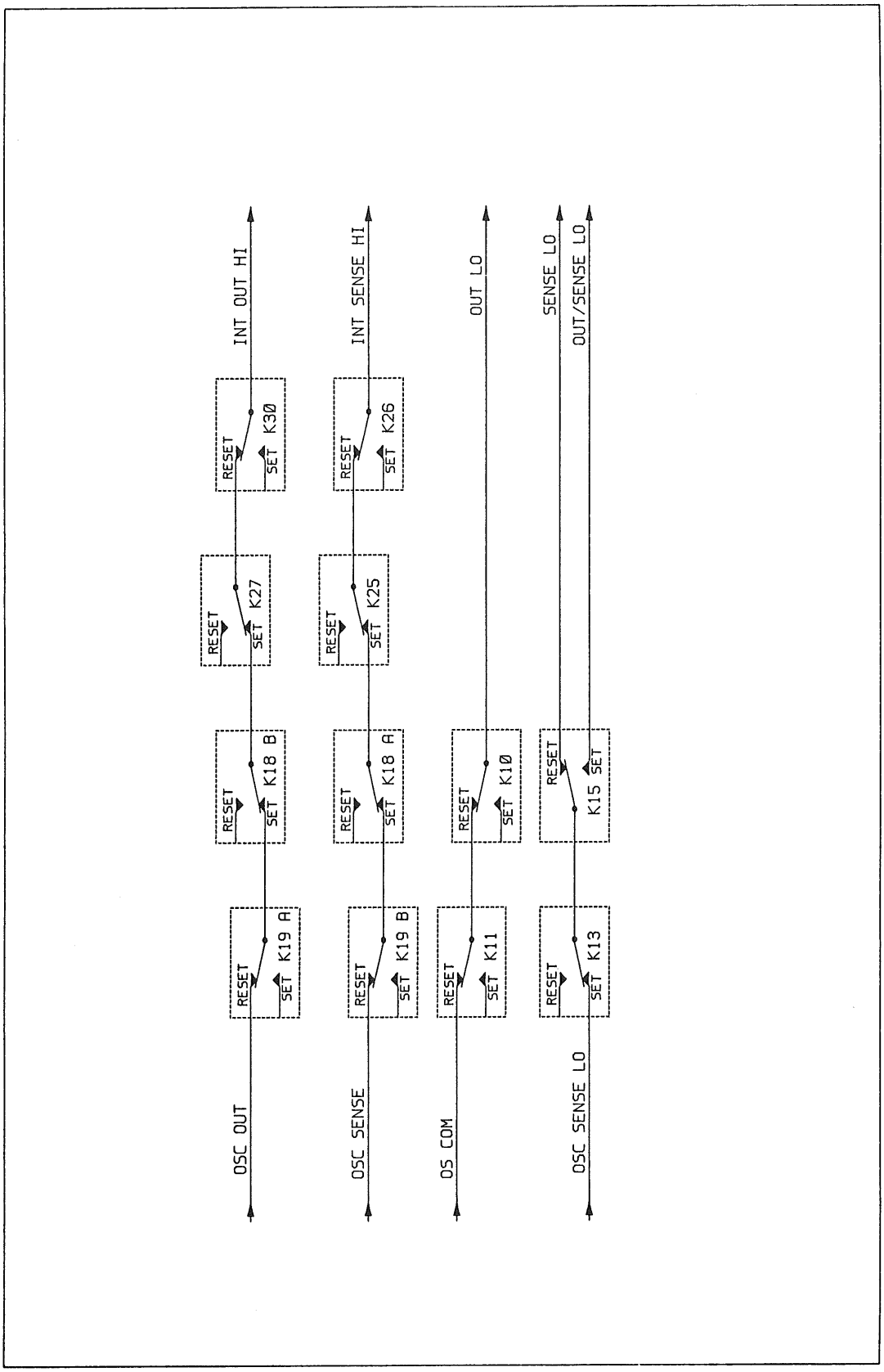


Figure 2-8. Switch Matrix Configuration for 2.2V and 22V ac Ranges

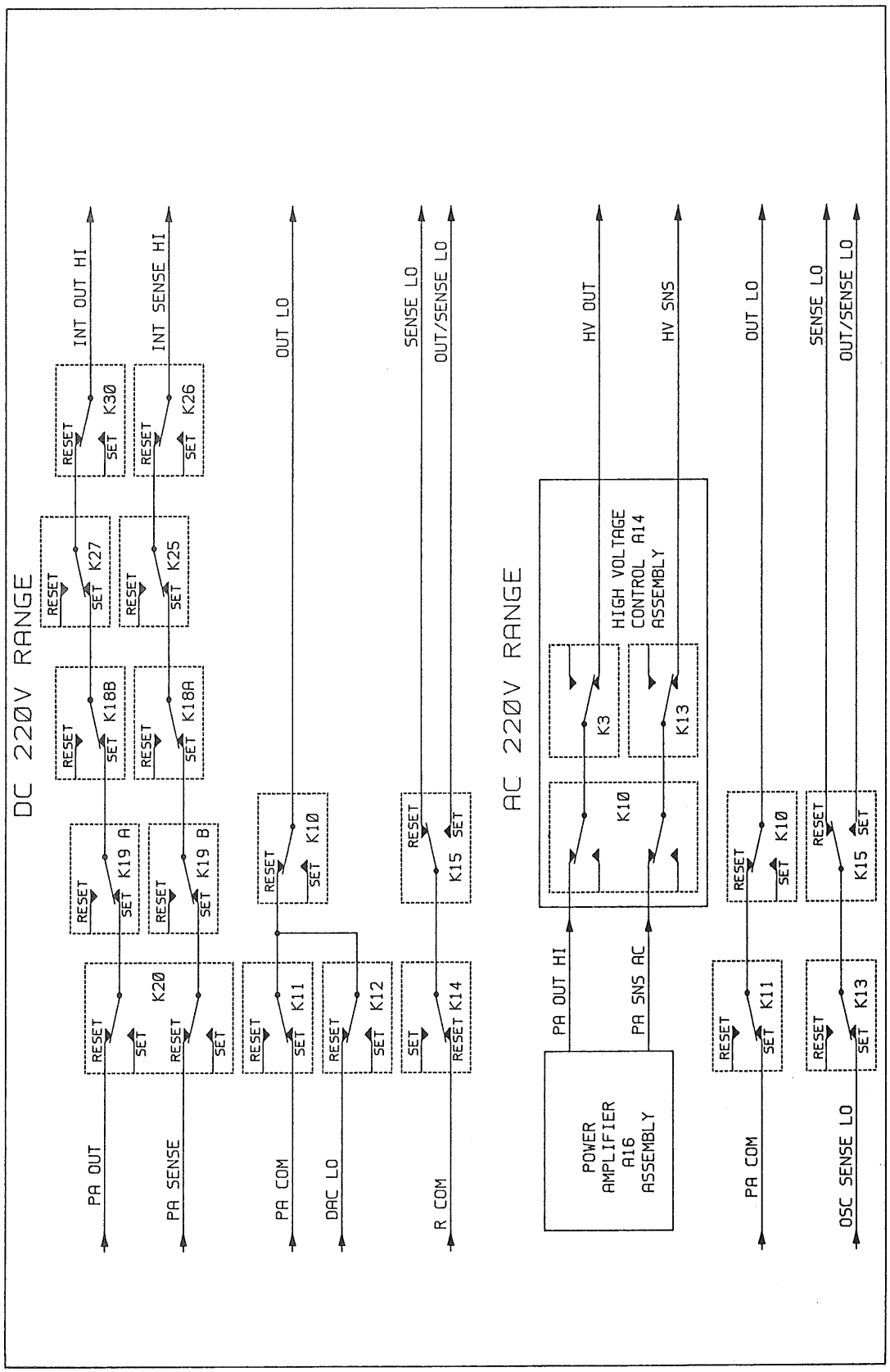


Figure 2-9. Switch Matrix Configuration for 220V dc and ac Ranges

2-92. SWITCH MATRIX OPERATION: 2.2V DC RANGE

Refer to Figure 2-10 for the following discussion. The dc 2.2V range circuit consists of the dc 2.2V attenuator and a dc 2.2V range amplifier as outlined on page 3 of the Switch Matrix schematic. This circuit contains a CA3096 transistor array IC (U19A-E), transistor Q4, FETs Q12 and Q13, resistors R20 and R25-R32, relays K1 and K2, part of the resistor network 4R07, and a dc amplifier heated hybrid.

The resistor network is bonded to the hybrid and this entire assembly is called the 5700A-4HR1 (HR1) on the schematic. Transistor Q3 drives the heater resistor on the hybrid. The heater control circuit adjusts the base voltage of Q3 to deliver the correct power to the heater resistor to maintain thermal control. Transistor Q8 protects the hybrid in case Q3 fails.

To produce the dc 2.2V range, the DAC assembly (A11) is set to the 11V range. DAC OUT HI and DAC SENSE HI are connected to pin 10 of the resistor network by relay K1, and DAC LO is connected to pin 9 by relay K2. The network divides the voltage by five. The divided voltage from pin 8 is connected to the input (pin 11) of the dc amplifier hybrid.

This temperature-controlled amplifier is used as a buffer amplifier. The output of the buffer amplifier (pin 18) drives the 2.2V range high current output stage consisting of U19, Q4, R25-R32, and CR7-CR9. This circuit enables the 2.2V range to support 50 mA of current with current limiting. FETs Q12 and Q13 provide localized feedback for the precision dc amplifier during unusual conditions, such as a short circuit at the OUTPUT binding posts or when this range is in standby.

Line 2.2V OUT is connected to INT OUT HI through relays K27 and K30 on the Switch Matrix. Line INT OUT HI is connected to the OUTPUT HI binding post through relay K1 on the Motherboard. Line 2.2V SENSE is connected to INT SENSE HI through relays K25 and K26 on the Switch Matrix. Motherboard relays K2 and K3 switch INT SENSE HI to the SENSE HI binding post during external sensing, or to OUTPUT/SENSE HI during internal sensing.

Line PA COM is connected to the OUTPUT LO binding post through relays K11 and K10. Switch Matrix relays K14 and K15 connect R COM to the SENSE LO binding post during external sensing, or OUTPUT/SENSE LO during internal sensing.

2-93. CALIBRATION OF THE 2.2V RANGE

Refer to Figure 2-11 for the following discussion. Calibration of the 2.2V range involves determining its offset and gain constants.

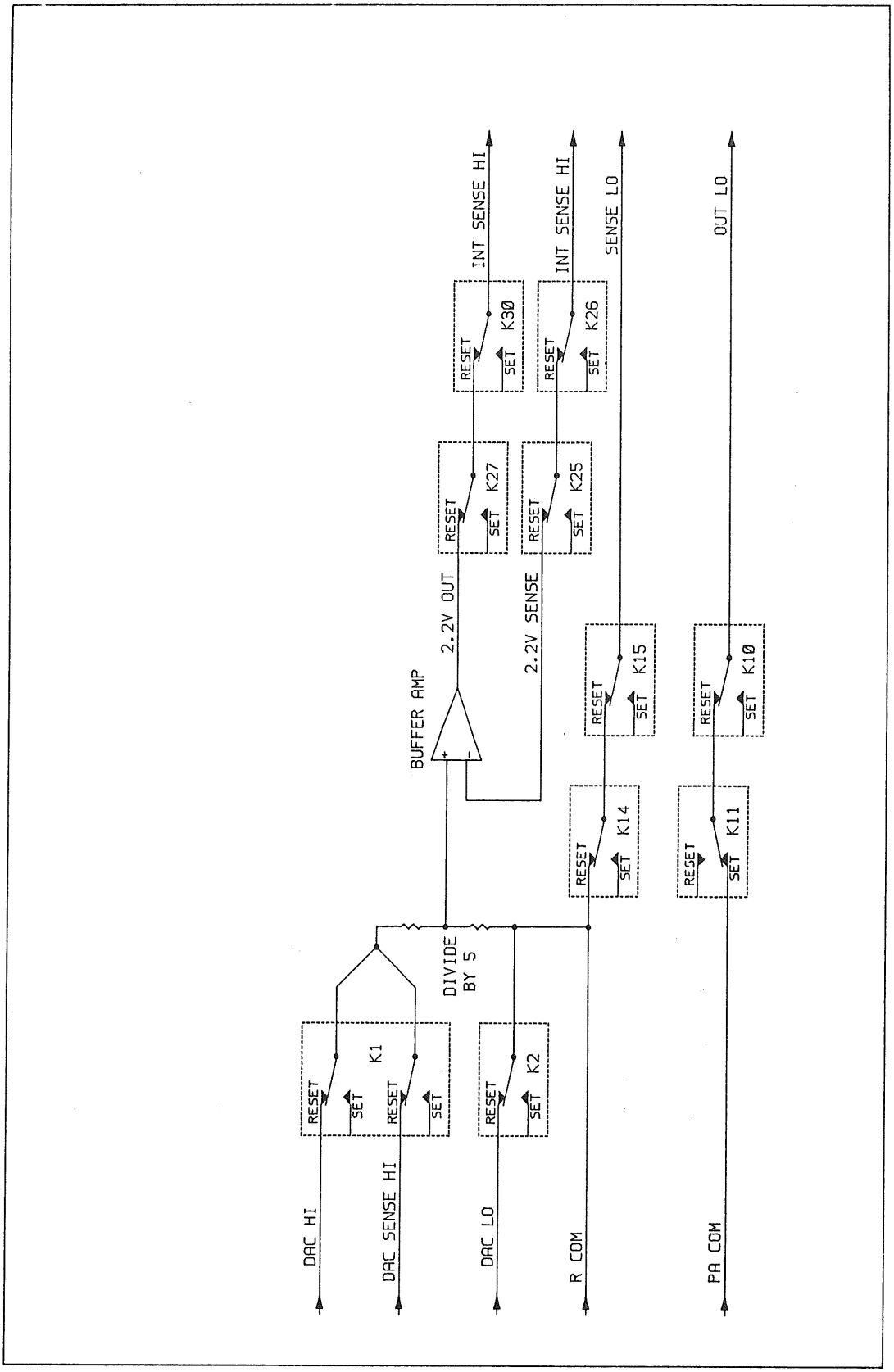


Figure 2-10. Switch Matrix Configuration for 2.2V dc Range

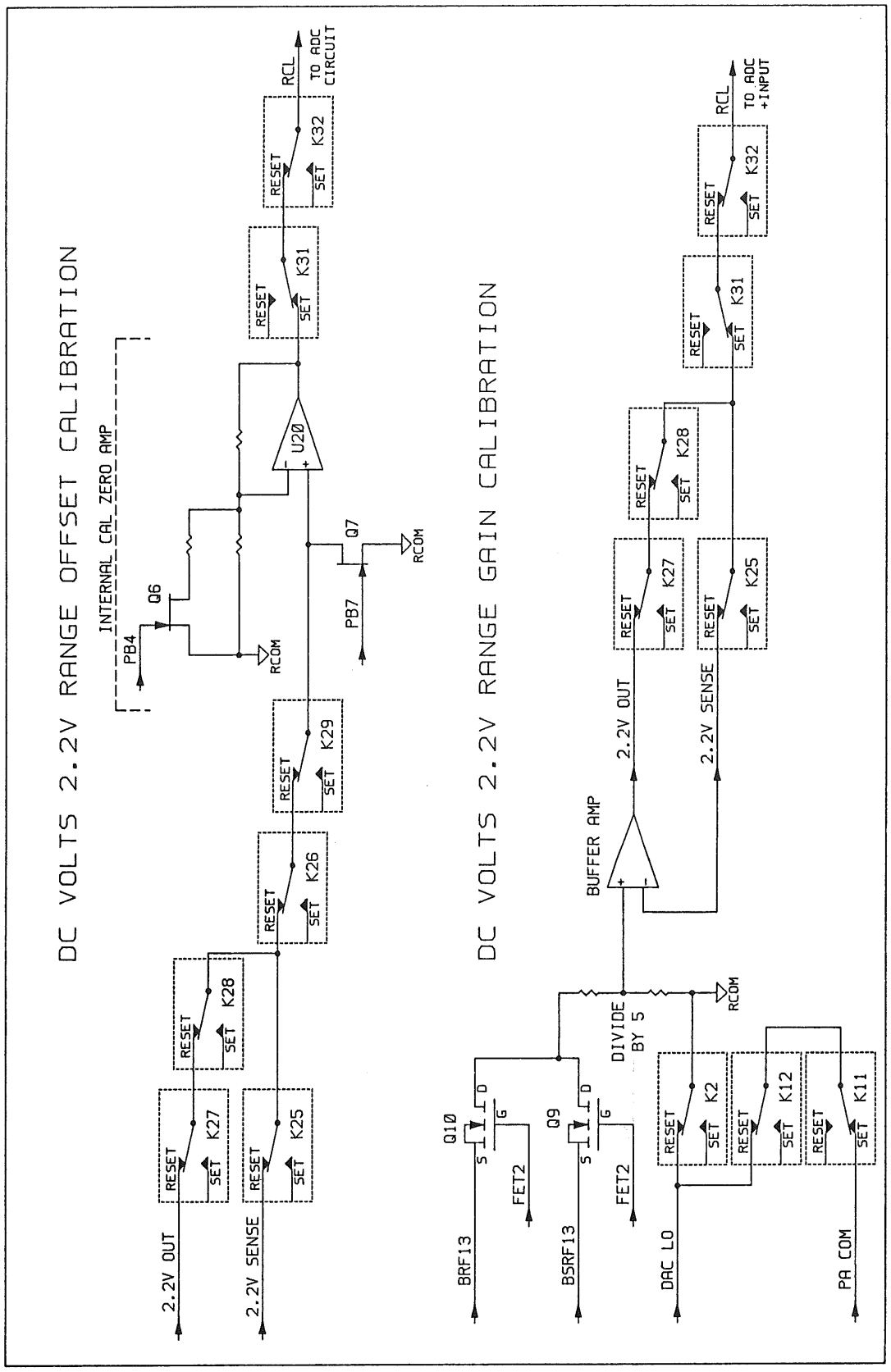


Figure 2-11. Calibration of the 2.2V dc Range

To calibrate the offset:

1. The gain of the internal cal zero amplifier is set to 130 by turning on Q6 via PB4.

2. A checkpoint reading is taken, which represents 0V at the input of the internal cal zero amplifier. In this configuration, PB7 turns on FET Q7 connecting RCOM to the internal cal zero amplifier input, K29 is open (set position), and the output of the cal zero amplifier is connected to RCL via relays K31 and K32.

3. The input of the internal cal zero amplifier is connected to the output of the 2.2V range. The 2.2V range is adjusted until the adc reads the same as the checkpoint reading within the given tolerance. In this configuration, 2.2V OUT and 2.2V SENSE are tied together by relay K28 and the output (INT SENSE HI) of the range is channeled into the internal cal zero amplifier input (page 1) through relay K29.

To calibrate the gain of the 2.2V range, the 13V buffered reference (BRF13 and BSRF13) from the DAC assembly (A11) is connected to the input of the 2.2V range by FETs Q9 and Q10 on page 3 of the schematic. Since this network divides the voltage by five, a voltage of 2.6V is obtained at the 2.2V OUT and 2.2V SENSE points. These points are tied together by relay K28. This voltage is then channeled to the RCL line by relays K31 and K32 where it is connected to the +input of the adc amplifier on the DAC assembly (A11). The DAC output is connected to the -input of the adc amplifier and is adjusted until a null is achieved. At this point, the DAC voltage represents the output voltage of the 2.2V range. Gain is determined since the output, input, and offset of the 2.2V range are now known.

2-94. SWITCH MATRIX OPERATION: 220 mV DC RANGE

Refer to Figure 2-12 for the following discussion. The 220 mV range is an extension of the dc 2.2V range. The 2.2V range is divided by ten to produce the 220 mV range. This 10:1 divider (on page 2 of the Switch Matrix Schematic) is part of the resistor network on the 4HR1 assembly.

The 220 mV range is passive with an output resistance of 50 ohms. This range is generated by connecting the 2.2V OUT and 2.2V SENSE to pin 3 of the 10:1 divider by relays K16 and K6. Lines PA COM and R COM are connected to pin 2 of the 10:1 divider by relays K11 and K21. This divided output from pin 1 is called AC/DC mV on the schematic. This portion of the resistive attenuator is also used for generating the ac 2.2 mV and 22 mV ranges. The AC/DC mV signal is then connected to INT SENSE HI through relay K17A on page 1 of the Switch Matrix schematic. Line INT SENSE HI is connected to the OUTPUT HI binding post through relays K2 and K3 on the Motherboard. Sensing for the LO occurs by connecting R COM and PA COM via K11 and K21. A single line is run out to the OUTPUT LO binding post by relay K33 on the Switch Matrix.

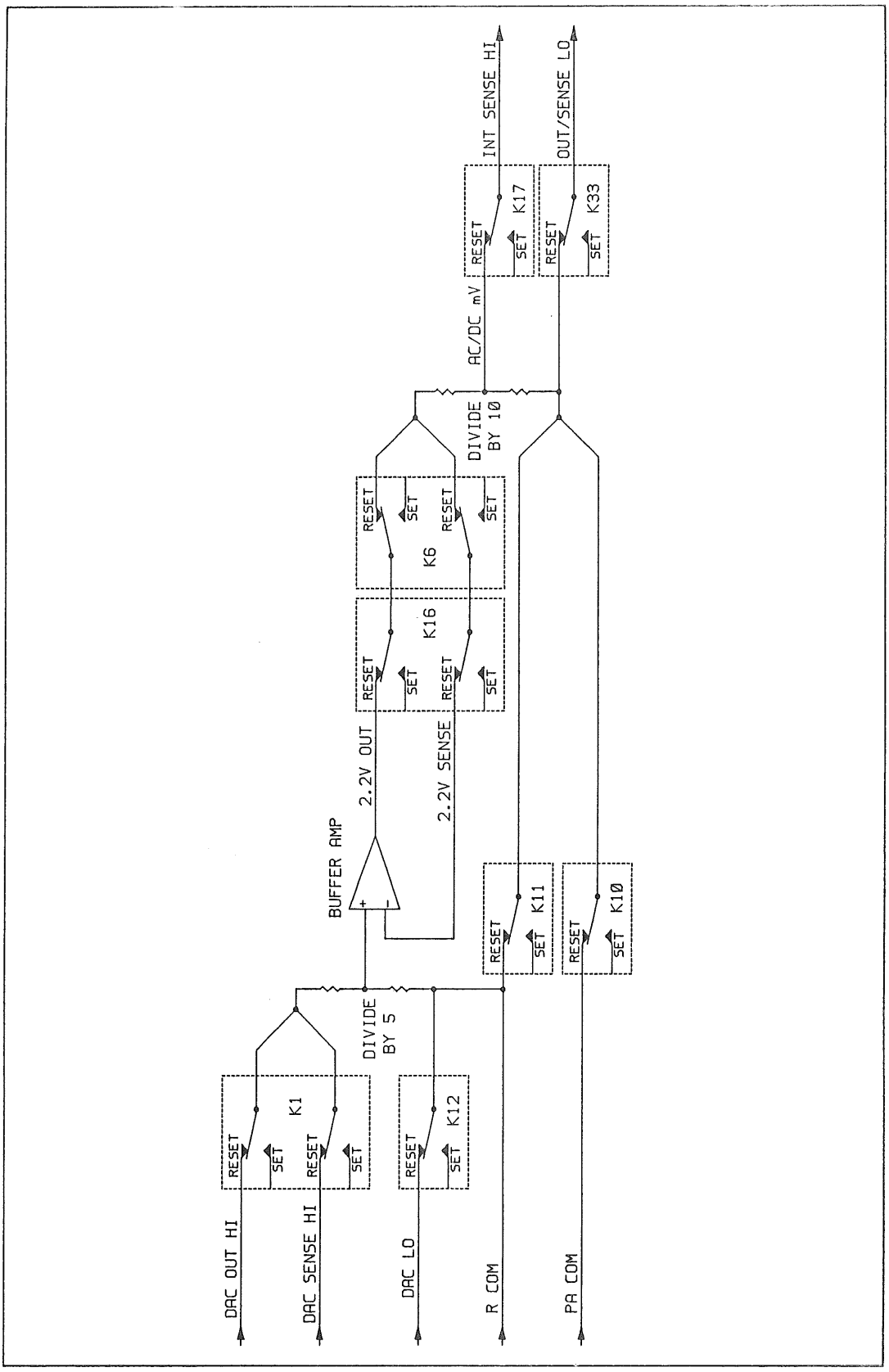


Figure 2-12. Switch Matrix Configuration for 220 mV dc Range

2-95. SWITCH MATRIX OPERATION: 220 mV AC RANGE

Refer to Figure 2-13 for the following discussion. As previously mentioned, the ac 220 mV range uses the same resistor network as the dc 220 mV range. In generating the ac 220 mV range the Oscillator assembly is set to the 2.2V range. Lines OSC OUT and OSC SENSE are connected to pin 3 of the 10:1 divider by relays K5 and K6. Lines OS COM and OSC SENSE LO are connected to pin 2 by relays K11 and K9 respectively.

This divided output from pin 1 is referred to as AC/DC mV on the schematic. The AC/DC mV is then connected to INT SENSE HI through relay K17 on page 1 of the Switch Matrix schematic. Signal INT SENSE HI is connected to the OUTPUT HI binding post through relays K2 and K3 on the Motherboard. Sensing for the LO occurs by connecting OS COM and OSC SENSE LO via K11 and K9. A single line is run out to the OUTPUT LO binding post by relay K33 on the Switch Matrix.

2-96. SWITCH MATRIX OPERATION: 2.2 mV AND 22 mV AC RANGES

Refer to Figure 2-13 for the following discussion. The ac 2.2 mV and 22 mV ranges use the 100:1 divider and the 10:1 divider of resistor network on 4HR1 for a total division of 1000:1. Switch Matrix operation for these two ranges is the same. For the 2.2 mV range, the Oscillator assembly is set to the 2.2V range. For the 22 mV range, the Oscillator assembly is set to the 22V range.

Signals OS COM and OSC SENSE LO are connected to pin 6 of the 100:1 divider and pin 2 of the 10:1 divider by relays K11 and K9. OSC OUT and OSC SENSE are connected to the input (pin 7) of the 100:1 divider by relay K3 (A and B). The output of this 100:1 divider is then connected to the input of the 10:1 divider (pin 3) by relay K7. At the output of the 10:1 divider (called AC/DC mV on the schematic) there is a total division of 1000:1. Connection to the binding posts is done in the same manner as in the ac 220 mV range. In all cases, the output impedance of the millivolt ranges is 50 ohms.

2-97. CALIBRATION OF THE mV RANGES

Calibration of the mV ranges involves determining the resistor ratios of the 10:1 divider and the 1000:1 divider (100:1 and 10:1 dividers cascaded). In addition, an offset calibration is performed on the 10:1 divider to remove thermal EMF error for the 220 mV dc range.

Refer to Figure 2-14 for the following discussion. The 10:1 divider offset is calibrated by configuring the Switch Matrix for the 220 mV dc range, except with the output of the range (AC/DC mV) switched into the input of the internal cal amplifier through relays K17 and K29. The Calibration procedure is the same as described for the 2.2V range offset calibration except that during a checkpoint reading, control line PC4 turns on Q11 which connects SWM SENSE LO to the input of the zero amplifier, representing 0V for the 220 mV range.

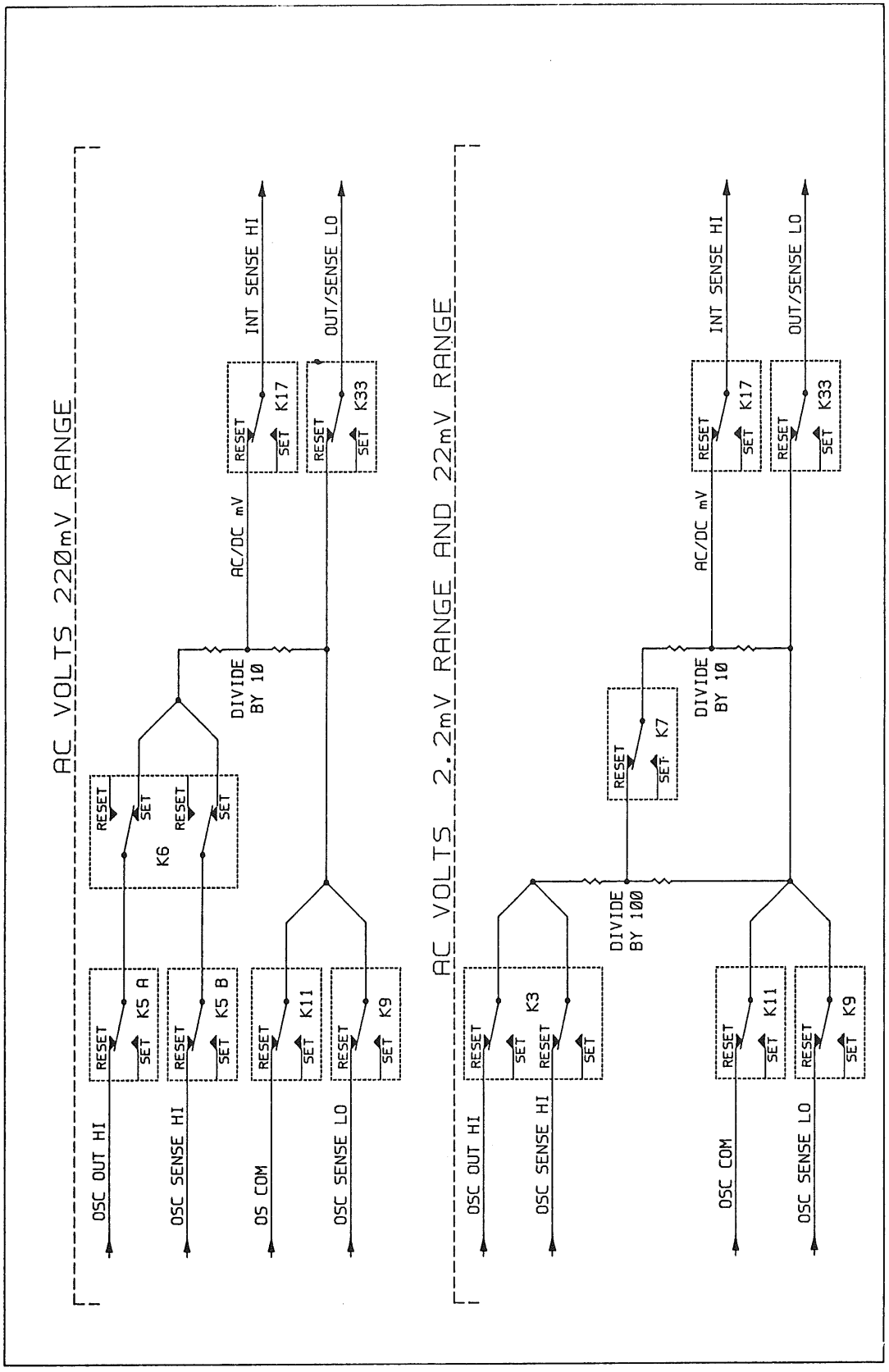


Figure 2-13. 220 mV ac, 2.2 mV ac, and 22 mV ac Ranges

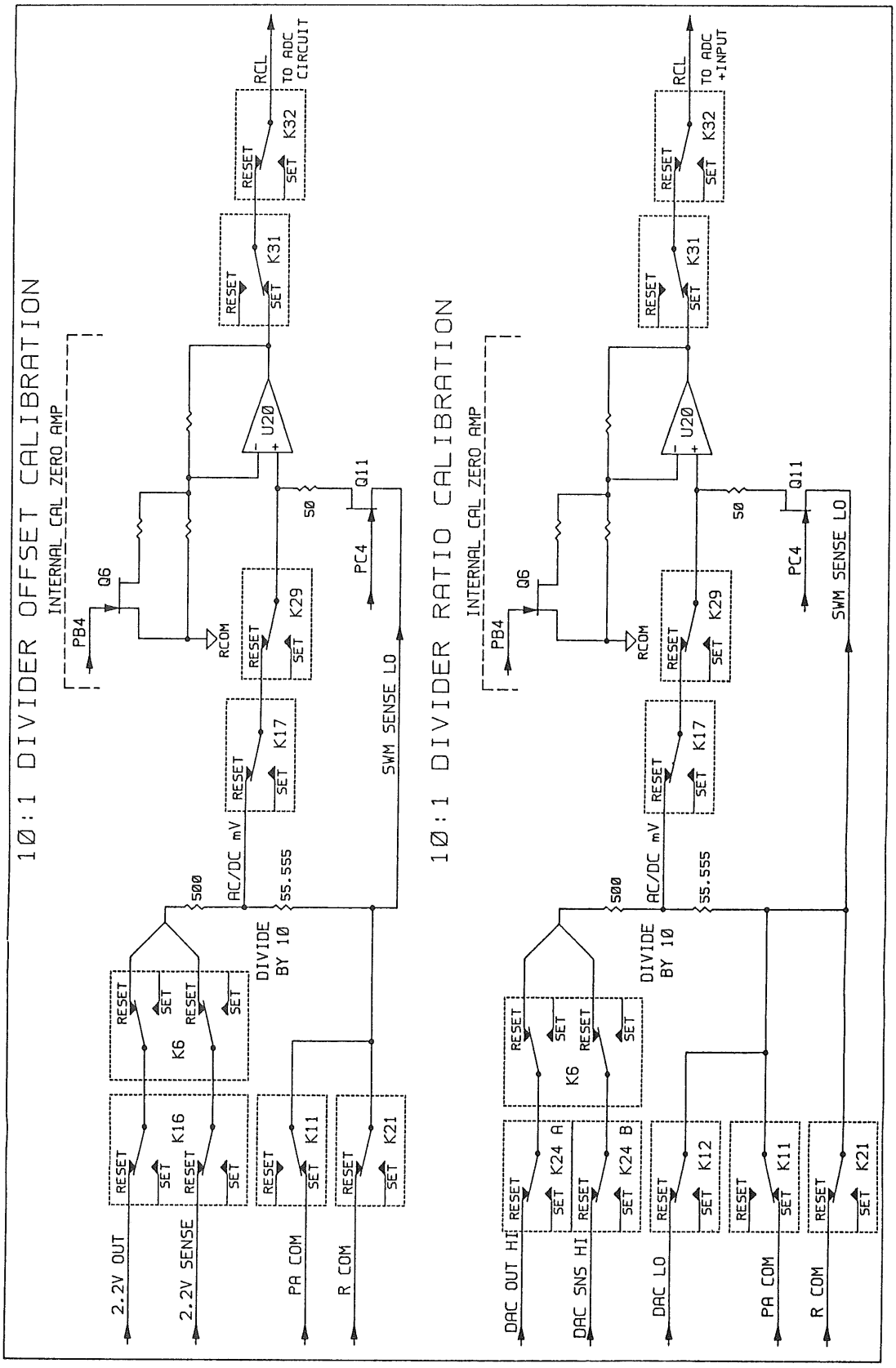


Figure 2-14. 10:1 Divider Calibration

Calibration of the 10:1 divider ratio is accomplished by connecting the DAC assembly output (DAC OUT HI and DAC SENSE HI) through relays K24 (A and B) and K6 to the input of the 10:1 divider. DAC LO, PA COM, and R COM are connected to the common of the 10:1 divider by relays K12, K11, and K21 respectively. The DAC output is set to 2.2V to produce approximately 0.22V at the output of the 10:1 divider (AC/DC mV). Relays K17 and K29 direct this voltage to the internal cal zero amplifier, which is configured for a gain of 10, giving 2.2V plus an unknown error at its output.

The equation for this output is the DAC output (2.2V) multiplied by the 10:1 divider ratio (unknown) multiplied by the internal cal zero amp gain (calibrated, approximately 10). Once the output of the internal cal zero amplifier is determined, the 10:1 divider ratio is the only unknown, so it can be calculated.

To determine the output of the internal cal zero amplifier for this configuration, a checkpoint reading is first taken by connecting both inputs of the DAC's adc amplifier to the DAC output, which is set to 2.2V. This reading represents a null at 2.2V. The output of the internal cal zero amplifier is then channeled to the RCL line by relays K31 and K32 and to the +input of the adc amplifier on the DAC assembly with the DAC output still connected to the -input. An adc reading is now taken and the checkpoint reading is subtracted from it. This value is the adc's representation of the deviation of the internal cal zero amplifier output from 2.2V.

However, due to inaccuracy in the adc, an additional step must be taken. The -input of the adc amplifier is connected to RCOM and the +input to the DAC output. The DAC output is adjusted until the adc reads the previous value within the given tolerance. At this point, the DAC output voltage represents accurately the deviation of the internal cal zero amplifier output from 2.2V. The output of the internal cal zero amplifier is now calculated, allowing the 10:1 divider ratio to be determined.

Refer to Figure 2-15 for the following discussion. Calibration of the 100:1 divider ratio is similar to calibration of the 10:1 divider ratio. The 13V buffered reference (BRF13 and BSRF13) is connected to the input of the 100:1 divider pin 7 by relay K4 (A and B). DAC LO, PA COM , and R COM are connected to pin 6 of the 100:1 divider by relays K12, K11, and K21 respectively. The voltage at the divider output (pin 5) is approximately 0.13V. Relay K7 connects the output of the 100:1 divider to the input of the 10:1 divider. Relays K6 and K8 connect it to the ac mV CAL line, which is the input to the internal cal zero amplifier. The result is 1.3V at the amplifier output. This voltage is switched onto the RCL line by relays K31 and K32 to the DAC assembly, where the DAC is nulled to it. At this point, the DAC voltage represents the internal cal zero amplifier output and the 100:1 divider ratio is calculated.

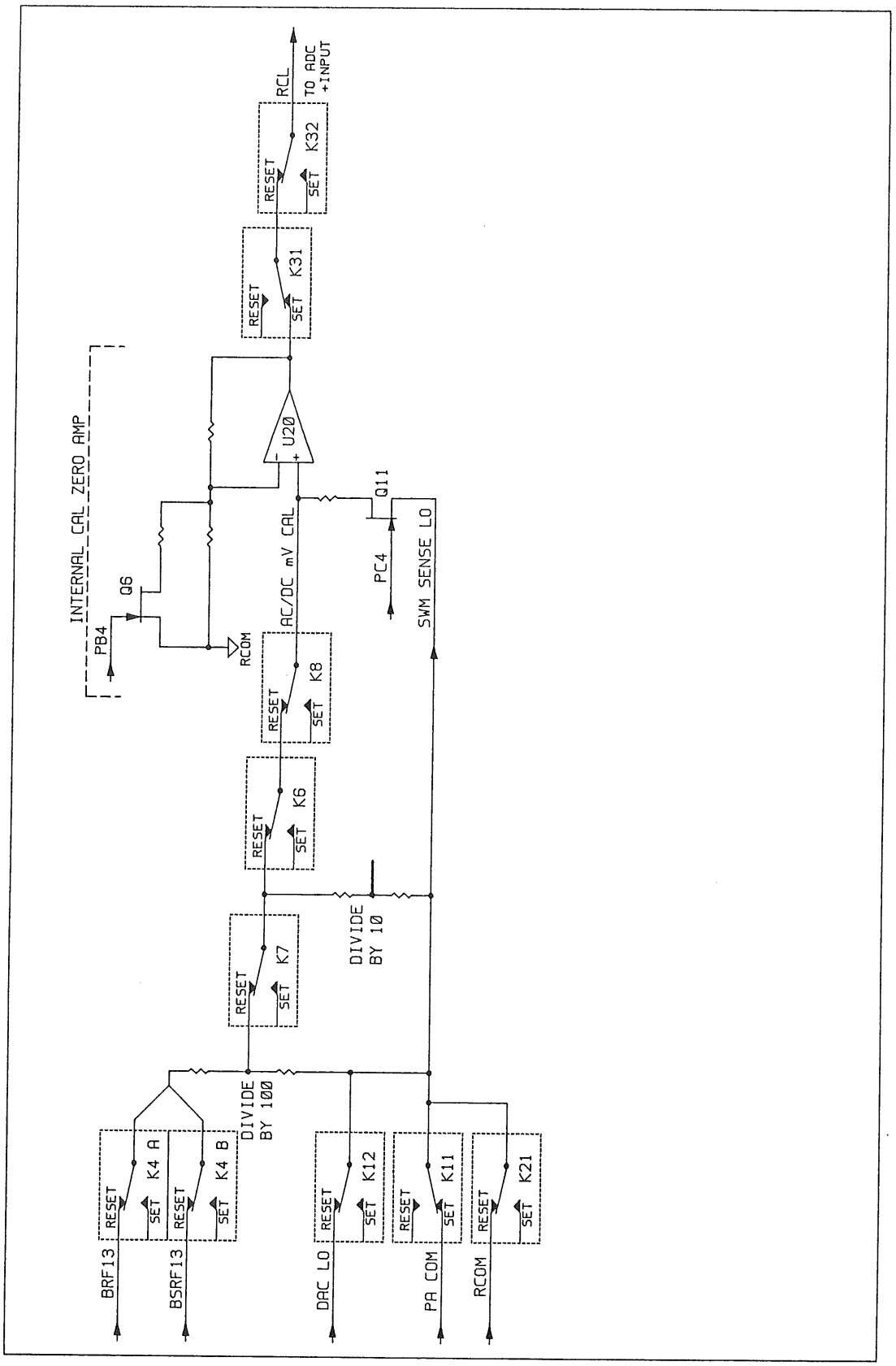


Figure 2-15. 100:1 Divider Gain Calibration

2-98. INTERNAL CAL ZERO AMPLIFIER

The main function of the internal cal zero amplifier is to remove the offsets of each of the dc ranges except the 1100V range. (The 1100V dc range is zeroed at the High Voltage/High Current assembly.) The internal cal zero amplifier is switched into two gain configurations for range zeroing; a gain of 130 for the 22V ranges and below, and a gain of 10 for the 220V range. Each range is channeled into the internal cal zero amplifier via relay K29. The range is then compared against 0V by connecting R COM to the amplifier via FET Q7. For the 220 mV range, the reading for 0V (or checkpoint reading) is taken by turning on Q11 instead of Q7 in order to achieve a 50 ohm impedance. The output of the amplifier is connected to the RCL line by relays K31 and K32, and then channeled to the DAC assembly where the signal is measured by the adc.

The internal cal zero amplifier is outlined in a broken line rectangle on page 1 of the schematic. Its functional parts are U20-U21, R43-44, R46-47, Q6-7, Q11, and Z2. When Q7 is on, the input of the zero amplifier is connected to 0V for a reference point. When Q6 is on, the gain of the zero amplifier is 130. Op amp U21 and its associated resistors form a current-cancellation circuit. It senses the output of the zero amplifier and creates a current equal in magnitude but opposite in polarity to the current through the gain resistors (Z2), resulting in zero current in the precision common (RCOM).

2-99. SWITCH MATRIX 5725A AMPLIFIER INTERFACE

The Switch Matrix also provides switching between the calibrator and the 5725 Amplifier. The ac and dc input signals necessary to operate the 5725A are connected by relay K22. Relay K23 connects B SNS LO to either OSC SENSE LO or R COM via relay K14.

2-100. DAC Assembly (A11)

The DAC (digital-to-analog converter) is the basic building block of the calibrator. Other assemblies create ac and dc voltages and currents with its precision dc voltage. The DAC contains five assemblies:

- o DAC Main Board (A11)
- o DAC Filter SIP (A11A1)
- o DAC Buffered Reference SIP (A11A2)
- o Reference Hybrid (HR5)
- o DC Amplifier Hybrid (HR6).

The DAC assembly serves two main functions:

- o To provide a highly repeatable stable dc voltage
- o To support calibration of the calibrator

The DAC's adc circuit is used to accomplish calibration. It is made up of an analog to digital converter (adc) and the adc amplifier. Together, these are used to completely characterize the calibrator, using only one external voltage source and two external resistor standards.

2-101. BASIC DAC THEORY OF OPERATION

Figure 2-16 is a simplified schematic of the DAC assembly. The DAC uses a pulse-width-modulated scheme to produce a precision dc voltage of 0V to 22V with positive and negative polarity. The DAC contains:

- o A 13V temperature-controlled reference hybrid (HR5)
- o Duty-cycle control circuitry
- o A five-pole active filter (A11A1 assembly)
- o An output stage
- o Digital control circuitry

These basic subcircuits work together for a stable and linear dc voltage.

The DAC assembly also contains:

- o A sense-cancellation circuit
- o Linearity control circuits
- o Negative offset circuit
- o An output switching circuit

The two inputs of the five-pole filter are two precision square waves with different fixed amplitudes and independently variable duty cycles controlled by software. The filter's first input square wave is called the first channel. It is switched between the reference voltage (13V) and 0V.

The filter's second input square wave is called the second channel. It is switched between approximately 0.78 mV and 0V. Its amplitude is derived by resistively dividing the 13V reference. This second channel is used for extra resolution.

The filter rejects all ac components of the waveforms above 10 Hz. Since the frequency of the square waves is 190 Hz, the output of the filter is a dc voltage which is the sum of average voltages of the two waveforms. The Output Stage, which consists of the dc amplifier hybrid and the output buffer, isolates the filter output from the DAC output and gives current drive to the DAC output.

The output stage has a current limit of approximately 60 mA. It can be configured for a gain of one for the 11V range, or a gain of two for the 22V range. Relays on the DAC output lines allows them to be inverted for negative polarity.

To change the DAC voltage, the average value of the two square waves must be varied. To determine the average value, multiply the waveforms amplitude by its duty cycle. Vary the duty cycle and keep the amplitude fixed to change the DAC voltage.

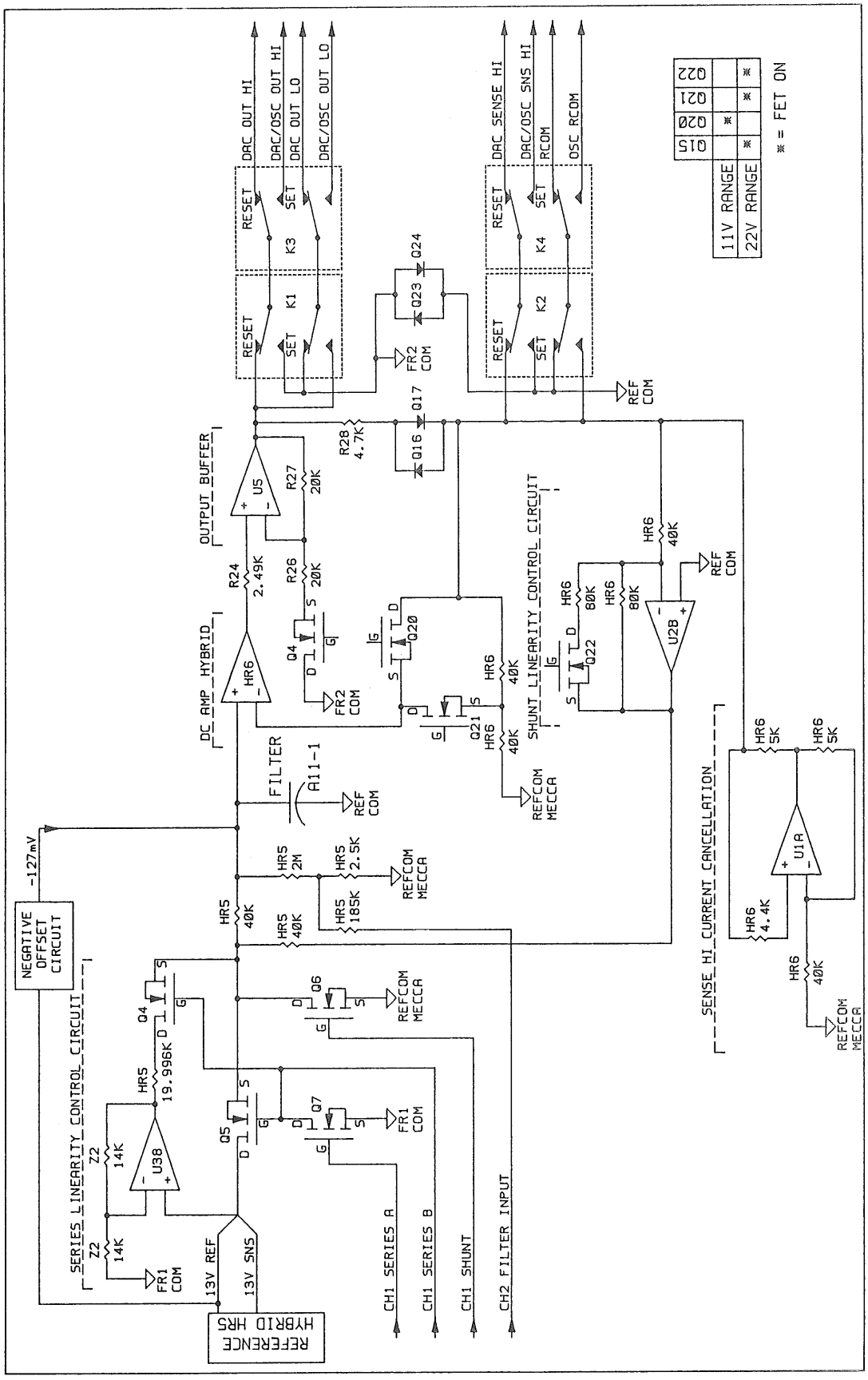


Figure 2-16. DAC Assembly Simplified Schematic