For example, if the duty cycle of the first channel is 10% and the second channel 50%, the overall average voltage would be:

(0.1 x 13V) + (0.5 x 0.78 mV) = 1.300390V.

The duty cycle resolution is 0.0024%, which gives a first channel resolution of 0.309 mV and second channel resolution of 18.5 nV.

The duty cycle control circuitry creates the two digital square waves for the first and second channels. These two waveforms are first run through optocouplers for isolation and then into analog switching and level shifting circuits. These circuits derive the proper signals to switch the input of the filter at the levels explained above.

2-102. DAC ASSEMBLY DIGITAL CONTROL

The digital control circuit is located on page 6 of the DAC schematics. The 82C55 Programmable Peripheral Interface IC (U31) is the heart of this circuit.

This IC, which is under software control via the guarded digital bus, has three ports that provide 24 static lines. Port A (PA0-PA7) is configured as a read-only port register. It passes the adc readings from the ADC IC (U25) to the guarded digital bus.

PB0-PB4 of port B control relays K1-K4 and K6-K8 via relay drivers U33 and U34. PB0 is also control line DAC OUT SEL used to turn on FET Q25, via FET Q26, and connect RCOM to SCOM during calibrator operation in the ac function.

PC7 of port C, buffered by U8A, provides the enable for these relay drivers. Relay driver U33 controls latching relays K7 and K8. Outputs from U33 are also used by Relay driver U34 to control latching relays K1-K6. PB5-PB7 are decoded by U32 to create six control lines. These control lines are used to select one input to the adc amplifier -input. K5SEL is an input to the relay drivers to control latching relay K5. The remaining five control lines are used by comparators in U35 and U36. These comparators provide the proper level shifting to create control lines BSRF6 SEL, BSRF13 SEL, REF6 SEL, REF13 SEL, and ADC COM SEL. These control lines are used to control FETs on the DAC Buffered Reference SIP assembly (A11A2).

PC0 of port C is buffered by U8 (B and C) and routed through opto-isolator U37 to create RANGE SELECT, which sets the DAC to the 11V or 22V range. PC1 is used in the duty cycle control circuit to shut off the 8 MHz clock via buffer U8F and the first channel via OR gate U9D. This is done during calibrator operation in the resistance function. PC2 controls a FET in U23 for use in self-diagnostics. PC3 and PC4 are level-shifted by comparators in U36 before they are used to control FETs in U23. PC5 of port C is connected to a comparator in U36. This comparator provides the proper level shifting to create control line ADCAMP OUT SEL to control a FET in U23. PC6 is control line ADC TRIGGER which triggers the adc (analog-to-digital converter) IC U25. A0, A1, and CS*, from the guarded digital bus, are used by OR gates in U9 (B and C) to create control line ADC READ for use by the adc IC U25.

2-103. DAC ASSEMBLY REFERENCE CIRCUITRY

The reference circuitry is on the reference hybrid, located on the HR5 assembly. The HR5 assembly contains a ceramic substrate reference hybrid bonded to a resistor network.

All components on this assembly are surface mount devices, except U6 and U7. The resistors are screened with a thick film paste. Associated resistors, capacitors, and zener diodes are mounted on the main board to supply this hybrid with the appropriate power and ground returns.

As previously explained, the amplitudes of the pulse width modulated signals for the first and second channel are assumed to be fixed. Any change in amplitude shows up as an error on the output of the DAC. Since the reference is used to determine the amplitude, it must be very stable and generate little noise.

The 13V reference contains two cascaded 6.5V temperature compensated transistor/zener diode pairs called ref amps (U6 and U7). The excellent temperature characteristics of the ref amps are obtained by biasing the collector current on their transistors with a value such that the TC (temperature coefficient) of its base-emitter junction cancels the TC of the zener diode. Since the base-emitter junction and the zener diode are in series, the result is a near zero TC.

Correct bias currents are achieved with a thin-film resistor network in a surface-mount package mounted on the hybrid.

The reference circuit is designed such that the effects of the thin-film resistors and op amp errors are second order. Thus, accuracy is determined almost entirely by the ref amps.

To further reduce the effects of ambient temperature variations, the hybrid is heated to a constant 62 oC by the heater control circuitry on page 1 of the DAC schematic.

Temperature is sensed near the ref amps by a thermistor (RT1). If the substrate temperature changes, the thermistor resistance changes. This creates a correction voltage to the base of Q2 (on the main board). This, in turn, causes the power into the heater resistor, which is screened on the back of the substrate, to increase or decrease as necessary to maintain a stable temperature.

Thermal runaway is prevented by a protection circuit. Once the substrate temperature reaches approximately 67^{o}C, the change in resistance of RT2 causes Q9 to turn on. As transistor Q9 turns on, it steals base current from Q1 on the main board, which brings it out of saturation. This breaks the current path through the heater resistor. This condition exists only if there is a failure.

The exact value of the reference is determined during calibration. Because of the stability of the reference, it can be used for future internal calibration procedures to remove short term errors in the calibrator.

The 13V output, REF13 HI, is from pin 9 and REF13 SENSE is on pin 12. Also, a 6.5V reference line, REF6, is brought out on pin 14 of the reference for use during calibration.

In order to make these reference voltages available to other assemblies, the 6.5V and 13V references are buffered on the DAC Buffered Reference SIP assembly (A11A2). This assembly also contains the circuitry to switch the references and buffered references into the input of the adc during calibrator calibration. Refer to the section on the DAC Buffered Reference SIP for more information.

2-104. DUTY-CYCLE CONTROL CIRCUIT

Duty-cycle control circuitry is pictured on page 3 of the schematics. DAC output voltages are represented in software by what are called first and second channel counts. Each count is a 16-bit number which is sent to the DAC assembly via the guarded digital bus.

For example, a first channel count of 20,000 (in decimal) represents a DAC output voltage of approximately 6.5V (half the reference voltage).

The first function of the duty-cycle control circuitry is to convert each count into a stable, TTL level, square wave, with a duty cycle proportional to the numeric value of the count. This is accomplished with the 82C54 programmable interval timer (U6).

A low-level 8 MHz clock is generated on the Regulator/Guard Crossing assembly (A17) and routed to the DAC assembly via the motherboard. This low-level clock, CLK and CLK*, is amplified to a TTL level by comparator U7 to generate the 8 MHz clock which is used by U6 and the adc IC U25.

The 82C54 programmable interval timer receives its input counts from the guarded digital bus and creates the second channel signal on OUT2 (pin 20) and the first channel signal on OUT1 (pin 16).

The second channel signal is buffered by U8 (D and E) and runs through opto-isolator U12 to become CH2 FLOATING. This signal alternately turns FETs Q30 and Q32 on and off to turn the 3V source (called 3V) into a floating 3V pulse width modulated waveform called CH2 FILTER INPUT.

The 3V source is created from the 13V reference. The 13V reference is buffered by op amp U1B, configured as a voltage follower. The output from U1B is divided down to 3V by a 100 kilohm and 30 kilohm resistor in the HR5 assembly, creating 3V.

This 3V is again buffered by op amp U11, configured as a voltage follower, to create the 3V, which is switched by FETs Q30 and Q32. CH2 FILTER INPUT uses three resistors on the HR5 assembly to resistively divide its 3V amplitude by an additional factor of approximately 3800.

The first channel signal is buffered by U8 (G and H) and run through opto-isolator U13, to become CH1 FLOATING. Since the first channel is much more critical than the second, CH1 FLOATING is clocked into a flip flop (U14) to insure an accurate waveform.

To clock in this waveform, the low-level 8 MHz clock (CLK and CLK*) from the Regulator/Guard Crossing assembly (A17) is isolated by transformer T1 and amplified to a TTL level by comparator U10. This generates the clock inputs for U14. The output Q1 (pin 5) from U14 creates CH1 SERIES A, which switches Q7. The output Q1* (pin 6) is inverted by Q35, creating CH1 SHUNT, which switches Q6. The output Q1*, which is a TTL level, is also amplified by components Q33, Q34, VR11, VR12, and R44-R46, so it switches from 0 to 18V, creating CH1 SERIES B, which switches Q4 and Q5.

The watchdog timer sets the first channel filter input to 0V if a failure occurs on the 8 MHz clock. This circuit uses a monostable multivibrator (one shot) U15, C63, and R48. The 8 MHz clock is divided to 4 MHz by U14. This 4 MHz clock is connected to U15 and discharges C63 to ground. If the 4 MHz clock stops, C63 charges up, causing the Q1 output of U15 to go low. This logic low on Q1 is connected to the preset pin of U14 (PRI), which causes its Q1 output high and its Q1* output low. This condition turns on the shunt switch and turns off the series switch, which forces the filter input to be REFCOM.

2-105. DAC FILTER CIRCUIT

The dac filter circuit is located on the DAC Filter SIP (A11A1) assembly. The dominant pole of the filter is near 10 Hz. This gives 120 dB of rejection at 190 Hz.

The +30FR1 supply and 15V zener diode, VR1, create the 15V supply (15V) for the op amps in the filter circuit. 15V is also connected to the main DAC board, where it is used with R111 as a pull up for the RANGE SELECT control line.

2-106. DAC OUTPUT STAGE

The output stage of the DAC assembly consists of the DC Amplifier Hybrid assembly (HR6) and the output buffer circuitry. Like the Reference Hybrid, the DC Amplifier Hybrid is constructed of surface-mount components (except precision op amp U2), on a ceramic substrate hybrid, bonded to a resistor network.

It is temperature-controlled by a heater control circuit in the same manner as explained on the Reference Hybrid. Transistor Q3 provides proper power to the heater resistor.

The DC Amplifier Hybrid consists of a precision op amp U2, with a bootstrapped power supply (Q1, Q2, R1-R4, VR1-VR2). The op amp has low noise and low offset. It is bootstrapped to improve the common-mode rejection in its noninverting configuration.

The DC Amplifier assembly interfaces with the output buffer (U5) to create the output stage. Control line RANGE SELECT configures this output stage for unity gain for the 11V range or a gain of 2 for the 22V range. In the 11V range, Q15 is turned off, which gives U5 unity gain, and Q20 is on, which gives the DC Amplifier unity gain.

In the 22V range, Q20 is off and Q21 is on, which switches in the 40 kilohm feedback resistors located on the HR6 assembly. Precise ratio matching of these resistors provides high accuracy in the 22V range.

FET Q15 is on in the 22V range so that the output of the dc amplifier is half the output of the DAC. This is necessary so that the output of the dc amplifier is approximately the same as its inputs, which allows the bootstrap circuit to work.

The output buffer (U5) provides drive for the DAC output. It is used in a feedback loop with the DC Amplifier Hybrid so that the dc accuracy is dependent upon the dc amplifier, and the output drive capability is dependent on the output buffer.

The output buffer is current-limited to a short circuit current of about 60 mA. The short-circuit protection circuitry works as follows:

The supply current is sensed by R23. When the output current of U5 reaches approximately 50 mA, the voltage across R23 is large enough to turn on Q10. As Q10 turns on, the voltage across R20 increases, and pulls down the supply voltage at pin 4 of U5. In order to prevent the supply of U5 from dropping below the input, Q8 saturates turning on Q11 which shorts the input to FR1 COM. When the short is removed, R22 and C41 cause Q11 to turn off slowly, which prevents a large overshoot at the DAC output.

2-107. SENSE CURRENT CANCELLATION CIRCUIT

This circuit uses op amp U1A and four resistors on the HR6 assembly. This circuit supplies the sense current of equal, but opposite, polarity to the feedback resistors in the 22V range. This eliminates current in the sense lead during external sensing.

2-108. LINEARITY CONTROL CIRCUIT

The linearity control circuitry contains the series linearity control circuit and the shunt linearity control circuit, as outlined on the schematic. These linearity control circuits eliminate filter current in the series switch (Q5) and the shunt switch (Q6). This is necessary because Q5 and Q6 have finite resistance (3 to 5 ohms) and a small mismatch in the resistances can cause a linearity error.

The series linearity control circuit uses op amp U38, resistor network Z2, and a single 19.996 kilohm resistor on the HR5 assembly. This circuit eliminates filter current in the series switch Q5.

When the series switch (FET Q5) is on, it connects the 13V reference to the first channel input of the filter, and FET Q4 is also turned on. This causes U38 to supply the current to the filter through the 19.996 kilohm resistor in HR5 and Q4, which makes the resistance from TP2 to TP5 look like near 0 ohms.

The shunt linearity control circuit uses op amp U2B, FET Q22, three 80 kilohm resistors on the HR6 assembly, and one resistor in the HR5 assembly.

Op amp U2B is configured as an amplifier with an inverting gain of 1 in the 11V range, and an inverting gain of 0.5 in the 22V range. This gain is determined by FET Q22 and the three 80 kilohm resistors in the HR6 assembly.

When the shunt switch (FET Q6) is on, connecting the input of the filter to REFCOM, the current from the filter flows through the two 40 kilohm resistor (pin 7 to pin 8) on the HR6 assembly to the output of U2B. This cancels out the current that would flow through Q6 which makes it look like 0 ohms.

2-109. NEGATIVE OFFSET CIRCUIT

This circuit creates a constant offset voltage of approximately -127 mV at the filter input. Thus, for a DAC output voltage of 0V, the first channel count must be approximately 400 to offset this negative voltage. This guarantees a minimum duty cycle pulse width of approximately 50 us.

This minimum duty cycle is necessary to overcome the offset of the output stage and to allow the reference voltage to settle out after being switched into the filter input. Op amp U2A and two 20 kilohm resistors in HR6 form an amplifier with an inverting gain of 1. This amplifier input is the 13V reference which produces -13V at its output. This -13V is divided by resistors in the HR5 assembly to create the -127 mV on the filter input.

2-110. DAC OUTPUT SWITCHING

The floating outputs of the DAC are switched with latching-type relays K1, K2, K3, K4, and K8.

Relays K1 and K2 determine the polarity of the DAC. In the reset position, the DAC output is positive. In the set position, output is negative. Relay K1 also generates DAC LO DIAG and DAC HI DIAG which are used by the adc circuit during DAC diagnostics.

Relays K3 and K4 switch the DAC to various assemblies. In the reset position, the DAC is available to all assemblies except the oscillator. Relays K3 and K4 are set during operation in the ac function so the DAC output is connected to the DAC/OSC lines which run only to the Oscillator assembly. Also during operation in the ac function, control line DAC OUT SEL turns on FET Q25, via FET Q26, to connect SCOM to RCOM.

Relay K8, when in the set position, allows the DAC to be sensed right on the output of the DAC assembly.

2-111. DAC BUFFERED REFERENCE SIP

The DAC Buffered Reference SIP assembly (A11A2) has two main functions. First, it buffers the the 6.5V and 13V references so they can be used by other assemblies.

The 6.5V reference, REF6, is buffered by op amps U1A and U2A which creates BRF6 and its sense line BSRF6. The 13V reference, REF13 FILT, is buffered by op amps U1B and U2B which creates BRF13 and its sense line BSRF13. These are routed to other assemblies in the calibrator for use during calibrator calibration.

Second, it allows the the reference voltages, or the buffered reference voltages, to be switched to the REFCAL line, which is connected to the inverting input of the adc amplifier by K5 during calibration of the DAC assembly.

Control line REF6 SEL and FETs Q1 and Q2 connect the 6.5V reference REF6 to REFCAL.

Control line BSRF6 SEL and FETs Q5-Q7 tie BRF6 and BSRF6 together and connects them to REFCAL.

Control line REF13 SEL and FETs Q8 and Q9 connect the 13V reference REF13 to REFCAL.

Control line BSRF13 SEL and FETs Q12-Q14 tie BRF13 and BSRF13 together and connects them to REFCAL.

ADC COM can also be connected to REFCAL by FET Q15 and control line ADC COM SEL.

2-112. SELF-CALIBRATION HARDWARE

The main components of the calibration hardware are the adc amplifier and the adc (analog to digital converter). This adc circuitry converts dc analog voltages into 22-bit binary numbers which the software interprets.

2-113. ADC AMPLIFIER

ADC amplifier circuitry is located on page 4 of the DAC schematic. The adc amplifier is used like a null detector. It has two inputs (inverting and noninverting) and a single output with ADC AMP OUT and ADC AMP SENSE connected together.

The noninverting input (+INPUT) is switched between ADC COM, RCL, or DAC SENSE CAL by relays K6 and K7. DAC SENSE CAL is the output of the DAC and RCL is the calibration line which other assemblies use during their calibration.

The inverting input (-INPUT) is switched between DAC SENSE CAL and REFCAL by relay K5. ADC amplifier inputs are high impedance. The output voltage is the voltage difference between the inputs multiplied by the overall adc amplifier gain of 11.

To determine adc amplifier output, the following formula is used: (Noninverting input - inverting input) X 11 = adc amplifier output.

For example if the noninverting input is a 5.0V and the inverting input is at 5.1V, the output would be -1.1V. (The calculation for this example is (5.0V - 5.1V) X 11 = -1.1V.) Op amp U20A configured as an amplifier with an inverting gain of 1 is used to cancel the current in ADC COM generated from op amp U19A.

Zener diodes VR19 and VR20 keep the output of the adc amplifier from exceeding ±4.0V. Similarly, this protection is provided for the adc amplifier inputs by VR17, VR18, VR21 and VR22.

The advantage of having a gain of 11 is that the noise of the adc is divided by this gain. For example, if the noise of the adc is 4 uV rms, the effective noise of the adc becomes 4 uV/11 = 0.36 uV rms, referred to as the adc amplifier inputs.

2-114. ADC INPUT SELECTION

The input to the adc chip, U25, is selected by a quad FET analog switch array, U23. A large filter (R74 and C84) and a buffer (U24) are put on the adc input line to filter out 60 Hz and 190 Hz before it is connected to the adc chip input (pin 22).

During calibrator diagnostics, control line PC2 selects the SDL (system diagnostic line) line, which is used by other analog assemblies to monitor their diagnostic voltages.

During diagnostics of the DAC assembly control, line PC3 selects DAC HI DIAG which is divided by R79 and R84. Control line PC4 selects DCAMP HEATER and REF HEATER which are summed and divided by R80, R81, and R83.

Since DCAMP HEATER and REF HEATER are referenced to FR1 COM, DAC LO DIAG is buffered by U22 to provide the proper current return.

During calibrator calibration, control line ADC OUT SEL selects the output of the adc amplifier.

2-115. ADC CIRCUIT

The adc (analog-to-digital converter) is shown on page 5 of the DAC schematic.

Most of the adc is contained on one chip (U25) which uses the Fluke-patented recirculating remainder technique.

The adc has rms noise of approximately 20 uV between readings. This is reduced by a factor of 5 by averaging the readings. The adc measures input voltages between -1.8V and +1.8V.

Hardware for the adc has four major sections external to adc IC U25. These sections are:

- o ADC reference voltage
- o ADC dac
- o ADC comparator/amplifier
- o Timing/data control circuitry.

The adc reference voltage circuit is made up of zener diodes VR29, VR30, and resistors R91-R93, which generate a 6.4V reference. This -6.4V is inverted by U27B to create the +6.4V reference and is also buffered by U27A and connected to U25. A reference common point for the adc reference is made by buffering ADC COM with op amps U20B and U26A, resulting in an isolated ADC COM. Buffering allows the common point to be referenced to ADC COM, yet current from R85, C89, C90, R93, VR29, and VR30 to return to SCOM through the output of the buffer instead of through ADC COM.

The adc dac contains the dac amplifier, U28B, and a binary ladder network consisting of resistors in Z10. Digitally controlled analog bit switches are contained in U25. The bit switches determine the output voltage of U28B by control of the binary ladder network. The output voltage of U28B can be varied from -1.95V to 1.95V.

The adc comparator/amplifier contains op amp U29, two remainder storage capacitors (C89 and C90), an autozero storage capacitor (C95), and several digitally-controlled analog switches in U25.

The supplies for U29 are bootstrapped off its input voltage. This circuitry includes U28A, VR31-VR34, R95-R100, Q56, Q57, and C97.

The timing/data control circuit is the digital portion of U25. This internal circuitry controls the adc by manipulating the switches in the adc comparator/amplifier and the bit switches in the adc dac.

An adc conversion cycle is triggered by the falling edge of control line ADC TRIGGER from the digital control circuit. Once triggered, the adc, under control by U25, generates five 6-bit nibbles without any further interaction.

Once the adc is triggered, it goes through five measurement cycles. Each cycle is made up of three functions, an autozero function, a compare function and a remainder store function. Figure 2-17 illustrates these three functions.

Before the adc is triggered, it stays in the autozero function. In this function, the adc dac is set to 0V with some offset error. Through U25, pin 3 of U29 is connected to ADC COM and pins 2 and 6 are connected together. In this function, the offset of the adc dac is stored on C95.

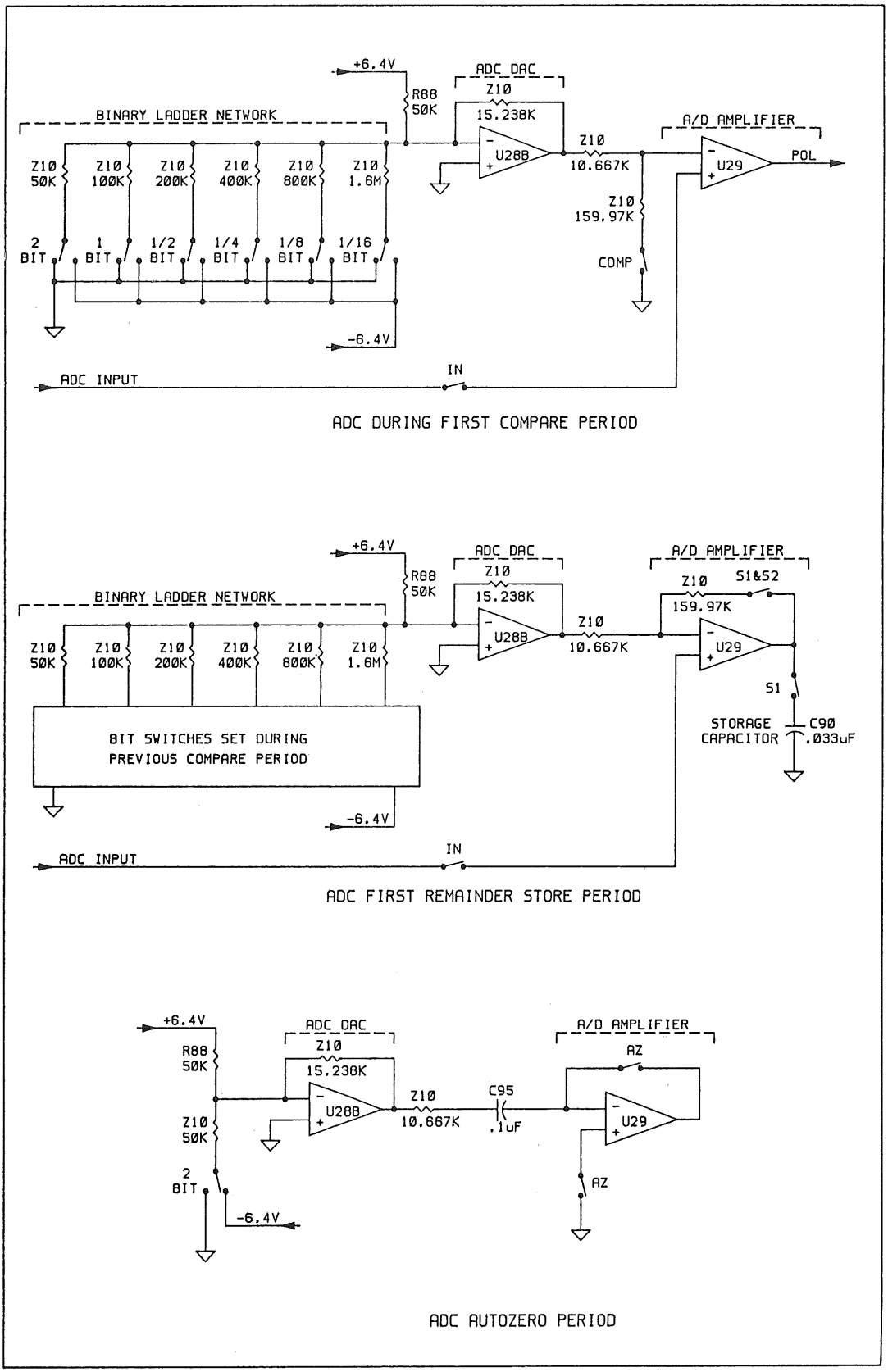

Figure 2-17. ADC Circuit Measurement Functions

In the compare function, U29 compares the adc dac with the adc input (during the first pass) or the stored remainder (C89 or C90) during the remaining four passes. The voltage to be measured is switched into pin 3. The adc dac is connected to pin 2 and adjusted according to the polarity output of U29 resolving the voltage on pin 3. During this function the six bits of one nibble are determined.

During the remainder store function, U29 amplifies and stores the difference between the ADC INPUT and the adc dac output on one of the remainder storage capacitors, C89 or C90. In this function, U29 is configured by the adc as a difference amplifier with a gain of 16. The output of U29 is now the difference between the input voltage and the DAC voltage, multiplied by 16. This voltage is stored on C89 or C90.

On the next cycle, this remainder voltage is switched into U29 as the input voltage during the compare function.

Once this is repeated five times, U25 sends out an interrupt signal (ADC INT) to tell the processor that it is waiting to read. To read the five passes of the adc, the processor reads port A of the 82C55 five times.

For the most critical applications, the adc measures the output of the adc amplifier. Since the output of the adc amplifier is adjusted until it reaches a checkpoint voltage, the adc needs only to be repeatable at this voltage and low in noise. This reduces the constraints on adc linearity and long term stability which allows a much simpler adc reference to be used.

2-116. HOW THE DAC IS USED IN SELF-CALIBRATION

For internal and external calibration, the adc amplifier output is switched to ADC INPUT.

The adc amplifier acts as a null meter. It measures the voltage difference between its inverting and noninverting inputs and amplifies it by a gain of 11.

The adc amplifier can measure common-mode voltages up to 14V. Input switching circuitry allows the DAC SENSE, buffered and unbuffered reference, RCL, and ADC COM to be switched into the adc amplifier inputs.

To make a typical cal measurement, software sets the DAC to the approximate expected common-mode voltage. The DAC is then switched into both adc amplifier inputs and an adc reading is taken. This is the checkpoint measurement. It represents the adc amplifier common-mode and offset error, and the errors in the adc and adc amplifier input switching. The unknown voltage is switched into one input of the adc amplifier and the DAC is adjusted by software until the adc reading matches the checkpoint reading. At this point the unknown voltage is equal to the DAC voltage and is represented by the current DAC counts.

2-117. DAC ASSEMBLY CALIBRATION

The DAC assembly is completely characterized using a single external 10V source. Calibration occurs in the following steps:

Ratio calibration of the first and second channels is performed first. The first channel count is set for a DAC output of near 0V. The second channel count is set to its minimum value of approximately 10,000. The DAC output is connected to the input of the zero amplifier on the Switch Matrix assembly (A8) and its output connected to the +input of the adc amplifier via the RCL line and the -input is connected to ADC COM.

The adc measures this value and stores it as a checkpoint reading. The first channel is decremented by one count and the second channel is increased until the adc reads the same as the previous checkpoint. The number of counts the second channel is increased represents the channel ratio constant.

The ±11V and ±22V range zeros are calibrated next. This is done by the same technique as the ratio cal except the checkpoint reading is obtained by connecting the input of the zero amplifier on the Switch Matrix assembly to RCOM. The DAC output (DAC SENSE CAL) is then connected to the zero amplifier input and adjusted until the adc reads the same as the previous checkpoint. This determines the exact first and second channel counts for a 0V output.

Next, the +11V and +22V range gain constants are calibrated by nulling the DAC to the external 10V source, connected to the front panel binding posts of the calibrator. This 10V source is connected to the RCL line by relays on the Switch Matrix assembly (A8).

The RCL line is connected to the +INPUT of the adc amplifier. The DAC output is connected to the -INPUT of the adc amplifier and is adjusted until the adc reads a null. This determines the first and second channel counts required for an exact 10 V output from the DAC. Software determines floating point gain constants from these counts.

The exact value of all the reference voltages (6.5V and 13V) are determined next. The reference voltage to be determined is connected to the -INPUT of the adc amplifier. The DAC output is connected to the +INPUT and adjusted until the adc reads a null. The reference voltage is the value to which the DAC is set. This procedure is done for the 6.5V buffered and unbuffered, and 13V buffered and unbuffered references.

2-118. Oscillator Section Overview

The ac module consists of two plug-in assemblies, the Oscillator Output assembly (A13) and the Oscillator Control assembly (A12). These assemblies generate a precision amplitude-stabilized ac sine wave from 0.22V to 22V with a frequency range of 10 Hz to 1.2 MHz. This signal is either routed to the OUTPUT binding posts if the desired output is within this range, or used internally by the Power Amplifier, High Voltage, Wideband, Current, Switch Matrix, or an Auxiliary Amplifier (Model 5725A, 5205A, 5215A, or 5220A) for voltages and/or functions outside this range.

Output sensing of the amplitude helps obtain an accurate output signal regardless of output amplitude and load variations. Sensing is available for all voltage ranges above 200 mV at the calibrator SENSE binding posts. In the current function, and for voltages less than 200 mV, sensing is performed internally and output accuracy is guaranteed only for specified operating conditions.

The Oscillator Output assembly (A13) creates an ac voltage. The Oscillator Control assembly (A12) controls the amplitude of this ac signal by comparing the SENSE HI signal from the Oscillator Output with an accurate dc voltage from the DAC assembly (A11). The Oscillator Control assembly adjusts the amplitude of the Oscillator Output via the OSC CONT line. The frequency accuracy is controlled by the phase-locked loop circuit on the Oscillator Output assembly, which phase locks to the signal created by the Current/Hi-Res assembly (A7), or to an external signal connected to the 5700A rear panel through the PHASE LOCK IN jack.

The following discussions separately cover these two assemblies.

2-119. Oscillator Control Assembly (A12)

The Oscillator Control assembly (A12) contains all the precision ac amplitude control circuitry except the output AGC amplifier, which is located on the Oscillator Output assembly (A13). The primary function of the Oscillator Control assembly is to monitor the output of the 5700A in the ac voltage function, and to adjust the output until the rms voltage across the SENSE point is equal to the voltage requested by the operator. This assembly provides amplitude control for both the ac current function and the Wideband AC Module (Option -03) during low-frequency operation.

The oscillator control circuitry contains an averaging converter, an error intergrator, a three-pole filter, an ac/dc thermal transfer circuit, an ac/ac thermal transfer circuit, a 15-bit dac, and a digital control circuit.

All power supplies used by this assembly are generated by the Guard Crossing/Regulator assembly (A17) except the +5 OSC supply, which is generated by a three-terminal +5V regulator (U25) from the +15 OSC supply. The ±15 OSC supplies are buffered by L3, L4, C34 and C35 to create the ±15A supplies, and L1, L2, C86 and C87 to create the ±15B supplies. A +2.5V reference voltage is created from the +5LH supply by resistors R52 and R53. A -200 mV reference voltage is created from the -15V OSC supply by resistors R57 and R58 for use exclusively by the protection circuitry for the thermal sensors U14 and U16.

2-120. OSCILLATOR CONTROL DIGITAL CONTROL

The digital control circuit contains an 82C55 Programmable Peripheral Interface (U20) and latching relay drivers (U23, U24). The 82C55 is controlled via the guarded digital bus, and has three ports that generate 24 outputs. Port A (PA0-PA7) is a common input bus (DATA) for the relay drivers (U23, U24) and the 14-bit DAC (U10). Relay driver U23, which controls latching relays K1 through K4, K6, and K8, is strobed by PC5 and enabled by PC7 of port C. Relay driver U24, which controls latching relays K5, K7, and K9, is strobed by PC6 and enabled by PC7 of port C. The SW control bus contains control lines SW1-SW4 from PB4-PB7 of port B which control a CMOS analog switch IC U19. PC1-PC4 of port C create control lines GCAL, AC*/DC, DAC* and BIT14* respectively. The Oscillator Output assembly (A13) generates two more control lines: LFCOMP* and HFCOMP*. These control lines are routed to this assembly via the Motherboard and enter on pins 18A/C and 19A/C of connector P502.

A self-diagnostic circuit contains a multiplexer (U18) and resistor networks Z5 and Z6. It monitors ±15V, VREF, and the outputs of the error integrator and 14-bit DAC. These inputs are divided by the resistor networks, while U18 applies one to the SDL line. The SDL line is routed to the DAC assembly (A11) to be measured by the adc circuit.

2-121. OSCILLATOR INPUT SWITCHING

Relay K1 selects an input to the Oscillator Control assembly. During ac voltage operation, relay K1 is reset. This connects the input (SENSE HI) to the averaging converter and the ac sense buffer to OSC SENSE HI. The reference voltage, VREF, is connected to both DAC/OSC OUT HI and DAC/OSC SENSE HI, which is the dc voltage from the DAC assembly (A11). During internal calibration K1 is set, so VREF is the 6.5V reference voltage (BRF6 and BSRF6) from the DAC assembly. The input to the averaging converter and ac sense buffer is DAC/OSC OUT HI and DAC/OSC SENSE HI from the DAC assembly.

2-122. SENSE CURRENT CANCELLATION

The SENSE HI current cancellation circuit, containing op amp U1, Q1, Q2, K8, K2B and associated components, supplies the current into SENSE HI (Z2 pin 1) so that no current is pulled from the OSC SENSE HI line. During operation in the 2.2V and 22V, range K8 is set so the input is OSC OUT. In the 220V range K8 is reset so OSC SENSE HI is connected to the input. Relay K2B is reset in the 2.2V range and set in the 22V range. Transistors Q1 and Q2 form a bootstrapped supply for U1.

The SENSE LO current cancellation circuit, built around op amp U2, forces the return current back to SCOM instead of OSC SENSE LO. Relay K2A is reset in the 2.2V range and set in the 22V range.

To better understand the detailed circuit descriptions for the averaging converter, error intergrator, and three-pole filter, refer to Figure 2-18.

2-123. AVERAGING CONVERTER

The averaging converter contains the buffer amplifier and rectifying amplifier circuits as outlined on page 1 of the schematic.

The buffer amplifier is a non-inverting unity gain amplifier (U3). Input to the buffer amplifier is either a 0 or 20 dB attenuator contained in Z2 as selected by K3. In the 2.2V range, SENSE HI is connected directly to the buffer amplifier with K3 in the reset position. In the 22V range, K3 is in the set position, so the buffer amplifier input (SENSE HI) is attenuated 20 dB by the 18 kilohm and 2 kilohm resistors in Z2. The buffer amplifier output voltage is always between 0.22 and 2.2V, and is capacitively coupled to the rectifying amplifier by C22 and C25.

The rectifying amplifier is comprised of U5, U7, Q3 and Q4, and has an inverting gain of 2. When the input voltage (from the buffer amp) is positive, feedback is negative through CR5 and a 2 kilohm resistor in Z1 (pins 6 and 5). When the input voltage is negative, the feedback path is through CR4 and a different 2 kilohm resistor in Z1 (pins 3 and 5). This amplifier produces a full-wave rectified negative output current proportional to input voltage. Output current is summed at the input of the error intergrator with the positive adjustable reference current (VREF, which is the output of the DAC assembly).

2-124. ERROR INTEGRATOR

The error integrator circuit contains op amp U11, CMOS analog switch U8A, and capacitors C42 and C43. When operating at frequencies above 119 Hz, op amp U11 and C43 form an integrator. When operating at frequencies below 119 Hz, control line LFCOMP* goes low to close U8A, adding C42 to C43. This reduces the integrator crossover point by a factor of ten. If the magnitude of the averaging converter dc output current is different than the reference current, the output of the error integrator begins to change. Error integrator output goes through a three-pole filter and is buffered by U9A to generate OSC CONT. OSC CONT is routed to the Oscillator Output assembly to adjust the Oscillator amplitude. The output of the error integrator is also monitored by the diagnostic circuit via ERROR INT. OUT.

2-125. THREE-POLE FILTER

The three-pole filter contains op amp U9B, CMOS analog switches U8B-U8D, and C26-C31. This circuit filters out ac from the output of the error integrator. Control line LFCOMP* goes low when operating at 119 Hz or less to reduce the crossover point.

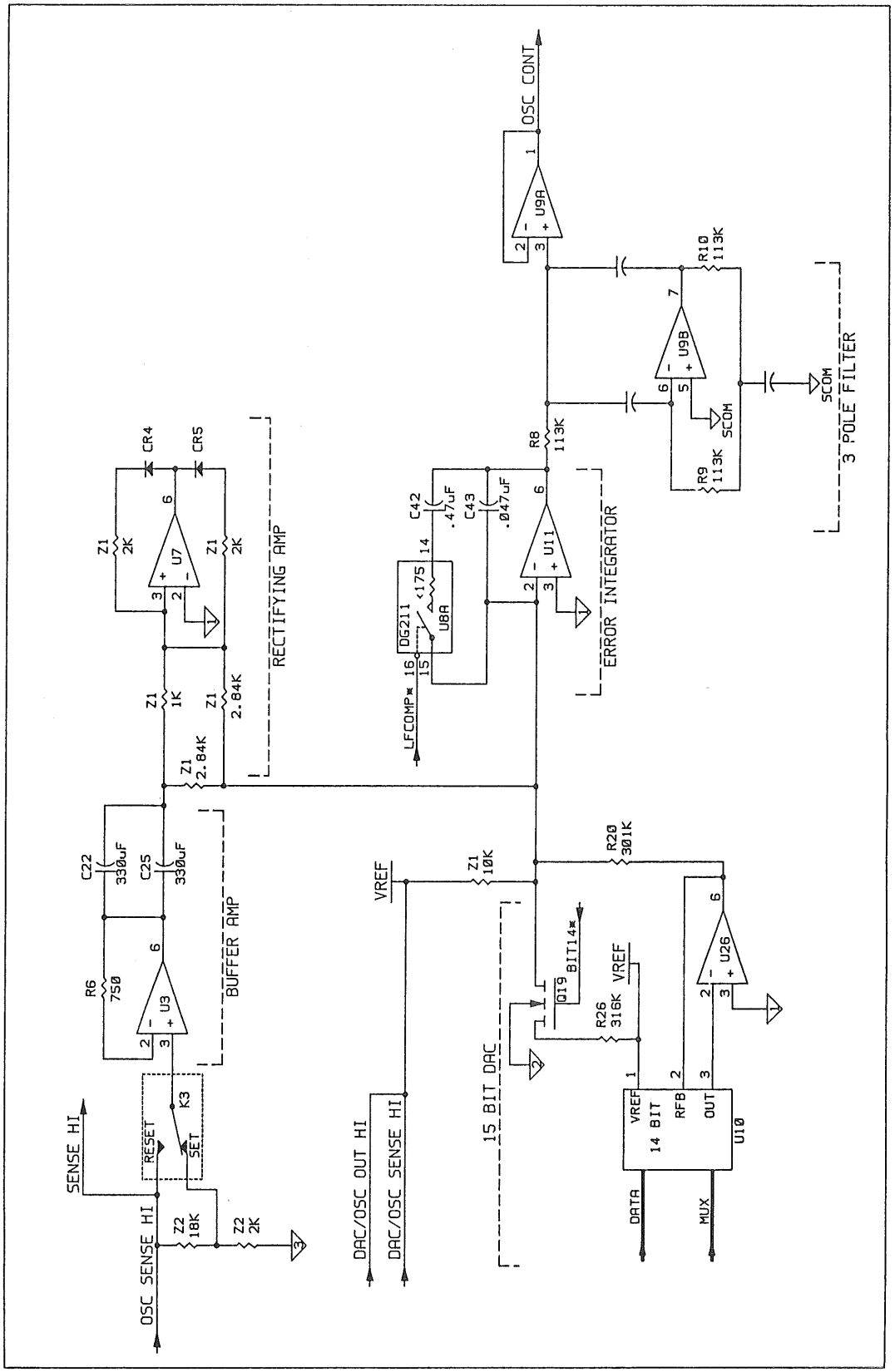

Figure 2-18. Oscillator Control Analog Control Loop

2-126. ANALOG AMPLITUDE CONTROL LOOP

This loop is comprised of the averaging converter, error integrator, three-pole filter, and the agc amplifier on the Oscillator Output assembly (A13). It stabilizes the 5700A output voltage in the presence of load changes. This loop by itself is very stable but does not have the conversion accuracy or gain flatness necessary to meet the precise amplitude specifications of the 5700A. Thus this circuit is used only to provide quick load regulation recovery and short term output stability.

2-127. AC/DC THERMAL TRANSFER CIRCUIT

Refer to Figure 2-19 for the following discussion. The ac/dc thermal transfer circuit achieves basic mid-band amplitude accuracy. This is done by first applying the reference voltage (VREF) to the thermal rms sensor (U14) and measuring the output. Next, the ac voltage is applied to the thermal rms sensor and the dc output is compared to the previous reading. The sensor detects the difference between the ac and dc input voltages to within a few ppm.

If there is an ac/dc difference, the dc reference current applied to the error integrator of the analog control loop is adjusted via the 15-bit dac until the ac/dc difference is zero. The ac/dc thermal transfer circuit that performs this function is further described in detail. It contains the the dc sense buffer, ac sense buffer, ac/dc thermal sensor, and the square-root amplifier and 15-bit dac as outlined on the schematic.

As previously mentioned, the input to the thermal rms sensor is either the dc reference voltage (VREF) buffered by the dc sense buffer or the ac voltage (SENSE HI) buffered by the ac sense buffer.

The dc sense buffer circuit uses op amp U30 as a buffer amplifier. Enhanced-mode FET Q10 provides feedback for U30 while FETs Q8 and Q9 are off. During a dc transfer, control line AC*/DC and comparator U21C turn on the FETs, applying the output of the dc sense buffer to the input of thermal rms sensor U14.

The ac sense buffer circuit contains op amps U12A, U12B, U13; FETs Q6, Q7, Q11, Q12; relay K4, and associated components. Relay K4 selects the input resistance to amplifier U13, which has a nominal inverting gain of 0.316 in the 22V range and 3.16 in the 2.2V range.

During operation in the 22V range, relay K4 is set, feeding the input, SENSE HI, through the 20 kilohm resistor in Z3. When operating in the 2.2V range, the 2.22 kilohm and 20.0 kilohm resistors in Z3 are put in parallel by K4 in the reset position, reducing the input resistance to 2 kilohm.

During an ac transfer, control line AC*/DC and comparator U21D turn on FET Q12 so the output of amplifier U13 is applied to the input of thermal rms sensor U14. At this time, FET Q11 is turned off and the feedback path for U13 is through the 6.32 kilohm resistor in Z3.

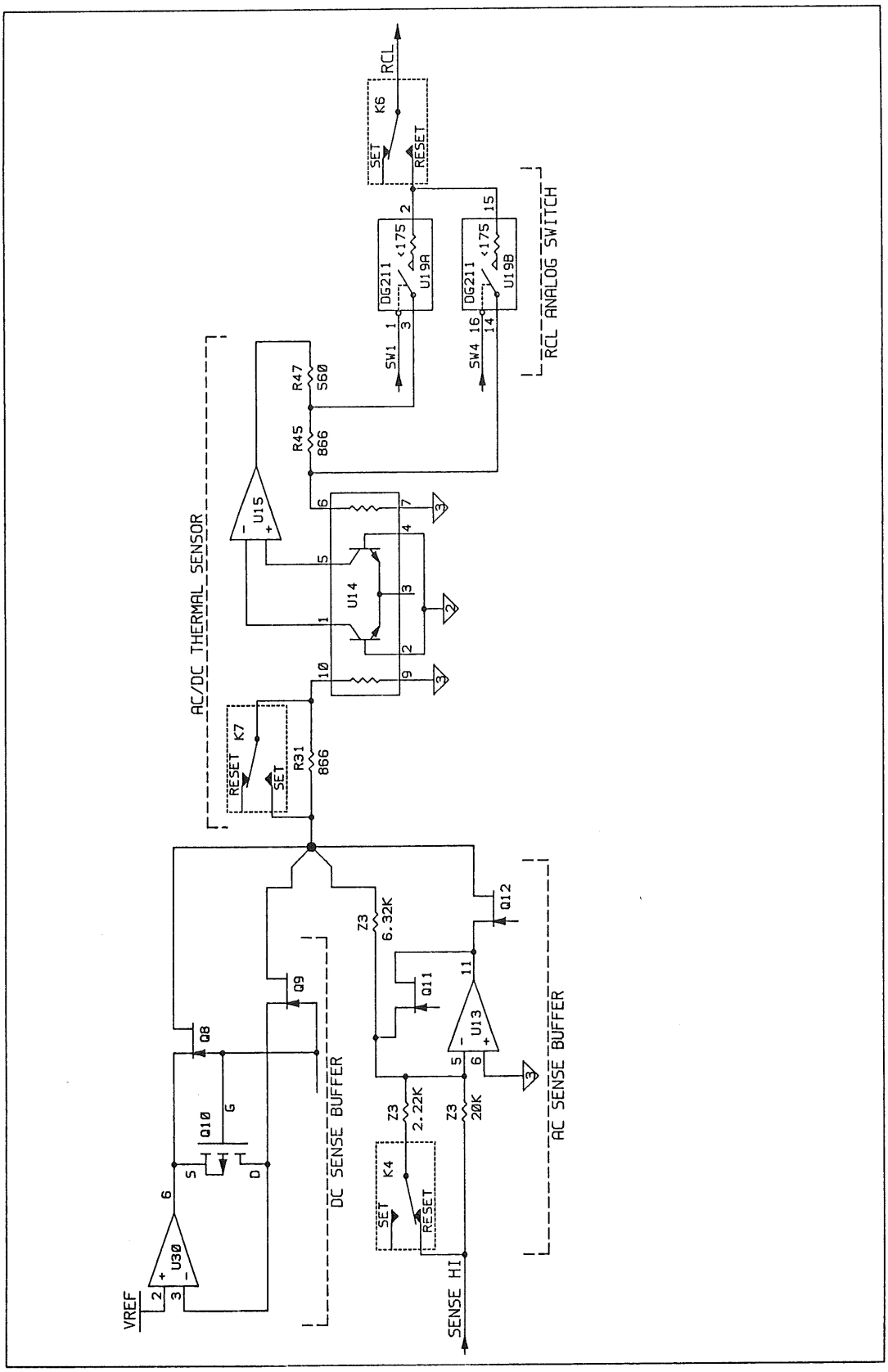

Figure 2-19. AC/DC Thermal Transfer Circuit

During a dc transfer, Q12 is off and comparator U21B turns on FET Q11, providing the feedback path for U13. Op amps U12A and U12B provide low offset and increase the gain. Control line HFCOMP and comparator U22C turn on FETs Q6 and Q7 during operation in the 1 MHz range.

The output of either the dc sense buffer or the ac sense buffer becomes the input of thermal rms sensor U14. During operation from 0.22V to 0.7V in the 2.2V range, or 2.2V to 7V in the 22V range, relay K7 is set, directly connecting the input signal to the sensor. The input to the thermal sensor is through R31 by K7 in the reset position during operation from 0.7V to 2.2V in the 2.2V range, or 7V to 22V in the 22V range.

Comparator U21A provides protection for thermal rms sensor U14. If the junction temperature of the sensor goes above 200 oC, the voltage at pin 3 increases, driving the output of U21A negative. This turns off the FETs controlling the output of the dc sense buffer and ac sense buffer, removing the input to the thermal sensor.

The ac/dc thermal sensor and square-root amplifier, as outlined on the schematic, contain the thermal sensor U14, op amp U15 and transistor array U17. The dc voltage from the thermal sensor is connected to U15B configured as an integrator. Comparator U22B is used to control FETs Q18 and Q20. These FETs are turned on, adding C84 and C62 to the integrator, by control lines LFCOMP* and AC*/DC both at logic low. The output of integrator U15B is used by the square-root amplifier contained in U15A, U15C and U17. This circuit keeps the settling time of the sensor constant when its input is varied between full and 1/3 scale. The output of the sensor is connected to the RCL line by relay K6 and CMOS analog switch U19A and U19B. During operation from 0.22V to 0.7V in the 2.2V range, or 2.2V to 7V in the 22V range, sensor output is connected to the RCL line through buffer U31, U19B, and K6 in the set position. During operation from 0.7V to 2.2V in the 2.2V range, or 7V to 22V in the 22V range, sensor output is connected to the RCL line through U19A and K6. Control lines SW1 and SW4 control U19A and U19B respectively. The RCL line is routed to the DAC assembly (A11) where its amplitude is measured by the adc circuit.

To do an ac/dc transfer, the dc sense buffer is connected to the thermal sensor and the sensor output is connected to the +input of the DAC's adc circuit. The -input of the adc circuit is connected to the DAC output (VREF), and the difference between the two is measured and stored in memory. Next, the output of the ac sense buffer is connected to the sensor and the sensor output is connected to the +input of the DAC's adc circuit. The difference is measured and compared to the previous reading. The difference between these two readings is the difference in rms value of the ac and dc input voltages. If there is an ac/dc difference, the dc reference current applied to the error integrator of the analog control loop is adjusted via the 15-bit dac until the ac/dc difference is zero.

The 15-bit dac contains an AD7534 dac IC (U10), FET Q19 and op amp U26. The first 14 bits (bits 0-13) are generated by the dac IC U10, and bit 14 is generated by Q19, R26, and control line BIT14. Control busses DATA and MUX from the digital control circuit select the data and address for U10. The output is inverted by U26 to create 14 BIT DAC OUT, which is applied to the summing node of the error integrator by R20. This output is also monitored by the diagnostic circuit.

2-128. OSCILLATOR CALIBRATION

Calibration consists of determining the offset and gain errors of the ac/dc switching circuitry. Errors are measured at dc using the calibrator DAC and the 6.5V reference as the primary sources of accuracy. This characterization is valid for frequencies up to 1 kHz. Above 1 kHz, ac/ac characterization is used to insure the output accuracy.

The DAC assembly (A11) is set to 0V with its output connected to the ac sense buffer (via SENSE HI) by relay K1 in the set position. The output of the ac sense buffer is connected to the RCL line by K6 in the set position and by control line GCAL and comparator U22A turning on Q13. The 0V input is stored as Vin1. The output measured by the adc circuit on the DAC assembly is stored as Vout1.

Relay K1 ties 6.5V reference BRF6 and BSRF6 to VREF, where it is measured at the output of the thermal sensor in the same manner as a dc transfer. This measured output is stored in memory.

The DAC output is set to 20V or 2V and is measured at the output of the thermal sensor in the same manner as an ac transfer. The DAC is then adjusted until this measured output is the same as stored in the previous step. The DAC setting is stored as Vin2 and the 6.5V reference is Vout2. The gain can now be calculated with the formula: (Vout2 - Vout1)/(Vin2 - Vin1).

2-129. AC/DC FREQUENCY RESPONSE CHARACTERIZATION

Characterization is accomplished by first performing an ac/dc transfer with the Oscillator Output set to a low frequency. The ac/ac thermal sensor circuit, containing the thermal sensor U16 and op amp U15D, characterizes the frequency response of the main ac/dc thermal sensor. This sensor has no active circuitry at its input, and all switching is done by relays to insure a flat frequency response.

In the 20V range, the Oscillator Output is switched through R34 to the ac/ac thermal sensor via SENSE HI, K5, and K9 in the set position. In the 2.2V range, R34 is bypassed by K9 in the reset position. The output of this sensor is routed to the RCL line via U19C and K6. A reading is taken and stored in memory as ACref.

The output frequency of the Oscillator Output is changed to the first cal point and the 15-bit dac is adjusted until the reading from this ac/ac thermal sensor is the same as ACref.

The RCL line is then switched back to the ac/dc thermal sensor. A reading is taken stored in memory as ACdif. The gain constant is calculated using the formula (ACdif + Vdac)/Vdac, where Vdac is the DAC assembly (A11) voltage.

This ac/ac transfer function is also performed for the 220V range and the 1100V range. These ranges are generated by the Power Amplifier assembly (A16) and the High Voltage/High Current assemblies (A14 and A15). High voltage ac signals are attenuated and connected to AC CAL, where they are connected to the sensor though relay K5 in the reset position. In the 220V range, the output of the sensor is divided by Z4 and connected to the RCL line by U19D and K6.

Protection for this thermal sensor is provided by comparator U22D, FET Q14, zener diodes VR5, VR6, resistor network Z10, and diodes CR12 and CR13. During normal operation, U22D keeps Q14 off. If the junction temperature of the sensor goes above 200 oC, the voltage at pin 3 increases, driving the output of U22D positive. This turns on Q14, shunting the input of the sensor to common through CR12 and CR13.

2-130. Oscillator Output Assembly (A13)

The Oscillator Output assembly is controlled by the Oscillator Control assembly. Refer to Figure 2-20 and the schematic diagram for the following discussion.

The Oscillator Output assembly generates an ac sine wave from 0.22V to 22V with a frequency range of 10 Hz to 1.1999 MHz. There are five frequency ranges (100 Hz, 1 kHz, 10 kHz, 100 kHz and 1 MHz) and two voltage ranges (2.2V and 22V). The output signal is either routed to the OUTPUT binding posts, or it is used internally by the Power Amplifier, High Voltage, Wideband AC Module (Option -03), Current, or Switch Matrix assemblies, or it is routed to an Auxiliary Amplifier for generation of voltages and/or functions outside this range. Output sensing is available for all voltage ranges above 220 mV at the SENSE binding posts.

The Oscillator Output assembly contains a fixed-amplitude quadrature RC oscillator, a 0.22-22V digital/linear gain-controlled amplifier, a fixed-amplitude variable phase-shifting network, phase-locked loop control circuitry for phase locking to an external signal or the PLOCK signal from the Current/Hi-Res assembly (A7), and digital control circuitry.

All power supplies used by this assembly except the -12S supply are generated by the Guard Crossing/Regulator assembly (A17). The -12S supply is generated on this assembly by a three-terminal -12V regulator (U2) using the -17S supply as its input.

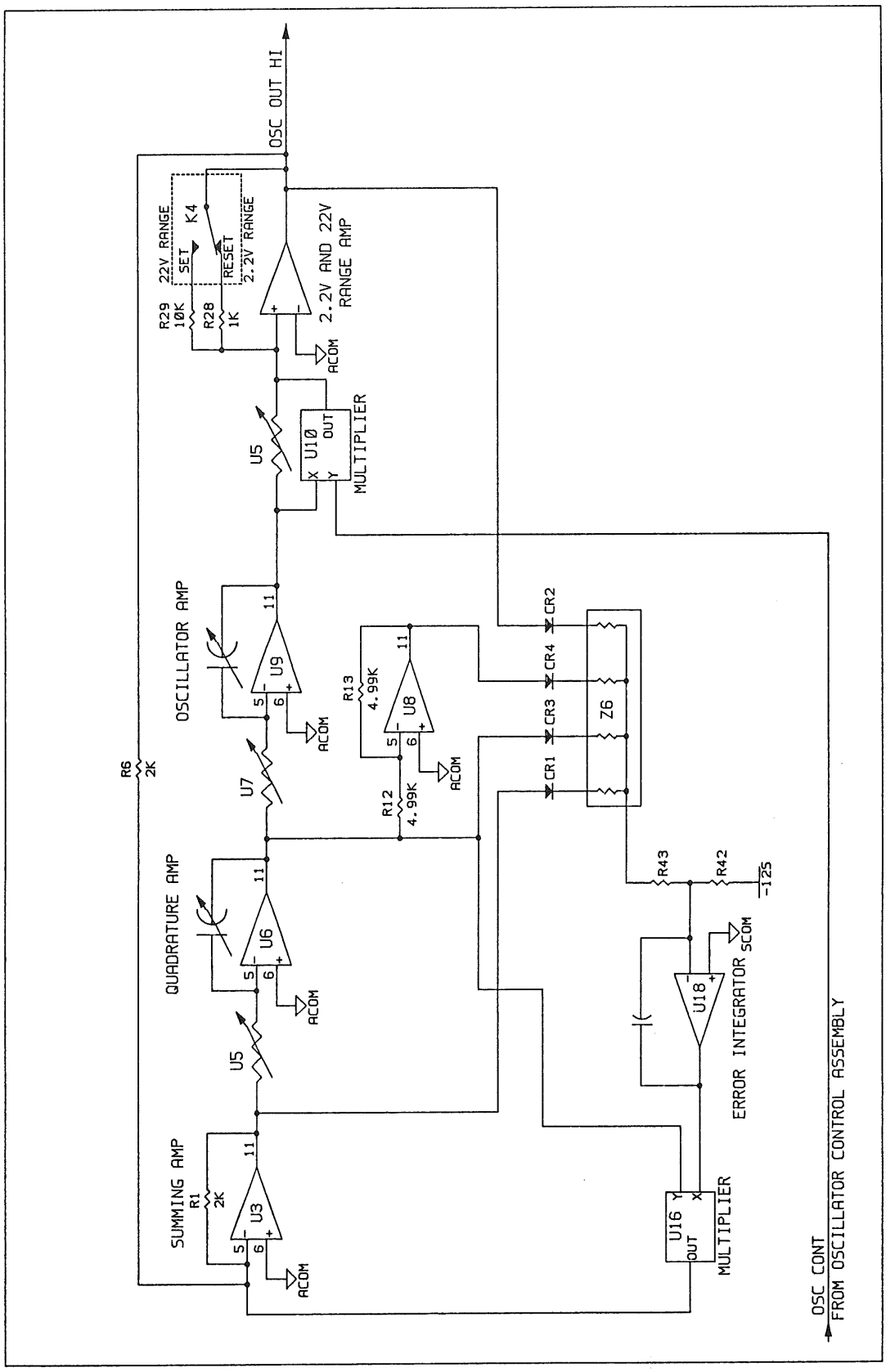

Figure 2-20. Quadrature RC Oscillator Circuit

2-131. OSCILLATOR OUTPUT DIGITAL CONTROL

The digital control circuit consists of an 82C55 Programmable Peripheral Interface (U26), a 5801 Latching Relay Driver (U24), and three HC374 Octal D-Type Flip Flops (U12, U32, U33). The Programmable Peripheral Interface (U26) is under software control via the guarded digital bus and has three ports which generate 24 outputs. Port A (PA0-PA7) is a common input bus for U24, U12, U32, U33, and U28. Latching relay driver U24 controls the four latching relays K1-K4. Relays K1-K3 select the frequency range and K4 selects the voltage range. This IC is strobed by PC3 of port C and enabled by PC6 of port C. To insure that the relays are latched properly the driver must be enabled for 10 ms.

Latch U32 is clocked by PC0 and generates the data bus FREQ DATA for controlling 8-bit resolution hybrid resistive dacs U5 and U7. Latch U12 is clocked by PC1 and generates the data bus AMPL DATA for controlling U11, which is identical to U5 and U7. Latch U33 is clocked by PC2 and generates control bus PHASE, which controls multiplexer U27 in the phase shifter circuit and control bus MUX, which controls the SDL multiplexer U25 in the diagnostic circuit. This diagnostic circuit monitors the $\pm$44S supplies, $\pm$15S supplies, INTEGRATOR OUT, LOOP FILTER OUT, and $\overline{\text{AMP1}}$ which is from U30, the A13A1 assembly. These voltages are divided by Z2 and Z3 and connected to the SDL line by multiplexer U25, where they are measured by the adc circuit on the DAC assembly (A11).

PB0-PB2 of port B generates control bus PLOCK RNG which is used in the phase-locked loop circuit. PB4 is control line 0/180 to control FET Q7 via comparator U31B in the phase-locked loop circuit. PB6 is control line LFCOMP* to control FET Q6 via comparator U20A in the integrator circuit. PB7 is control line HFCOMP*, which is routed to the Oscillator Control assembly (A12). PC4 and PC5 are control lines DAC STRB and DAC SEL respectively, which control the dual 8-bit dac U28 in the phase shifter circuit. PC7 is control line INH to enable the multiplexer U25 in the diagnostic circuit.

2-132. QUADRATURE RC OSCILLATOR

The quadrature oscillator is a double integrator type. It contains two op amp RC integrators and a unity-gain inverting summing amplifier. The integrators are identical and use relay-switched feedback capacitors to select five frequency ranges. An 8-bit resolution resistive dac selects frequency within a range.

The summing amplifier uses op amp U3 to provide a 180° phase shift in the oscillator loop at unity gain. Its exact phase shift and gain are adjusted by the amplitude control and phase-locked loop circuits to satisfy the conditions required for amplitude stable oscillation: exactly 360° loop-phase and unity gain. This amplitude control circuit uses an integrator and multiplier as outlined on page 1 of the schematic. These two circuits are described in detail later.

The two op amp RC integrators are the quadrature amplifier and the oscillator amplifier. Their purpose is to provide -90° each to the loop phase with an amplitude slope of -20dB/decade. The quadrature amplifier contains op amp U6, 8-bit resolution resistive dac U5, and relays K1B, K2B, and K3B. The relays select feedback capacitors C25, C24, C22, and C21 for frequency ranges 100 Hz, 1 kHz, 10 kHz and 100 kHz respectively. For the 1 MHz range, all the above capacitors are removed from the loop, and the only feedback path is C19. The input resistor is the 8-bit resolution resistive dac U5 which is under the control of the FREQ DATA bus from the digital control circuit. Its equivalent resistance is R = (256/X)*2 kilohm, where X is the digital code on the FREQ DATA bus. The oscillator amplifier contains op amp U9 and performs the same function as the quadrature amplifier. Its input resistance is controlled by resistive dac U7. Relays K1A, K2A, and K3A select the feedback capacitance. Since their phase shift is constant with frequency and the sum of the phase shifts around the loop is zero for all frequencies, we have satisfied one half of the requirement for oscillation. In summing the gain in dB around the loop it is apparent that unity gain occurs at only one frequency. This happens when the closed loop gains of the integrators are unity. This corresponds to F = 1/(2 x PI x R x C), which is the frequency of oscillation.

2-133. OSCILLATOR AMPLITUDE CONTROL

Since small excess phase shifts exist in all three amplifiers and the gain of the summing amplifier cannot be made exactly one, it is impossible to generate an amplitude-stable sinusoidal waveform from just these elements. A control circuit consisting of an error integrator and a linear four-quadrant multiplier is used to sense the output amplitude and stabilize it by adjusting the loop phase shift slightly.

To do this, a fourth oscillator signal is generated using U8 to invert the output of the quadrature amplifier. The Oscillator now has four equal-amplitude signals all spaced 90° apart. These signals are rectified and summed by CR1-CR4 and Z6 in such a way that a dc representation of the output amplitude is created. This dc signal is summed with a -12V reference voltage by the error integrator circuit which contains op amp U18. If there is a magnitude difference between the rectified dc and the reference, the output of the error integrator changes. This in turn controls the amplitude of the oscillation. This is done via multiplier U16, a linear-variable resistance with a value inversely proportional to the error integrator output voltage.

If the control input (x input) to the multiplier is zero, the equivalent resistance from the signal input (y input) is infinite. If the control input is negative, the equivalent resistance is negative. The Y signal input of the multiplier is the quadrature amplifier output. Any nonzero control voltage changes the phase shift of the loop by injecting a small amount of out-of-phase current into the summing amplifier. This negative feedback is used to stabilize the amplitude of the oscillating signal by allowing one output amplitude only to satisfy the required conditions of oscillation. During operation in the 100 Hz range, control line LFCOMP* and comparator U20A turn off FET Q6.

2-134. PHASE-LOCKED LOOP

The Oscillator Output assembly is phase locked to an external frequency to increase frequency accuracy. This external frequency comes from the High-Resolution Oscillator on the Current/Hi-Res assembly (A7) or from an external source connected to the rear-panel PHASE LOCK IN jack.

The frequency capture range is approximately ±5% of the nominal output frequency range. This is done by comparing the oscillator output frequency SUMMING AMP OUT or INT OSC OUT against the external frequency source P LOCK HI with a phase detector. The P LOCK HI signal is referenced to P LOCK LO. The phase-locked loop circuit locks SUMMING AMP OUT to the external frequency when the calibrator is in the 22V range or less. The phase-locked loop circuit locks INT OSC OUT, which is 180° out of phase from SUMMING AMP OUT, during calibrator operation at higher voltages. This occurs because the output from the Power Amplifier and High Voltage assemblies (which are used to generate the higher voltage ranges) are 180° out of phase from the Oscillator output. When the 5700A is in the higher voltage ranges, control line 0/180 and op amp U31B turn on Q7, which selects INT OSC OUT to the Zero Crossing Detector.

Since the phase detector circuit requires digital inputs, both signals are converted to square waves using U23A/B as dual zero crossing detectors. Square waves from the zero crossing detector circuitry are fed to the phase detector circuit containing U22A/B and U21. The phase detector circuit looks for the falling edge of both signals. The first signal that makes a positive to negative transition causes the phase detector to turn on either the positive (CR5, CR6) or the negative (CR7, CR8) charge pump, depending on which signal is first. The Charge Pump is turned off when the other signal makes its transition. Thus the signal with the highest frequency has its respective charge pump pulsed on and off while the other charge pump remains off.

The accumulated charge is integrated by the loop filter circuit, which contains op amp U31A, multiplexer U17, Z1, and C75-C84. Multiplexer U17 is controlled by the PLOCK RNG control bus from the digital control circuit. This multiplexer changes the cross-over point of the loop filter by selecting C83 and C84 for feedback in the 100 Hz range. Capacitors C81 and C82 are used for the 1 kHz range, C79 and C80 for the 10 kHz range, C77 and C78 for the 100 kHz range, and C75 and C76 for the 1 MHz range.

The output of the loop filter controls two multipliers (U15 and U19) similarly to the amplitude control section. The only difference is that the signal input is derived from the in-phase signal. In the case of U15, the input signal is QUADRATURE AMP OUT, which changes the unity-gain frequency of the oscillator amplifier. In the case of U19, the input signal is SUMMING AMP OUT, which changes the unity-gain frequency of the quadrature amplifier. The new frequency of oscillation is the new unity gain frequency of the integrators. Under phase-locked conditions, neither charge pump is allowed to turn on because neither signal reaches the phase detector first.

2-135. 2.2V AND 22V RANGE OUTPUT AMPLIFIER

The 2.2V and 22V range output amplifier is an inverting wide-band low-distortion amplifier that provides output signal OSC OUT HI at the OUTPUT binding posts in the 2.2V and 22V ranges. OSC OUT HI is used by the Power Amplifier and High Voltage assemblies to generate the higher voltage ranges.

This amplifier uses a surface-mount gain block (U30) called the Oscillator Wideband SMD PCA (A13A1) and a complementary Darlington emitter follower bootstrapped output stage. Relay K4 selects feedback resistor R28 for the 2.2V range and R29 for the 22V range. It also changes the open-loop frequency response for each voltage range. Its gain within a range is controlled by the gain control multiplier circuit and the dac gain control circuit.

The dac gain control circuit contains the same 8-bit resolution resistive dac (U11) as in the oscillator with the exception that it is controlled by the AMPL DATA control bus from the digital control circuit. This resistive DAC provides the coarse gain control. The gain control multiplier circuit contains a multiplier U10, which provides a small linear control range of several dac counts. The control input to the multiplier, OSC CONT, comes from the Oscillator Control assembly (A12). This allows the output amplitude to be adjusted as required by the Oscillator Control Assembly. The theory of operation for the rest of the output stage is described following the A13A1 theory.

2-136. Oscillator Wideband SMD Assembly (A13A1)

The A13A1 is a surface-mount assembly on the Oscillator Output assembly (A13) that provides the 22V output signals of the 5700A. It is essentially an operational amplifier built using discrete components to provide the necessary speed, power output and breakdown voltage required for such a high output signal.

The input stage is a differential pair (Q2 and Q3) that is buffered by a source follower Q1. The transconductance is determined by R3, R4 and R26. The inherent input offset voltage of this stage is corrected by U1 and U2 and related components. The output of Q3 is level-shifted by VR5-VR7 before being applied to the mid stage. Transistor Q4 serves as a high-impedance current sink used to bias the input stage to approximately 10 mA. Potentiometer R30 adjusts the dc zero at the output of U2.

The mid stage is a common-emitter, Miller-compensated gain stage (Q5) that drives a common-base level shifter (Q13) on the Oscillator Output assembly. This stage is current limit protected by R12 and Q4. The dominant pole is set with the Miller capacitor C5 and the input stage transconductance. The mid stage is biased to 10 mA by Q6 and related components.

The output stage of the amplifier is a bootstrapped complementary Darlington pair. The only parts of the output stage on this A13A1 assembly are the input transistors Q7 and Q8. The output bias current is set by R17 and CR4-CR5 to be approximately 40 mA. This keeps the output stage class A for all normal output conditions.

2-137. OUTPUT STAGE

The output stage circuit is a complementary Darlington emitter follower bootstrapped buffer amplifier. The input transistors are Q7 and Q8 on the A13A1 assembly. These transistors drive the output transistors Q8 and Q14 respectively. Transistors Q10 and Q11 in the positive side and Q16 and Q17 in the negative side are parallel transistors bootstrapped by VR3 and VR4. Current sources CR13, CR14, CR17, CR18, CR15, CR16, CR11, and CR20 provide the bias current for their respective bootstrapped transistors. Current limiting for the positive side is provided by Q9 and R91. During an overcurrent condition, the voltage drop across R91 turns on Q9, which draws current away from the base of Q11. Current limiting is done in the same manner for the negative side with Q15 and R99.

Switch S1 can be switched to pull the input of the A13A1 output stage low for troubleshooting the output stage. Refer to the Oscillator Output troubleshooting section for more information.

2-138. PHASE SHIFTER

The phase shifter circuit provides a fixed amplitude variable phase auxiliary signal at the rear panel of the calibrator. This signal is the same frequency as the output, but can be phase shifted over a 360^{o} range. The four phases (each 90^{o} apart) for the oscillator circuit are divided by Z4 and Z5. These signals are connected to the dual four-channel multiplexer (U27), which is under the control of the PHASE control bus from the digital control circuit. This multiplexer selects any two adjacent oscillator phases (e.g. 0^{o} and 90^{o}) that are connected to the input of a dual monolithic DAC U28. These signals are then scaled by the dac (U28), also under the control of the digital control circuit. The two outputs of this dac are summed by op amp U29. Using this method, the output of U29 is a phase shifted signal between 0 and 360^{o}, where the scaling of the signals controls the phase shift within a 90^{o} range.

2-139. Power Amplifier Assembly (A16)

The Power Amplifier assembly outputs dc voltages from $\pm$22V to $\pm$ 219.99999V and ac voltages from 22V to 219.99999V rms. The frequency limit for 220V ac output is 100 kHz. Output voltage limits are derated at frequencies above 100 kHz. At 1 MHz, the maximum output voltage is 22V rms. The Power Amplifier drives the High Voltage assemblies (A14, A15) in all high voltage and high current functions.

This assembly also contains calibration circuitry that enables the internal calibration system to determine exact Power Amplifier ac and dc gain, offsets and frequency response.

The main sections of this assembly are the input stage, mid stage, output stage, sense-current cancellation circuit, the dc and ac gain calibration circuits, and the Power Amplifier Digital Control SIP assembly (A16A1), which is mounted on the Power Amplifier assembly.

2-140. POWER AMPLIFIER DIGITAL CONTROL SIP ASSEMBLY (A16A1)

Digital control for the Power Amplifier assembly is contained on the SIP assembly (A16A1) mounted at the bottom of the Power Amplifier. This assembly configures the Power Amplifier assembly for its various modes of operation. (Also see "±PA Supplies Digital Control" in the Power Amplifier Supply theory of operation.)

The heart of the Digital Control assembly is an 82C55 Programmable Peripheral Interface IC (U11) operating under software control via the guarded digital bus. This IC has three ports that generate 24 outputs. These outputs control two 5801 relay driver ICs (U10, U12), two LM339 Comparators (U13, U15) and an analog multiplexer (U14) used for diagnostics.

Relay driver U10 generates eight control lines (LC0*-LC7*) that control four latching relays (K1-K4). Relay driver U12 generates eight control lines (C0*-C7*) for non-latching relays K10-K17. C0* also controls FETs Q57 and Q58. Port A (PA0-PA7) from U11 provides an input bus common to relay drivers U10 and U12. Each driver has separate strobe and enable lines from port C of U11. Driver U10 is strobed by PC7 and enabled by PC5. Driver U12 is strobed by PC4 and enabled by PC6. When a STROBE line is selected, data on the bus (PA0-PA7) is strobed into the respective driver chip. When an ENABLE is selected, this strobed data appears at the output, thereby energizing the appropriate relays. Latching relays only need to be energized for 10 ms; non-latching relays need to be energized continuously.

As an example, the following steps are taken to set up latching relays controlled by relay driver U10.

1. Write the proper data for these relays to port A of the 82C55 (U11).

2. Write hex A to PC4-PC7 to strobe the data into U10.

3. Write hex 0 to PC4-PC7, wait 10 ms and write hex 2 to PC4-PC7. This takes U10's output out of tri-state and energizes the proper relay coils for 10 ms. Since PC4 and PC6 are always low, U12 is undisturbed.

Two LM339 quad comparators (U13 and U15) get their data from port B of U11 (PB0-PB7) and generate control lines SW0-SW7. SW0-SW2 are inputs to decoder U9, which generates eight additional control lines (CONT0*-CONT7*) for controlling FETs and solid state switches. Control line SW3 controls FETs Q50 and Q51. Control lines SW4-SW7 are routed through the Motherboard to the Filter/Power Amplifier Supply assembly (A18) to control the +PA and -PA supplies.

The diagnostic circuit enables the 5700A to monitor eight diagnostic (MUX) signals on the Power Amplifier assembly. A 4051 analog multiplexer (U14) is controlled by PC0-PC3 from U11. This multiplexer selects of the eight MUX signals to the SDL line, where it is measured by the adc circuit on the DAC assembly (A11). Resistor network Z2 and various resistors and zener diodes on the Power Amplifier assembly divide these MUX signals down to a proper level for measurement by the adc circuit. The eight monitored points are:

- o MUX0 Output of U7; indicates the status of the amplifier loop
- o MUX1 +PA Supply
- o MUX2 -PA Supply
- o MUX3 Power Amplifier output
- o MUX4 Indicates the temperature of the Power Amplifier assembly
- o MUX5 Power Amplifier dc input
- o MUX7 Diagnoses the state of the hybrid heater-control circuit

2-141. PA COMMON CIRCUITRY

Common circuitry consists of the +PA and -PA supplies, input stage, mid stage, and the output stage. These four circuits are described under the next four headings.

Power Amplifier input node, gain, and feedback are different for dc and ac operation. Power Amplifier gain is -20 in the dc function, determined by the ratio of resistor network bonded to the HR8 assembly (500 kilohm/25 kilohm). Gain in the ac function is -10, which is determined by the ratio resistors [(R11 + R12 + R13)/R17]. This is described in more detail under "DC Voltage Function" and "AC Voltage Function".

2-142. +PA AND -PA SUPPLIES

The ±PA supplies are high voltage supplies generated by the Filter/PA Supply assembly (A18). These supplies can be controlled by the Digital Control SIP assembly (A16A1) and are switched between the two modes shown in Table 2-13.

- o ±185V
- o ±365V

Theory of operation for the Filter/PA Supply assembly (A18) describes how these voltages are generated and selected.

Table 2-13. +PA and -PA Supply Settings at Different Outputs

CALIBRATOR OUTPUT	+PA	-PA
Less than 22V ac or dc	+185V	-185V
22 to 110V dc	+185V	-185V
110 to 220V dc	+365V	-185V
-220 to -110V dc	+185V	-365V
22 to 101V ac (freq < 120 kHz)	+185V	-185V
22 to 85V ac (freq > 120 kHz)	+185V	-185V
Other voltages	+365V	-365V
220 to 550V dc or ac	+185V	-185V
550 to 1100V dc or ac	+365V	-365V
220 mA to 2.2A	+365V	-365V

2-143. PA INPUT STAGE

The input stage consists of a heater-controlled hybrid HR8, op amp U7, transistor Q6, and JFET Q2. The HR8 assembly consists of an op amp mounted on a heated-substrate hybrid, with a resistor network bonded to it. Hybrid HR8 provides the input stage with excellent dc characteristics of low offset, noise and drift. The hybrid heater-control circuit (on page 3 of the schematic) adjusts the base voltage of Q38 to deliver the correct current to the heater resistor. This maintains the hybrid assembly at a constant temperature in spite of environmental temperature variations. Transistor Q35 protects the hybrid in case Q38 fails. Input of the hybrid op amp is protected by CR13 and CR14. Output of the hybrid op amp is connected to the input of a faster op amp (U7), which provides additional dc gain and a higher slew rate. JFET Q2 and transistor Q6 combined with these two op amps complete the input stage. Q2 is a very low-bias-current, high-frequency JFET.

In mid to high-frequency operation, Q2 is effectively the only path for the input stage signal. HR8 and the U7 op amps are bypassed at these frequencies by R89, C42, R24, and C12. As a result, the base of Q6 is at ac ground. In dc to mid-frequency operation, the gate of Q2 is at ground potential. At any frequency, the potential difference between the gate of Q2 and the base of Q6 results in a current through Q6 as determined by the network consisting of R22, R145, and L11 and by the transconductance of Q2 and Q6. The input stage is called a transconductance stage because an input voltage results in a current output at the collector of Q6.

This current output is coupled to the mid stage (Q12, Q14, and Q16) by Q8, Q9, Q13 and C15, where it results in a voltage across the base-emitter of Q16 (the input of the mid stage). Current source Q9 determines bias current in Q2 and Q6. Variations of Q6 output current become voltage variations at the base of Q16. This transfer is through Q8 and Q13 at dc and low frequencies, and through C15 at high frequencies.

The input stage operates with low voltage supplies (±17V) whereas Q16 of the mid stage is connected to the -PA supply, which can be as high as -365V. This potential difference is dropped across level shifter Q13.

2-144. PA MID STAGE

The mid stage (Q12, Q14, and Q16), biased by the 8 mA current source (CR53, Q31, Q32 and R87 on page 2 of the schematic), is a voltage amplifier providing additional gain. The base of transistor Q16 is the input to the mid stage. MOSFETs Q12 and Q14 are biased by R41 and R53 respectively. Components CR21, CR23, and VR22 protect Q12 from excessive source-to-gate voltage, and R112 prevents Q12 from oscillating. Components CR25, CR29, VR28, and R113 perform the same function for Q14. A signal at the base of Q16 appears amplified at the drain of Q12. Total impedance from the drain of Q12 to ground, divided by R58, determines gain at dc and low frequencies. At high frequencies, the effective drain to ground impedance is R53. Relay K12A parallels C18 and C57 during dc operation for a lower bandwidth. Capacitors C18 and C57 provide the Miller capacitance for the amplifier.

Transconductance gain of the input stage and the Miller capacitance determine Power Amplifier frequency response at high frequencies. All the voltage gain of the Power Amplifier comes from the input and mid stages.

2-145. PA OUTPUT STAGE

The Output Stage is an emitter follower that provides current gain but no voltage gain. It is needed because the mid stage cannot drive the rated load by itself.

Voltage across R74 and R35 determines the bias current through the output stage. This voltage equals the voltage across Q7, minus the value (4 x Vbe) (for each transistor Q4, Q5, Q10, and Q11). Transistor Q7 is configured as a Vbe multiplier, the voltage across which (and thus the output stage bias current) is the value (1 + (R23+R26)/R32). The output bias current is 50 mA.

NMOSFETs Q1, Q3, and transistor Q5 source current, while PMOSFETs Q15, Q17, and transistor Q10 sink current from the load. This output stage can drive up to 50 mA of load current as determined by the current limit circuit on ±PA supplies on the Filter/PA Supply assembly (A18).

Zener diodes VR15 and VR18 bootstrap NMOSFETs Q3 and Q15 respectively, and provide the power supplies SC+ and SC- to op amp U1 in the sense current cancellation circuit. Two stacked NMOSFETs (Q1, Q3) on the top end (+PA side), and two stacked PMOSFETs (Q15, Q17) on the bottom end (-PA side) withstand the high voltage drops between ±PA supplies and output. NMOSFETs Q1 and Q3 are biased by R15 and R19 respectively. PMOSFETs Q15 and Q17 are biased by R52 and R57 respectively. Components CR5, CR7 and VR6 protect Q1 from excessive source-to-gate voltage and R108 prevents Q1 from oscillating. Protection is also provided for remaining MOSFETs in the output stage. Output of this stage, called PA OUT HI, is the output of the Power Amplifier assembly. Components R120 and L10 isolate capacitive loads.

2-146. PA SENSE CURRENT CANCELLATION CIRCUITRY

During dc operation of the Power Amplifier, sense current in the 500 kilohm feedback resistor (on the resistor network in the HR8 assembly) can cause an output error because of the finite resistance path of the connection to the load. Op amp U1 eliminates this error by feeding an equal and opposite current in this path. The magnitude of this current is determined by PA OUT HI, which is connected to the non-inverting input of U1. This circuit generates a current through R8, which is equal to current flowing through the 500 kilohm feedback resistor. Sense-current cancellation is active only in dc 220V range.

2-147. PA IN STANDBY

The Power Amplifier schematic shows all relays and DG211 FET switches in the standby condition. The Power Amplifier 25 kilohm input resistor and R17 are tied to OS COM through Q39 and R118. Power Amplifier output is close to zero and the whole loop is stabilized.

To better understand Power Amplifier configuration in the ac/dc 220V range, refer to Figure 2-21.

2-148. PA OPERATION: 220V DC RANGE

During dc operation, Power Amplifier gain is -20, as determined by the 500 kilohm/25 kilohm resistor network on the HR8 assembly. Control line SW3, inverted by U8, turns on Q51. This references the +input of the precision op amp in the input stage to R COM. The DAC assembly is set to the negative 11V range and its outputs, DAC OUT HI and DAC SENSE HI, are connected to pin 2 of the resistor network on the HR8 assembly by relay K2. The sense current cancellation circuit is active during dc operation. Its output, SIG1, is connected to the resistor network feedback resistor pin 1 by relay K15A. The amplifier has a much lower bandwidth in this mode because of the much higher Miller capacitance in C57. Lower bandwidth results in lower amplifier noise.

The output signal, PA OUT HI, is routed to the High Voltage Control assembly (A14), where it goes through relay K10 and becomes PA OUT DC. PA OUT DC is routed to the Switch Matrix for connection to the OUTPUT HI binding post. The sense signal, PA SENSE DC from the Sense Current Cancellation circuit, is routed to the Switch Matrix assembly (A8) for connection to the OUT/SENSE HI or SENSE HI binding posts, thus making the binding post the sense point in internal sense and allowing for external sense through the SENSE HI binding post.

2-149. PA OPERATION: 220V AC RANGE

During ac operation, Power Amplifier gain is -10 as determined by the 4.99 kilohm input resistor R17, and 49.9 kilohm feedback resistors (R11 + R12 + R13). Control line SW3 turns Q50 on, which references the +input of the precision op amp in the input stage to OS COM. The Oscillator assembly (A13) is set to the 22V range and its output OSC OUT HI is connected to the input resistor R17 by relay K10A. The Power Amplifier output is connected to the feedback resistors R11-R13 by relay K12B.

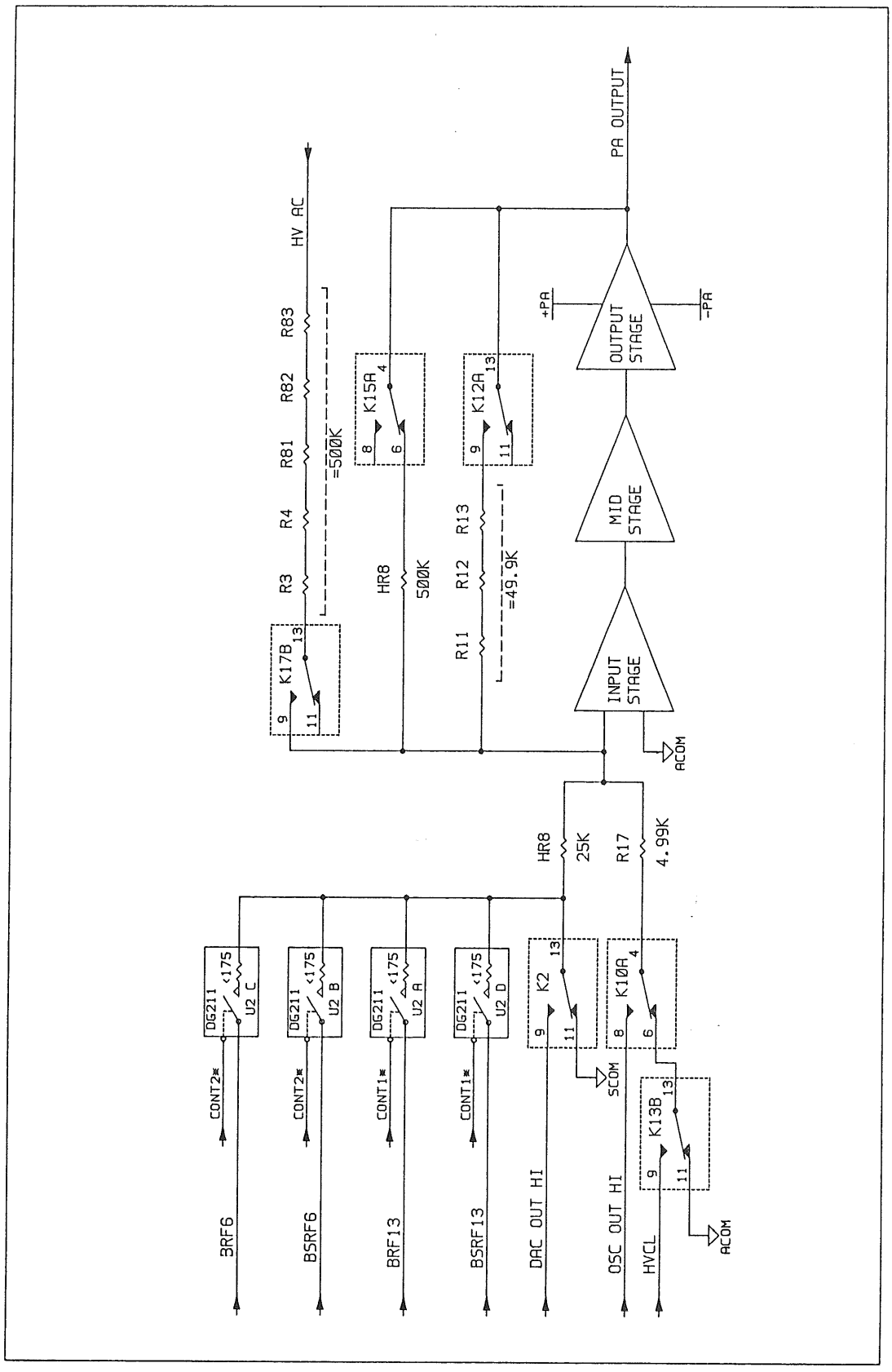

Figure 2-21. Power Amplifier Simplified Schematic

The Power Amplifier output is attenuated by a precise 1/100 by 220V range ac attenuator. The attenuated signal is connected to OSC SENSE HI, where it is sent to the Oscillator Control assembly (A12). The Oscillator Control assembly regulates the Oscillator Output so that an exact calibrated ac signal appears at OSC SENSE HI. Since the 220V range ac attenuator is completely characterized (as explained below), the exact desired signal appears at PA SENSE AC and hence at the appropriate sense point at the output.

The 220V range ac attenuator circuit contains op amp U4, a 400 kilohm/4 kilohm resistor network Z1, and transistor Q54. PA SENSE AC, which is connected to PA OUT HI at the load, is connected to the 400K input resistor (pin 1) of Z1 by relay K16. The 400 kilohm/4 kilohm node (pin 3) of Z1 is connected to the inverting input of U4.

During ac operation, control line CO* is inverted by U8, which turns on Q58 to connect the non-inverting input to OSC RCOM. Transistor Q54 supplies current gain for the output of U4 to drive the capacitance of the OSC SENSE HI line. This voltage is connected to the 4 kilohm feedback resistor (pin 4) of Z1. The output is connected to OSC SENSE HI by relays K10B and K11. The dc feedback 500 kilohm/25 kilohm resistor network and the sense-current cancellation circuitry are disconnected by energizing K15.

The sense signal, PA SENSE AC, and the output signal, PA OUT HI, are routed to the High Voltage Control assembly (A14), where relays K10, K13, and K3 connect them to HV SNS and HV OUT. HV SNS and HV OUT are connected to the binding posts by the Motherboard relays in the same manner as in the 1100V high voltage mode. Refer to the High Voltage assembly theory of operation for more information.

2-150. HIGH VOLTAGE ASSEMBLY SUPPORT MODE

2-151. High Voltage AC 1100V Range

During high voltage ac operation, the output of the Power Amplifier is routed to the input of a step up/down transformer on the High Voltage Control assembly (A14). Overall gain from the Oscillator Output to the High Voltage Output is -100 as determined by the 4.99 kilohm input resistor R17, and 500 kilohm feedback resistor (R3 + R4 + R81 + R82 + R83). Relay K10A connects the ac signal OSC OUT HI from the Oscillator Output assembly to input resistor R17. Relay K12 remains open as shown on the schematic, while K15 is energized to remove feedback used in 220V-dc operation.

Output from the High Voltage Control assembly, called HVAC on the schematic, is connected to the feedback resistors. Relay K17B is energized to close the feedback loop. Relay K13A is energized to enable U3 and its associated circuitry to provide dc feedback around the Power Amplifier. This maintains the dc level at the High Voltage-transformer input at zero. Control line SW3 is high, which turns Q50 on and turns Q51 off. Because sensing back to the Oscillator Control assembly is done by the High Voltage/High Current assembly, the output of the 220V range ac attenuator is disabled from OSC SENSE HI by relay K11.

Because sensing to the Oscillator Control assembly is done by the High Voltage assembly, the output of the 220V range ac attenuator is disabled from OSC SENSE HI by relays K10B and K11.

2-152. High Voltage DC 1100V Range and Current 2.2A Range

Operation of the Power Amplifier is the same for the 1100V dc and the 2.2A current functions. In these functions, the output of the Power Amplifier is routed to a step up/down transformer on the High Voltage Control assembly (A14). The Power Amplifier is configured the same as for 220V ac operation, except that the input is the square-wave signal HVCL from the High Voltage Control assembly, rather than OSC OUT HI, through relays K13B and K10A.

2-153. 220V DC INTERNAL CALIBRATION NETWORK

The 220V dc internal calibration network is used to determine the exact gains and offsets of the power amplifier. This circuit uses part of the resistor network HR8 as the input attenuator, and uses op amp U9, and zener diodes VR57 and VR58. Relay K4 connects the output of this circuit to the RCL line.

Zener diodes VR57 and VR58 reduce the power supplies for chopper-stabilized amplifier U9, which is used as a voltage follower.

2-154. PA CALIBRATION

The following paragraphs explain internal calibration taken by the Power Amplifier assembly. These steps include calibrating the offset, gain, and frequency characteristics of the Power Amplifier.

The first step is to measure the offset of the Main Amplifier (220V range). The DAC output is amplified by the Power Amplifier, which is configured for the dc 220V range, and its output connected to the internal cal zero amplifier located on the Switch Matrix assembly. Output of this internal cal zero amplifier is channeled to the DAC's adc amplifier circuit by the RCL line. Input of the internal cal zero amplifier is first connected to R COM where a checkpoint reading is taken by the DAC's adc circuit. The output of the Power Amplifier is then connected to the input of the internal cal zero amplifier and the DAC output is adjusted to the checkpoint reading out of the zero amplifier. This adjusted DAC output is a measure of the offset of the Power Amplifier. Also, refer to the Switch Matrix theory of operation.

The 175 kilohm/25 kilohm (internal cal) resistor network located on HR8 is calibrated next. This is illustrated in Figure 2-22. Offset of the 220V dc internal cal amplifier U9 is measured first. This is done by connecting pin 6 of 175 kilohm/25 kilohm resistor network to RCOM by relay K1, and pin 7 to ACOM by U5C and relay K3. ACOM is connected to RCOM through 051 during this step. Output of this internal cal amplifier is connected to the RCL line by relay K4, where it is measured by the adc circuit on the DAC assembly. As before, the DAC's output needed to obtain the checkpoint for this step represents the offset of the internal calibration amplifier.

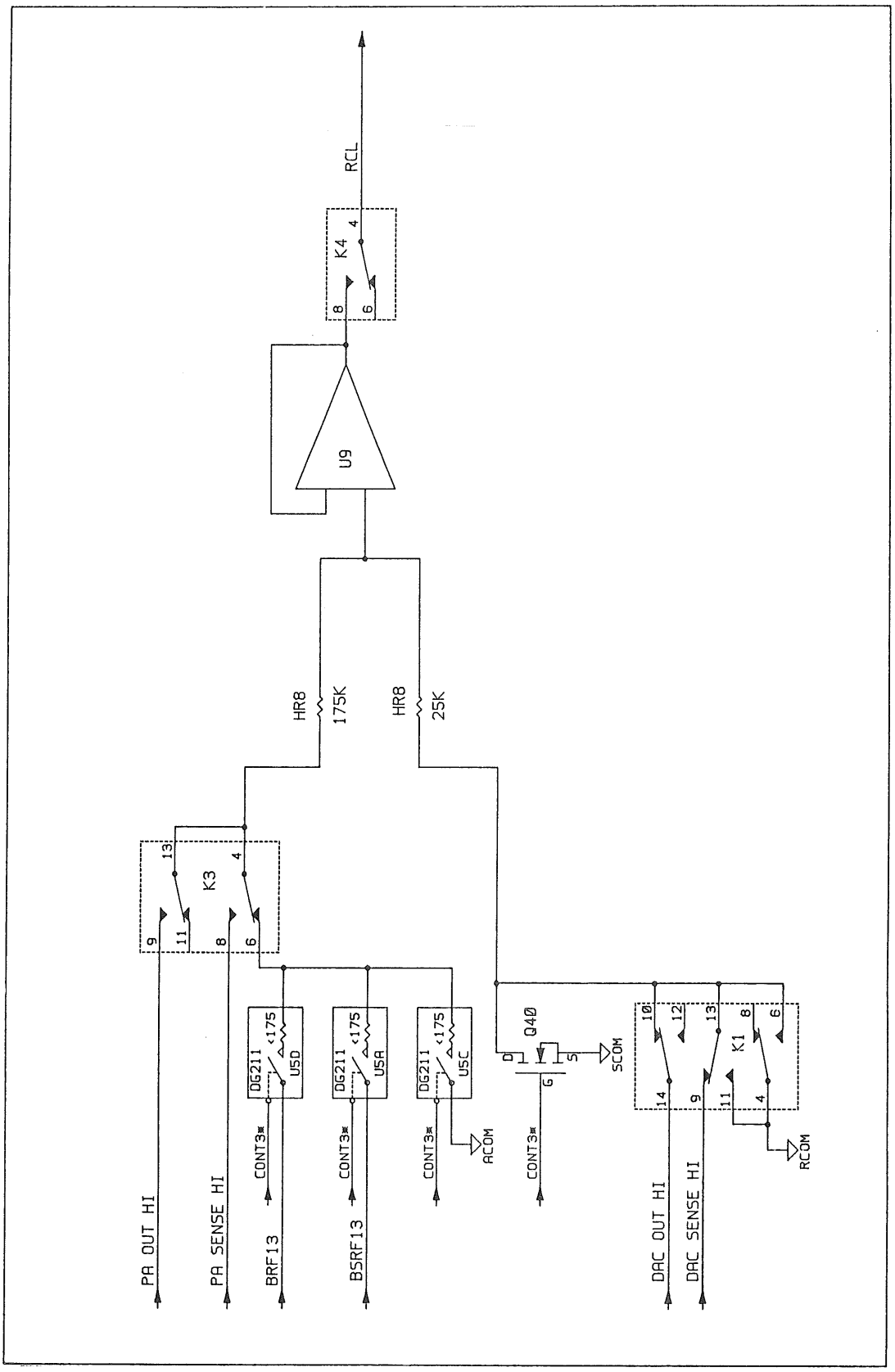

Figure 2-22. Power Amplifier DC Calibration Network

Resistor network attenuation is calibrated next. Components U5A, U5D and K3 connect BSRF13 and BRF13 to the 175 kilohm end, while K1 connects R COM to the 25 kilohm end of the resistor network. The resulting 1.625V at the output is connected to the RCL line by relay K4, where it is connected to the +input of the adc amplifier circuit on the DAC assembly. The DAC output is connected to the adc circuit -input, and adjusted until the checkpoint reading is obtained. The exact value of this voltage is now known, so the system software computes the exact attenuator ratio from this known voltage, BSRF13 value, and the previous offset measurement.

Power Amplifier dc gain of approximately -20 is calibrated next. The Power Amplifier is configured as in the 220V dc operation, except the input is connected to the DAC's 6.5V reference BRF6 and BSRF6 by U2C and U2D respectively. The resulting -130V at the Power Amplifier output is connected to the 175 kilohm end of the internal cal resistor network by relay K3. The 25 kilohm end of this network is connected to DAC OUT HI and DAC SENSE HI by relay K1. The output of the internal cal amplifier is connected to the DAC's adc circuit as in the previous steps, and the DAC OUTPUT is adjusted until checkpoint is measured by the adc circuit. Since the exact attenuation of the resistor networks is already known, the exact Power Amplifier output voltage can be calculated. This in turn gives the exact Power Amplifier dc gain, since the exact value of 6.5V reference BSRF6 is known.

Attenuation of the 220V range ac attenuator (U4 and 396 kilohm/4 kilohm resistor network Z1) is calibrated next. This is illustrated in Figure 2-23. First, the offset of the attenuator circuit is measured by connecting the non-inverting input of U4 to ACOM through Q57 and thus to RCOM through Q51. Then, the Power Amplifier is configured for the 220V dc range with its inputs connected to the DAC's 6.5V reference BRF6 and BSRF6 by U2B and U2C respectively. The resulting -130V is connected to the 400 kilohm input resistor (Z1) of the 220V range ac attenuator by relay K16. RCOM (ACOM) is connected to the non-inverting input of U4 by Q58.

The +1.3V from the output of the attenuator circuit is connected to the RCL line by relays K10B and K11. This voltage on the RCL line is connected to the +input of the adc amplifier circuit on the DAC assembly. The DAC output is connected to the -input of the adc amplifier circuit, and is adjusted until a null is achieved. The exact value of this voltage is now known so the system software can compute the exact attenuator ratio.

The 220V range ac attenuator's attenuation ratio can vary over the frequency range. This variation can be accounted for if the frequency response of this network is characterized at a few spot frequencies. This is done by connecting the Power Amplifier output, which is set to 22V, to the AC CAL line by relay K14. The AC CAL line goes into the AC/AC CAL thermal sensor located on the Oscillator Control assembly. The Power Amplifier output of 22V is also attenuated through the AC Attenuator and sensed by the Oscillator Control via OSC SENSE HI. The Oscillator adjusts its output, and hence the Power Amplifier output,

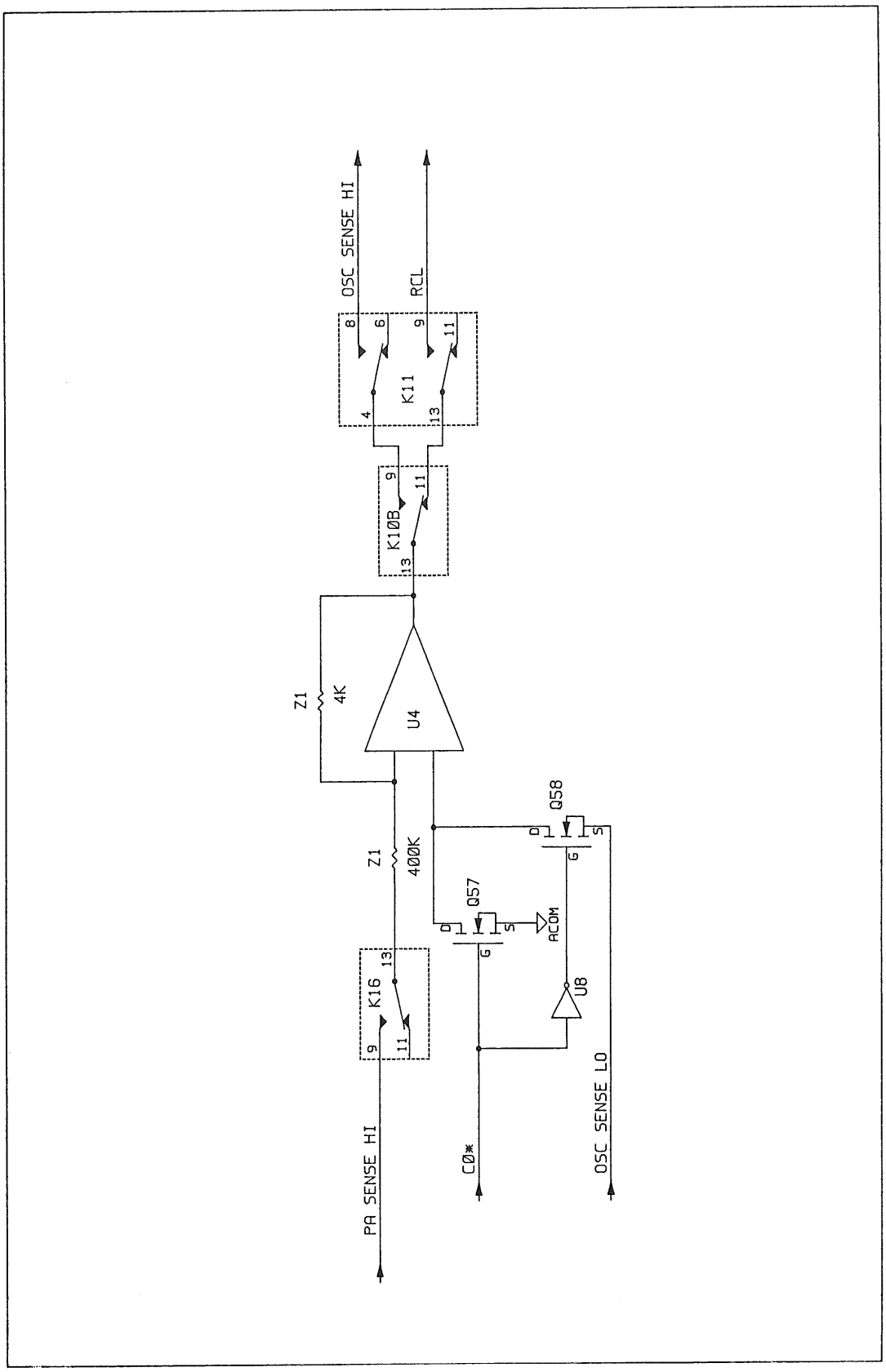

Figure 2-23. Power Amplifier Calibration AC Attenuator

until the ac/ac cal thermal sensor measures the same ac level for all these spot frequencies. The signal levels at OSC SENSE HI are stored in software at all such points.

The ac/ac cal thermal sensor located on the Oscillator Control assembly has a flat frequency response. The change in the ac attenuator's output at various frequencies for a constant thermal sensor output defines the frequency response of the Power Amplifier ac attenuator. These computed ac attenuator factors are stored in the system memory and are taken into account when the calibrator is configured to output ac voltages from the Power Amplifier.

Output stage current is limited to about 250 mA; Q60 limits the current sourced by the output stage, and Q61 limits the current sinked by the output stage. Transistor Q62 limits the current flowing through the middle stage. These current limits both protect the power amplifier circuitry and improve power amplifier transient response. Diode CR64 is a current source that maintains a current flow of at least 5 mA through the output devices at all times.

2-155. High Voltage Assemblies (A14 and A15)

The High Voltage/High Current assembly (A15) and the High Voltage Control assembly (A14) are used in with conjunction with other assemblies in the calibrator to generate the ±1100V dc, 1100V ac, and the 2.2A ranges. The two assemblies work together in generating these ranges. This theory of operation explains how these ranges are generated and discusses the individual circuits on each assembly. Refer to the High Voltage/High Current assembly simplified schematics (Figures 2-24 through 2-28) or the schematic diagram to understand this theory of operation better.

2-156. 1100V AC RANGE

Refer to Figure 2-24 for the following discussion. The ac signal generated by the Oscillator Output assembly (A13) is amplified by the Power Amplifier assembly (A16). The output of the Power Amplifier, PA OUT DC, is routed to the High Voltage Control assembly (A14), where it is further amplified by transformer T1 to generate the 1100V ac range. This high voltage signal from T1 is also the feedback signal to the Power Amplifier assembly. Relays K14-K16 connect the transformer windings in series during operation below 120 Hz.

Line PA OUT DC is connected to one side of the primary winding of step-up transformer T1 by relay K1 on the High Voltage Control assembly (A14). The other side of the primary winding is tied to PA COM through R67. One side of the secondary winding is tied to PA COM by relays K9 and K6. The other side of the secondary winding, the high voltage ac signal, is connected to HV OUT by relays K5, K12 and K3. Line HV OUT is connected to the OUTPUT HI binding post by relays K9 and K1 on the Motherboard.

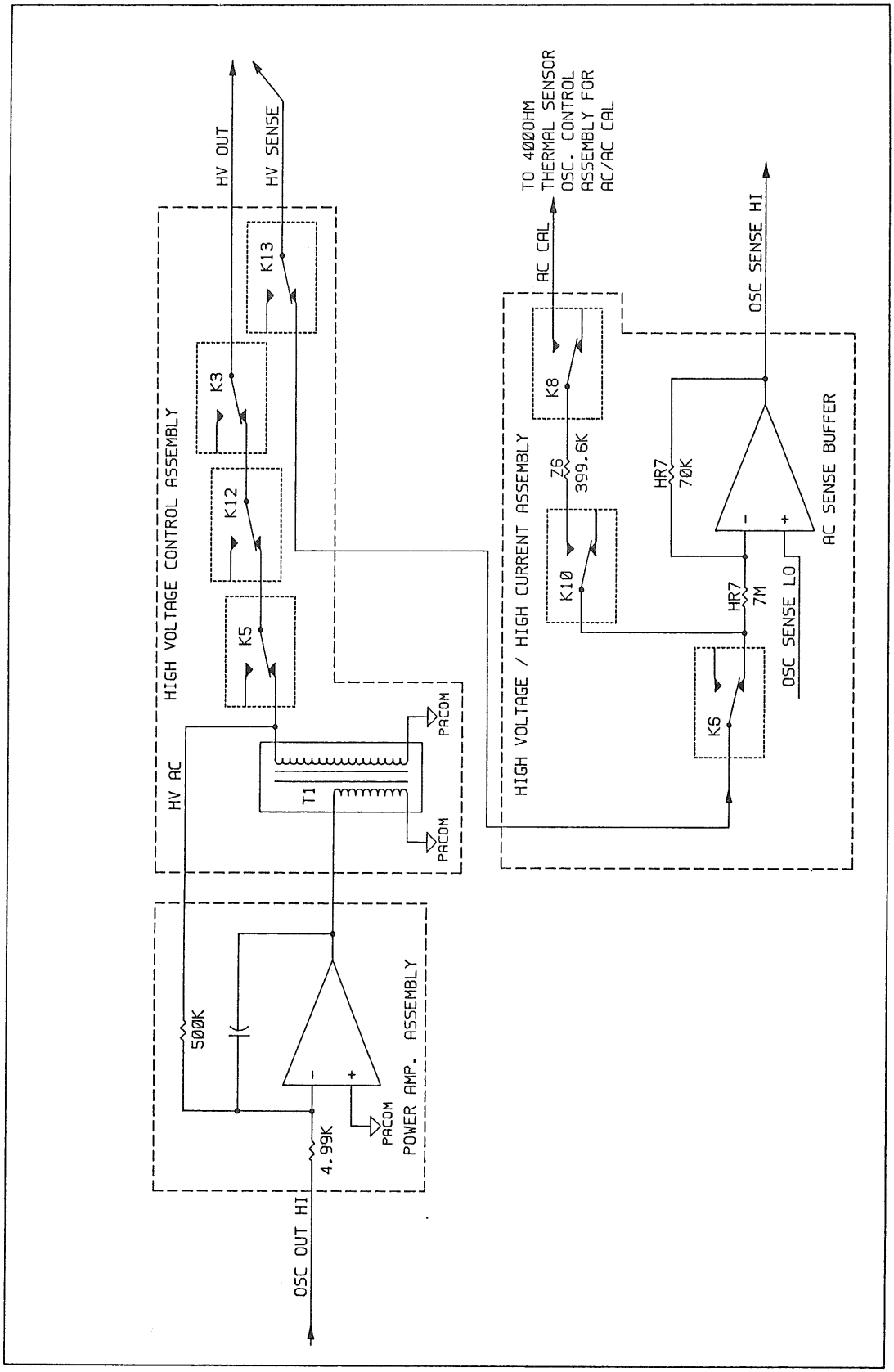

Figure 2-24. High Voltage/High Current Assembly 1100V AC Range

This high voltage ac signal is also connected to HVAC by relay K5. Line HVAC is the feedback signal to the Power Amplifier assembly. During high voltage operation, the input resistor of the Power Amplifier assembly is 5 kilohms. Line HVAC is connected to the feedback resistance, which is a series of resistors totaling 500 kilohm. This creates a gain of 100 to the Oscillator Output.

The SENSE HI binding post is connected to HV SENSE by relays K3, K2, and K10 on the Motherboard. HV SENSE, which is tied to HV OUT at the load, is connected to INT HV SNS by relay K13 on the High Voltage Control assembly (A14). INT HV SNS is routed to the High Voltage/High Current assembly (A15), where it is connected to the ac sense buffer circuit by relay K6. This circuit attenuates the high voltage signal by 100 and connects it to OSC SENSE HI through relay K4B. The level of attenuation is determined by the 7 megohm input and 70 kilohm feedback resistors on the HR7 assembly. OSC SENSE HI is used by the Oscillator Output assembly, which adjusts its output signal to maintain an exact feedback signal level. HV OUT and HV SENSE are routed to the High Voltage assembly (A15) where components CR9, CR10, and R33-R35 keep the voltage difference between them at 0.7V should they become disconnected at the load. Relay K11 connects HV OUT to HV SENSE during calibration in the ac function.

2-157. 1100V DC RANGE

Refer to Figure 2-25 for the following discussion. The High Voltage assembly (A15) amplifies the output of the DAC assembly (A11), set to the 11V range, by a gain of -100 to generate the 1100V dc range.

For operation in the 1100V dc range, DAC OUT HI and DAC SENSE HI from the DAC assembly, set to the 11V range, are tied together and connected to the input of the dc HV amplifier circuit by relay K1. The dc HV amplifier circuit, the HV dc output series pass and current limit circuit, and the HV dc power supply circuit on the High Voltage Control assembly (A14) constitute an overall amplifier with an inverting gain of 100. This gain is determined by the 70 kilohm input and 7 megohm feedback resistors on the HR7 assembly.

High voltage dc output, generated on the High Voltage Control assembly (A14), is obtained by filtering an approximate trapezoidal wave. The overall loop gain of this amplifier divides this ripple so the high voltage dc output is clean and stable.

Signal routing to the front panel binding posts is done in the same manner as the ac 1100V range.

2-158. HVDC POWER SUPPLY FILTER CIRCUIT

The high voltage dc power supplies are generated by the High Voltage Control assembly (A14) in conjunction with the Power Amplifier assembly (A16). The High Voltage Control assembly generates an amplitude-controlled square wave, SQ OUT, from the magnitude control circuitry. The magnitude control circuit contains all the circuitry on page 2 of the High Voltage Control assembly schematic.

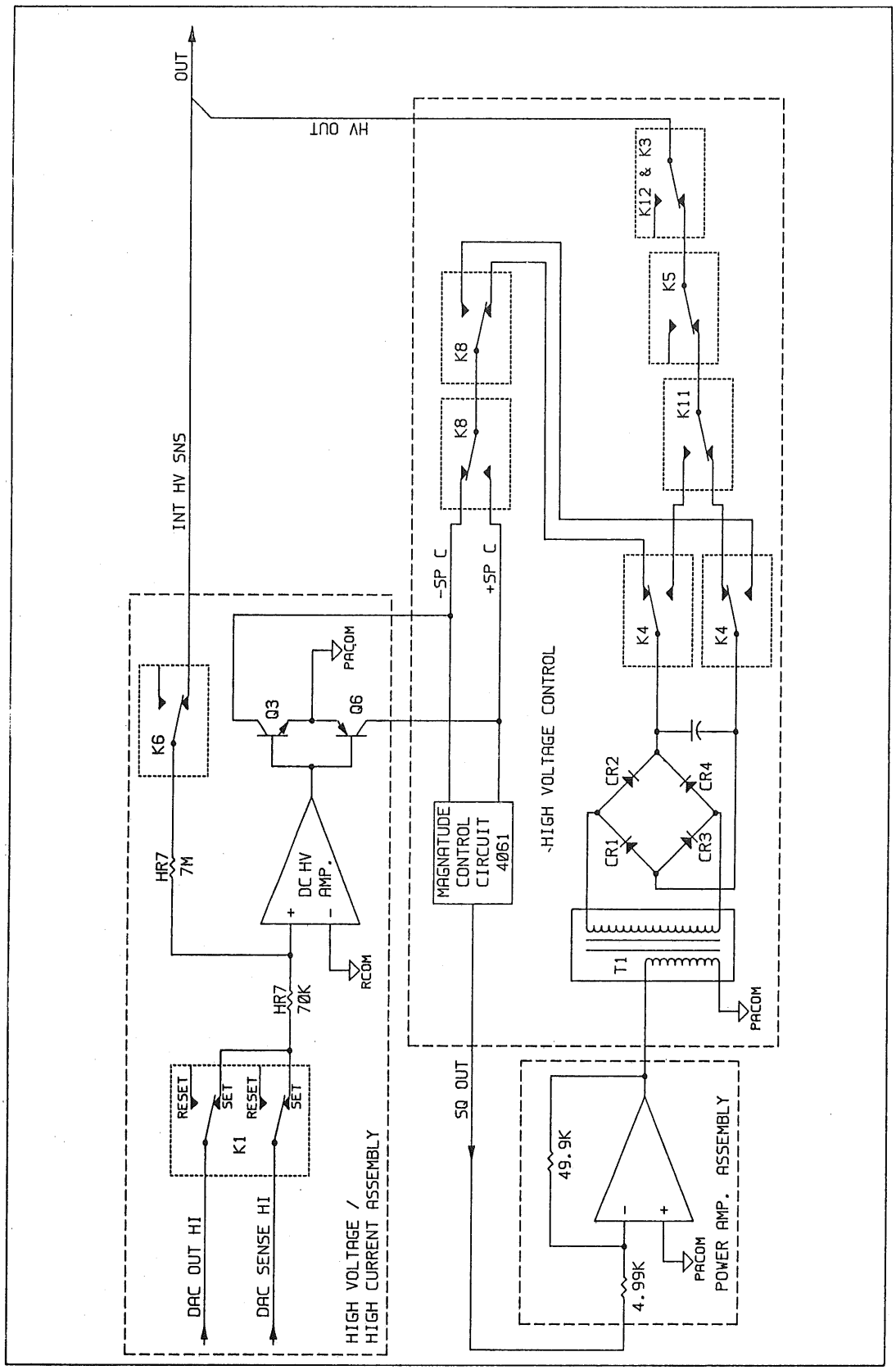

Figure 2-25. High Voltage/High Current Assembly 1100V DC Range

Signal SQ OUT is amplified by the Power Amplifier assembly with its output, PA OUT DC, connected to one side of the primary winding of transformer T1 by relay K1. The other side of the primary is connected to PA COM by R67. The secondary windings of T1 are connected to a bridge rectifier, CR1-CR4, by relays K9 and K6. The dc voltage from this rectifier is called +HVDC and -HVDC. Resistors R3-R5 form a 600 kilohm bleeder resistor for C1. Line HVDC is selected between +HVDC and -HVDC by relays K4 and K11. Line HVDC is connected to HV OUT by relays K5, K12 and K3.

During operation with a negative DAC voltage and a positive output from the High Voltage/High Current assembly, +HVDC is connected to HV OUT by relays K4, K11, K5, K12 and K3. +SP C is created from -HVDC by relays K4 and K8. During operation with a positive DAC voltage and a negative output from the High Voltage/High Current assembly, -HVDC is connected to HV OUT by relays K4, K11, K5, K12 and K3. -SP C is created from +HVDC by relays K4 and K8. Zener diodes VR4 and VR5 keep -SP C and +SP C, respectively, from exceeding 16V. The dc voltage level of +SP C and -SP C is controlled by the HV dc output series pass and current limit circuit on the High Voltage/High Current assembly. This in turn controls the magnitude of SQ OUT which sets the level of HVDC.

2-159. HV DC OUTPUT SERIES PASS AND CURRENT LIMIT CIRCUIT

The HV dc output series pass circuit controls the level of +SP C when the high voltage output is positive, and -SP C when the high voltage output is negative. Typically +SP C and -SP C are approximately $\pm$6.8V dc with ripple equal and opposite polarity from the HVDC ripple.

When the DAC assembly is set to the +11V range, the output from the High Voltage assembly (with a gain of -100) is in the -1100V range. In this mode, -SP C is connected to the collector of transistor Q3. The output from the dc HV amplifier follows a change in the output voltage from the DAC assembly. This change controls how much Q3 is turned on or off. As the DAC voltage is increased, Q3 turns on pulling -SP C to PACOM. This causes the magnitude control circuit to increase the amplitude of SQ OUT which increases the output from the Power Amplifier assembly, thus increasing the HVDC until the overall loop is stable.

Operation in the +1100V range is basically the same, with transistor Q6 controlling +SP C in the same manner as above.

Current limiting is provided by Q4 if more than 35 mA is drawn from the output. If this condition occurs, Q4 pulls down CUR LIM, which is routed to the High Voltage Control assembly. (CUR LIM is also called RST.) When CUR LIM (RST) is pulled low, PS OFF goes high to turn off the square wave, SQ OUT, which shuts down the HVDC supplies. The generation of SQ OUT is described under the heading, "Magnitude Control".

2-160. DC HV AMPLIFIER/AC SENSE BUFFER

The dc HV amplifier and the ac sense buffer are basically the same circuit. The configuration is changed to provide the 100:1 amplification of dc voltage and the 100:1 attenuation of the high voltage ac signal. This is defined by the way the HR7 resistor network is configured in the circuit. This configuration is described in the 1100V ac range and 1100V dc range theory.

This circuit contains the HR7 resistor network and the circuitry contained in detail 1 as shown on page 1 of the High Voltage (A15) schematic. It is used in both the ac and dc voltage modes. Detail 1 contains the HR7 hybrid assembly which is an op amp mounted on a heated substrate hybrid bonded to a resistor network. The HR7 assembly gives this circuit excellent dc characteristics of low offset, noise and drift. The hybrid heater control circuit adjusts the base voltage of Q8 to deliver the proper power to the heater resistor. This maintains the HR7 assembly at a constant temperature in spite of environmental temperature variations. Transistor Q9 protects the hybrid in case Q8 fails. The output of the HR7 op amp is connected to a faster op amp (U2), which provides additional gain and a high slew rate. The output of U2 is called HVAMP OUT on the schematic.

In the dc voltage function, the output of this circuit, configured as a dc HV amplifier, is connected to the series pass circuit by relay K5B. Relays K5A, K7 and K14 add C4 in parallel with the 7 megohm feedback resistor in the HR7 assembly to filter the noise. ACOM is connected to RCOM by relay K3.

During operation in the ac voltage function relays are positioned as shown on the schematic. Components VR7 and VR8 provide input protection for the op amp on the HR7 assembly. Op amp U1 is added to the circuit by relays K9, K8B and K6. This op amp inverts HVAMP OUT so that the signal to OSC SENSE HI is in phase with the output of the Oscillator assembly. ACOM is connected to OSC RCOM by relays K3 and K4A.

2-161. 2.2A RANGE

Refer to Figure 2-26 for the following discussion. Most of the same circuitry is used to create the ac and dc 2.2A current ranges. The Current assembly (A7) is configured to the 22 mA range and connected to the IHV line which drives the 2.2A amplifier circuit on the High Voltage assembly (A15). This 2.2A amplifier provides a gain of 100 to the 22 mA range from the Current assembly to create the 2.2A range.

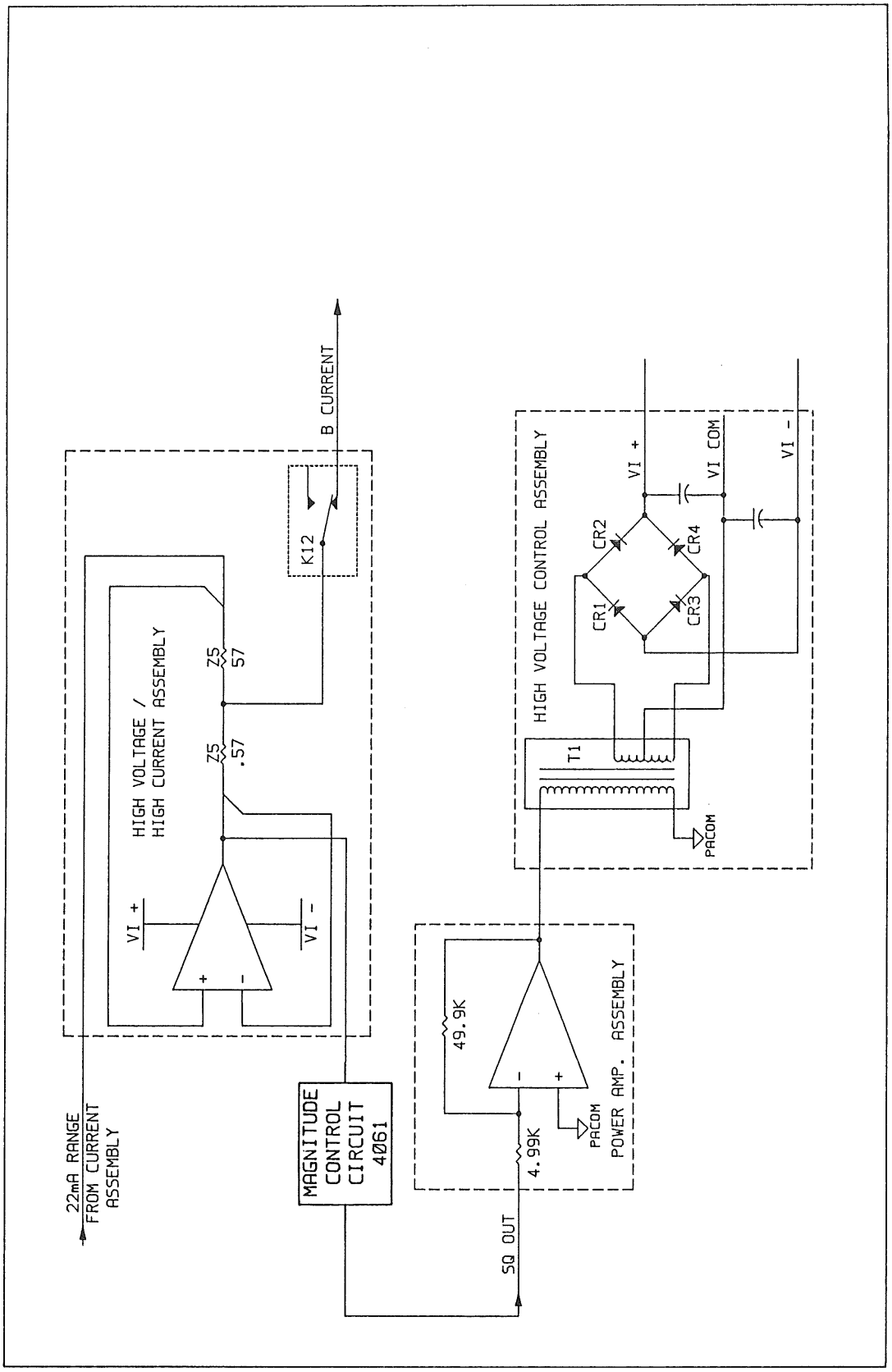

Figure 2-26. High Voltage/High Current Assembly 2.2A AC and DC Ranges

Resistor network Z5 and hybrid H4 determine the performance of the 2.2A range. Current from the A7 assembly develops a voltage across the 57 ohm portion of Z5. The 2.2A current amplifier circuit forces the same voltage across the 0.57 ohm portion of Z5. Because the ratio of these resistors is 100, the current through 0.57 ohm resistor is 100 times that coming from the Current assembly (A7). Relay K12 connects this 2.2A range current to B CUR where it is routed to the Current assembly (A7), which provides the proper relay switching to the front panel binding posts.

The 2.2A amplifier circuit contains the heater-controlled hybrid H4, op amps U3-U5, and transistors Q11-Q16. This circuitry is outlined as detail 2 on page 2 of the High Voltage/High Current assembly schematic. The H4 hybrid consists of an op amp mounted on a heated substrate. The heater control circuit adjusts the base voltage of Q18 to deliver the proper power to the heater resistor. This maintains the hybrid at a constant temperature in spite of environmental temperature variations. Transistor Q19 protects the hybrid in case Q18 fails.

The output of the H4 hybrid is a voltage directly proportional to the current output G OUT. Q22 and R72-R76 form a high-frequency path for loop stability. In the ac current function, op amp U3A and its associated circuitry create a half-wave signal equal to the positive peaks of the ac signal from H4. Resistor R47 keeps this half-wave signal approximately 0.7V above 0V. This half-wave signal is then subtracted from the ac signal coming from H4 by op amp U3B and its associated circuitry. This creates a half-wave signal equal to the negative peaks of the ac signal from H4. Resistor R45 keeps this half-wave signal approximately 0.7V below 0V. Transistor Q15 and resistor R50 generate a current from the negative peaks created by U3B. Transistor Q16 and R48 generate a current from the positive peaks created from U3A. The current from Q15 and R50 develops a voltage across the 191 ohm resistor (R69). This voltage is used by op amp U4 which drives transistors Q11 and Q12 in the Darlington configuration for current gain. Resistor R67 is the feedback path for U4. The voltage across 191 ohm resistor R69 is the same as across the 0.1 ohm resistors R68 and R78. Since the value of R68 and R78 is 1000 times less than R69, the current through R68 is 1000 times greater. The current from Q16 and R48 is increased by 1000, in the same manner as previously stated, with op amp U5, resistors R56 and R57, and Darlington-configured transistors Q13 and Q14.

Only half of the circuitry is used, since the output current is either positive or negative in the dc current function. When outputting a positive current, the voltage from H4 is negative. Since there is no positive voltage, the output of U3A is zero, thus no current is developed by R48 and Q16. At this time the negative voltage from U3B generates an output current in the same manner as in the ac current function. The opposite occurs when outputting a negative dc current.

2-162. 2.2A POWER SUPPLY FILTER CIRCUIT

The 2A range power supply filter circuit on the High Voltage Control assembly (A14), operating in conjunction with the Power Amplifier assembly (A16), generates the VI ±supplies used by the 2.2A amplifier circuit on the High Voltage/High Current assembly (A15). The High Voltage Control assembly generates an amplitude controlled square wave, SQ OUT, from the square wave generator and square wave amplifier circuits. This SQ OUT is amplified by the Power Amplifier assembly (A16), which is set for a gain of 10. This amplified output, PA OUT DC, is connected to the primary side of transformer T1 by relay K1. The stepped-down secondary voltage is full-wave rectified by CR5 and filtered by C3 and C4 to generate the VI+ and VI- supplies respectively. VI± are low-voltage, high current supplies. These supplies, along with the secondary center tap VI COM, are routed to the High Voltage assembly.

VI+ supplies the output current when sourcing while VI- sinks it. To minimize power dissipation, the magnitude of the VI± supplies is controlled to minimize the emitter to collector voltage on the output stage transistors (Q11, Q14). This is done by controlling the magnitude of the SQ OUT signal. The controlling function is described later in the Magnitude Control theory.

2-163. HIGH VOLTAGE DIGITAL CONTROL

Digital control circuitry on the High Voltage Control assembly (A14) also contains the control for the High Voltage/High Current assembly (A15). The heart of the digital control circuitry is an 82C55 Programmable Peripheral Interface IC (U9), which is under software control via the guarded digital bus. This IC has three ports which generate 24 outputs. These outputs are used to control four 5801 driver ICs (U10-U13), and an analog multiplexer (U14) for self diagnostics.

All relays on both HV assemblies are controlled by drivers U10, U11, U12, and U13. Driver U12 controls relays K14-K16, and generates seven control lines for controlling various FETs and CMOS Analog Switch ICs contained on both assemblies. Port A (PA0-PA7) of U9 provides a common input bus for all drivers. Port C (PC0-PC5) of U9 provides the strobe and enable lines for these drivers. Driver U10, which controls the non-latching relays (K1-K6, K8-K13) on the High Voltage Control assembly, is strobed by PC1. PC0 is inverted by U8C to provide the enable. Driver U11 controls latching relay K7 on the High Voltage Control assembly and latching relays K1-K3 on the High Voltage/High Current assembly. This driver is strobed by PC3. PC2 is inverted by U8D to provide the enable. Driver U13, which controls the non-latching relays on the High Voltage/High Current assembly (K4-K12 and K14), is strobed by PC5 and enabled in the same manner as U10. Driver U12, which generates the Control Lines, is strobed by PC4 and enabled in the same manner as U10. Control line RST, from this driver, is inverted by U8E to create PS OFF. This control line is used by the magnitude control circuit described later.

The diagnostic circuit enables the 5700A to monitor seven points on either the High Voltage/High Current assembly (A15) or the High Voltage Control assembly (A14). A 4051 analog multiplexer (U14) is controlled by PB4-PB7 of port B of U9. This multiplexer selects which one of these seven voltages are to be applied to the SDL line where it is measured by the adc circuit on the DAC assembly (A11). HV MUX0-HV MUX3 are points on the High Voltage/High Current assembly. HV MUX0 and HV MUX1 monitor the oven temperature of the H4 and HR7 hybrids respectively. The output of the dc HV amplifier/ac sense buffer circuit is divided by R18 and R19 to generate HV MUX2. HV MUX3 monitors the current draw through the HV dc output series pass circuit to detect an overcurrent condition in the high voltage dc mode. Resistors R28 and R27 sense the current for a positive high voltage output and a negative high voltage output respectively. MUX5-MUX7 are points on the High Voltage Control assembly. MUX5 monitors the high voltage output. HV OUT is divided by R9-R13 and R64.

This divided output is connected to the output peak measure circuit which uses op amp U1B. In the dc V function, this circuit is a voltage follower. In the ac voltage function, this circuit is a peak detector.

The output of U1B charges C5 with R17 being the discharge path. This provides a positive dc voltage at MUX5. The output of the absolute value circuit is divided by R55 and R56 to generate MUX6. The output of the reference and error amplifier circuit is divided by R46 and R47 to generate MUX7.

2-164. HIGH VOLTAGE CALIBRATION

Refer to Figure 2-27 for the following discussion. The resistor network, (70 kilohm and 7 megohm) which is part of the HR7 hybrid/resistor network assembly, determines the accuracy of both 1100V ac and dc ranges. Calibration involves determining its offset and gain constants.

To determine the offset, DAC outputs are connected to 70 kilohm input resistor by K1. The output of the dc HV amplifier is inverted by U1 and its output is connected to the 7 megohm feedback resistor by K9, K8B, and K6. This configuration creates an inverting amplifier with a gain of 100. Relay K9 connects the output of this amplifier to the RCL line, where it is measured by the adc circuit on the DAC assembly (A11). The DAC's adc circuit first connects both its +input and -input to RCOM and takes a checkpoint reading. The +input is then connected to the RCL line, which at this time is the amplifier output, and adjusts the DAC output to obtain the same reading as the previous check point. This offset cal constant is stored in nonvolatile memory.

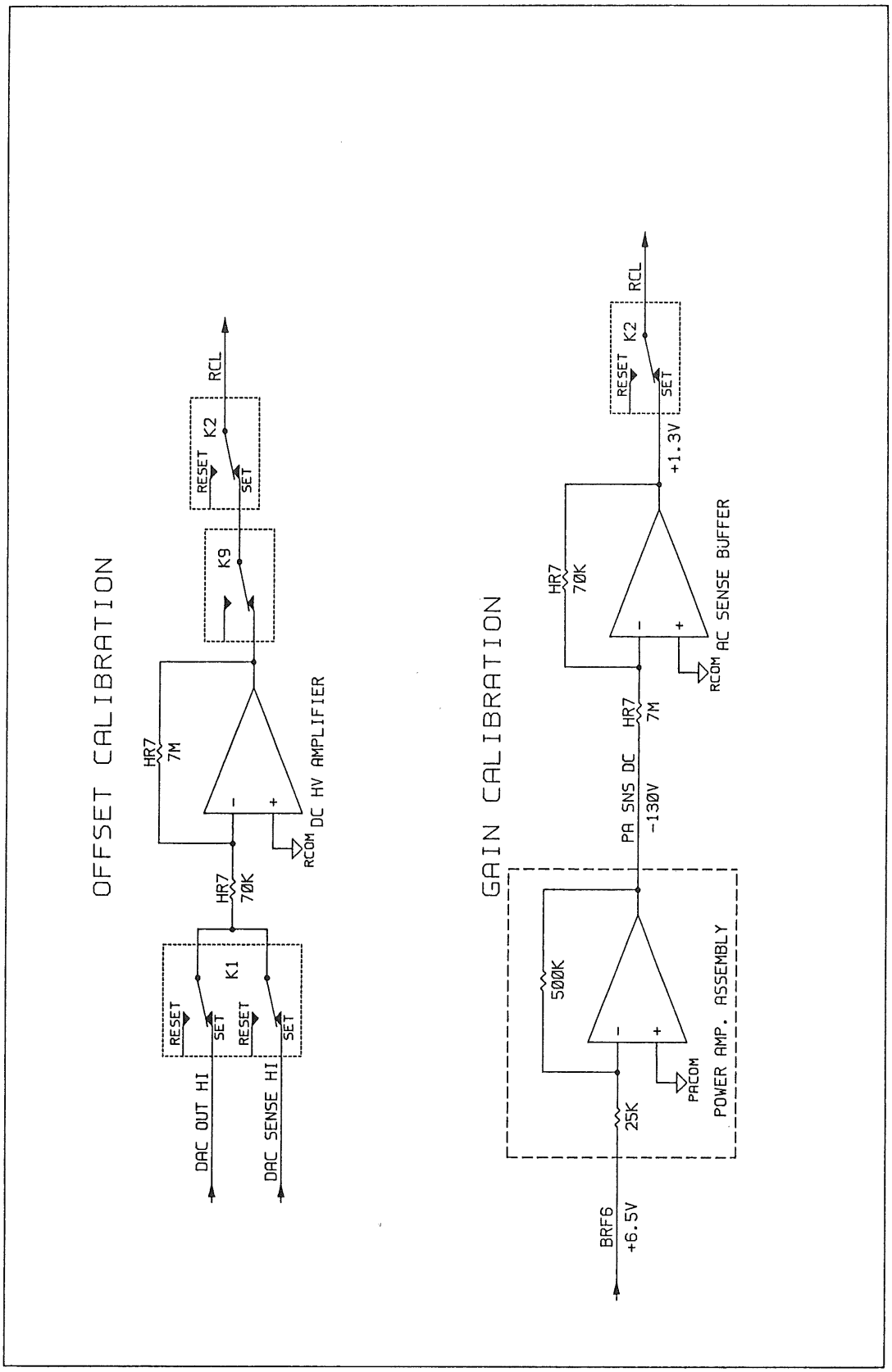

Figure 2-27. High Voltage/High Current Assembly Calibration

To determine the gain, the High Voltage/High Current assembly is configured in the ac 1100V range, except PA SNS DC is connected directly to the 7 megohm input resistor of the ac sense buffer by relays K8 and K6 instead of going through step-up transformer T1. The 6.5V reference (BRF6) is connected to the Power Amplifier assembly (A16) which is configured for an inverting gain of 20 to create a -130V output. The ac sense buffer circuit attenuates this signal by 100 to generate 1.3V at its output. This 1.3V is connected to the RCL line by relay K2 where it is connected to the +input of the adc circuit on the DAC assembly. DAC OUT HI, which is connected to the -input, is adjusted until a null is achieved. The gain can be determined by using this and the previous offset reading. This determines the exact ratio of 70 kilohm and 7 megohm resistor network on the HR7 assembly. This known ratio can then be used to output very accurate dc voltages in 1100V dc range.

2-165. CALIBRATION OF THE AC FUNCTION

The HR7 resistor network, previously calibrated at dc, is further characterized for its frequency response. The 5700A is placed in the ac 1100V range, except with HV OUT and HV SENSE tied by relay K11 on the High Voltage/High Current assembly (A15) instead of being tied at the load. The Oscillator Output assembly is set so the output of the High Voltage/High Current Voltage assembly is approximately 695V at 130 Hz. This high voltage output (INT HV SNS) is connected to the AC CAL line, through 399.6 kilohm resistor Z6, by relays K10 and K8A on the High Voltage assembly. The AC CAL signal is routed to the Oscillator Control assembly (A12) where it is measured by a 400 ohm rms sensor.

Since the voltage is approximately 700V and it is applied through a 399.6 kilohm resistor (Z6) to the 400 ohm rms sensor, approximately 1.75 ma of current flows through the rms sensor on the Oscillator Control assembly. A dc reading of the sensor, which is approximately 0.7V (1.75 mA x 400 ohms), is taken and then stored in memory with the Oscillator Output level.

The Oscillator Output frequency is then increased to 500 Hz. The Oscillator Output level is adjusted so the dc reading from the rms sensor is the same as for 130 Hz, and stored in memory. This step is again repeated at 1 kHz. This characterizes the HR7 resistor network's frequency response. An accurate ac voltage can now be obtained at any frequency between 50 Hz and 1 kHz. The theory of operation for the rms sensor is contained in the Oscillator Control (A12) theory.

2-166. CALIBRATION OF THE CURRENT FUNCTION

Refer to Figure 2-28 for the following discussion. The resistor network Z5 determines the accuracy of the 2.2A current range. Calibration involves determining its offset and gain constants. The 5700A is configured as in the 2.2A dc function, except that the Current assembly (A7) is set to the 2.2 mA range.

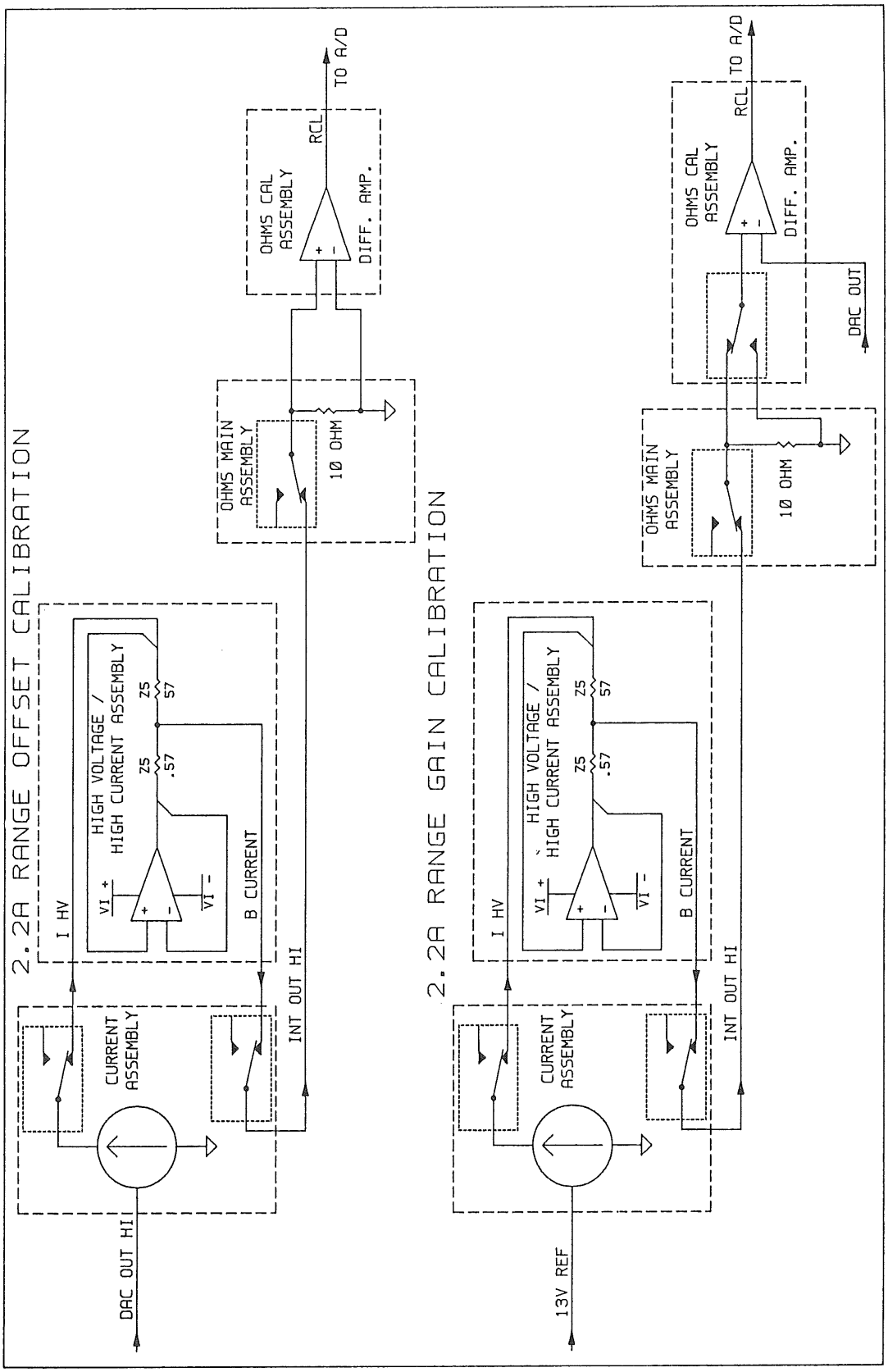

Figure 2-28. High Voltage/High Current Assembly 2.2A Range Calibration

To determine offset, the output (B CUR) is routed back to the Current assembly where it is connected to INT OUT HI. INT OUT HI is routed to the Ohms Main assembly (A10), where it is connected to a previously calibrated 10 ohm resistor. The voltage generated across this 10 ohm resistor is routed to the differential amplifier on the Ohms Cal assembly (A9). The output of the differential amplifier is routed to the DAC assembly (A11) where it is measured by its adc circuit. A checkpoint reading is first taken by removing INT OUT HI from the 10 ohm resistor and measuring the voltage across the resistor. The offset is then measured by connecting INT OUT HI to the 10 ohm resistor. The DAC assembly, which controls the output of the Current assembly, is adjusted until the adc circuit measures the same as the previous checkpoint reading.

To determine gain, the 5700A is configured as in the previous step, except with the Current assembly outputting 1.3 mA generated from the 13V reference (BRF13 and BSRF13) from the DAC assembly. This 1.3 mA is amplified 100 times by the 2.2A amplifier. The resulting 130 mA is connected to the 10 ohm resistor on the Ohms Main assembly by the same path as for the offset calibration. The resulting 1.3V across this 10 ohm resistor is routed to the Ohms Cal assembly (A9), where it is connected to the -input of the differential amplifier. The +input of the differential amplifier is connected to the output of the DAC assembly. The output of the differential amplifier is connected to the RCL line which is routed to the adc circuit on the DAC assembly. The DAC output, which is the +input of the differential amplifier, is adjusted until a null is measured on the RCL line by the DAC's adc circuit. This step is repeated by changing the -input of the differential amplifier to the other side of the 10 ohm resistor. The software now computes the exact voltage drop across the 10 ohm resistor. Gain is determined by using this and the previous offset reading.

2-167. HIGH VOLTAGE MAGNITUDE CONTROL

The square wave (SQ OUT) used in the previously described functions, is created and amplitude controlled by the High Voltage Control assembly (A14). This circuitry, shown on page 2 of the schematic, contains the absolute value circuit, signal/polarity selection circuit, reference and error amplifier, square wave generator, and the square wave amplifier.

The absolute value circuit contains op amp U2A, U2B, Q3, diodes CR8 and CR9, capacitor C20, and resistors R27-R32. During operation in the ac current function, this circuit creates an absolute value of the G OUT signal from the the collectors of the 2.2A output transistors. Op amp U2A generates a negative half-wave signal equal to the positive peaks of G OUT. Resistors R32 and R27 sum this half-wave signal and the input signal G OUT at the input of U2B. Capacitor C20 averages the voltage so the output of U2B is a dc voltage which represents the positive peak voltage of G OUT. In the high voltage dc function, the 2.2A amplifier circuit is not used, so the output of U2B is 0V.

The signal/polarity selection circuit generates the ERROR SIGNAL used by the error amplifier. It contains op amp U2C, CMOS analog switch U6, and resistor R35-R39. Control line V/I controls U6B and U6C which select the VI± when in the current mode. Control lines ±* and ± control U6A and U6D respectively. These switches, operating in conjunction with U6B and U6C, select between VI±, -SP C or +SP C. In the current function, U2C subtracts the power supply voltage (VI±) from the absolute voltage created by the absolute value circuit to create ERROR SIGNAL. This gives a measure of the emitter to collector voltage of the driving device for each operating function. In the positive dc voltage function, U2C is configured as a unity-gain inverting op amp. In the negative dc voltage function, U2C is configured as a voltage follower.

The reference and error amplifier circuit contains op amp U2D, CMOS analog switch U7B, zener diode VR1, transistors Q2 and Q4, diodes CR10-CR11, capacitor C18, and resistors R40-R45. Zener diode VR1, R40-R45, Q4, and U7B create a reference voltage. Control line V/I controls U7B which switches R43-R45 in or out to change this reference voltage value, depending on the operating function. In the HV dc range, R40 and R41 are used, balancing the error amplifier with the ERROR SIGNAL near 6.8V. In the 2A dc range, U7B and Q4 are on, R43 is paralleled with R41, and R45 is paralleled with R40, so the error amplifier balances when the ERROR SIGNAL is near 3.1V. In the 2A ac function, Q4 is off, R44 is in series with R45, so the error amplifier balances when the ERROR SIGNAL is about 5.2V. The output of U2C, ERROR SIGNAL, is summed with the reference voltage by R40 and R41. This voltage is connected to the error amplifier U2D which, with C18, is configured as an integrator. The error amplifier generates the signal AMPLITUDE, which dynamically controls the amplitude of the square wave. This AMPLITUDE is connected to the input of U7C. -AMPLITUDE, provided by inverting op amp U1A, is connected to the input of U7D. Control line PS OFF provides a soft start of the error amplifier. With this line high, Q2 is turned on, shorting C18, which sets the AMPLITUDE control line to 0V. Once the High Voltage/High Current assembly is set up for proper operation, this line goes low to turn off Q2.

The square wave generator circuit creates a 1 kHz signal QSQB and its complement QSQB*. These signals are generated by R26, C17, and astable multivibrator U4. Control line FREQ controls the CMOS analog switch U7A, which parallels R25 to R26. This changes the frequency of oscillation to prevent beating when putting out 2A ac near 1 kHz. Control line PS OFF goes high to shut down this oscillator when its not required.

The square-wave amplifier contains op amp U3 and CMOS analog switches U7C and U7D. Switch U5C is connected to the AMPLITUDE voltage and is controlled by QSQB from the square wave generator. Switch U7D is connected to AMPLITUDE through inverting op amp U1A and is controlled by QSQB* from the square wave generator. The input signal to the square wave amplifier is the output of U7C and U7D. Since QSQB* is the complement of QSQB, the resulting square wave has a positive peak equal to AMPLITUDE, and a negative peak equal to -AMPLITUDE. This square wave is amplified by U3, which is configured for a gain of 2.6, to create SQ OUT. SQ OUT is the square-wave signal used by the Power Amplifier assembly in the previously described functions.

2-168. Ohms Overview

The Ohms function for the 5700A is provided by two plug in circuit boards, the Ohms Main assembly (A10) and the Ohms Cal assembly (A9). These two assemblies function as one to supply fixed values of resistance from 1 ohm to 100 megohm. Resistance output is available in values of $1x10^n$ (1, 10, 100, 1k ... 100M) and $1.9x10^n$ (1.9, 19, 190, ... 19M) from short to 100 megohm. After the ohms function is calibrated, the Output Display shows the true value of the resistance selected.

These assemblies are also used to calibrate the 5700A Current function. The Ohms Main assembly contains all the resistor values except the 1 ohm, 1.9 ohm, and short, which are located on the Ohms Cal assembly. It also contains the relays and their drivers to switch these values as requested under program control.

The Ohms Cal assembly contains all calibration circuits except for one op amp on the Ohms Main assembly. It also contains a circuit to provide accurate calibration of two-wire ohmmeters. In addition, there are relays, relay drivers, and logic to interface the Ohms assemblies to the digital bus.

2-169. Ohms Main Assembly (A10)

The Ohms Main assembly uses three Fluke hermetically-sealed thin film resistor networks (Z1, Z2 and Z3) to obtain values from 10 ohm to 19 megohm. The values are arranged in two strings, one for decade values and the other for the multiples of 1.9. The 100 megohm value is achieved by inserting a 90 megohm film resistor (R1) in series with the decade string.

2-170. SELECTION OF RESISTANCE VALUES

Refer to Figure 2-29 for the following discussion. Relays select the resistance values. All resistor values have four-wire connections except 100 megohm, which is two-wire. The output high and sense high side of a resistance value is connected to INT OUT HI and INT SENSE HI by relays K1 and K2 in the reset position, except 100 megohm, which is connected to INT OUT HI by K5. Relays on the Motherboard connect INT OUT HI and INT SENSE HI to the OUTPUT HI and SENSE HI binding posts.

The low side of the 1x string is connected to OHMS SENSE LO and OHMS OUT LO by relay K27 (A and B) in the reset position. The low side of the 1.9x string is connected to the same lines by relay K39 (A and B). These lines are routed to the Ohms Cal assembly where they are connected via relays to the OUTPUT LO and SENSE LO binding posts.

The 10 megohm value is selected by K7 (reset) and K8 (energized) and the 1 megohm value by K9 and K10 (reset). Selection of decades below 1 megohm is done by K15 and K16 (reset) plus a pair of relays from K17 through K26A. For example, to select 10 kilohm, relays K18A and K20A are reset.

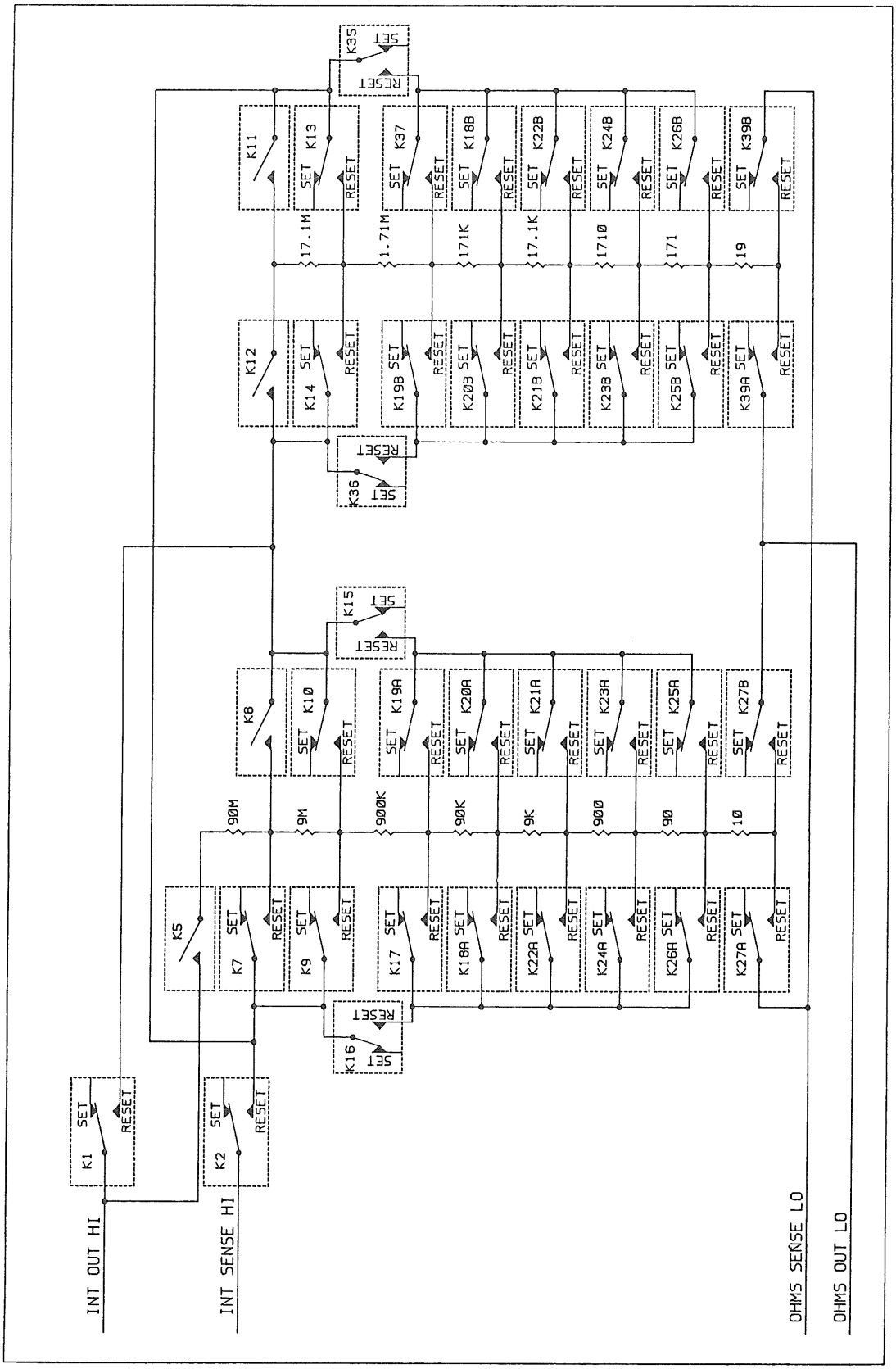

Figure 2-29. Ohms Main Assembly Simplified Schematic

The 19 megohm value is selected by K11 and K12 (energized), and the 1.9 megohm value by K13 and K14 (reset). Selection of 1.9 decades below 1.9 megohm is done by K35 and K36 (reset) plus a pair of relays from K18B through K26B and K37.

Two lines, OHMS OUT HI and OHMS SENSE HI, are brought over to the Ohms Cal assembly to connect to 1 ohm, 1.9 ohm, and short. These lines also access resistance values during calibration. Relay K29 connects OHMS OUT HI to the $1x10^n$ string when set, and to the $1.9x10^n$ string when reset. Relay K30 connects OHMS SENSE HI to the $1.9x10^n$ string during calibration.

Relays K3, K28, K31-K34, and op amp U1 and its associated components are only used during calibration. Operation of this circuitry is described in the "Calibration" part of the Ohms Cal theory.

Relays K4 and K6 are used during two-wire compensation. This is described in the "Two-Wire Compensation" part of the Ohms Cal theory.

2-171. OHMS MAIN ASSEMBLY SUPPORT OF CURRENT FUNCTION CALIBRATION

To calibrate the current function, the Current assembly routes output current to the Ohms Main assembly, where it is connected through a resistance. Current is determined by measuring the voltage across this resistance. During calibration, half of K38 connects DAC OUT LO to the SENSE LO side of the $1x10^n$ string (Z1 pin 6). The Current assembly generates approximately 60 uA of current on the DAC OUT LO line, which can cause an error during measurement. To prevent this error, half of relay K38 connects the -17S supply through R6 to the DAC OUT LO line. This generates an opposite-polarity 60 uA current to cancel the current from the Current assembly.

2-172. OHMS DIGITAL CONTROL

The Ohms Main assembly is digitally controlled by the 82C55 Programmable Peripheral Interface IC on the Ohms Cal assembly. This IC, under system software control through the guarded digital bus, has three ports generating 24 outputs. PA0-PA7 of port A, PB0-PB3 of port B, and PC0-PC4 of port C are routed on the Motherboard to the Ohms Main assembly. These lines and two decoders in U9 and U10 control nine relay driver ICs, which in turn control 39 Ohms relays. Relay driver U3 drives non-latching relays K5, K6, K8, K11, K12 and K38. Relay drivers U2, U5-U8, and U11-U13 drive the latching relays.

Port A (PA0-PA7) is a common input bus for all relay drivers. IC U9 decodes PB0-PB3 to strobe the latching relay drivers. This signal causes the contents of the data on the input bus to be latched into the latch portion of the selected device. IC U10 decodes PC0-PC3 to provide four enable lines. Each line goes to two latch/drivers and when true (0V), drives the relay coils on or off according to the contents of the latch. Since these are latching relays, they are pulsed only briefly. The latching relays each have two coils, one to set the relay and one to reset it. When the ohms function is not being used, all relays are set, as shown on the schematic.

PC4 is the strobe line for non-latching relay driver U3. The enable is connected to LH COM so the relays receive constant drive. These non-latching reed relays are shown in the non-energized state.

2-173. Ohms Cal Assembly (A9)

The Ohms Cal assembly (A9) contains the 1 ohm, 1.9 ohm, and short resistance values. It also contains a digital control circuit, and a two-wire compensation circuit to allow accurate calibration of two-wire ohmmeters. A differential amplifier circuit and a 2/5/10V source circuit are used during calibration of the ohms function.

2-174. OHMS CAL DIGITAL CONTROL

The heart of the Ohms Cal assembly digital control circuit is the 82C55 Programmable Peripheral Interface IC (U11) mentioned previously under "Digital Control". This IC has three ports generating 24 outputs. These outputs control seven 5801 latching relay drivers ICs (U14-U20), a 4051 analog multiplexer (U21) for self diagnostics, and several FET switches.

Port A (PA0-PA7) is a common input bus for latching relay drivers and multiplexer U21. These lines also go to the Ohms Main assembly as previously described to control relay drivers there.

Lines PB0-PB3 of port B goes to decoder U12 (PB3 is inverted by U22) and to the Ohms Main assembly. The output of U12 strobes latch/driver ICs to latch data on input bus lines.

Lines PC0-PC3 of port C go to decoder U13 and to the Ohms Main assembly. Decoder U13 enables two latch/driver ICs at a time. Setting the enable true (0V) causes the relay coils to be driven on or off depending on the contents of the latch portion of the selected ICs. Since these are latching relays, they are pulsed only briefly.

The outputs PB4, PB5 and PB6 of U11 are connected to the gates of FETs Q2, Q3 and Q4 respectively. The Programmable Peripheral Interface IC turns them on for a one (5V) and off for a zero (0V). PB7 is connected to the base of Q6 through R31. When PB7 is true (5V), it turns on Q6, which turns on Q5, which in turn supplies +17S to U6. PC4 goes to the Ohms Main assembly where it strobes relay latch/drivers for the non-latching relays.

Line PC6 goes to the diagnostic circuit where it enables and disables output from the multiplexer (U21). Connected to the input of the multiplexer are five voltage dividers made from resistors in Z3 and Z4.

Two inputs to these dividers are connected. One is 10V OUT HI from the 2/5/10V source circuit. The other is 2W COMP from the two-wire compensation circuit. These inputs are connected to the SDL line by the multiplexer, where they are routed to the adc circuit on the DAC assembly and measured during calibrator diagnostics. PC7 is not used.

2-175. 1, 1.9, AND SHORT RESISTANCE

Although located on the Ohms Cal assembly, the 1 ohm value, 1.9 ohm value, and short operate as part of the Ohms Main assembly, filling out the range of values available to the operator. The 1 ohm value is made of four 4 ohm wirewound resistors in parallel (R41). The 1.9 ohm value is made of two 3.8 ohm wirewound resistors in parallel (R42). Relays K4 and K5 connect the 1 ohm and 1.9 ohm values to OHMS OUT HI and OHMS SENSE HI. Relays K6 and K30 connect them to OHMS OUT LO and OHMS SENSE LO. Relays K7 and K8 select the short.

The Ohms Cal assembly contains the relays that switch the low side of the selected resistance onto the output bus. (High sides are connected to the output bus by relays on the Ohms Main assembly.) Relay K24 connects OHMS OUT LO to OUT LO and K25 connects OHMS SENSE LO to INT SENSE LO.

2-176. TWO-WIRE OHMMETER COMPENSATION CIRCUIT

Refer to Figure 2-30 for the following discussion. The Ohms Cal assembly contains a two-wire lead drop compensation circuit that allows accurate calibration of two-wire ohmmeters. The error normally encountered when calibrating a two-wire ohmmeter is due to the voltage drop in the path resistance between the meter and the calibration resistor. This circuit reduces the voltage drop to an insignificant level.

2-177. Two-Wire Compensation Power Supplies

The floating supplies for U7 and U8 consist of a dc-to-dc converter made up of U6, T1 and associated components. Switching-regulator control IC U6 switches +17S through the primary of T1 at about 30 kHz as determined by R27 and C21. The switching creates high-frequency spikes on the +17S line which are filtered out by L2, R25, C18, C19, C20, and C52. When the two-wire compensation circuit is not in use, control line PB7 turns Q5 and Q6 off, which removes +17S, switching off U6. The secondary of T1 is rectified and filtered by CR1, CR2, CR9, CR10, C22, and C23. The voltage is then regulated by 8.2V zener diodes VR1 and VR2. Additional filtering is provided by L3, L4, R43, R44, C24, and C25. Two capacitors (C53 and C54) between A COM and S COM reduce switching noise that would otherwise appear across the calibration resistor.

2-178. High Side Cancellation

The high side voltage drop is eliminated by U7 and U8. Chopper-stabilized op amp U7 and buffer amplifier U8 supply up to 10 mA. The current from the high side of the ohmmeter being calibrated enters at the OUTPUT HI binding post, goes through K1 and K6 on the Ohms assembly, and is routed to the Ohms Cal assembly where it connects to A COM. The A COM connection is a common for the floating supply that powers U7 and U8. The current then flows out of U8 through 500 ohm in Z2 and through K29 to the calibration resistor via the OHMS OUT HI line.

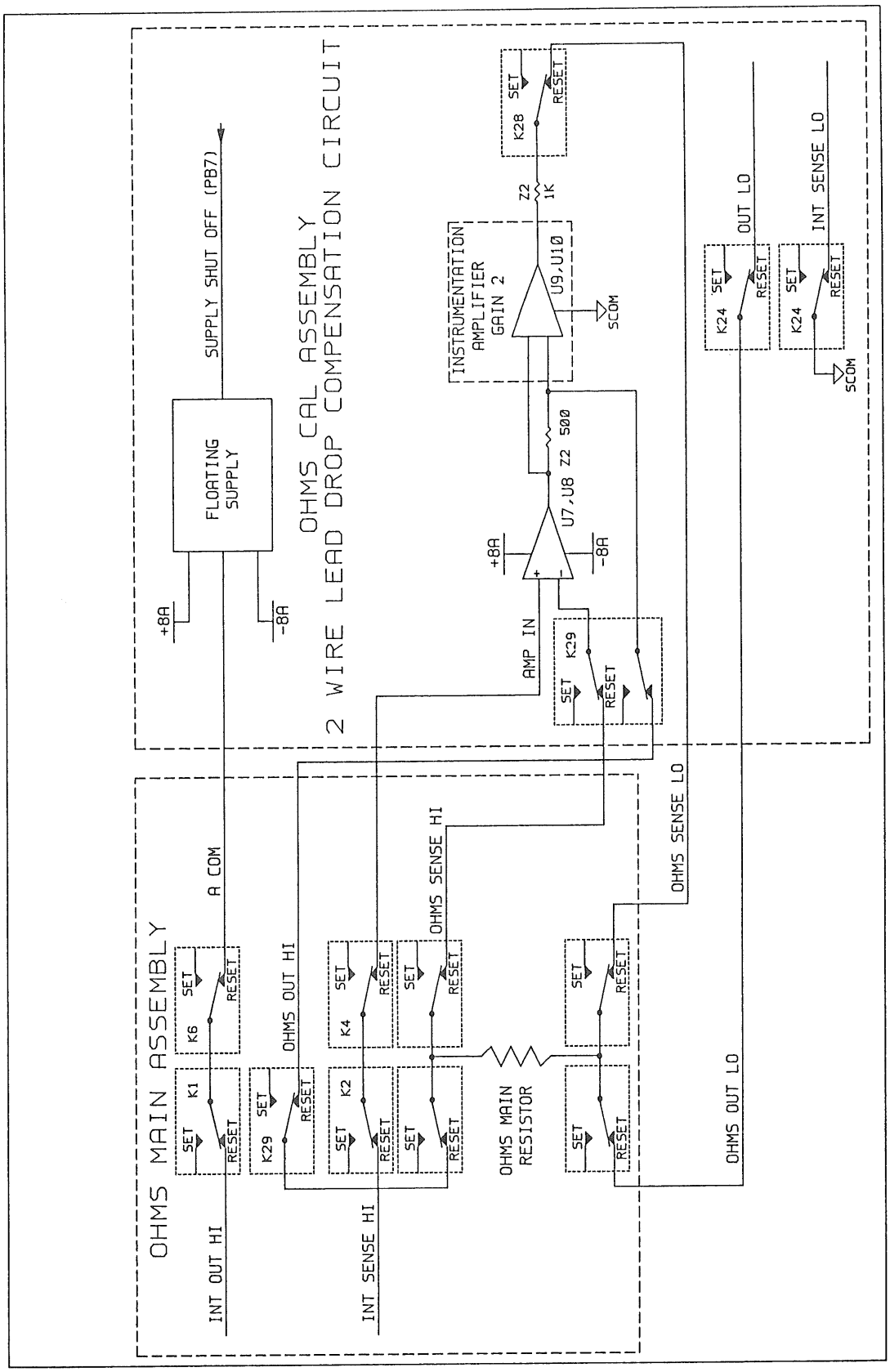

Figure 2-30. Two-Wire Lead Drop Compensation Circuit

K29 connects the -input of U7 to the sense point of the calibration resistance via OHMS SENSE HI. Relays K2 and K4 on the Ohms Main assembly connect the +input of U7, AMP IN, to INT SENSE HI. Relays on the Motherboard connect INT SENSE HI to the OUTPUT HI binding post. Connected this way, U7 controls the voltage at the output of U8 so that the voltage at the input of U7 stays zero. This forces the voltage drop in the path to zero. Diodes CR3-CR6 and resistor R45 provide protection for U7.

2-179. Low Side Cancellation

The voltage drop in the low side path is cancelled by current from high current op amp U9. U9 is driven by dual FET input op amp U10. The two non-inverting inputs of U10 are connected across the 500 ohm resistor in Z2. This enables U10, in conjunction with the four 10K resistors in Z2, to sense the current in the high side path and to supply (through U9 and the 1 kilohm resistor in Z2) a current equal but opposite to the current through the low side path. This cancels the drop in that path. This cancelling current goes through relay K28A to the low sense point of the calibration resistor via OHMS SENSE LO. From there it goes through the output low path to the OUTPUT LO binding post and then through the sense low path back to the Ohms Cal assembly and through K28B to S COM.

2-180. OHMS CALIBRATION

The remaining circuitry is used only for calibration of the resistor values. All values except 1 ohm and 1.9 ohm are calibrated using a single external 10 kilohm resistance standard connected to the binding posts. The 1 ohm and 1.9 ohm values are calibrated using an external 1 ohm standard. How to do the procedure is described in Section 7 of the Operator Manual.

2-181. Calibrating to the External 10 Kilohm Standard

Refer to Figure 2-31 for the following discussion. The first step in ohms calibration is to compare the 10 kilohm standard against the 10 kilohm value on the Ohms Cal assembly. This is done by passing a current through both values and measuring the voltage drop across each. The ratio of the voltages is equal to the ratio of the resistances.

The source of current comes from the 2/5/10V source circuit, which contains U1, Q1, Q2, Q3 and Z1. The buffered 13V reference voltage from the DAC assembly (A11) is switched through K9 to a voltage divider made up of resistors in Z1.

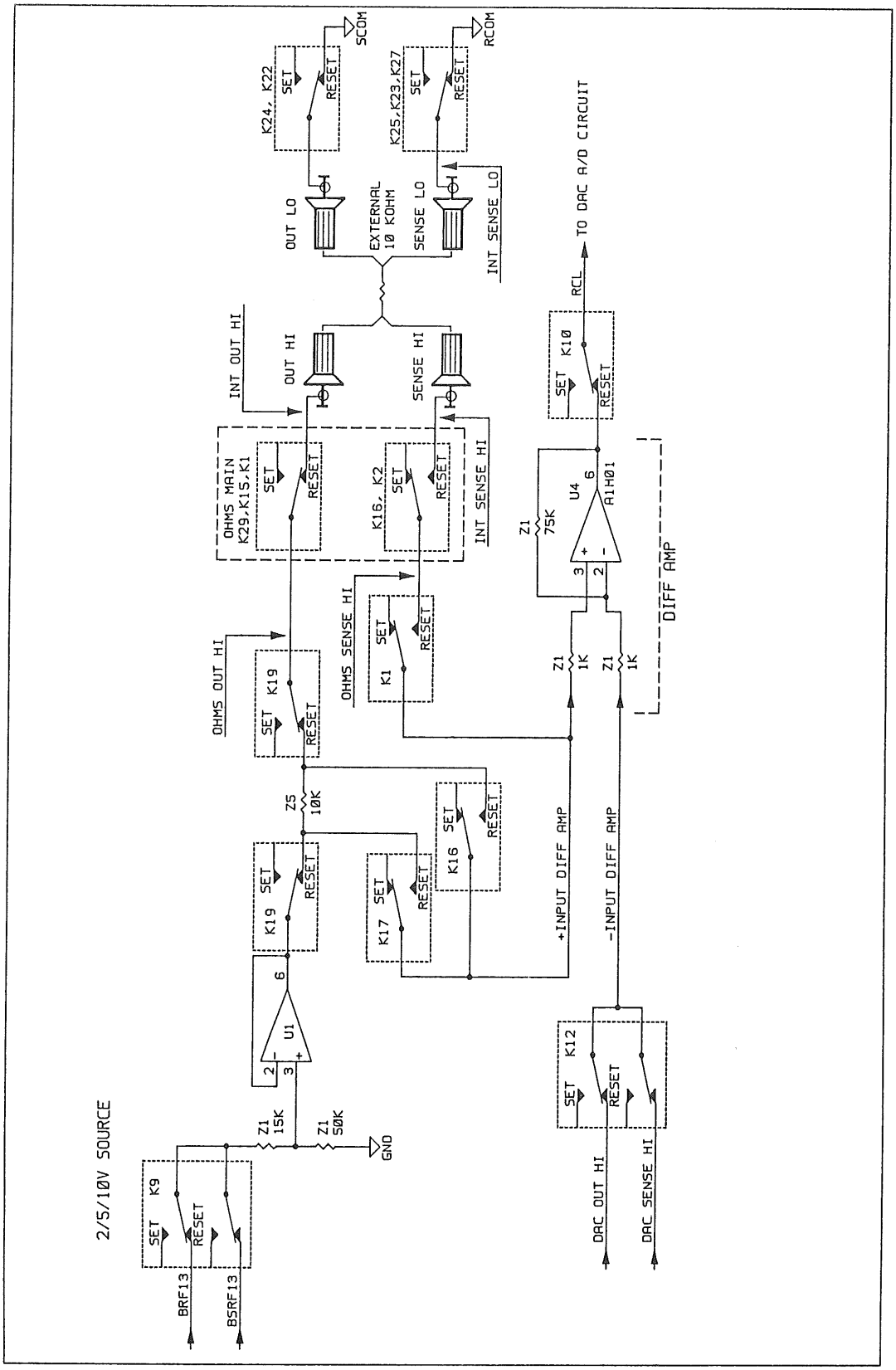

Figure 2-31. Calibration to an External 10 Kilohm Standard

To calibrate the 10 kilohm resistance, control lines PB4 and PB5 turn off FETs Q2 and Q3 respectively. In this mode, the output of the divider uses the 15 kilohm and 50 kilohm values to produce an output of 10V. This voltage is buffered by U1 and Q1. The current from this source, 10V OUT HI, is sent through K19 to one side of the 10 kilohm resistance in Z5. 10V SENSE HI is connected to 10V OUT HI by K31A on the Ohms assembly. The other side of the 10 kilohm resistance in Z5 is connected to OHMS OUT HI by K19. This is routed to the Ohms Main assembly where is goes through K29, K15 and K1 to INT OUT HI, which is connected to the OUTPUT HI binding post by relays on the Motherboard. From there it goes through the external 10 kilohm standard and back in through the OUTPUT LO binding post and over to the Ohms Cal assembly where it connects to S COM through K24 and K22.

The voltage drops are measured by comparing each voltage to the DAC assembly output in a differential amplifier circuit made of U2 through U5.

Since the DAC and differential amplifier are referenced to R COM, this line is brought out through K27, K23 and K25 to INT SENSE LO. This is connected to the SENSE LO binding post (which is connected to the sense low point of the standard). Line DAC OUT LO is tied to S COM by relay K31. The high side of the DAC, DAC OUT HI and DAC SENSE HI, are tied together and connected by K12 to U2, which is the differential amplifier -input.

The voltage to be measured is connected to U3, which is the differential amplifier +input. The output of U2 and U3 goes to U4 through gain setting resistors in Z1. These set the gain of the differential amplifier to 75. The differential amplifier generates a current through the 1 kilohm (pins 1-2) and 75 kilohm (pins 2-3) resistors in Z1 to R COM. This current on R COM can cause an error during measurement. Op amp U5, configured as an inverting amplifier, generates an equal current of opposite polarity through 76 kilohm resistor R18 to cancel the current from the differential amplifier. The output of U4 goes through K10 to the RCL line. This line is connected to the DAC assembly, where it goes through an amplifier to the adc circuit.

The calibration program uses the adc circuit to measure the differential amplifier output voltage. First the differential amplifier offset voltage is determined. (This offset is different for each input condition.) Readings are taken to determine each offset voltage by checking the output of the differential amplifier at equal voltages on the inputs. This is done by switching K11 to the reset position to connect the differential amplifier +input and -input together, then measuring the output with the DAC's adc circuit.

Once the offsets are known, the software determines the calibration voltages by adjusting the DAC output until the adc reading is the same as the offset. At that point, the DAC output equals the voltage being measured.

Three readings are required to determine the ratio of the two resistances. For the first reading, K16 connects the differential amplifier +input to the 10 kilohm resistor in Z5. For the second reading, K17 connects the +input to the other side of that resistor. Subtracting the first reading from the second gives the voltage across the internal 10 kilohm. For the third reading, K1 on the Ohms Cal assembly connects the + input to OHMS SENSE HI. OHMS SENSE HI is connected to INT SENSE HI by K16 and K2 on the Ohms Main assembly. INT SENSE HI is connected to the SENSE HI binding post by relay K2 on the Motherboard which is the sense high side of the 10 kilohm external standard. The ratio of this third reading to the difference of the first two readings is proportional to the ratio of the two resistances. Thus by knowing the resistance of the external standard, the software can calculate the value of the internal 10 kilohm resistance value.

2-182. Calibrating 10 kilohm and 19 kilohm

The next step in calibrating the ohms function is to determine the 10 kilohm and 19 kilohm values on the Ohms Main assembly. This is done just like the 10 kilohm value on the Ohms Cal assembly, except the 10 kilohm resistance on the Ohms Cal assembly acts as the standard and is placed in series with 10 kilohm or 19 kilohm on the Ohms assembly.

This is done using K19 on the Ohms Cal assembly and K29, K20A and K27 on the Ohms Main assembly for the 10 kilohm, and K29, K20B and K39 for the 19 kilohm value. The source on the Ohms Cal assembly again outputs 10V. Again three readings are taken. The first and second are the same as previously described. For the third reading, the differential amplifier +input is connected through K1 on the Ohms Cal assembly and through K18A on the Ohms Main assembly for 10 kilohm and K30 and K18B for 19 kilohm. The software then calculates the 10 kilohm and 19 kilohm values using the ratio of readings and the known value of the 10 kilohm on the Ohms Cal assembly.

2-183. Calibrating 100 kilohm

Once the 10 kilohm value is determined, the 100 kilohm value is calibrated by comparing its value against 10 kilohm. The 10V source is connected across 100 kilohm. Since the 10 kilohm resistance is used as part of 100 kilohm, the current goes through both.

Relays K33 and K19A on the Ohms Main assembly connect 10V OUT HI to 100 kilohm. Relays K23 and K27 on the Ohms Cal assembly connects OHMS SENSE LO to RCOM. OHMS OUT LO, DAC OUT LO, and 10V SENSE LO are connected to SCOM. Relay K22 on the Ohms Cal assembly connects OHMS OUT LO to SCOM. OHMS OUT LO is connected to DAC OUT LO by K31 on the Ohms Cal assembly, and to 10V SENSE LO by K31B and K28 on the Ohms Main assembly.

Only two readings are required because this time there is no path resistance to subtract out. DAC OUT HI and DAC SENSE HI are tied together and connected to the -input of the differential amplifier by relay K12.

For the first reading, the +input of the differential amplifier is connected to the sense side of the 100 kilohm point in the string through K1 on the Ohms Cal assembly and K17 on the Ohms Main assembly. For the second reading, the + it is connected to the 10 kilohm point by K18A. The software calculates the 100 kilohm value from the ratio of the readings and the known 10 kilohm value.

2-184. Completion of High Resistance Value Calibration

Once 100 kilohm is determined, 1 megohm and the other values up to 100 megohm are determined in a similar way. Using the same techniques, 190 kilohm is calibrated against 19 kilohm, and so forth up to 19 megohm.

Too much current noise is generated by U3 in the differential amplifier circuit for accurate calibration of resistances above 1 megohm. For these values, U1 on the Ohms Main assembly (a low-bias current FET op amp) is switched ahead of U3.

The 1 kilohm and 1.9 kilohm resistance values are determined from the 10 kilohm and 19 kilohm respectively. The resistance values of the 100 ohm and 190 ohm use the same technique, but using 5V instead of 10V from the 2/5/10V source circuit. To get 5V, Q2 is turned on to parallel the 11.535 kilohm value in Z1 with the 50 kilohm value.

The 10 ohm and 19 ohm resistance values are determined using 2V from the 2/5/10V source and using internal 10:1 divider (Z5) in conjunction with the DAC. To get 2V, Q2 and Q3 are both turned on, which parallels both the 11.535 kilohm value and the 3.846 kilohm value with the 50 kilohm value. The lower voltage is required to lower the power dissipation in the resistors.

Using 2V presents a problem for the DAC. Instead of working at 10V and 1V, it would be working at 2V and 0.2V. This level is too low to get accurate results from the DAC. To solve this problem, the DAC is used only at 2V and the 0.2V level is achieved using a 10:1 divider. The DAC calibrates this 10:1 divider at 10V and 1V. The divider is made of a 90 kilohm and a 10 kilohm resistor in Z5. To calibrate the divider, 10V is applied to the top of the divider through K18. The low side of the divider is connected to R COM (K21 and K27), DAC OUT LO (K21) and S COM through K20 on the Ohms Cal assembly, K27A/B on the Ohms Main assembly and K22 on the Ohms Cal assembly. Two readings are taken. Their ratio is equal to the division ratio of the divider. The -input of the differential amplifier is connected to the DAC output by K12. For the first reading, K15 connects the top of the divider to the +input of the differential amplifier. For the second reading, K16 connects the divider point to the +input of the differential amplifier. The exact ratio of this divider can now be determined by these two readings.

Refer to Figure 2-32 for the following discussion. To calibrate the 10 ohm resistor, the DAC output is connected to the top of the divider by K14. The 2V source is connected across 100 ohm on the Ohms Main assembly. This is done by 10V OUT HI, set to 2V, connected to the high side of the 100 ohm string by K33 and K23A on the Ohms Main assembly. Line 10V SENSE HI is also connected to this point by K31A and K32A on the Ohms assembly. Line OHMS OUT LO and OHMS SENSE LO are connected to the low side of the 100 ohm string by K27B and K27A respectively. Line OHMS OUT LO is connected to SCOM by K22 on the Ohms Cal assembly and is also connected to 10V SENSE LO by K32B and K31B on the Ohms Main assembly. OHMS SENSE LO is connected to the low side of the internal divider by K20 on the Ohms Cal assembly. The Ohms Cal assembly also connects RCOM to the low side of the divider by K27 and K21. Relay K21 also connects this point to DAC OUT LO.

Two measurements are taken. The first is with the +input of the differential amplifier connected to the DAC output through K15. The - input is connected to the sense point of the 100 ohm resistance by K24A on the Ohms Main assembly and K2 on the Ohms Cal assembly. The DAC is adjusted until its value is the same as the voltage across 100 ohms. Then the inputs of the differential amplifier are moved. The +input is connected to the divider output on the Ohms Cal assembly by K16. The - input is connected to the sense point of the 10 ohm resistance by K26A on the Ohms Main assembly and K2 on the Ohms Cal assembly. The DAC is again adjusted until the voltages are equal. The differential amplifier sees 0.2V on each input for this measurement but the DAC is at 2V. The value of 10 ohm is determined from the two DAC settings and the division ratio of the divider on the Ohms Cal assembly. The same procedure is used to determine the 19 ohm value from the 190 ohm value.

2-185. Calibrating to the External 1 ohm Standard

The 1 ohm and 1.9 ohm resistor values are calibrated by comparing them against a 1 ohm external standard. The technique used is different from that used for the 10 kilohm external standard.

The Current assembly supplies a 130 mA (65 mA for 1.9 ohm calibration) current through both resistors. This current goes out the OUTPUT HI binding post to the 1 ohm standard. It comes back in through the OUTPUT LO binding post and through the internal 1 ohm resistance by K26 and K6, or 1.9 ohm by K26 and K30 before going to S COM through K22.

For the first reading, the inputs to the differential amplifier are connected across the sense points of the 1 ohm standard. Relay K1 connects the differential amplifier +input to OHMS SENSE HI, which is connected to INT SENSE HI by K16 and K2 on the Ohms Main assembly. INT SENSE HI is connected to the SENSE HI binding post by relays on the Motherboard. Relay K13 connects the differential amplifier -input to INT SENSE LO which is connected to SENSE LO binding post by relays on the Switch Matrix assembly.

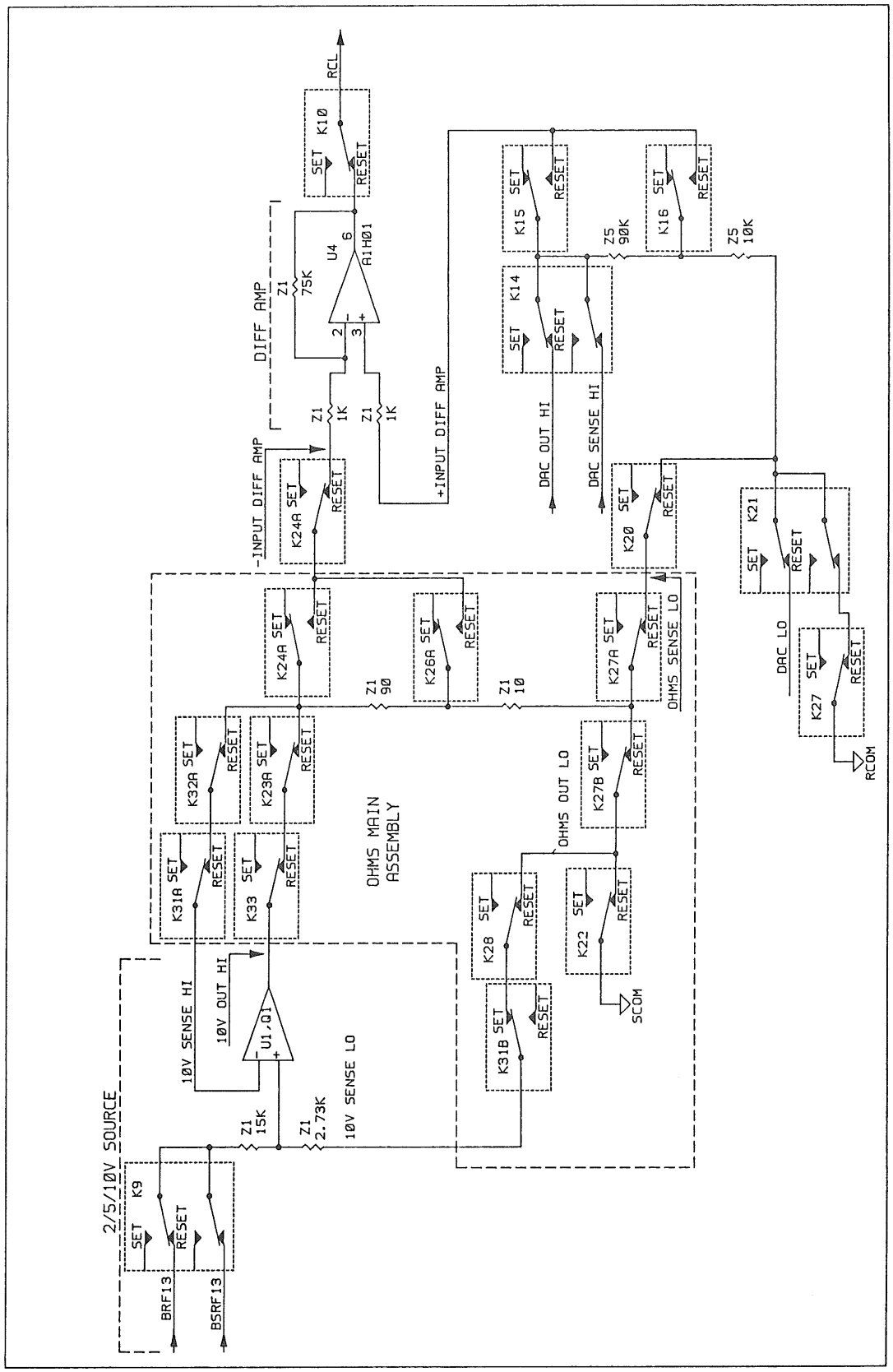

Figure 2-32. Ratio Calibration, 10 ohm From 100 ohm

The voltage between the inputs is 0.13V, which is amplified by 75 by the differential amplifier to approximately 9.75V and sent to the DAC assembly on the RCL line. Another differential amplifier on the DAC assembly compares the 9.75V to the DAC output. Before the reading is taken, however, amplifier offsets are determined.

When the DAC output equals the output of the differential amplifier on the Ohms Cal assembly, the reading is stored and a second reading is taken. For this reading, the inputs to the differential amplifier on the Ohms Cal assembly are connected across the 1 ohm or 1.9 ohm on the Ohms Cal assembly. The +input of the differential amplifier is connect through K1 and K4 and the -input is connected through K2 and FET Q4. The second reading is taken the same way as the first. The ratio of the two DAC settings are equal to the ratio of the values of the two resistors. The value of the 1 ohm and 1.9 ohm resistors are determined from this ratio and the value of the external standard.

2-186. Current/High Resolution Oscillator Assembly Overview (A7)

The Current/Hi-Res (High-Resolution Oscillator) Assembly combines two functions on one circuit board. The Current section generates dc and ac currents in the range of 20 uA to 220 mA. The Hi-Res section generates a high-resolution signal accurate in frequency to 4-1/2 digits, which is used by the phase-locked loop circuit on the Oscillator Output assembly (A13). These two functions are independent circuits except for the sharing of some digital controlling and self-diagnostic monitoring. The following theory describes the digital control circuitry used by both circuits, then independently covers the Current and Hi-Res functions.

2-187. CURRENT/HI-RES DIGITAL CONTROL

The heart of the Current/Hi-Res assembly digital control circuitry is a 82C55 Programmable Peripheral Interface IC (U7), which is under software control via the guarded digital bus. This IC has three ports which generate 24 outputs. These outputs control three UCN5801 latching relay drivers ICs (U8-U10), a UCN5800 relay driver (U11) for controlling non-latching relays, a 4051 analog multiplexer (U12) for self diagnostics, and several FET switches throughout the assembly. Port A (PA0-PA7) is a common input bus called CONTROL BUS on the schematic. This CONTROL BUS transmits the desired state of all the relays (K1-K17) in the Current section, and also to control two synthesizer ICs (U16, U17) in the Hi-Res section.

Four relay driver ICs drive latching controlling relays K1-K13 and K16. The CONTROL BUS (port A of U7) is a common input bus. Port C of U7 (PC0-PC5) provides the strobe and enable lines for these relay drivers. PC0 enables U8, while PC1 enables U9 and U10. PC2, PC3, PC4, and PC5 strobe U11, U8, U9, and U10 respectively.

Relay driver U11 controls the three non-latching relays K14, K15, and K17 on this assembly. It also generates control line RLY11* to control K11 on the Motherboard. Relay K11 routes I-GUARD, described later, to the rear panel for operation when the rear-panel binding posts are in use.

The diagnostic circuit allows the calibrator to monitor five points on the assembly. Points DUMMY LOAD, OVEN TEMP, and CUR/COMP MONITOR are from the Current section. Points HI-RES LOOP and HI-RES CLOCK come from the Hi-Res section. Outputs PB0-PB2 select which point the multiplexer U12 monitors. PC6 enables the output of U12 to the SDL line, where it is measured by the adc circuit on the DAC assembly (A11).

Outputs PB3-PB5 generate control lines FET3, FET1, and FET2 respectively, which are used by the Current section. FET1 controls NMOSFETs Q21 and Q22, FET2 controls Q20 and Q23, and FET3 controls quad CMOS analog switch U5.

Outputs PB6 and PC7 generate control lines HI-RES RANGE and HI-RES ON/OFF respectively, which are used by the Hi-Res section. These lines control quad CMOS analog switch U18 and comparator U13.

2-188. Current Section (A7)

The current section of the A7 assembly uses dc voltage from the DAC assembly and ac voltage from the Oscillator Output assembly to generate both ac and dc current outputs.

Four ranges of output current are generated:

	DC Current	AC Current
220 uA Range:	0 - 219.9999 uA	9.000 uA - 219.999 uA
2.2 mA Range:	0.220000 mA - 2.199999 mA	0.22000 mA - 2.19999 mA
22 mA Range:	2.20000 mA - 21.99999 mA	2.2000 mA - 21.9999 mA
220 mA Range:	22.0000 mA - 219.9999 mA	22.000 mA - 219.999 mA

Each range provides dc or ac current. AC current is available from 40 Hz to 10 kHz.

A 2.2A range is generated on the High Voltage/High Current assembly (A15) and routed to this assembly for switching to the OUTPUT binding posts. This is further described under the heading, "2.2A Range."

The transconductance amplifier, shunt resistors, feedback loop, and complementary drive circuits form a loop to create the output current. In addition to these circuits, the Current assembly contains input switching, output switching, a current guard, and a current/compliance voltage monitor. Each of these circuits is described in detail. To better understand the theory of operation, refer to Figure 2-33 and the schematic.

2-189. CURRENT INPUT SWITCHING

Relay K1, CMOS analog switch U5B, and FETs Q20-Q23 select the input source voltage. For dc operation, the 22V range of the DAC assembly (A11) is brought in on the B IN and B FB lines from the Switch Matrix assembly (A8). For ac operation, the 22V range of the Oscillator Output assembly (A13) is brought in on the B IN and B FB lines. During calibration of the current functions, the 13V buffered dc reference BRF13 and BSRF13 are selected when K1 is set and U5B is closed.

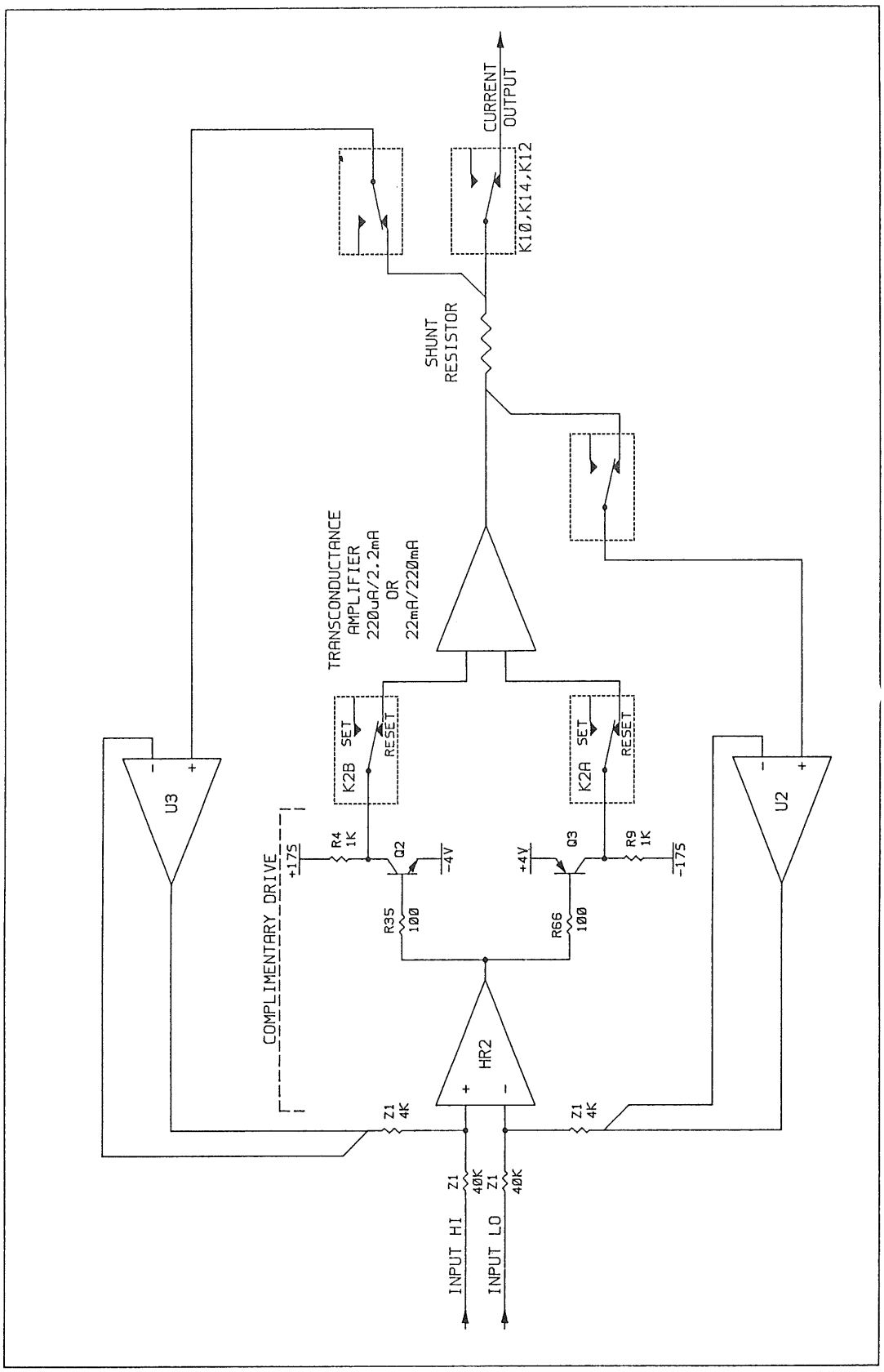

Figure 2-33. Current Output Simplified Schematic

The input signal return paths are selected for ac or dc operation by control lines FET1 and FET2, and NMOSFETs Q20-Q23. With a dc or 13V reference input, control line FET1 goes high, turning on Q21 and Q22, connecting RCOM and DAC OUT LO to the respective circuit. For ac current input, control line FET2 goes high, turning on Q20 and Q23, connecting OSC SENSE LO and OSCOM to the respective circuit.

2-190. COMPLEMENTARY DRIVE CIRCUIT

The circuitry containing transistors Q2, Q3, Q18 and Q19 provides the complementary drive to the output transconductance amplifiers from the single-ended output dc amplifier on hybrid HR2. Transistors Q2 and Q18 provide the drive during a positive input, while Q3 and Q19 provide the drive during a negative input. Relay K2 switches the drive to the 220 uA/2.2 mA transconductance amplifiers when reset, or to the 22 mA/220 mA transconductance amplifier when set.

The HR2 assembly consists of an op amp mounted on a heated-substrate hybrid, bonded to the shunt resistor network. The HR2 assembly gives this circuit excellent dc characteristics of low offset, noise and drift. The hybrid heater control circuit, outlined on page 2 of the schematic, adjusts the base voltage of Q1 to deliver the proper power to the heater resistor. This maintains the HR2 assembly at a constant temperature in spite of environmental temperature variations. Transistor Q14 protects the hybrid in case Q1 fails.

2-191. TRANSCONDUCTANCE AMPLIFIERS

The transconductance amplifiers are the 220 uA/2.2 mA range amplifier and the 22 mA/220 mA range amplifier circuits. The 220 uA and 2.2 mA ranges are provided by the 220 uA/2.2 mA range transconductance amplifier, containing transistors Q4, Q5, and relay K3. With relay K3 reset as shown on schematic, the amplifier is in the 220 uA range. To place the amplifier in the 2.2 mA range, relay K3 is set so emitter resistors R10 and R12 are shunted by R11 and R13 respectively.

The the 22 mA/220 mA range transconductance amplifier contains transistors Q6-Q13 and relay K4. It provides the 22 mA and 220 mA ranges. In the 22 mA range, the transconductance amplifier is composed of Q6-Q9 with K4 in the reset position. In the 220 mA range, the transconductance amplifier is composed of Q6-Q13 with K4 in the set position. In this range, Q10-Q13 are in the Darlington configuration with Q6-Q9 respectively. This provides the additional current gain needed for the 220 mA range.

2-192. SHUNT RESISTORS

A resistor network is used to sense the output current in each of the four current ranges. This network is composed of four four-terminal resistors attached to the heated substrate of HR2. The shunt resistors are 10 kilohm for the 220 uA range, 1 kilohm for the 2.2 mA range, 100Q for the 22 mA range, and the 10 ohm for the 220 mA range. Relays K5-K9 select the INPUT, OUTPUT, and SENSE binding posts for each of the four ranges as Table 2-14 shows:

Table 2-14. Relay Settings for Current Range Selection

RELAY	RANGE			
	220 uA	2.2 mA	22 mA	220 mA
K5	R	S	S	S
K6	R	S	R	R
K7	R	S	R	R
K8	R	R	S	R
K9	R	R	R	S

S=SET R=RESET

2-193. FEEDBACK LOOP

The output current develops a 2.2V full-scale voltage across the appropriate shunt resistors. Buffer amplifiers U2 and U3 isolate the shunt from the remaining feedback circuit. The negative feedback buffer is op amp U2 configured as a voltage follower. The positive feedback buffer is made of U3 configured as a voltage follower.

Both the feedback voltage from U2 and U3, and the input voltage from K1 and Q20-Q23 are applied to the precision dual 10:1 matched voltage divider network Z1. Any voltage difference between the two halves of the network is amplified by the dc amplifier on the heated substrate hybrid HR2. This amplified dc is applied to the complementary drive circuit and in turn to the transconductance amplifiers to complete the feedback loop.

Therefore, with a 22V full scale input and the 10:1 divider, the voltage across the shunt network is forced to 2.2V by the feedback loop. The 2.2V across the shunt is developed by the full-scale output current on any of the four ranges. By programming the input voltage over a 10:1 range, the output current follows with a 10:1 range. By switching the shunt resistors, four 10:1 ranges give a total output range of 20 uA to 220 mA.

2-194. CURRENT OUTPUT SWITCHING

Relays K10-K15 switch the output current for the various modes of operation required by this assembly. When K13 is reset, it switches in a dummy load (R14) to prevent transients during switching, and also for use during diagnostics. Non-latching relay K15 connects the return lines to the output whenever an output is called for. Non-latching relay K14 connects the output signal to latching relay K12. Relay K12 switches the output to the AUX CURRENT OUTPUT binding post while in the reset position, or to the OUTPUT HI binding post while in the set position.

The four ranges of output current can be connected to the B CUR line by relay K11. B CUR is routed to the rear-panel 5725A connector. This allows all current ranges to be available from the binding posts on the 5725A Amplifier if so selected by the operator.

2-195. GENERATION OF THE 2.2A RANGE

To generate the 2.2A range, the Current assembly is set to the 22 mA range with its output directed to the High Voltage/High Current assembly (A15). This connection is made via the IHV line by relay K10 in the set position. The High Voltage/High Current assembly amplifies current by 100 to create the 2.2A range. This high current output is returned to the Current assembly via the B CUR line. Relay K11 in the set position directs it to the output relays, K12-K15, of the Current assembly.

During internal calibration of the 2.2A range, the Current assembly is set to the 22 mA or 2.2 mA range and directed to the High Voltage assembly in the same manner as previously described.

Internal calibration of the 2.2A range and gain of the High Voltage/High Current assembly is discussed further in the theory for the High Voltage assemblies.

2-196. CURRENT GUARD BUFFER

Buffer amplifier U4, configured as a voltage follower, is used to provide a guard voltage equal to the output voltage across the external load. The guard voltage, if used, prevents any output current from being shunted away from the load due to leakage or shunt capacitance in the system cabling.

2-197. COMPLIANCE LIMITER

A compliance limiter circuit consisting of Q24, Q25, and associated components clamps the output to $\pm$11V during an over-compliance condition.

2-198. CURRENT/COMPLIANCE VOLTAGE MONITOR

The current/compliance voltage monitor circuit, which contains CMOS analog switch U5A, U5C, U5D, op amp U6, and associated components, measures the voltage on either side of the current shunts. This allows the 5700A to detect an over-current or over-compliance condition. A logic low on control line FET3 closes U5A to connect the monitor circuit to the input side of the shunt resistor. The measurement at this point is the sum of the output compliance voltage and voltage drop across the shunt, which is proportional to the output current. A logic high on control line FET3 opens U5C, which allows pull-down resistor R36 to close U5D. This connects the monitor circuit to the output side of the shunt resistor, which gives the output compliance voltage.

Op amp U6 and associated components create an absolute value circuit whose output, CUR/COMP MONITOR, is always a positive dc voltage. During operation in the ac current function U6B generates a negative half-wave signal equal to the positive peaks of its input. Resistors R31 and R30 sum this half-wave signal and the input signal at the input of U6A. Capacitor C14 averages the voltage so the output of U6A is a dc voltage which represents the average value of the selected input.

The diagnostic circuit connects CUR/COMP/ MONITOR to the SDL line, on which it is routed to the DAC assembly (A11) to be measured by the adc circuit. The calibrator software computes the difference between the two measurements and divides the result by the shunt value to determine the output current.

2-199. CURRENT ASSEMBLY CALIBRATION

Refer to Figure 2-34 for the following discussion. Internal calibration of the Current assembly is a process of determining the offset and gain constants for each of the four current ranges.

To determine the offset of the 220 mA range, the Current assembly is set to the positive dc 220 mA range with its input from the DAC assembly set to 0V. The output of the Current assembly is routed to the Ohms Main assembly (A10), via INT OUT HI, where it is connected to the previously calibrated 100 ohm resistor.

To get a checkpoint reading, the Current assembly output is removed from the 100 ohm resistor on Ohms (via the output switching relays). The 100 ohm resistor is connected to a differential amplifier on the Ohms Cal assembly (A9). The output of this differential amplifier is connected to RCL, which is routed to the adc circuit on the DAC assembly. The adc circuit measures the voltage, which is the drop across the 100 ohm resistor with no current applied through it. This value is the checkpoint reading and is stored in memory.

The output of the Current assembly is reconnected to the 100 ohm resistor. Next, the DAC assembly, which is the Current input, is adjusted until the adc circuit measures the same reading as the check point.

Gain is determined by connecting the input of the Current assembly to the 13V reference BRF13 and BSRF13 via relay K1. The resulting 130 mA from the Current assembly is routed via INT OUT HI to a previously calibrated 10 ohm resistor on the Ohms Main assembly. The +input of the differential amplifier, located on the Ohms Cal assembly, is connected to one side of this 10 ohm resistor and the -input of the differential amplifier is connected to the output of the DAC assembly. The output of the differential amplifier is connected to the adc circuit in the DAC assembly via the RCL line, and the DAC output is adjusted until a null is achieved. This determines the exact voltage drop across the 10 ohm resistor. The exact gain can now be calculated using this and the previous offset reading.

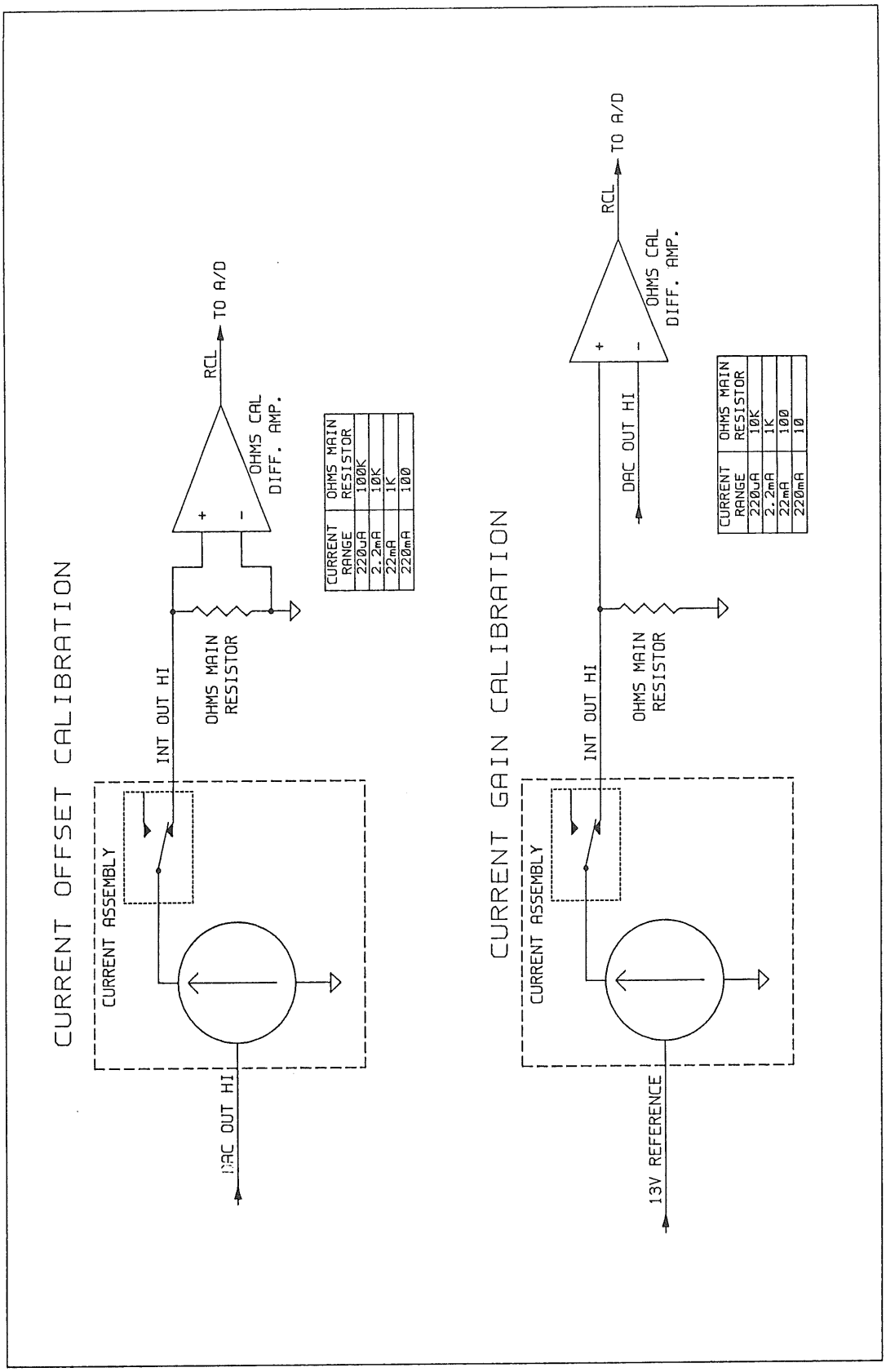

Figure 2-34. Current Assembly Calibration

The current output, now calibrated at dc, is further characterized for its frequency response. The Current assembly is configured to the ac current function with input from the Oscillator Output assembly (A13) set to 20V at a low frequency. The output side of the appropriate shunt resistor is connected to SCOM by relay K17B, and the resulting 2V on the input side of the shunt resistor is connected to the AC CAL line through U22 by relay K17A. The AC CAL signal is routed to the Oscillator Control assembly (A12) where a 400 ohm rms sensor measures the ac voltage on this line. A dc reading of the sensor is taken. It and the Oscillator Output level are stored in memory. The Oscillator Output frequency is then increased and the Oscillator Output level is adjusted, and stored in memory, so the dc reading from the rms sensor is the same as the previous reading. This is repeated at various frequencies up to 10 kHz to characterize the entire frequency response of the ac current output.

2-200. High-Resolution Oscillator Assembly (A7)

The High-Resolution Oscillator supplies a square-wave signal (HI-RES) in the range of 10 Hz to 1.2 MHz with a frequency resolution of 4-1/2 digits. The output signal is routed on the Motherboard P LOCK HI line to the Oscillator Output assembly, where it phase-locks the oscillator.

During calibrator operation using an external phase-lock signal, or during a non-ac operation, the Hi-Res Oscillator is shut off by control line HI RES ON/OFF from the digital control circuit. The hi-res circuitry uses a phase-locked loop circuit containing the reference frequency amplifier/divider, phase detector/divider, loop filter, and vco circuit as outlined on the schematic. A 5-500k divider and output switching circuitry creates the final output frequency. These circuits are described in the following paragraphs.

The Hi-Res Oscillator output is divided into five ranges as shown below:

- Range 1: 10.00 Hz to 119.99 Hz
- Range 2: 0.1200 kHz to 1.1999 kHz
- Range 3: 1.200 kHz to 11.999 kHz
- Range 4: 12.00 kHz to 119.99 kHz
- Range 5: 0.1200 MHz to 1.1999 MHz

Note that the frequency resolution on each range changes from four digits for outputs of 12 to 99 to five digits for outputs of 100 to 119. For example, the output of range 1 has four digits of resolution from 10.00 Hz to 99.99 Hz and five digits resolution from 100.00 Hz to 119.99 Hz. The range 2 output has four digits resolution from 120 Hz to 990 Hz and five digits resolution from 1000.0 Hz to 1.1999 kHz. The resolution break points are similar for the other ranges.

2-201. REFERENCE FREQUENCY AMP/DIVIDER

A 2 MHz reference frequency is generated by the reference frequency amp/divider circuit as outlined on the schematic. This circuit uses the 8 MHz system clock lines CLK and CLK*, generated by the Guard Crossing assembly (A17). This 8 MHz signal is a low-level clock (200 mV p-p) and it is amplified to 5V p-p by comparator U13A. This 5V 8 MHz clock is turned off when the Hi-Res Oscillator is not being used by control line HI-RES ON/OFF from the digital control circuit and nor gate U15D. The 8 MHz clock is then divided to 2 MHz by flip-flops U14A and U14B to generate 2 MHz REF, which is the reference frequency for synthesizer IC U16. It is filtered by R63 and C49 to generate HI-RES CLOCK, which is monitored by the diagnostic circuit.

2-202. PHASE-LOCKED LOOP

The phase-locked loop circuit contains the phase detector/dividers, loop filter, and vco (voltage-controlled oscillator) circuits as outlined on the schematic.

The phase det/dividers circuit contains synthesizer IC U16. This IC contains two programmable divide-by-n counters and a phase detector. The divide-by-n counters are controlled by inputs from the control bus, which are latched into internal latches on the IC. Information on the control bus is entered and latched into U16 by NOR gate U15A and control lines CS7* and WR*. The first divide-by-n counter is programmed to divide 2 MHz REF by 2000 to give 1 kHz, which is applied to one input of the internal phase detector. The other divide-by-n counter is used to divide the feedback frequency at pin 3, which is generated by the VCO circuit, by 6,010 to 12,000 in one-digit steps, and then apply it to the second input of the phase detector. The loop is locked when the two inputs to the phase detector are the same frequency and phase.

With the 1 kHz reference frequency and the feedback divider programmed between 6,010 and 12,000, the input frequency at pin 3 of U16 must be between 6.010 MHz and 12.000 MHz (1 kHz x 6010 = 6.010 MHz and 1 kHz x 12000 = 12.000 MHz).

Phase detector (U16) outputs ("0V" on pin 14 and "0R" on pin 15) are used by the loop filter circuit, which controls the VCO circuit.
If the divided feedback frequency is greater than the 1 kHz reference frequency, or if the phase of the divided feedback frequency is leading the output, 0V pulses low and output 0R remains high. If the divided feedback frequency is less than the 1 kHz reference frequency, or if the phase of the divided feedback frequency is lagging the output, then 0R pulses low and output 0V remains high. When the feedback frequency and the 1 kHz frequency are the same and in phase, the outputs 0V and 0R both remain high except for a short period when both pulse low in phase. This condition occurs when the loop is locked.

Outputs from the phase detector (0V and 0R) are connected to the loop filter circuit which contains the two op amps in U20. U20A and U20B amplify and filter, respectively, any phase difference and apply it to varactor diode CR9 in the vco circuit.

The vco circuit contains varactor diode CR9 and a vco IC U19. The vco frequency is controlled by CR9, which gets its bias voltage from amplifier U20. This circuit is designed to always operate over a 2:1 range from 6 MHz-12 MHz. To lock the loop, amplifier U20 changes the bias on varactor diode CR9 until the divided vco frequency has the same frequency and phase as the 1 kHz reference frequency at the input to the phase detector in U16. Once the loop is locked, the output of the phase-locked loop circuit is between 6 and 12 MHz. This output frequency is connected to the 5-500k divider circuit for further division.

Supply voltage is applied to vco U19 whenever the Hi-Res function is used by the circuitry containing analog CMOS switch U18A, transistor Q15, and zener diode VR3. VCO U19 is energized when control line HI-RES ON/OFF goes low to close U18A, which turns on transistor Q15, connecting zener diode VR3 to the -17LH power supply.

R53 and R54 divide the bias voltage input of the vco circuit to generate the HI-RES LOOP line, which is monitored by the diagnostic circuit.

2-203. 5-500K OUTPUT DIVIDER

The 5-500k output divider circuit contains a synthesizer IC U17 which has a reference (R) divider and a divide by N counter. These dividers are controlled by inputs from the CONTROL BUS which are latched into internal latches on the IC. The information on the CONTROL BUS is entered and latched into U17 by nor gate U15B and Control lines CS13* and WR*. With the phase-locked loop output frequency locked at any frequency between 6 MHz and 12 MHz, divider U17 is programmed to divide by some value between 5 and 500,000 as required to give the correct output frequency. The 6 MHz - 12 MHz input from the phase-locked loop circuit is divided by the reference divider to generate the 24 kHz-2.4 MHz frequency range at pin 18. This divided reference frequency is connected to pin 3 which is the input of the divide by N counter. The divide by N counter does further division to generate the 20 Hz-24 kHz frequency range at pin 15. As an example, an output of 6.7 kHz is in range 3 with the loop locked at 6.7 MHz [the internal divider in U16 was programmed to divide by 6,700 (6,700 x 1 kHz = 6.700 MHz)] and the two dividers in U17 are programmed for a total division of 500 (6.7 MHz/500 = 13.4 kHz). This 13.4 kHz signal is divided in half by the output switching circuit to generate the 6.7 kHz output.

2-204. HI-RES OUTPUT SWITCHING

The output switching circuit contains three analog CMOS switches in U18, and flip-flops in U21. Flip-flop U21A divides the reference divider output of U17 by two to create the 12kHz-1.2 MHz range. Flop-flop U21B divides the divide-by-N counter output of U17 by two to create the 10 Hz-12 kHz range. Control line HI-RES RANGE and NOR gate U15C control the analog CMOS switches U18B and U18C. These switches select the 12 kHz-1.2 MHz or the 10 Hz-12 kHz frequency range, respectively, from the flip-flops. Flip-flop U21A divides this frequency by two. Control line HI-RES ON/OFF and switch U18D connect this output square-wave signal to the P LOCK HI line when the variable phase output function is activated by the operator.

Table 2-15 shows how the dividers are set, the total division of the vco frequency, and the vco frequency. To determine the exact vco frequency, multiply the calibrator output frequency by the number in the total division bracket. For example, the output frequency is set to 42 kHz and the vco frequency is 42k x 200 = 8.4 MHz. Note that the total division includes division by two by U21 in the output switching circuit.

Table 2-15. Divider Settings and VCO Frequencies

CALIBRATOR OUTPUT FREQUENCY @ TP16	U17 R DIVIDER SETTING	U17 N DIVIDER SETTING	TOTAL DIVISION OF VCO @TP13	VCO FREQUENCY @TP13
10 Hz-12 Hz	500	1000	1M	10 MHz-12 MHz
13 Hz-15 Hz	400	1000	800k	10.4 MHz-12 MHz
16 Hz-30 Hz	200	1000	400k	6.4 MHz-12 MHz
31 Hz-60 Hz	100	1000	200k	6.2 MHz-12 MHz
61 Hz-120 Hz	50	1000	100k	6.1 MHz-12 MHz
130 Hz-150 Hz	400	100	80k	10.4 MHz-12 MHz
160 Hz-300 Hz	200	100	40k	6.4 MHz-12 MHz
310 Hz-600 Hz	100	100	20k	6.2 MHz-12 MHz
610 Hz-1.2 kHz	50	100	10k	6.1 MHz-12 MHz
1.3 kHz-1.5 kHz	400	10	8k	10.4 MHz-12 MHz
1.6 kHz-3.0 kHz	200	10	4k	6.4 MHz-12 MHz
3.1 kHz-6.0 kHz	100	10	2k	6.2 MHz-12 MHz
6.1 kHz-12 kHz	50	10	1k	6.1 MHz-12 MHz
13 kHz-15 kHz	400	0	800	10.4 MHz-12 MHz
16 kHz-30 kHz	200	0	400	6.4 MHz-12 MHz
31 kHz-60 kHz	100	0	200	6.2 MHz-12 MHz
61 kHz-120 kHz	50	0	100	6.1 MHz-12 MHz
130 kHz-150 kHz	40	0	80	10.4 MHz-12 MHz
160 kHz-300 kHz	20	0	40	6.4 MHz-12 MHz
310 kHz-600 kHz	10	0	20	6.2 MHz-12 MHz
610 kHz-1.2 MHz	5	0	10	6.1 MHz-12 MHz

2-205. Rear Panel Assembly (A21)

Functional circuitry on the Rear Panel assembly includes a relay control circuit, phase lock in/variable phase out I/O circuit, address mapping, clock regeneration circuit, IEEE-488 interface, RS-232-C interface, interfaces for the 5205A, 5215A, and 5220A amplifiers, and a 5725A Amplifier interface. Three amplifiers can be physically connected to the 5700A: 5725A, 5220A with 5205A, or 5220A with 5215A). Only one can be used at a time. Depending on the amplifier's mode of operation, the output of the 5700A is either an ac or a dc voltage. The following theory of operation describes each of these circuits.

2-206. REAR PANEL POWER SUPPLIES

Power supplies are divided into guarded and unguarded. Unguarded supplies +5V LOGIC, +12V, and -12V are referenced to +5V LOGIC COMMON and are generated on the Digital Power Supply assembly (A19). Guarded supplies +5LH and -5LH are referenced to LH COM, and the supply +5RLH is referenced to RLH COM. These supplies are generated on the Regulator/Guard Crossing assembly (A17). Some ICs on the A17 assembly do not have power and ground pins shown on the schematic. This information is included in the table on page 1 of the Rear Panel schematic.

2-207. REAR PANEL ADDRESS MAPPING

The rear panel decodes address lines from the bus connected to the main CPU through connector P91. Decoding is accomplished with a C22V10 PLD (U8) with the following chip selects:

- RPDUARTCS* D00000-D0001F
- RPIEEECS* D00020-D0002F
- Y52XXRD* D00030-D00031
- Y5205WR* D00032-D00033
- Y5220WR* D00034-D00035

2-208. CLOCK REGENERATION CIRCUIT

In order to minimize EMI (electro-magnetic interference) inside the 5700A chassis, the rear panel accepts a low-level (~200 mV p-p sinewave) 3.68 MHz clock from the CPU assembly and conditions it to proper TTL clock levels.

This is done by a differential amplifier, U18, which amplifies the incoming signals 3.6864MHZCLK and 3.6864MHZCLK*. The output of U18 is a TTL level 3.68 MHz clock called RP3.68MHZ that is buffered by PLD U8 creating RPCLK for use by DUART (dual universal asynchronous receiver/transmitter) U5, and IEEE interface IC U2.

2-209. IEEE-488 (GPIB) INTERFACE

The IEEE-488 (GPIB) interface circuit provides the interface between the IEEE-488 connector (J1) and the calibrator processor on the CPU (A20) assembly. The circuitry uses a TMS9914 (U2) General Purpose Interface Bus (GPIB) adapter to meet the requirements for talker/listener operation on the IEEE-488 bus. This circuit translates asynchronous 8 bit data and control information, under control of an external controller, and converts this information to an acceptable format for the CPU. responds.

The TMS9914 has internal circuitry which handshakes in the proper GPIB protocol and stores data in an internal buffer. This IC also has the capability of interrupting the CPU. The CPU can then handle the interrupt through its own handler routine. The data lines between U2 and J1 are buffered by a 75160A (U3) data buffer, and the command lines are buffered by a 75162A (U4) command buffer.

J1 is a standard IEEE-488 connector. The shell of this connector is tied to chassis ground for EMI/RFI shielding.

2-210. RS-232C INTERFACE

The RS-232C interface circuit uses a 68C681 DUART (U5), a 1488 line driver (U6), and a 1489 line receiver (U7).

The DUART does the parallel to serial data conversion and provides two channels of serial RS-232C communication.

The first channel is available to RS-232C connector J2 to meet serial interface needs between the 5700A and the external world. The transmit line (*TXDA) is driven by U6D to TX of J2, pin 2. The receive line RX goes from J2, pin 3 through receiver U7C to the receive line *RXDA of the DUART.

The second channel is connected to the 5725A Amplifier interconnect connector (J7) to provide the 5725A digital control interface to the CPU assembly. Transmit line *TXDB is driven by U6B to B-SCT of J7, pin 18. Receive line B-SCR from J7, pin 17 goes through receiver U7B to the receive line *RXDB of the DUART. These lines are also connected to J10, pins 2 and 3, for internal software testing.

The DUART (U5) also has six input lines, four of which are used to monitor CTSA*, B-CINT*, CAL SWA*, and CAL SWB*. The CTS (clear to send) line from J2, pin 5 goes through receiver U7A becoming CTSA*. Line CAL SWA* comes from the rear panel CALIBRATION switch.

The B-CINT* input (5725A cable interlock) is a logic signal used to let the 5700A know that the interface cable to the 5725A Amplifier is connected and the 5725A is energized.

The DUART (U5) generates four output lines. The first, RTSA*, is driven by U6C to the RTS (ready to send) pin 4 of J2. The remaining three are used in the auxiliary amplifier interface logic circuit.

5220EN* is the output enable for octal latch U10. 5220ADIR* is the output enable for buffer U11. 5205EN* is the output enable for octal latch U9.

2-211. AUXILIARY AMPLIFIER INTERFACE

The Auxiliary Amplifier interface connects the 5700A to a 5205A or 5215A Precision Power Amplifier or the 5220A Transconductance Amplifier. The connection to the 5205A or 5215A is closed loop while the connection to the 5220A is open loop.

Three amplifiers can be physically connected to the 5700A: 5725A, 5220A with 5205A, or 5220A with 5215A). Only one can be used at a time. Depending on the amplifier's mode of operation, the output of the 5700A is either an ac or a dc voltage.

Relays on the Switch Matrix assembly connect OUTPUT HI signal to B IN, SENSE HI to B FB, and INT SENSE LO to B SNSLO, the driving signals for the 5205A, 5215A, and 5220A Auxiliary Amplifiers. These signals are routed to the rear panel from the Motherboard through connector J8 and an external cable. The 5205A and 5220A configurations are described later.

2-212. 5205A INTERFACE

The 5205A is a power amplifier with gain of -100 and a bandwidth of dc to 100 kHz. When the 5205A function is selected via the calibrator keyboard, the output of the calibrator is routed to connector J3 (pins 1, 9, 2, and 10) on the rear panel, which is closed-loop interfaced to the 5205A.

NOTE

Model 5215A is also compatible with the 5205A connector. The 5215A provides the same ac functions of the 5205A, but not the dc functions.

During this mode of operation, the calibrator is configured to the ac 11V range. Relay K1 is energized and relay K3 is set connecting B IN to 5205A INPUT HI, B FB to 5205A SENSE HI2, PA COM to 5205A INPUT LO, and B SNSLO to 5205A SENSE LO. Relay K4 is energized, connecting 5205A SENSE LO to 5205A SENSE L and 5205A SENSE HI to buffer amplifier U13. The output of buffer U13 is connected to K3 pin 9.

Relay K11 connects the 5205A voltage guard signal V-GRD2 to the 5700A voltage guard V GUARD.

In addition to the ac signal, the 5700A/5205A interface is composed of four control lines and logic power. +5V LOGIC provides logic power for the opto-isolators in the 5205A and +5V LOGIC COMMON provides the return. The rear panel data bus, 5205AEN*, and Y5205WR* are used by latches in U9 to create control lines CONTROL and OPERATE to connector J3, pins 14 and 15, respectively.

CONTROL, when asserted low, places the 5205A in the "5200 Control" mode and sets up the 5205A for commands. OPERATE, when asserted low, commands the 5205A to go into operate.

The 5205A generates STATUS and TRIP signals that are connected to buffer U12 where they are monitored, via the DATA BUS and control line Y52XXRD*, by the 5700A.

STATUS, when asserted low, indicates that the 5205A is in the operate mode. TRIP, when asserted low, tells the 5700A that the 5205A has experienced a fault or overload and is no longer in the OPERATE mode.

2-213. 5220A INTERFACE

The 5220A is a transconductance amplifier with a gain of one. Its output range is from 0 to 20A, thus its input voltage is from 0 to 20V.

When the 5220A is selected via the front panel, the output of the 5700A is routed to connector J4 on the rear panel, which is the interface to the 5220A.

The 5220A is designed to be operated with the 5700A in an open loop configuration. In this mode of operation, relays K2 and K3 are reset and relays K1 and K5 are energized.

This configuration ties B IN to B FB and connects them to 5220A INPUT HI. B SNSLO and PACOM are tied together and connected to 5220A INPUT LO. In this mode, the 5700A senses at the rear panel.

In addition to 5220A INPUT HI and 5220A INPUT LO, the interface between the 5700A and 5220A is composed of ten control lines.

Lines BD0-BD3 form a four-bit bidirectional data bus. Data from the 5220A is buffered and read on the DATA BUS by buffer U12 and control line Y52XXRD*. Data to the 5220A is generated from the DATA BUS by latches in U10 and control lines 5220AEN* and Y5220WR*. This data is buffered by U11 and controlled by 5220ADIR* before connecting to J4, pins 4, 12, 3, and 11.

Lines BC0, BC2, BC3, and BC6 form a four bit address bus. This address is generated from the DATA BUS by latches in U10 and control lines 5220AEN* and Y5220WR*.

The 5220A generates status lines ACK* and WR*, which are connected to buffer U12 where they are monitored, via the DATA BUS and control line Y52XXRD*, by the 5700A. ACK* is asserted low when a valid address is accepted by the 5220A. WR* is asserted low when its OK to read the 5220A status.

2-214. 5725A INTERFACE

The 5700A is designed to work in close connection the 5725A Amplifier. The function of the rear panel in this system is to provide relay switching for the 5725A signals. The 5725A performs the same functions as both the 5205A and 5220A amplifiers. All voltage outputs from the 5725A are routed back to the binding posts on the 5700A. All current outputs from the 5725A are sourced at the 5725A OUTPUT binding posts. You can configure the 5700A to also source all its current outputs through the 5725A OUTPUT binding posts for convenience.

Connector J8 and Cable 4406 interface all the 5700A I/O signals between the motherboard and the rear panel. Connector J7 interfaces the 5700A to the 5725A Amplifier. The interface between these two connectors is accomplished through relays K1, K2, and K6-K9. Relays K6-K9 break all the I/O lines except B-SENSE HI, B-OUT HI, V-GUARD, and B-IGRD, and connect them all to V-GUARD when the 5725A is not in use.

During 5725A operation, relays K1, K2, K6, and K7 switch the 5700A analog signals B IN, B FB, B SNSLO, and PACOM to lines BOOST IN, B-FEEDBACK, B-SENSE LO, and BPA COM on connector J7.

High voltage output of the 5725A (B-OUT HI and B-SENSE HI) is connected to the 5700A Motherboard via cable 4406 where it can be switched to the 5700A binding posts by relays on the Motherboard.

Relays K8 and K9 connect the 5725A current function lines I-RET, and B-CUR on connector J8 to B-IRTN, and B-CURRENT, on connector J7 when the 5725A is outputting 5700A current (<=2.2A). Line B-RCL is used during 5725A calibration. Line B-RCL on J7 is connected to J8 through relay K6. Line B-RCL is routed via the motherboard to the Current assembly (A7) where it is switched to the calibrator RCL line by a relay.

2-215. PHASE LOCK IN/VARIABLE PHASE OUT

The Oscillator Output assembly (A13) can be phase locked to an external signal connected to the PHASE LOCK IN BNC connector J6. Relay K10B connects the shell of this BNC connecter to chassis ground through protection resistor R19 when the 5700A is on internal operation, or to P LOCK LO when the 5700A is phase locked to the external signal coming in on J6.

This incoming signal is called PHLK IN on the schematic. Relay K10A switches an external phase-lock signal from J6 to the input of Q1 and Q2. FETs Q1 and Q2 provide current limiting for PHLK IN. Signal P LOCK is routed to connector J8 where it is connected to the Oscillator Output assembly via the Motherboard.

Components CR1, CR2, VR1, VR2, R4, and R5 provide amplitude protection for the phase lock circuitry on the Oscillator Output assembly by limiting the amplitude of P LOCK.

The Variable Phase Out BNC connector (J5) is connected to P SHIFT and its shell is connected to PA COM by energizing relay K12. Signal P SHIFT is a fixed-amplitude variable phase signal generated by the Oscillator Output assembly (A13). Refer to the Oscillator Output assembly theory of operation for a detailed description on the generation of P SHIFT. Resistor R18 serves as overcurrent protection for the BNC shell connection on J5.

2-216. REAR PANEL RELAY CONTROL

The relays on the Rear Panel assembly are used as the interfaces for the 5205A, 5215A, 5220A, or 5725A amplifiers, or for switching the PHASE LOCK IN and VARIABLE PHASE OUT signals.

The relay switching circuitry is under control of the guarded digital bus via connector J8. This guarded digital bus is generated on the Regulator/Guard Crossing assembly (A17).

The relay control circuitry is located on page 5 of the Rear Panel schematic. This circuit uses an 82C55 programmable peripheral interface (U14) and two relay drivers (U16 and U17) to control the 12 relays on this assembly and one relay (K12) on the analog motherboard. The 82C55 (U14), which is under control of the guarded digital bus via connected J8, has three ports generating 24 outputs.

Port A (PA0-PA7) provides the input lines for relay driver U16.

Port B (PB0-PB7) provides the input lines for relay driver U17.

PC0-PC2 of port C provides the CLEAR, STROBE, and OUTPUTENABLE lines for these relay drivers.

Relay Driver U16 controls two latching relays (K2 and K3) and four non-latching relays (K1, K4, K5, and K7). Relay driver U17 controls one latching relay (K6) and five non latching relays (K8-K12). Relay driver U17 also creates control line RLY12* (pin 13) which controls relay K12 on the Analog Motherboard assembly (A3).

2-217. REAR PANEL CPU INTERFACE

The rear panel is interfaced to the CPU assembly (A20) via connector J8 on the rear panel. The CPU has:

- o Five address lines (RPA1-RPA5) which comprise the ADDRESS BUS
- o Seven control lines which comprise the CONTROL BUS
- o A low-level 3.6864 MHz clock (CLOCK, CLOCK*)
- o Eight data lines RPD0-RPD7

Interfacing between the Rear Panel data bus (D100-D107) and the CPU data bus (RPD0-RPD7) is done with a bus transceiver U1.

2-218. Wideband AC Module (Option -03)

The Option -03 Wideband AC Module consists of the Wideband Oscillator assembly (A6) and the Wideband Output assembly (A5).

The wideband module operates in conjunction with the Oscillator Output assembly (A13), and provides calibrated output voltages in the range of 300 uV to 3.5V rms at frequencies of 10 Hz to 30 MHz, into a 50 ohm load resistance.

The output impedance of the assembly is 50 ohms. It is designed to drive 50 ohm loads. The output of this option connects to the Type "N" wideband connector on the 5700A front panel.

The theory of operation covers the Wideband Oscillator assembly (A6) and the Wideband Output assembly (A5).

2-219. Wideband Oscillator (A6) (Option -03)

The Wideband Oscillator assembly generates sine wave outputs in the range of 1.1 MHz to 30 MHz, (with two-digit resolution) at a nominal full scale output of 700 mV rms.

The frequency source is a ECL-level square wave with a frequency range of 1.1 MHz to 30 MHz, created in the phase-locked loop and divider circuit. The amplitude of this square wave is controlled by the WB AMPLITUDE CONTROL line, which is a DC signal from the Wideband Output assembly, and the circuitry contained in the amplitude control amplifier.

The resulting variable frequency and amplitude square wave is converted to sine wave by one of the five-pole filters. This variable frequency and amplitude sine wave is routed to the Wideband Output assembly via connector J1 and a 75 ohm coaxial cable.

2-220. WIDEBAND OSCILLATOR POWER SUPPLIES

The +5LH, -5LH, +17S, and -17S supplies are generated on the Regulator assembly and routed to this assembly via the motherboard.

The -5LH supply is buffered by L12 and C49, creating the -5F supply.

The +5LH supply is divided by R66 and R67 to create the +2.5 supply which is the reference voltage for comparators in U7, U10, and U11.

Zener diode VR1 and resistor R39 create the +12 supply from the +17S supply. Zener diodes VR4 and VR5, resistors R40 and R41, and diodes CR8 and CR9 create the -12, -11, and -9.5 supplies from the -17S supply. These are used throughout the Wideband Oscillator assembly.

2-221. WIDEBAND OSCILLATOR DIGITAL CONTROL

The digital control circuit on the Wideband Output assembly creates control lines WB MUXA, WB MUXB, WB MUXC, WB FBS, and WB ON/OFF*. These lines are routed to the Wideband Oscillator via the Motherboard.

Control lines WB MUXA, WB MUXB, and WB MUXC are inverted and level-shifted by comparators in U7 to create the control lines for multiplexer U6. They are also used by the filter-select circuitry.

In this circuit, WB MUXA, WB MUXB, and WB MUXC are decoded by U8 to generate four control lines, These are inverted and level-shifted by comparators in U10 and U11. The output of these comparators create 16-32MHz FILTER, 8-16MHz FILTER, 4-8MHz FILTER, 2-4MHz FILTER, 1-2MHz FILTER, and Q8/Q9 SELECT, which are used in the filter switch drive circuitry.

Control line WB FBS is inverted and level-shifted by a comparator in U10. This creates FILTER BAND SWITCH, which is also used in the filter selection circuitry. Control line WB ON/OFF* shuts down the 8 MHz clock generator and vco when the wideband module is not in use.

2-222. PHASE-LOCKED LOOP AND DIVIDER CIRCUIT

The phase-locked loop and divider circuit uses 8 MHz clock generator U15, synthesizer IC U1, amplifier U2, vco U3, and dividers in U4 and U5 to generate an ECL-level square wave from 1.1 MHz to 30 MHz.

The 8 MHz clock generator creates the 8 MHz reference frequency from the 8 MHz system clock lines CLK and CLK*, which is a low level (~200 mV p-p) 8 MHz sine wave generated on the Regulator/Guard Crossing (A17) assembly. Comparator U15 converts this sine wave into a TTL-level 8 MHz square wave to provide the reference frequency for synthesizer IC U1.

Synthesizer IC U1 contains two programmable divide-by-N counters and a phase detector. The divide-by-N counters are controlled by inputs from the guarded digital bus, which are latched into internal latches on the IC. NOR gates in U14 are used to gate the chip select (CS14) and write (WR) lines from the digital bus. This forms the strobe pulse necessary to latch the frequency data into the synthesizer IC.

The first divide-by-N counter is programmed to divide the 8 MHz reference by 160 to give 50 kHz. This, in turn, is applied to one input of the internal phase detector. The other divide-by-N counter is used to divide the feedback frequency at pin 3 by 80 to 160 in 1 digit steps, and then apply it to the second input of the phase detector. The loop is locked when the two inputs to the phase detector are the same frequency and phase.

With a 50 kHz reference frequency and the feedback divider programmed between 80 and 160, the input frequency at pin 3 (feedback frequency) must be between 4 MHz and 8 MHz. (50 kHz X 80 = 4 MHz and 50 kHz X 160 = 8 MHz.)

The frequency into U1 pin 3 is generated by the vco (U3) and dividers in U4 and U5. A flip flop in U4 divides the vco frequency by 2 and the binary counter in U5 further divides by 4 to give a total division of 8.

If the input to U1 pin 3 is between 4 MHz and 8 MHz, then the vco frequency before the divide-by-8 must be 32 MHz to 64 MHz.

The phase detector outputs ("OV" on pin 14 and "OR" on pin 15) of the synthesizer U1 are used by the amplifier (U2) to control the vco (U3). If the divider feedback frequency is greater than the 50 kHz reference frequency, or if the phase of the divider feedback frequency leads the output, then OV pulses low while output OR remains high.

If the divider feedback frequency is less than the 50 kHz reference frequency, of if the phase of the divider feedback frequency lags the output, then OR pulses low and the output OV remains high.

When the feedback frequency and the 50 kHz reference frequency are the same and in phase, the output OV and OR both remain high except for a small period when both pulse low in phase. This condition occurs when the loop is locked.

The vco frequency is controlled by varactor diodes, CR1 + CR2, which get their bias voltage from amplifier U2. Amplifier U2, which gets its input from the phase detector outputs (OV and OR) of U1, changes the bias on varactor diodes CR1 and CR2 until the divided vco frequency has the same frequency and phase as the 50 kHz reference frequency at the input to the phase detector in U1.

Any phase difference is amplified by U2 and filtered by L6, C53, and C17 to bring the loop into lock.

The vco is shut off whenever the Wideband AC module is not in use. To shut off the vco control line WB ON/OFF* is set low and inverted by a comparator in U7 which then turns on Q3.

With transistor Q3 on, transistor Q2 is turned off which removes the -5V supply from the vco to stop the oscillation.

With the vco frequency between 32 and 64 MHz, U4 divides by 2 to give a symmetrical square wave of 16 to 32 MHz, which is the top octave range required for this assembly. Further division by two (pin 15), four (pin 13), eight (pin 4), and sixteen (pin 2) by binary counter U5 gives the other ranges required of 8 to 16 MHz, 4 to 8 MHz, 2 to 4 MHz, and 1 to 2 MHz.

Multiplexer U6, under software control via control lines WB MUXA, WB MUXB, WB MUXC, and comparators in U7, can be programmed to select which of the 5 ranges is needed to give the output frequencies of 1 to 32 MHz.

2-223. AMPLITUDE CONTROL AMPLIFIER AND X10 WIDEBAND AMPLIFIER

The square wave output generated by the phase-locked loop and divider circuit (1-32MHZ OUTPUT) is connected to the amplitude control amplifier circuit.

This circuit uses transistor array U9 to form a differential gain-control amplifier. Gain of the amplifier is controlled by the dc signal AMPLITUDE CONTROL, connected to U9 pin 10.

DC signal AMPLITUDE CONTROL is generated by the thermal rms sensor amplitude control circuitry on the Wideband Output assembly (A5) and is discussed in that section.

The gain controlled square wave output of U9 (pin 6) is further amplified by the x10 wideband amplifier circuit. Transistors Q4, Q5, and Q6 are configured as an amplifier with a gain of ten. This amplifier raises the gain-controlled square wave to the level needed to drive output filters. The output of this circuit is a square wave with an amplitude between 1.4V p-p to 6.0V p-p.

2-224. WIDEBAND OSCILLATOR FILTERS

Each of the five octave frequency ranges has a 5-pole filter to change the square wave input to a sine wave output with a nominal full scale output of 700 mV rms.

The filter switch drive circuit uses control lines from the filter select circuit (that contains transistor arrays U12 and U13) to provide the drive to properly turn on and off FETs and transistors in each of the filters.

The filter inputs and outputs are switched on by FETs and the filter output is applied to output driver Q7. The corresponding filter is selected automatically as each octave range is selected. The operation of the 16-32 MHz filter is described. The other four filters operate in a similar fashion.

The input FET Q101 is turned on via control line 16-32MHZ FILTER and a transistor in U13. This applies the signal FILTER INPUT from the X10 wideband amplifier to follower Q102. Transistor Q102 drives the filter that contains L102, L103, L104, C109 and C112. FET Q105 is turned on, in the same manner as FET Q101, to connect the sine wave output of this filter to FILTER OUTPUT. This is applied to output driver transistor Q7.

To obtain the required amount of filtering over the entire octave range, additional capacitors C110 and C111 are switched into the filter by PIN diodes CR102 and CR103 when operating below 70% of the full range (22 MHz in this case).

Diodes CR102 and CR103 are activated by turning on Q103 and Q104, respectively. Transistors Q103 and Q104 are turned on via control line Filter Band Switch and a transistor in U12.

Two additional FETs, Q8 and Q9, are used to isolate the 16-32 MHz filter and the 8-16 MHz filter, from the three other lower frequency filters, whenever the two high frequency filters are used. The isolation provided by FETs Q8 and Q9 eliminates both the input and output load capacity and circuit board capacity of the three lower frequency filters, so that follower Q6 can drive the high frequency filter input without distortion of the waveform. This also eliminates loading the filter outputs, which changes the filter frequency response.

2-225. Wideband Output Assembly (A5) (Wideband AC Module, Option -03)

The Wideband Output assembly (A5) takes the sine wave signal from either the Wideband Oscillator assembly (A6) or the Oscillator Output assembly (A13), and amplifies it to a power level that drives 3.5V into a 50 ohm load at the output.

The Oscillator Output assembly generates the sine wave signal from 10 Hz to 1.1 MHz, and the Wideband Oscillator assembly generates the sine wave signal from 1.2 MHz to 30 MHz. This provides a total frequency range of 10 Hz to 30 MHz.

The Wideband Output assembly contains a power amplifier circuit that increases the gain and/or power level of the input signal. Also contained on the assembly are a thermal rms sensor circuit necessary for amplitude control, the 50 ohm attenuators needed to reduce the output level through all of the amplitude ranges, an overload control circuit, and digital control circuitry.

Figure 2-35 is a simplified schematic for the Wideband Output assembly.

The Wideband Output assembly has three basic operating ranges:

1. The first range is for Wideband AC module operation at frequencies between 10 Hz and 11.9 kHz. In this frequency range, relay K1A is in the set position so the input signal is from the Oscillator Output assembly with its amplitude is controlled by the Oscillator Control assembly (A12).

   The amplitude control circuit on the Wideband Output assembly is only used for overload protection. This is done by control line PB0 which goes high and turns on FETs Q2 and Q3 via comparator U4B.

   These FETs shunt the rms sensor's input and output to ground through 200 ohm resistors (R2 and R18) to reduce the sensitivity of the sensor.

2. The second range is for operation at frequencies between 12 kHz and 1.1 MHz. In this mode the input signal is also from the Oscillator Output assembly, but the amplitude is controlled by the amplitude control circuit on the Wideband Output assembly.

   Relay K10 is in the set position to connect the output of the rms sensor and amplitude control circuit to the RCL line where it is measured by the adc circuit on the DAC assembly.

   The DAC assembly operates in conjunction with the Oscillator Control assembly to adjust the amplitude of the Oscillator Output signal.

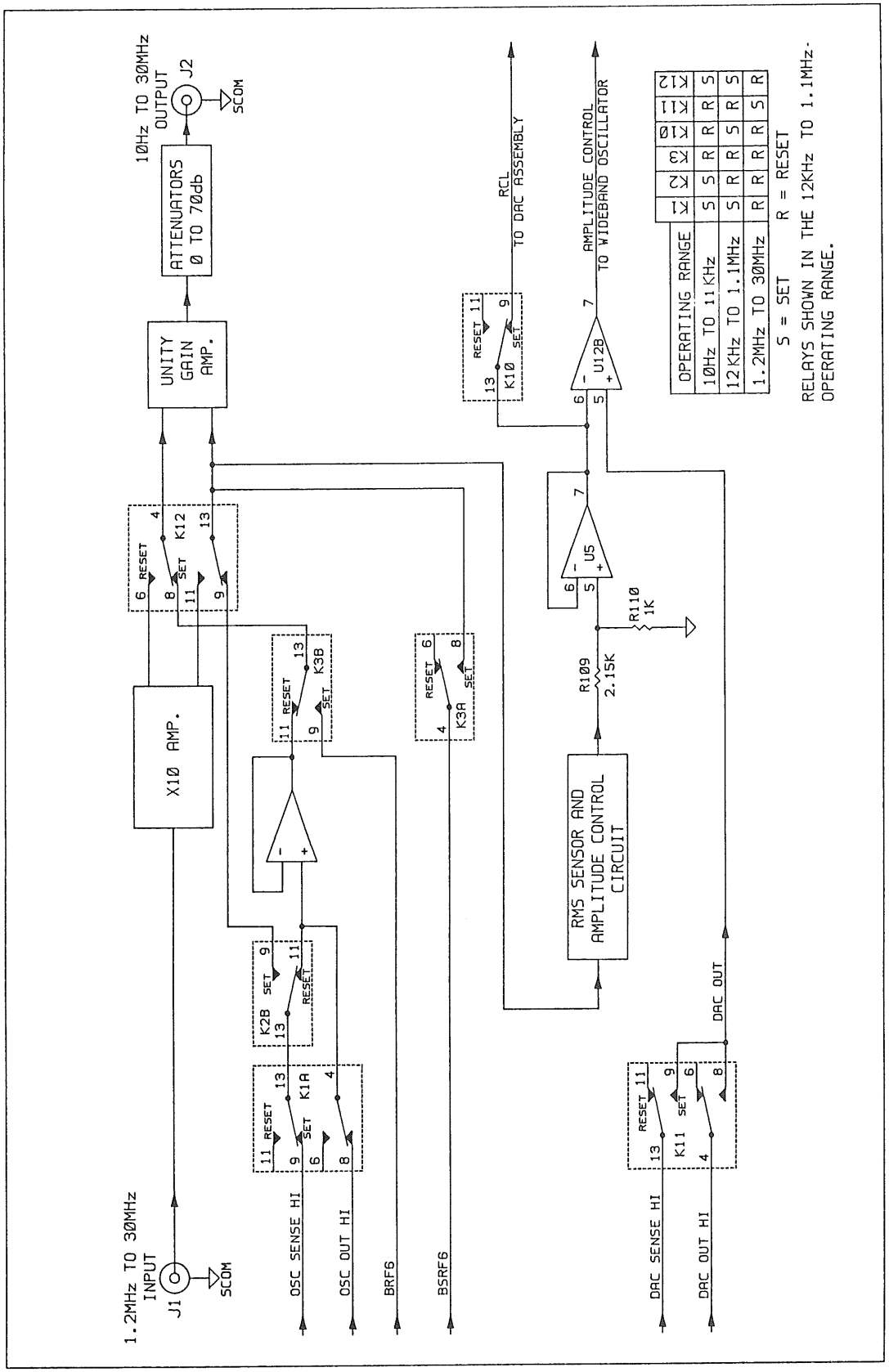

Figure 2-35. Wideband Output Assembly Simplified Schematic

3. The third range is for operation at frequencies between 1.2 MHz and 30 MHz. In this mode the input signal is from the Wideband Oscillator assembly via connector J1. Its amplitude is controlled by the amplitude control circuit on the Wideband Output assembly.

   In this mode the output of the DAC assembly, DAC OUT HI and DAC SENSE HI, are connected to DAC OUT by relay K11 in the set position. Op amp U12B compares DAC OUT to the output of the rms sensor and amplitude control circuit. Any difference between these two signals is amplified and routed to the Wideband Oscillator assembly via the AMPLITUDE CONTROL line.

   The Wideband Oscillator uses the Amplitude Control line to adjust its AC amplitude until the sensor output is equal to the DAC voltage.

2-226. WIDEBAND OUTPUT POWER AMPLIFIER CIRCUIT

The power amplifier circuit, as outlined on page 1 of the Wideband Output assembly schematic, contains all the circuitry shown on page 2 of the schematic. This circuitry consists of the x10 amplifier, the unity-gain amplifier, and the 10 Hz to 1.1 MHz buffer circuit as outlined on the schematic.

The x10 amplifier circuit is used only during operation in the 1.2 MHz to 30 MHz range. The 1.2 MHz to 30 MHz sine wave input comes from the Wideband Oscillator assembly via a coaxial cable and connector J1. This input signal has a nominal full-scale amplitude of 700 mV rms.

The x10 amplifier circuit uses transistors Q4, Q5, Q6, Q7, Q8, Q9, and Q10 to amplify this signal by a factor of 10. Amplifier U11A keeps the DC offset on the output to near zero. The output of the X10 amplifier is applied to the unity gain amplifier by relay K12 in the reset position. The output impedance of the unity gain amplifier is 50 ohms, therefore the x10 amplifier must produce 7.0V rms to give 3.5V rms into the 50 ohm load.

The 10 Hz to 1.1 MHz buffer circuit is used during operation in the 10 Hz to 12 kHz range or the 13 kHz to 1.1 MHz range. In this mode, the input signal comes from the Oscillator Output assembly. This input signal is buffered by Q17 and applied to relay K12. Amplifier U11B keeps the DC offset on the output near zero for the 10 Hz to 1.1 MHz range.

The unity-gain amplifier is connected to either the output of the x10 amplifier or the output of the 10 Hz to 1.1 MHz Buffer by relay K12. The unity gain amplifier uses transistors Q11-Q16 and associated components. This circuit increases the power to a level that drives 3.5V rms into a 50 ohm load. The four 1/2 watt resistors in parallel (R96, R97, R98, R99) along with the output resistance of the amplifier form the 50 ohm output resistance.

The output of this amplifier, called 10HZ TO 30MHZ OUTPUT, is a sine wave with an amplitude between 1.1V and 3.5V rms into 50 ohms. This output signal is used by the attenuators to provide the overall output range of the Wideband Output assembly. Resistors R41 and R42, and capacitor C23 divide this output signal to create OUTPUT OFFSET for diagnostics.

2-227. WIDEBAND OUTPUT ATTENUATORS

The 10 Hz to 30 MHz sine wave signal output of the power amplifier circuit connects to the 50 ohm output attenuator composed of attenuator networks Z1 and Z2 and relays K4, K5, K6, K7, and K8.

Relay K4 switches the 10 dB attenuator into the circuit when activated or bypasses it when not activated.

Relay K5 switches the 20 dB attenuator into the circuit when activated or bypasses it when not activated.

Relays K6 and K7 switch the 40 dB attenuator into the circuit when activated and bypasses it when not activated. The attenuator can therefore reduce the signal level in 10 dB steps from 0 to 70 dB.

The output amplitude of the power amplifier circuit can be continuously varied over a 10 dB range, which when combined with the 0 to 70 dB attenuator, gives the the continuous output range of 300 uV to 3.5V rms.

When energized, relay K8 enables the output signal to be connected to the output coaxial connector J2.

2-228. WIDEBAND OUTPUT RMS SENSOR AND AMPLITUDE CONTROL CIRCUIT

The rms sensor circuit is used for:

- o Amplitude control
- o Overload control over the frequency range of 12 kHz to 30 MHz
- o Overload control only over the frequency range of 10 Hz to 12 kHz

The rms sensor and amplitude control circuit is composed of U1, U2A, U2B, U3, U5, U12A, U12B, and associated components. Thermal sensor U1 provides a dc voltage equal to the rms value of the input voltage (at pin 6).

Input voltage to the thermal sensor comes from the power amplifier circuit. DC voltage output from the thermal sensor is connected to U2A configured as an intergrator. The output of the intergrator is connected to a square-root amplifier configured by U2B U3, and U12A, which keeps the settling time of the sensor constant.

The dc output of this sensor circuit (available at TP1) is buffered by U5. In the 12 kHz to 1.1 MHz range, the output of U5 is connected to the RCL line by relay K10 in the set position. In the 1.2 MHz to 30 MHz range, the output of U5 is compared by U12B to DAC OUT.

The DAC assembly (A11) output, DAC OUT HI and DAC SENSE HI, are tied together by relay K11 to create DAC OUT.

Relay K2A connects capacitor C7 into the rms sensor circuit in the 10 Hz to 11 kHz range to add additional filtering for low frequency signals.

2-229. WIDEBAND OUTPUT OVERLOAD CONTROL CIRCUIT

The overload control circuit contains comparator U4 (A and B), FETs Q2 and Q3, transistor Q1, and associated circuitry. This circuit protects the rms sensor and attenuators during an overload condition. Comparator U4A detects an overload condition by comparing the dc output of the rms sensor against a reference voltage.

The reference voltage is determined by zener diode VR2 and resistor R21. If the dc output of the rms sensor reaches a voltage 10% greater than the normal full-scale voltage, the output of U4A goes negative. This negative voltage causes a positive voltage at the output of U4B which turns on FETs Q2 and Q3. These FETs protect the rms sensor from damage by shunting its input and output to ground through the 200 ohm resistors R2 and R18.

The negative voltage at the output of U4A also turns off transistor Q1 and causes control line U9 ENABLE to go high. This disables relay driver U9, which turns off all attenuator relays (K4-K7) and output relay K8.

2-230. WIDEBAND OUTPUT DIGITAL CONTROL

The heart of the Wideband Output assembly digital control circuitry is a 82C55 programmable peripheral interface IC (U7), which is under software control via the guarded digital bus.

This IC has three ports, generating 24 outputs. These outputs control three relay drivers (U6, U9, U10) and a 4051 analog multiplexer IC (U8) for self diagnostics.

Port A (PA0-PA7) is used as a common input bus for the relay drivers. Relay driver U6 controls latching relays K1, K2, K10, K11, and K12. Driver U6 is enabled by PC3 and strobed by PC2. Relay driver U9 controls non-latching relays K4-K8. Driver U6 is strobed by PC0 and enabled by control line U9 ENABLE, which is generated in the overload control circuit. Relay driver U10 controls latching relays K3 and K9. It is strobed by PC1 and enabled by PC3.

Relays K1 and K12 are controlled by the same drive lines and, when in the set position, select the input from the Oscillator Output (A13) assembly during operation between 10 Hz and 1 MHz.

Relay K9 connects a 50 ohm load (R43 and R44 in parallel) to the RCL line where the adc circuit on the DAC assembly can monitor the output voltage and thereby determine proper operation of the output attenuator resistors and relays.

The 4051 analog multiplexer IC (U8) is used by self-diagnostic routines for the Wideband AC module. This allows the 5700A to monitor three points on the Wideband Output assembly and one point on the Wideband Oscillator assembly. Points AMPLITUDE CONTROL, OUTPUT OFFSET, and SENSOR CAL are monitored on the Wideband Output assembly, and point PLL DIAGNOSTIC is monitored on the Wideband Oscillator assembly. PC4-PC6 of port C select which point the multiplexer monitors. PC7 enables the output of U8 to the SDL line where is is measured by the adc circuit on the DAC assembly (A11).

2-231. WIDEBAND OUTPUT CALIBRATION

Linearity of the rms sensor is determined by configuring the Wideband Output similarly to the second range of operation as described earlier. A difference is that the Oscillator Output assembly operates at 1 kHz instead of between 12 kHz and 1.1 MHz during operating in this range.

The Oscillator Output is set to 2.5V at 1 kHz. The resulting dc voltage from the rms sensor is connected to the RCL line by relay K10 in the set position. The RCL line is routed to the +input of the adc circuit on the DAC assembly, and the adc -input is connected to the DAC output. The difference between the two is measured and stored in memory. The Oscillator Output is increased to 7.0V and the difference between the two adc inputs is again measured. Software uses these values to determine the linearity of the rms sensor.

The previously calibrated 6.5V reference BRF6 and its sense line BSRF6, from the DAC assembly is used to calibrate the 10 dB, 20 dB, and 40 dB attenuators.

Relays K3 A and B and K12 are in the set position. This connects the 6.5V reference to the unity-gain amplifier and the attenuators. Output at the WIDEBAND type-N connector is connected back to the OUTPUT HI SENSE and OUTPUT LO SENSE binding posts.

Attenuation is calibrated starting with 70 dB and decreased in 10 dB steps to 0 dB. The Switch Matrix assembly connects the output of the Wideband AC module to its internal cal zero amplifier circuit during all attenuator calibrations except the 0 dB and 10 dB. The internal cal zero amplifier circuit provides a gain of 10 to Wideband output during 20 dB to 70 dB attenuation calibration. The output of this amplifier is connected to the RCL line which is routed to the +input of the adc circuit on the DAC assembly. Output from the DAC is connected to the -input of the adc circuit and adjusted until a null is achieved. The exact attenuator value is then determined.