



## 2N50

Preliminary

Power MOSFET

### 2A, 500V N-CHANNEL POWER MOSFET

#### DESCRIPTION

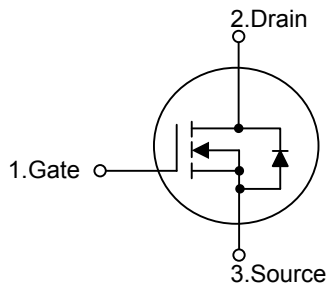
The UTC **2N50** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **2N50** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

#### FEATURES

- \*  $R_{DS(ON)} = 4.9\Omega @ V_{GS} = 10V$
- \* High Switching Speed
- \* 100% Avalanche Tested

#### SYMBOL

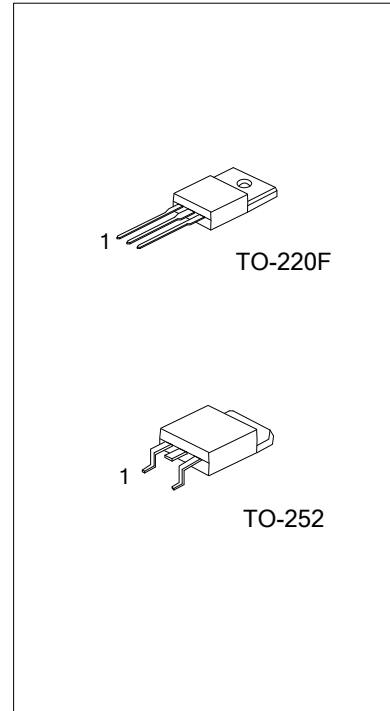


#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N50L-TF3-T	2N50G-TF3-T	TO-220F	G	D	S	Tube
2N50L-TN3-R	2N50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>2N50L-TF3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Free</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TF3: TO-220F, TN3: TO-252</p> <p>(3) G: Halogen Free, L: Lead Free</p>
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■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	500	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous ( $T_C=25^\circ\text{C}$ )	$I_D$	2 (Note 3)	A
	Pulsed (Note 2)	$I_{DM}$	8 (Note 3)	A
Avalanche Current (Note 2)		$I_{AR}$	2	A
Avalanche Energy	Single Pulsed	$E_{AS}$	82	mJ
	Repetitive (Note 4)	$E_{AR}$	3.3	mJ
Power Dissipation ( $T_C=25^\circ\text{C}$ )	TO-220F	$P_D$	23	W
	TO-252		50	
Derate above $25^\circ\text{C}$	TO-220F		0.18	W/ $^\circ\text{C}$
	TO-252		0.4	
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature		$T_{STG}$	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. Drain current limited by maximum junction temperature
4. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$

■ THERMAL DATA

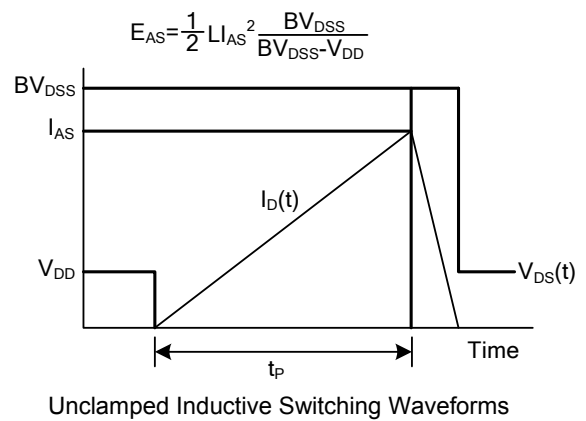
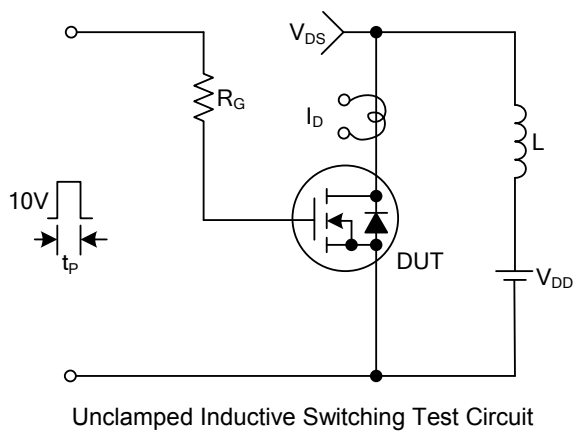
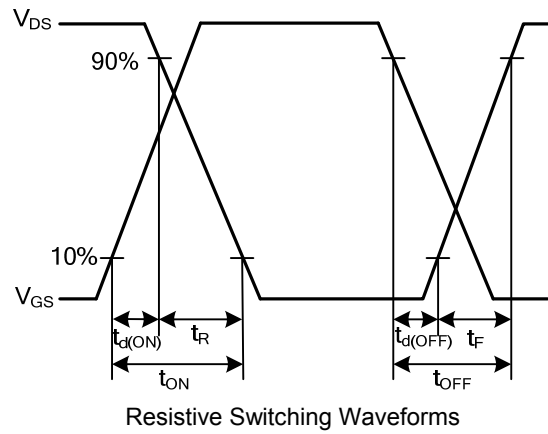
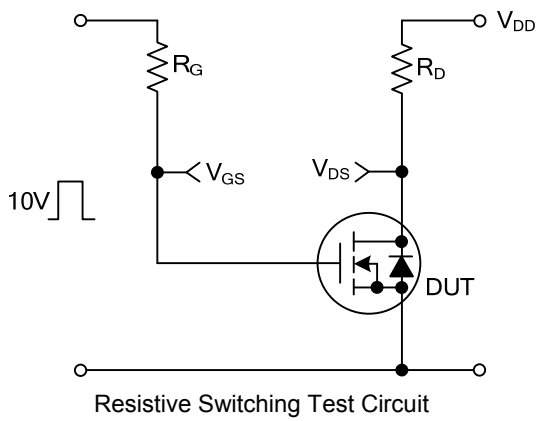
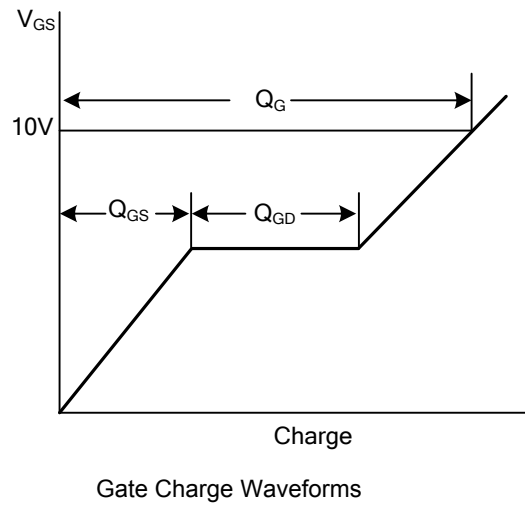
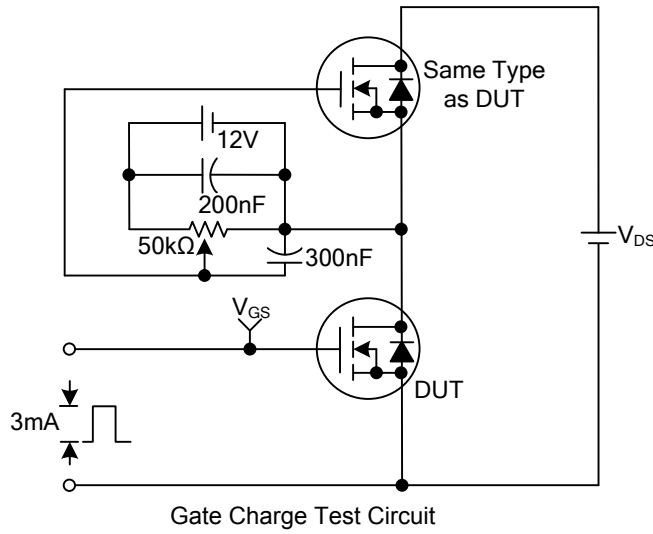
PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220F	$\theta_{JA}$	62.5	$^\circ\text{C/W}$
	TO-252		110	
Junction to Case	TO-220F	$\theta_{JC}$	5.5	$^\circ\text{C/W}$
	TO-252		2.5	

■ ELECTRICAL CHARACTERISTICS ( $T_c=25^\circ\text{C}$ , unless otherwise noted)

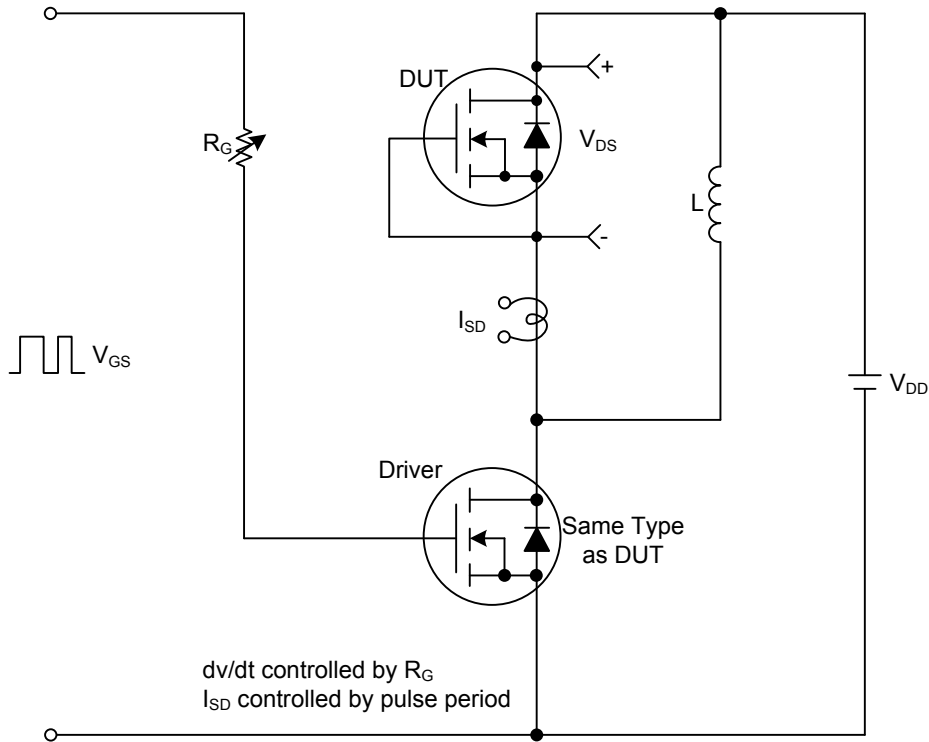
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=500\text{V}$ , $V_{GS}=0\text{V}$			25	$\mu\text{A}$
Gate- Source Leakage Current	Forward	$V_{GS}=+30\text{V}$ , $V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-30\text{V}$ , $V_{DS}=0\text{V}$			-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=1\text{A}$		3.9	4.9	$\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{MHz}$		236		pF
Output Capacitance	$C_{OSS}$			40		pF
Reverse Transfer Capacitance	$C_{RSS}$			22		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{GS}=10\text{V}$ , $V_{DS}=400\text{V}$ , $I_D=2\text{A}$ (Note 1, 2)		20	25	nC
Gate to Source Charge	$Q_{GS}$			2	3	nC
Gate to Drain Charge	$Q_{GD}$			12	15	nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=250\text{V}$ , $I_D=2\text{A}$ , $R_G=25\Omega$ (Note 1, 2)		10		ns
Rise Time	$t_R$			20		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			60		ns
Fall-Time	$t_F$			20		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				2	A
Maximum Body-Diode Pulsed Current	$I_{SM}$				8	A
Drain-Source Diode Forward Voltage	$V_{SD}$	$I_S=2\text{A}$ , $V_{GS}=0\text{V}$			1.2	V
Body Diode Reverse Recovery Time	$t_{RR}$	$I_S=2\text{A}$ , $V_{GS}=0\text{V}$ , $dI_F/dt=100\text{A}/\mu\text{s}$		300		ns
Body Diode Reverse Recovery Charge	$Q_{RR}$	(Note 1)		2.1		$\mu\text{C}$

- Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$   
 2. Essentially independent of operating temperature

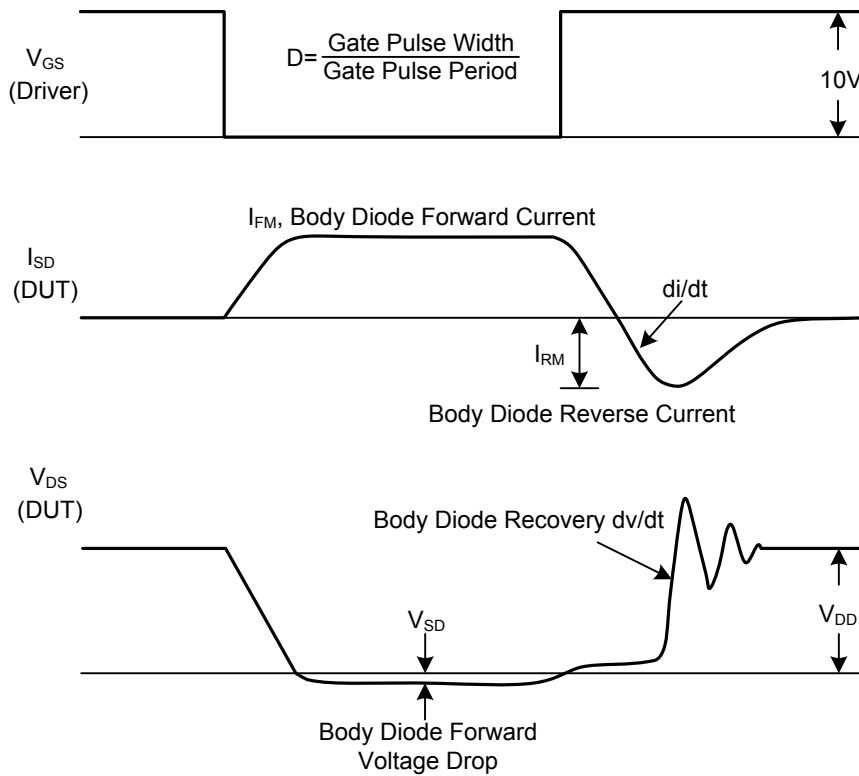
■ TEST CIRCUITS AND WAVEFORMS



■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms



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