PART 2 OF THIS SERIES ON THE DESIGN OF A 20-BIT DAC DISCUSSES THE ALL-IMPORTANT TECHNIQUES FOR TESTING THE PERFORMANCE–LINEARITY, SETTLING TIME, AND NOISE–AT SUCH MINUSCULE DATA LEVELS. SEE PART 3 IN THE NEXT ISSUE.

Measurement techniques help hit the 1-ppm mark

A TRUE 20-BIT DAC that fits on a circuit board and costs approximately $100 to build is a design milestone (see *EDN*, April 12, 2000, pg 95 or www.ednmag.com/ednmag/reg/2001/04122001/08ms743.htm). Claiming to achieve this level of performance is one thing, but proving it with precise measurements is another. The measurement techniques are at times more exacting than the actual circuit's design. Part 2 of this series presents approaches and circuits for measuring linearity, settling time, and noise.

MEASURE LINEARITY TO 1 PPM

Of these three measurements, determining the DAC's linearity requires the greatest effort. Verifying 1-ppm linearity of the DAC and the integral ADC requires special considerations, and, interestingly, some help from the 19th century. Testing necessitates some form of voltage source that produces equal-amplitude output steps for incremental digital inputs. Additionally, for measurement confidence, it is desirable that the source be substantially more linear than the 1-ppm requirement. This demand is stringent and painfully close to the state of the art.

The most linear "digital-to-analog" converter is also one of the oldest. Lord Kelvin's KVD (Kelvin-Varley divider) is, in its most developed form, linear to 0.1 ppm. This manually switched device features 10 million individual dial settings arranged in seven decades. You can think of the device as a three-terminal potentiometer with fixed "end-to-end" resistance and a seven-decade switched wiper position (**Figure 1a**).

The actual construction of a 0.1-ppm KVD is

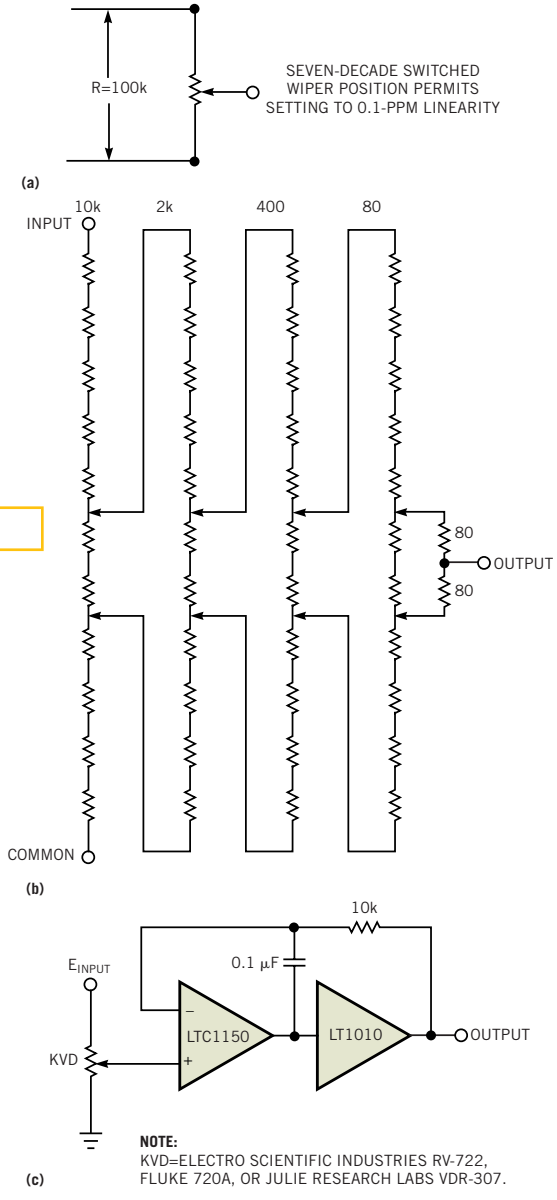


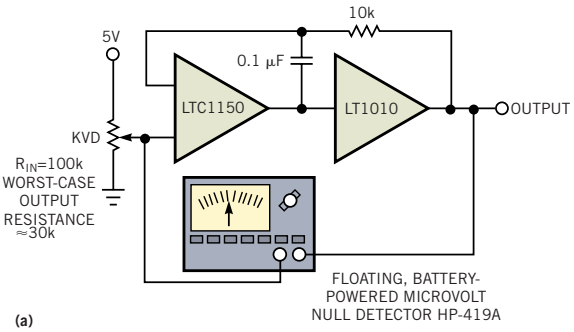
Figure 1

A conceptual KVD is a three-terminal potentiometer with a seven-decade switched wiper position (a). You can expand this four-decade KVD by continuing the divide-by-5 chains (b). Adding an output buffer to the KVD gives output-drive capability (c).

NOTE:
KVD=ELECTRO SCIENTIFIC INDUSTRIES RV-722, FLUKE 720A, OR JULIE RESEARCH LABS VDR-307.

more artistry and witchcraft than science. The market is relatively small, the vendors few, and the resultant price high. If $13,000 for a bunch of switches and resistors seems offensive, try building and certifying your own KVD. The KVD in **Figure 1b** has a 100-kΩ input impedance. Thus, wiper's output resistance is high and varies with setting. As such, a very low bias-current follower is necessary to unload the KVD without introducing significant error (**Figure 1c**). The LT1010 output buffer allows for driving cables and loads and, more subtly, maintains the amplifier's high open-loop gain.

The schematic in **Figure 1c** is deceptively simple. In practice, construction details are crucial. Parasitic thermocouples, or namely the Seebeck effect; layout; grounding; shielding; guarding; cable choice; and other issues affect achievable performance. Part 3 discusses these issues in detail. In fact, as good as the chopper-stabilized LTC1150 is with respect to drift, offset, bias current, and CMRR (common-mode rejection ratio), selection is necessary if you seek sub-ppm nonlinearity performance. An error-budget analysis details some of the selection criteria (**Figure 2**). You can test the buffer with **Figure 2a**'s circuit. As you run the KVD through its entire range, the floating null detector must remain well within 1 ppm, or 5 μV, and preferably at less than 0.5 ppm. This test ensures that you account for all error sources, particularly I_B and CMRR, whose effects vary with operating point. Measured performance indicates that the sum of all errors called out in **Figure 2b** are well within desired limits.



(a)

ERROR SOURCE	WORST-CASE SPEC	REALISTIC SELECTION TARGET	ERROR IN PPM
E_{OS}	5 μV	0.5 μV	0.1
$E_{OS\Delta T}$	0.05 μV/°C	0.05 μV/°C	0.01/°C
I_B	50 pA	10 pA	0.1
CMRR	110 dB	140 dB	0.1
FINITE GAIN	140 dB	140 dB	0.1

(b)

Figure 2

You can determine buffer error by measuring the I/O deviation with a floating microvolt null detector. This technique permits evaluation of fixed and operating-point-induced errors (a). An error-budget analysis for the KVD buffer details the selection criteria (b).

CIRCUIT CONSTRUCTION IS CRITICAL

The detailed schematic of the sub-ppm-linearity voltage source includes offset trim, a stable voltage source, and a second KVD to drive the main KVD (**Figure 3**). Additionally, an ensemble of three HP3458A voltmeters monitors the output. The offset trim bleeds a small current into the main KVD ground return, producing a few microvolts of offset-trim range. This range allows you to functionally trim out all sources of zero error, such as amplifier offsets and parasitic thermocouple mismatches, permitting a true zero-volt output when the main KVD setting is all zeros. Three voltmeters, which have a specification of less than 0.1-ppm nonlinearity on the 10V range, "vote" on the source's output. In other words, each voltmeter monitors the source's output. Then, you correct each reading for absolute error and average the three corrected readings to obtain the apparent linearity.

The single-point-grounding scheme prevents the mixing of return currents and the attendant errors. The shielded cables for connecting the KVDs and voltmeters should have low-thermal-activity specifications. Keithley type SC-93 and Guildline #SCW are suitable. Crush-type copper lugs, as opposed to soldered types, provide lower parasitic-thermocouple activity at KVD and DVM connection points. However, you must keep the lugs clean to prevent oxidation, thus avoiding excessive thermal voltages (see Part 3). A copper deoxidant (Caig

TABLE 1–HIGH-SENSITIVITY, LOW-NOISE AMPLIFIERS

Instrument type	Manufacturer	Model number	Maximum bandwidth	Sensitivity or Gain	Availability	Comments
Differential amplifier	Tektronix	1A7/1A7A	500 kHz/1 MHz	10 μV/DIV	Secondary market	Requires 500 series mainframe, settable bandstops
Differential amplifier	Tektronix	7A22	1 MHz	10 μV/DIV	Secondary market	Requires 7000 series mainframe, settable bandstops
Differential amplifier	Tektronix	5A22	1 MHz	10 μV/DIV	Secondary market	Requires 5000 series mainframe, settable bandstops
Differential amplifier	Tektronix	ADA-400A	1 MHz	10 μV/DIV	Current production	Stand-alone with optional power supply, settable bandstops
Differential amplifier	Tektronix	AM-502	1 MHz	Gain=100,000	Secondary market	Stand-alone with optional power supply, settable bandstops
Differential amplifier	Preamble	1822	10 MHz	Gain=1000	Current production	Stand-alone, settable bandstops
Differential amplifier	Stanford Research Systems	SR-560	1 MHz	Gain=50,000	Current production	Stand-alone, settable bandstops, battery or line operation

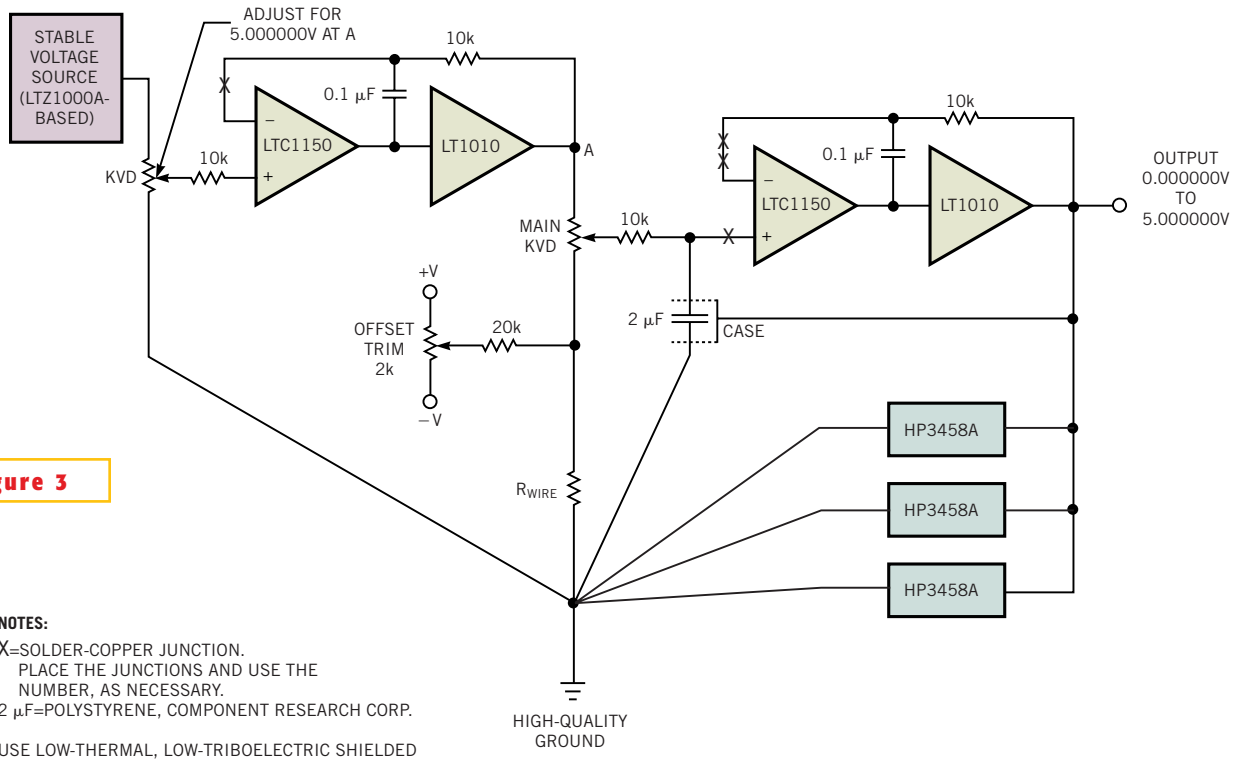


Figure 3

NOTES:

X=SOLDER-COPPER JUNCTION.
PLACE THE JUNCTIONS AND USE THE NUMBER, AS NECESSARY.
2 µF=POLYSTYRENE, COMPONENT RESEARCH CORP.

USE LOW-THERMAL, LOW-TRIBOELECTRIC SHIELDED CABLE FOR KVD AND DIGITAL-VOLTMETER CONNECTIONS.

The complete sub-ppm-linearity voltage source includes offset trim, a stable voltage source, and a second KVD to drive the main KVD.

Labs "Deoxit" D100L) is effective for maintaining such cleanliness. Low thermal lugs and jacks, preterminated to cables, are also available (Hewlett-Packard 11053, 11174A) and convenient.

Thermal baffles that enclose the KVD and DVM connections tend to thermally equilibrate their associated banana-jack terminals, minimizing residual parasitic-thermocouple activity. Additionally, you should restrict the number of connections in the signal path. You also need to balance electrical connections in the signal path against each other such that the net signal-path degradation due to thermocouples is nominally equal to zero. When you introduce a deliberate thermocouple, be sure to match materials. Complying with this guideline may necessitate a deliberate introduction of solder-copper junctions, marked "X" on **Figure 3**, to obtain optimum differential cancellation (see Part 3). Simply breaking the appropriate wire or pc trace and soldering it facilitates this cancellation. Ensure that the introduced thermocouples temperature-track the junctions they are supposed to cancel. You can usually ensure temperature

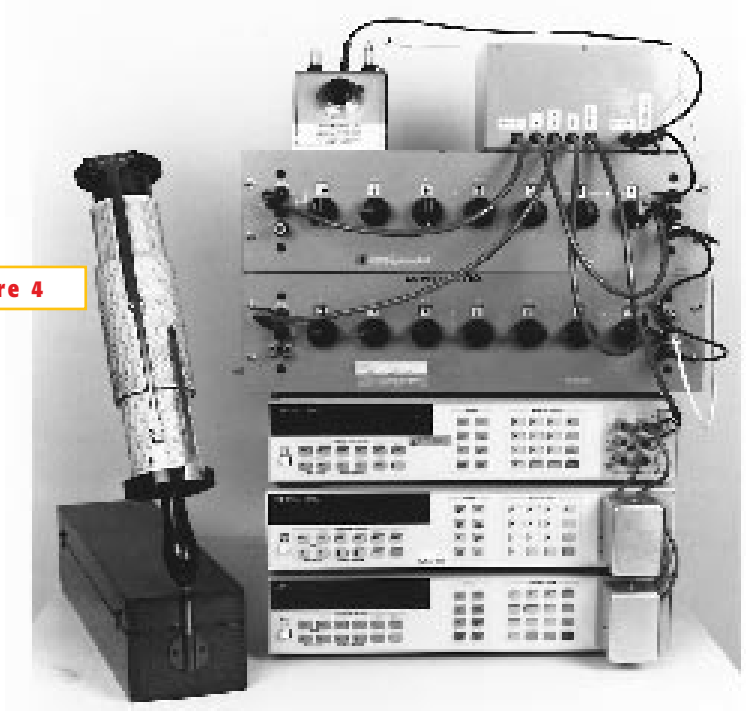


Figure 4

In the sub-ppm-linearity voltage source, the LTZ1000A-based reference and buffers are at the upper right. Offset trim is at the upper left, and reference and main KVDs are at the upper center and center middle, respectively. Three HP3458 DVMs at the bottom monitor output. The computer in the left foreground aids linearity calculations.

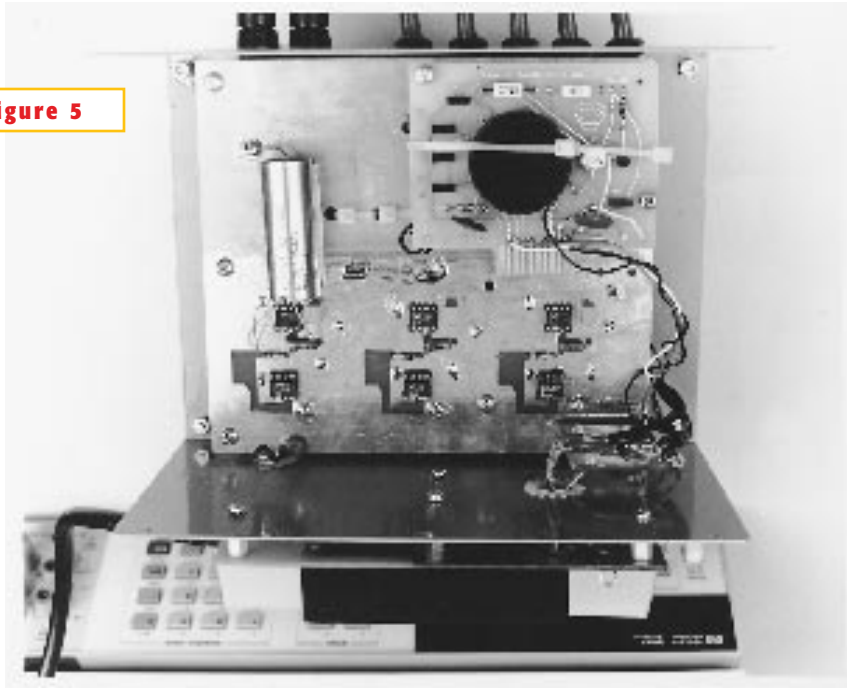
tracking by locating all junctions close to each other.

The noise-filtering capacitor at the main KVD is a low-leakage type; the output buffer drives the capacitor's metal to guard against surface leakage.

When studying this measurement approach, it is essential to differentiate between linearity and absolute accuracy. This differentiation eliminates concerns with absolute standards, permitting certain freedoms in the measurement scheme. In particular, although **Figure 3** uses single-point grounding, the circuit does not use remote sensing. This choice is deliberate, made to minimize the number of potential error-causing parasitic thermocouples in the signal path. Similarly, the design does not use a ratiometric reference connection between the KVD LTZ1000A voltage source and the voltmeters for the same reason. In theory, a ratiometric connection affords lower drift. In practice, the resultant introduced parasitic thermocouples obviate the desired advantage. Additionally, the aggregate stability of the LTZ1000A reference and the voltmeter references (also, incidentally, LTZ1000A based) is comfortably inside 0.1 ppm for periods of 10 minutes, which is more than enough time for a 10-point linearity measurement.

Figures 4 and **5** are photographs of the voltage source and the reference-buffer-box internal construction. This KVD-based, high-linearity voltage source has been in use for years. The measurement regime involves three steps:

Figure 5

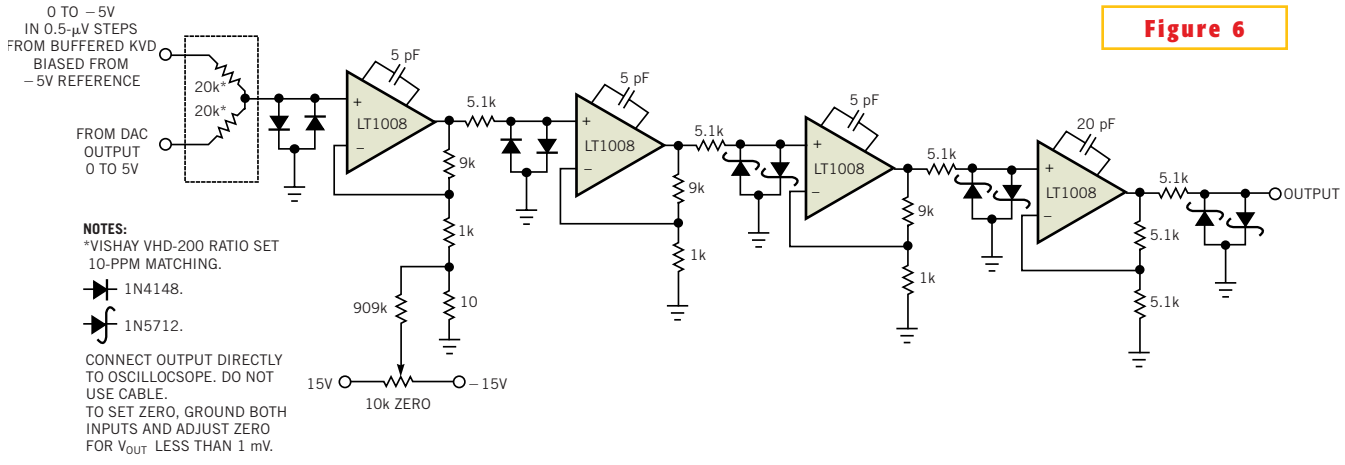


In the reference-buffer box, the LTZ1000A reference circuitry is at the lower left, buffer amplifiers are in the center, the capacitor-case bootstrap connection is center-right, and single-point-ground "mecca" is at the upper left. The power supply at the top mounts outside of the box, minimizing magnetic-field disturbances.

- verifying KVD linearity by intercomparison with other KVDs and by an independent calibration laboratory,
- taking worst-case voltmeter ensemble deviations over 0 to 5V every 0.5V, and
- performing 100 runs (10 per day, once per hour).

During this period, the total linearity uncertainty defined by the source and its monitoring voltmeters is just 0.3 ppm. This value is more than three times better than the desired 1-ppm performance, promoting confidence in your measurements. A delightful activity, particularly for those wholly unenthralled with Web surfing, is to spend hours "surfing the Kelvin." This activity consists of dialing various KVD settings and noting ADC

Figure 6

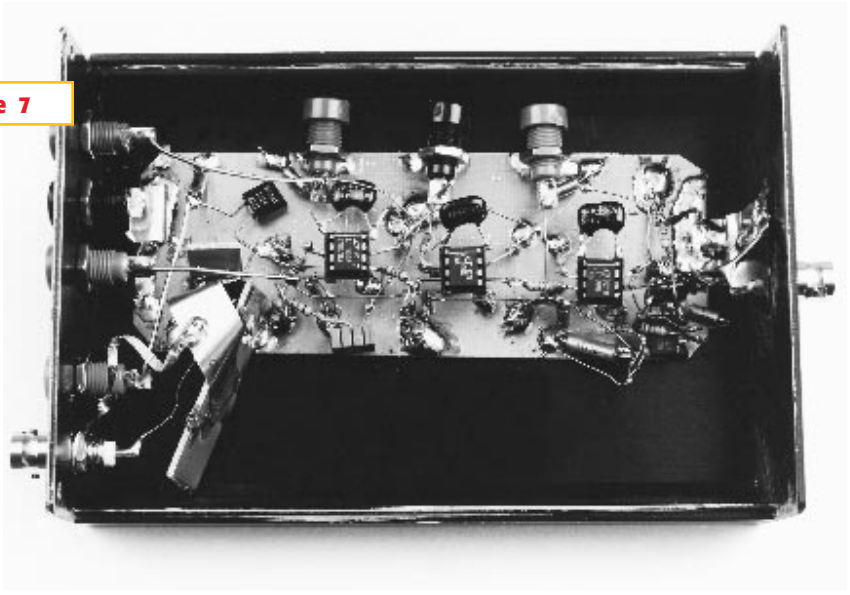


A clamped, distributed gain-of-2000 amplifier permits DAC settling-time measurements without saturation effects.

agreement within 1 ppm. This astonishingly nerdy behavior thrills certain types.

MEASURING DAC SETTLING TIME

Figure 7



The settling-time amplifier's bandwidth is only 10 kHz, but its high gain of 2000 necessitates careful layout to avoid parasitic-feedback-induced oscillation. The input at lower left is fully shielded to prevent radiative feedthrough to amplifier, and the enclosure shields the circuit from stray RF and pickup.

Measuring the 20-bit DAC's output settling time is a challenging task. Although the time scale involved is relatively slow, the LSB step size of 5-μV presents problems. The issue reduces to obtaining a great deal of gain without inducing overdrive in the monitoring oscilloscope. Such overdrive will corrupt the measurement, rendering displayed results meaningless.

The input structure of **Figure 6** resistively balances the DAC output against the precision variable reference supply, such as in **Figure 3**, which is adjustable in 0.5-μV steps. The circuit's remainder constitutes a clamped, distributed gain-of-2000 amplifier. Diode clamping at each gain-stage input prevents saturation from occurring even with large DAC-reference supply imbalances. The distributed gain allows a 10-kHz bandwidth while maintaining clamping effectiveness. The monitoring oscilloscope, operating at 5 or 10 mV/DIV (5 to 10 μV at the DAC output) can readily discern 5-μV settling without incurring deleterious overdrive.

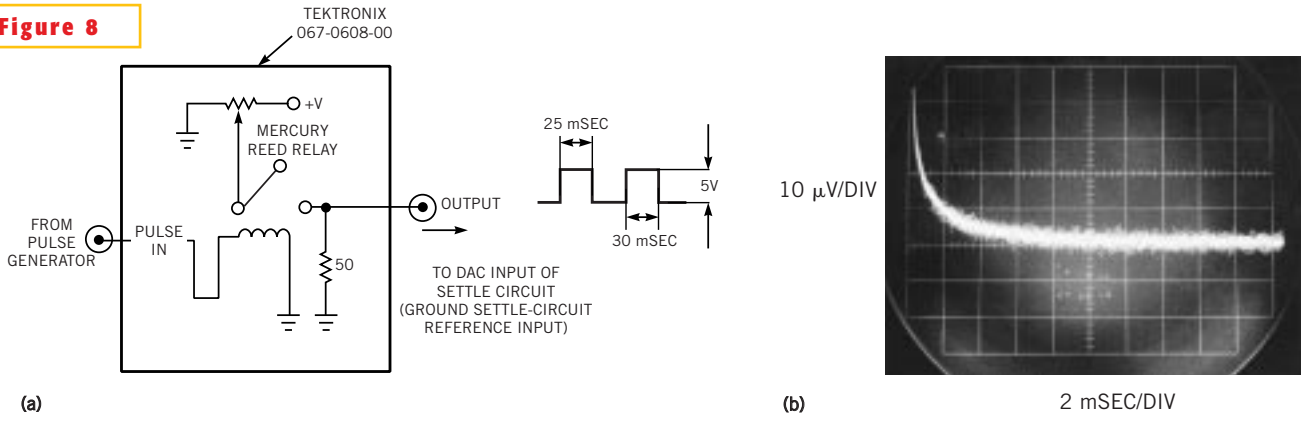
Layout and construction of this circuit requires care. A linear layout minimizes parasitic feedback paths, preventing oscillation (**Figure 7**). The construction fully shields the DAC input-step signal, preventing feedthrough to various sensitive points within the amplifier. Finally, the entire circuit sits in a shielded enclosure to minimize effects of stray RF and pickup.

You can test the settling-time test circuit by applying a test step that settles much faster than the DAC. One method is to use a mercury-wetted reed-relay-based pulse generator to supply the step (**Figure 8a**). The mercury-wetted reed relay opens in 5 nsec, and the when the relay opens, the circuit's output settles essentially instantaneously relative to DAC speed and settling-time-amplifier bandwidth. The relay in **Figure 8a** is commercially available, but you can obtain similar results with standard mercury-based reed relays. You test **Figure 6**'s response by grounding one input and driving the other input with **Figure 8a**'s pulse generator. The test circuit settles to within 1 ppm (±5 μV) in 2 msec (**Figure 8b**). This time is much faster than the DAC's settling time, lending confidence to the settling-time results of Part 1.

MEASURING MICROVOLT NOISE LEVELS

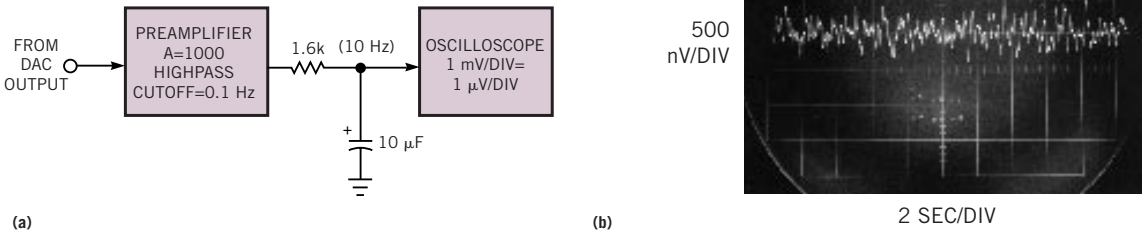
Verifying DAC output noise requires a quiet, high-gain amplifier at the oscilloscope. **Figure 9a** shows one way to take

Figure 8



A mercury wetted reed-relay-based pulser supplies a clean step to test the settling-time circuit (a), which responds to the test step with 2-msec settling to ±1ppm (±5 μV) (b).

Figure 9



A microvolt noise measurement necessitates a high-gain preamplifier for the oscilloscope (a). DAC output noise in a 0.1-to-10-Hz measurement bandpass, set by the preamplifier and discrete filter, is less than 1 mV, or approximately 0.2 LSB (b). Equipment limitations set the measurement noise floor at 0.2 µV.

the measurement. The input preamplifier, operating at a gain of 1000, has a highpass cutoff at 0.1 Hz and drives the oscilloscope via a 10-Hz discrete lowpass filter. The oscilloscope, set to 1 mV/DIV, indicates 1 µV/DIV referred to the preamplifier input. **Figure 9b** indicates that the DAC output noise is well below an LSB, about 0.9 µV. Equipment limitations set the measurement noise floor at 0.2 µV. These signal levels dictate a completely shielded, coaxial path from breadboard to oscilloscope (**Figure 10**).

Table 1 lists some applicable high-sensitivity amplifiers suitable for the noise measurement. Current-generation oscilloscopes rarely have sensitivities greater than 2 mV/DIV, although older instruments offer more capability. The **table** lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurement. These units feature wideband, low-noise performance. It is particularly significant that many of these instruments are no longer in production. This fact is in keeping with current instrumentation trends, which emphasize digital-signal acquisition as opposed to analog-measurement capability.

The monitoring oscilloscope should have exceptional trace clarity. In the latter, high-quality analog oscilloscopes are unmatched. The exceptionally small spot size of these instruments suits low-level noise measurement. Tektronix types 453, 453A, 454, 454A, 547, and 556 are excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise-floor-limited background. The digitizing uncertainties and raster-scan limitations of DSOs impose display-resolution penalties. Many DSO displays will not even register the fine structure of the noise waveform.□

Author's biography

Jim Williams is a staff scientist at Linear Technology Corp (Milpitas, CA, www.linear-tech.com), where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA) where he first encountered serious 1-ppm measurement using the KVD. A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

Acknowledgments

I am indebted to Lord Kelvin and to Warren Little of the CS Draper Laboratory (née Massachusetts Institute of Technology Instrumentation Laboratory) standards lab. Warren taught me, with great patience, the wonders of KVDs some 30 years ago, and I am still trading on his efforts.

Figure 10

The noise-measurement test setup includes a shielded DAC breadboard (foreground), a preamplifier (left), and a lowpass filter attached to the oscilloscope (center). The measurement path is fully coaxial.