FLUKE 900

SERVICE MANUAL

NOTE: This manual documents FLUKE 900 instruments S/N 4720000 and above.
It also documents any FLUKE 900 with the Simulation Option (900-001) installed.

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FLUKE P/N 889691

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Table of Contents

1 Service Manual Introduction

1.1 Description of Operator, Service Manuals

Documentation for the FLUKE 900 Dynamic Troubleshooter includes the Service Manual, Operator Manual and Training Manual. For the purposes of maintenance and repair relevant sections of the Operator Manual are:

Section 1.2 on Specifications
Section 1.4 on Shipping, Unpacking, and Connection
Section 1.5 on Keyboard Operation
Section 1.6 on Option Setting

It is recommended that the reader become familiar with this information and perhaps the section on Technical Principles from the Operator Manual before undertaking service repair of the unit.

While some tasks in the Maintenance section of this Service Manual are relatively simple, calibration and most troubleshooting require a thorough understanding of the information presented in sections 1, 2 and 3 of this Service Manual.

1.2 Basic Operation of Keyboard and Display

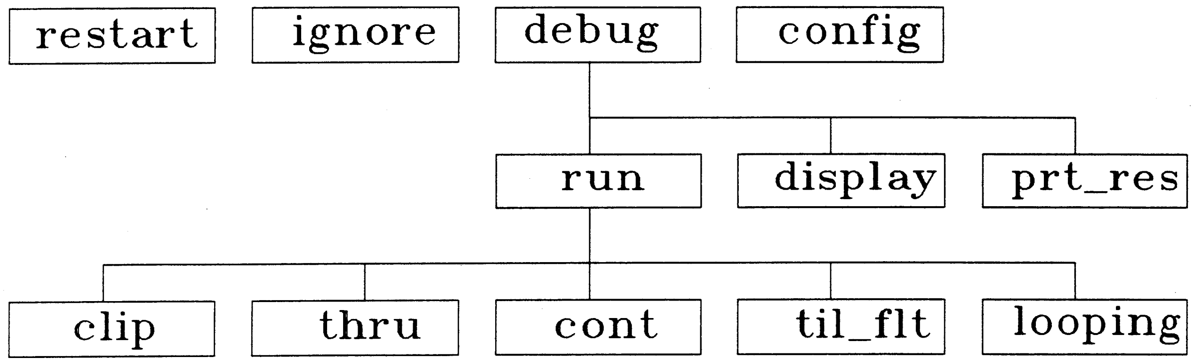
The FLUKE 900 display has 4 major areas:

- Information area in the upper portion of the screen
- Status line reverse highlighted in the middle of the screen
- Command line for entering instructions below the status line
- Function key labels reverse highlighted at the bottom of screen

There are 5 Function Key labels and they are represented in this manual as: F1(label). Permanently labelled keys are represented as: ENTER. Operational modes progress down a tree of levels and sub-levels with the Function Keys. ESC, on the left of the Function Keys, moves operation up one level of the menu tree. ETC brings up more labels on the same level of the tree.

Data that is typed in appears on the command line, but is only acted upon after ENTER is pressed. CE performs a backspace function on the command line; SHIFT CE erases the last word; CNTR CE erases the whole line.

The Debug mode is used for observing selftest results, running selftests and printing results. It may be entered, after a successful selftest, by pressing F4(system) ETC F1(debug) from the main screen of the initial level. Debug is accessible directly after a poweron selftest fails. The menu tree for the Function Keys after a fail appears as:



F1(restart) will re-execute the poweron selftest.
F2(ignore) will bring up the main screen directly. If any of the failed selftests involve actual testing circuitry (eg. FMxx), the operator will not be permitted to actually run a test cycle. File manipulation, RD Test and System setting changes are possible, however.

Debug has three main keys: F1(run), F2(display), F3(prt_res). The last one means "print results" and sends a formatted listing of all test results from the last test(s) executed to the serial RS232 port. "display" brings to the screen, the characteristic 4 byte individual result of the test whose number was entered on the command line. This test must first have been run, either explicitly or during the powerup.

The key labels under "run" are words that can be used to compose a command line instruction. Some typical instructions are:

Run_test clip Run_test 0	These two equivalent instructions run the clip continuity test. A clip must be inserted in the Input Buffer and clipped onto the Dummy Chip Module which must be plugged into the ZIF socket. Results are shown on the screen.
Run_test 40	Test 40 is executed and result bytes displayed in the case of a failure.
Run_test 1 thru 40	Tests 1 through 40 are executed successively.
Run_test continuous	The series of poweron tests are executed repeatedly with the number of passed and failed cycles displayed on the screen. ESC will terminate it upon completion of the currently executing test.. This is a useful burnin procedure.
Run_test 46 continuous until_fault	Test 46 is executed repeatedly while displaying the number of passed cycles until the point at which a failure occurs.
Run_test 1 looping	Test 1 will execute repeatedly to facilitate signal tracing with an oscilloscope.

At any point in the menu tree or any operational mode of the tester, a hard or soft reset may be executed. Pressing SHIFT and ESC simultaneously causes a soft reset that returns the display to the initial power-on screen. This action does not erase any files that are resident in volatile system RAM. For service purposes a soft reset during selftest is a convenient way to truncate the selftest and bring up the main screen immediately. Pressing CNTR and ESC simultaneously causes a hard reset that clears memory and restarts selftest.

There is a special keyboard mode used mainly for calibration called the "engineering menu". It may be entered from the main poweron screen by simultaneously pressing CNTR and an unlabeled key found between NEXT and TEST. Its use will be described in the section on calibration.

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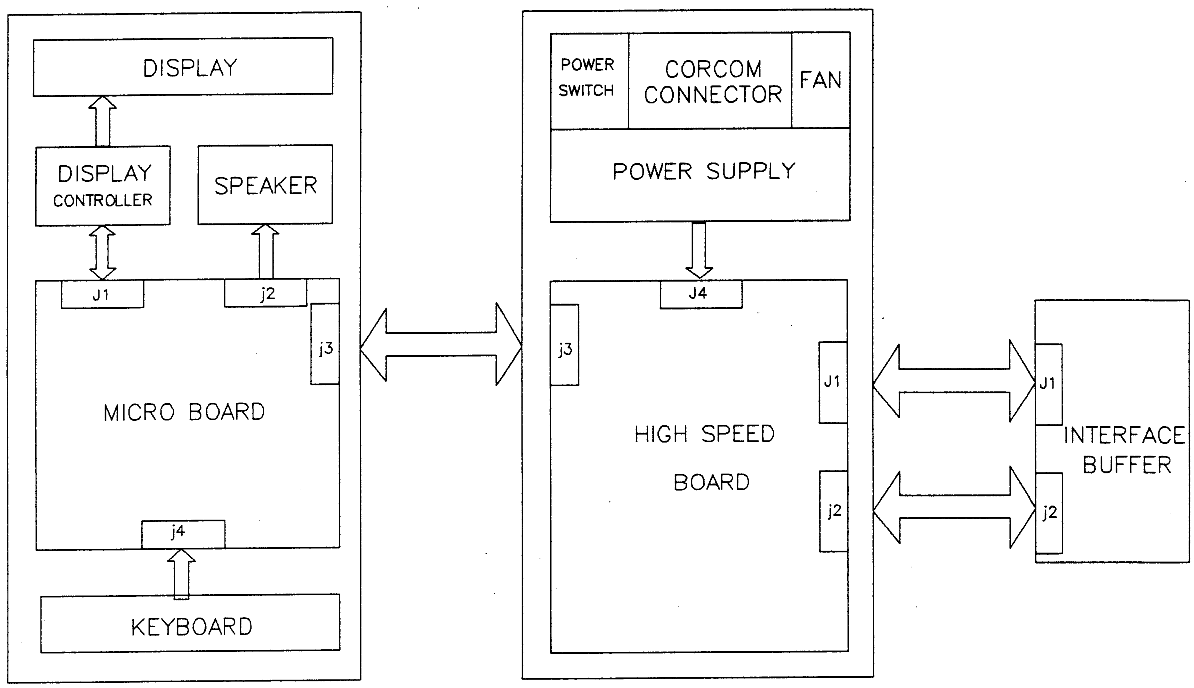
2 Theory of Operation

2.1 General

Major functional blocks of the tester correspond, in general, to physical modules. Shown below is a diagram of the modules and their interconnections.



The Interface Buffer (IB) acquires and conditions signals from the board under test. It accepts 28 signal channels from an interchangeable clip and, by means of a single threshold setting, translates them into ECL digital data for transmission to the High Speed Board.

The Micro Board (MB) controls the operating system, user interface and test parameter storage. The Micro Board has a Z80 microprocessor running from about 320K of paged memory space. The software is mainly comprised of interrupt routines that service four 8536 CIO devices. Two CIOs are on the MB, the "Keyboard" and "Map" devices, while two CIOs are on the HSB, the "Time" and "Frequency" devices.

The Micro Board sets up the High Speed Board (H3) with the proper configuration for a test before letting it run at high speed without intervention. The setup of the test proceeds by loading a series of shift registers with data appropriate for the test to be performed. Four 8 bit registers are cascaded to make a set of 32 bits in length. Six such sets are located on the H3, two on the IB.

During the test phase, signals received by the H3 are routed immediately to a comparison circuit to be matched against one of two possible signals. In the case of a signal extracted from a DUT input pin, the comparison is made with itself (no failure should appear). In the case of a DUT output pin signal, the comparison is made with the identical RD pin signal. The RD pins are continuously monitored by a resistive load to determine whether they are input or output and thus how to route the equivalent DUT signals. At each signal transition, the DUT/RD discrepancy is timed to see if it exceeds a set FMASK value. If so, and if not overridden by a Gate or Trigger setting, the faults are latched and displayed on the monitor LEDs and LCD Screen.

2.2 Interface Buffer

Pages 3,4,5,6 of the IB schematics show the signal path for each of the 28 channels that can come from a DUT. 10K resistors connect each channel to an output bit on the cascaded shift registers shown on page 1. In actual usage, these are resistors pulled up to 5 volts by default to resolve floating unconnected inputs on a UUT which could otherwise confuse test results. In addition, the check for a low condition on a pin is made while attempting to pull it high; the high check is made with the 10K resistor pulled down to ground.

After the impedance matching components and protection diodes, each channel feeds a comparator referenced to a bias voltage. The outputs are differential ECL levels for relative noisefree transmission to the High Speed Board.

The shift registers shown on page 2 are used to control the bias setting for threshold, the Reset line setting and external frequency multiplexing. Eight bits drive a DAC which resolves a 0 to 5 volt range into 100 mV increments. Five bits control the polarity, voltage and status of the Reset driver (Page 1). Three bits route one of several lines through an analog multiplexer to a voltage-controlled oscillator (U25). The measurement of the VCO frequency on the HSB is used to determine clip size (from a characteristic voltage divider in each clip), threshold verification and VCC accuracy.

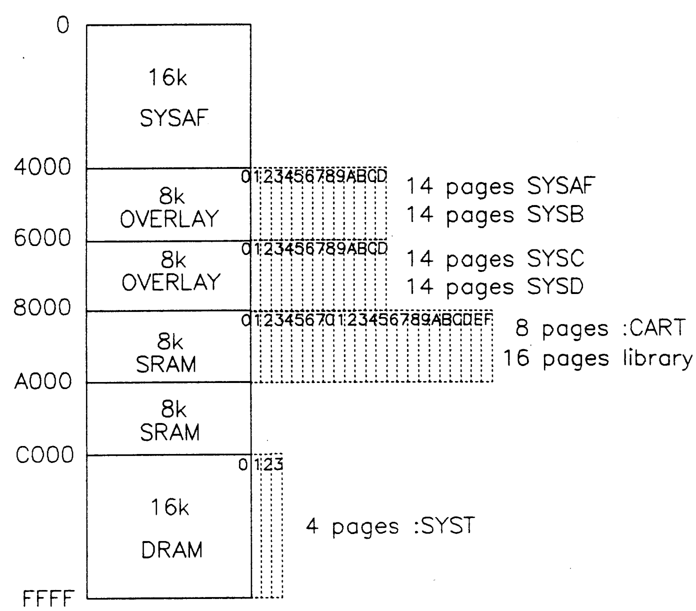
2.3 Micro Board

The Micro Board architecture is shown in the accompanying diagram. Note that, for simplification, bus buffers are not shown and all chip select signals are shown as CS to a device instead of the actual signal (eg. CS for MAP CIO is actually MAPSEL). The Z80 CPU runs at 6 MHz and operates with the Wait State Generator PAL (U69) to give the delayed control signals WRD and RDD. The CPU signals WR and RD are thus modified for the timing requirements of the Display Controller and the 8536 CIO chips. The four CIO devices are complex counter/timer and parallel I/O ports. Two are located on the MB, two on the HSB, and they interrupt the CPU for servicing of their particular function.

The MAP CIO sets up the memory map and paging scheme through PALs U58, U59, U72, U73. Port A is configured as output for the PAL chip selects. Port B is output for the EPROM chip selects. Port C is output for the RAM chip selects. The internal timer on this CIO is used for general timeout purposes in such functions as cartridge operations and library loading.

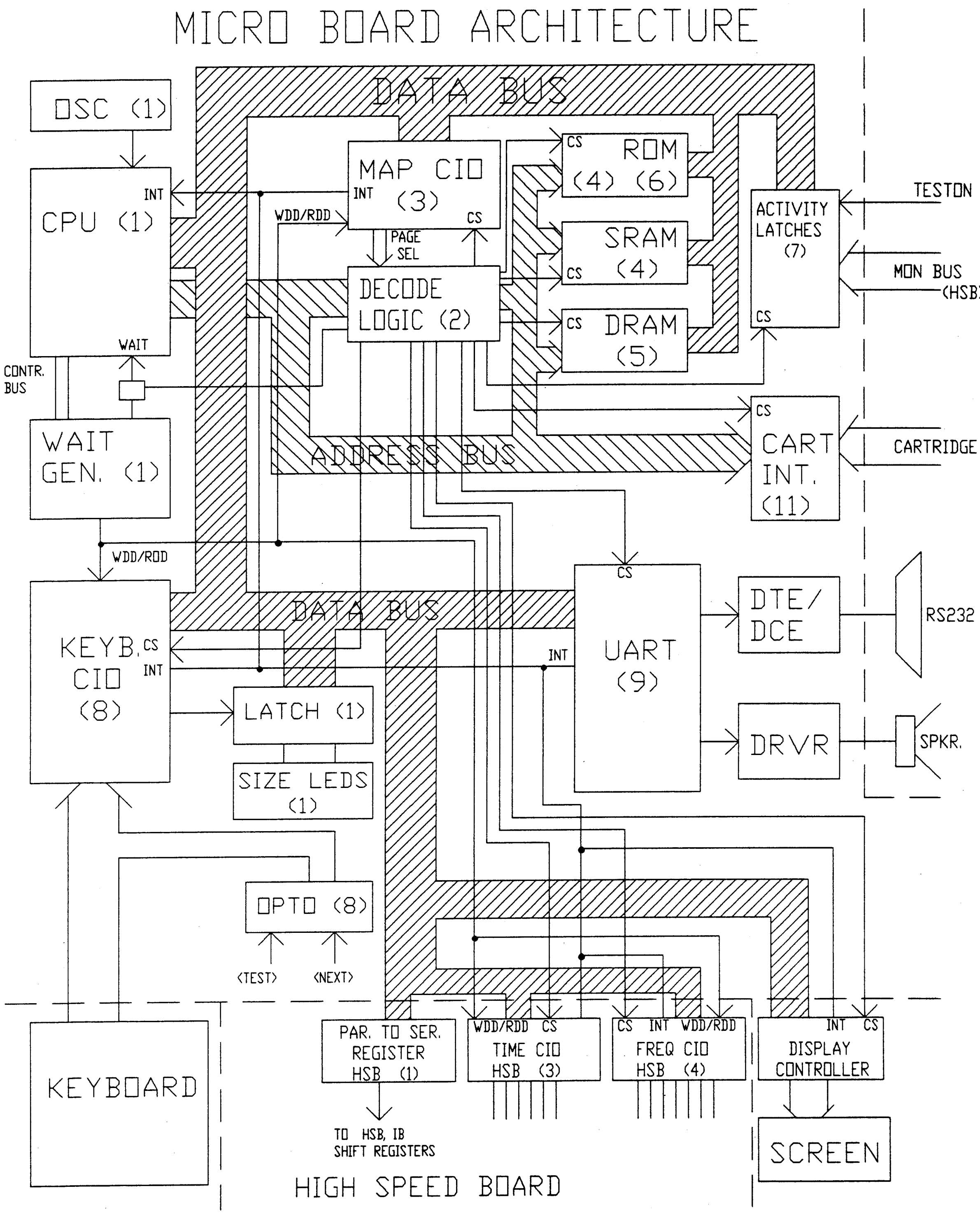
The Decode Logic consists of the PALs referred to previously and it generates chip selects for all peripheral devices and extends the 64K address range of the Z80 as shown in the memory map diagram.

The first 16K is the power on boot ROM space (ROM SYSAF is part of it). The next 8K of CPU address space is used to access 14 pages of 8K in size residing on the SYSAF and B ROMs. The next 8K starting at address 6000 accesses 14 pages residing on SYSC and D ROMs. The range 8000 to C000 is 16K of static RAM. The first RAM chip has a battery and retains the System Mode option parameters. It also has 8 pages of cartridge memory and 16 pages of library ROM. The final 16 K is overlayed with 4 pages comprising the DRAM and used for internal functions and 48K of ":SYST" sequences.



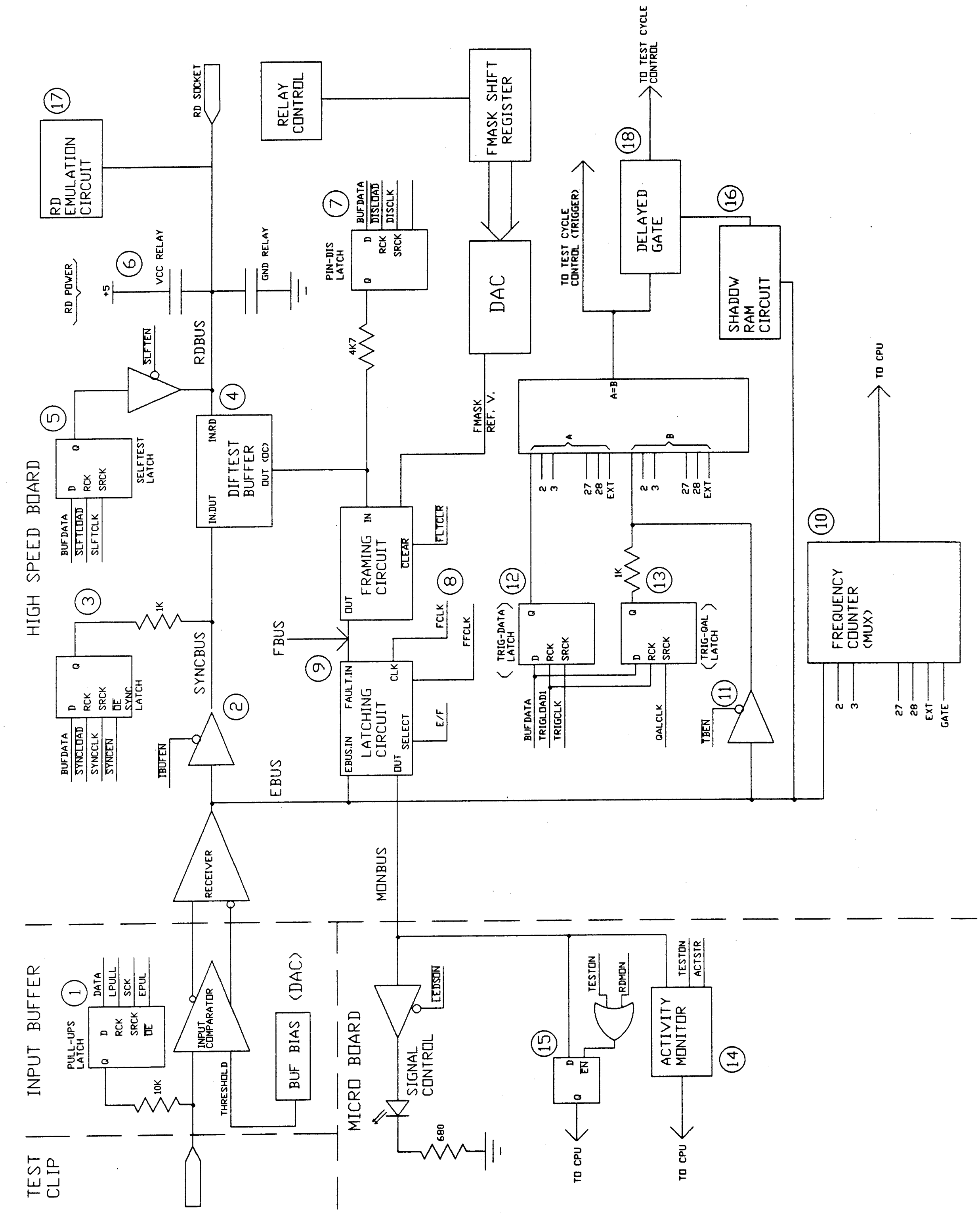
The Keyboard CIO outputs levels on port A which are read back on port B when a key is depressed. Three internal timers designated "watchdog", "key_time" and "key" take care of debouncing and repeating key actions. The TEST and NEXT keys found on the Interface Buffer are routed through the HSB and optocoupled on the MB to connect to the keyboard CIO. The chip size LEDs are driven by a latch controlled by this CIO.

The dual UART located at U11 is used for two functions. First, the serial RS232 interface is connected through a DTE/DCE selectable routing circuit so it can interface to various computers and printers. Second, various standard frequencies are generated to drive a speaker providing audible beep tones. The socket at U62 contains the battery and circuit for the real time clock function.


MICRO BOARD ARCHITECTURE
DATA BUS
OSC (1)
CPU (1)
INT
WAIT
CONTR. BUS
WAIT GEN. (1)
WDD/RDD
MAP CIO (3)
INT
CS
WDD/RDD
PAGE SEL
DECODE LOGIC (2)
CS
ROM (4) (6)
SRAM (4)
CS
CS
DRAM (5)
ACTIVITY LATCHES (7)
CS
TESTON
MON BUS (HSB)
CS
CART INT. (11)
CARTRIDGE
ADDRESS BUS
KEYB. CIO (8)
CS
INT
DATA BUS
LATCH (1)
SIZE LEDS (1)
OPTO (8)
(TEST)
(NEXT)
CS
UART (9)
INT
DTE/DCE
RS232
DRVR
SPKR.
KEYBOARD
PAR. TO SER. REGISTER HSB (1)
TO HSB, IB SHIFT REGISTERS
WDD/RDD CS
TIME CIO HSB (3)
CS INT WDD/RDD
FREQ CIO HSB (4)
INT CS
DISPLAY CONTROLLER
SCREEN
HIGH SPEED BOARD

2.4 High Speed Board

The accompanying diagram shows one channel routing a signal from the test clip through the Interface Buffer to the High Speed Board (H3) where it is processed by Dynamic Reference Comparison. The Micro Board then receives indicators from the H3 to display a test result. There are 28 such channels in parallel. The circuit elements that are depicted as latches in the diagram are implemented with shift registers that are first serial loaded, then clocked to a parallel output latch. The diagram's latches are single bits of a 28 bit shift register comprised of four cascaded 8 bit 74595s.


TEST CLIP
INPUT BUFFER
MICRO BOARD
HIGH SPEED BOARD
PULL-UPS LATCH
INPUT COMPARATOR
THRESHOLD
BUF BIAS (DAC)
RECEIVER
MONBUS
EBUS
SYNCBUS
RDBUS
FBUS
SYNC LATCH
SELFTEST LATCH
DIFTEST BUFFER
RD EMULATION CIRCUIT
RD POWER
VCC RELAY
GND RELAY
RD SOCKET
RELAY CONTROL
PIN-DIS LATCH
FMASK SHIFT REGISTER
DAC
FMASK REF. V.
FRAMING CIRCUIT
LATCHING CIRCUIT
TRIG-DATA LATCH
TRIG-QAL LATCH
DELAYED GATE
TO TEST CYCLE CONTROL
TO TEST CYCLE CONTROL (TRIGGER)
SHADOW RAM CIRCUIT
FREQUENCY COUNTER (MUX)
TO CPU
SIGNAL CONTROL
ACTIVITY MONITOR
A=B

The busses shown are as follows:

EBUS
External bus represents DUT signals after conversion to TTL levels using a single threshold in the IB. EBUS is labelled on pages 2, 4, 6, 8, 9, 10, 11 of the H3 schematics.

RDBUS
Reference device bus carries EBUS input pin signals to the RD socket and RD output pin signals to the DIFTEST circuit. RDBUS is labelled on pages 7, 8, 9, 10, 11 of the H3 schematics.

FBUS
Fault bus indicates on which pins the RDBUS and EBUS were different for longer than the FMASK value. The FBUS consists of the op amp output signals labelled Fxx on pages 8, 9, 10, 11 of the H3 schematics.

SYNCBUS
Synchronizing bus is either the EBUS or a pattern from the device library, depending on whether the Sync Vectors technique is employed to synchronize RD and DUT. The SYNCBUS consists of the 74244 output signals found on the extreme left side of pages 8, 9, 10, 11 of the H3 schematics.

MONBUS
Monitor bus is either the same as EBUS or FBUS, depending on which is selected for display on the monitor LEDs. The Mon bus may be found at connector J3 on the right side of pages 8, 9, 10, 11, of the H3 schematics and on page 13 of the MB schematics.

The 18 circuit blocks shown in the diagram on the previous page are the same ones listed across the top of the Selftest/Circuit Block Reference Table (Section 4.2). Fifteen of the blocks described below are found on the H3 Board.

1. Pullups Latch
On the Interface Buffer, signals from the test clips are pulled up to VCC or down to Gnd through a 10K resistor from the output of this shift register latch. It is found on page 1 of the IB schematic, U1, U2, U3, U4. The register at U24 of the IB drives a DAC which sets the threshold.

2. Inbuf
These buffers found on pages 8, 9, 10, 11, of the H3 schematics (U186, U140, U95, U42), feed the EBUS through to the SYNCBUS. They are tristated when the Sync Latch is driving.

3. Sync Latch
Synchronizing patterns from the library data are shifted into the registers shown on pages 8, 9, 10, 11, (U182, U136, U91, U45) and then latched to the output as a test vector. The stimulus for the RDTest function is provided in the same way.

4. Diftest Buffers
This circuit uses one of two possible resistor values (Hi or Lo) to determine whether the RDBUS can drive and therefore whether the pin is an output. The final output indicates the discrepancy between RDBUS and EBUS/SYNCBUS. It may be found at the outputs of the exclusive OR gates on pages 8, 9, 10, 11.

5. Self Test Latch
The shift register latch used to inject patterns onto the RDBUS during power-on verification in earlier revison boards is incorporated into the Logic Cell Array at U105, near the ZIF socket of the H3 Board. This is shown as circuit block 17 on the block diagram. If a RD is inserted during the power-on test an apparent failure will result.

6. RD Supply Relays
Certain ZIF socket pins are connected to VCC or Gnd by closure of the relays shown on page 7. The shift registers U155 and U102 control their selection.

7. Pin Dis Latch
These shift register latches can override the fault indication output from the Diftest circuit to ignore a fault on a pin. They are shown on pages 8, 9, 10, 11, as U180, U134, U89, U40.

8. FFCLK Line
The CPU can simulate a fault by asserting this line which is ORed with the pin fault lines to produce FLTS, the master fault indicator (page 11, A-10). Shift register U67 (page 3) provides data to a DAC which provides the FMASK reference voltage used in the framing circuit. The charging of precision capacitors to this voltage establishes an FMASK value. Note that the 74ALS09s driving the capacitors are specially prescreened to be uniform.

9. Mon Mux
The latches at U198, U153, U112, U64 hold the individual pin faults. The PALs driving them are also latches which accumulate faults for 40 ns after the first line fails but no further. In this way, the results are frozen in a window around the first fail for later reading by the CPU over the Mon Bus. When no faults are present, the signal M/F selects U164, U122, U76, U43 (pages 8, 9, 10, 11) to route the EBUS onto the MONBUS.

10. Freq Circuit
The 8536 CIO at U27 (page 4) controls the multiplexing and measurement of signal frequency among the 29 channels (28 pins plus 1 external). Port A is configured as output and used to drive the muxes at U55, U66, U124, U141. Port B drives the FREQ PAL except for PB5 which is an input flagging the occurrence of Gate. Port C is an input to read the frequency count.

11. Trig Buf
These buffers U191, U154, U98, U81 on page 2 enable the EBUS to the trigger comparator when TBEN signal is active.

12. Trig Data Latch
The shift register latches U166, U189, U100, U78 are loaded with data indicating 1s and 0s of the Trigger word. The first word is serial shifted and latched followed by the second word which is not latched until the occurrence of the first.

13. Trig Qual Latch
The shift register latches at U168, U188, U96, U56 are loaded with data indicating which pins have a 1 or 0 and which have "don't care" conditions. Two successive words are loaded as in the Trig Data case.

14. Activity Circuit
This circuit on page 7 of the Micro Board schematics operates by latching the state of all pins at the start of test and generating an exclusive OR pulse if the state ever changes. In this way, the PALs U32, U21, U16, U22 are alerted of active pins.

15. Mon Bus Readback
The Mon Bus which comes from the High Speed Board to the Micro Board via the connector J3 is shown on page 13 of the MB schematics. The latches and PALs on page 7 use the Mon Bus to hold the state of all pins at the end of test (for the EoT test result). The state of pins at the start of test is also latched here for the purpose of checking H or L conditions on DUT pins.

16, 18. Shadow Ram and Delayed Gate Circuit
This circuit is implemented in the Logic Cell Array at U123 (page 6) and associated PALs. Both of these functions affect the gating of comparison. Shadow RAM inhibits comparison during reading of an uninitialized DUT memory cell. Delayed gate inhibits the normal gate signal from going true for a fixed time interval after its pin conditions are satisfied.

17. RD Emulation Circuit
This Logic Cell Array, located at U105 (page 12), simulates certain Reference Devices instead of using an RD in the socket. If an H3 Board does not have the Simulation Option installed, U105 is still present to perform selftest functions.

Test cycle control is applied to all 28 channels together and is found on page 3 of the H3 schematics. The Time CIO at U26 is configured so PA0, 1,2 enable the Trigger flip flops and GATE PAL. PA3 is an output for enabling comparison during selftest. PA4 is an input that detects whether gate occurred. PA5 is an input indicating a short in the RD socket. PA6, 7 are inputs that detect whether trigger word 1 and 2 occurred.

Port B controls the Test Cycle PAL; PB1 is an input which stops test after a fault has been captured. PB2, 3, 4, 5 are inputs from a counter which acts as a prescaler for the time-to-fault interval. An internal CIO timer converts it to a value in the proper range. PB6 is an output that clears the fault under CPU control, while PB7 is an input indicating a fault is present. Port C is configured as an output and it selects which shift register will receive the data stream from the register U36 on page 1 of the H3 schematics.

2.5 Test Clips

The standard Test Clips have no active components, but the ribbon cable is terminated at both ends with a series 300 ohm resistor for impedance matching. There are 10 Kohm pullup resistors in the Interface Buffer which are applied to the DUT through the 600 ohms of the Test Clip.

The High Impedence Test Clip has an active buffer at the clip head which presents 500 Kohm impedence to the DUT. The clip head is powered from the VCC pin of the DUT.

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3 Selftest

3.1 Reading Selftest Results

Immediately after poweron, the tester executes a series of selftests that take about one minute. The selftests may also be initiated at any time by simultaneously pressing CNTR and ESC. The tests are numbered 0 to 55 and all but a few are run automatically. These few plus a number of "extended tests" denoted by Exx (eg. E60), can be run by manually keying them in when analyzing a problem. All the tests may be run individually in this way to produce "individual test results".

When a failure is encountered during poweron selftest, two rows of digits display "general results" and sometimes a third and fourth row appear. Rows 1 and 2 indicate the failing test numbers; rows 3 and 4 indicate fault flags that are tied to memory and shift registers. Flag failures indicate major functional problems and general test results indicate which tests are failing. "Individual test results" are more detailed dispays of the failing tests and they indicate which channels (lines) are faulty.

In cases where a failure is severe and the LCD screen may not function, the LEDs around the ZIF socket may indicate the problem.

Hardware and software problems occasionally result in system crashes that present a message on the command line. One cause of such a crash is a corrupted simulation library file. A summary of these messages appears in Section 3.4 .

3.1.1 General Selftest Results

The general results on the first two lines are clustered in groups of five as shown in the example below. The test numbers are shown above and below the digits. 0 indicates Pass, 1 indicates Fail and X indicates that a test result is not available.

```
  0-4    5-9   10-14  15-19  20-24  25-29

X0000  00000  11111  00000  00000  0XX11
00000  01000  00011  XXX11  11100  XXXXX

30-34  35-39  40-44  45-49  50-54  55-59
```

The cross reference of test numbers to test names is listed below:

0	SLFT_CLIP	29	FM40_FLT
1	PULL0_MON	30	FM40_NFLT
2	PULL1_MON	31	FM80_FLT
3	PULL0_FLT	32	FM80_NFLT
4	PULL1_FLT	33	FM120_FLT
5	SYNC0_Hres_FLT	34	FM120_NFLT
6	SYNC1_Hres_FLT	35	FM160_FLT
7	SYNC0_Lres_FLT	36	FM160_NFLT
8	SYNC1_Lres_FLT	37	FM200_FLT
9	PINDIS0_FLT	38	FM200_NFLT
10	PINDIS1_FLT	39	FM240_FLT
11	SLFTST0_FLT	40	FM240_NFLT
12	SLFTST1_FLT	41	ACT_DIS_CLR
13	VccON_FLT	42	PULL0_ACT_TSTON
14	GndON_FLT	43	PULL1_ACT_TSTON
15	PULLPOS_FREQ	44	PULL0_ACT_ACTSTR
16	TRIGQAL0_EQUAL	45	PULL1_ACT_ACTSTR
17	TRIGQAL1_EQUAL	46	FREQ_BIAS_SHORT
18	QAL0_EQUAL	47	FREQ_BIAS_LONG
19	QAL1_EQUAL	48	KEYBOARD_OPEN
20	TRIG0_EQUAL	49	TEST_CYCLE
21	TRIG1_EQUAL	50	UART_TEST
22	PULL0_TRIG_EQUAL	51	DGATE_TEST
23	PULL1_TRIG_EQUAL	52	PULL0_XTRIG
24	PULL0_TRIGQAL	53	PULL1_XTRIG
25	FM_STAT_NFLT	54	PULL_XEVENT
26	FM_STAT_FLT	55	SHAD_INIT
27	FMASK_WB_TEST		
28	FMASK_CAL		

Tests 0, 47 and 50 are not automatically run during the poweron selftest, but can be run by themselves explicitly. This is also the case for a group of tests known as "engineering" or "extended" tests which are designated Exx as follows:

E60	WALK_SIZELEDS
E61	TEST_MEMORY
E62	WALK_MONLEDS
E63	UPDATE_VCC_LIM
E64	SHAD_ADDR
E70	KEY_CLOSURE
E71	DISP_RAM
E74	DISP_CHAR_SET
E75	CART_SLFT
E76	TEST_C_ENG
E77	ACT_CROSS
E78	TRG_CROSS
E79	FRQ_CROSS
E80	FLT_CROSS

3.1.2 Flag Results

Flags may appear on lines 3 and 4 of the general results screen. A 0 means "OK" and a 1 means "fault". At the present time, only the first row is used.

```
          BYTE0      BYTE1      BYTE2      BYTE3
            |          |          |          |
        00000000   00000000   00000000   00000000
        00000000   00000000   00000000   00000000
        ||||||||
   BIT: 76543210
```

BYTE0: Indicates DRAM chip which failed memory test

B7: U86
B6: U82
B5: U87
B4: U83
B3: U88
B2: U84
B1: U89
B0: U85

BYTE1: Indicates shift register bank which failed
- B7: INTERFACE BUFFER (IB U1,U2,U3,U4)
- B6: DELAYED GATE
- B5: SELFTEST (HSB U38,U76,U115,U150)
- B4: FMASK (HSB U72)
- B3: TRIGGER QUALIFIER (HSB U57,U87,U142,U162)
- B2: TRIGGER DATA (HSB U66,U91,U140,U163)
- B1: PIN DISABLE (HSB U41,U80,U119,U154)
- B0: SYNC (HSB U46,U82,U121,U156)

BYTE2: General
- B7: NVRAM bad
- B6: NVRAM checksum error, rewritten with default data
- B5: Not used
- B4: Not used
- B3: ROM bad (U77)
- B2: ROM bad (U76)
- B1: ROM bad (U75)
- B0: ROM bad (U74)

BYTE3: General
- B7,6,5,4: Not used
- B3: FMASK calibration error
- B2: Threshold calibration error
- B1: FLTS line not readable
- B0: Threshold setting error

3.1.3 Chip Size LED Error Codes

If selftest fails, on rare occasions, the chip size LEDs may light to indicate an error. In the list below, the 8 LEDs are shown with a 0 for unlighted and a 1 for lighted.

00000001: KEYBOARD CIO PortA. CPU cannot communicate.
00000010: KEYBOARD CIO PortB
00000011: TIME CIO PortA
00000100: TIME CIO PortB
00000101: FREQ CIO PortA
00000110: FREQ CIO PortB
00000111: Display not ready
00001000: ROM checksum error
00001001: SRAM error
00001010: Stack underflow
00001011: Unimplemented interrupt occurred
00001100: Invalid interrupt vector
00001101: Not used
00001110: Incorrect peripheral serviced
00001111: UART transmit error
00010000: UART other errors (special receive conditions)
00010001: UART parity error
00010010: DRAM error
00010011: Overlay error
00010100: Not used
00010101: MAP CIO PortA
00010110: MAP CIO PortB
00010111: Display memory error

3.2 Running and Reading Individual Selftests

The individual selftest results indicate which specific lines or channels are failing. A full printout of all failing individual results may be printed out as explained in Section 1.2. Alternatively, a single individual result may be viewed on the display by pressing the following keys after the general poweron selftest fails: F3(debug) F2(display) "test #" ENTER. The individual result then appears as four bytes with a 1 indicating a problem.

```
        BYTE0     BYTE1     BYTE2     BYTE3
          |         |         |         |
       00000000  00000000  00000000  00000000
  BIT: 76543210  76543210  76543210  76543210
```

BYTE0	BYTE1	BYTE2	BYTE3
b7: X	b7: PIN 3	b7: PIN 7	b7: PIN 11
b6: X	b6: PIN 26	b6: PIN 22	b6: PIN 18
b5: X	b5: PIN 4	b5: PIN 8	b5: PIN 12
b4: EXT LEAD	b4: PIN 25	b4: PIN 21	b4: PIN 17
b3: PIN 1	b3: PIN 5	b3: PIN 9	b3: PIN 13
b2: PIN 28	b2: PIN 24	b2: PIN 20	b2: PIN 16
b1: PIN 2	b1: PIN 6	b1: PIN 10	b1: PIN 14
b0: PIN 27	b0: PIN 23	b0: PIN 19	b0: PIN 15

Refer to the individual descriptions of Section 3.3 for any bit assignments that may differ from those generally used above. In particular, bits 5,6,7 of BYTE 0, which are not used for most tests, may have a meaning which is noted for a specific test.

3.3 Individual Selftest Descriptions

TEST 0
SLFT_CLIP

The SLFT_CLIP routine is used for verifying test clips. The test clip in question is inserted into the Interface Buffer and the other end is inserted into the ZIF RD socket via the Test Clip Verification Module. When the test is running, the size of the current test clip is displayed. The failure information is displayed as follows (Only special bits are shown, all others refer to regular pin number):

BYTE 0 -	B7 -	Not used
	B6 -	Not used
	B5 -	Clip size code invalid
	B4 -	Frequency reading invalid

TESTS 1,2
PULL0_MON, PULL1_MON

These tests supply a walking 0 or 1 across all lines from the pull-ups latch, through the input buffer, to the MONBUS where the levels are read by the CPU.

TESTS 3,4
PULL0_FLT, PULL1_FLT

These tests supply a walking 0 or 1 across all lines from the pull-ups latch, through the input buffer, through the fault circuitry to the MONBUS where the levels are read by the CPU.

TESTS 5,6
SYNC0_Hres_FLT, SYNC1_Hres_FLT

These tests supply a walking 0 or 1 across all lines from the sync latch, through the HI resistors, through the fault circuitry to the MONBUS where the levels are read by the CPU.

TESTS 7,8
SYNC0_Lres_FLT, SYNC1_Lres_FLT

These tests supply a walking 0 or 1 across all lines from the sync latch, through the LO resistors, through the fault circuitry to the MONBUS where the levels are read by the CPU.

TESTS 9,10
PINDIS0_FLT, PINDIS1_FLT

These tests supply a walking 0 or 1 across all lines from the pin disabling latch, through the fault circuitry to the MONBUS where the levels are read by the CPU.

TESTS 11,12
SLFTST0_FLT, SLFTST1_FLT

These tests supply a walking 0 or 1 across all lines from the selftest latch, through the fault circuitry to the MONBUS where the levels are read by the CPU.

TESTS 13,14
VccON_FLT, GndON_FLT

These tests walk the Vcc or Gnd relays on. Their operation is verified through the fault circuitry to the MONBUS where the levels are read by the CPU.

TEST 15
PULLPOS_FREQ

This test walks a positive pulse through the pull-ups latch to the frequency circuitry.

TESTS 16,17
TRIGQAL0_EQUAL, TRIGQAL1_EQUAL

These tests walk a 0 or a 1 through the trigger and qualifier latches and the results are determined through reading the EQUAL line.

TESTS 18,19
QAL0_EQUAL, QAL1_EQUAL

These tests walk a 0 or a 1 through the qualifier latches and the results are determined through reading the EQUAL line.

NOTE: For tests 18 and 19, an X in the general test result means that individual results are unavailable.

TESTS 20,21
TRIG0_EQUAL, TRIG1_EQUAL

These tests walk a 0 or a 1 through the trigger latches and the results are determined through reading the EQUAL line.

NOTE: For tests 20 and 21, an X in the general test result means that individual results are unavailable.

TESTS 22,23
PULL0_TRIG_EQUAL, PULL1_TRIG_EQUAL

These tests walk a 0 or a 1 through the pull-ups latches, through the trigger circuitry and are read through the EQUAL line.

NOTE: For tests 22 and 23, an X in the general test result means that individual results are unavailable.

TEST 24
PULL0_TRIGQAL

This test walks a 0 through the pull-ups latches, through the trigger and qualifier circuitry and the results are determined through reading the EQUAL line.

NOTE: For test 24, an X in the general test result means that individual results are unavailable.

TESTS 25,26
FM_STAT_NFLT, FM_STAT_FLT

These tests perform a static FMASK test. All lines are expected to pass for the "_NFLT" test while all lines are expected to fail for the "FLT" test.

TEST 27
FMASK_WB_TEST

This test does an approximate test using fixed values for FMASK. It uses a tolerance three times that of the FMxx tests. This test is performed to determine whether or not the FMASK curve is within a very wide margin.

TEST 28
FMASK_CAL

This routine determines the calibration values to be used by FMASK.

TESTS 29,31,33,35,37,39
FMxx_FLT

These tests use a pulse of fixed duration (40, 80, 120, 160, 200 and 240ns) and set FMASK to just below the duration of the pulse. All lines are expected to produce a fault. Those which do not are flagged as faulty.

TESTS 30,32,34,36,38,40
FMxx_NFLT

These tests use a pulse of fixed duration (40, 80, 120, 160, 200 and 240ns) and set FMASK to just above the duration of the pulse. All lines are expected to produce no fault. Those which do are flagged as faulty.

TEST 41
ACT_DIS_CLR

This test checks the disabling and clearing functions of the activity circuitry. It disables the activity circuit and pulses all lines. Any lines which indicate activity are flagged as faulty. It also verifies that the activity latches may be cleared and that a single edge on all lines produces a 1 (activity occurred) in all latches.

The bits in the results indicate normal pin numbers with the exception of the following:

BYTE 0 -	B7 -	N/U
	B6 -	N/U
	B5 -	Could not clear PAL latches.
	B4 -	Could not activate all lines with a single edge.

TESTS 42,43
PULL0_ACT_TSTON, PULL1_ACT_TSTON

These tests walk a rising edge(1) or a falling edge(0) from the pull-ups latches through the activity circuitry. The activity circuit is controlled by the TSTON signal.

TESTS 44, 45
PULL0_ACT_ACTSTR, PULL1_ACT_ACTSTR

These tests walk a rising edge(1) or a falling edge(0) from the pull-ups latches through the activity circuitry. The activity circuit is controlled by the ACTSTR signal.

TESTS 46,47
FREQ_BIAS_SHORT, FREQ_BIAS_LONG

These two tests are almost identical, the only difference being that the long test verifies all possible values of threshold and the short test only tests at 1 volt increments. The tests are a collection of several subtests involving frequency and threshold hardware on the High Speed Board and Input Buffer and they are detailed below. As they are being done, the left part of the screen shows timing values from the frequency test and the right side of the screen shows the highest and lowest differences between expected and measured voltage values.

Many of the subtests require that a voltage on the Interface Buffer be measured. One of several possible voltages is selected using the analog mux on the input buffer. This feeds the into the VCO, the output of which is sent to the High Speed Board where the frequency is measured. The same thing is also done for 0 volts and 2.5 volts to obtain a calibration ratio that is used to determine the exact voltage of the signal selected.

Interface Buffer shift register subtest

This tests to see if data can be shifted through the shift registers on the Interface Buffer correctly. There are two banks of registers on the board. Only the pullup registers are explicitly tested because there is no feedback line from the threshold registers. The threshold registers are implicitly tested by the other tests. The test procedure is as follows:

a) shift data - msbit = 0
b) read the voltage of the msbit: must be <2V
c) shift data - msbit = 1
d) read the voltage of the msbit: must be >2V

If this test fails it does not set one of the data bits but rather sets the shifting error flag.

Frequency HW subtest

The frequency hardware tested is on the High Speed Board. It can be configured in several different ways (the setup for this is shown in the MODE box on the schematic), all of which are independently tested.

1. Read a frequency. A 25MHz clock is generated and the frequency is measured.
2. Read the period. Pin #2 is selected through the frequency mux (this hardware is tested in a different selftest). It is setup to read the period and then the CPU generates a cycle of fixed duration on this line using the pullup registers on the Interface Buffer. The period displayed should be approximately 990 us.
3. Read the high time and low time. These are done in the same way as the period test except the times are displayed. Low time should be approximately 815 us and high time 175 us.

Threshold HW subtest

This subtest programs a value of threshold and reads it back to verify that it is within an acceptable range. The variation between the measured value and the value programmed (in mV) is displayed on the screen. The long test goes through all possible settings between 0 and 5 volts and the short test only goes in steps of 1 volt.

After the threshold setting has been tested the threshold is calibrated to compensate for input offsets in the comparators. The pullups are used to set the actual threshold on the input to the comparator to 4.16 and 0 volts and then the threshold is adjusted to see what offset added to the amount programmed (4.2 and 0 volts) will be closest to the actual threshold of the comparators. If the adjustment exceeds an allowable amount the calibration part of this test will fail.

Reset HW subtest

For this subtest the reset relays are set so that power for reset comes from 5 volts and the output is fed into the analog mux.
a) reset = high: must be > 4 volts
b) reset = low: must be < 1 volt
c) reset = off: must be < 4 volts & > 1 volt

Result bytes:

BYTE 0

b7 -	0
b6 -	0
b5 -	0
b4 -	0
b3 -	Threshold calibration failed. Ignore this bit unless the other bits in this byte are clear. If they are clear and this bit fails the output of the threshold Op Amp has too great an offset.
b2 -	Unable to complete test. Something is wrong with the CPU - CIO interface.
b1 -	The threshold was too high. The output of the Op Amp was greater than expected by more than the allowable amount.
b0 -	The threshold was too low. The output of the Op Amp was less than expected by more than the allowable amount.

BYTE 1

b7 -	Vcc(IB) is too high (> 5.2V). The main Vcc voltage as read at the Interface Buffer is too high. If this test fails, <u>ALL</u> other selftests are invalid.
b6 -	Vcc(IB) is too low (< 4.84V). The main Vcc voltage as read at the Interface Buffer is too low. If this test fails <u>ALL</u> other selftests are invalid.
b5 -	0
b4 -	0
b3 -	0
b2 -	Unable to turn off the reset line. The reset output from the Interface Buffer could not be made to go tri-state.
b1 -	Unable to drive the reset line low. The reset output from the Interface Buffer could not be made to go low.
b0 -	Unable to drive the reset line high. The reset output from the Interface Buffer could not be made to go high.

BYTE 2

b7 -	Period measured was too long. There are several possible causes. The 25MHz crystal could be oscillating at the wrong frequency, the WSG pal could be faulty, almost any of the 4 frequency chips could be bad.
b6 -	Period measured was too short. There are several possible causes. The 25MHz crystal could be oscillating at the wrong frequency, the WSG pal could be faulty, almost any of the 4 frequency chips could be bad.
b5 -	No results obtained from period read. The test has timed out. Something is wrong with the CPU - CIO interface.
b4 -	Unable to set up the period read. Something is wrong with the CPU - CIO interface.
b3 -	HW oscillator (25MHz) is too fast. There are several possible causes. The 25MHz crystal could be oscillating at the wrong frequency, almost any of the 4 frequency chips could be bad, the 2925 clock generator could be bad, there could be a problem in the frequency muxes.

b2 - HW oscillator (25MHz) is too slow. There are several possible causes. The 25MHz crystal could be oscillating at the wrong frequency, almost any of the 4 frequency chips could be bad, the 2925 clock generator could be bad, there could be a problem in the frequency muxes.

b1 - No results obtained from freq read. The test has timed out. Something is wrong with the CPU - CIO interface.

b0 - Unable to set up the frequency read. Something is wrong with the CPU - CIO interface.

BYTE 3

b7 - The active low duty cycle measured was too long. There are several possible causes. The 25MHz crystal could be oscillating at the wrong frequency, almost any of the 4 frequency chips could be bad, the WSG pal could be faulty, the 2925 clock generator could be bad, there could be a problem in the frequency muxes.

b6 - The active low duty cycle measured was too short. There are several possible causes. The 25MHz crystal could be oscillating at the wrong frequency, almost any of the 4 frequency chips could be bad, the WSG pal could be faulty, the 2925 clock generator could be bad, there could be a problem in the frequency muxes.

b5 - No results obtained from low read. The test has timed out. Something is wrong with the CPU - CIO interface.

b4 - Unable to set up the low read. Something is wrong with the CPU - CIO interface.

b3 - The active high duty cycle measured was too long. There are several possible causes. The 25MHz crystal could be oscillating at the wrong frequency, almost any of the 4 frequency chips could be bad, the WSG pal could be faulty, the 2925 clock generator could be bad, there could be a problem in the frequency muxes.

b2 - The active high duty cycle measured was too short. There are several possible causes. The 25MHz crystal could be oscillating at the wrong frequency, almost any of the 4 frequency chips could be bad, the WSG pal could be faulty, the 2925 clock generator could be bad, there could be a problem in the frequency muxes.

b1 - No results obtained from high read. The test has timed out. Something is wrong with the CPU - CIO interface.

b0 - Unable to setup the high read. Something is wrong with the CPU - CIO interface.

TEST 48
KEYBOARD_OPEN

This test verifies that all keys are in the open state including the keys on the buffer. The last two bytes of the individual test result will contain two set bits which may be interpreted from the following matrix to identify the key that was depressed.

KEYBOARD MATRIX

```
byte   3--> b7     b6     b5     b4      b3      b2      b1      b0
  2
  |     J4|  16 |  15 |  14 |  13  |  12  |  11  |  10  |  9
  V     ---+-----+-----+-----+------+------+------+------+---
 b0      1 |   G |   A | ESC | SHFT | CNTR |   Y  |   S  |  M
        ---+-----+-----+-----+------+------+------+------+---
 b1      2 |   I |   C |  F2 |space | < ,  | = +  |   U  |  O
        ---+-----+-----+-----+------+------+------+------+---
 b2      3 |   K |   E |  F5 |BoL<- |PgUp ^| : ;  |   W  |  Q
        ---+-----+-----+-----+------+------+------+------+---
 b3      4 |   L |   F |  F4 |EoL-> |PgDn v| ? _  |   X  |  R
        ---+-----+-----+-----+------+------+------+------+---
 b4      5 | # 3 | ! 1 | ETC |ENTER |spare1| ( 9  | & 7  | %5
        ---+-----+-----+-----+------+------+------+------+---
 b5      6 | $ 4 | @ 2 |NEXT |TEST  |spare2| ) 0  | * 8  | "6
        ---+-----+-----+-----+------+------+------+------+---
 b6      7 |   J |   D |  F3 |spare3| > .  | / -  |   V  |  P
        ---+-----+-----+-----+------+------+------+------+---
 b7      8 |   H |   B |  F1 | CE   ||<-->||   Z  |   T  |  N
        ---+-----+-----+-----+------+------+------+------+---
```

TEST 49
TEST_CYCLE

This test verifies that:
- the following lines are not broken or shorted:
  - /SYNCEN
  - /SHORT interrupt line
  - /RELEN
- the following timers are good:
  - Test time timer
  - 10 ms system timer
  - 1 ms free running timer
- gate and trigger work properly

/SHORT is checked to see if the line is high (ie. not shorted to ground). /SYNCEN and /RELEN are tested by having sync latches or relays cause a fault and verifying that the fault occurred.

Four bytes of test results are presented:
BYTE 0

b7 thru 5 - 0 (not used)
b4 - /STRFRQ output of TC PAL not working
b3 - Interrupts failed
b2 - /SYNCEN line test failed
b1 - /SHORT test failed
b0 - /RELEN test failed
NOTE: only interrupts generated by TIME port are tested.

BYTE 1

b7 thru 3 - 0 (not used)
b2 - test time timer
b1 - 10 ms timer
b0 - 1 ms timer

Each bit in bytes 2 and 3 corresponds to one execution of the test cycle, set up to produce the expected results. If any bit in bytes 2 or 3 is set it means that results were not as expected. For example, if b6 in byte 2 is set it means that the gate function was observed to be not active or faults were detected. Trigger is programmed with one word (level) in byte 2 trigger test; for byte 3, trigger is programmed with two words (edge). For all W2 related tests (byte 3 bits 3 thru 0), W1 always occurs.

BYTE 2

b7 - gate did not occur no faults
b6 - gate occurred no faults
b5 - gate did not occur, faults
b4 - gate occurred, faults
b3 - trigger did not occur, no faults
b2 - trigger occurred, no fault
b1 - trigger did not occur, faults
b0 - trigger occurred, faults

BYTE 3

b7 - trigger W1 did not occur, no faults
b6 - trigger W1 occurred, no faults
b5 - trigger W1 did not occur, faults
b4 - trigger W1 occurred, faults
b3 - trigger W2 did not occur, no faults
b2 - trigger W2 occurred, no faults
b1 - trigger W2 did not occur, faults
b0 - trigger W2 occurred, faults

TEST 50
UART_TEST

The RSCNT3, RSCNT2, and RSCNT1 lines on the Micro Board control the configuration of the rs232 port (DTE,DCE). These lines are put into a normally illegal state that allows the outputs of the UART to be fed into the inputs. This can be done in two ways and all tests are done in both configurations.

There are two tests: the first tests the control lines (DTR, CTS, ...) and the second transmits data between the transmitter and receiver. The second test is not done if the first fails.

1. Test the control lines (byte 2 & 3 results). Each of the control lines is tested with the other control line in a fixed state, first high then tested again with it low. At the top of the results for each byte the setting of the configuration lines is shown. For each test the state of the state of the two output control lines is shown as well as the input line and what state is expected on it.

2. Test the data lines. This test is NOT done unless test 1 passes. The baud rate is programmed to 9600 regardless of the setting of the rs232 port. At the end of the test it is reprogrammed with the correct value. A small block of data is sent and compared with what was received. The receiving of data is interrupt driven so that this test may fail if there is something wrong with this part of the board. The setting of the configuration lines is shown for each test.

RESULT BYTES

BYTE 0 = all bits 0

BYTE 1
b7 - 0
b6 - 0
b5 - 0
b4 - 0
b3 - 0
b2 - 0
b1 - 1 if serial data test failed with RSCNT[3,2,1]=001
b0 - 1 if serial data test failed with RSCNT[3,2,1]=110

NOTE RSCNT[3,2,1] means that control signals RSCNT3, RSCNT2, RSCNT1 to U1, U2, U7 on the Micro Board (page 9 of schematics) were held in the states shown during the test.

BYTE 2 - RSCNT[3,2,1] = 001
b7 - DTR=0, RTS=1, test for CTS=1
b6 - DTR=0, RTS=0, test for CTS=0
b5 - DTR=1, RTS=1, test for CTS=1
b4 - DTR=1, RTS=0, test for CTS=0
b3 - DTR=0, RTS=0, test for DCD=0
b2 - DTR=1, RTS=0, test for DCD=1
b1 - DTR=0, RTS=1, test for DCD=0
b0 - DTR=1, RTS=1, test for DCD=1

BYTE 3 - RSCNT[3,2,1] = 110
b7 - DTR=0, RTS=1, test for CTS=1
b6 - DTR=0, RTS=0, test for CTS=0
b5 - DTR=1, RTS=1, test for CTS=1
b4 - DTR=1, RTS=0, test for CTS=0
b3 - DTR=0, RTS=0, test for DCD=0
b2 - DTR=1, RTS=0, test for DCD=1
b1 - DTR=0, RTS=1, test for DCD=0
b0 - DTR=1, RTS=1, test for DCD=1

TEST 51
DGATE_TEST

This test is performed only if the Simulation Option (900-001) is installed. It verifies the functionality of the delayed-gate circuit. It checks the operation of the pre-scaler, the delay function, the duration function and the delayed-gate-activity circuit. Results are interpreted as follows:

	B7	B6	B5	B4	B3	B2	B1	B0
BYTE0	0	0	DGATE ACT	DGATE CLR	INF DUR	0 DELAY	PRE-SCALER	INVERT FAIL
BYTE1	/15 1.667M	/14 1.786M	/12 2.083M	/10 2.5M	/8 3.125M	/6 4.17M	/4 6.25M	/2 12.5M
BYTE2	D 128	U 64	R 32	A 16	T 8	I 4	O 2	N 1
BYTE3	128	D 64	E 32	L 16	A 8	Y 4	2	1

INVERT FAIL - Could not invert gate signal.

PRE-SCALER - A division factor other than one in BYTE 1 failed.

0 DELAY - The test for bypassing the delayed gate circuit failed

INF. DUR. - The test for infinite duration failed (Duration prematurely terminated.

DGATE ACT - The dgate activity latch failed to register activity.

DGATE CLR - The dgate activity latch was not cleared by TESTSTR.

Note: While this test is running in "looping" mode, the expected values and the measured results are displayed continuously on-screen in the following format (NOTE: The NEXT key advances to the next part of the test):

	Expected Minimum	Measured Value	Expected Maximum
For Example:	140.00 n	160.00 n	180.00 n

Sequence of results during test:

Message #	Minimum	Measured	Maximum	Circuitry Tested
#1	24.950 M	25.000 M	25.050 M	Prescaler - divide by 1
#2	12.450 M	12.500 M	12.550 M	Prescaler - divide by 2
#3	8.2833 M	8.3333 M	8.3833 M	Prescaler - divide by 3
#4	6.2000 M	6.2500 M	6.3000 M	Prescaler - divide by 4
#5	4.9500 M	5.0000 M	5.0500 M	Prescaler - divide by 5
#6	4.1167 M	4.1667 M	4.2167 M	Prescaler - divide by 6
#7	3.5214 M	3.5714 M	3.6214 M	Prescaler - divide by 7
#8	3.0750 M	3.1250 M	3.1750 M	Prescaler - divide by 8
#9	2.7278 M	2.7778 M	2.8278 M	Prescaler - divide by 9
#10	2.4500 M	2.5000 M	2.5500 M	Prescaler - divide by 10
#11	2.2227 M	2.2727 M	2.3227 M	Prescaler - divide by 11
#12	2.0333 M	2.0833 M	2.1333 M	Prescaler - divide by 12
#13	1.8731 M	1.9231 M	1.9731 M	Prescaler - divide by 13
#14	1.7357 M	1.7857 M	1.8357 M	Prescaler - divide by 14
#15	1.6167 M	1.6667 M	1.7167 M	Prescaler - divide by 15

#16	79.000 n	120.00 n	161.00 n	Duration - Bit0
#17	199.00 n	240.00 n	281.00 n	Duration - Bit1
#18	439.00 n	480.00 n	521.00 n	Duration - Bit2
#19	919.00 n	960.00 n	1.0010 u	Duration - Bit3
#20	1.8790 u	1.9200 u	1.9610 u	Duration - Bit4
#21	3.7990 u	3.8400 u	3.8810 u	Duration - Bit5
#22	7.6390 u	7.6800 u	7.7210 u	Duration - Bit6
#23	15.319 u	15.360 u	15.401 u	Duration - Bit7
#24	119.00 n	120.00 n	241.00 n	Delay - Bit0
#25	239.00 n	240.00 n	361.00 n	Delay - Bit1
#26	479.00 n	480.00 n	601.00 n	Delay - Bit2
#27	959.00 n	960.00 n	1.0810 u	Delay - Bit3
#28	1.9190 u	1.9200 u	2.0410 u	Delay - Bit4
#29	3.8390 u	3.8400 u	3.9610 u	Delay - Bit5
#30	7.6790 u	7.6800 u	7.7610 u	Delay - Bit6
#31	15.359 u	15.360 u	15.441 u	Delay - Bit7
#32	79.000 n	120.00 n	201.00 n	DGATE Inversion Test
#33	229.00 n	320.00 n	401.00 n	DGATE Infinite Duration Test

TEST 52
PULLO_XTRIG

If the Simulation Option (900-001) is installed, this test verifies the operation of the trigger circuit inside the shadow RAM ASIC chip configured for extended trigger. It walks a 0 through each line on the pull-ups latches and tries to trigger on each event.

	B7	B6	B5	B4	B3	B2	B1	B0
BYTE 0	0	ALL=1 FAIL	TSTON FAIL	TRIG	1	28	2	27
BYTE 1	3	26	4	25	5	24	6	23
BYTE 2	7	22	8	21	9	20	10	19
BYTE 3	11	18	12	17	13	16	14	15

ALL=1 FAIL - Indicates that one or more lines could not be set high initially (i.e. Lines shorted low). If only one line is shorted, that line is displayed. If multiple lines are shorted, individual lines cannot be displayed.

TSTON FAIL - The TSTON line failed to control the triggering.

TEST 53
PULL1_XTRIG

If the Simulation Option (900-001) is installed, this test verifies the operation of the trigger circuit inside the shadow RAM ASIC chip. It walks a 1 through each line on the pull-ups latches and tries to trigger on each event.

	B7	B6	B5	B4	B3	B2	B1	B0
BYTE 0	0	ALL=0 FAIL	TSTON FAIL	TRIG	1	28	2	27
BYTE 1	3	26	4	25	5	24	6	23
BYTE 2	7	22	8	21	9	20	10	19
BYTE 3	11	18	12	17	13	16	14	15

ALL=0 FAIL - Indicates that one or more lines could not be set low initially (i.e. Lines shorted high). If only one line is shorted, that line is displayed. If multiple lines are shorted, individual lines cannot be displayed.

TSTON FAIL - The TSTON line failed to control the triggering.

TEST 54
PULL_XEVENT

If the Simulation Option (900-001) is installed, this test verifies the operation of the event counter inside the shadow RAM ASIC chip configured for extended trigger. The tests are as follows:

1. Circuit configured as: EVENT-CLOCK=EQUAL, CLOCK-ENABLE=MATCH
   - Check for false clocking (clocking with CLOCK-ENABLE inactive)
   - Check for proper counting (set count = 255 and provide 255 clocks)
2. Circuit configured as: EVENT-CLOCK=MATCH, CLOCK-ENABLE=TSTON
   - Check for false clocking (clocking with CLOCK-ENABLE inactive)
   - Check for proper counting (set count = 255 and provide 255 clocks)

The results are interpreted as follows:

	B7	B6	B5	B4	B3	B2	B1	B0
BYTE 0	0					1-PTC	1-NTC	1-CDIS
BYTE 1	1-C7	1-C6	1-C5	1-C4	1-C3	1-C2	1-C1	1-C0
BYTE 2						2-PTC	2-NTC	2-CDIS
BYTE 3	2-C7	2-C6	2-C5	2-C4	2-C3	2-C2	2-C1	2-C0

NOTE: 1-x, 2-x refer to configurations 1 and 2 as described above.

PTC- Premature Terminal Count. The terminal count was reached before expected. The following byte indicates the number of clocks which occurred when terminal count was reached.

NTC- No Terminal Count. Terminal count did not occur after supplying 255 clocks.

CDIS- Count Disable. The event counters clock-enable line is not functioning, allowing the counter to count when clock-enable is inactive.

TEST 55
SHAD_INIT

If the Simulation Option (900-001) is installed, this tests the shadow RAM initialization and readback functions using the SRAM master pattern.

1. Manual initialization test:
   - Manually write all locations with 0.
   - Read back all locations checking for 0.
   - Manually write all locations with 1.
   - Read back all locations checking for 1.

2. Auto initialization test:
   - Auto initialize all locations with 0.
   - Read back all locations checking for 0.
   - Auto initialize all locations to 1.
   - Read back all locations checking for 1.

RESULT BYTES:

	B7	B6	B5	B4	B3	B2	B1	B0
BYTE 0	0				AI1	AI0	MI1	MI0
BYTE 1								
BYTE 2								
BYTE 3								

AI1- Auto-Initialization to 1 failed.
AI0- Auto-Initialization to 0 failed.
MI1- Manual-Initialization to 1 failed.
MI0- Manual-Initialization to 0 failed.

TEST E60
WALK_SIZELEDS

This test turns off all of the SIZE LED's and walks each one on. It then turns on all of the LED's and walks each one off. This test is visual and is not executed during power-up selftest.

TEST E61
TEST_MEMORY

This test verifies the ckecksums of all of the ROMs and tests most of the RAM. The SRAM that is in use when the test is started is not tested. This test will normally take about five minutes to complete.

Byte 0 - bit 0 is set if the system failed. This is the lower 1/4 of the SYSAF EPROM.

Byte 1 - bit 7 is set if any overlay failed. The other bits indicate which overlay failed first. When one overlay fails the remaining ones are not tested. They are tested in ascending order.

0000 - SYSCOM, SYSB or SYSD
0001 - SEQ, SYSB or SYSD
0010 - COMPIL, SYSB or SYSD
0011 - USER, SYSB or SYSD
0100 - MATH, SYSB or SYSD
0101 - DISP, SYSB or SYSD
0110 - COM, SYSB or SYSD
0111 - FILE_U, SYSB or SYSD
1010 - RDTEST, SYSAF or SYSC
1011 - SLFTST, SYSAF or SYSC
1100 - MISC, SYSAF or SYSC
1101 - EDITOR, SYSAF or SYSC
1110 - LOG, SYSAF or SYSC
1111 - OTHER, SYSAF or SYSC

Byte 2 - data bits that failed when the SRAM was tested.

Byte 3 - This indicates the DRAM chips that failed on earlier Micro boards that used 8 DRAM chips. For boards that have 2 DRAM devices only at U82 and U86, any bit can indicate either of the DRAMs.

B7 - U86
B6 - U82
B5 - U87
B4 - U83
B3 - U88
B2 - U84
B1 - U89
B0 - U85

TEST E62
WALK_MONLEDS

This test turns off all of the MONITOR LED's and walks each one on. It then turns on all of the LED's and walks each one off. This test is visual and is not executed during power-up selftest.

TEST E63
UPDATE_VCC_LIM

This test reads the current value of Vcc on the buffer and updates the stored minimum and maximum readings if necessary.

TEST E64
SHAD_ADDR

The shadow RAM addressing test takes approximately 3 minutes to run.

RESULT BYTES:

	B7	B6	B5	B4	B3	B2	B1	B0
BYTE 0	WR	ADD	ADD					
BYTE 1	PT	NT						
BYTE 2	A15	A14	A13	A12	A11	A10	A9	A8
BYTE 3	A7	A6	A5	A4	A3	A2	A1	A0

ADD - Failed addressing test on LCA at U105 of High Speed Board.
Result bytes 2 and 3 identify the address lines in error.

WR -The byte written was not verified immediately after being written.

PT - Premature termination of initialization cycle.

NT - Initialization cycle not terminated.

TEST E70
KEY_CLOSURE

This test asks the operator to press the indicated key. When the key is pressed, the test moves on to the next key, approximately 150 combinations in all. This test does not return results in memory.

TEST E71
DISP_RAM

This test performs a ramtest of the display's memory. Results returned are as follows:

```
           B7  B6   B5   B4   B3   B2   B1  B0
          +---+----+----+----+----+----+---+---+
  BYTE 0  | 0 |BUSY|DATA|ADDR|A11 |A10 | A9| A8|
          +---+----+----+----+----+----+---+---+
  BYTE 1  | A7| A6 | A5 | A4 | A3 | A2 | A1| A0|
          +---+----+----+----+----+----+---+---+
  BYTE 2  | D7| D6 | D5 | D4 | D3 | D2 | D1| D0|
          +---+----+----+----+----+----+---+---+
  BYTE 3  | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0 |
          +---+----+----+----+----+----+---+---+
```

BUSY - Indicates that the display is always busy
DATA - Indicates that the data bit test failed (results in byte 2)
ADDR - Indicates that the address bit test failed (results in bytes 0 & 1)

NOTE: The DATA and ADDR tests are not executed if the BUSY test fails.

TEST E74
DISP_CHAR_SET

This test writes the character set to the screen. The order is not by ASCII code but rather by logical character grouping. This test returns no results in memory.

TEST E75
CART_SLFT

This test formats the cartridge. It is intended for "BURN-IN". This test returns no results in memory.

TEST E76
TEST_C_ENG

This is a similar test to TEST_CYCLE (49).
The only difference is that the RD power line is momentarily shorted to verify that an interrupt caused by a shorted RD is handled properly.

TEST E77
ACT_CROSS

This test verifies that there is no cross talk between lines that can affect activity circuit. The line being checked is held low while all other lines are toggled. The line is then held high while all other lines are toggled. The activity circuit is used to trap any activity on the inactive line.
This test cannot be executed with a clip inserted.

TEST E78
TRG_CROSS

This test verifies that there is no cross talk between lines that can affect the trigger circuit. The line being checked is held low while all other lines are toggled. The line is then held high while all other lines are toggled. The trigger circuit is used to trap any activity on the inactive line.
This test cannot be executed with a clip inserted.line.

TEST E79
FRQ_CROSS

This test verifies that there is no cross talk between lines that can affect frequency measurement circuit. The line being checked is held low while all other lines are toggled. The line is then held high while all other lines are toggled. The frequency circuit is used to trap any activity on the inactive line.
This test cannot be executed with a clip inserted.

TEST E80
FLT_CROSS

This test verifies that there is no cross talk between lines that affect the fault circuit. The line being checked is held low while all other lines are toggled. The frequency circuit is used to trap any activity on the inactive line.
This test cannot be executed with a clip inserted.

3.4 System Error Codes

System Error Codes appear on the command line of the 900 when its microprocessor operation hangs up. These codes are used mainly for design debug, but are included here for completeness in the event a software bug is encountered. The most common cause of such a system crash is the loading of a corrupted simulated reference device file.

These codes are not of much use for hardware troubleshooting. The only hardware code is 80 and its message appears similar to the following:

System Error #80
PC = 536A
Overlay = Selftest
Cannot clear Fault Latches

This indicates that at the time of the crash, the microprocessor Program Counter contained the value 536A and memory addressing was in the Selftest overlay.

<u>File Management Error Codes</u>

01	FILE IS OPEN
02	DEVICE ALREADY FORMATTED
03	FILE NOT FOUND
04	FILE ALREADY EXISTS
05	INSUFFICIENT SPACE ON DESTINATION DEVICE
07	WRITTEN BYTE FAILED TO VERIFY
08	CANNOT WRITE DEVICE
09	FILE CANNOT BE DELETED
0A	DEVICE DOES NOT EXIST
0B	FILE NOT OPEN
0C	ERROR SETTING PAGE
0D	ERROR SETTING CHAPTER
0E	ERROR ACCESSING DEVICE
0F	PASSWORD INVALID
10	INSUFFICIENT STACK SPACE FOR TRANSFER
11	UNABLE TO COMPRESS
12	CHECKSUM ERROR ON FILE
13	COPY PROTECTED
14	DEVICE NOT FORMATTED
15	FILE UNRECOVERABLE/NOT FOUND
16	FILE IS DELETE PROTECTED
17	DEVICE HAS NO OVERHEAD
18	DIRECTORY EXCEEDS PAGE OVERHEAD
19	DCB DATA DOES NOT MATCH DEVICE DATA
1A	ERROR IN OVERHEAD DATA
1B	ADDRESS IS OUT OF FILE BOUNDS
1C	FILE IS TOO BIG TO BE LOADED
1D	DEVICE PASSWORD INCORRECT
1E	END OF FILE REACHED

1F DEVICE IS MODIFY PROTECTED
20 DEVICE IS COPY PROTECTED
21 DEVICE IS DELETE PROTECTED
22 INVALID FILE TYPE
23 FILE EXCEEDS ALLOWABLE SIZE
24 FILE IS CORRUPT

Hardware Error Code

80 CANNOT CLEAR FRAMING (FLM LATCHES)

Register Error Codes

BO STACK/HEAP COLLISION
B1 UNBALANCED DEFINITION
B2 CURSOR LIMIT ERROR - LINE
B3 CURSOR LIMIT ERROR - COLUMN
B4 COMMAND WAS ABORTED

Communications Error Codes

D0 FILE NOT IN COMPILED-TRANSMISSION FORMAT
D1 PARITY ERROR
D2 FRAMING ERROR
D3 OVERRUN ERROR

4 Troubleshooting

4.1 Test Result Interpretation

The first step in troubleshooting is to use the poweron self test to establish a result failure profile. Select <<prt_res>> from the debug screen to dump the detailed results to a printer connected to the RS232 port. The listing will consist of general results, flags and failing individual results. If no printer is available, record the individual results as they appear on the display after pressing <<display>> "test #" <ENTER> for each failing test number.

The following rules are suggested for interpreting the listed results:

RULE 1:
Investigate flag failures before other failed tests. They indicate catastrophic operational failures and cause a number of other tests to fail. The exception to this rule is when only the following flag(s) are present:

Interface Buffer Register (BYTE 1 b7)
Threshold Calibration (BYTE 3 b2)
FMASK Calibration (BYTE 3 b3)

These flags can be caused by many things and it is usually better to begin by investigating other failing tests first.

RULE 2:
If Test 46 fails and the power supply bits of the individual result are set (bits 6,7 of BYTE1), check the power supply voltages with a voltmeter. A problem here will cause many other failures. If the voltages are good, then start investigating other failed tests before number 46. The functions it exercises are complex and not easy to troubleshoot.

RULE 3:
If multiple tests or multiple lines are failing, this indicates a control circuit problem. A single line failing can be caused by a component in the signal path of that channel.

RULE 4:
When multiple tests or lines are failing, use the table that follows in this section to identify the common circuit blocks. Refer to the theory in Section 2 to crossreference these blocks to the board schematics. The fault can normally be isolated to the common circuitry. In addition, signal flow diagrams at the end of this section can be of some help, since they depict the active circuitry for a number of tests.

For example, if tests 1 and 2 pass on a certain line while tests 3 and 4 fail on the same line, the Interface Buffer must be good, since the stimulus for tests 1 through 4 comes from the Buffer.

4.2 Selftest / Circuit Block Reference Table

The following table describes state of major hardware blocks during each individual selftest.

Conventions:

S0	static low level
S1	static high level
W0	walking low level
W1	walking high level
A	active
-P	pulsed low
+P	pulsed high
F	FBUS monitored
E	EBUS monitored
WVcc	walking Vcc pulse thru RD power relays
WGnd	walking ground pulse thru RD power relays

STATE OF MAJOR BLOCKS OF HARDWARE FOR EACH TEST (VER. 5.00 AND LATER)

CONVENTIONS: A=ACTIVE W=WALKING (LINE BY LINE) S=STATIC P=PULSED(-=LO, +=HI) BLANK=NOT APPLICABLE or OFF

NAME OF ROUTINE	TEST #	PULL-UPS LATCH	INBUF	SYNC LATCH	DIFTEST DRIVERS HI	DIFTEST DRIVERS LO	SELF TEST LATCH	RD SUPPLY RELAYS	PIN DIS LATCH	FFCLK LINE	MON MUX	FREQ CCT.	TRIG BUFF	TRIGGER LATCHES DATA	TRIGGER LATCHES QUAL	ACT CCT	MON BUS RDBK	SHAD CCT.	RD EMUL CCT.	DGATE CCT.	ADDITIONAL DATA
SLFT_CLIP	0						W0/W1				E						A				TEST CLIP LOOPBACK TEST
PULL0_MON	1	W0									E						A				
PULL1_MON	2	W1									E						A				
PULL0_FLT	3	W0	A		A	A	S1		S1	P	F						A				
PULL1_FLT	4	W1	A		A	A	S1		S1	P	F						A				
SYNC0_Hres_FLT	5			W0	A		S1		S1	P	F						A				
SYNC1_Hres_FLT	6			W1	A		S1		S1	P	F						A				
SYNC0_Lres_FLT	7			W0		A	S1		S1	P	F						A				
SYNC1_Lres_FLT	8			W1		A	S1		S1	P	F						A				
PINDIS0_FLT	9			S0	A	A	S1		W0	P	F						A				
PINDIS1_FLT	10			S0	A	A	S1		W1	P	F						A				
SLFTST0_FLT	11			S0	A	A	W0		S1	P	F						A				
SLFTST1_FLT	12			S0	A	A	W1		S1	P	F						A				
VccON_FLT	13			S0	A	A		WVcc	S1	P	F						A				Vcc RELAYS - PINS 8,9,27,28,1,4,5
GndON_FLT	14			S1	A	A		WGnd	S1	P	F						A				Gnd RELAYS - PINS 8-12,14,28,4,7,24,25
PULLPOS_FREQ	15	W +P										A									
TRIGQAL0_EQUAL	16													W0	W0						
TRIGQAL1_EQUAL	17													W1	W1						
QAL0_EQUAL	18													S1	W0						
QAL1_EQUAL	19													S0	W1						
TRIG0_EQUAL	20													W0	S1						
TRIG1_EQUAL	21													W1	S0						
PULL0_TRIG_EQUAL	22	W0											A	S1	S1						
PULL1_TRIG_EQUAL	23	W1											A	S0	S1						
PULL0_TRIGQAL	24	W0											A	S0	S1						
FM_STAT_NFLT	25			S1	A	A	S1		S1	S0	F						A				
FM_STAT_FLT	26			S0	A	A	S1		S1	S0	F						A				
FMASK_WB_TEST	27			S1	A	A	-P		S1	S0	F						A				WIDE-BAND FMASK TESTS
FMASK_CAL	28			S1	A	A	-P		S1	S0	F						A				FMASK CALIBRATION TEST
FM40_FLT	29			S1	A	A	-P		S1	S0	F						A				PULSE = 40ns, FMASK < PULSE
FM40_NFLT	30			S1	A	A	-P		S1	S0	F						A				PULSE = 40ns, FMASK > PULSE
FM80_FLT	31			S1	A	A	-P		S1	S0	F						A				PULSE = 80ns, FMASK < PULSE
FM80_NFLT	32			S1	A	A	-P		S1	S0	F						A				PULSE = 80ns, FMASK > PULSE
FM120_FLT	33			S1	A	A	-P		S1	S0	F						A				PULSE = 120ns, FMASK < PULSE
FM120_NFLT	34			S1	A	A	-P		S1	S0	F						A				PULSE = 120ns, FMASK > PULSE
FM160_FLT	35			S1	A	A	-P		S1	S0	F						A				PULSE = 160ns, FMASK < PULSE
FM160_NFLT	36			S1	A	A	-P		S1	S0	F						A				PULSE = 160ns, FMASK > PULSE
FM200_FLT	37			S1	A	A	-P		S1	S0	F						A				PULSE = 200ns, FMASK < PULSE
FM200_NFLT	38			S1	A	A	-P		S1	S0	F						A				PULSE = 200ns, FMASK > PULSE
FM240_FLT	39			S1	A	A	-P		S1	S0	F						A				PULSE = 240ns, FMASK < PULSE
FM240_NFLT	40			S1	A	A	-P		S1	S0	F						A				PULSE = 240ns, FMASK > PULSE
ACT_DIS_CLR	41	A									E					A					PULSE ACTCLR! & ACTEN!
PULL0_ACT_TSTON	42	W -P	A								E					A					ACTIVITY CCT CONTROLLED BY TESTON
PULL1_ACT_TSTON	43	W +P	A								E					A					ACTIVITY CCT CONTROLLED BY TESTON
PULL0_ACT_ACTSTR	44	W -P									E					A					ACTIVITY CCT CONTROLLED BY ACTSTR
PULL1_ACT_ACTSTR	45	W +P									E					A					ACTIVITY CCT CONTROLLED BY ACTSTR
FREQ_BIAS_SHORT	46											A									FREQ H/W TEST SHORT
FREQ_BIAS_LONG	47											A									FREQ H/W TEST LONG
KEYBOARD_OPEN	48																				CHECKS THAT ALL KEYS ARE OPEN
TEST_CYCLE	49	A	A	A	A	A	A	A	A	A	A		A	A	A						INTERRUPTS, TIMERS, TRIGGER, GATE, SYNC
UART_TEST	50																				CHECKS OUT UART/RS232 CIRCUITRY
DGATE_TEST	51											A								A	DGATE - DELAY, DURATION, DIVIDER
PULL0_XTRIG	52	W0																A			EXTENDED TRIGGER - TRIGGER/GATE TEST
PULL1_XTRIG	53	W1																A			EXTENDED TRIGGER - TRIGGER/GATE TEST
PULL_XEVENT	54	A																A			EXTENDED TRIGGER - EVENT COUNTER TEST
SHAD_INIT	55																	A			SHADOW RAM INITIALIZATION TEST
	56																				
	57																				
	58																				
	59																				

E N G I N E E R I N G T E S T S

NAME OF ROUTINE	TEST #	PULL-UPS LATCH	INBUF	SYNC LATCH	DIFTEST DRIVERS HI	DIFTEST DRIVERS LO	SELF TEST LATCH	RD SUPPLY RELAYS	PIN DIS LATCH	FFCLK LINE	MON MUX	FREQ CCT.	TRIG BUFF	TRIGGER LATCHES DATA	TRIGGER LATCHES QUAL	ACT CCT	MON BUS RDBK	SHAD CCT.	RD EMUL CCT.	DGATE CCT.	ADDITIONAL DATA
WALK_SIZELEDS	E60																				WALK SIZE LED'S ON & OFF
TEST_MEMORY	E61																				PARTIAL MEMORY TEST
WALK_MONLEDS	E62																				WALK MONITOR LED'S ON & OFF
UPDATE_VCC_LIM	E63																				UPDATE Vcc MIN AND MAX READINGS
SHAD_ADDR	E64																	A			SHADOW RAM ADDRESSING TEST (3 min)
	E65																				
	E66																				
	E67																				
	E68																				
	E69																				
KEY_CLOSURE	E70																				CHECK OF KEY COMBINATIONS
DISP_RAM	E71																				DISPLAY RAM TEST/DISPLAY VISUAL TEST
RESERVED	E72																				
RESERVED	E73																				
DISP_CHAR_SET	E74																				DUMPS CHAR SET TO DISPLAY
CART_SLFT	E75																				CARTRIDGE SELFTEST ** DESTRUCTIVE **
TEST_C_ENG	E76	A	A	A	A	A	A	A	A	A	A		A	A	A						INTERRUPTS, TIMERS, TRIGGER, GATE, SYNC
ACT_CROSS	E77	A									A					A					CROSSTALK TEST - ACTIVITY CIRCUIT
TRG_CROSS	E78	A											A	A	A						CROSSTALK TEST - TRIGGER CIRCUIT
FRQ_CROSS	E79	A										A									CROSSTALK TEST - FREQUENCY CIRCUIT
FLT_CROSS	E80																				CROSSTALK TEST - FAULT CIRCUIT

4.3 Selftest Circuit Block Diagrams

Each selftest or group of similar selftests is shown on a block diagram with indicators for:

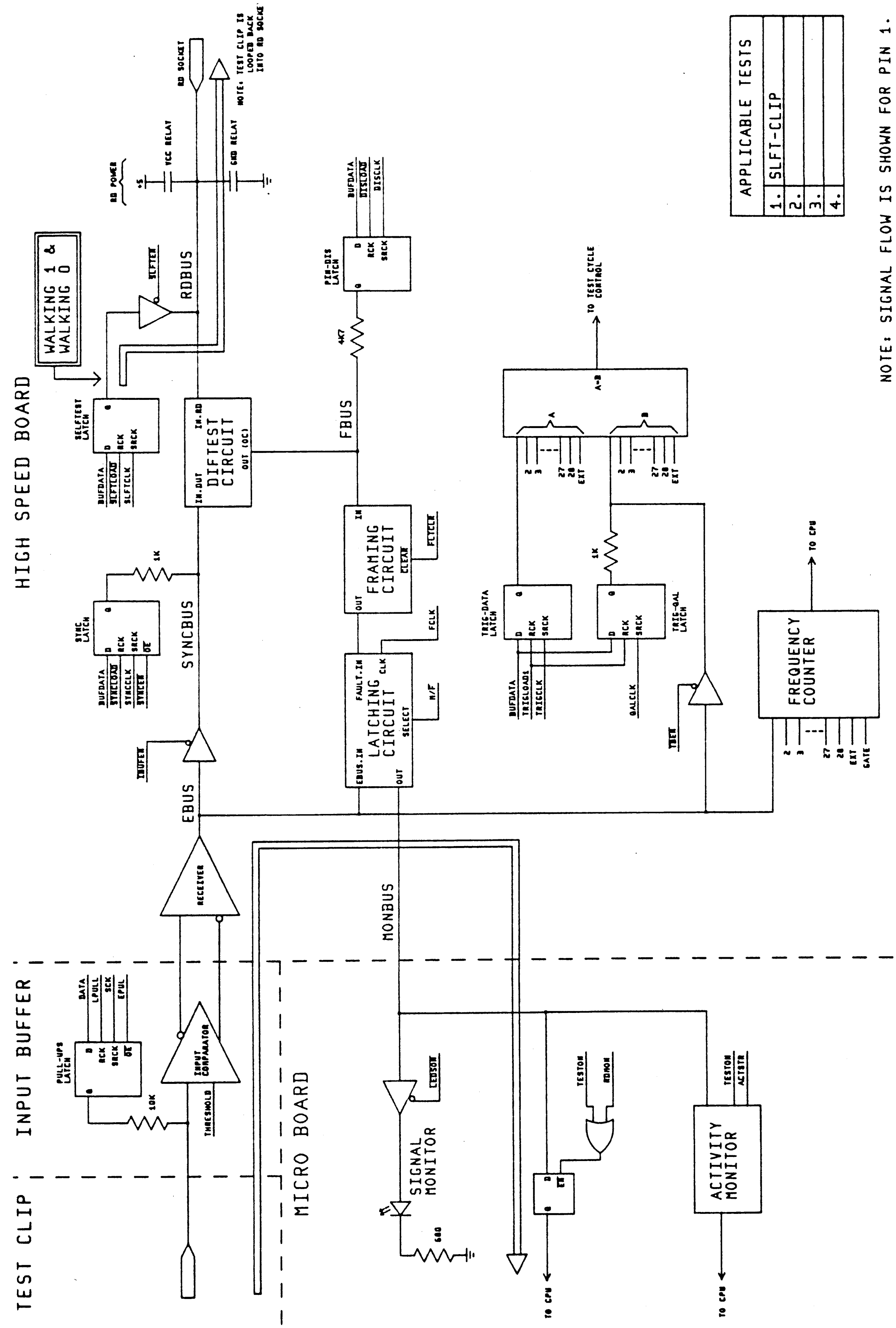
- stimulus type
- stimulus origin
- signal flow

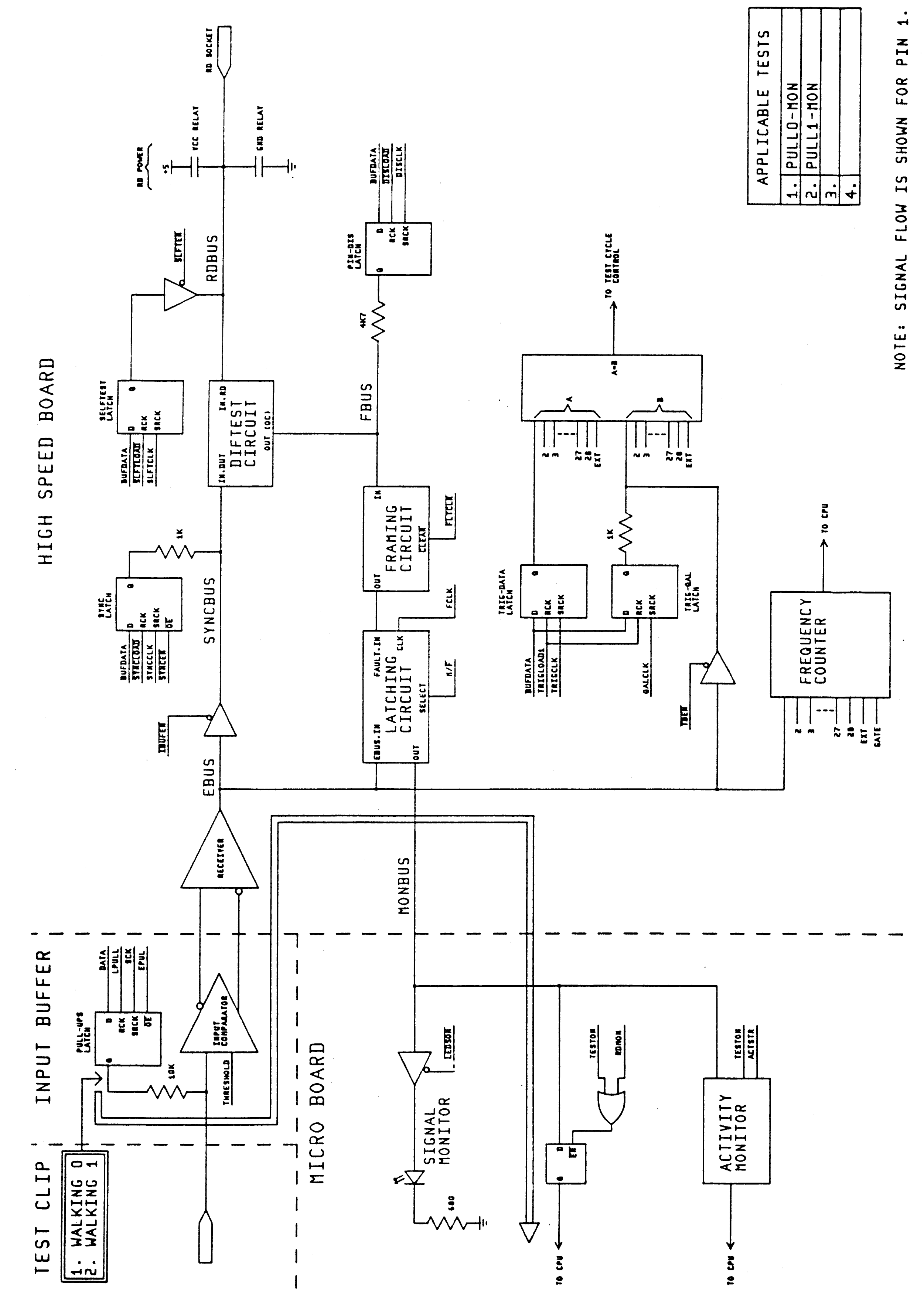
A separate diagram appears for:

Test 0
Tests 1,2
Tests 3,4
Tests 5-8
Tests 9,10
Tests 11,12
Tests 13,14
Test 15
Tests 16,17
Tests 18,19
Tests 20,21
Tests 22,23
Test 24
Tests 25,26
Tests 27,28
Tests 29-40
Test 41
Tests 42-45

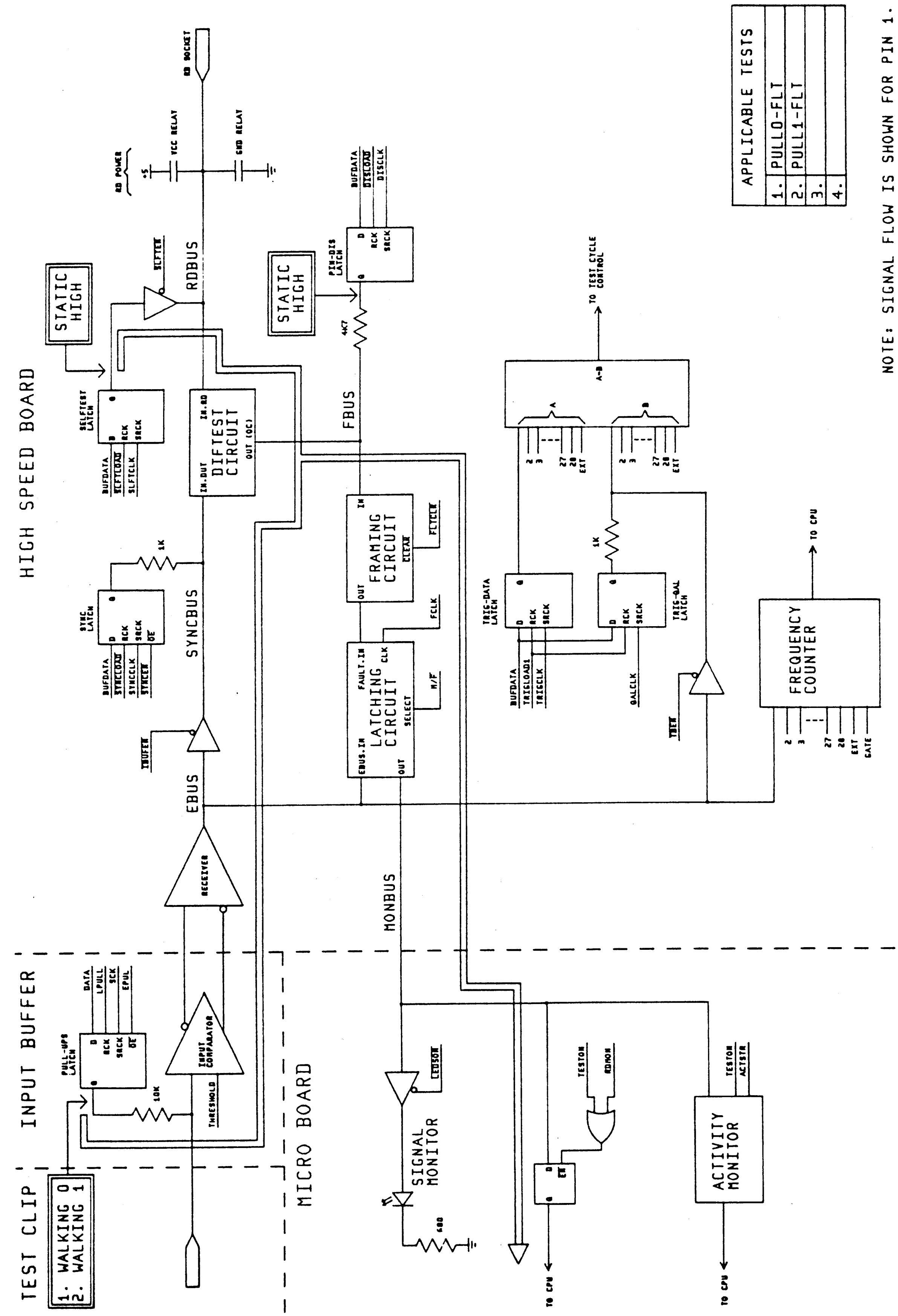
Tests 46 through 55 and the Extended Tests do not have separate diagrams.

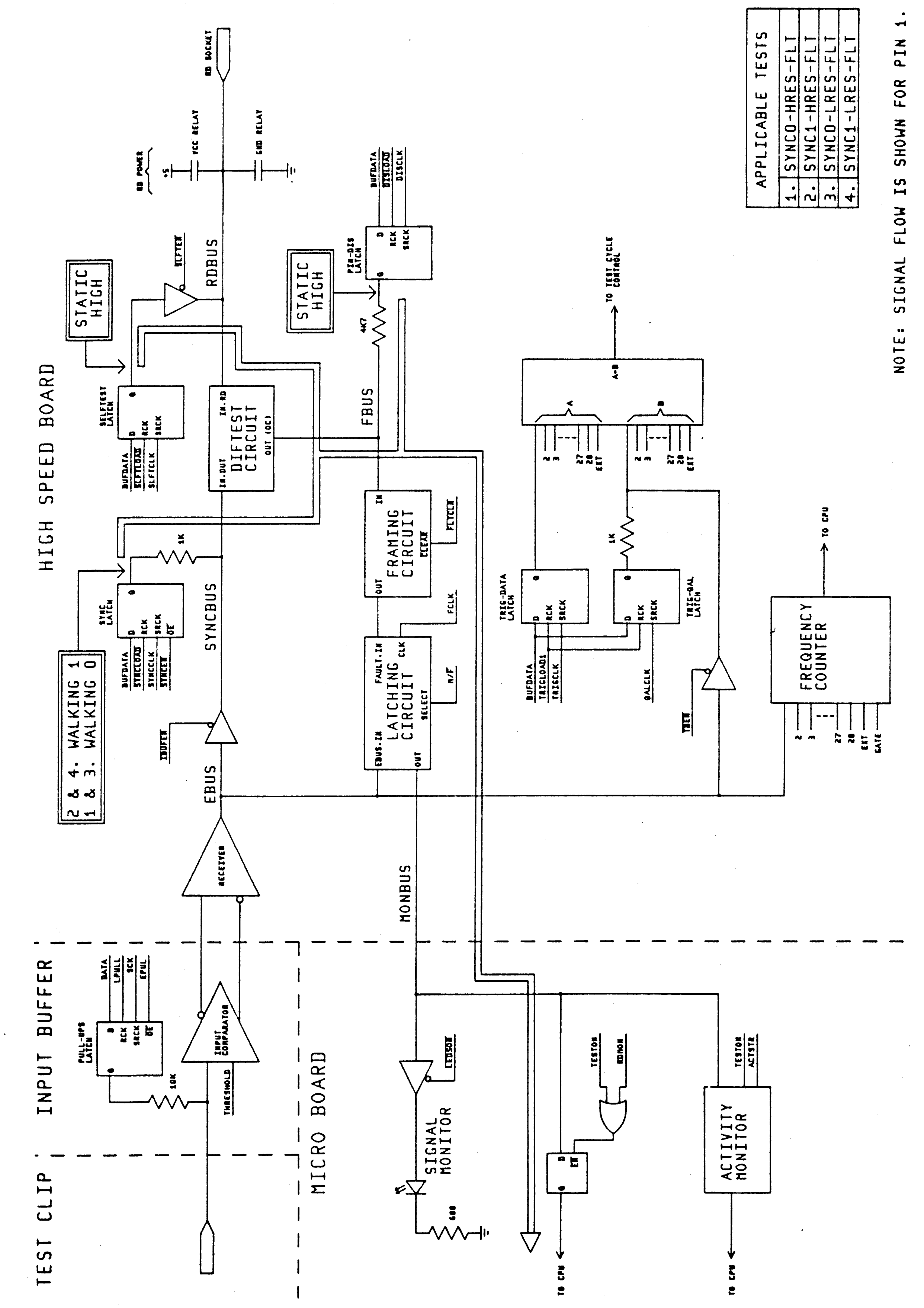
Tests 46,47 and 49 are comprehensive tests that exercise most of the circuitry. Tests 48 and 50 (keyboard and UART) narrowly exercise their appropriate circuits. Tests 51 through 55 exercise the Simulation Option circuitry with activity from the Interface Buffer through to the EBUS. This circuitry for Delayed Gate and Shadow RAM is not shown on the diagrams in this section, but is shown on the similar diagram of Section 2.4.

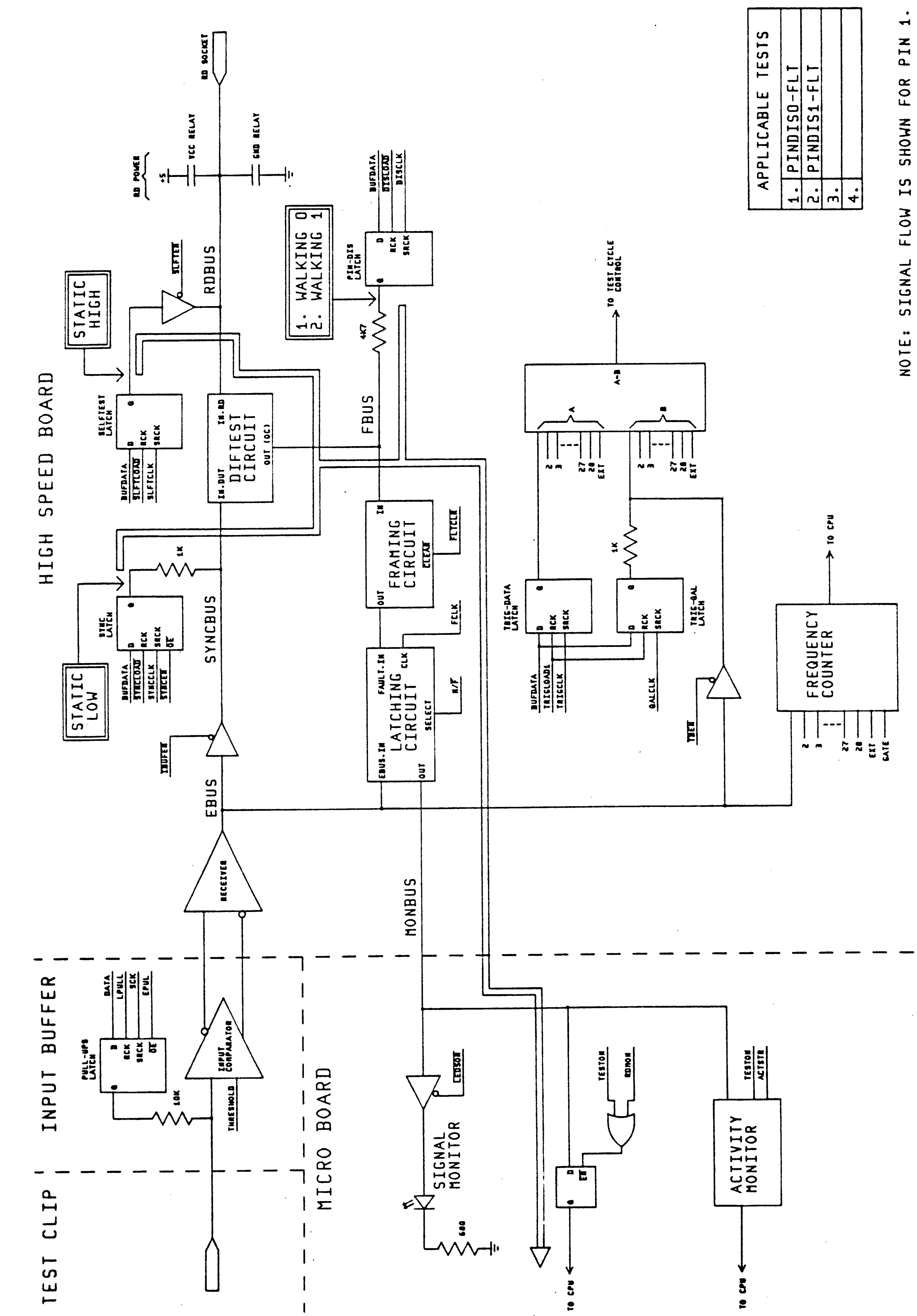

HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
WALKING 1 &
WALKING 0
RDBUS
SYNCBUS
FBUS
EBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
APPLICABLE TESTS
1. SLFT-CLIP
2.
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.

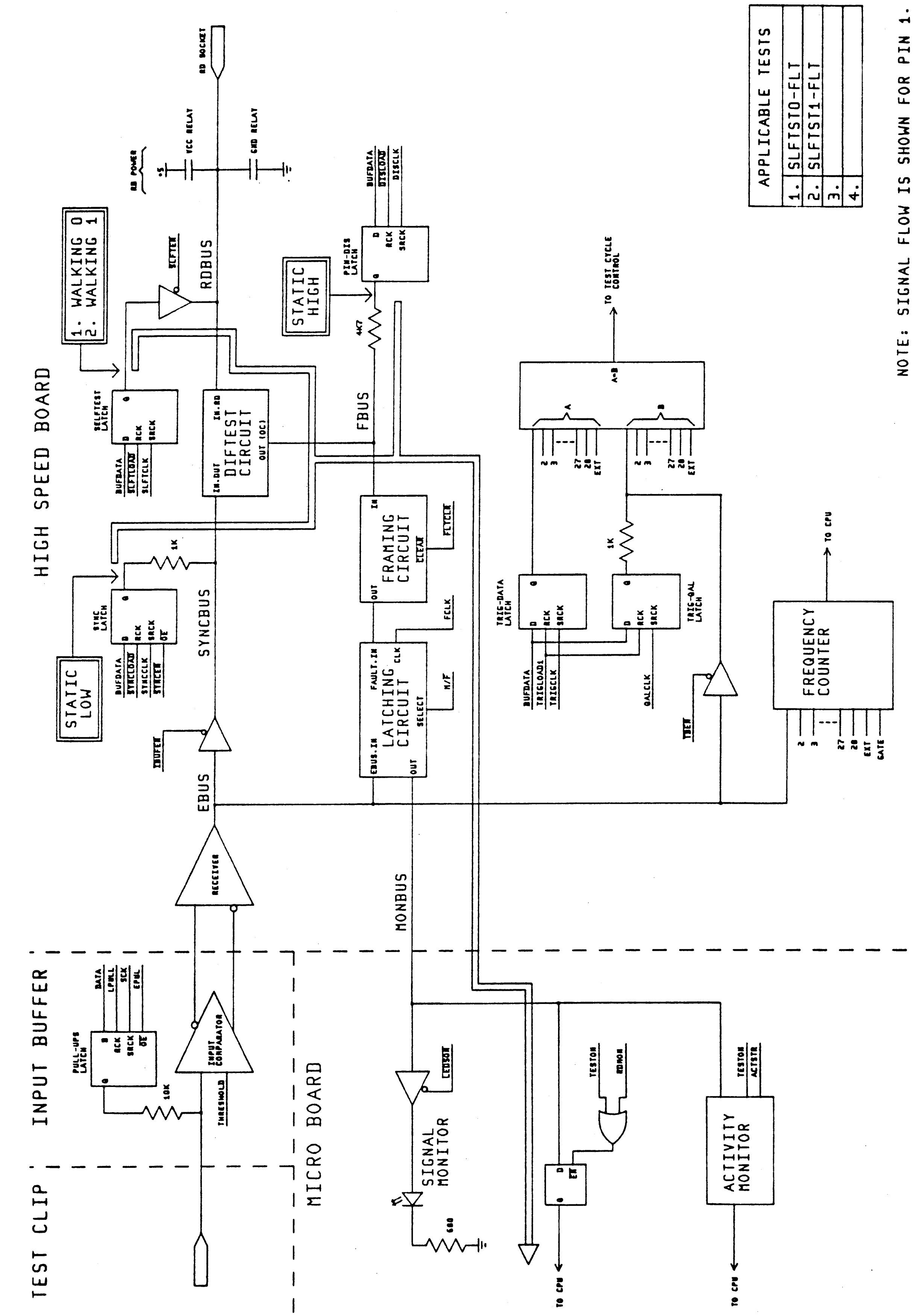


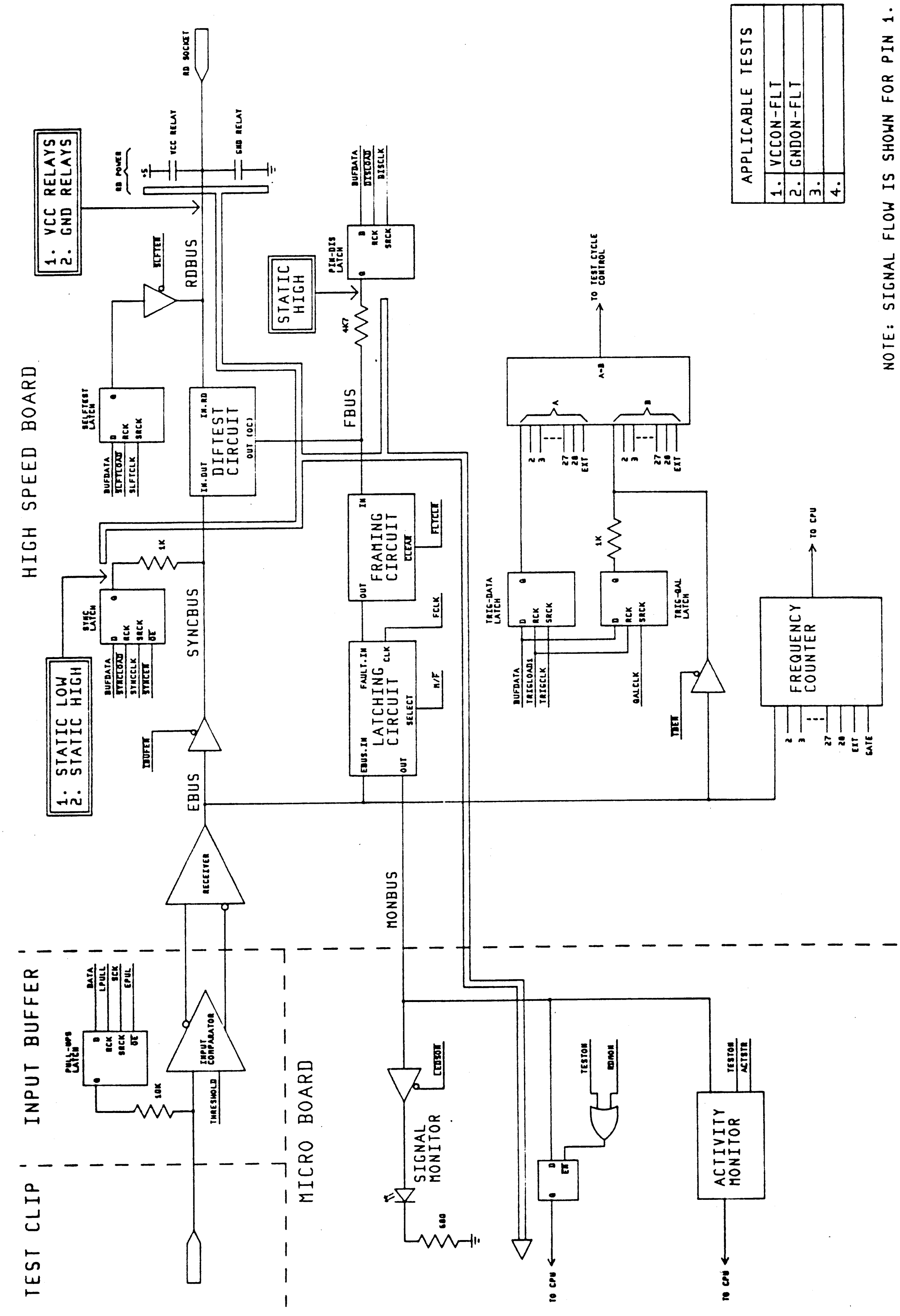
TEST CLIP
1. WALKING 0
2. WALKING 1
INPUT BUFFER
HIGH SPEED BOARD
MICRO BOARD
PULL-UPS LATCH
INPUT COMPARATOR
THRESHOLD
10K
RECEIVER
EBUS
SYNCBUS
RDBUS
FBUS
MONBUS
SYNC LATCH
SELFTEST LATCH
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
PIN-DIS LATCH
TRIG-DATA LATCH
TRIG-QAL LATCH
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
RD SOCKET
VCC RELAY
GND RELAY
RD POWER
TO TEST CYCLE CONTROL
TO CPU
APPLICABLE TESTS
1. PULL0-MON
2. PULL1-MON
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.

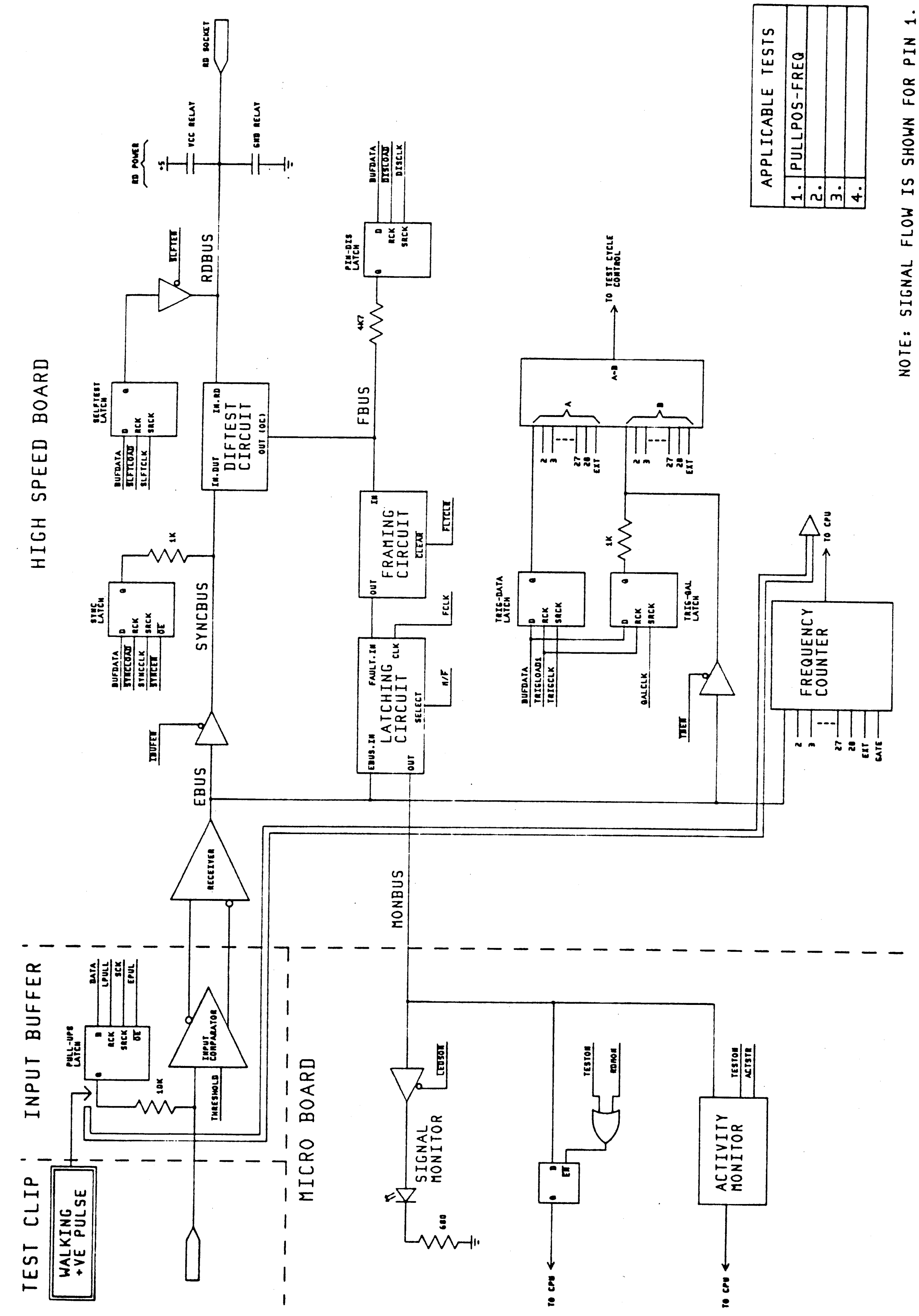

HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
1. WALKING 0
2. WALKING 1
APPLICABLE TESTS
1. PULL0-FLT
2. PULL1-FLT
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.
STATIC HIGH
STATIC HIGH
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR

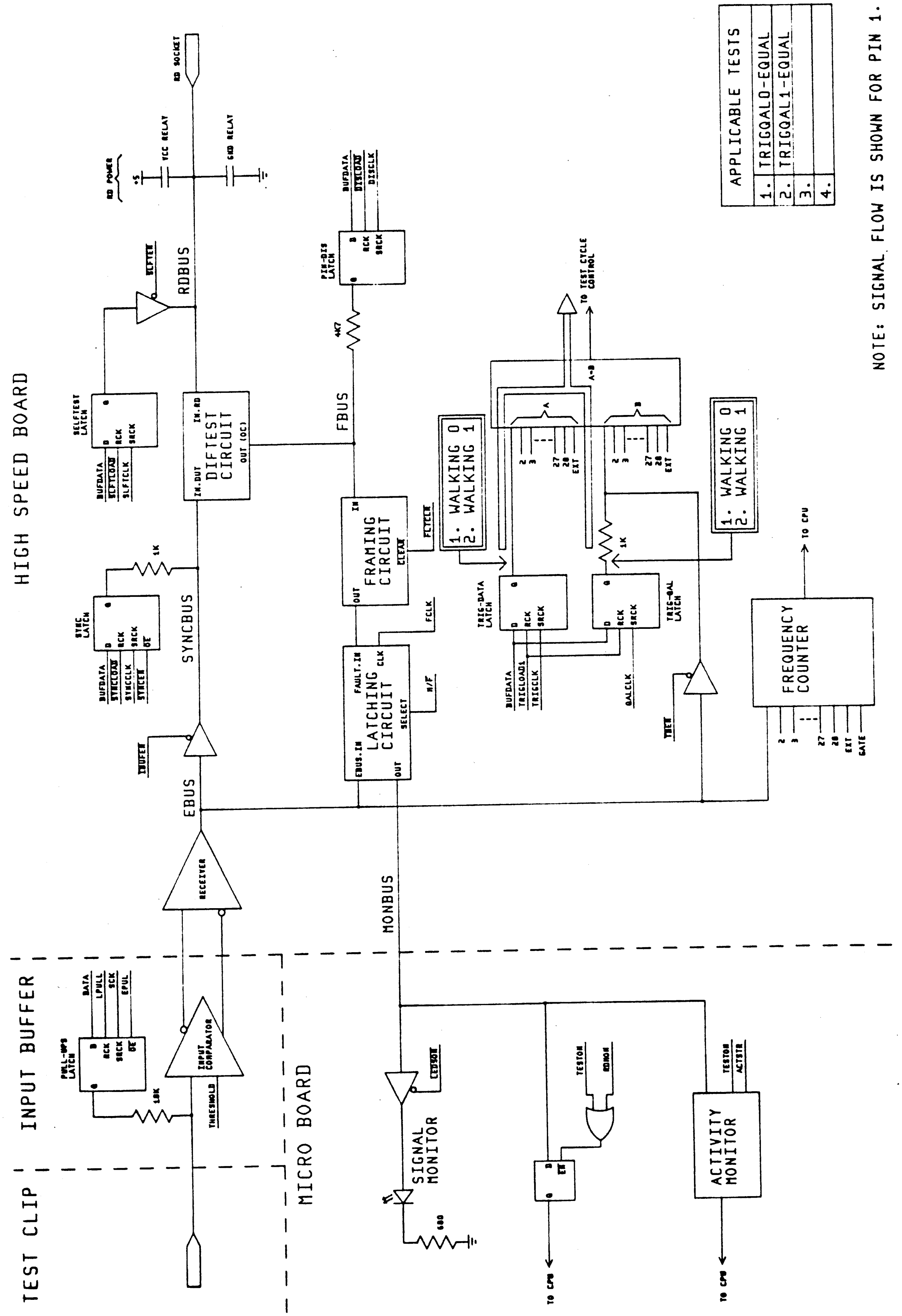

TEST CLIP
INPUT BUFFER
MICRO BOARD
HIGH SPEED BOARD
STATIC HIGH
2 & 4. WALKING 1
1 & 3. WALKING 0
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
SELFTEST LATCH
SYNC LATCH
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
PIN-DIS LATCH
TRIG-DATA LATCH
TRIG-QAL LATCH
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
RECEIVER
INPUT COMPARATOR
PULL-UPS LATCH
THRESHOLD
RD SOCKET
VCC RELAY
GND RELAY
RD POWER
TO TEST CYCLE CONTROL
TO CPU
APPLICABLE TESTS
1. SYNC0-HRES-FLT
2. SYNC1-HRES-FLT
3. SYNC0-LRES-FLT
4. SYNC1-LRES-FLT
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.


APPLICABLE TESTS
1. PINDIS0-FLT
2. PINDIS1-FLT
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.
HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
STATIC HIGH
STATIC LOW
1. WALKING 0
2. WALKING 1
RDBUS
FBUS
SYNCBUS
EBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
RECEIVER
INPUT COMPARATOR
THRESHOLD
4K7
1K
10K
TO CPU


HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
APPLICABLE TESTS
1. SLFTST0-FLT
2. SLFTST1-FLT
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.
1. WALKING 0
2. WALKING 1
STATIC HIGH
STATIC LOW
RDBUS
FBUS
SYNCBUS
EBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
RECEIVER
INPUT COMPARATOR
THRESHOLD
SELFTEST LATCH
SYNC LATCH
PIN-DIS LATCH
TRIG-DATA LATCH
TRIG-QAL LATCH
PULL-UPS LATCH
RD SOCKET
VCC RELAY
GND RELAY
RD POWER
TO TEST CYCLE CONTROL
TO CPU
A=B
1K
4K7
10K

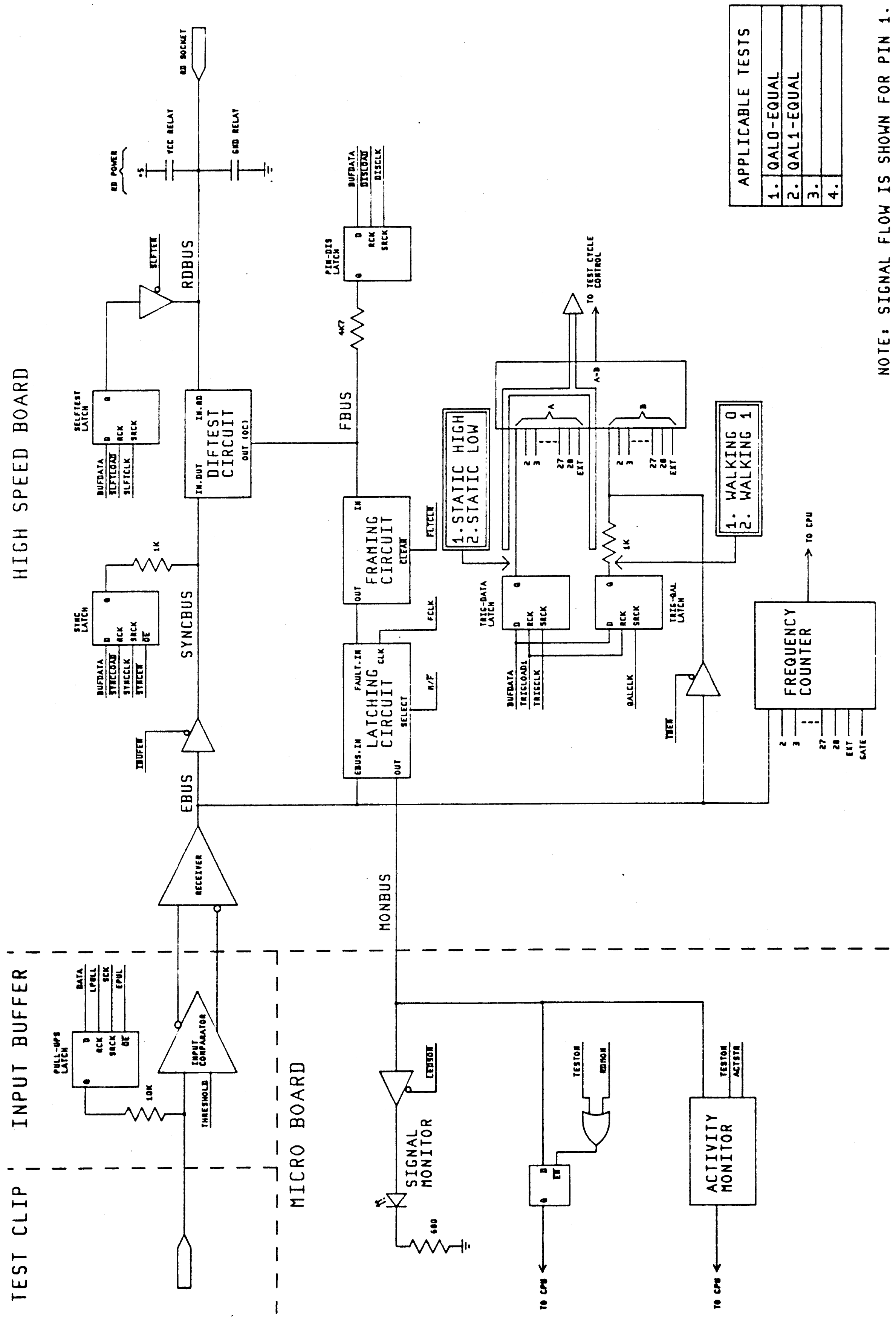

APPLICABLE TESTS
1. VCCON-FLT
2. GNDON-FLT
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.
TEST CLIP
INPUT BUFFER
HIGH SPEED BOARD
MICRO BOARD
1. VCC RELAYS
2. GND RELAYS
1. STATIC LOW
2. STATIC HIGH
STATIC HIGH
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR


HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
WALKING +VE PULSE
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
RECEIVER
INPUT COMPARATOR
THRESHOLD
SELFTEST LATCH
SYNC LATCH
PULL-UPS LATCH
PIN-DIS LATCH
TRIG-DATA LATCH
TRIG-QAL LATCH
RD SOCKET
VCC RELAY
GND RELAY
RD POWER
TO TEST CYCLE CONTROL
TO CPU
APPLICABLE TESTS
1. PULLPOS-FREQ
2.
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.

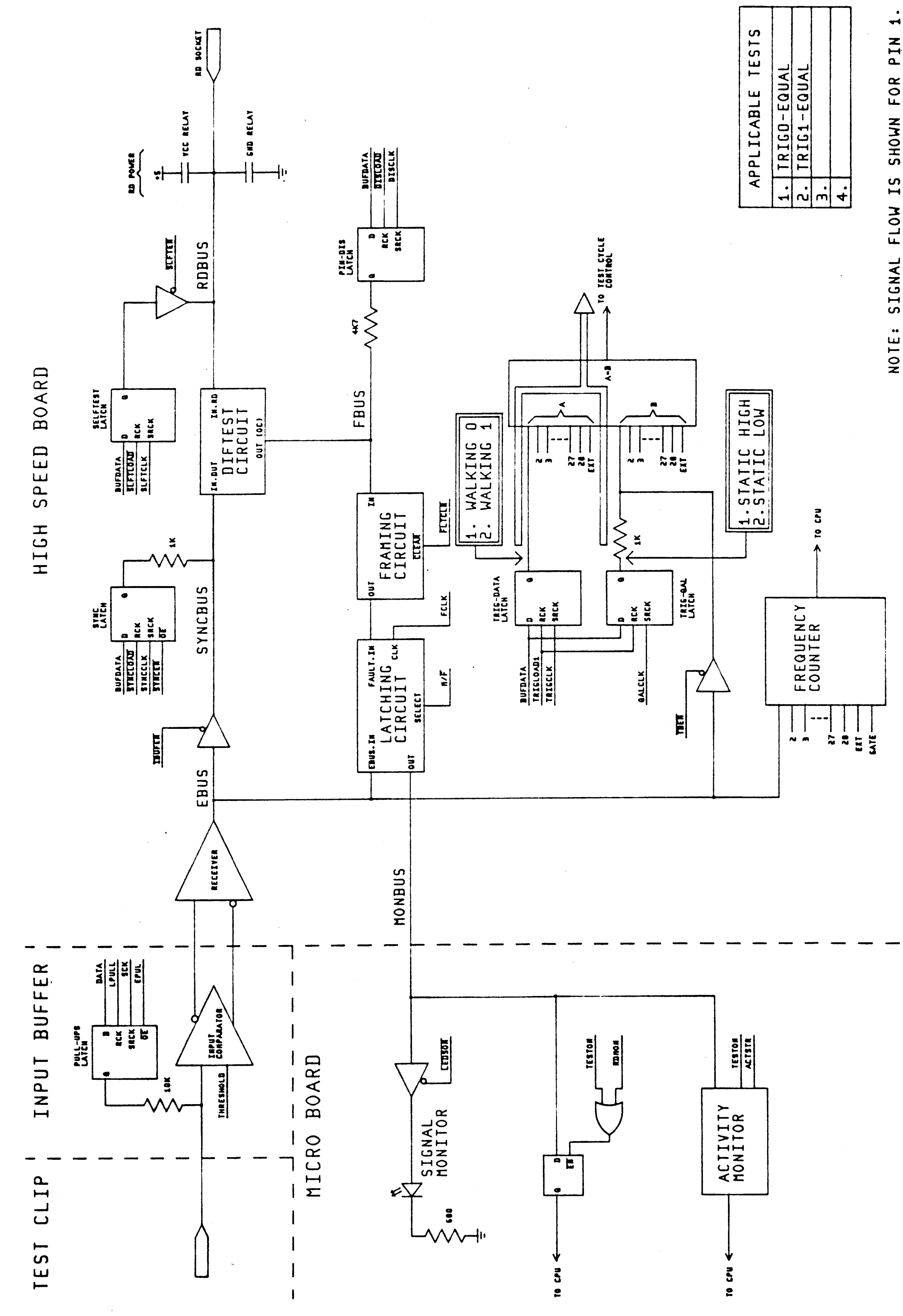


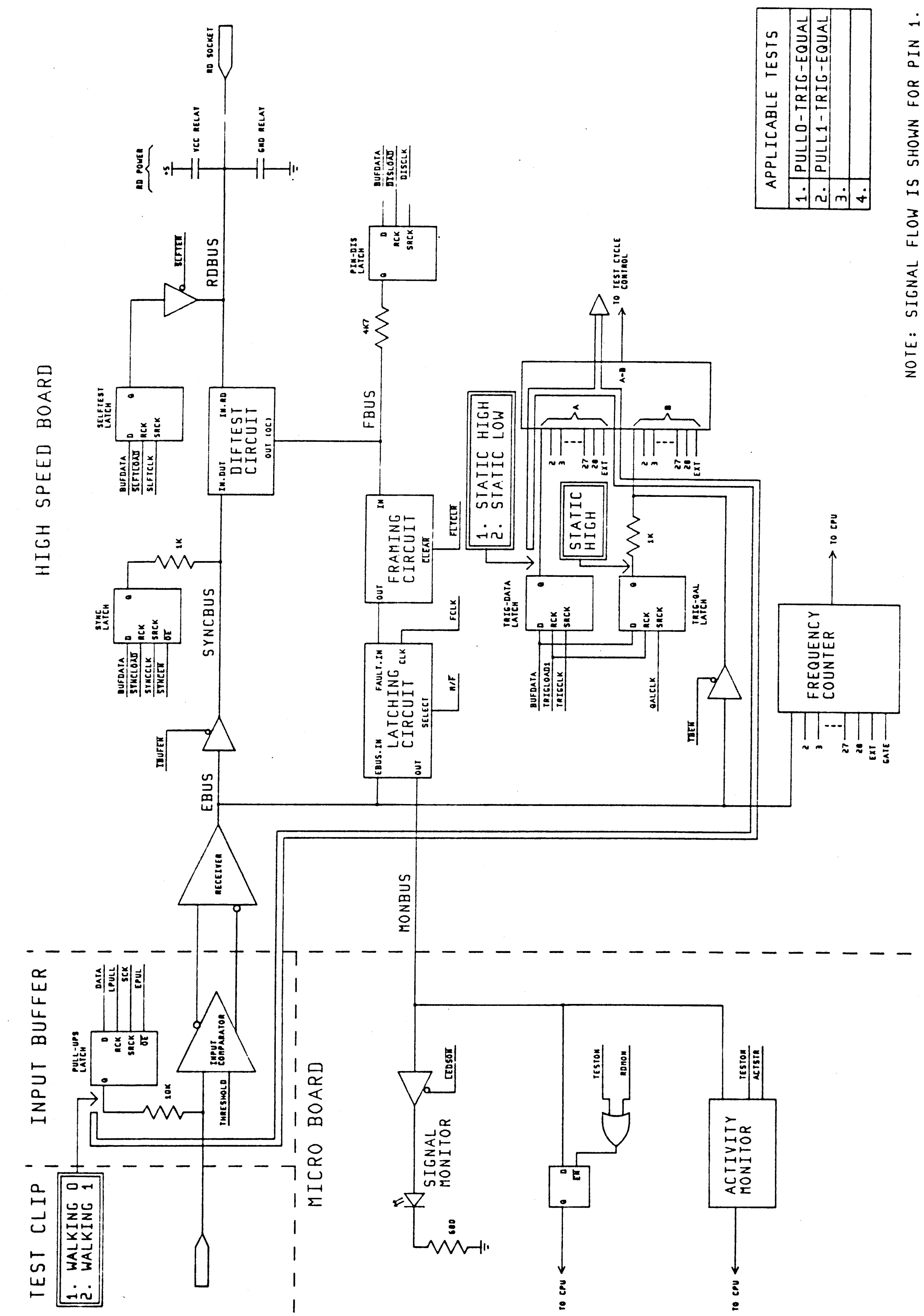
APPLICABLE TESTS
1. TRIGQAL0-EQUAL
2. TRIGQAL1-EQUAL
3.
4.

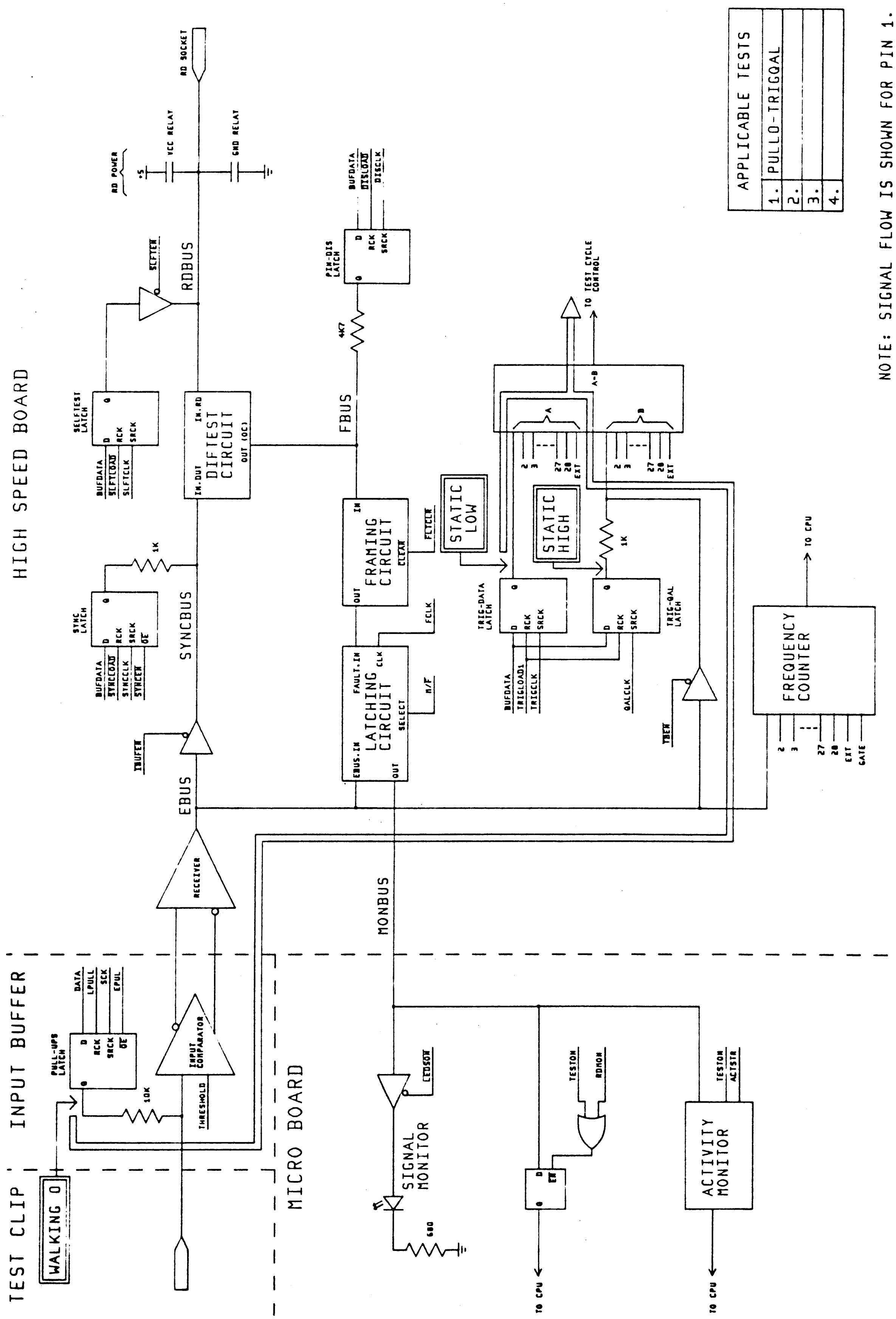
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.

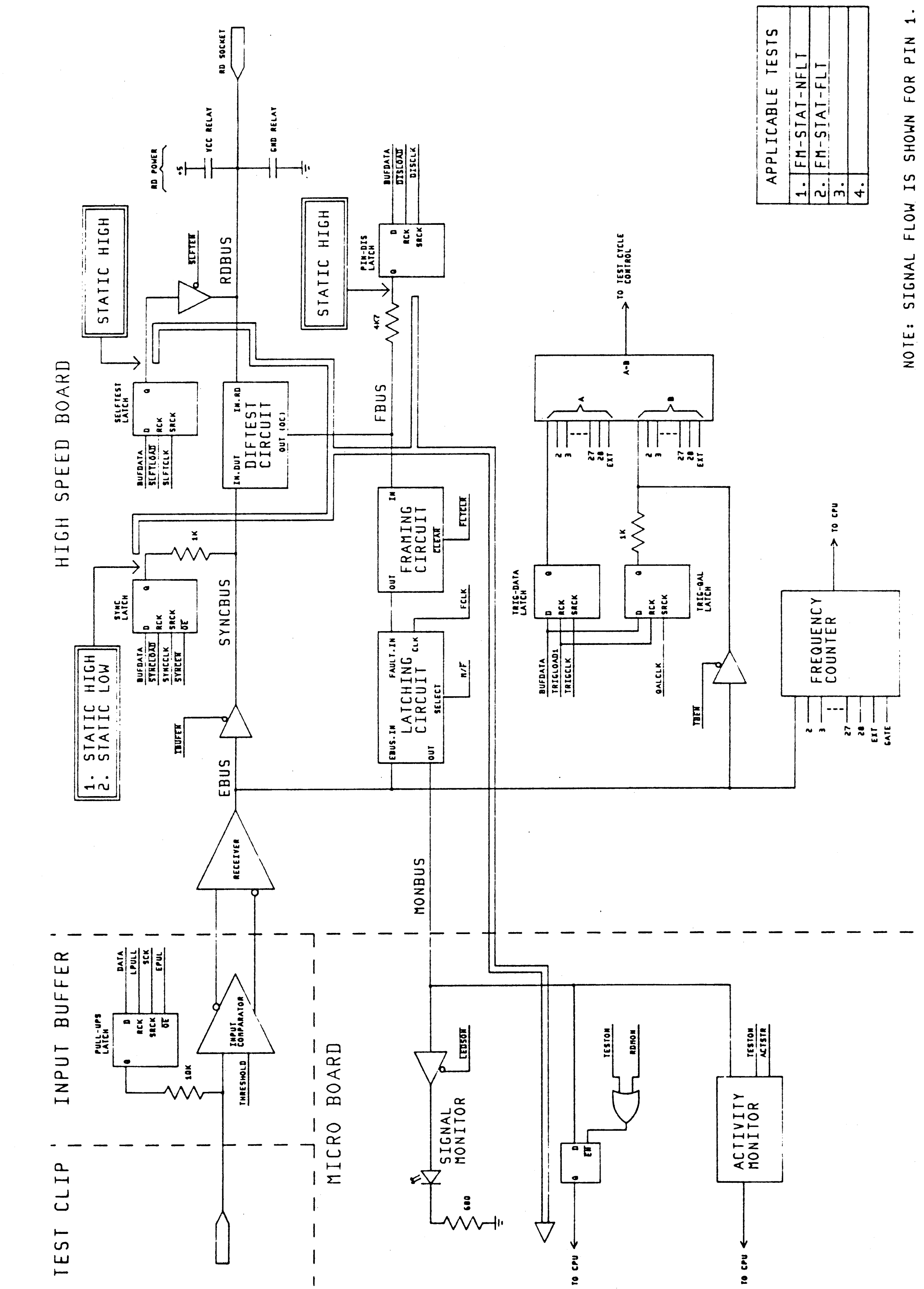


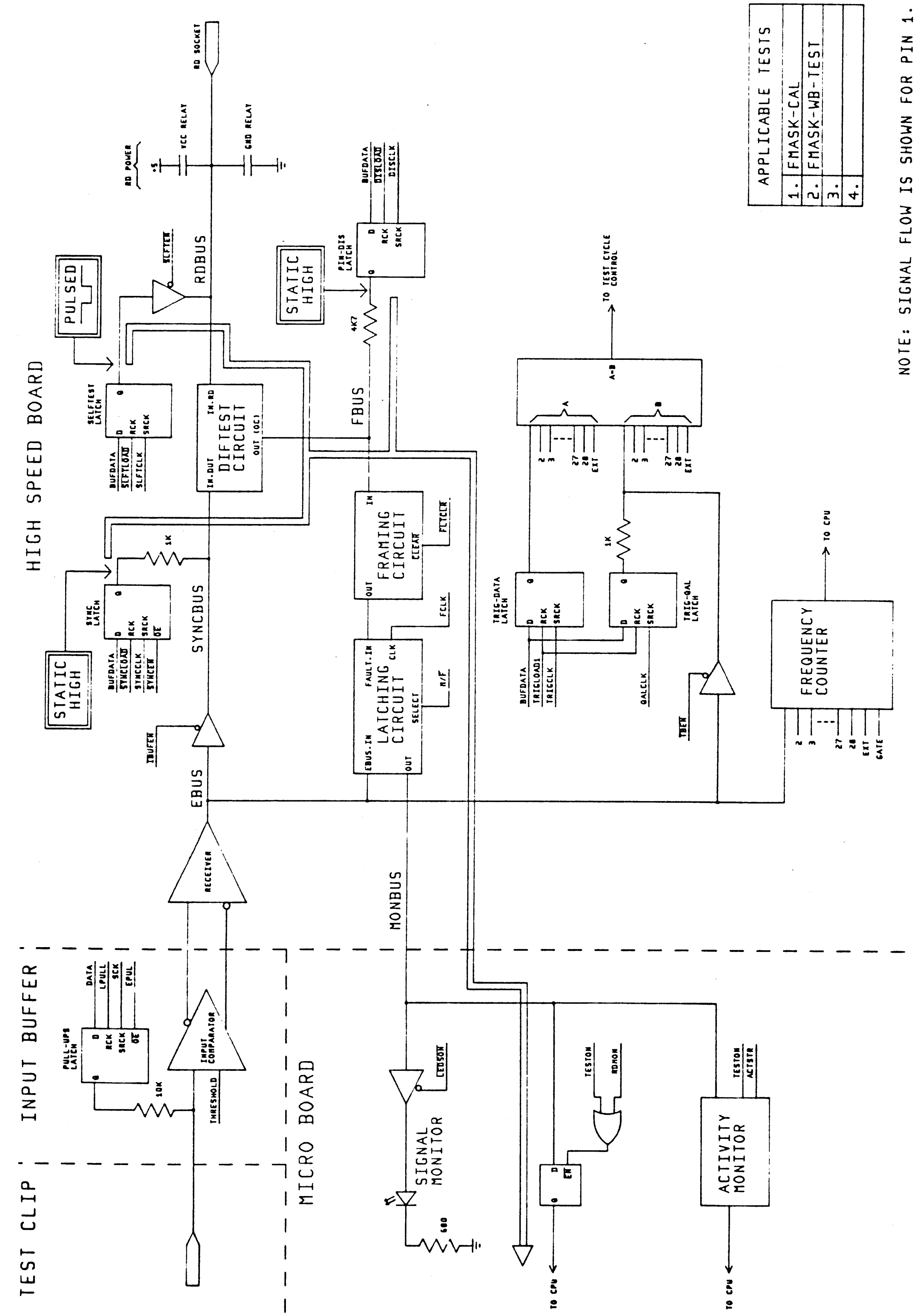
HIGH SPEED BOARD
TEST CLIP
INPUT BUFFER
MICRO BOARD
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
RECEIVER
INPUT COMPARATOR
SIGNAL MONITOR
ACTIVITY MONITOR
FREQUENCY COUNTER
1. STATIC HIGH
2. STATIC LOW
1. WALKING 0
2. WALKING 1
APPLICABLE TESTS
1. QAL0-EQUAL
2. QAL1-EQUAL
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.


HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
RD SOCKET
RD POWER
VCC RELAY
GND RELAY
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
SELFTEST LATCH
SYNC LATCH
PIN-DIS LATCH
PULL-UPS LATCH
INPUT COMPARATOR
THRESHOLD
RECEIVER
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
TRIG-DATA LATCH
TRIG-QAL LATCH
TO TEST CYCLE CONTROL
1. WALKING 0
2. WALKING 1
1. STATIC HIGH
2. STATIC LOW
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
TO CPU
1K
4K7
10K
APPLICABLE TESTS
1. TRIG0-EQUAL
2. TRIG1-EQUAL
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.


APPLICABLE TESTS
1. PULL0-TRIG-EQUAL
2. PULL1-TRIG-EQUAL
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.
HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
1. WALKING 0
2. WALKING 1
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
1. STATIC HIGH
2. STATIC LOW
STATIC HIGH
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR

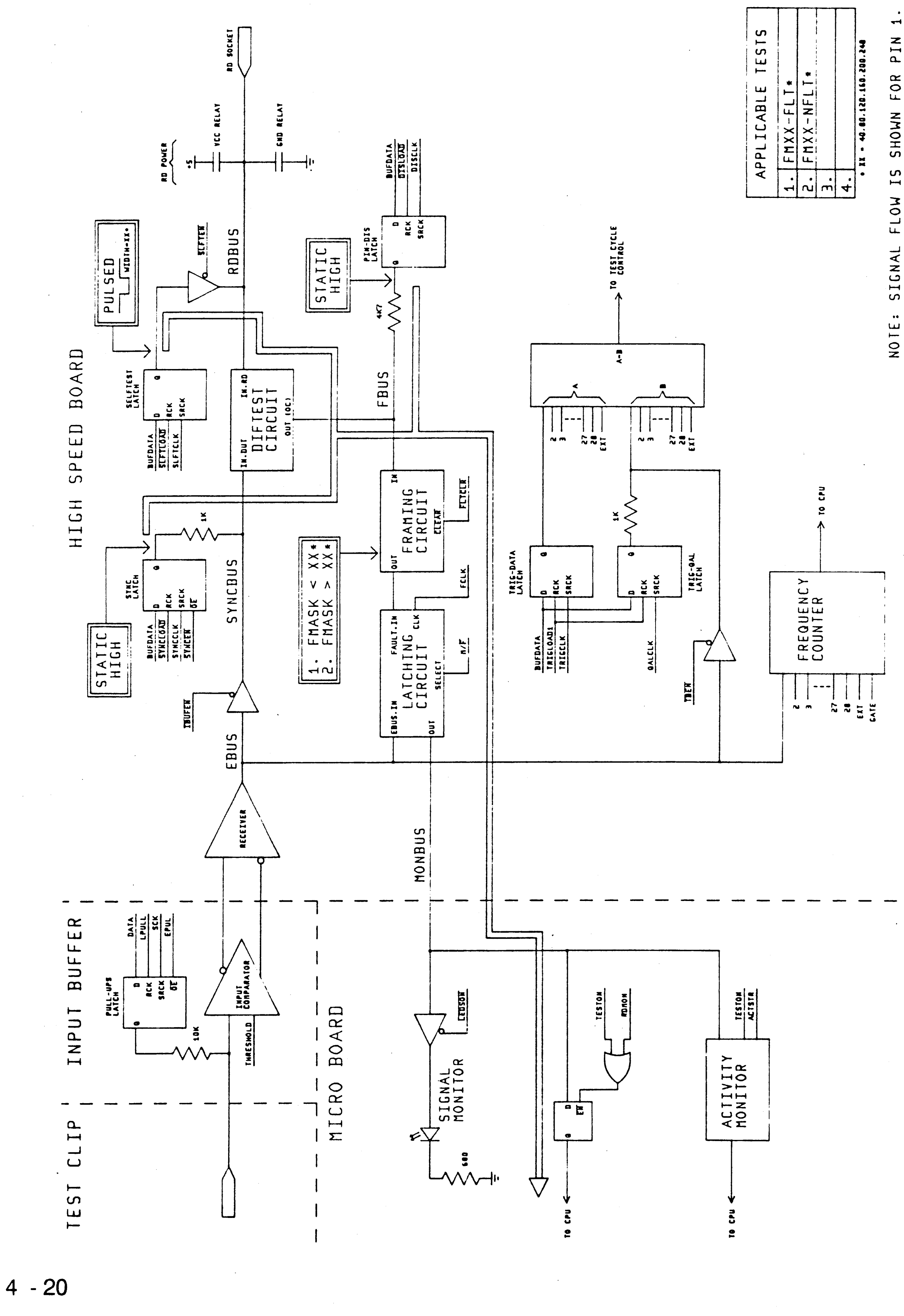

APPLICABLE TESTS
1. PULLO-TRIGQAL
2.
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.
TEST CLIP
INPUT BUFFER
HIGH SPEED BOARD
MICRO BOARD
WALKING 0
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
STATIC LOW
STATIC HIGH
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
RECEIVER
INPUT COMPARATOR

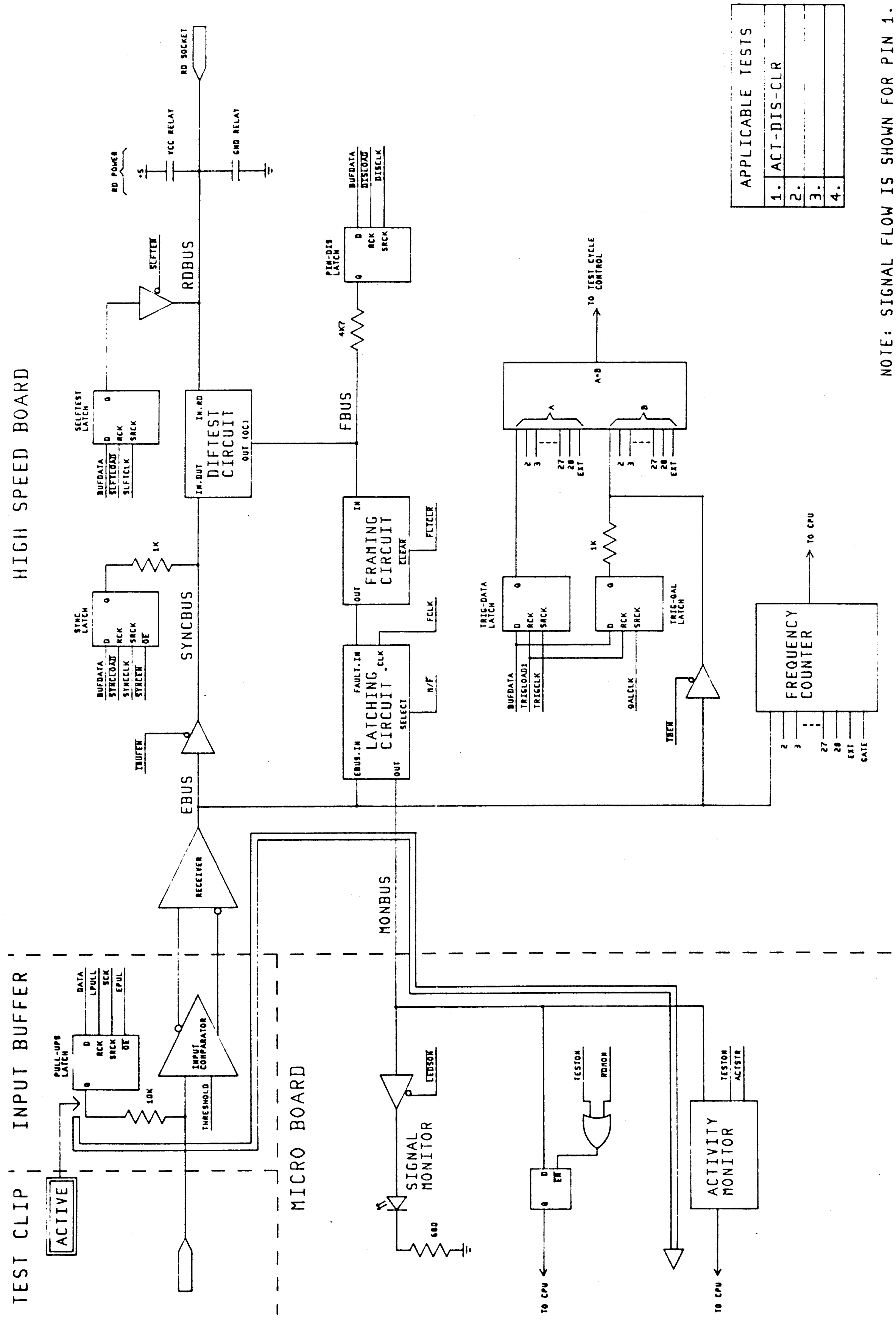

APPLICABLE TESTS
1. FM-STAT-NFLT
2. FM-STAT-FLT
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.
HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
STATIC HIGH
STATIC HIGH
1. STATIC HIGH
2. STATIC LOW
RD SOCKET
VCC RELAY
GND RELAY
RD POWER
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
FREQUENCY COUNTER
RECEIVER
INPUT COMPARATOR
THRESHOLD
SIGNAL MONITOR
ACTIVITY MONITOR
SELFTEST LATCH
SYNC LATCH
PIN-DIS LATCH
TRIG-DATA LATCH
TRIG-QAL LATCH
PULL-UPS LATCH
TO TEST CYCLE CONTROL
TO CPU
TO CPU
TO CPU

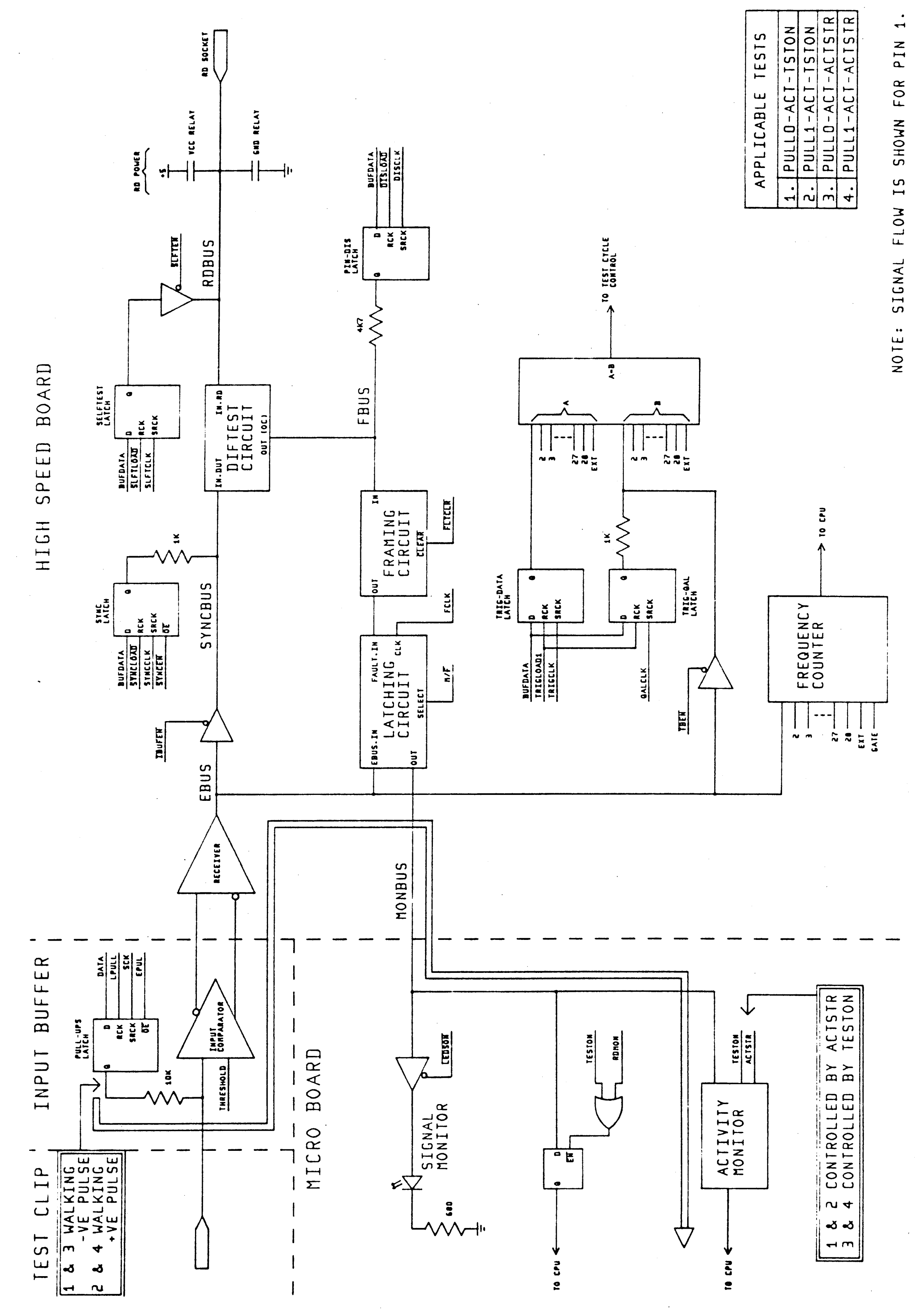


APPLICABLE TESTS
1. FMASK-CAL
2. FMASK-WB-TEST
3.
4.

NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.


HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
APPLICABLE TESTS
1. FMXX-FLT*
2. FMXX-NFLT*
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.
RD SOCKET
RD POWER
VCC RELAY
GND RELAY
RDBUS
PULSED
STATIC HIGH
SELFTEST LATCH
PIN-DIS LATCH
DIFTEST CIRCUIT
FBUS
TO TEST CYCLE CONTROL
SYNC LATCH
SYNCBUS
FRAMING CIRCUIT
1. FMASK < XX*
2. FMASK > XX*
LATCHING CIRCUIT
TRIG-DATA LATCH
TRIG-QAL LATCH
FREQUENCY COUNTER
TO CPU
EBUS
RECEIVER
MONBUS
PULL-UPS LATCH
INPUT COMPARATOR
THRESHOLD
SIGNAL MONITOR
ACTIVITY MONITOR


HIGH SPEED BOARD
TEST CLIP
INPUT BUFFER
MICRO BOARD
ACTIVE
RD SOCKET
RDBUS
SYNCBUS
EBUS
FBUS
MONBUS
RECEIVER
INPUT COMPARATOR
THRESHOLD
DIFTEST CIRCUIT
FRAMING CIRCUIT
LATCHING CIRCUIT
FREQUENCY COUNTER
SIGNAL MONITOR
ACTIVITY MONITOR
TO TEST CYCLE CONTROL
TO CPU
APPLICABLE TESTS
1. ACT-DIS-CLR
2.
3.
4.
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.



HIGH SPEED BOARD
INPUT BUFFER
TEST CLIP
MICRO BOARD
1 & 3 WALKING -VE PULSE
2 & 4 WALKING +VE PULSE
RD SOCKET
VCC RELAY
GND RELAY
RD POWER
RDBUS
SELFTEST LATCH
DIFTEST CIRCUIT
SYNC LATCH
SYNCBUS
EBUS
FBUS
PIN-DIS LATCH
FRAMING CIRCUIT
LATCHING CIRCUIT
RECEIVER
INPUT COMPARATOR
THRESHOLD
PULL-UPS LATCH
MONBUS
SIGNAL MONITOR
ACTIVITY MONITOR
TRIG-DATA LATCH
TRIG-QAL LATCH
FREQUENCY COUNTER
TO TEST CYCLE CONTROL
TO CPU
APPLICABLE TESTS
1. PULL0-ACT-TSTON
2. PULL1-ACT-TSTON
3. PULL0-ACT-ACTSTR
4. PULL1-ACT-ACTSTR
1 & 2 CONTROLLED BY ACTSTR
3 & 4 CONTROLLED BY TESTON
NOTE: SIGNAL FLOW IS SHOWN FOR PIN 1.

4.4 Failure Examples

4.4.1 IB Reversal

This failure usually results in error on lines 9, 10, 19, 20. The following components will be damaged:

U8, U9, U10, RN40, RN41

```
File: SELFTEST_RESULT.sys:SYST

    Selftest results

Software version: X.XX
Library version: X.XX

HSB rev: 1
     - Delayed Gate Installed

MB rev: 0

IB rev: 0

General results:
     x1111 11111 11111 10000 00010 01111
     01010 10101 01111 11x0x x0xxx xxxxx

Flags:
     00000000 10000000 00000000 00001100
     00000000 00000000 00000000 00000000

Individual results:
   1 00001111 11111111 11111111 11111111
   2 00001111 11111111 11111111 11111111
   3 00001111 11111111 11111111 11111111
   4 00001111 11111111 11111111 11111111
   5 00001111 11111111 11111111 11111111
   6 00001111 11111111 11111111 11111111
   7 00001111 11111111 11111111 11111111
   8 00001111 11111111 11111111 11111111
   9 00001111 11111111 11111111 11111111
  10 00001111 11111111 11111111 11111111
  11 00001111 11111111 11111111 11111111
  12 00001111 11111111 11111111 11111111
  13 00001101 00101000 00101000 00000000
  14 00000100 00110100 10101010 10100010
  15 00011111 11111111 11111111 11111111
  23 00011111 11111111 11111111 11111111
  26 00001111 11111111 11111111 11111111
  27 00001111 11111111 11111111 11111111
  28 01000000 00000000 00000000 00000000
  29 00001111 11111111 11111111 11111111
  31 00001111 11111111 11111111 11111111
  33 00001111 11111111 11111111 11111111
  35 00001111 11111111 11111111 11111111
  37 00001111 11111111 11111111 11111111
  39 00001111 11111111 11111111 11111111
  41 00010000 00000000 00000000 00000000
  42 00001111 11111111 11111111 11111111
  43 00001111 11111111 11111111 11111111
  44 00001111 11111111 11111111 11111111
  45 00001111 11111111 11111111 11111111
  46 00001000 11000110 00010000 00000000
```

4.4.2 Static-blown HSB

Damage usually occurs due to touching of J1 or J2 connector. Most of the time the only component needing replacement will be differential ECL receiver.

```
File: SELFTEST_RESULT.sys:SYST

     Selftest results

Software version: X.XX
Library version: X.XX

HSB rev: 1
      - Delayed Gate Installed

MB rev: 0

IB rev: 0

General results:
     x1111 00000 00000 00000 00010 00000
     00000 00000 00111 11x0x x0xxx xxxxx

Flags:
     00000000 00000000 00000000 00000100
     00000000 00000000 00000000 00000000

Individual results:
  1 00000000 00000010 00000000 00000000
  2 00000000 00000010 00000000 00000000
  3 00000000 00000010 00000000 00000000
  4 00000000 00000010 00000000 00000000
 23 00000000 00000010 00000000 00000000
 42 00001111 11111111 11111111 11111111
 43 00000000 00000010 00000000 00000000
 44 00000000 00000010 00000000 00000000
 45 00000000 00000010 00000000 00000000
 46 00001000 00000000 00000000 00000000
```

4.4.3 Missing -5 V

Mostly due to faulty power supply, this failure will affect almost all tests.

```
        File: SELFTEST_RESULT.sys:SYST

       FLUKE 900 - Selftest results

Software version: X.XX
Library version: X.XX

HSB rev: 0

MB rev: 0

IB rev: 0

General results:
    x1111 00000 00000 10000 00001 00000
    00000 00000 01111 11x0x xxxxx xxxxx

Flags:
    00000000 00000000 00000000 00000100
    00000000 00000000 00000000 00000000

Individual results:
  1 00000000 00000000 00001111 01000000
  2 00000000 00000000 00001111 01000000
  3 00000000 00000000 00001111 01000000
  4 00000000 00000000 00001111 01000000
 15 00000000 00000000 00001111 01000000
 24 00000000 00000000 00001110 01000000
 41 00010000 00000000 00000000 00000000
 42 00001111 11111111 11111111 11111111
 43 00001111 11111111 11111111 11111111
 44 00000000 00000000 00001111 01000000
 45 00000000 00000000 00001111 01000000
 46 00001000 00000000 00000000 00000000
```

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5 Maintenance

5.1 Performing a Complete System Checkout

The Basic Functional Test is built into the system software as the power on selftest, which takes about 1 minute.

- Power the Fluke 900 up by setting the power switch to position "1".
- Monitor results of the built-in selftest. It should pass and proceed to the initial screen.
- Check the System Firmware Revision indicated at the bottom of the LCD display. All systems should have version 4.09 or higher. Systems with the Simulation Option (900-001) must have version 5.05 or higher. All systems can have the Learn feature and extended FMask and Threshold ranges when fitted with System Firmware Revision 6.00 or higher. The most current Library Firmware Revision (as of January 1992) is 6.00. It has only minor device additions to version 5.00, the recommended minimum.

The Extended Functional Test checks features which cannot be tested during the power up selftest (eg. RS232), or which have LED visual display only.

- Put the Fluke 900 into debug mode (refer to Section 1.2 for instructions).

  Run test 50 (RS232) to verify that it passes. Note that no external device should be connected to the RS232 port during this test.
- Run test E60 to check the size LEDs with walking 1 and 0 patterns.
- Run test E62 to check the monitor LEDs with walking 1 and 0 patterns.
- Run test E76 to verify test cycle control. Ignore failures in BYTE1 of the test results.

The following procedure will register the limits of the power supply output voltage.

- From debug mode run test E63 continuously for as long as monitoring is required (usually about 5 minutes).
- Stop the execution of the test by pressing any key. It will not display voltage results on this menu, but will on the Engineering Menu as explained below. Return to the main screen by pressing CNTR three times.
- Bring up the special Engineering Menu by simultaneously pressing ESC and an unlabelled keyswitch found between NEXT and TEST . Press F4(Vcc) and the upper and lower voltage limits will be displayed, as they are measured on the Interface Buffer.
- Vcc should be between 5.00 and 5.04 volts.

5.2 Performing Adjustments

5.2.1 Adjustment to Vcc

The Vcc level is adjustable over a narrow range around 5.0 volts from a potentiometer on the power supply module.

- With the unit face-down and power off, remove the four screws from the bottom of the unit which hold the upper and lower halves together. Turn the unit face-up. The right side of the top half may be raised up and to the left, somewhat like opening a book, while still maintaining electrical connections between the two halves. This permits access to the PS potentiometer.
- Power up the unit and wait for a successful selftest.
- Follow the procedure outlined at the end of Section 5.1 to enter the Engineering Menu and display the Vcc value. The potentiometer may be reached through a hole in the top of the power supply cover. It is located in the middle of the edge closest to the center of the unit. The value should be set to about 5.02 to be within the limits of 5.00 to 5.04 volts.

5.2.2 Adjustment to Display Contrast

The display contrast is adjustable from a potentiometer on the Micro Board.

- With the unit face-down and power off, remove the four screws from the bottom of the unit which hold the upper and lower halves together. Turn the unit face-up. The right side of the top half may be raised up and to the left, somewhat like opening a book, while still maintaining electrical connections between the two halves. This permits access to the potentiometer.

  Power up the unit and observe the main screen while turning the potentiometer located on the Micro Board near the Display Controller connector.

5.2.3 Changing System Firmware

The main screen after a successful power up selftest indicates the system firmware revision on the left and the library firmware revision on the right. System firmware resides on 4 EPROMs, standard library firmware on a single EPROM and custom library firmware on a single EPROM (eg. Simulation Library for Sales Demo UUT).

- Remove the Micro Board as described in Section 5.3.
- Remove the existing EPROMs and insert new ones according to the following list:

U60	SYS-AF
U61	SYS-B
U76	SYS-C
U77	SYS-D
U74	Custom Library EPROM (if present)
U75	Standard Library

The EPROM positions are shown in the layout diagram of Section 6 (Schematics). Do not Mix the EPROM devices as the unit will not operate properly.

- Reassemble the unit by reversing the disassembly instructions. In particular, make sure that the display controller, speaker wires and keyboard cables are connected. It is recommended that you not screw the top and bottom parts together with the final 4 screws, until you verify that the tester passes selftest.

5.2.4 Fuses and 110/220 V Conversion

The line fuse is located in a recessed compartment next to the power cord receptacle. To replace it, remove the power cord and slide the clear plastic panel over, exposing the fuse receptacle. Pull the black plastic lever to pop out the fuse. The proper rating for replacement fuses is 3A, 250 V.

For conversion between 120 V and 240 V, the small circuit card under the fuse must be removed, turned over and reinserted. The voltage setting is marked appropriately on each side of the card. To slide the clear plastic cover over completely to allow removal of the small card, it is necessary to flex the adjacent top cover of the tester.

5.3 Disassembly and Assembly Instructions

Before replacing any system modules, turn the unit off, remove the power cord and disconnect the Interface Buffer.

5.3.1 Microprocessor Board

1. With the unit face-down, remove the four screws from the bottom of the unit which hold the upper and lower halves together.

2. Turn the unit face-up and raise the right side of the top half up and to the left, somewhat like opening a book. This will expose a connector (J3) which attaches the two halves.

3. Press the ejectors at either end of the male connector and remove the mating female connector. The two halves should now be completely separated.

4. Remove the connector (upper left area of top half, component side) attaching the Micro Board to the Display Controller Board.

5. Remove the two speaker wires from their mating jacks (upper left area of top half, component side).

6. Remove the five screws and one nut which fasten the Micro Board to the top half of the unit and carefully lift the board out slightly. Note that the LEDs around the ZIF socket may adhere to the keyboard decal and require gentle pressure to separate.

7. Disconnect the two keyboard connectors from the Micro Board and remove the board completely.

8 To reinstall the Micro Board, first connect the two keyboard connectors to the new Micro Board. Put the new board in place.

9. Follow steps 6 through 1 (reversing the instructions). Note that a grounding wire is installed under the nut on the metal standoff. Some earlier models have selftapping screws that fit directly into the plastic standoffs. Do not tighten these too much as the plastic threads may be stripped. Most units have metal inserts in the standoffs and machine screws.

5.3.2 Keyboard

1. Follow steps 1 through 7 in Section 5.3.1.

2. Peel the keyboard away from the top cover and discard.

3. Clean the surface of the top cover if necessary such that nothing will prevent the new keyboard from laying flat.

4. Insert the new keyboard connectors through the opening in the top cover.

5. Peel away the backing on the new keyboard and carefully place it onto the top cover such that the LED and ZIF socket cutouts line up. The keyboard should fit into the indented area in the top cover.

6. Apply pressure in smoothing out the keyboard in order to work any air bubbles which may be trapped under it.

7. Reassemble as in step 9 in Section 5.3.1.

5.3.3 Speaker

1. Follow steps 1 through 7 in Section 5.3.l.
2. Remove the 4 screws which attach the speaker to the top cover.
3. Put the new speaker in place and install the 4 mounting screws.
4. Reassemble as in steps 8 and 9 of Section 5.3.1.

5.3.4 Display Controller

1. Follow steps 1 through 7 in Section 5.3.l.
2. Remove the 4 screws which attach the Display Controller Board to the top cover.
3. Move the cables from the old Controller Board to the new one, maintaining their orientation.
4. Ensure that the new Controller Board has the correct character generator installed. Replace if necessary.
5. Position the board onto its mounting holes and install the 4 mounting screws.
6. Reassemble as in steps 8 and 9 of Section 5.3.l.

5.3.5 Display

1. Follow steps 1 through 7 in Section 5.3.l.
2. Remove the 4 screws which fasten the display to the top cover.
3. Move the cable attached to the old display to the new display.
4. Ensure that the plastic window (top cover) is clean.
5. Position the new display against the plastic window and insert the 4 screws in their previous mounting position. Screw them in only lightly.
6. Power up the unit and verify that the bottom line of the display lines up properly with the edge of the keyboard. If not it may be repositioned before a final tightening of the 4 mounting screws.
7. Reassemble as in steps 8 and 9 of Section 5.3.l.

5.3.6 High Speed Board

1. Follow steps 1 through 3 in Section 5.3.1
2. Remove the 7 screws fastening the High Speed Board to the bottom cover.
3. Disconnect the power connector (J4).
4. Place the new board into position and follow steps 3 through 1, reversing the instructions.

5.3.7 Power Supply

1. Follow steps 1 through 3 in Section 5.3.1
2. Remove the 4 screws fastening the power supply top cover to the bottom enclosure.
3. Remove the 4 corner screws fastening the bottom enclosure to the standoff pillars. Remove the fifth screw on the bottom enclosure that is found between the fan and corcom AC connector.
4. Disconnect the power connector from the High Speed Board.
5. Follow steps 4 through 1, reversing the instructions, to reinstall.

5.3.7.1 Fan

1. Remove the Power Supply as described in the previous section.
2. Remove the 4 screws fastening the fan to the PS bottom enclosure.
3. Cut the red and black fan power wires about one inch from the fan.
4. Discard the old fan and connect new power wires to the red and black wires.

   Note: Connections are to be soldered and covered with heat shrinkable tubing to insulate them.

5. Attach the new fan to the PS enclosure with its 4 screws.
6. Follow steps 4 through 1 in Section 5.3.7, reversing the instructions to reinstall the Power Supply.

5.3.8 Interface Buffer Board

1. With the unit turned off, disconnect the J1 and J2 connectors which attach the Interface Buffer to the main unit.
2. Remove the cover from the Interface Buffer.
3. Remove the 4 screws securing the board to the bottom cover.
4. Place new board in position and fasten it to the bottom cover with the 4 screws.
5. Replace the top cover.

5.4 Calibration Procedures

The Interface Buffer and the High Speed Board are calibrated during the manufacturing process. After service repair of one of the signal channels, it should be calibrated again in a known-good machine.

5.4.1 Interface Buffer Calibration

Remove the cover of the IB and connect J1 and J2 ribbon cables to the HSB. Turn the power on and wait for completion of the selftest. Select debug mode and run test 46 (Freq_bias_short). This may be run in looping fashion as well . Two offset values appear on the screen. They will be within + or - 10 when the IB is calibrated properly.

Resistor R57 determines the offset values. Trial and error selection of a value between 350K and 450K is the recommended procedure. First remove R57 so it is open circuit and gives a large negative offset value. Then connect jumper leads to U25 pin3 and U26 pin1 (these are the endpoints of R57). While test 46 is looping, connect various resistors to the jumper leads until an acceptable offset value is achieved.

5.4.2 High Speed Board Calibration

This section describes the HS Board fault mask calibration procedure, the preliminary conditions and the final criteria to be met to consider a board calibrated. The main requirement is that the absolute value of the offset for all pins be less than or equal to 4. Also described is the way to isolate faulty chips in some special cases related to fmask calibration.

5.4.2.1 Calibration Data Format

The calibration data printout consists of seven blocks. The first one's header is "Limits table", and this name will be used to refer to the block.

The rest have a common header: "F_MASK offset table". These blocks will be referred to with their individual headers: "duration 40 ns", "duration 80 ns" up to "duration 240 ns" or simply "40 ns", "80 ns", etc.

Each block consist of five columns, the first being pin number, the other four being "offsets". In other words, each pin has four offsets labeled U-H, D-H, U-L, D-L.

NOTE: The first two columns in Limits Table Block are meaningless and should be ignored.

5.4.2.2 Calibration Standards

The main condition standard is that the absolute value of the offset for all pins should be less or equal to 4. A board that fulfills this condition and passes all tests in the selftest is considered calibrated and does not need any further adjustments.

NOTE: the first block (Limits table) does not need to fulfill this condition if all other blocks are OK.

In each block, the line with the biggest offset is marked with a ">" character so only such lines need to be checked. This rule does not apply to limits table block which has to be checked line after line if needed.

5.4.2.3 HSB Component Placement

There are seven white rectangles outlined on the HS Board that are called F1,F2,..,F7. F1 is located at the bottom, then F2 and so on. Within each rectangle there are four identical fields designated UB1, UB2, UB3, UB4. A 74ALS09 chip is placed between UB2 and UB3. Each UB field has a place for an additional resistor and capacitor (see fig. 1). Whenever the word "resistor" or "capacitor" is used in this section, it relates to these additional components. The words channel, line and pin are used to mean one of the 28 signal paths.

The following table relates the 28 channels to the components in the UB fields.

Area	UB1	UB2	UB3	UB4
F7	1	27	28	2
F6	4	24	26	3
F5	5	23	25	6
F4	20	9	22	7
F3	21	19	10	8
F2	16	12	18	11
F1	15	13	17	14

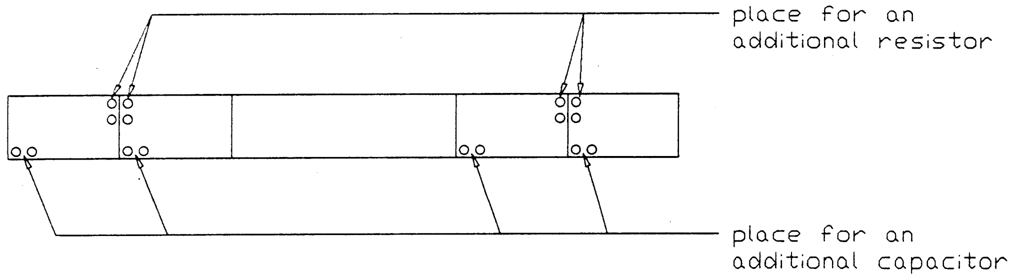

fig. 1

5.4.2.4 The Offset Shift (OS) Definition

For any line that needs to be corrected the necessary shift should be determined. The general rule is: if there are excessive negative offsets a resistor will be put on this line, and if there are excessive positive offsets a capacitor will be used.

OS should be calculated for the calibration data block that has the biggest offset for a given channel.
NOTE: Limits table cannot be used for OS calculation.

The OS calculating procedure is explained with the two following examples.

5.4.2.4.1 Example 1 (for negative offsets)

Assume line 3 has the biggest offset in 80 ns block.

```
          ..80 ns..

pin#  U-H  D-H  U-L  D-L
 .     .    .    .    .
 3    -3   -4   -5   -7
 .     .    .    .    .
```

The biggest offset is D-L. It has to be moved up 3 units to make it -4 and therefore within spec. All other offsets will be moved by the same amount, therefore U-H will be 0. The best situation, however, is when there is a safety margin at the top and the bottom. In this case all offsets should be moved up by 5 units. Then after correction it would be:

```
      ...80 ns..

pin#  U-H  D-H  U-L  D-L
 .     .    .    .    .
 3    +2   +1    0   -2
 .     .    .    .    .
```

According to table 1 in Section 5.4.2.5 , a 47K resistor should be used (it gives OS 5). Other blocks will be also affected by this resistor. Therefore, all of them have to be checked to determine whether they are still within specification. If any block is pushed out of spec with this resistor (for example if 240 ns has offset 0 it will be 4 after correction) the OS calculation procedure has to be repeated. OS is acceptable if all blocks are within +-4 margin after correction.
If the OS and resistor cannot be defined (if the smallest possible OS in one block pushes another one out of spec) go to Section 5.4.2.6.2.

5.4.2.4.2 Example 2 (for positive offsets)

Assume line 5 has the biggest offset in 160 ns block.

```
            ..160 ns..
pin#  U-H  D-H  U-L  D-L
 .     .    .    .    .
 5    +3   +4   +6   +6
 .     .    .    .    .
```

The biggest offset are D-L and U-L. They have to be moved down 2 units to make it +4. Offsets should be moved down by 5 or 4 in order to create the safety margins as in the previous example. If we choose 4 (either of the two values may be selected) it will be:

```
            ..160 ns..

pin#  U-H  D-H  U-L  D-L
 .     .    .    .    .
 5    -1    0   +2   +2
 .     .    .    .    .
```

The needed capacitor can be found using table 2 in Section 5.4.2.5. It is 3.3 pF. All other blocks should be now checked as described in 5.4.2.4.1.
If the OS and capacitor cannot be defined (if the smallest possible OS in one block pushes another one out of spec) go to Section 5.4.2.6.2.

5.4.2.5 The Correcting Component Definition

If a pin has an excessive positive offset, a capacitor has to be added. In case of a too large negative offset a resistor should be used.
The value of the component to be added can be defined with the following tables:
NOTE: All values in the following tables are only approximated; the tolerance is +/- 1.

TABLE 1
Offset Shift

R	40	80	120	160	200	240	Fluke P/N
365k	0	0	0	1	1	1	921168
150k	1	1	2	2	3	3	921171
113k	1	2	2	3	4	4	921176
86k	2	2	3	4	5	5	921184
57k	3	4	5	6	6	7	921189
47k	4	5	6	6	7	8	921192

TABLE 2
Offset Shift

C	40	80	120	160	200	240	Fluke P/N
1.0pF	1	1	1	2	2	2	921197
1.5pF	1	1	2	2	3	3	921200
1.8pF	1	1	2	3	3	3	921205
2.2pF	2	2	3	3	4	4	921213
3.3pF	2	3	3	4	4	5	921218
4.7pF	2	3	4	5	6	6	921221
6.8pF	3	4	6	6	7	8	921226

NOTE: All the offsets in Table 2 are meant as negative (i.e. they must be subtracted from the values in the calibration data printout).

5.4.2.6 Calibration Procedure

As a preliminary condition, the HS Board must pass all selftests with the exception of tests 28 through 40 which are related to the calibration.

Unless otherwise specified all points in the following procedure should be performed in the order stated. First load the calibration data as follows:

- Go to engineering menu: start from the main screen and press [CNTR] and the point between [NEXT] and [TEST].
- Go to calibration mode: press [F5](calib) .
- Press [F1](f_mask) and wait until the loading of data is done.
- Print calibration data to a printer connected to the serial port by pressing [F5](print). The data may also be displayed on the LCD display by pressing [F3](show) .

NOTE: Do not touch HS Board during loading of calibration data.

5.4.2.6.1 Offsets Block

All pins that have offset (one or more) bigger then 4 (positive or negative) should be corrected following the steps:

A - Define OS and component for all pins that need correction (see Section 5.4.2.4).

B - Place all components determined in step A on the board on related lines and then load calibration data again (see Section 5.4.2.6).

C - Press [F3](show) to display the data. Using "SHIFT" and "arrow down" keys, check the data (see Section 5.4.2.2); if there are still lines that need correction, do it the same way as described in step A, with one difference: the offset shift should be selected to be the minimum required with no safety margin.
If after these steps the board is still not calibrated go to Section 5.4.2.6.2

5.4.2.6.2 Limits Block

This block is related to the 74ALS09 chips that are located in F1, F2 etc. areas. There is only one such chip in each area.

Only two columns are relevant: U-L and D-L. The conditions they have to fulfill are as follows:
- each offset should be equal to -2,-1,0,1,2
- the difference between the lowest and the highest offsets should be 2 or less.

Example:

```
pin#      U-L     D-L
           .       .
           .       .
```

```
2      -2     -1
        .      .
15      0      1
        .      .
```

(U-L for pin 2) - (D-L for pin 15) = -2 -1 = -3 (failure)
This means that one of the 74ALS09 chips in F1 or F7 may have the saturation voltage at its output (Vol) too small or too big compared to the rest of '09s. The Vol can be measured by disabling Clip Check and RD Test and running a continuous test. From the main screen, proceed as follows:
- Press F1(manual) to go into Manual Mode
- Select a 28 pin device. Press F1(local) ETC F1(size) 2 8 ENTER.
- Set t_time to continuous. Press ETC F1(t_time) F2(cont.) ENTER.
- Press ESC to go back to the Manual menu.
- Disable RD Test. Press ETC F3(rd) F2(rdt_off) ESC.
- Disable Clip Check. Press F4(clip) F2(clip_chk) F1(on/off) ENTER ESC.
- Insert a 28 pin Test Clip into the Interface Buffer and press TEST.
- Measure, with a DVM, the voltage on the 74ALS09 outputs (it is enough to measure only one output per chip). Note that, for lines 14 and 28, the voltage will be zero because these are power supply lines for the 28 STD size).

74ALS09 chips are classified at the factory according to Vol rating and marked with a colored dot as follows:

Vol (mV)	group	marker
96 - 135	A	white
136 - 174	B	orange
175 - 212	C	green
213 - 251	D	blue
252 - 290	E	red
291 - 329	F	brown

Although these ranges cover all the possible values listed by vendors, it has been found that the normal range of Vol is from 136 to 212. All machines built up to the end of 1992 have 74ALS09 devices with orange or green dot markings.

All 74ALS09 chips on the board have to be from the same group, so the device with Vol too big or too small must be replaced with a properly rated 74ALS09.

After replacement, the calibration procedure should be restarted. If there is no need to replace a chip, go to Section 5.4.2.6.3

5.4.2.6.3 Selftest buffer and 86 gate related condition

The channels with a ">" character in any block should be checked to see if they meet the following conditions:

Check if abs((U-H) - (U-L)) = 0,1,2,3,4,5
abs((D-H) - (D-L)) = 0,1,2,3,4,5
abs((U-H)-(U-L)-(D-H)+(D-L)) = 0,1,2,3,4,5

If not, it means that for some reason there is too large a difference between the propagation time for a rising and falling edge from point A to point B (see fig. 2).

SELFTEST BUFFER

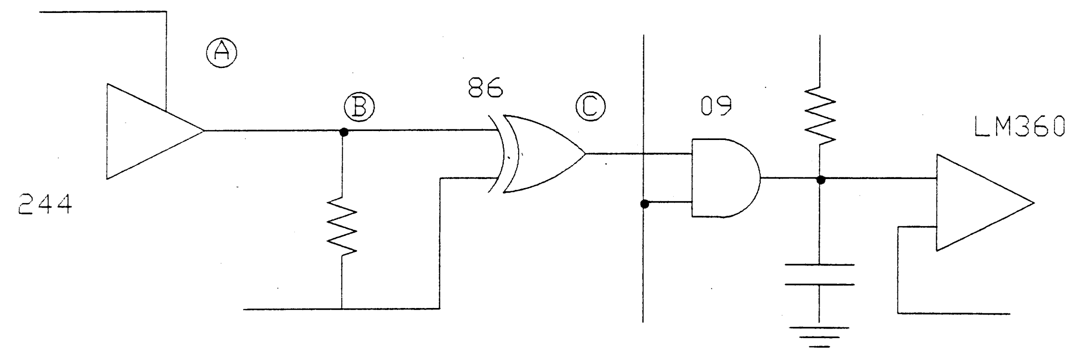

fig.2

The difference may be caused by one of the following:
- selftest buffer 74AS244
- logic comparator 74AHCT86

A bad component may be isolated with an oscilloscope as follows:
Scope setup:

chan A - 1 V/div
B - 1 V/div
timebase - 10 ns/div (100 ns/div and x10 scale)
horizontal
marker - + 1.4 V

Fluke 900 setup:

Bring up the F_Mask Calibration menu. From the main screen, press CNTR and the hidden key found at the point between NEXT and TEST. Press F5(calib) F1(f_mask).

- Connect probe A to the enable input on any 74AS244 selftest buffer (pin 1 or 19) and GND lead to the GND pin of this chip (pin 10).
- Connect probe B to the output of a buffer on this chip and the probe's GND lead to pin 10.
- Press F2(h_fault) and measure t1 and t2 as indicated on figure 3a. Next, connect

probe B to the output of a related '86 gate and measure t3 and t4.
- Press any key to abort the looping activity. Press F4 (l_fault) and measure t5, t6, t7, t8 as indicated on figure 3b. Pressing any key aborts the looping activity.

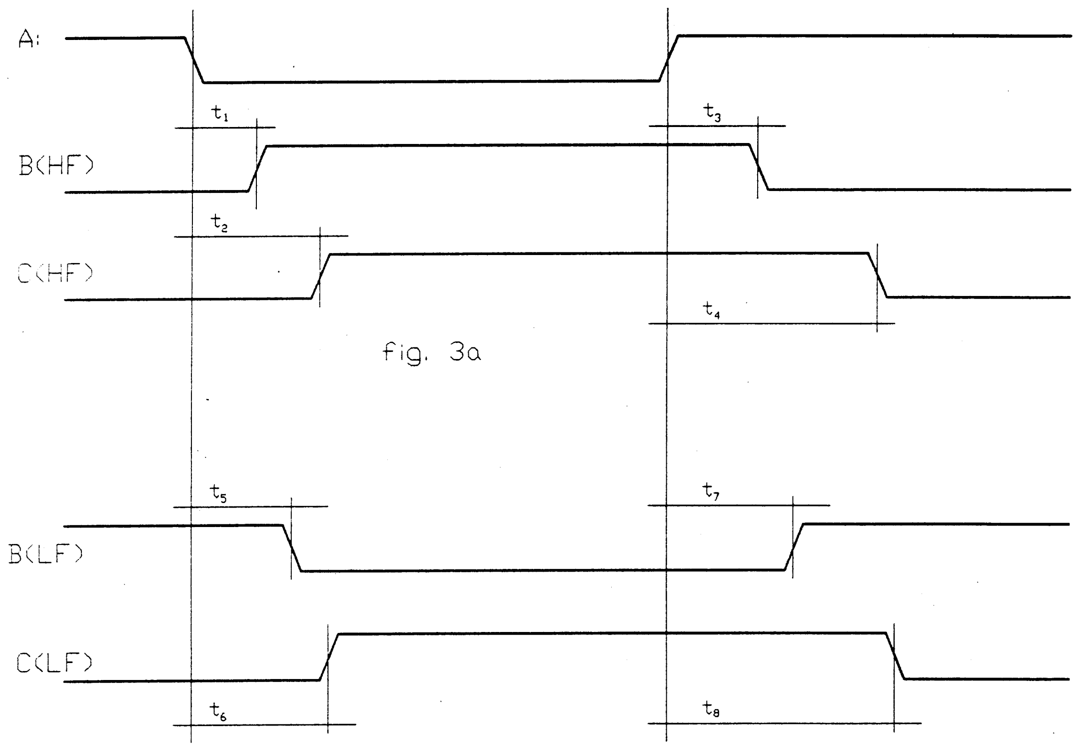

fig. 3b

Calculate the following values:
A = abs(t1-t5)
B = abs(t2-t6)
If A>B then 74AS244 generates too big an offset and should be replaced.
If A<B then 74AHCT86 is faulty and should be replaced.
If A=B then calculate new values:
A = abs(t3-t7)
B = abs(t4-t8)
Now, if A>B then 74AS244 generates too big an offset and should be replaced.
If A<B then 74AHCT86 is faulty and should be replaced.
If A=B any of them may be replaced.
The calibration procedure should then be restarted.

5.4.2.6.4 LM360 comparator related condition

Each pair of columns in the calibration results should differ by no more than 1. As an example:

```
          ..160 ns..

pin#  U-H  D-H  U-L  D-L
 .     .    .    .    .
 5    -1    0   +2   +2
 .     .    .    .    .
```

Check that (U-H) - (D-H) = 0 or +/-1 and
(U-L) - (D-L) = 0 or +/-1

If not, the LM360 comparator on this line is faulty and should be replaced. The calibration procedure should be restarted from the beginning.

5.5 Board Revisions, Upgrades and ECOs

This manual documents all 900 units with serial number 4720000 and above. Units with lower serial numbers are documented in a two volume Service Manual (part numbers 859413, 880195). The boards in such machines are designated IB, MB, M1, M2 and H1.

The table below lists the boards and ECOs applicable to the 900 revision level described in this manual.

BOARD	REVISION PCB #	APPLICABLE ECOs
Interface Buffer (IB)	300-506C	none
High Speed Board (HS2)	300-508-2	HS2 has factory-installed ECOs which make it equivalent to HS3
High Speed Board (HS3)	300-508-3	none
Micro Board (MB2)	300-507-2	ECO-016, ECO-018

5.5.1 Modification to MB for 64k Cartridges

ECO-016
This connects the 16th address line to the cartridge port.

Install wire from U9 pin 17 to J8 pin 5.

ECO-018
This connects the 16th address line to the cartridge buffer.

Install wire from U9 pin 3 to J6 pin 30.

5.5.2 900 System Firmware

The version of the 900 documented in this manual requires firmware level 5.00 or higher. At the end of 1992, the most current firmware was 6.00 . Refer to Section 5.2.3 for instructions on upgrading firmware.

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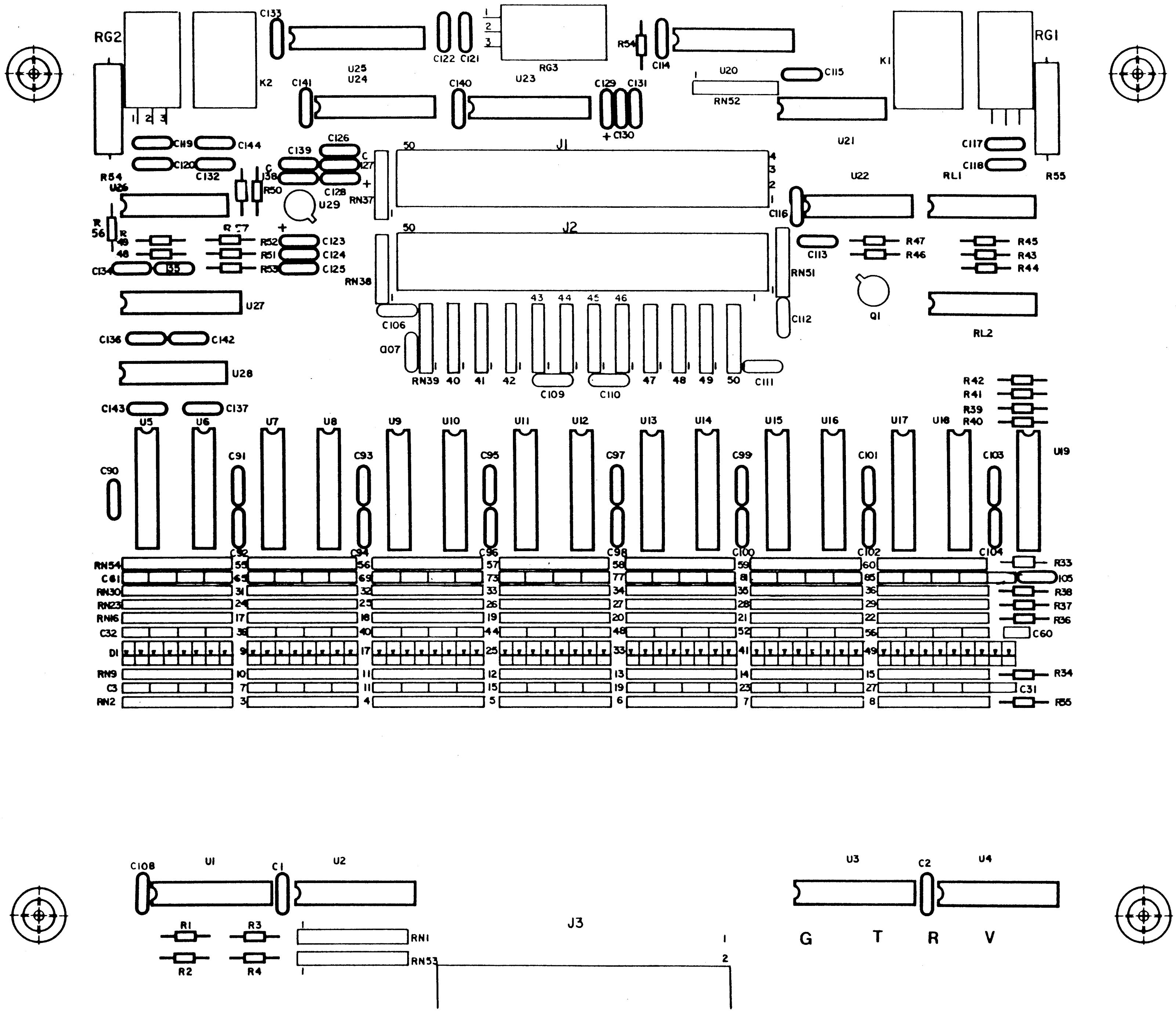
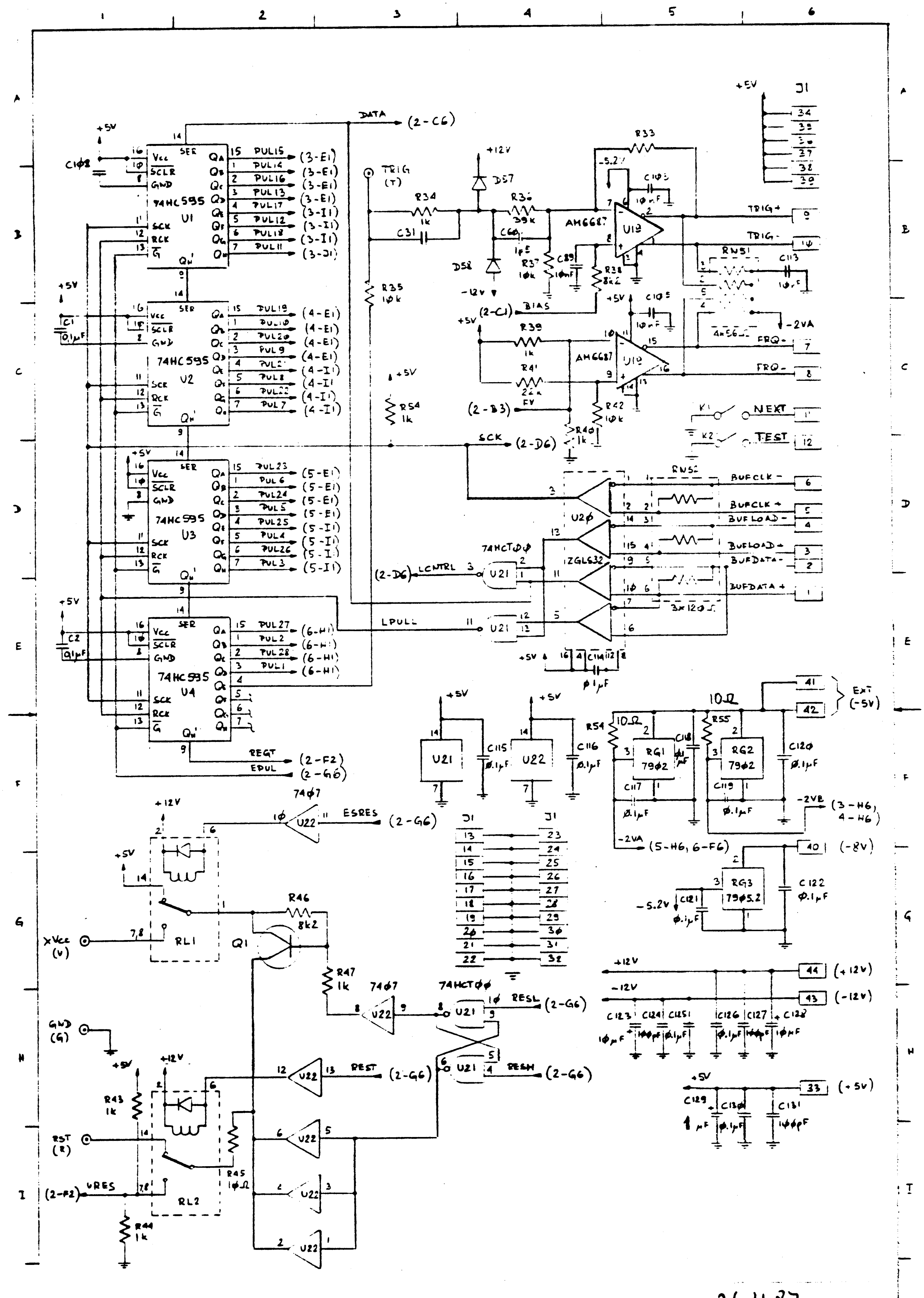
6 Schematics

6.1 INTERFACE BUFFER - IB

1 Layout Page
6 Schematic Pages


RG2
K2
U25
U24
U23
RG3
U20
RN52
K1
RG1
U21
J1
J2
U22
RL1
RL2
Q1
U26
U27
U28
U29
RN37
RN38
RN39
RN51
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
RN54
C61
RN30
RN23
RN16
C32
D1
RN9
C3
RN2
U1
U2
U3
U4
C108
C1
C2
R1
R2
R3
R4
RN1
RN53
J3
G
T
R
V



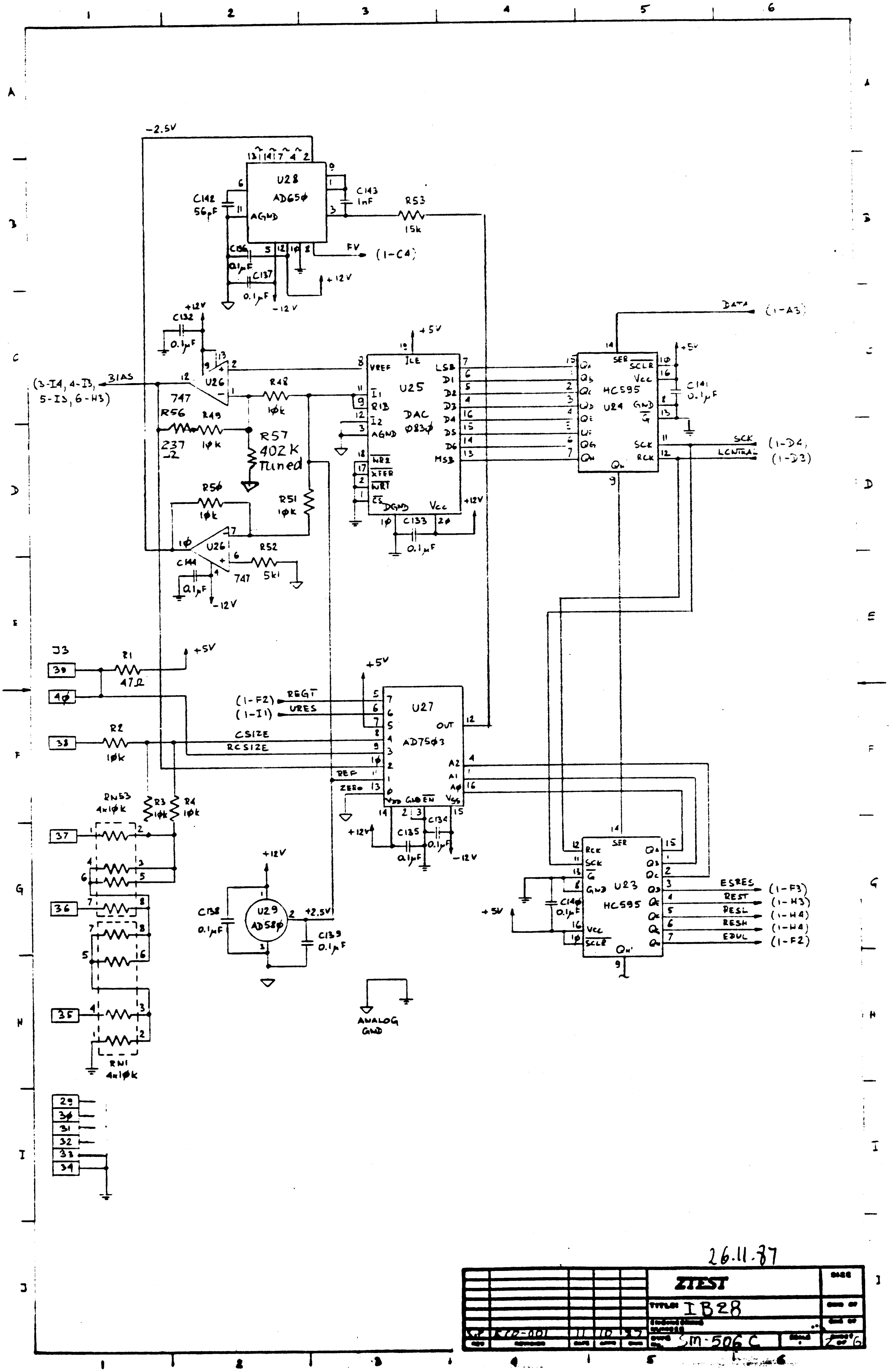
26.11.87

ZTEST

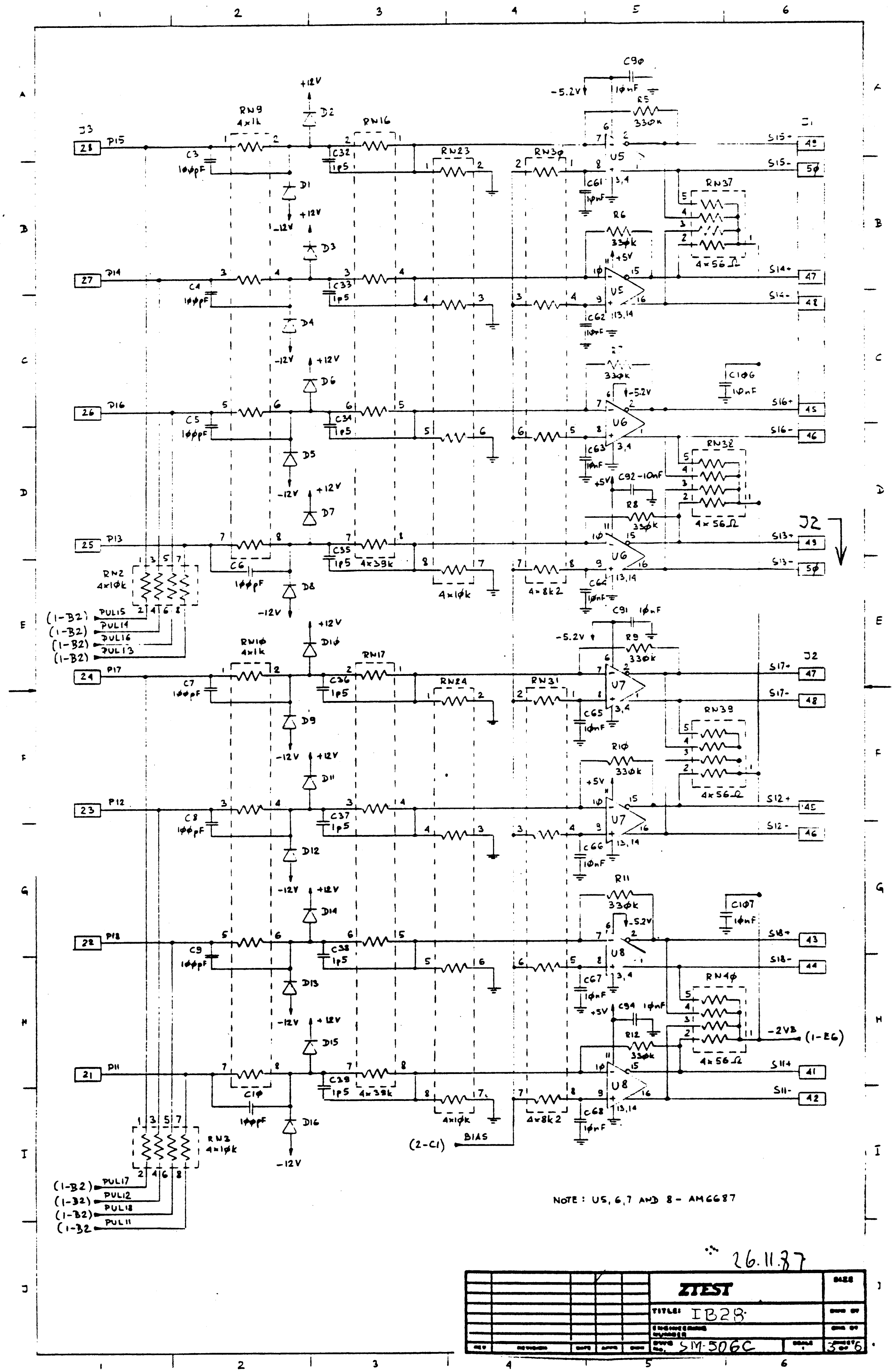
TITLE: IB28

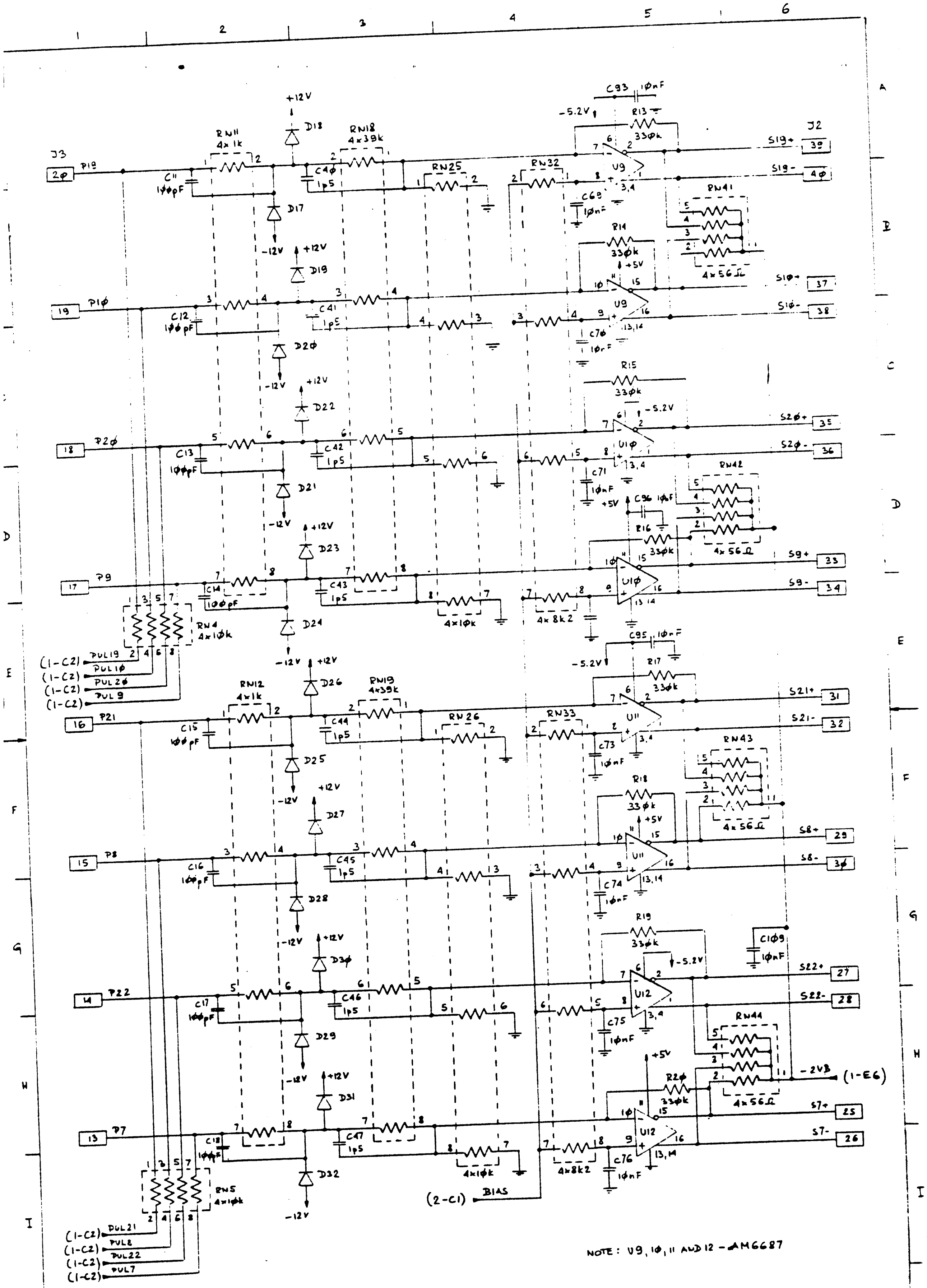
DWG No. SM-506C

SHEET 1 OF 6



-2.5V
U28
AD650
C142 56pF
C143 1nF
R53 15k
FV (1-C4)
C136 0.1μF
C137 0.1μF
+12V
-12V
DATA (1-A3)
C132 0.1μF
BIAS (3-I4, 4-I3, 5-I3, 6-H3)
U26 747
R48 10k
R56 237 -2
R49 10k
R57 402K Tuned
U25 DAC 0830
+5V
R50 10k
R51 10k
U26 747
R52 5k1
C144 0.1μF
C133 0.1μF
HC595 U24
C141 0.1μF
SCK (1-D4,
LCNTRL (1-D3)
J3
R1 47Ω
+5V
(1-F2) REGT
(1-I1) URES
U27 AD7503
R2 10k
CSIZE
RCSIZE
REF
ZERO
RN53 4x10k
R3 10k
R4 10k
C134 0.1μF
C135 0.1μF
U29 AD580
C138 0.1μF
C139 0.1μF
+2.5V
ANALOG GND
U23 HC595
C140 0.1μF
ESRES (1-F3)
REST (1-H3)
RESL (1-H4)
RESH (1-H4)
EDUL (1-F2)
RN1 4x10k
26.11.87
ZTEST
TITLE IB28
SM-506C
2 of 6


NOTE: U5, 6, 7 AND 8 - AM6687
26.11.87
ZTEST
TITLE: IB28
DWG No. SM-506C
SHEET 3 OF 6



NOTE: U9, 10, 11 AND 12 - AM6687

26.11.87

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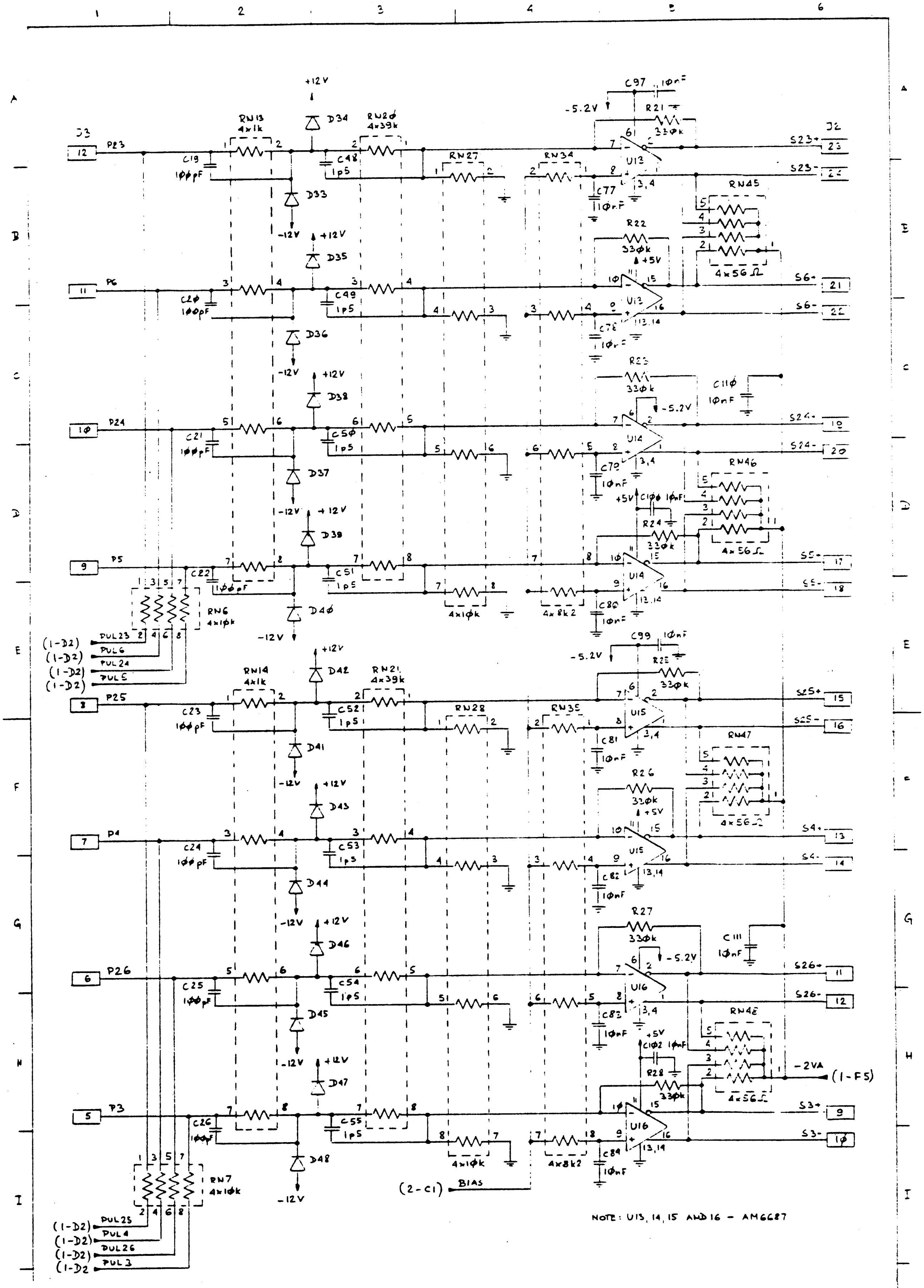
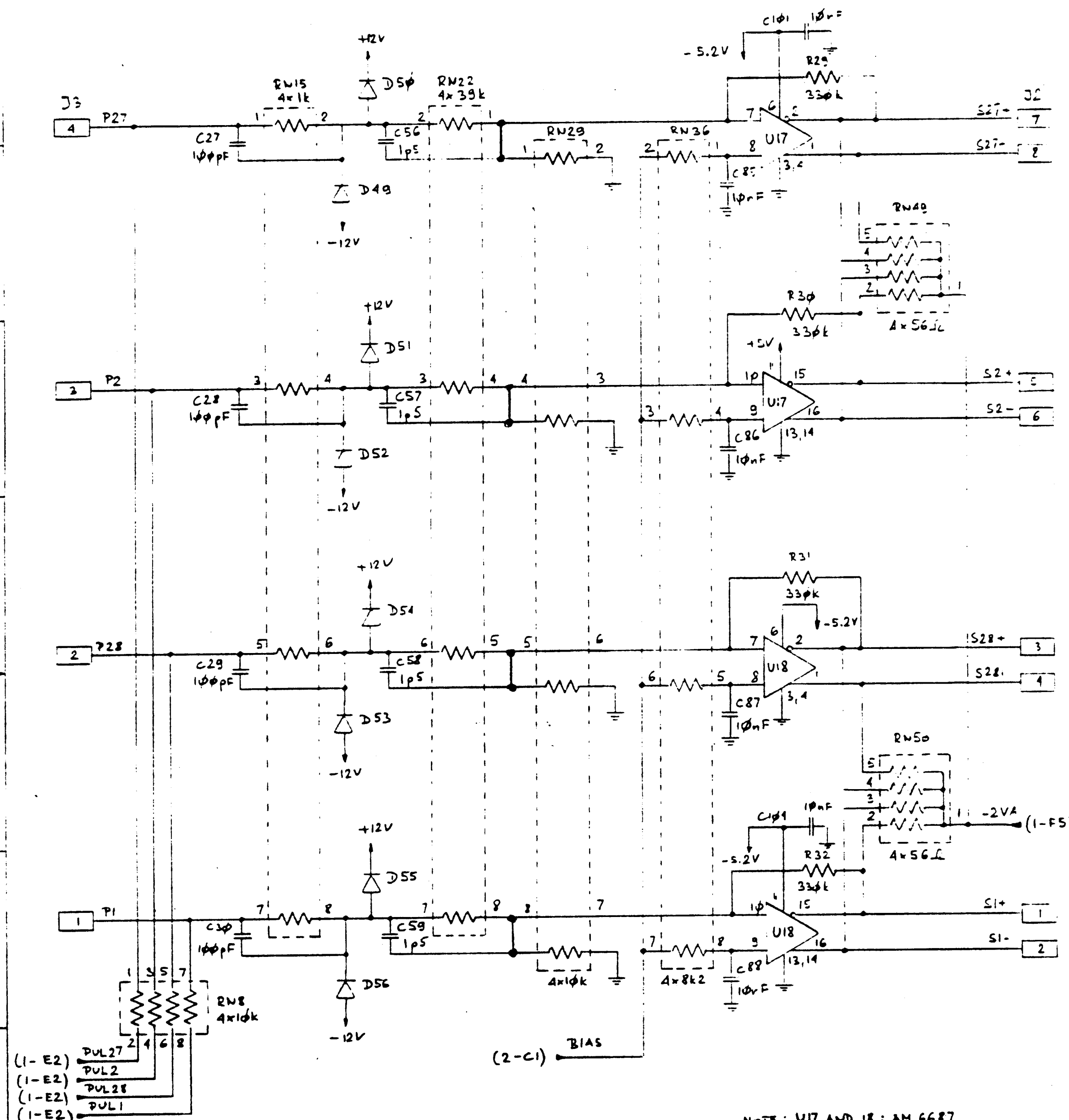
DWG No.	SM-506C
SHEET	4 OF 6



26.11.87.

	ZTEST
TITLE:	IB28
ENGINEERING NUMBER	
DWG No.	SM-506C
SHEET	5 OF 6



NOTE: U17 AND 18: AM 6687

26.11.87

ZTEST

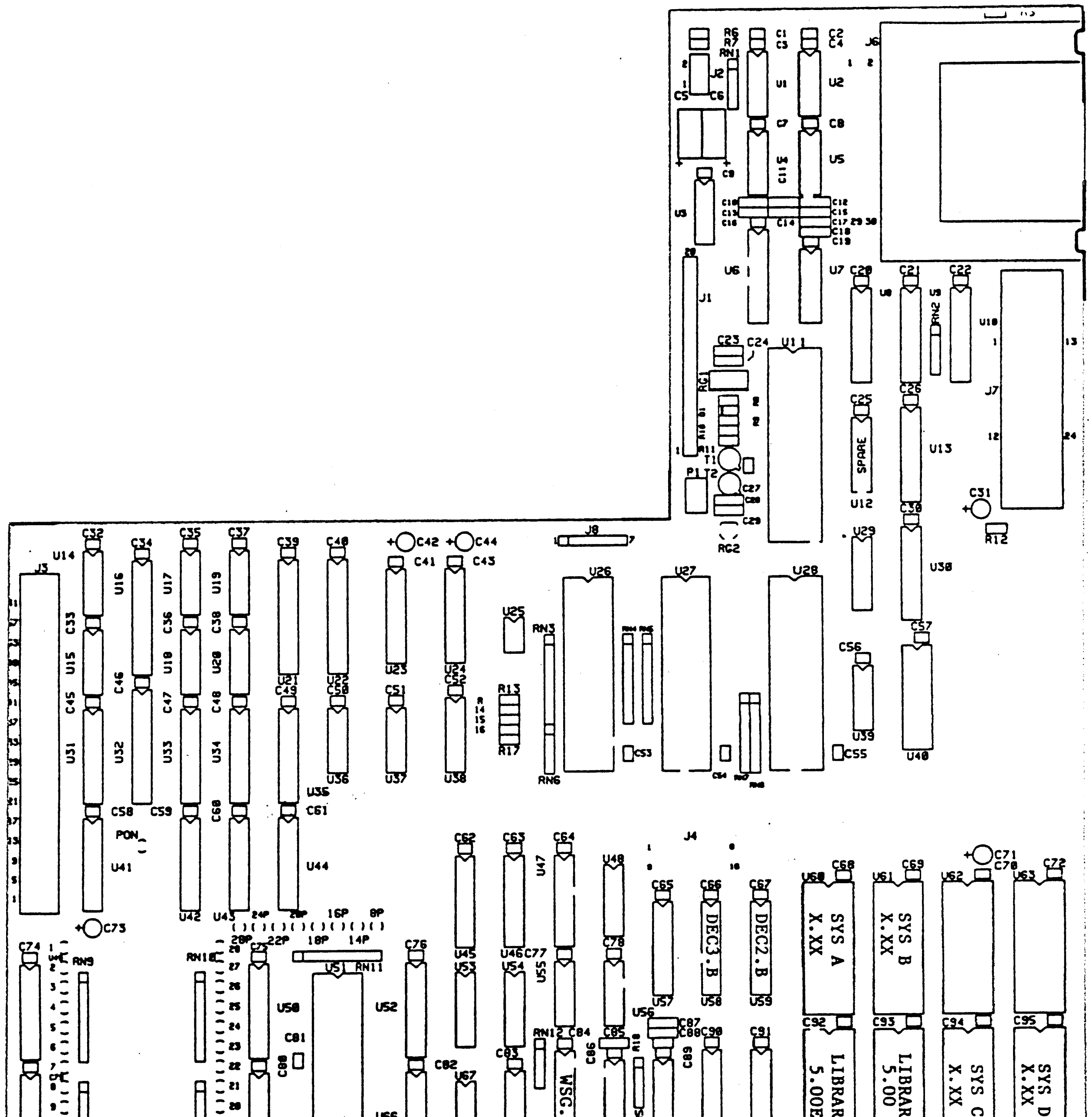
TITLE: IB2A

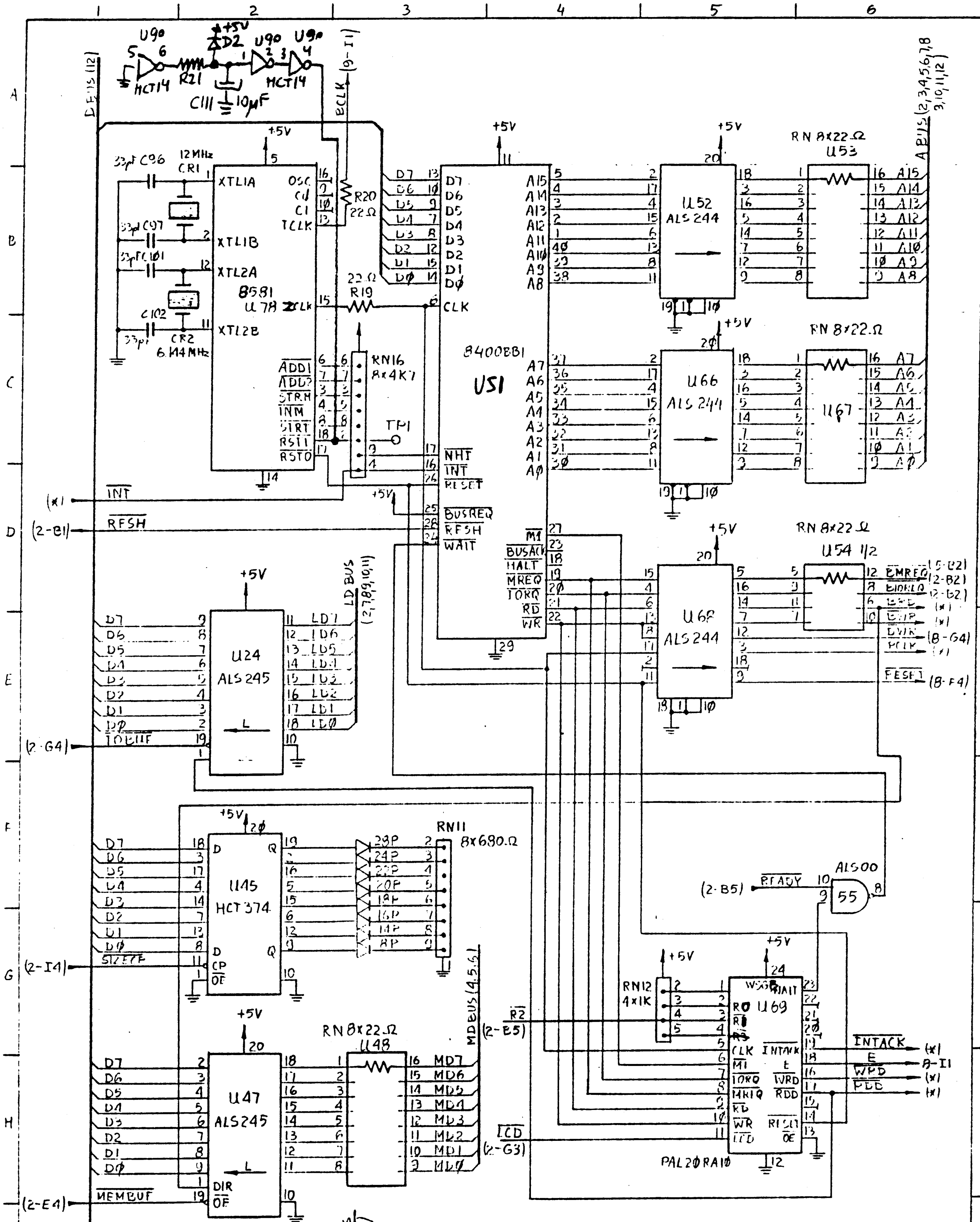
DWG NO. SM-506C

SHEET 6 OF 6

6.2 MICRO BOARD - MB rev.2 (M2)

1 Layout Page
13 Schematic Pages


SYS A X.XX
SYS B X.XX
SYS C X.XX
SYS D X.XX
LIBRARY 5.00E
LIBRARY 5.00
DEC3.B
DEC2.B
WSG.B
SPARE
300 507-2

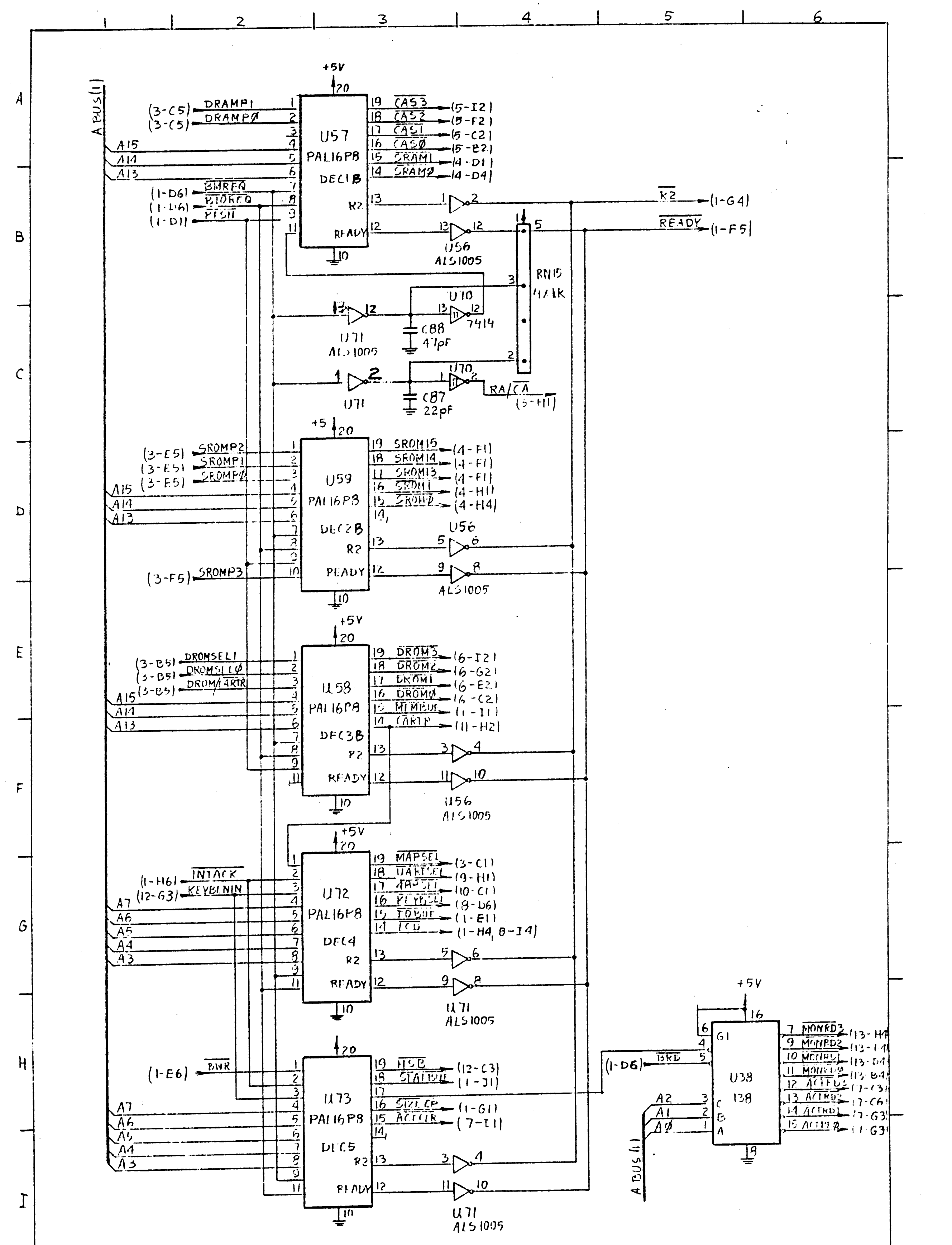


(*) multiple connections.

PCLK 3-E1, 8-E6, 9-I1, 10-F1, 12-H4
INT 3-D1, 8-D6, 9-H1, 10-E1, 12-H4
WRD 3-D1, 8-D6, 9-H1, 10-E1, 12-H4
RDD 3-D1, 8-D6, 9-H1, 10-D1, 12-H4
INTACK 2-G1, 3-E1, 8-E6, 9-H1, 10-F1, 12-H4
BWR 2-H2, 4-D1, 5-B2, 11-F2
BRD 2-H5, 4-H1, 5-B2, 6-F2, 8-H1, 11-H2

11.10.87

REV	REVISION	DATE	APPR	DWN	
					ZTEST
					TITLE: MB MICROPROCESSOR
					ENGINEERING NUMBER
					DWG No. SM-507 B · SCALE · SHEET 1 OF 13



11.10.87

ZTEST

REV	REVISION	DATE	APPR	DWN

TITLE: MB- MEMORY AND I/O DECODE

ENGINEERING NUMBER

DWG No. SM 501 B

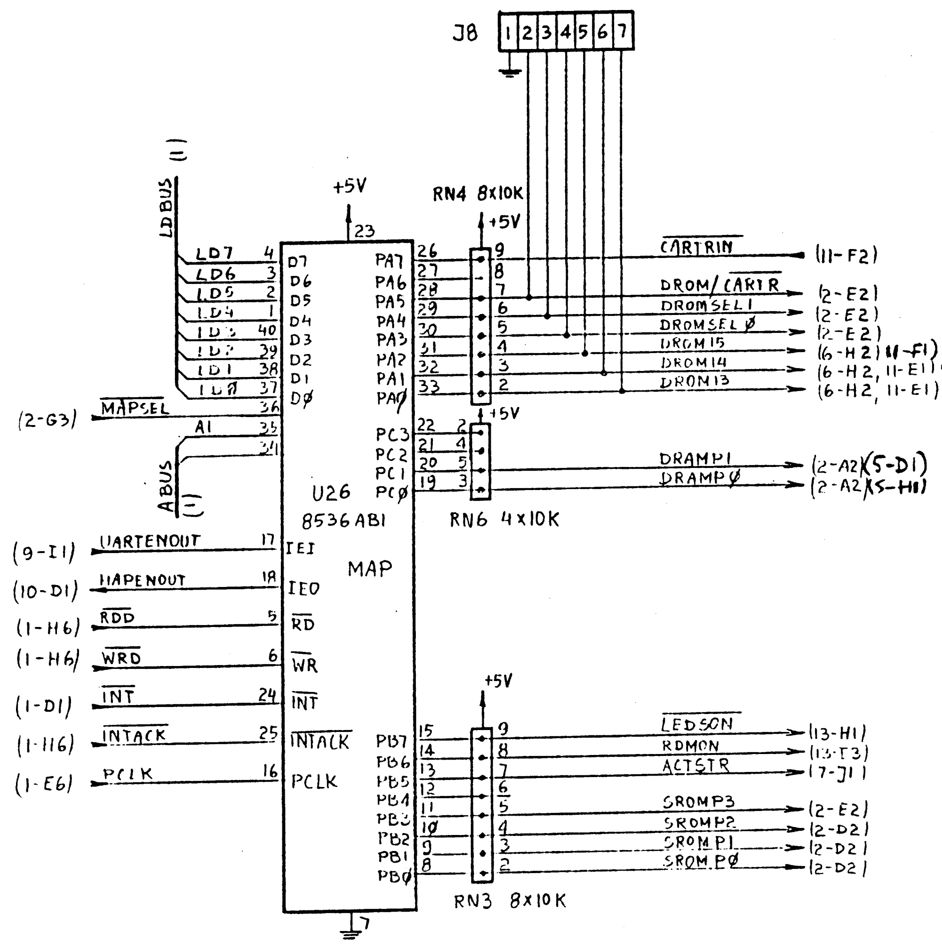
SIZE

DWN BY

CHK BY

SCALE

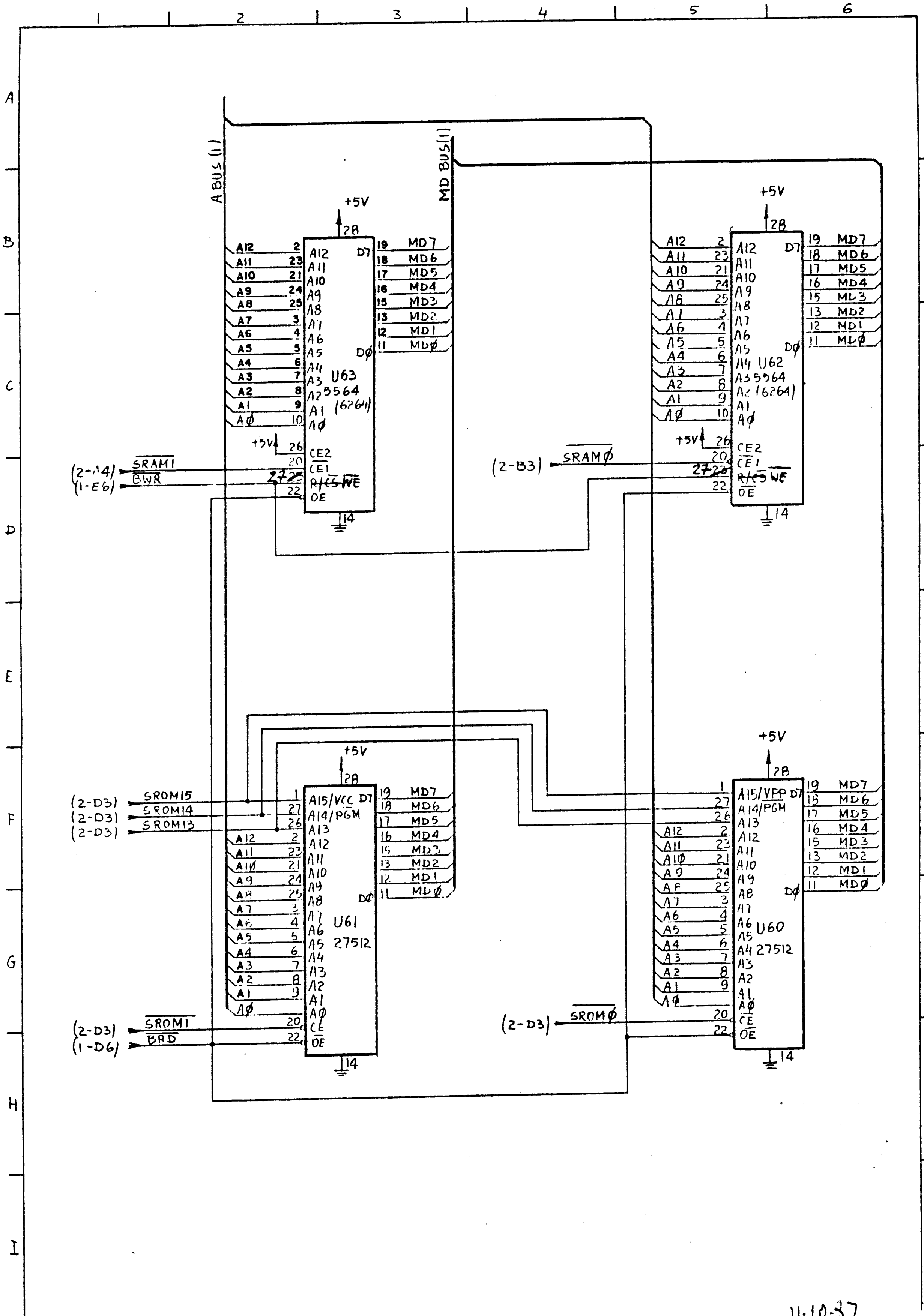
SHEET 2 OF 13



11.10.87

ZTEST	SIZE
TITLE: MB MEMORY MAPPER	DWN BY S.P.
ENGINEERING NUMBER	CHK BY
DWG No. SM-607B	SCALE 1 / SHEET 3 OF 13

REV | REVISION | DATE | APPR | DWN



REV	REVISION	DATE	APPR	DWN

ZTEST

TITLE: MB- SYSTEM ROM & RAM

ENGINEERING NUMBER

DWG No. SM-507 B

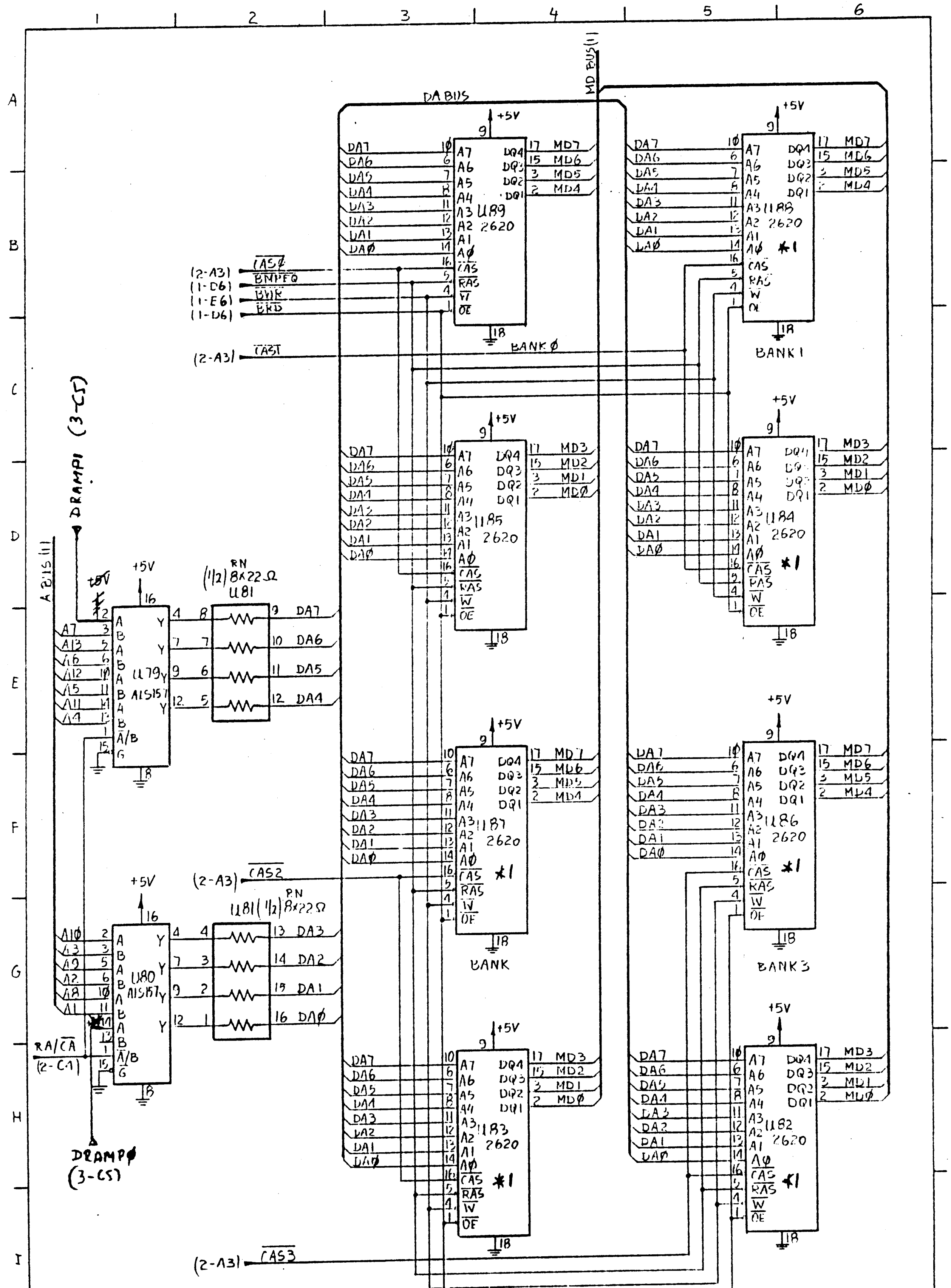
SIZE

DWN BY S.P.

CHK BY

SCALE

SHEET 4 OF 13

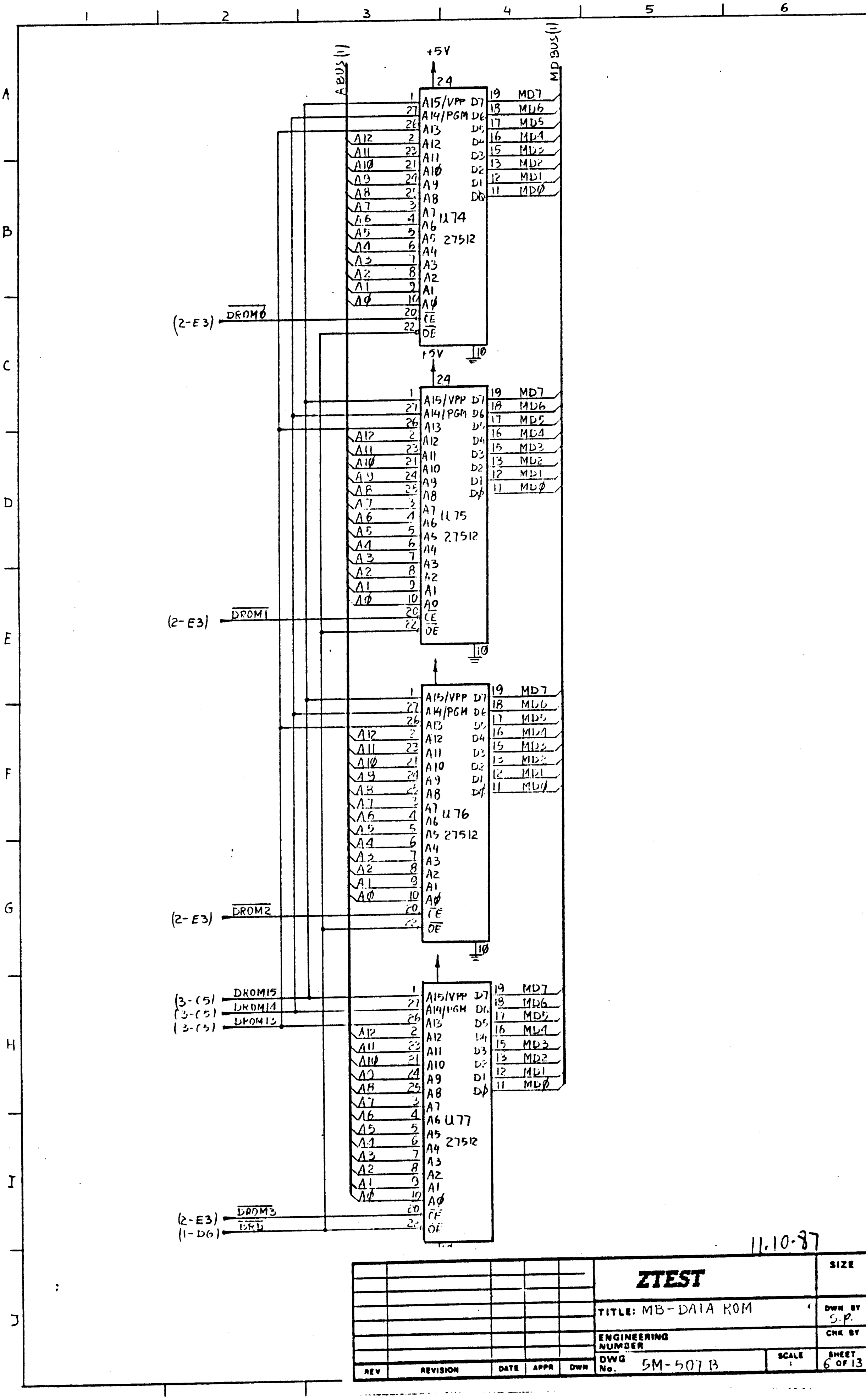


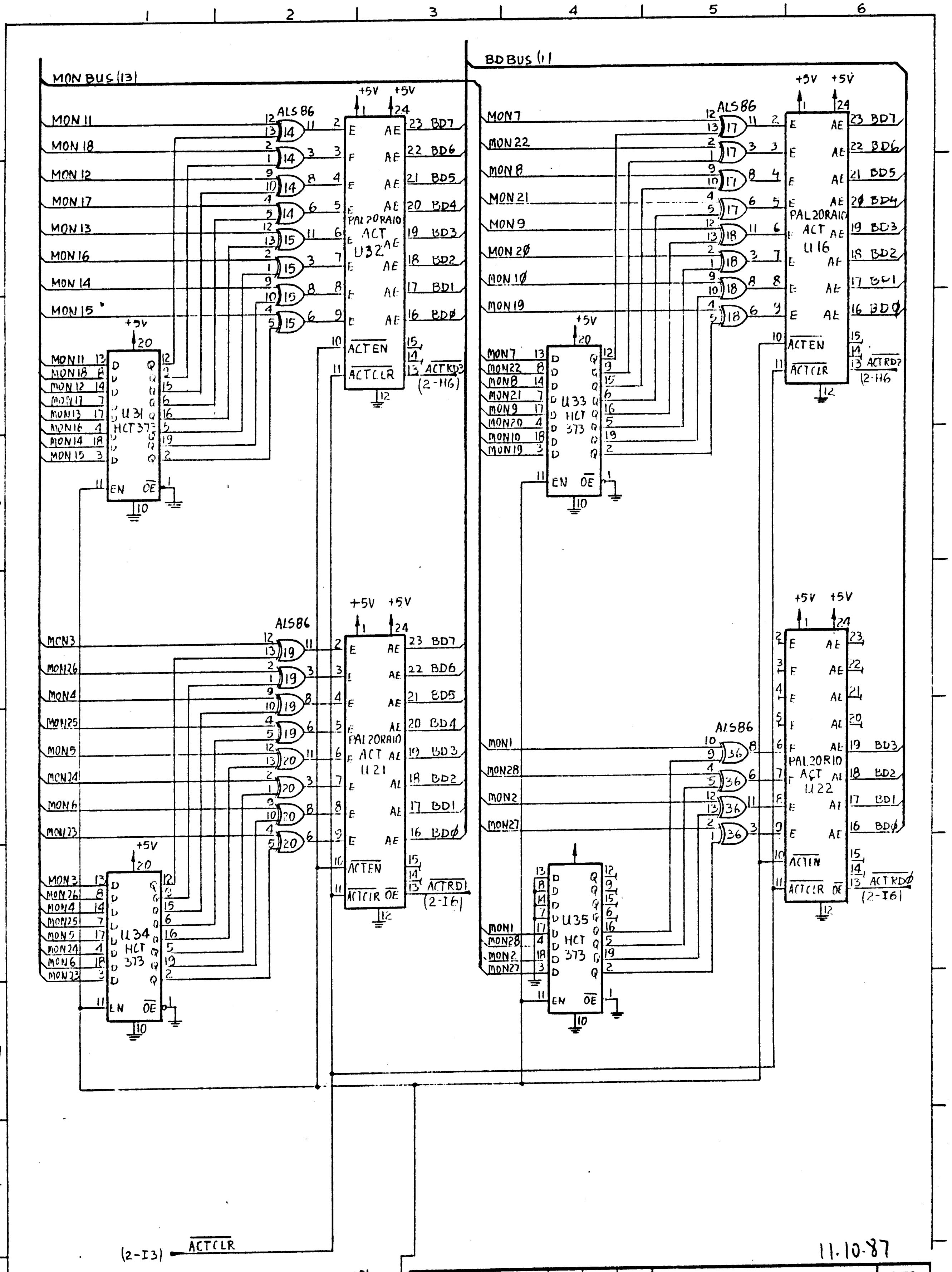
*1 - NOT INSTALLED WHEN U85 & U89 ARE 64Kx4

11 10.87

ZTEST	SIZE
TITLE: MB-DYNAMIC RAM	DWN BY S P
ENGINEERING NUMBER	CHK BY
DWG No. SM-507B	SCALE 1 / SHEET 5 OF 13

REV	REVISION	DATE	APPR	DWN


ABUS(1)
MDBUS(1)
+5V
U74 27512
U75 27512
U76 27512
U77 27512
A15/VPP
A14/PGM
CE
OE
(2-E3) DROM0
(2-E3) DROM1
(2-E3) DROM2
(2-E3) DROM3
(3-C5) DROM15
(3-C5) DROM14
(3-C5) DROM13
(1-D6) DRD
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MDØ
11.10.87
ZTEST
TITLE: MB-DATA ROM
DWN BY S.P.
CHK BY
ENGINEERING NUMBER
DWG No. 5M-507B
SCALE
SHEET 6 OF 13
SIZE
REV
REVISION
DATE
APPR
DWN



11.10.87

ZTEST					SIZE
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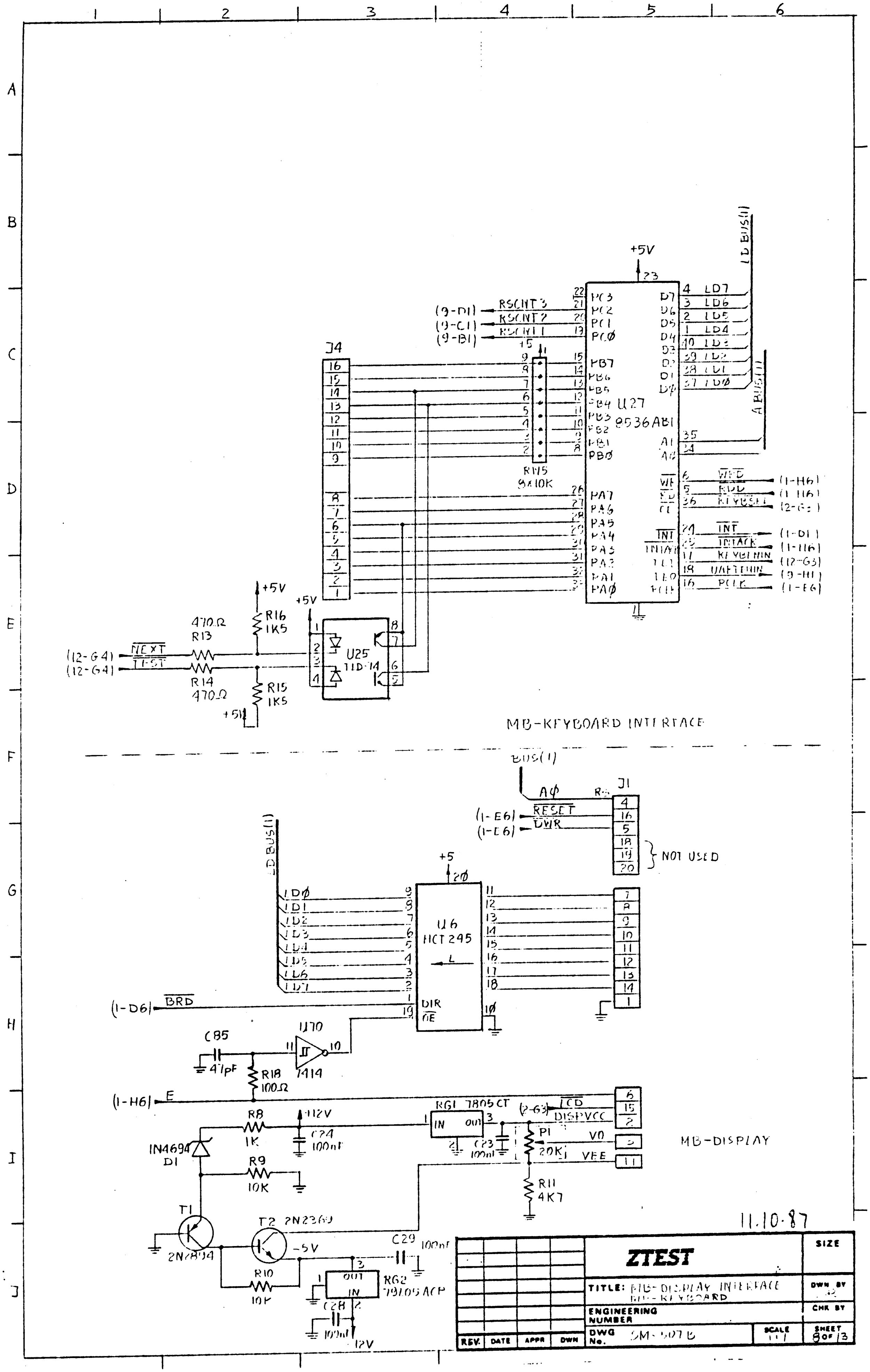
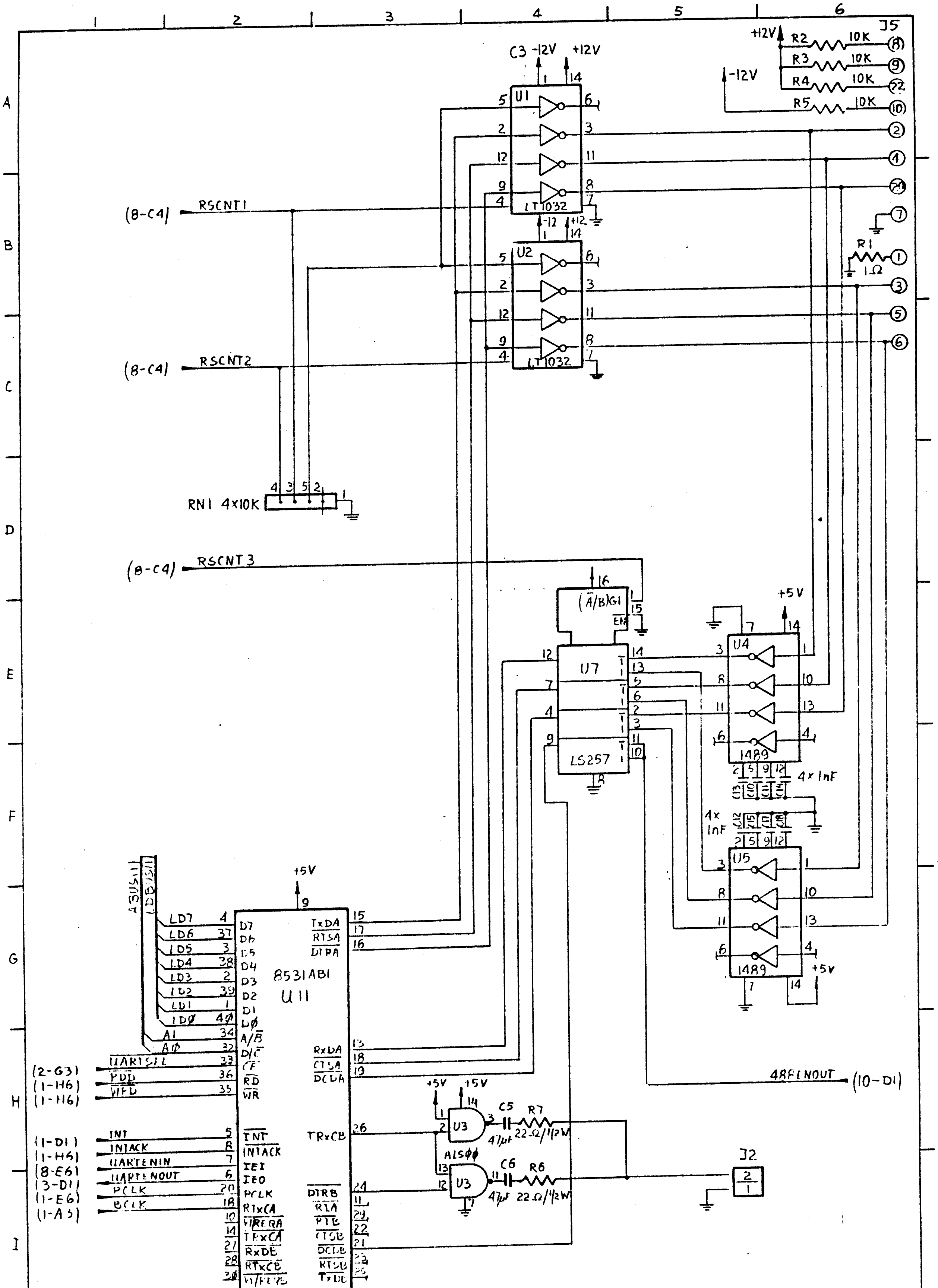
ENGINEERING NUMBER					CHK BY
REV	REVISION	DATE	APPR	DWN	DWG No. SM-507B	SCALE	SHEET 7 OF 13



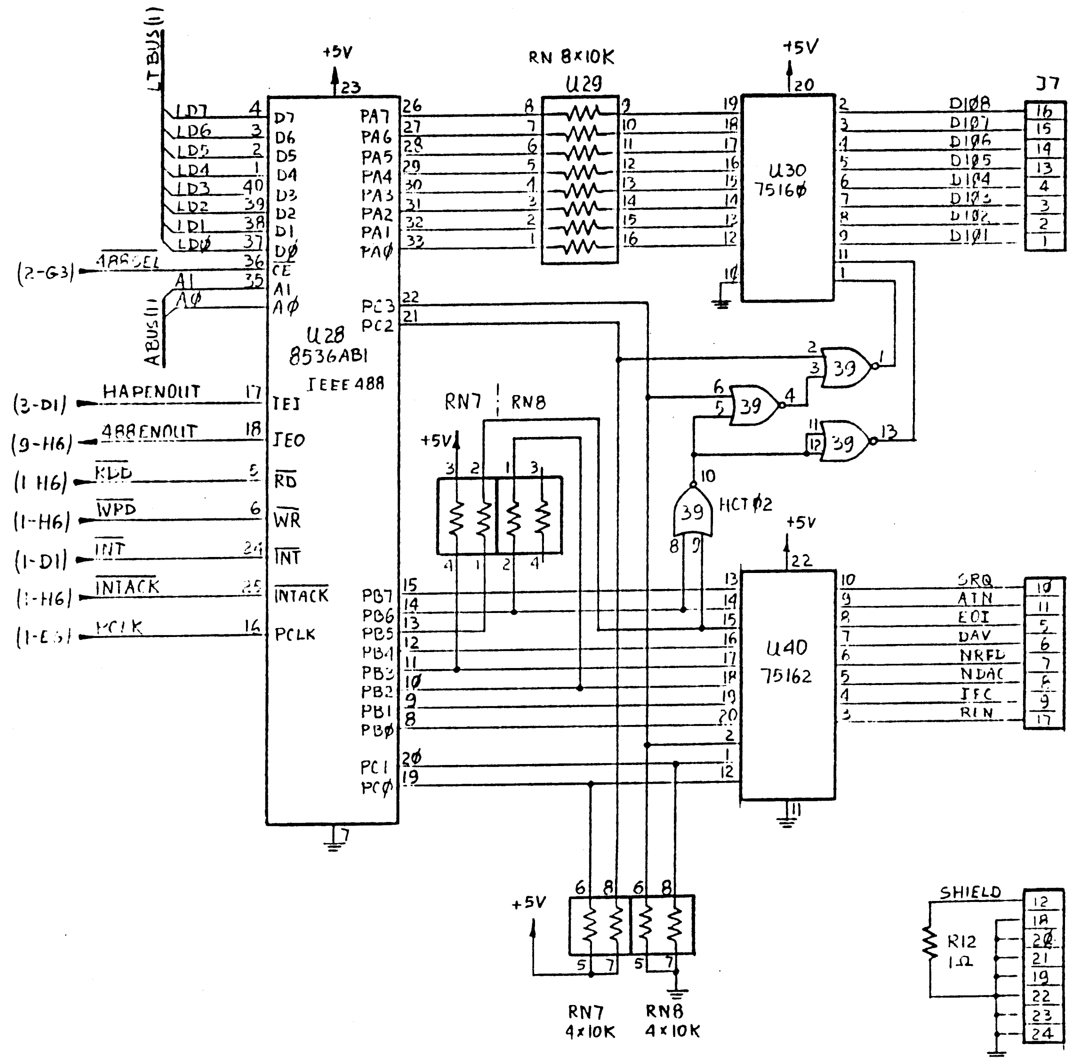
11.10.87

	ZTEST
TITLE:	MB-DISPLAY INTERFACE MB-KEYBOARD
ENGINEERING NUMBER	
DWG No.	SM-507B
SCALE	1:1
SHEET	8 OF 13



11.10.87

					ZTEST	SIZE
					TITLE: MB-RS232 INTERFACE	DWN BY S.P.
					ENGINEERING NUMBER	CHK BY
REV	REVISION	DATE	APPR	DWN	DWG No. SM-507B	SCALE	SHEET 9 OF 13



11.10.87

ZTEST

TITLE: MB- IEEE-488 INTERFACE

DWN BY S.P.

CHK BY

ENGINEERING NUMBER

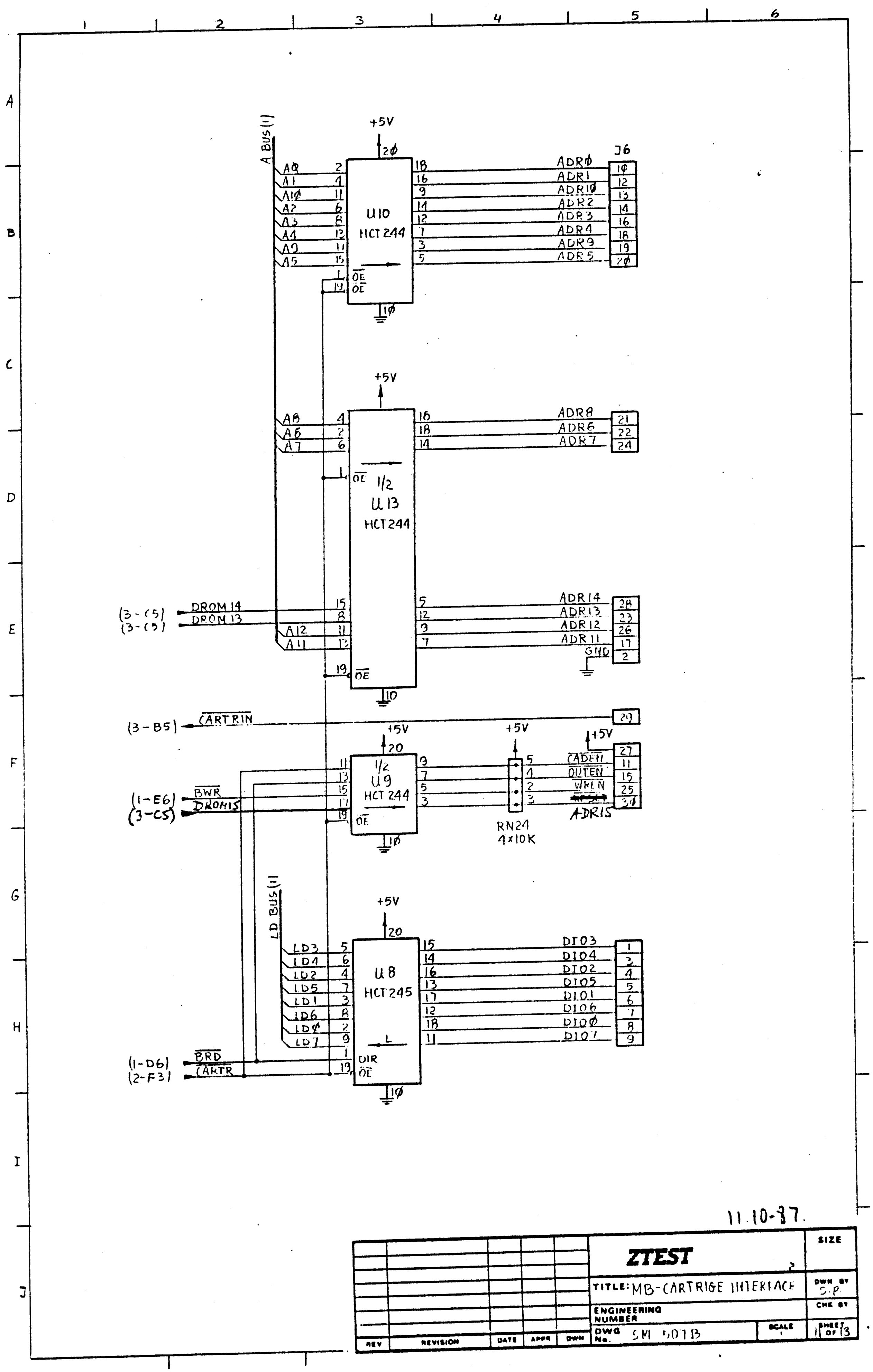
DWG No. SM-507 B

SCALE 1

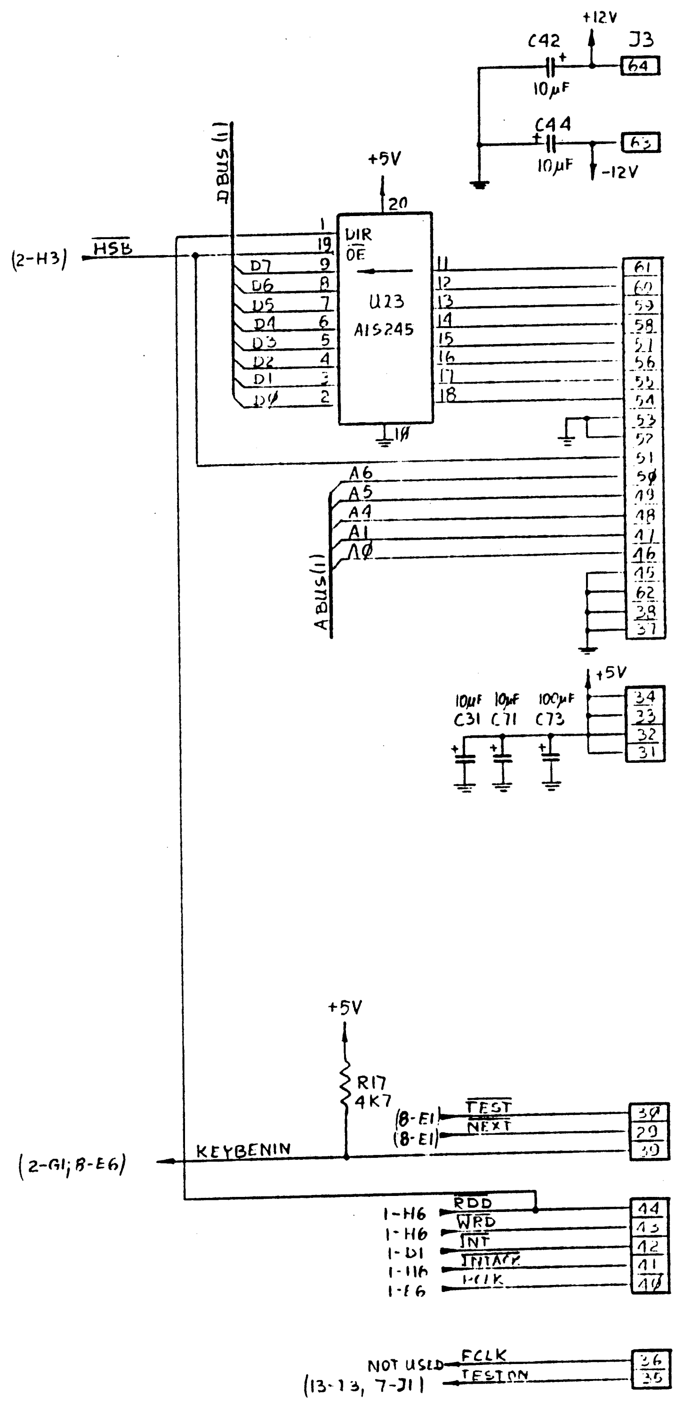
SHEET 10 OF 13

SIZE

REV | REVISION | DATE | APPR | DWN

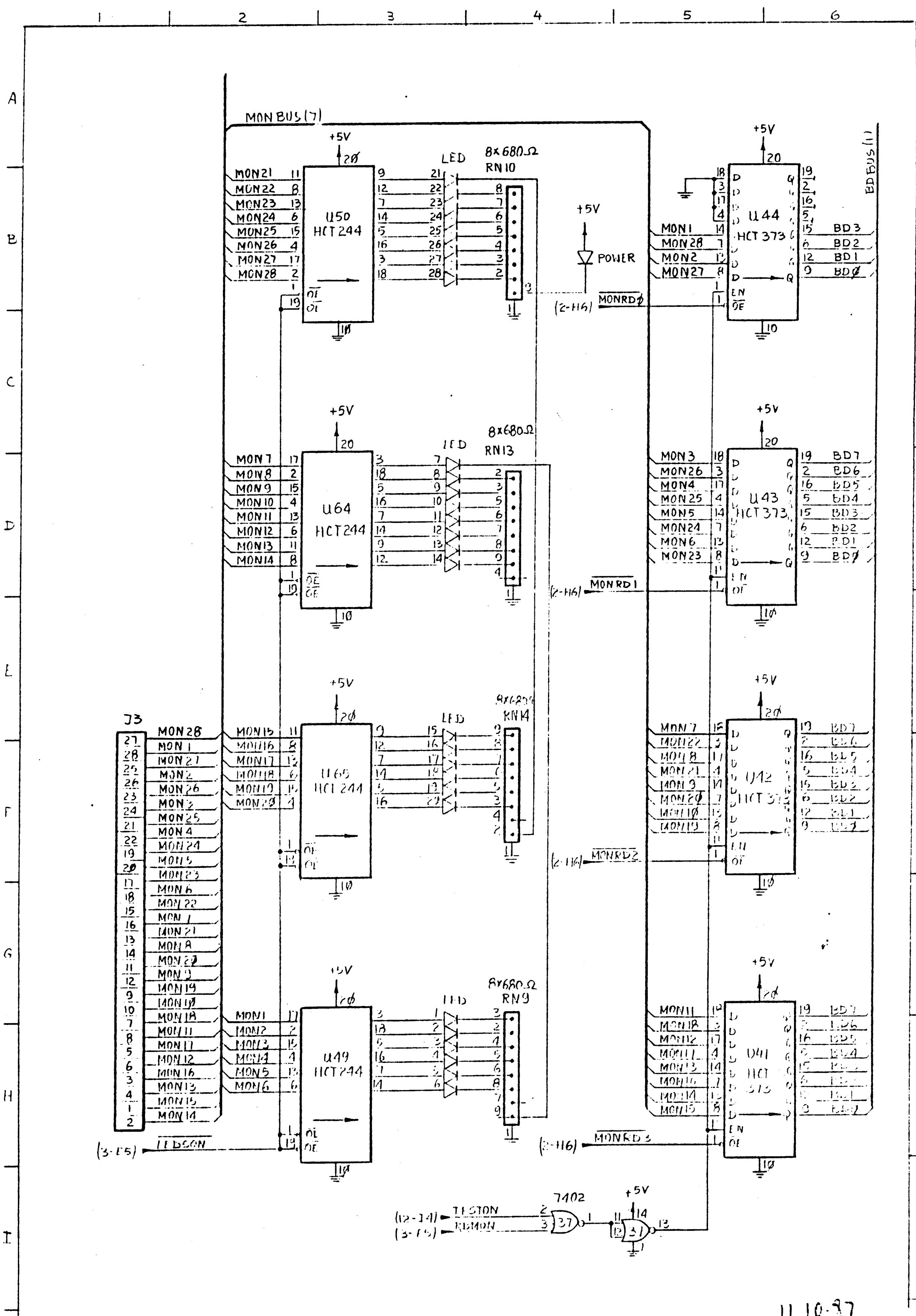


+5V
A BUS(1)
U10
HCT244
J6
ADR0
ADR1
ADR10
ADR2
ADR3
ADR4
ADR9
ADR5
1/2
U13
HCT244
ADR8
ADR6
ADR7
ADR14
ADR13
ADR12
ADR11
GND
DROM14
DROM13
(3-C5)
(3-C5)
CARTRIN
(3-B5)
1/2
U9
HCT 244
BWR
DROM15
(1-E6)
(3-C5)
RN24
4x10K
CADEN
OUTEN
WREN
ADR15
LD BUS(1)
U8
HCT245
DIO3
DIO4
DIO2
DIO5
DIO1
DIO6
DIO0
DIO7
BRD
CARTR
(1-D6)
(2-F3)
DIR
OE
11.10-87.
ZTEST
TITLE: MB-CARTRIGE INTERFACE
DWN BY S.P.
ENGINEERING NUMBER
DWG No. SM 5013
SHEET 11 OF 13



11.10.87

				ZTEST	SIZE
				TITLE: MB-HS BOARD INTERFACE	DWN BY S.P.
				ENGINEERING NUMBER	CHK BY
REV	REVISION	DATE	APPR	DWN	DWG No. SM-501B	SCALE 1	SHEET 12 OF 13



ZTEST

TITLE: MB-SIGNAL MONITOR

ENGINEERING NUMBER

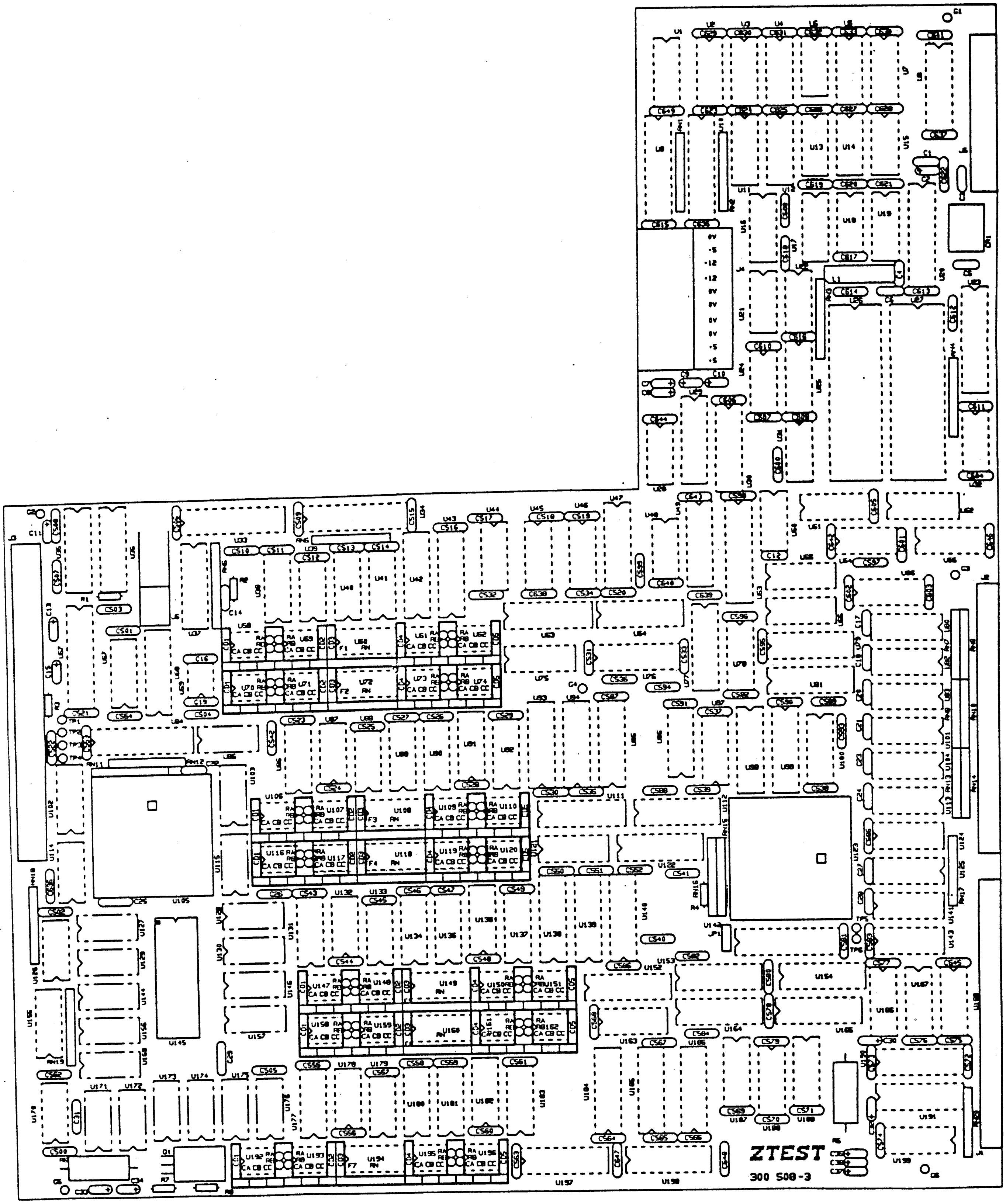
DWG No. SM-507 B

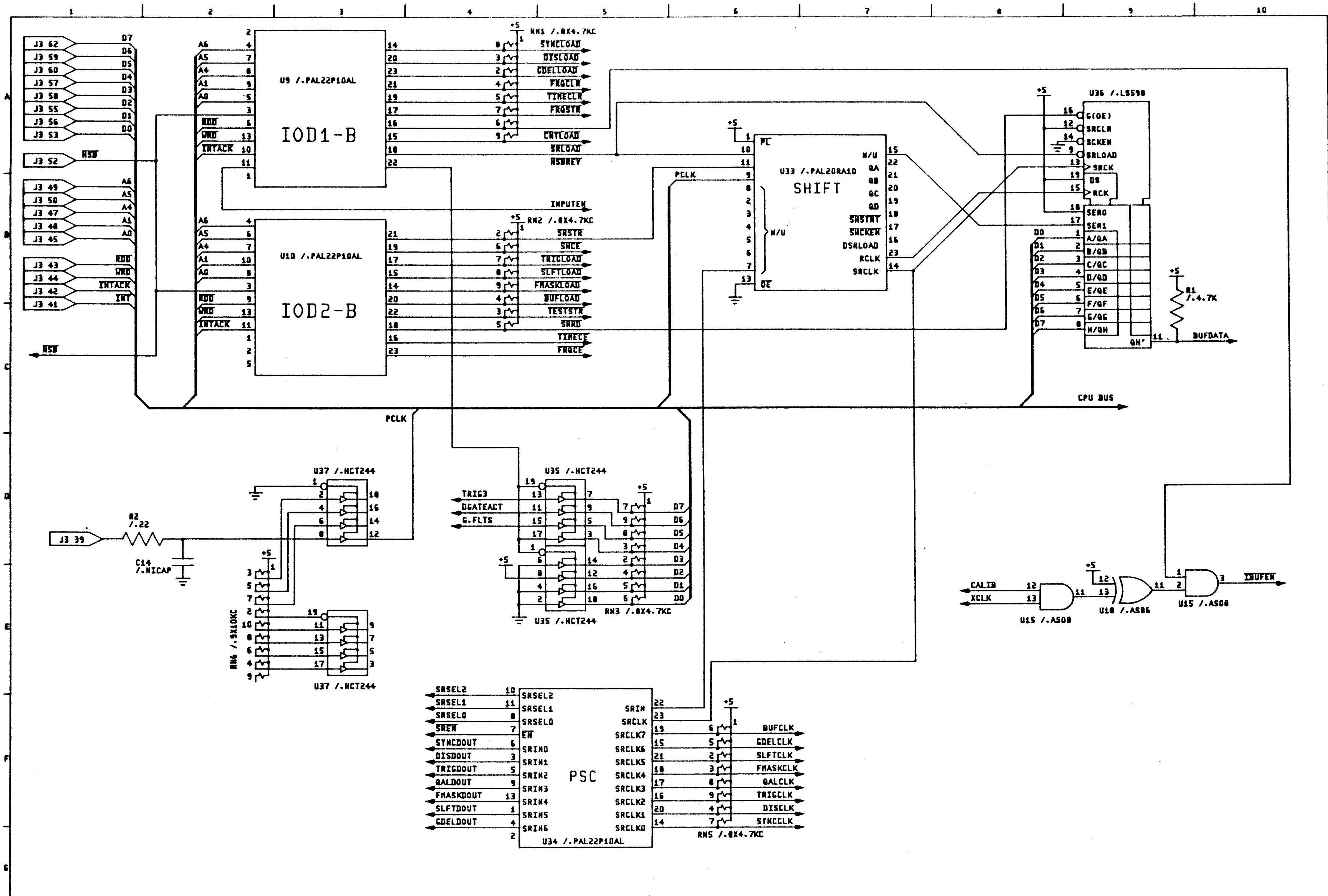
SIZE · DWN BY · CHK BY · SCALE · SHEET 13 OF 13

REV · REVISION · DATE · APPR · DWN

6.3 HIGH SPEED BOARD - HS rev.2/3 (H3)

1 Layout Page
12 Schematic Pages


ZTEST
300 508-3



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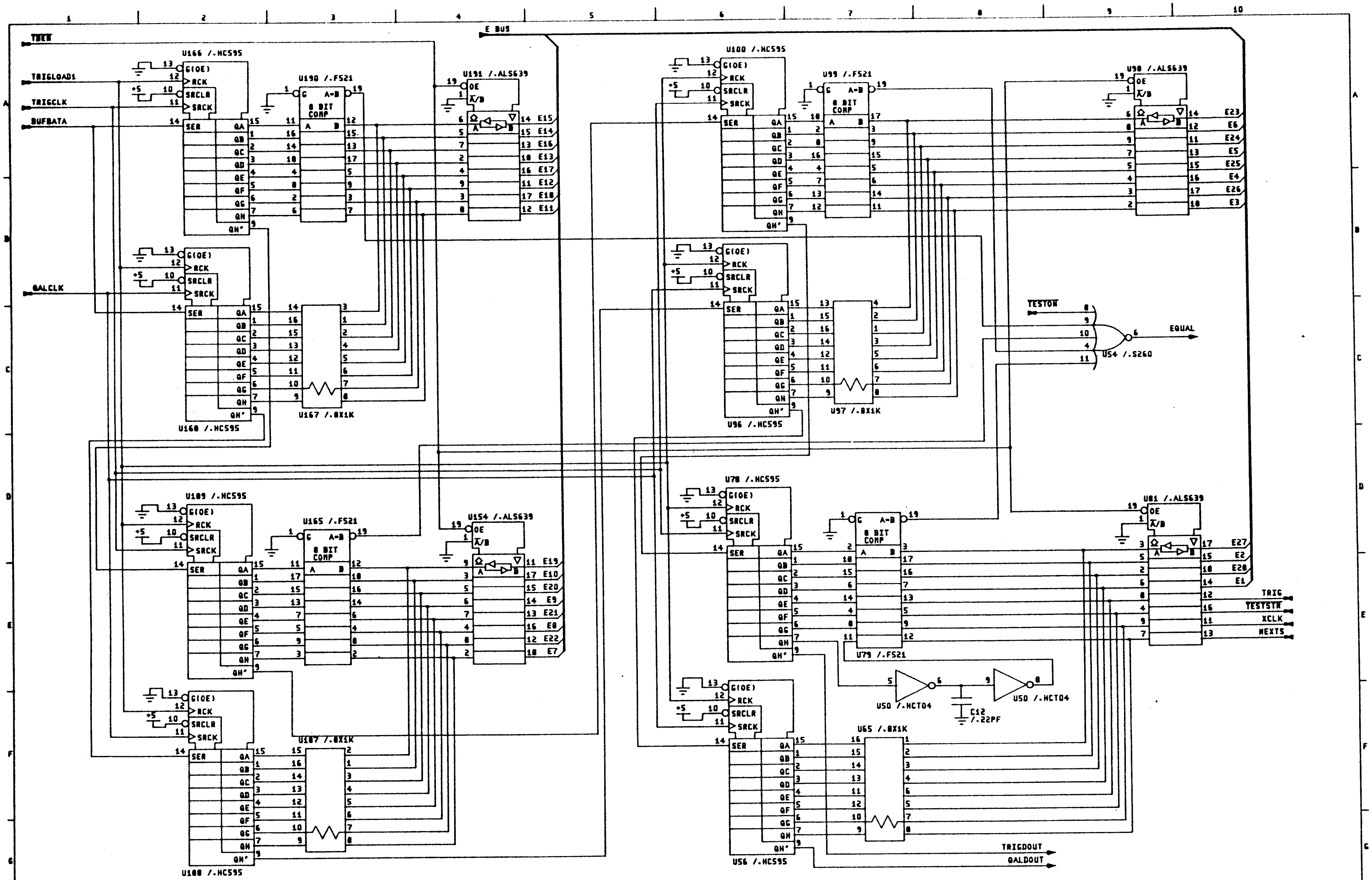
ZTEST

TITLE:	CPU INTERFACE			PROJ:	TM3000	D/M/Y:	18/9/89
BOARD:	HIGH SPEED	FILE:	CPU.CSD	DWG.	SM508	REV. 3	PARENT SHEET #	SHEET 1 OF 12



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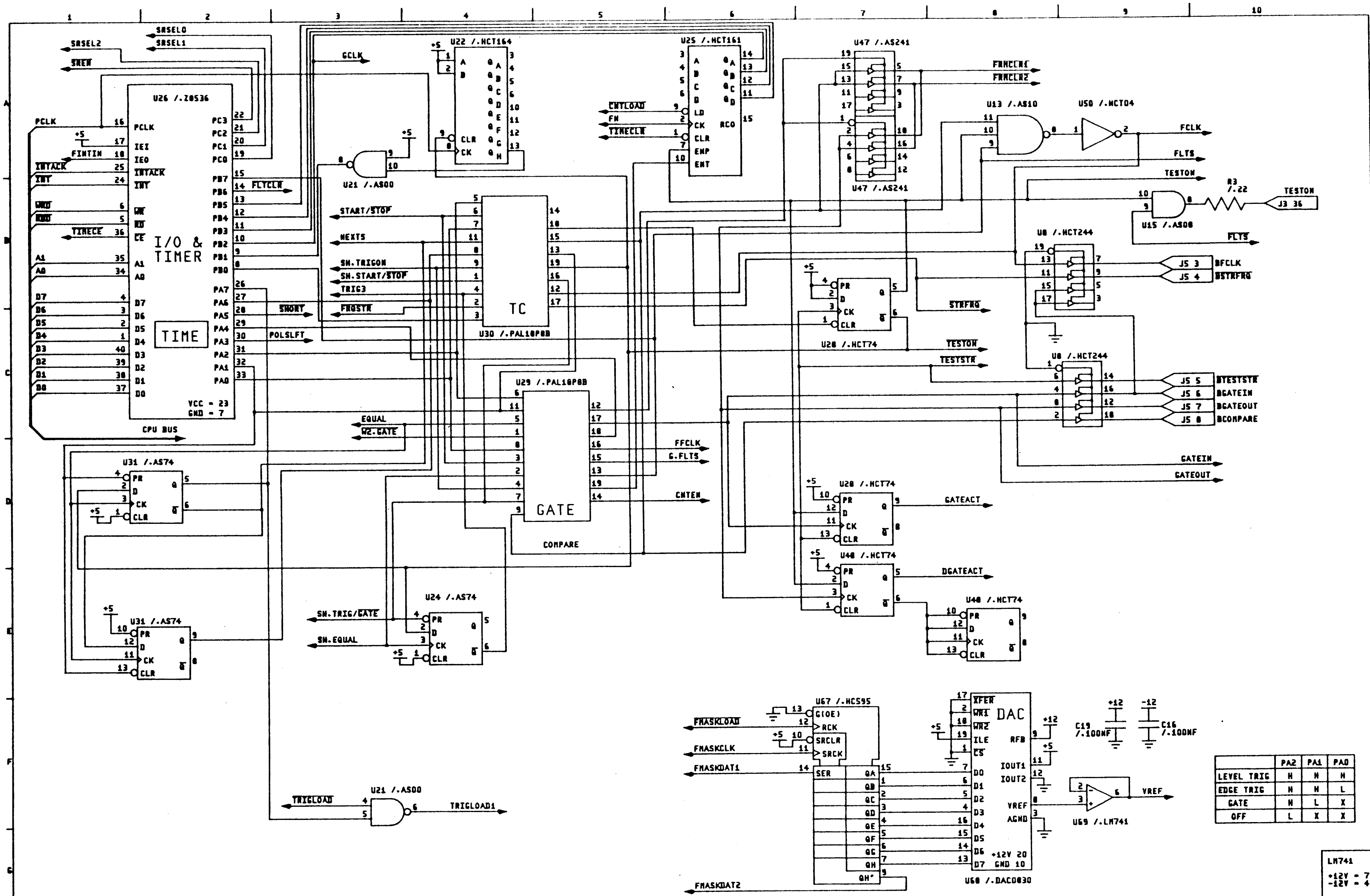
ZTEST

TITLE:	TRIGGER & GATE		PROJ:	TM3000		D/M/Y:	12/12/89
BOARD:	HIGH SPEED	FILE: GATE.CSD	DWG.	SM508	REV. 3	PARENT SHEET #	SHEET 2 OF 12



	PA2	PA1	PA0
LEVEL TRIG	H	H	H
EDGE TRIG	H	H	L
GATE	H	L	X
OFF	L	X	X

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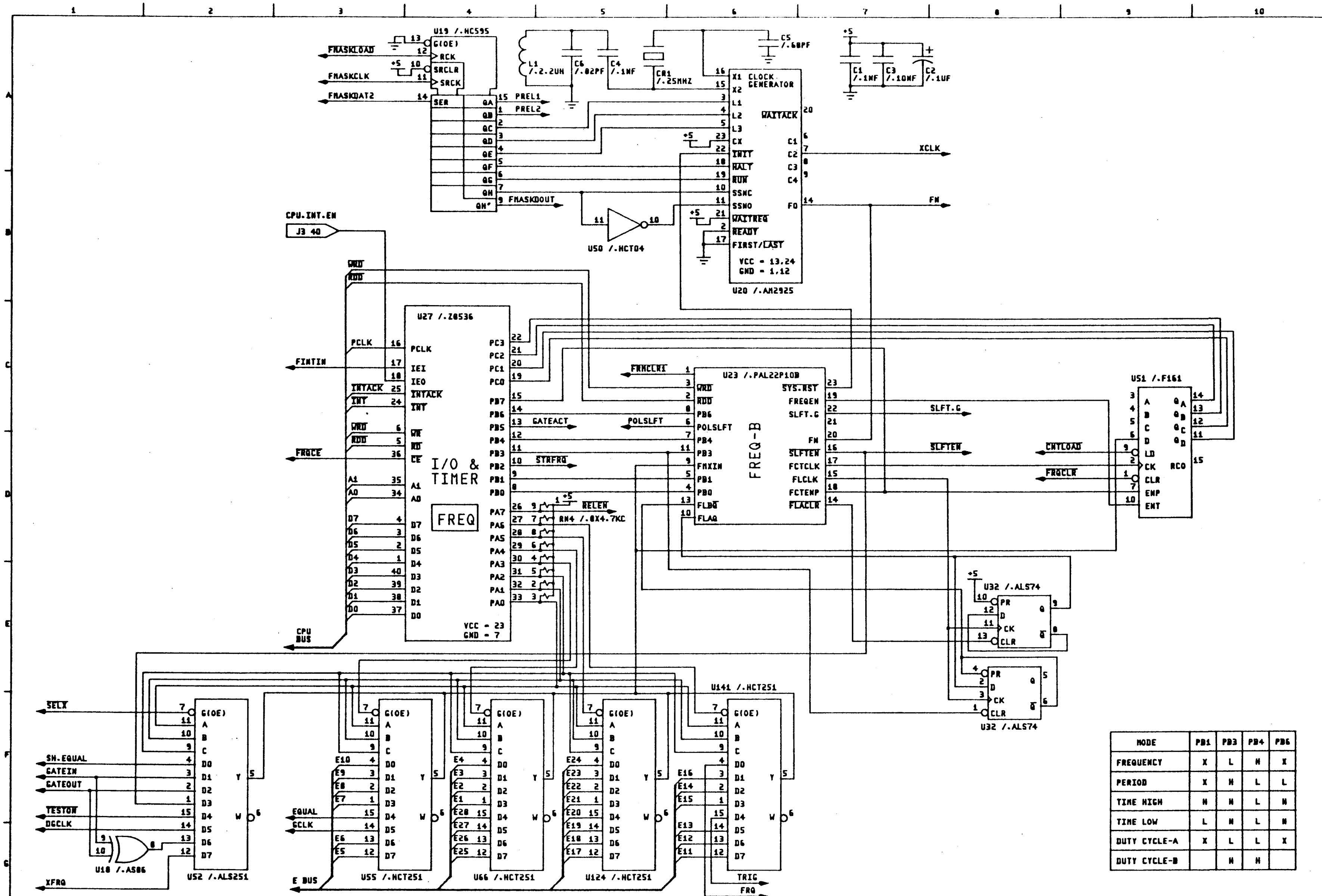
ZTEST

TITLE:	TEST CYCLE			PROJ:	TM3000			D/M/Y:	12/12/89
BOARD:	HIGH SPEED	FILE:	TCYCLE.CSD	DWG.	SM508	REV.	3	PARENT SHEET #	SHEET 3 OF 12



MODE	PB1	PB3	PB4	PB6
FREQUENCY	X	L	H	X
PERIOD	X	H	L	L
TIME HIGH	H	H	L	H
TIME LOW	L	H	L	H
DUTY CYCLE-A	X	L	L	X
DUTY CYCLE-B		H	H	

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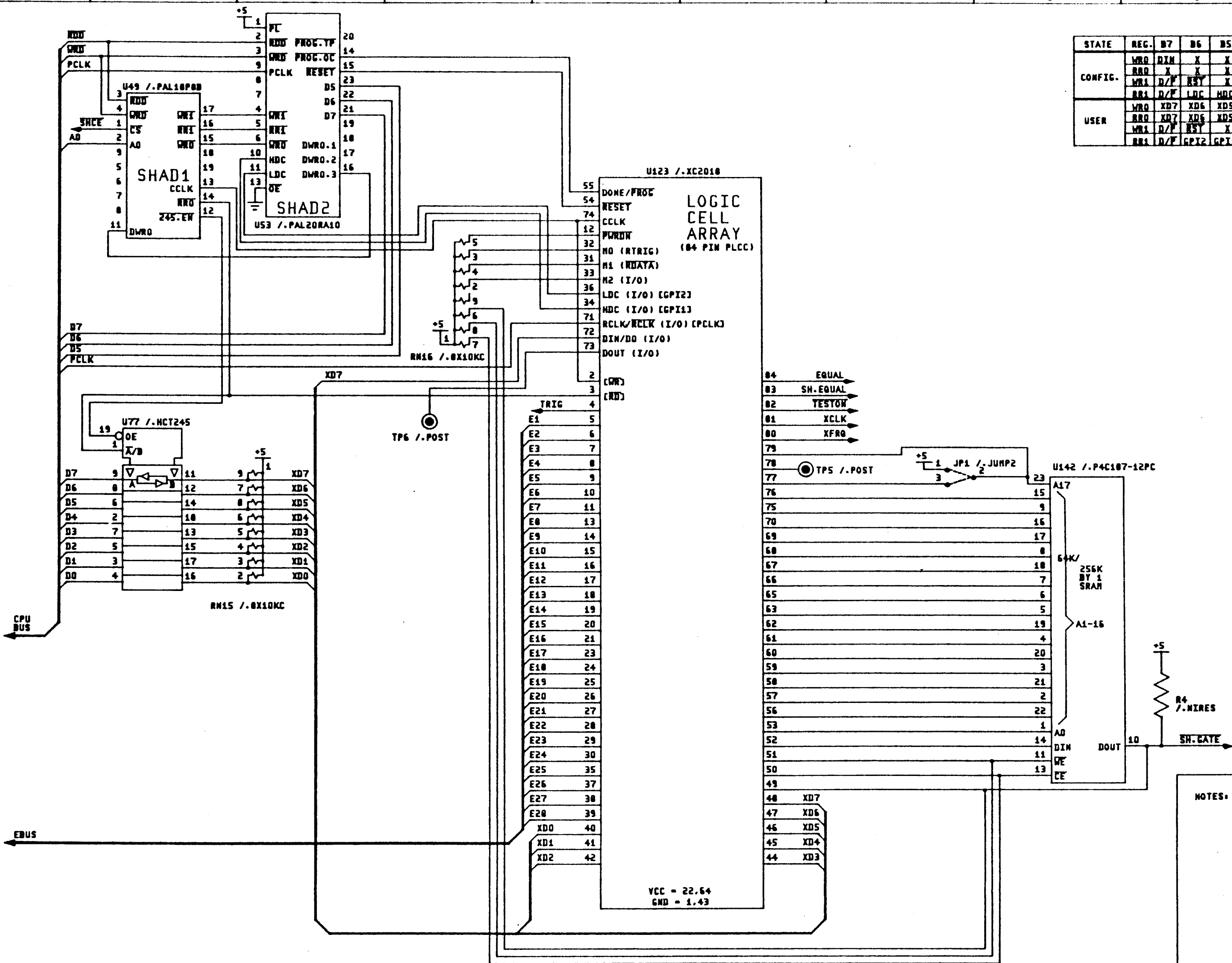
ZTEST

TITLE: FREQUENCY			PROJ: TM3000		D/M/Y: 12/12/89
BOARD: HIGH SPEED	FILE: FREQ.CSD	DWG. SM508	REV. 3	PARENT SHEET #	SHEET 4 OF 12



STATE	REG.	B7	B6	B5	B4	B3	B2	B1	B0
CONFIG.	WR0	DIN	X	X	X	X	X	X	X
	RR0	X	X	X	X	X	X	X	X
	WR1	D/F	RST	X	X	X	X	X	X
	RR1	D/F	LDC	HDC	X	X	X	X	X
USER	WR0	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
	RR0	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
	WR1	D/F	RST	X	X	X	X	X	X
	RR1	D/F	GPI2	GPI1	X	X	X	X	X

NOTES:
1. THE RESET OUTPUT OF THE PAL IS ACTIVE FOLLOWING POWER-UP UNTIL DE-ASSERTED BY WRITING WR1 BIT1 WITH A HIGH.
2. THE PROG LINE IS INACTIVE FOLLOWING POWER UP.
3. CONFIG MUST BE DELAYED BY AT LEAST 40MS AFTER POWER-UP
4. CCLK LOW TIME = 250 NS MIN = 5 US MAX
5. U49, U53, U77, U123, AND U142 ARE ONLY INSTALLED IN SYSTEMS WITH THE E-PACKAGE OPTION

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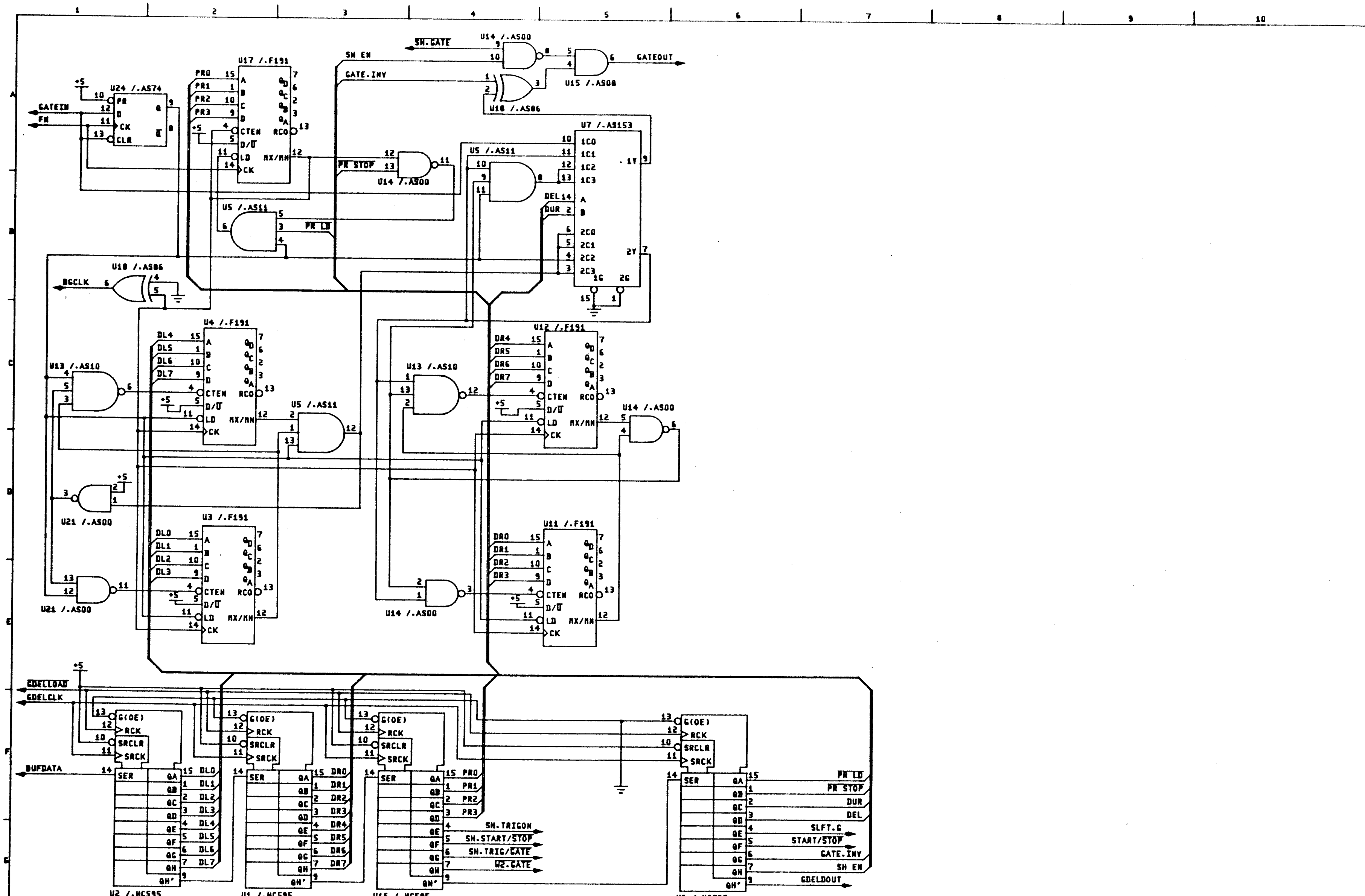
ZTEST

TITLE: SHADOW RAM | PROJ: TM3000 | D/M/Y: 12/12/89

BOARD: HIGH SPEED | FILE: SHRAM.CSD | DWG. SM508 | REV. 3 | PARENT SHEET # | SHEET 6 OF 12



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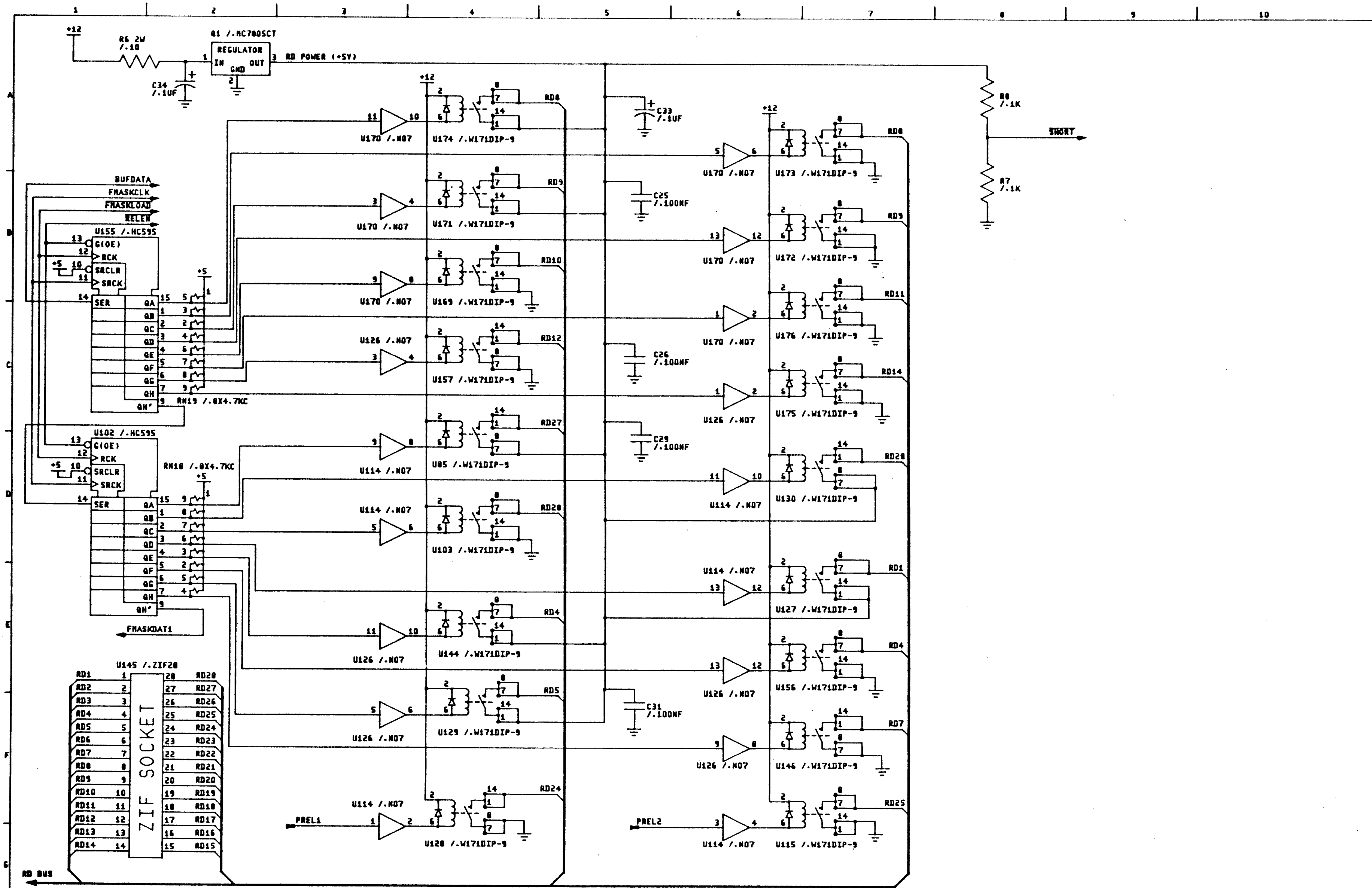
ZTEST

TITLE:	DELAYED GATE			PROJ:	TM3000	D/M/Y:	12/12/89
BOARD:	HIGH SPEED	FILE:	DGATE.CSD	DWG.	SM508	REV. 3	PARENT SHEET #	SHEET 5 OF 12



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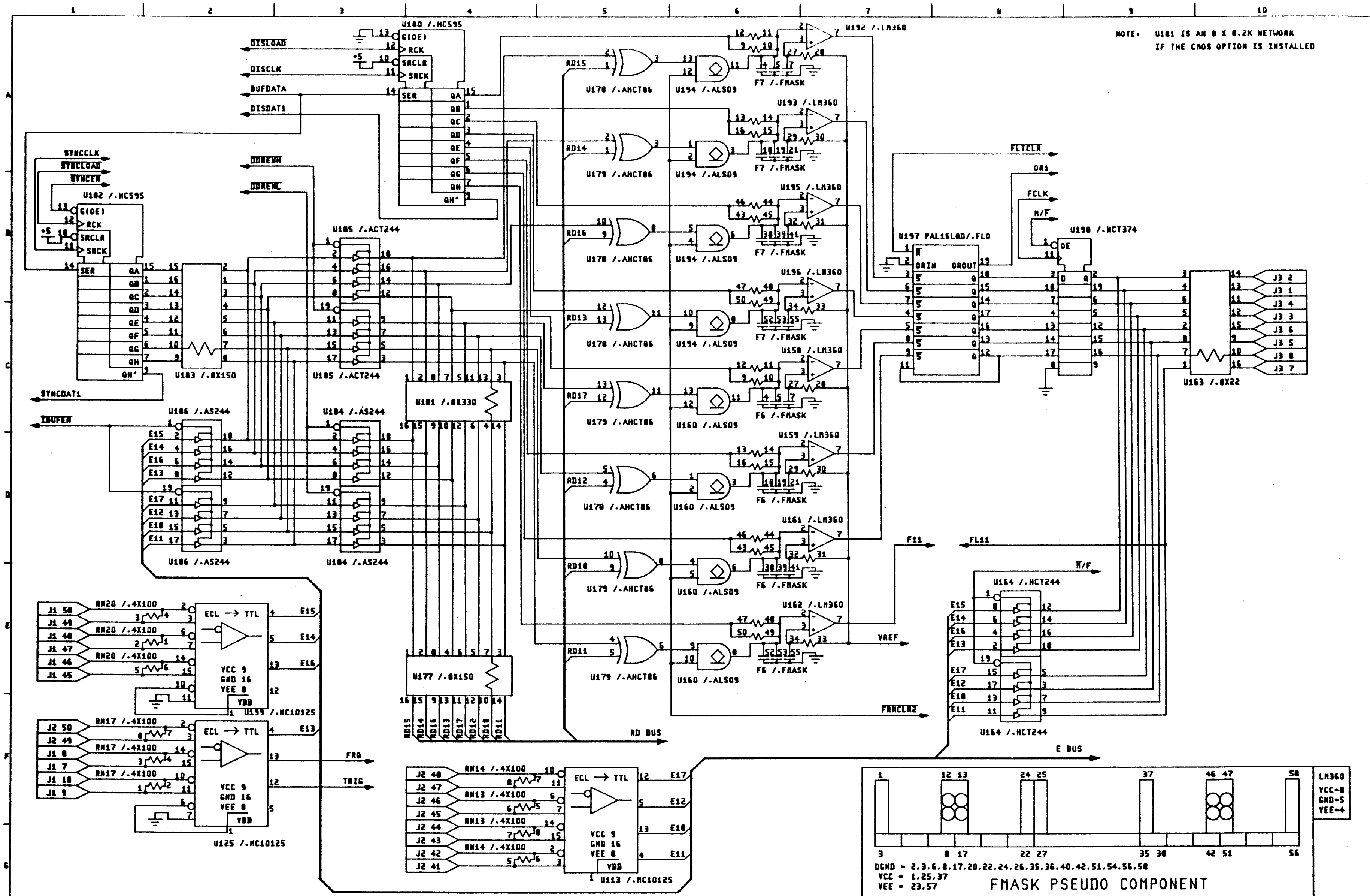
ZTEST

TITLE: RD RELAYS		PROJ: TM3000		D/M/Y: 12/12/89	
BOARD: HIGH SPEED	FILE: RELAYS.CSD	DWG. SM508	REV. 3	PARENT SHEET #	SHEET 7 OF 12



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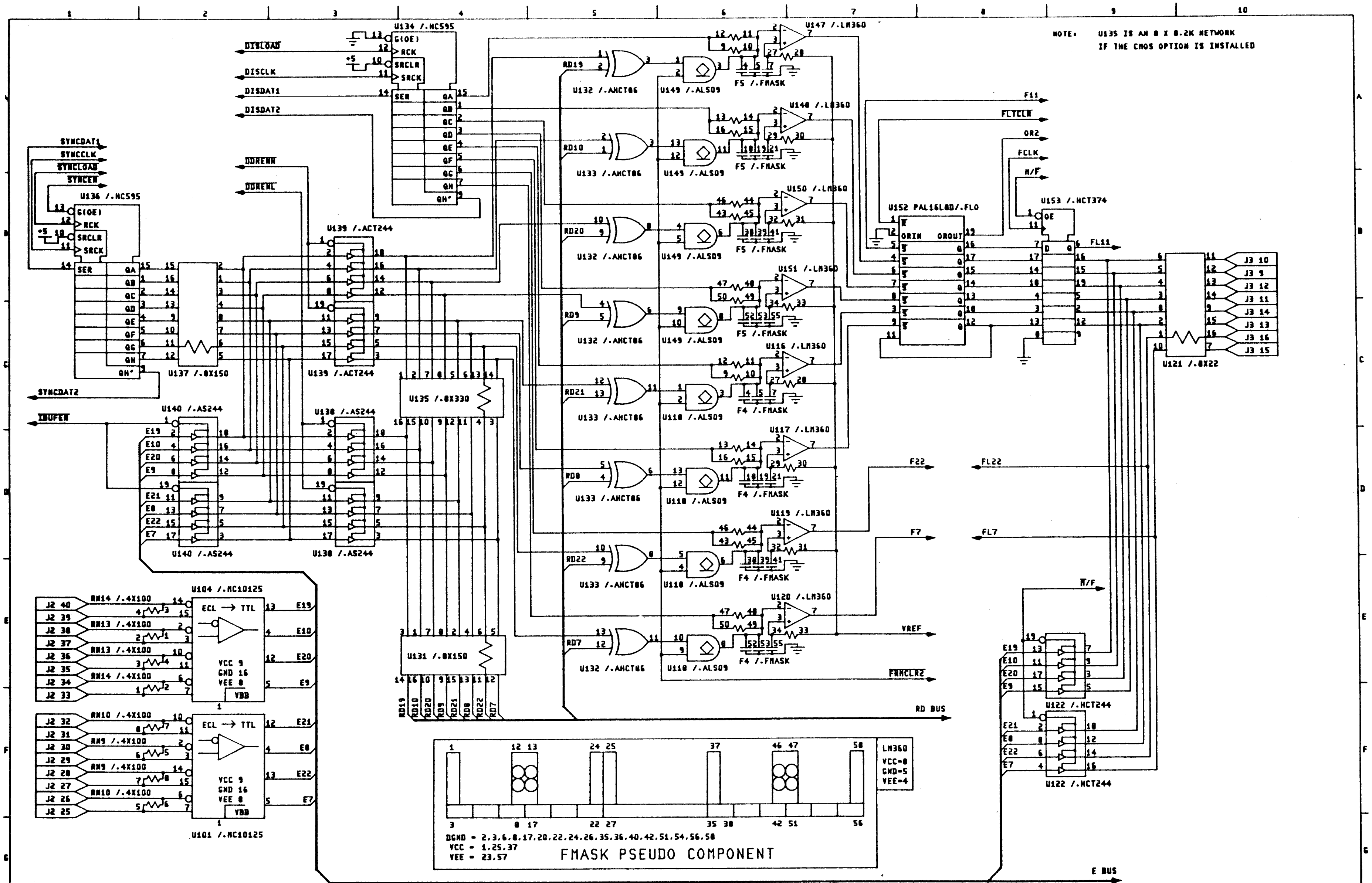
ZTEST

TITLE:	FLOW 1		PINS 11-18	PROJ:	TM3000		D/M/Y:	12/12/89
BOARD:	HIGH SPEED	FILE:	FLOW1.CSD	DWG.	SM508	REV. 3	PARENT SHEET #	SHEET 8 OF 12



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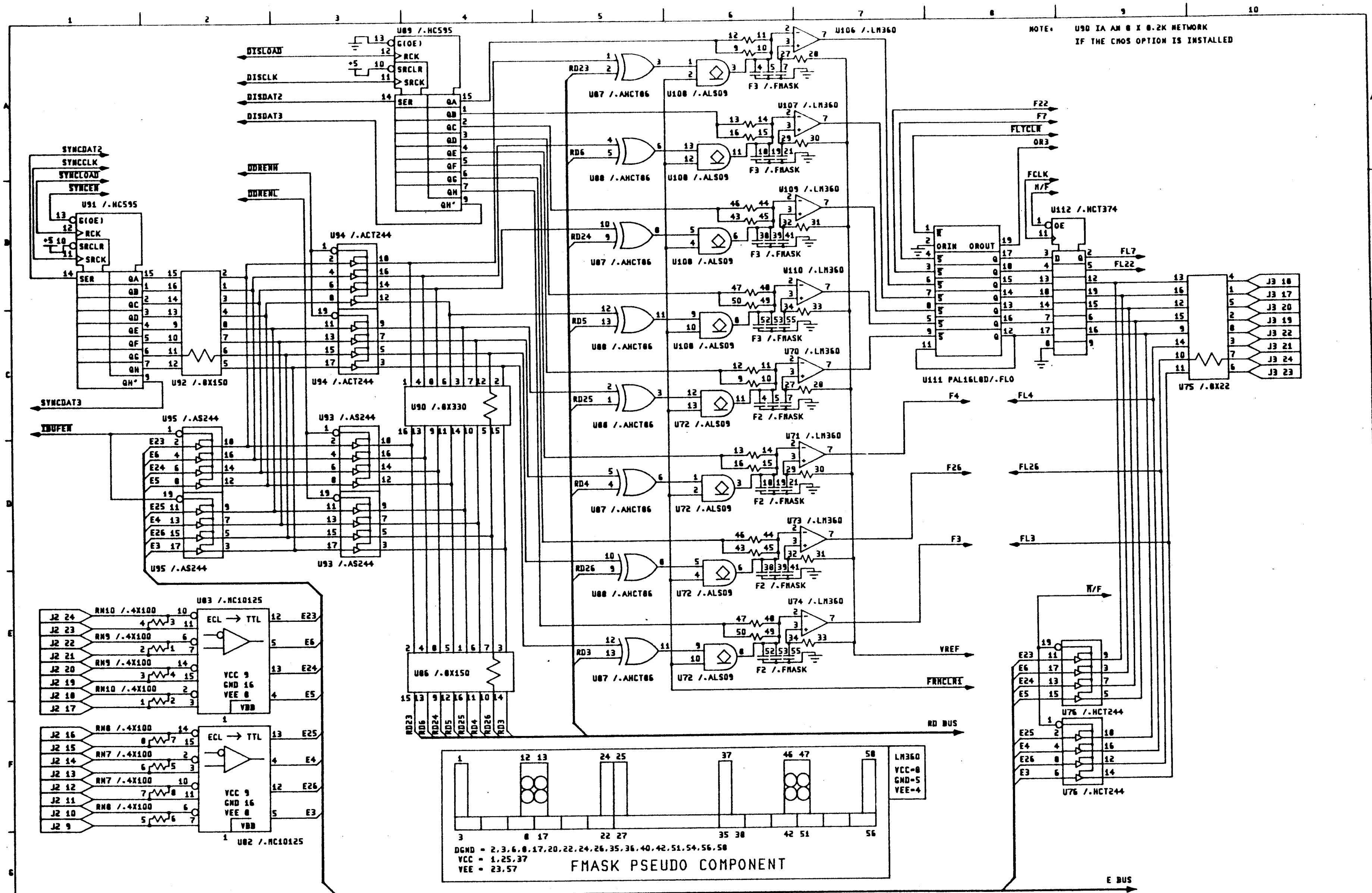
ZTEST

TITLE:	FLOW 2		PINS 7-10 19-22	PROJ:	TM3000	D/M/Y:	12/12/89
BOARD:	HIGH SPEED	FILE:	FLOW2.CSD	DWG.	SM508	REV. 3	PARENT SHEET #	SHEET 9 OF 12



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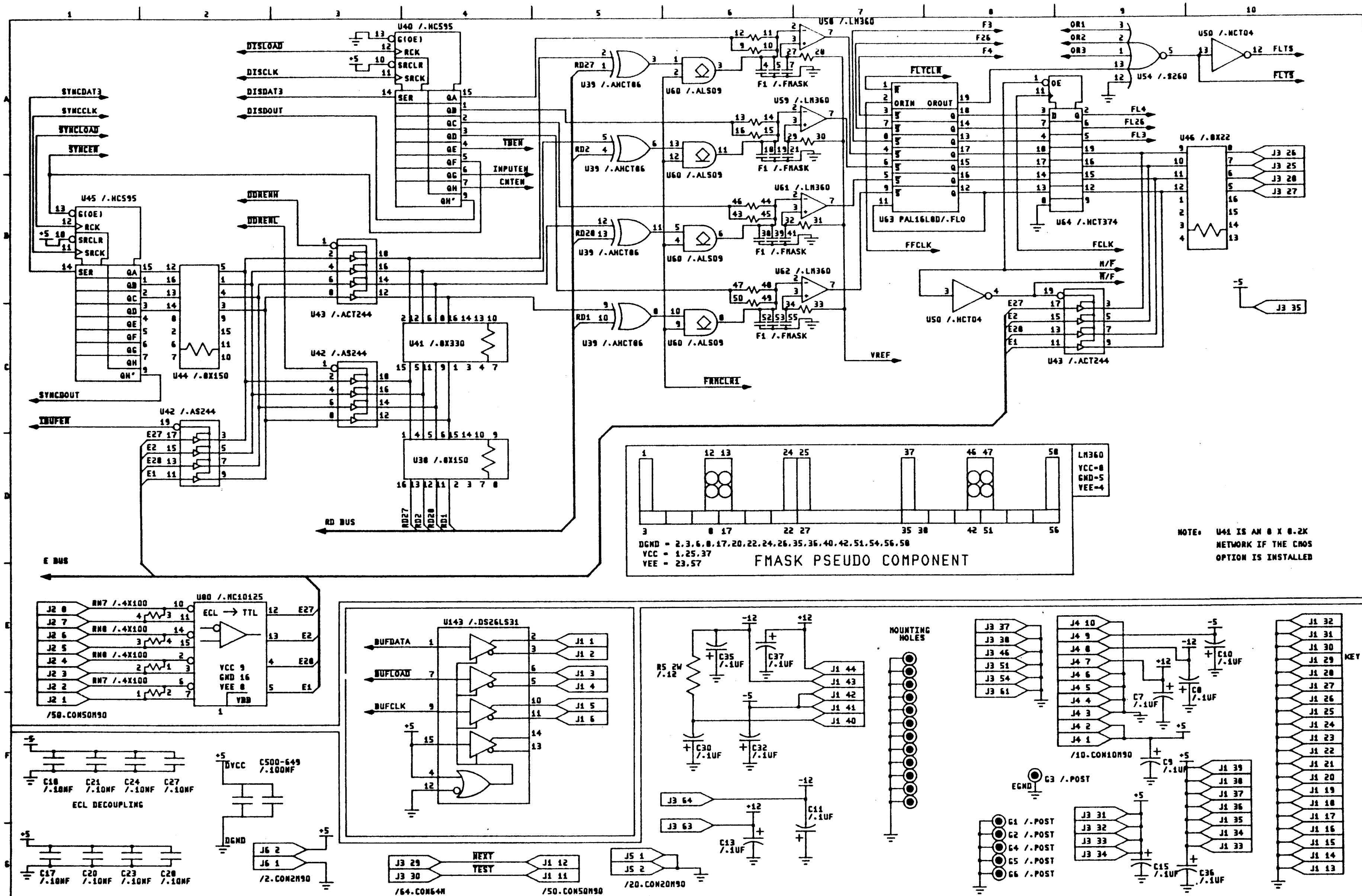
ZTEST

TITLE:	FLOW 3	PINS 3-6 23-26	PROJ:	TM3000		D/M/Y:	12/12/89
BOARD:	HIGH SPEED	FILE: FLOW3.CSD	DWG.	SM508	REV. 3	PARENT SHEET #	SHEET 10 OF 12



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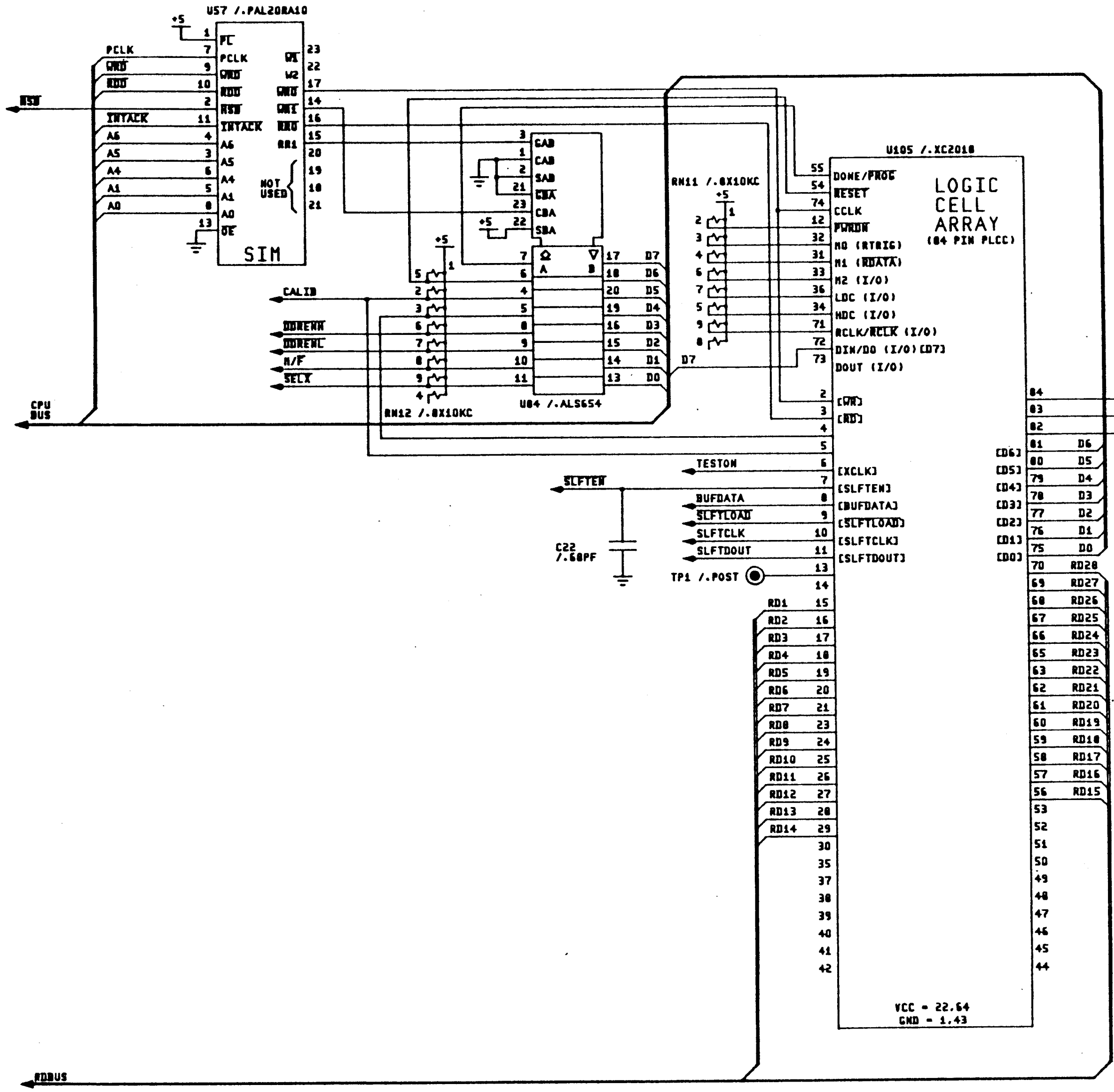
ZTEST

TITLE: FLOW 4	PINS 1,2 27,28	PROJ: TM3000		D/M/Y: 12/12/89	
BOARD: HIGH SPEED	FILE: FLOW4.CSD	DWG. SM508	REV. 3	PARENT SHEET #	SHEET 11 OF 12



STATE	REG.	B7	B6	B5	B4	B3	B2	B1	B0
CONFIG.	WR0	DIN	X	X	X	X	X	X	X
	RR0	X	X	X	X	X	X	X	X
	WR1	D/$\overline{\text{F}}$	$\overline{\text{RST}}$	SPARE	SPARE	$\overline{\text{DDRENH}}$	$\overline{\text{DDRENL}}$	M/F	$\overline{\text{SELX}}$
	RR1	D/$\overline{\text{F}}$	$\overline{\text{RST}}$	SPARE	SPARE	$\overline{\text{DDRENH}}$	$\overline{\text{DDRENL}}$	M/F	$\overline{\text{SELX}}$
USER	WR0	D7	D6	D5	D4	D3	D2	D1	D0
	RR0	D7	D6	D5	D4	D3	D2	D1	D0
	WR1	D/$\overline{\text{F}}$	$\overline{\text{RST}}$	CALIB	SPARE	$\overline{\text{DDRENH}}$	$\overline{\text{DDRENL}}$	M/F	$\overline{\text{SELX}}$
	RR1	D/$\overline{\text{F}}$	$\overline{\text{RST}}$	CALIB	SPARE	$\overline{\text{DDRENH}}$	$\overline{\text{DDRENL}}$	M/F	$\overline{\text{SELX}}$

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ZTEST

TITLE: RD EMULATION	PROJ: TM3000	D/M/Y: 12/12/89	
BOARD: HIGH SPEED	FILE: RDEMUL.CSD	DWG. SM508	REV. 3
PARENT SHEET #	SHEET 12 OF 12		

7 Fluke 900 Parts Lists

This section provides parts lists for the 900 and its assemblies. Components are listed alphanumerically by reference designator for each assembly.

The parts lists contain the following information:

- o Reference Designator
- o Description
- o Fluke Part Number
- o Total Quantity of part on assembly
- o Number of informational note (if applicable)

Parts Lists and Assemblies

7.1 900 Final Assembly

REFERENCE DESIGNATORS	DESCRIPTION	FLUKE PART NO	TOT QTY	NOTE
A1	IB PWB WITH CABLES	863451	1	1
A2	MICROPROCESSOR PWB	859780	1	2
A3	HIGH SPEED PWB, W/SIMU	865303	1	3
A4	POWER SUPPLY MODULE	858089	1	3
ASM1	TEST CLIP, 16 PIN DIP (0.3")	859053	1	
ASM2	TEST CLIP, 24 PIN DIP (0.3")	859074	1	
ASM3	TEST CLIP, 28 PIN DIP (0.6")	859293	1	
ASM4	TEST LEAD KIT,PVC,5 PROBES/5 LEADS	867226	1	
ASM5	RD TRAY AND CARTRIDGE HOLDER (1)	858993	1	
ASM6	DATA CARTRIDGE, 32K, (1)	857565	1	
ASM7	900 OPERATOR'S MANUAL	859400	1	
B1	TOP COVER/KEYBOARD ASSY.	883624	1	2
B1	FLUKE IB TOP COVER	940903	1	1
B2	FLUKE IB BOTTOM COVER	940908	1	1
B2	FLUKE 900 BOTTOM COVER	940916	1	3
F1-4	NEOPRENE DISCS	941554	4	3
I1-15,	BARB SERT (INSERT)	941596	17	3
IN1,IN2		941596		2
IN3-6	BARB SERT (INSERT)	941591	4	2
J1,J2	40 PIN CONNECTOR	941158	2	4
J3,J6	CONNECTOR STRIP	941133	3	4
J4,J5	20 PIN CONNECTOR	941161	2	4
J6-9	POLARIZATION PLUG	941146	4	4
K1	KEYBOARD	863472	1	2
K1-5	CLIP SET,PINCER,W/.025 DIA PIN	867080	1	
M1	AC LINE CORD	941356	1	
M1	HEX SOCKET	941500	1	2
M1-4	4X5/16 PHILIPS SCREW	941547	4	5
M1-4	RUBBER FEET	941372	4	1
M2	HEX THRD SPACER	941450	1	2
M2-6,	4X5/16 PHILIPS SCREW	941547	17	2
M7-14,		941547		3
M14-17		941547		4
M4	NON GLARE WINDOW PL	941468	1	4
M5,M6	TAP SCR PH	941455	2	4
M5-8	NPRN WASHER	941430	4	5
M5-8	HEX SOC SCR BH	941401	4	1
M7,M8	THRD-CTNG SCR P	941435	2	4
M9-12,M20-23	NPRN WASHER	941430	8	4
M9-12	FL LKWSHR INT	941393	4	5
M15	LABEL,ADHES,VINYL,BAR CODE,1.500,.312	844712	1	3
M17-21	RUBBER BUMPERS	941427	5	1
M19	WEATHER STRIPPING	921262	1	4
M20	CAUTION FLUKE LABEL	858105	1	2
M21	REAR PANEL FL. LABEL	858105	1	3
M22-25	MACH SCREW PH STL	941380	4	1
M22-26,	FL LKWSHR INT	941393	14	2
M27-35		941393		3
P1-5	TEST LEAD KIT,PVC,5 PROBES/5 LEADS	867226	1	
R1	RESISTOR 2.2K 1/4W 5%	941914	1	4
S/N	LABEL,ADHES,VINYL,BAR CODE,1.500,.312	844712	1	1
STA	CLIP, SELF TEST ASSY	919225	1	
SUB1	DISPLAY MODULE	859785	1	4
SUB2	CABLE ASSY. 20 POS.	883637	1	4

REFERENCE DESIGNATORS	DESCRIPTION	FLUKE PART NO	TOT QTY	NOTE
SUB3	SPEAKER ASSY.	883629	1	2
SUB3	DISPLAY CONTROLLER	859801	1	4
SUB4	CABLE ASSY. 40 POS.	883640	1	4
U1	CHARACTER ROM, PROGRAMMED	925276	1	4

NOTES:

1 = Used for Interface Buffer final assembly

2 = Used for Main Top final assembly

3 = Used for Main Bottom final assembly

4 = Used for Display modules final assembly

5 = Used for Speaker final assembly

7.2 A1 Interface Buffer IB

REFERENCE DESIGNATORS	DESCRIPTION	FLUKE PART NO	TOT QTY	NOTE
B1	FLUKE IB TOP COVER	940903	1	1
B2	FLUKE IB BOTTOM COVER	940908	1	1
C1,C2,C115-122,C124-127,	CAP 100nF .2 SPA	940994	27	
C130-141,C144	CAP 100nF .2 SPA	940994		
C3-31	CAP 100pF .1 SPA	940973	29	
C32-60	CAP 1.5pF 20% .1 SPA	940932	29	
C61-89	CAP 10nF .1 SPA	940981	29	
C90-114	CAP 10nF .2 SPA	940986	25	
C123,C128	CAP 10uF .2S TANT 25	941013	2	
C129	CAP 1uF .1 SPA	941000	1	
C142	CAP 56 pF .2 SPAC	940957	1	
C143	CAP 1nF .2 SPAC	940978	1	
CM1,CM2	CONNECTOR	941067	2	
CM3,CM4	CABLE EXTRACTOR	941070	2	
CM5	FLAT CABLE TIE	941414	3	
CM6	IB CABLE SET	864616	1	2
D1-58	DIODE	940528	58	
EXT,GND,GND,RST,V	JACKS EXTENDER PIN	941281	5	
EXT,GND,GND,RST,V	JACK	941278	5	
J1,J2	CONNECTOR-50 PIN STG	941062	2	
J1	POLARIZATION PLUG	941146	1	
J3	CONNECTOR	941088	1	
K1,K2	KEY - SWITCH-CAP	941286	2	
M1-4	RUBBER FEET	941372	4	1
M5-8	HEX SOC SCR BH	941401	4	1
M14	CONN. POLARIZING INS	941112	1	
M15	J1 & J2 FL. LABELS	941567	1	
M17-21	RUBBER BUMPERS	941427	5	1
M22-25	MACH SCREW PH STL	941380	4	1
NUT	HEX NUT STL	941398	3	
Q1	PNP TRANSISTOR	940572	1	
Q1-H	FL FBR WASHER	941443	1	
R1	RES,CF,47,+-5%,0.25W	441592	1	
R2-4,R37	RESISTOR 10K .25W 1%	941901	4	
R33	RESISTOR 330K .25W 5%	941922	1	
R34,R39,R40,R43,R44,R47	RESISTOR 1K .25W 5%	941864	6	
R35,R42	RESISTOR 10K .25W 5%	941893	2	
R36	RESISTOR 39K .25W 1%	941919	1	
R38,R46	RESISTOR 8.2K .25W 5%	941885	2	
R41	RESISTOR 22K .25W 5%	941914	1	
R45	RESISTOR 10 OHM .25W 5%	941828	1	
R48-51	RESISTOR 10K .25W 0.1%	941898	4	
R52	RESISTOR 5.1K .25W 5%	941880	1	
R53	RESISTOR 15K .25W 5%	941906	1	
R54,R55	RESISTOR 10 OHM 2W	941831	2	
R56	RESISTOR 237 OHM 1/4W 1%	941930	1	
R57	RESISTOR 402 OHM 1/4W 1%	941935	1	
RG1,RG2	REGULATOR -2V	941336	2	
RG3	REGULATOR -5.2V	941344	1	
RL1,RL2	RELAY	941815	2	
RN1-8,RN23-29,RN53	RN 4X10K SIP 8P 1%	942032	16	
RN9-15	RN 4X1K OHM SIP 8 2%	941997	7	
RN16-22	RN 4X39K SIP 8P 1%	942037	7	
RN30-36	RN 4X8K2 SIP 8 PIN	942016	7	
RN37-51	RN 4X56 OHM SIP5 2%	941968	15	

REFERENCE DESIGNATORS------------	--DESCRIPTION------------------------	FLUKE PART --NO--	TOT QTY-	NOTE
RN52	RN 3X120 OHM SIP 6PN	941976	1	
RN54-60	RN 4X33 KOHM SIP8 2%	941963	7	
S/N	LABEL,ADHES,VINYL,BAR CODE,1.500,.312	844712	1	1
SHRN	HEAT SHRINK 1/8 INCH	941497	5	
SUB2	IB CABLE SET	864616	1	2
SW1-3	MACH SCREW PH STL	941380	3	
U1-4,U23,U24	IC 74HC595	940809	6	
U5-19	IC 6687DL	940580	15	
U20	IC 26LS32	940549	1	
U21	QUAD 2 INPUT NAND	940598	1	
U22	IC 7407 HEX BUFFER	940619	1	
U25	8 BIT DAC	941211	1	
U26	OP AMP LM747	941323	1	
U27	IC ANALOG MUX	940895	1	
U28	IC V/F CONVERTER	940890	1	
U29	IC VOLT. REF.	940887	1	
U29H	FL FBR WASHER	941443	1	
WASH	FL LKWSHR INT	941393	3	

NOTES:

1 = Interface Buffer final assembly parts - not included in 863451 (A1)

2 = Part is complete IB cable set, including connectors (CM1-2 and J1-2), extractors (CM3-4), and cable ties (CM5).

7.3 A2 Micro Board M2

REFERENCE DESIGNATORS	DESCRIPTION	FLUKE PART NO	TOT QTY	NOTE
1-28,8P,14P,16P,18P,	RED LED 3-5	941245	36	
20P,22P,24P,28P		941245		
C1-4,C7-9,C16,C19-22,	CAP 100 nF .3 SPAC	940999	74	
C25-27,C32-41,C43,		940999		
C45-54,C58-70,C72,		940999		
C74-84,C86,C89-95,		940999		
C98-100,C106,C110		940999		
C5,C6	CAP 47uF 10V AXIAL	941018	2	
C23,C24,C28,C29	CAP 100nF .2 SPA	940994	4	
C42,C44,C71	CAP 10uF RADIAL .1	941005	3	
C73	CAP 100uF 10V RADIAL	941021	1	
C85	CAP 47 pF .2 SPA	940952	1	
C87	CAP 22pF .2 SPA	940937	1	
C88	220 pF CAP .2 SPAC	941026	1	
C96,C97,C101,C102	CAP 33pF .2 SPA	940940	4	
C111	10 MF 25V AXIAL CAP	941047	1	
CR1	CRYSTAL - 12 MHZ	941195	1	
CR2	CRYSTAL - 6.144 MHZ	941203	1	
CR	CR BRACKET	941484	1	
D1	DIODE - 8.2V ZENER	940536	1	
D2	DIODE	940528	1	
J1,J4	CONNECTOR STRIP	941133	2	
J2	JACK	941273	2	
J3	CONNECTOR 64 PIN F	941138	1	
J3	CONNECTOR-64PIN STAG	941091	1	
J5	CONNECTOR	941096	1	
J6	CONNECTOR - RT ANGLE	941104	1	
M1,M8	MACH SCREW PH STL	941385	2	
M2,M7	MACH SCREW PH STL	941380	2	
M3,M4	FL LKWSHR INT	941393	2	
M5,M6	HEX NUT STL	941398	2	
P1	POT 20K	941765	1	
PON	LED - GREEN	941252	1	
R1	RESISTOR 1 OHM 1/4W 5%	941823	1	
R2-5,R9,R10	RESISTOR 10K 1/4W 1%	941893	6	
R6,R7	RESISTOR 22 OHM 1/4W 5%	941844	2	
R8	RESISTOR 1K 1/4W 5%	941864	1	
R11,R17	RESISTOR 4.7K 1/4W 5%	941877	2	
R13,R14	RESISTOR 470 OHM 1/4W 5%	941856	2	
R15,R16	RESISTOR 1.5K 1/4W 5%	941869	2	
R18	RESISTOR 100 OHM 1/4W 5%	941849	1	
R19,R20	RESISTOR 22 OHM 1/4W 1%	941836	2	
R21	RESISTOR 150K 1/4W 5%	941950	1	
RG1	REGULATOR 5V	941331	1	
RG2	REGULATOR -5V	941349	1	
RN1,RN2,RN6	RN 4X10K SIP 5 PIN	942024	3	
RN3,RN4	RN 8X10K SIP 9 PIN	942029	2	
RN5,RN16	RN 8X4K7 SIP 9 PIN	942011	2	
RN9-11,RN13,RN14	RN 4X680 OHM SIP 9PN	941992	5	
RN12,RN15	RN 4X1K SIP 5 PIN	942003	2	
SP1	SPACER 1	921267	1	
SP2	SPACER 2	921671	1	
SP3,SP4	SPACER 3	921676	2	
SUB2	CABLE,64 POS	912063	1	

REFERENCE DESIGNATORS------------	--DESCRIPTION------------------------	FLUKE PART --NO--	TOT QTY-	NOTE
T1	PNP TRANSISTOR	940572	1	
T2	TRANSISTOR 2N2369A	921242	1	
T1-H,T2-H	FL FBR WASHER	941443	2	
U1,U2	RS232C DRIVER	941328	2	
U3,U55	IC 74ALS00	940585	2	
U4,U5	RS232C RECEIVER	940523	2	
U6,U8,U23,U24,U47	IC 74HCT245	940762	5	
U7	IC 74HCT257	940775	1	
U9,U10,U13,U46,U49,	IC 74HCT244	940754	8	
U50,U64,U65		940754		
U11	IC 8531A	940874	1	
U14,U15,U17-20,U36	IC 74AHCT86	940841	7	
U16,U21,U22,U32	IC PAL-ACT	941609	4	
U25	OPTO COUPLER	941257	1	
U26,U27	IC 8536A	940879	2	
U31,U33-35,U41-44	IC 74HCT373	940791	8	
U37	IC 74HCT02	940606	1	
U38	IC 74HCT138	940663	1	
U45	IC 74HCT374	940796	1	
U48,U53,U54,U67,U81	RN 8X22 OHM DIP 16PN	941955	5	
U51	CPU, 6 MHZ	940866	1	
U52,U68	IC 74ACT244	940759	2	
U56,U71	IC 74ALS1005	940648	2	
U57	IC PAL-DEC1B	941617	1	
U58	DECODER PAL-DEC3B	941638	1	
U59	DECODER PAL-DEC2B	941625	1	
U60,U61,U75-77	900 SYSTEM ROM SET, V5.05	890751	1	1
U62,U63	8K X 8 STATIC RAM	941794	2	
U66	IC 74ALS244	940742	1	
U69	WAIT STATE GENERATOR PAL-WSGB	941760	1	
U70	IC 74N14	940671	1	
U72	IC PAL-DEC4	941641	1	
U73	IC PAL-DEC5	941646	1	
U78	IC CLOCK GENERATOR	940882	1	
U79,U80	IC 74ALS157	940689	2	
U85,U89	DYNAMIC RAM 64K X 4	941786	2	
U90	IC 74HCT14	940676	1	
XU51	SOCKET - 40 PIN	942073	1	
XU60,XU61,XU74-77	SOCKET - 28 PIN	942065	6	
XU62	SMART WATCH	941351	1	

NOTES:

1 = V5.05 ROM set - 4 System ROMs and Library ROM. V6.00 ROM set is 921072.

7.4 A3 High Speed H3

REFERENCE DESIGNATORS	DESCRIPTION	FLUKE PART NO	TOT QTY	NOTE
B1-4	RUBBER FEET	941604	4	
C1,C4	CAP 1nF .2 SPAC	940978	2	
C2,C7-11,C13,C15,	CAP 1uF .1 SPA	941000	15	
C30,C32-37		941000		
C3,C17,C18,C20,C21,	CAP 10nF .2 SPA	940986	9	
C23,C24,C27,C28		940986		
C5,C22	CAP 68pF .2 SPA	940960	2	
C6	CAP 82pF .2 SPA	940965	1	
C12	CAP 22pF .2 SPA	940937	1	
C16,C19,C25,C26,C29,	CAP 100 nF .3 SPAC	940999	155	
C31,C500-582,C584-649		940999		
C1B1-4,C2B1-4,	CAP 47pF 2% .1 SPAC	940945	28	
C321-4,C4B1-4,		940945		
C5B1-4,C6B1-4,		940945		
C7B1-4		940945		
C1C1-4,C2C1-4,	CAP 10nF .1 SPA	940981	28	
C3C1-4,C4C1-4,		940981		
C5C1-4,C6C1-4,		940981		
C7C1-4		940981		
C1D1-5,C2D1-5,	CAP 100 nF .3 SPAC	940999	35	
C3D1-5,C4D1-5,		940999		
C5D1-5,C6D1-5,		940999		
C7D1-5		940999		
CR1	CRYSTAL - 25 MHZ	941190	1	
J1,J2	CONNECTOR	941059	2	
J3	CONNECTOR	941075	1	
J4	CONNECTOR	941083	1	
L1	INDUCTOR 2.2uH	941260	1	
M1,M2	RUBBER FEET	941372	2	
M3	HEX NUT STL	941398	1	
Q1	REGULATOR 5V	941331	1	
R1	RESISTOR 4.7K .25W 5%	941877	1	
R2,R3	RESISTOR 22 OHM .25W 5%	941836	2	
R5	12 OHM RESIS. 5W	941943	1	
R6	RESISTOR 10 OHM 2W 5%	941831	1	
R7,R8	RESISTOR 1K .25W 5%	941864	2	
R1B1-4,R2B1-4,	RESISTOR 4.7K 1% 0.25W	941872	28	
R3B1-4,R4B1-4,		941872		
R5B1-4,R6B1-4,		941872		
R7B1-4		941872		
1RN,2RN,3RN,	8 PIN 4X4.7K SIP	942040	7	
4RN,5RN,6RN,		942040		
7RN		942040		
RN1-5,RN18,RN19	RN 8X4K7 SIP 9 PIN	942011	7	
RN6	9x10K 10 PIN	942060	1	
RN7-10,RN13,RN14,	RN 4X100 OHM SIP 8PN	941971	8	
RN17,RN20		941971		
RN11,RN12,RN15,RN16	RN 8X10K SIP 9 PIN	942029	4	
SPC1-4	FBR SPACER	941448	4	
U1,U2,U6,U16,	IC 74HC595	940809	24	
U19,U40,U45,		940809		
U56,U67,U78,		940809		
U89,U91,U96,		940809		
U100,U102,U134,		940809		

REFERENCE DESIGNATORS------------	--DESCRIPTION------------------------	FLUKE PART --NO--	TOT QTY-	NOTE
U136,U155,U166,		940809		
U168,U180,U182,		940809		
U188,U189		940809		
U3,U4,U11,U12,U17	IC 74F191	940726	5	
U5	IC 74AS11	940650	1	
U7	IC 74AS153	940684	1	
U9	PAL-IOD1-B	941708	1	
U10	PAL-IOD2-B	941716	1	
U13	IC 74AS10	940643	1	
U14,U21	IC 74AS00	940593	2	
U15	IC 74AS08	940627	1	
U18	IC 74AS86	940846	1	
U20	IC 2925	940569	1	
U22	IC 74HCT164	940713	1	
U23	PAL-FREQ-B	941687	1	
U24,U31	IC 74AS74	940833	2	
U25	IC 74HCT161	940697	1	
U26,U27	IC 8536A	940879	2	
U28,U48	IC 74HCT74	940838	2	
U29	IC PAL-GATE	941690	1	
U30	IC PAL-TC	941752	1	
U32	IC 74ALS74	940825	1	
U33	IC PAL-SHIFT	941740	1	
U34	IC PAL-PSC	941724	1	
U35,U37,U76,U122,U164	IC 74HCT244	940754	5	
U36	IC 74LS598	940812	1	
U38,U44,U86,U92,U131,	RN 8X150 OHM DIP 16P	941984	8	
U137,U177,U183		941984		
U39,U87,U88,U132,U133,	IC 74AHCT86	940841	7	
U178,U179		940841		
U41,U90,U135,U181	RN 8X330 OHM DIP 16P	941989	4	
U42,U93,U95,U138,U140,	IC 74AS244	940747	7	
U184,U186		940747		
U43,U94,U139,U185	IC 74ACT244	940759	4	
U46,U75,U121,U163	RN 8X22 OHM DIP 16PN	941955	4	
U47	IC 74AS241	940739	1	
U49	IC PAL-SHAD1	941732	1	1
U50	IC 74HCT04	940614	1	
U51	IC 74F161	940700	1	
U52	IC 74LS251	940767	1	
U53	IC PAL-SHAD2	941737	1	1
U54	IC 74S260	940783	1	
U55,U66,U124,U141	IC 74HCT251	940770	4	
U57	IC PAL-SIM	941745	1	
U58,U59,U61,U62,	IC LM360	941310	28	
U70,U71,U73,U74,		941310		
U106,U107,U109,		941310		
U110,U116,U117,		941310		
U119,U120,U147,		941310		
U148,U150,U151,		941310		
U158,U159,U161,		941310		
U162,U192,U193,		941310		
U195,U196		941310		
U60,U72,U108,U118,	74ALS09 GROUP B OR C	NOTE 2	7	2
U149,U160,U194		NOTE 2		
U63,U111,U152,U197	IC PAL-FLO	941679	4	
U64,U112,U153,U198	IC 74HCT374	940796	4	

A3 High Speed (cont.)

REFERENCE DESIGNATORS	DESCRIPTION	FLUKE PART NO	TOT QTY	NOTE
U65,U97,U167,U187	RN 8X1 KOHM DIP 16P	942008	4	
U68	8 BIT DAC	941211	1	
U69	OP AMP	941315	1	
U77	IC 74HCT245	940762	1	1
U79,U99,U165,U190	IC 74F521	940804	4	
U80,U82,U83,U101,U104,	TRANSISTOR 2N2369A	921242	8	
U113,U125,U199		921242		
U81,U98,U154,U191	IC 74ALS639	940817	4	
U84	IC 74ALS654	940820	1	
U85,U103,U115,U127-130,	DIP RELAY	941810	18	
U144,U146,U156,U157,		941810		
U169,U171-176		941810		
U105,	GATE ARRAY	942131	2	
U123		942131		1
U114,U126,U170	IC 7407 HEX BUFFER	940619	3	
U142	64Kx1 SRAM	941802	1	1
U143	IC 26LS31	940544	1	
U145	28 PIN BLK ZIF SOCKT	942149	1	
XU49,XU77	20 PIN SOCKET	942094	2	
XU53,XU142	24 PIN N. SOCKET	942099	2	
XU105,XU123	84 PIN PLCC SOCKET	942078	2	
XU145	ZIP ADAPTOR	942144	1	
CALIBRATION COMPONENTS	CAP 1.0pF	921197		3
	CAP 1.5pF	921200		3
	CAP 1.8pF	921205		3
	CAP 2.2pF	921213		3
	CAP 3.3pF	921218		3
	CAP 4.0pF	921221		3
	CAP 6.8pF	921226		3
	RES 47K	921192		3
	RES 57K	921189		3
	RES 86K	921184		3
	RES 113K	921176		3
	RES 150K	921171		3
	RES 365K	921168		3

NOTES:

1 = Optional: part of -001 Simulation option

2 = Selected parts: all seven 74ALS09 must be the same color code (speed). Use 921234 for orange dot (group B), 921239 for green dot (group C).

3 = Calibration resistors and capacitors are used in the procedure outlined in Section 5.4.2.5

7.5 A4 Power Supply Module PA

REFERENCE DESIGNATORS------------	--DESCRIPTION-------------------------	FLUKE PART --NO--	TOT QTY-	N O T -E
B1-6	RUBBER BUMPERS	941427	6	
CON1,CON2	CONNECTOR	941125	2	1
J5	CONNECTOR	941120	1	2
M1	POWER SUPPLY CAGE	941229	1	
M2	BUSS FUSE 3 AMP	941422	1	
M3	NON-INSULAT TERMINAL	941369	1	
MOD1	POWER SUPPLY	941778	1	
MOD2	FAN 24VDC 23CFM	941232	1	
MOD3	POWER CONNECTOR	941117	1	
P1-17,P87,P19,P20,	PINS	941364	23	1
P1-3		941364		2
S1-15	MACH SCREW PH STL	941380	15	
S16-19	STL MACH SCR SL	941463	4	
SUB1	POWER SWITCH ASSEMBLY	921247	1	
SUB2	AC CONNECTOR	921254	1	
SUB3	DC CONNECTOR	921259	1	
S1	POWER SWITCH	942110	1	3
S2	GREY CAP FOR SWT	941505	1	3
W1,	WIRE	921684	2	1
W1		921684		2
W1-17	FL LKWSHR INT	941393	17	

NOTES:

1 = Part of DC connector, P/N 921259

2 = Part of AC connector, P/N 921254

3 = Part of power switch assembly, P/N 921247

7.6 900-001 Simulation Option

REFERENCE DESIGNATORS	DESCRIPTION	FLUKE PART NO	TOT QTY	NOTE
U49	IC PAL-SHAD1	941732	1	
U53	IC PAL-SHAD2	941737	1	
U77	IC 74HCT245	940762	1	
U123	GATE ARRAY	942131	1	
U142	64Kx1 SRAM	941802	1	