

SCHEMATICS

2008JAN25

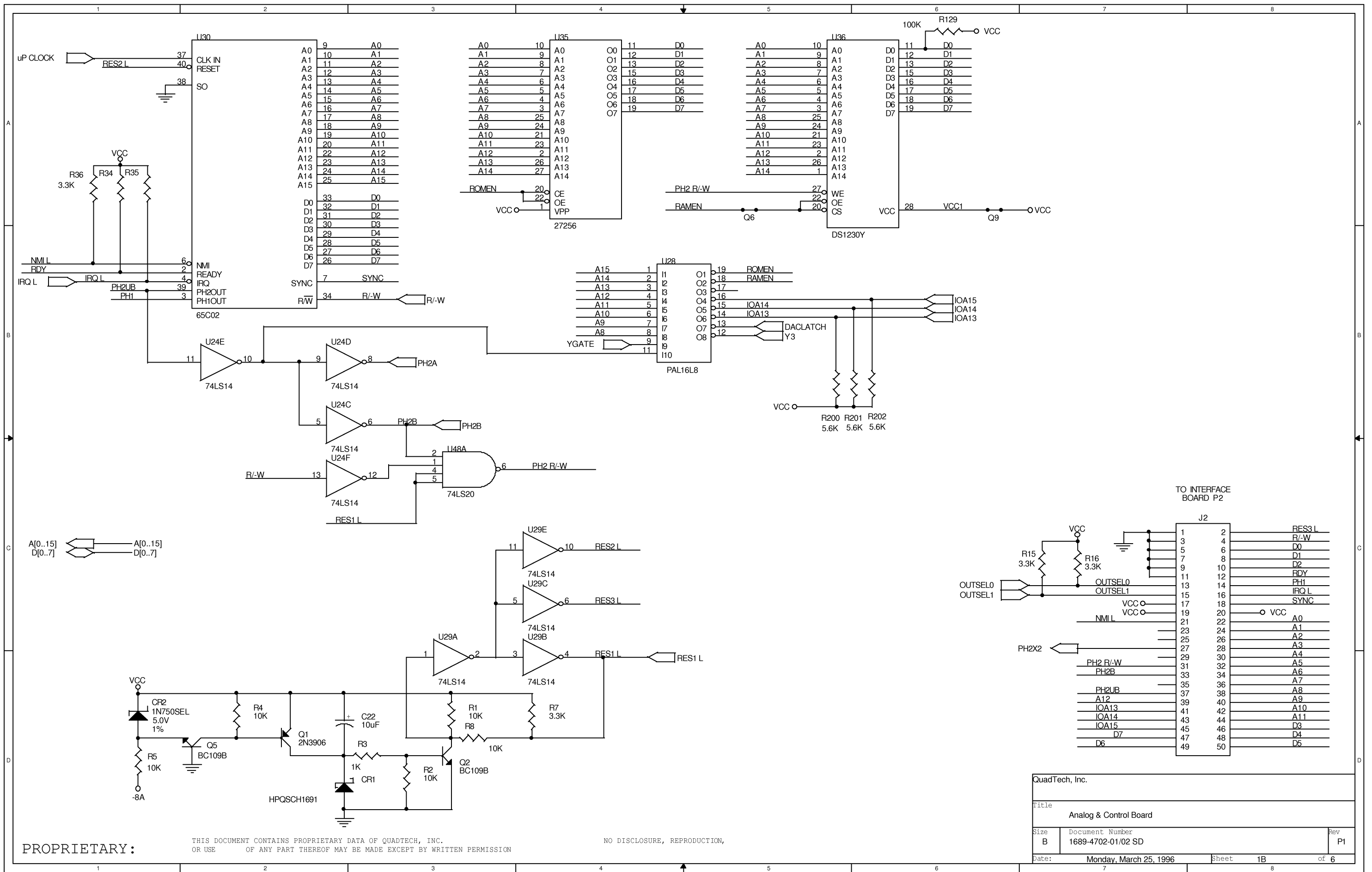
SECOND GENERATION GENRAD QUADTECH DIGIBRIDGE

1659

1689

1692

1689M

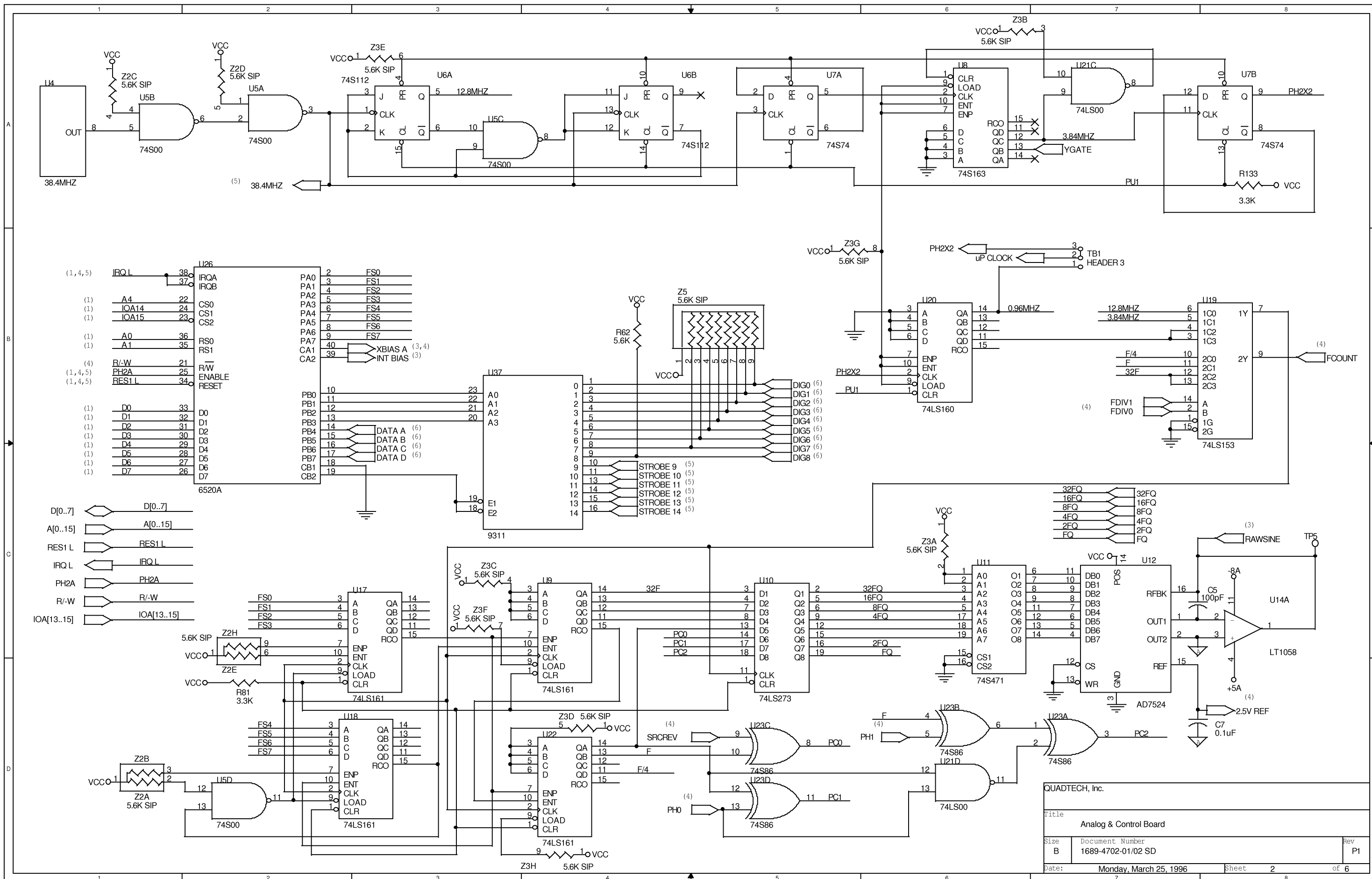


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Title Analog & Control Board			
Size B	Document Number 1689-4702-01/02 SD	Rev P1	
Date: Monday, March 25, 1996	Sheet 1B	of 6	

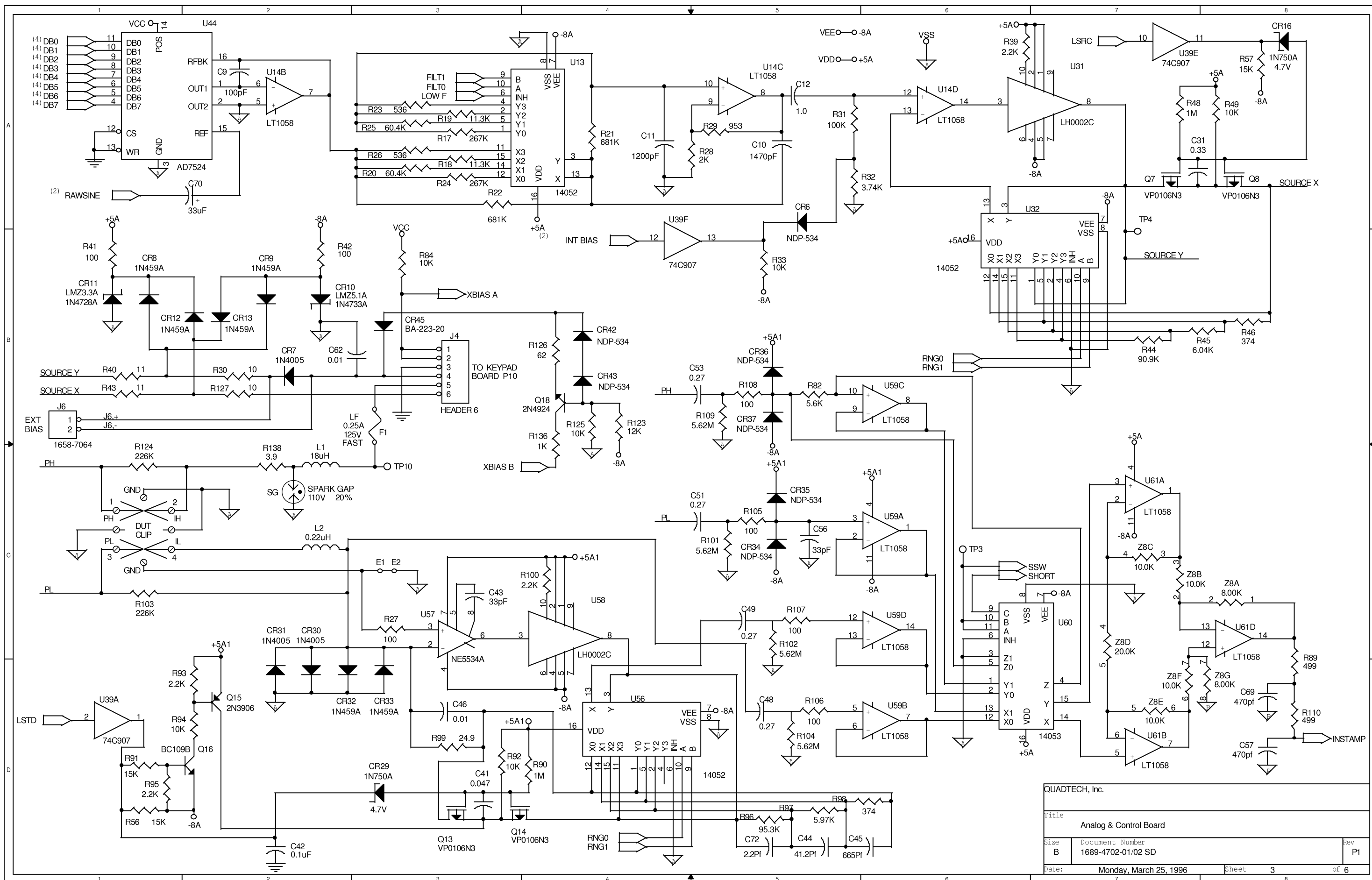


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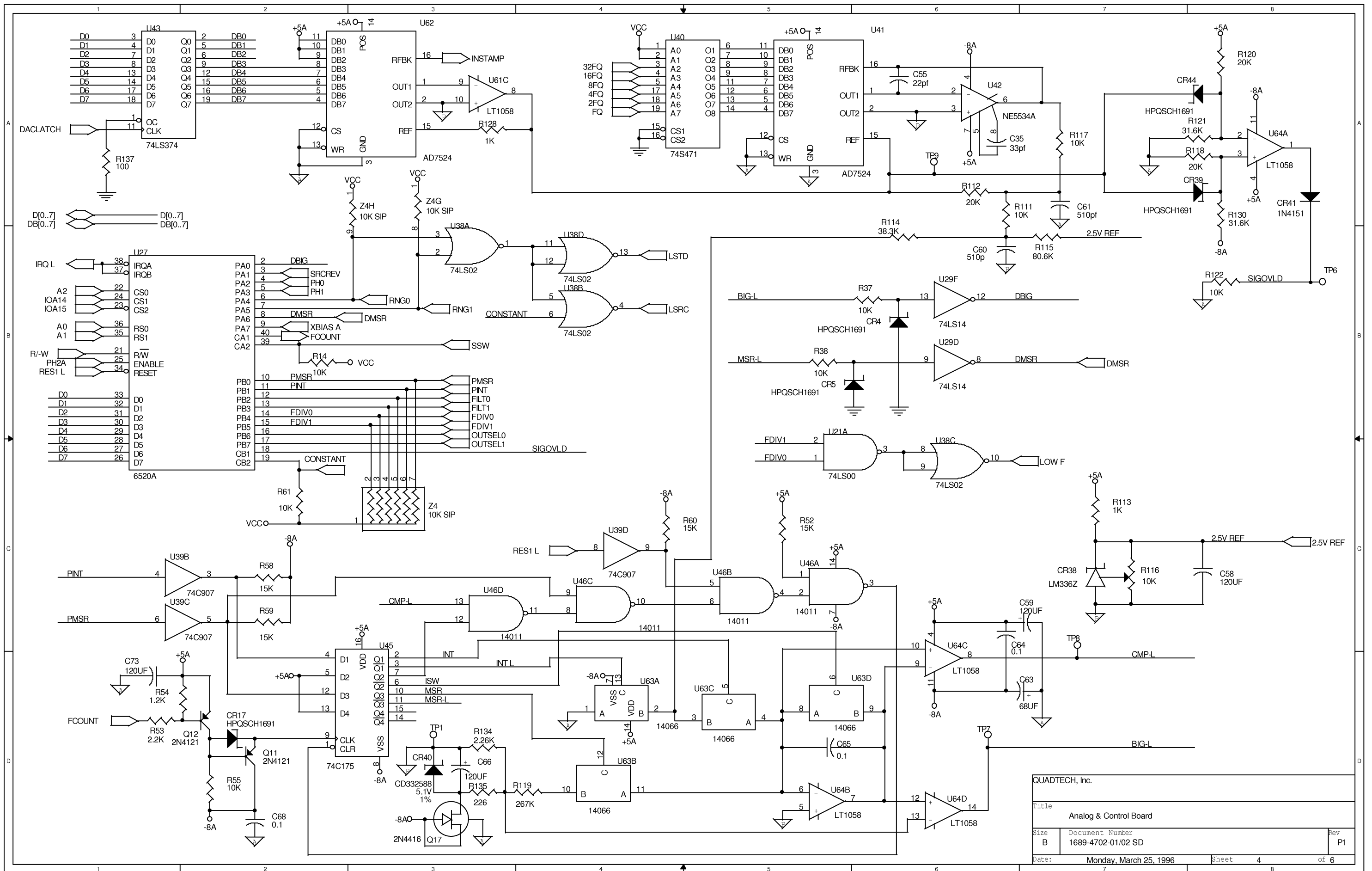
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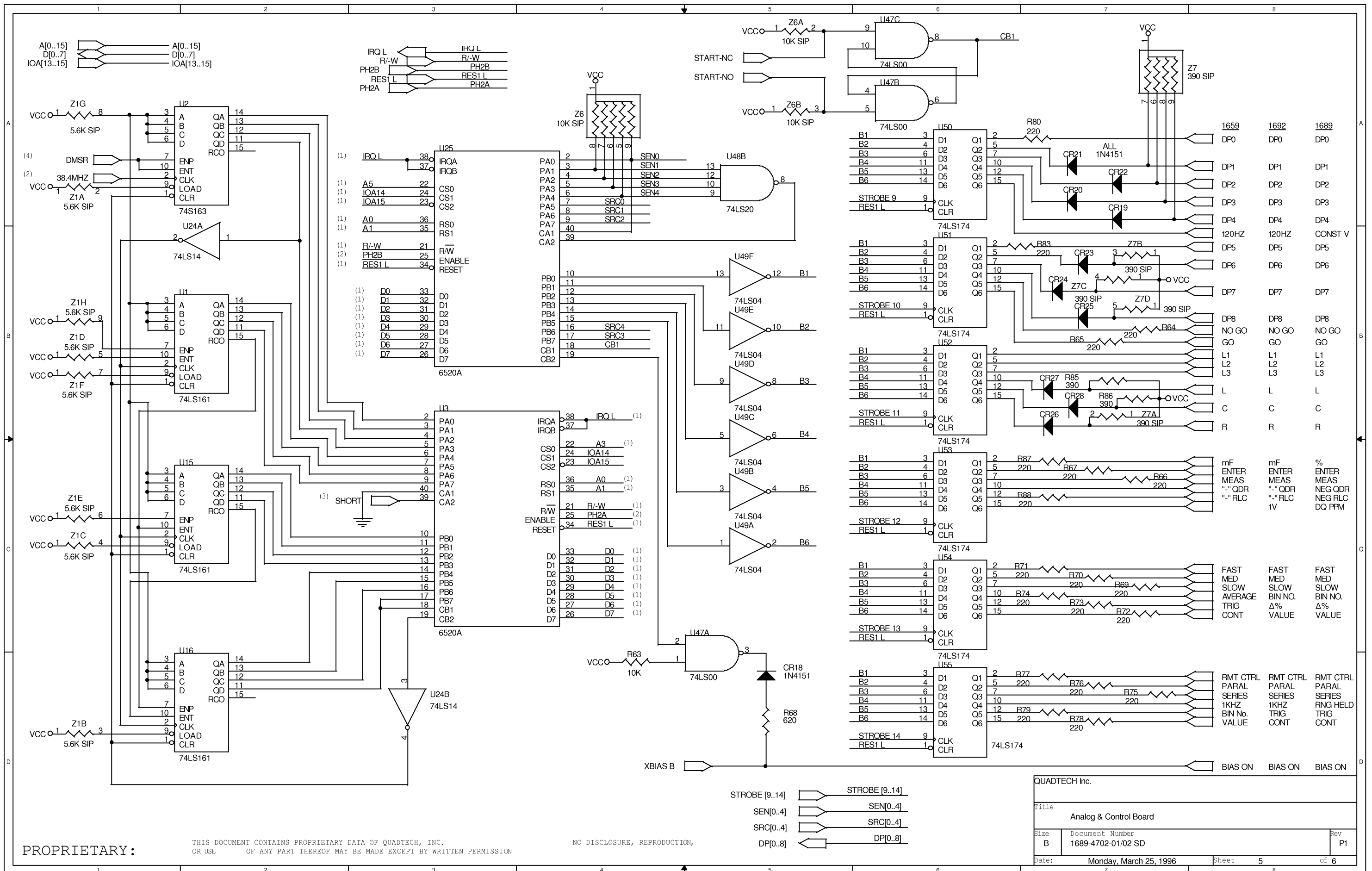
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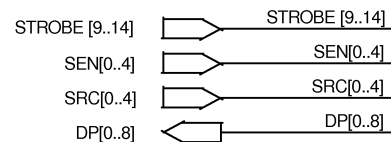
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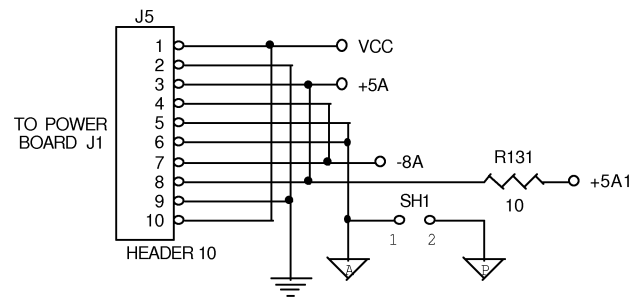
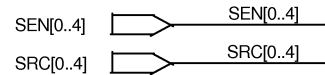
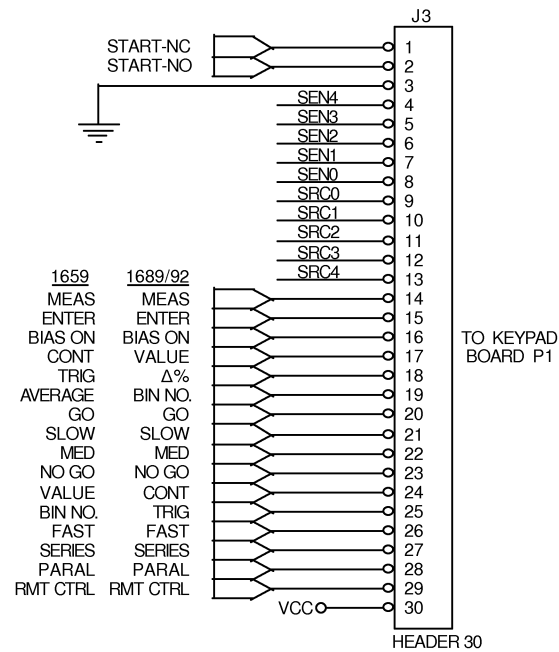


QUADTECH Inc.

Title
Analog & Control Board

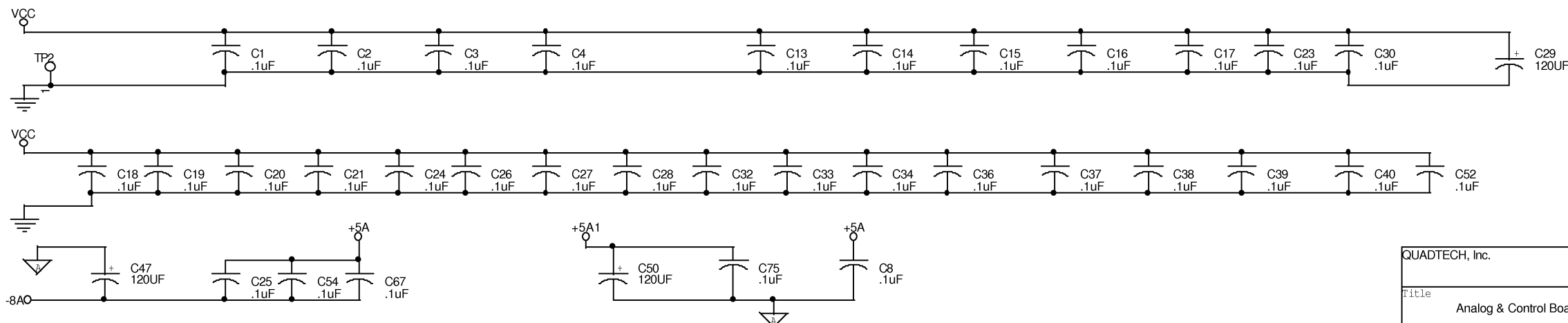
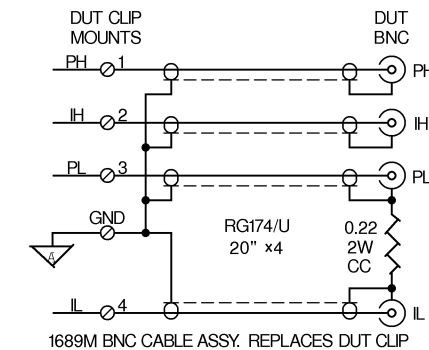
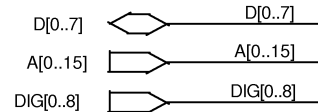
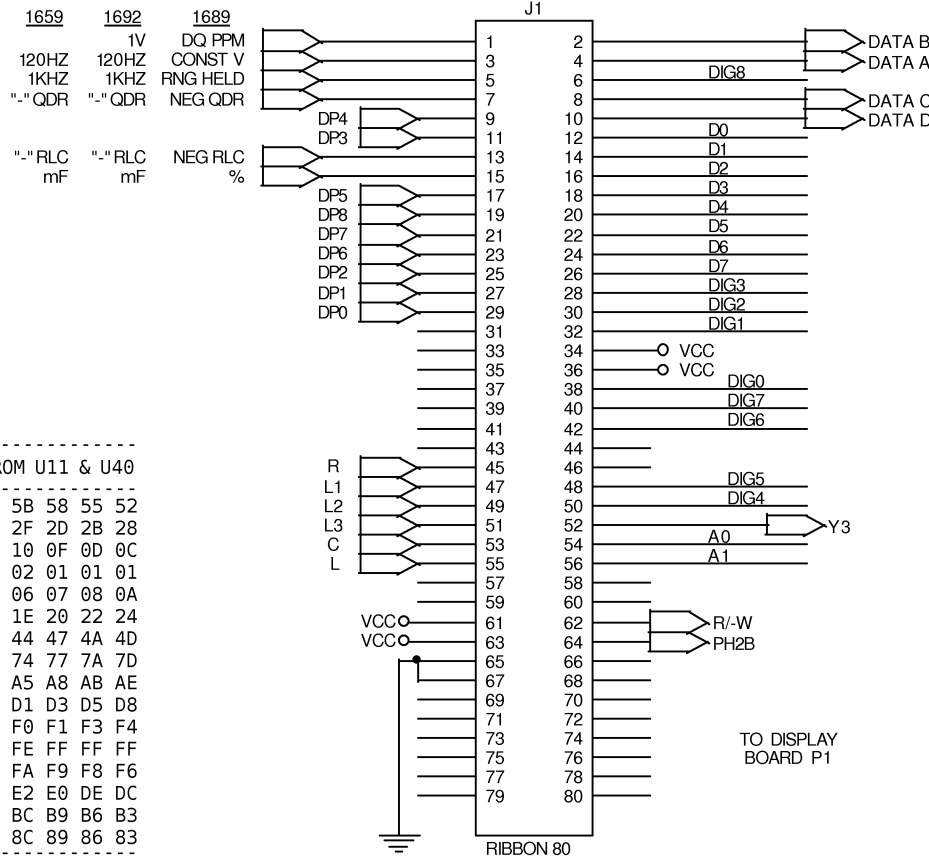
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CONTENTS OF 74S471 SINEWAVE GENERATION PROM U11 & U40

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0010	4F	4D	4A	47	44	41	3F	3C	39	37	34	32	2F	2D	2B	28
0020	26	24	22	20	1E	1C	1A	18	16	15	13	11	10	0F	0D	0C
0030	0B	0A	08	07	06	05	04	03	03	02	02	02	01	01	01	01
0040	01	01	01	01	02	02	02	03	03	04	05	06	06	07	08	0A
0050	0B	0C	0D	0F	10	11	13	15	16	18	1A	1C	1E	20	22	24
0060	26	28	2B	2D	2F	32	34	37	39	3C	3F	41	44	47	4A	4D
0070	4F	52	55	58	5B	5E	61	64	67	6A	6D	70	74	77	7A	7D
0080	80	83	86	89	8C	90	93	96	99	9C	9F	A2	A5	A8	AB	AE
0090	B1	B3	B6	B9	BC	BF	C1	C4	C7	C9	CC	CE	D1	D3	D5	D8
00A0	DA	DC	DE	E0	E2	E4	E6	E8	EA	EB	ED	EF	F0	F1	F3	F4
00B0	F5	F6	F8	F9	FA	FA	FB	FC	FD	FD	FE	FE	FE	FF	FF	FF
00C0	FF	FF	FF	FE	FE	FE	FD	FC	FB	FA	FA	F9	F8	F6	F6	F6
00D0	F5	F4	F3	F1	F0	EF	ED	EB	EA	E8	E6	E4	E2	E0	DE	DC
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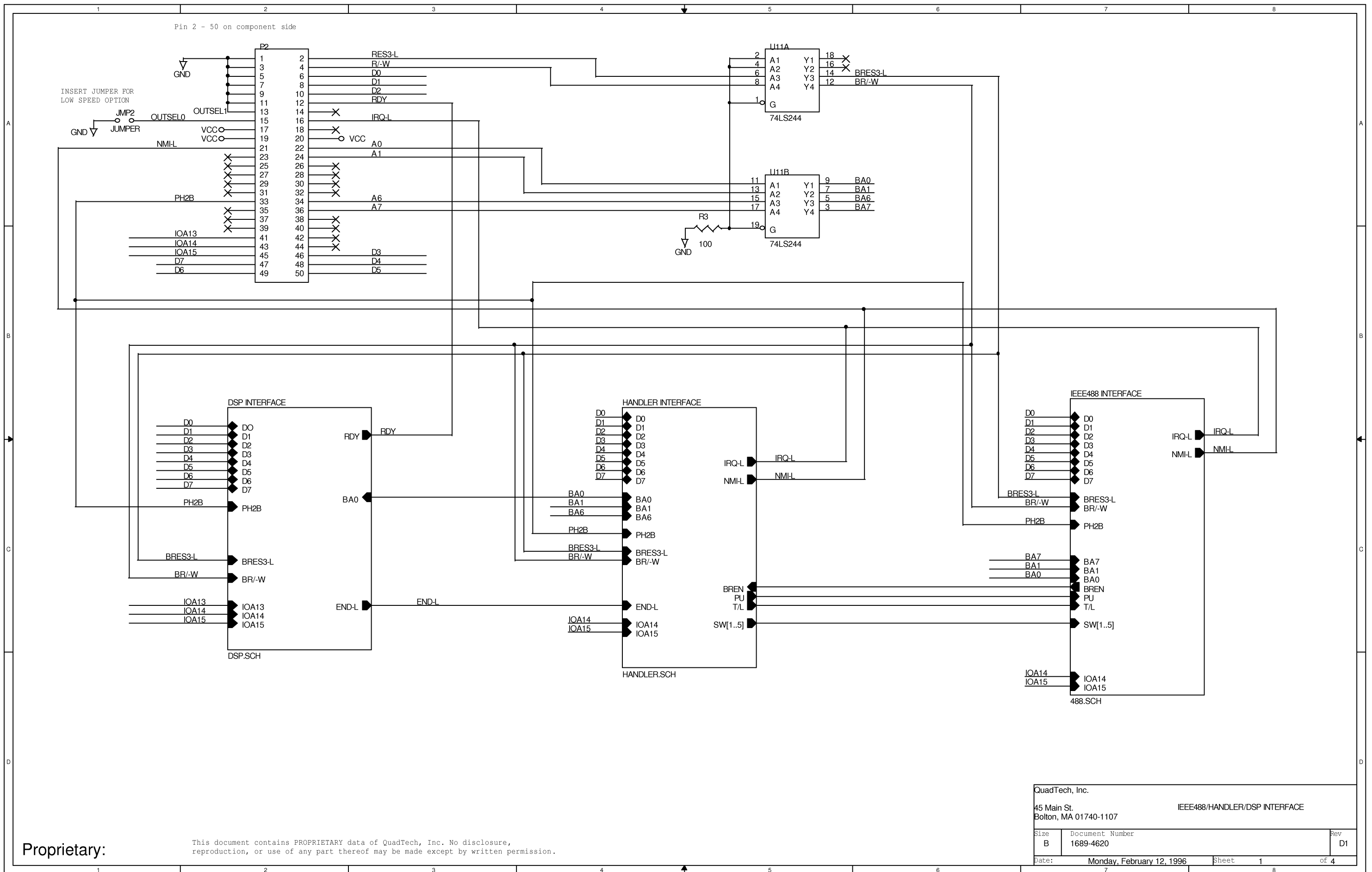


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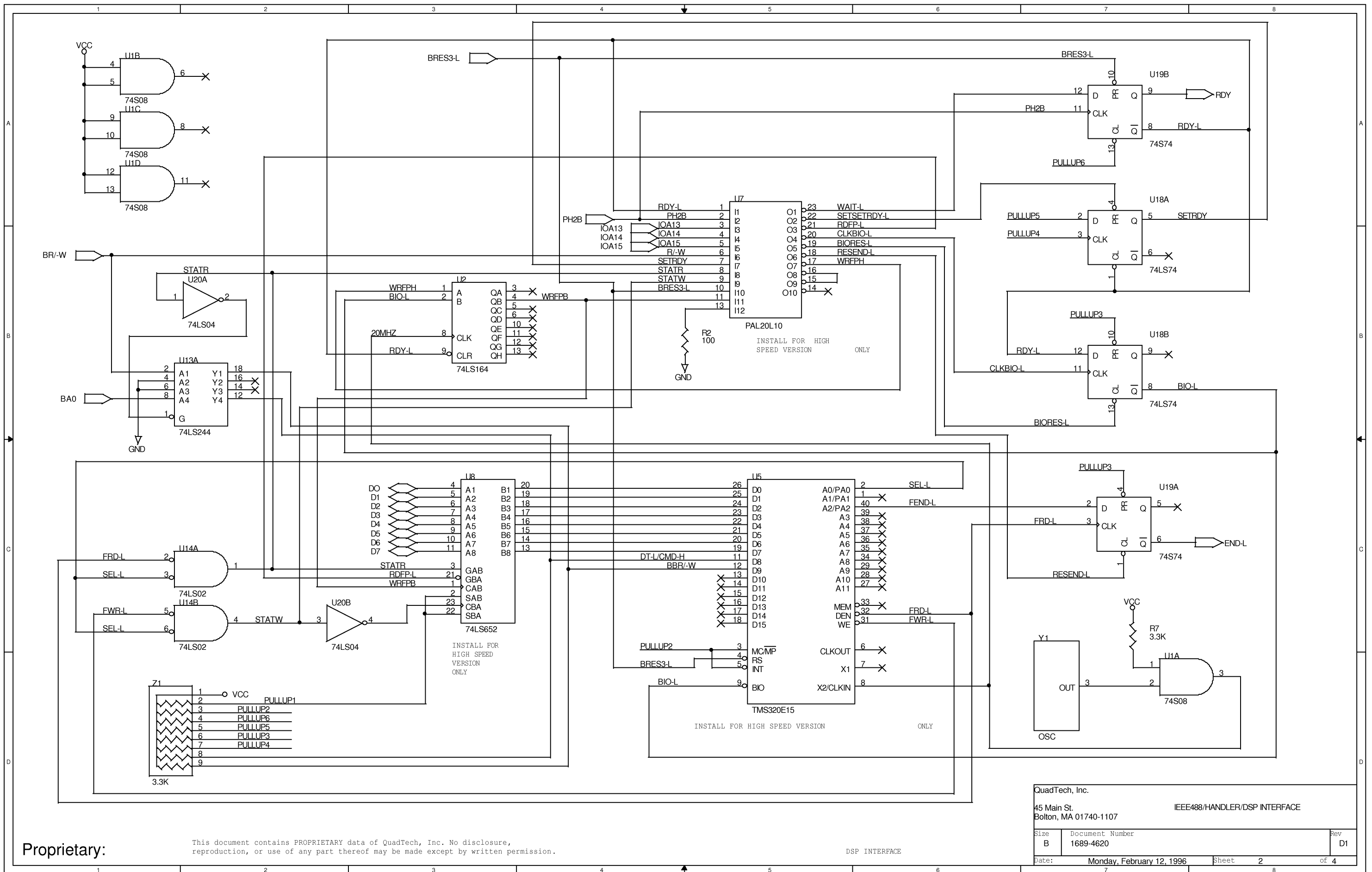
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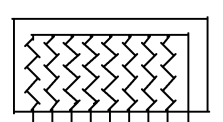
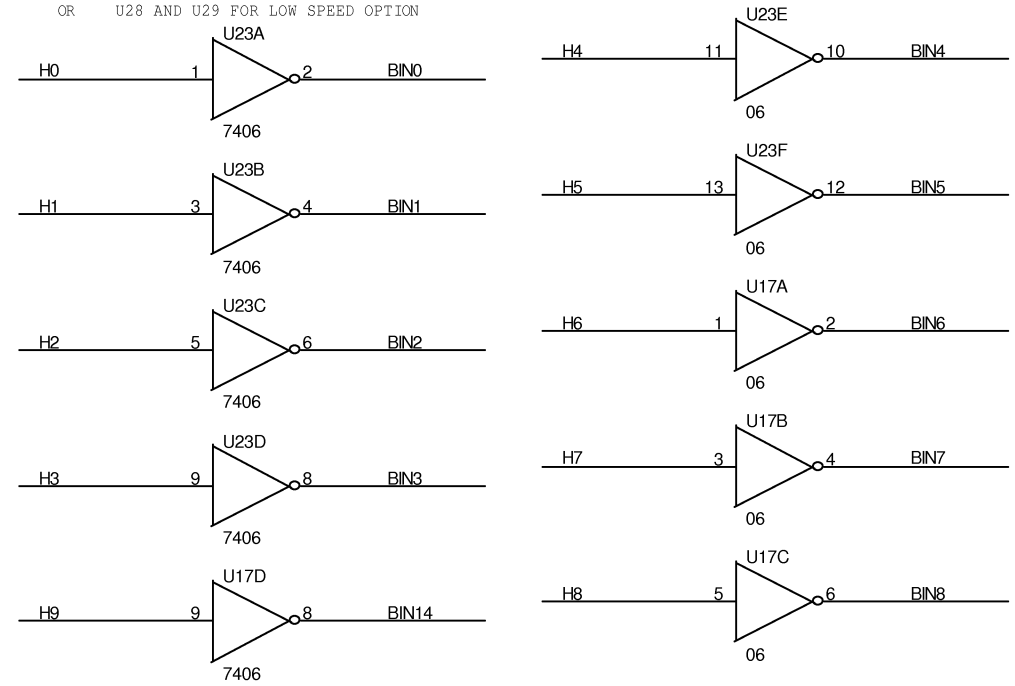
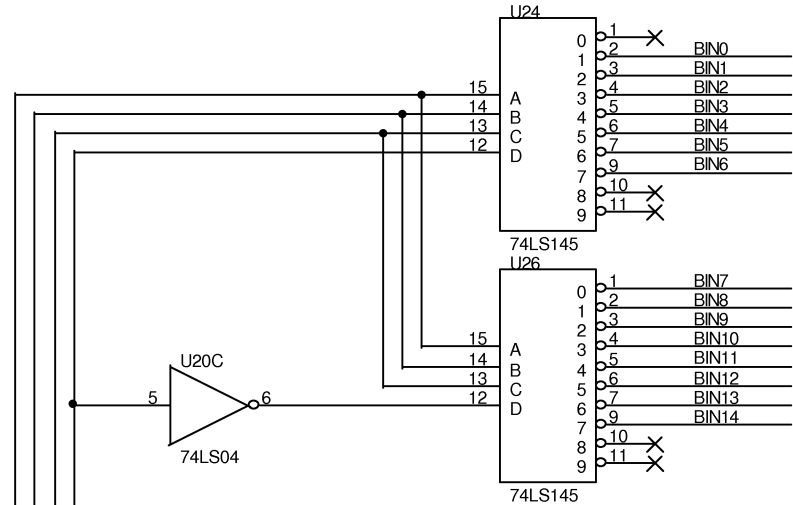
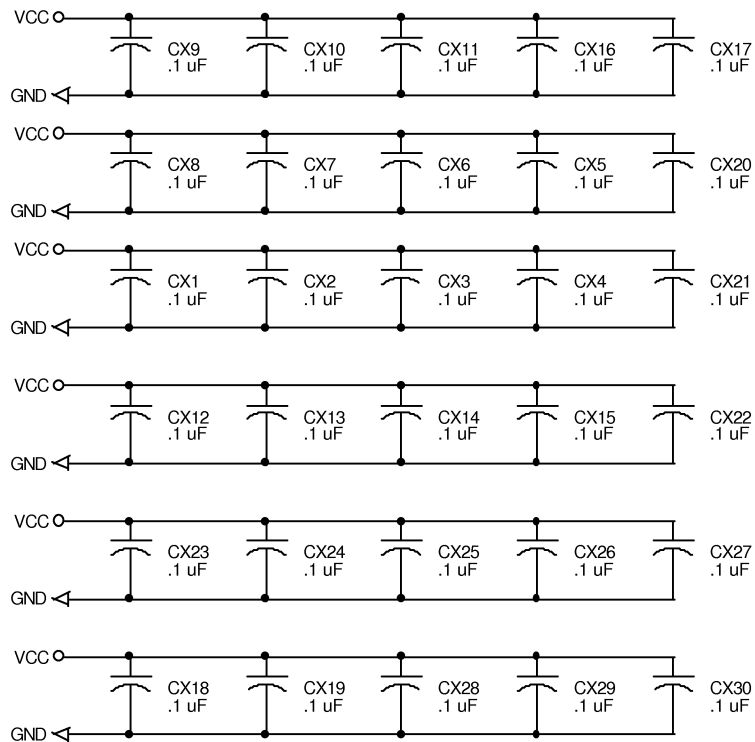
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DSP INTERFACE

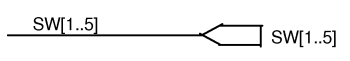
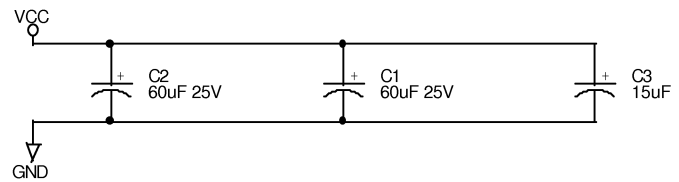
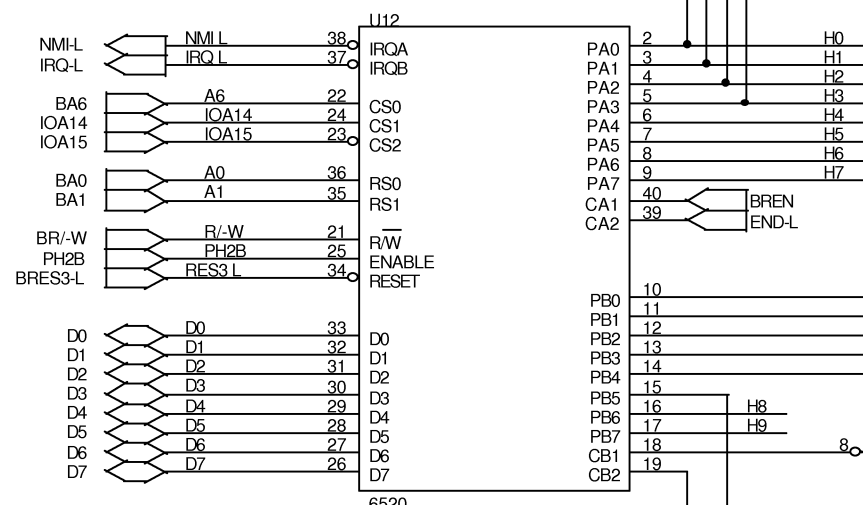
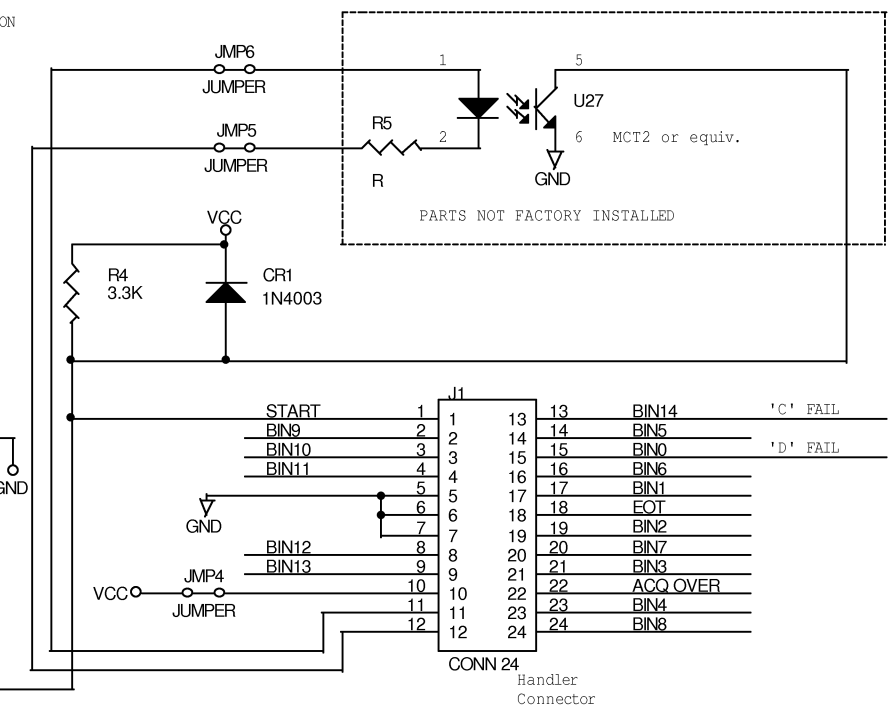
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INSTALL U21 AND U22 FOR HIGH SPEED OPTION

OR U28 AND U29 FOR LOW SPEED OPTION



JUMPER JP3 and JP4 FOR OPTIONAL OPTO ISOLATION Not Factory installed



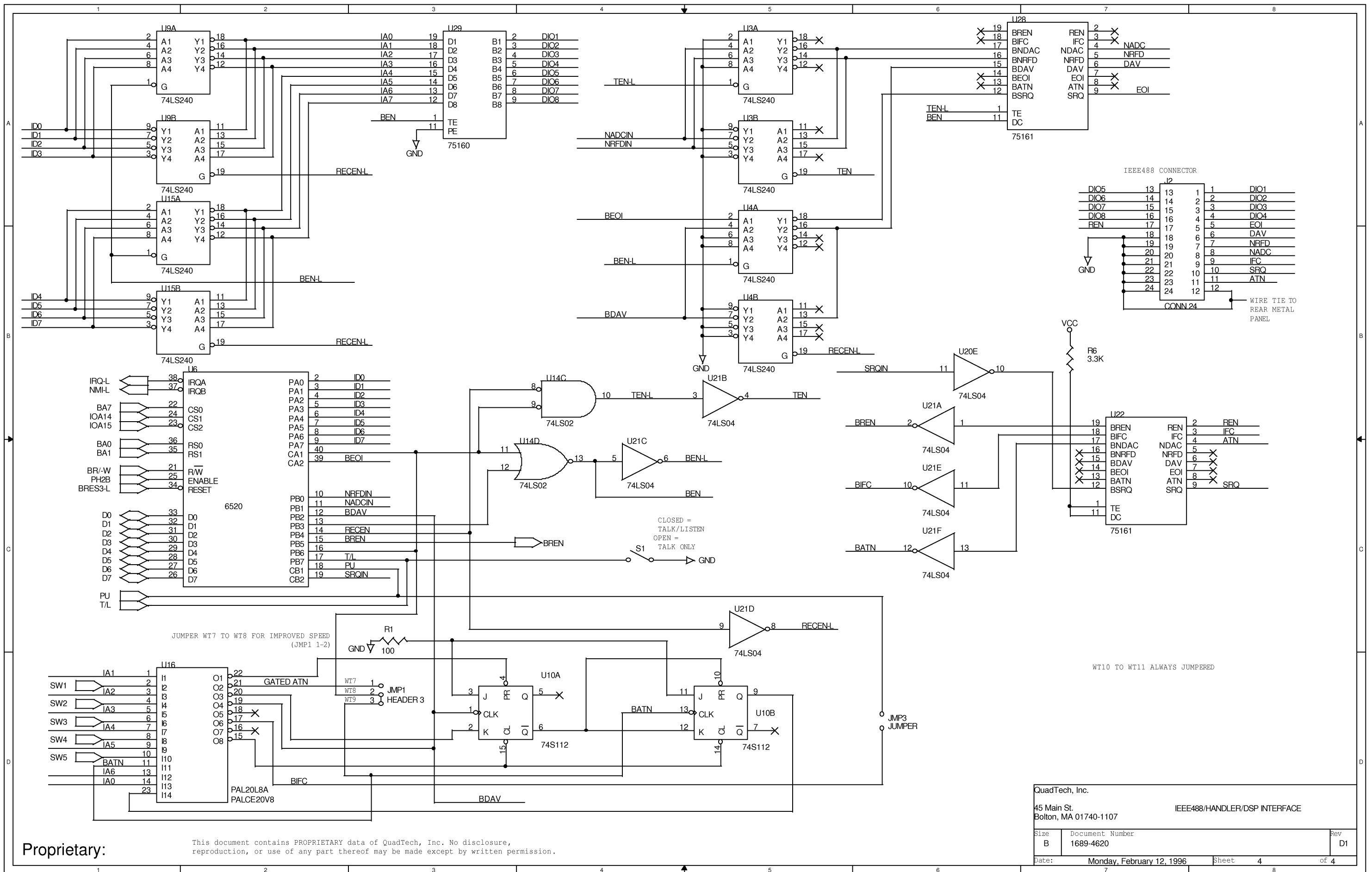
FACTORY SETTINGS
SW1, SW2 OPEN
SW3, SW4, SW5 CLOSED

HANDLER INTERFACE

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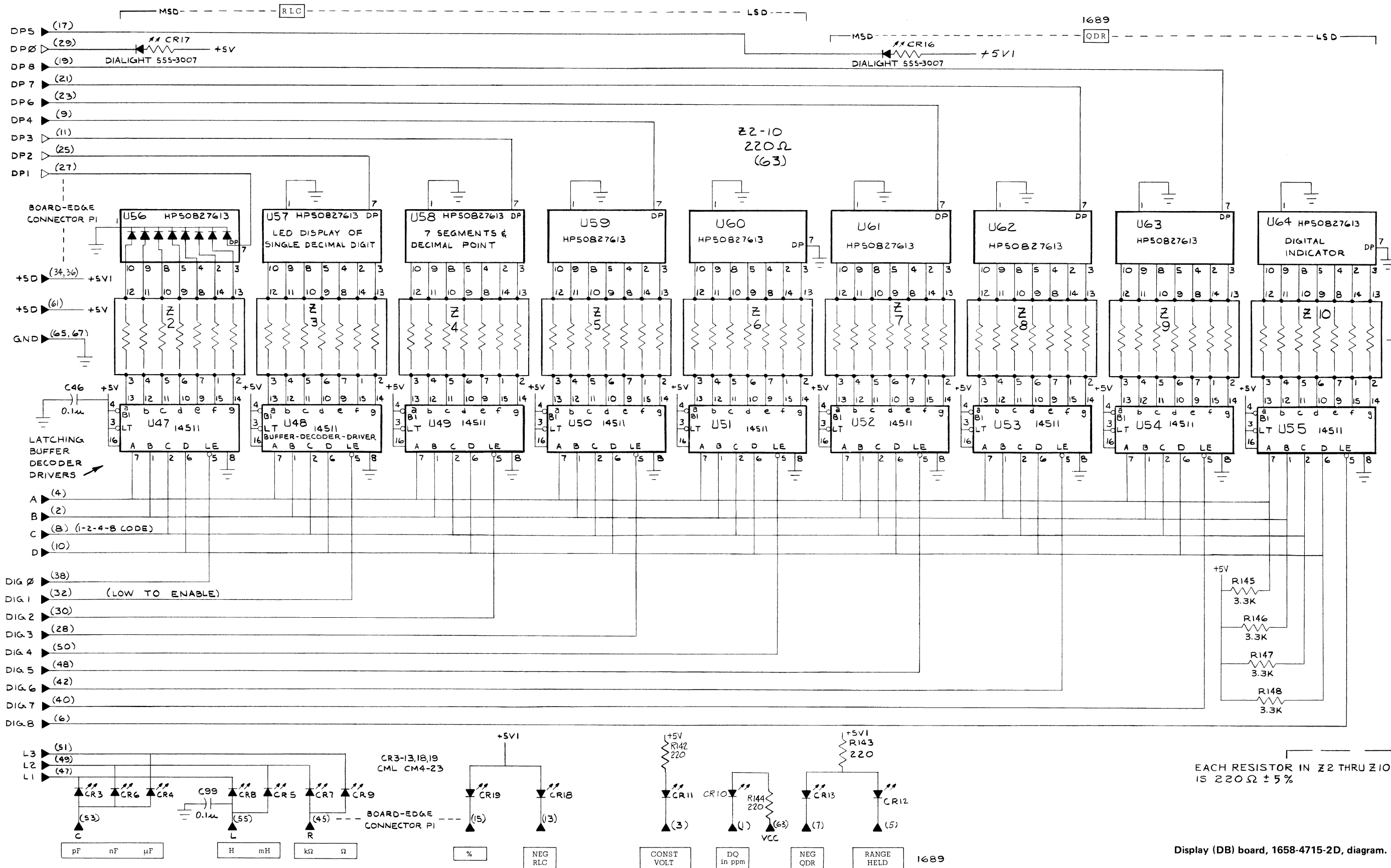


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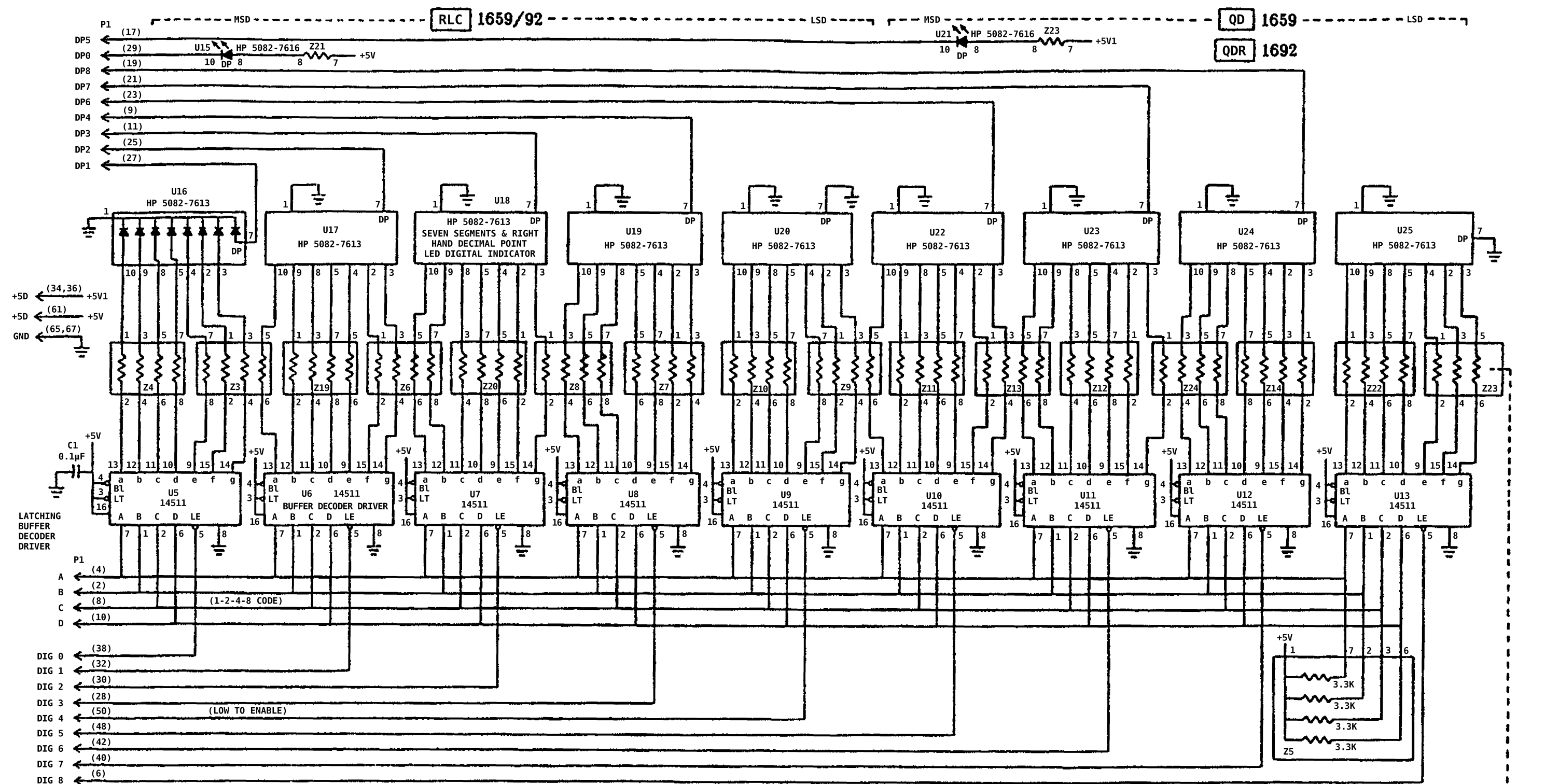
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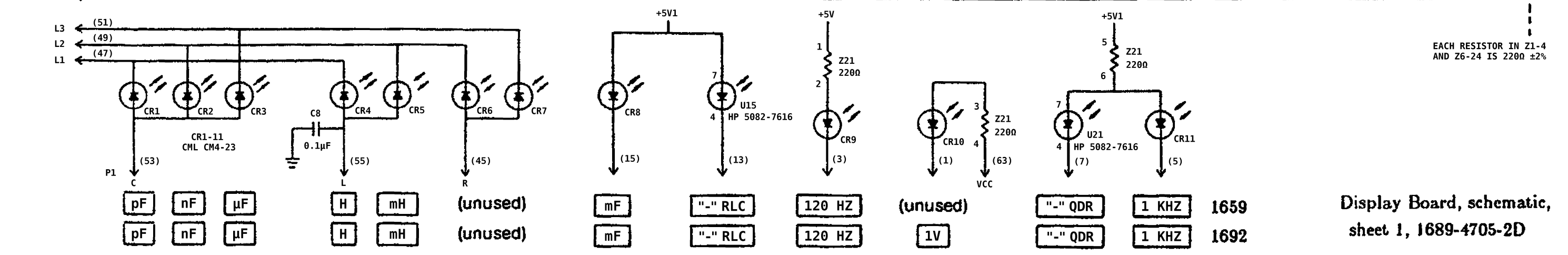


EACH RESISTOR IN Z2 THRU Z10 IS 220Ω ± 5%

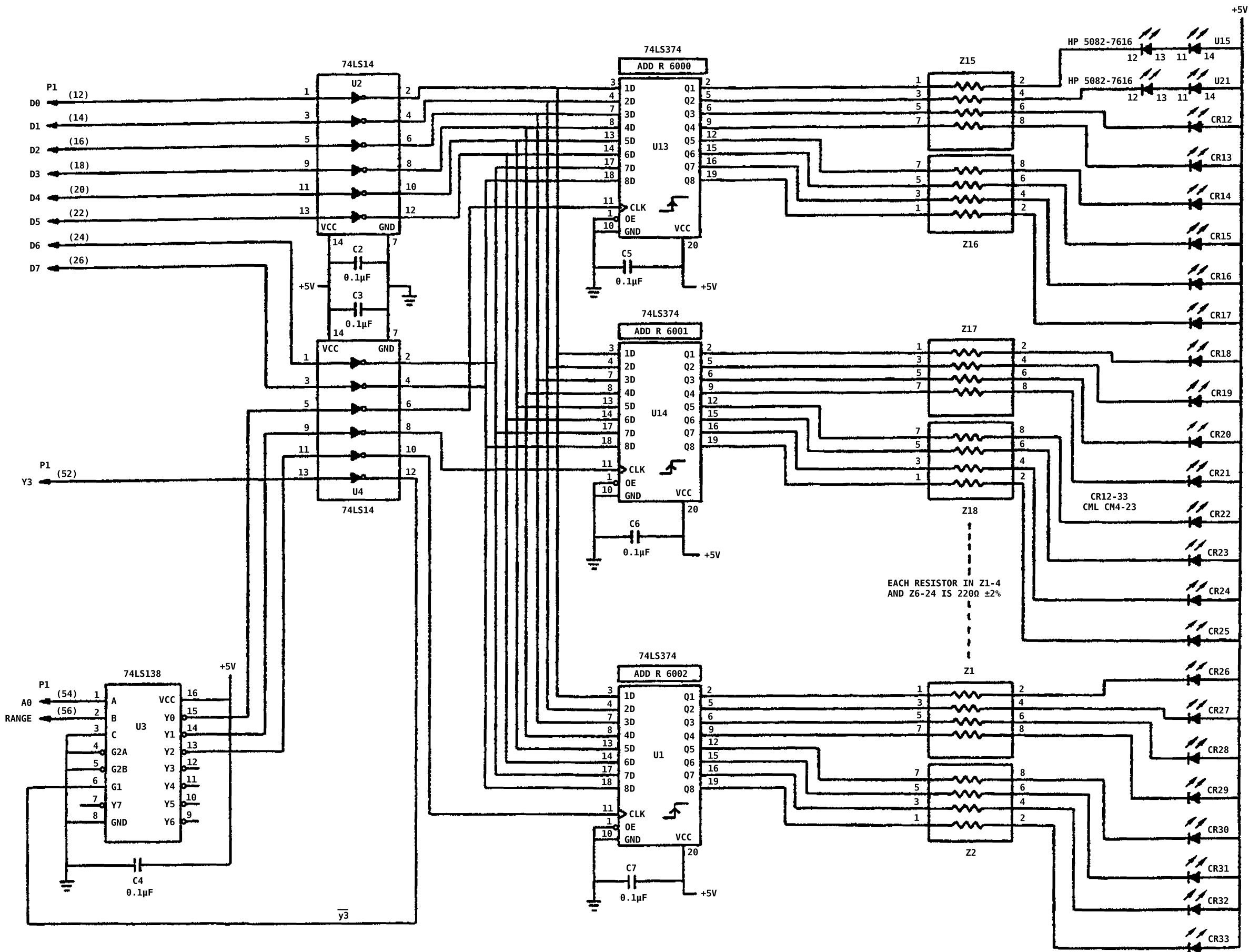
Display (DB) board, 1658-4715-2D, diagram.



EACH RESISTOR IN Z1-4 AND Z6-24 IS 220Ω ±2%

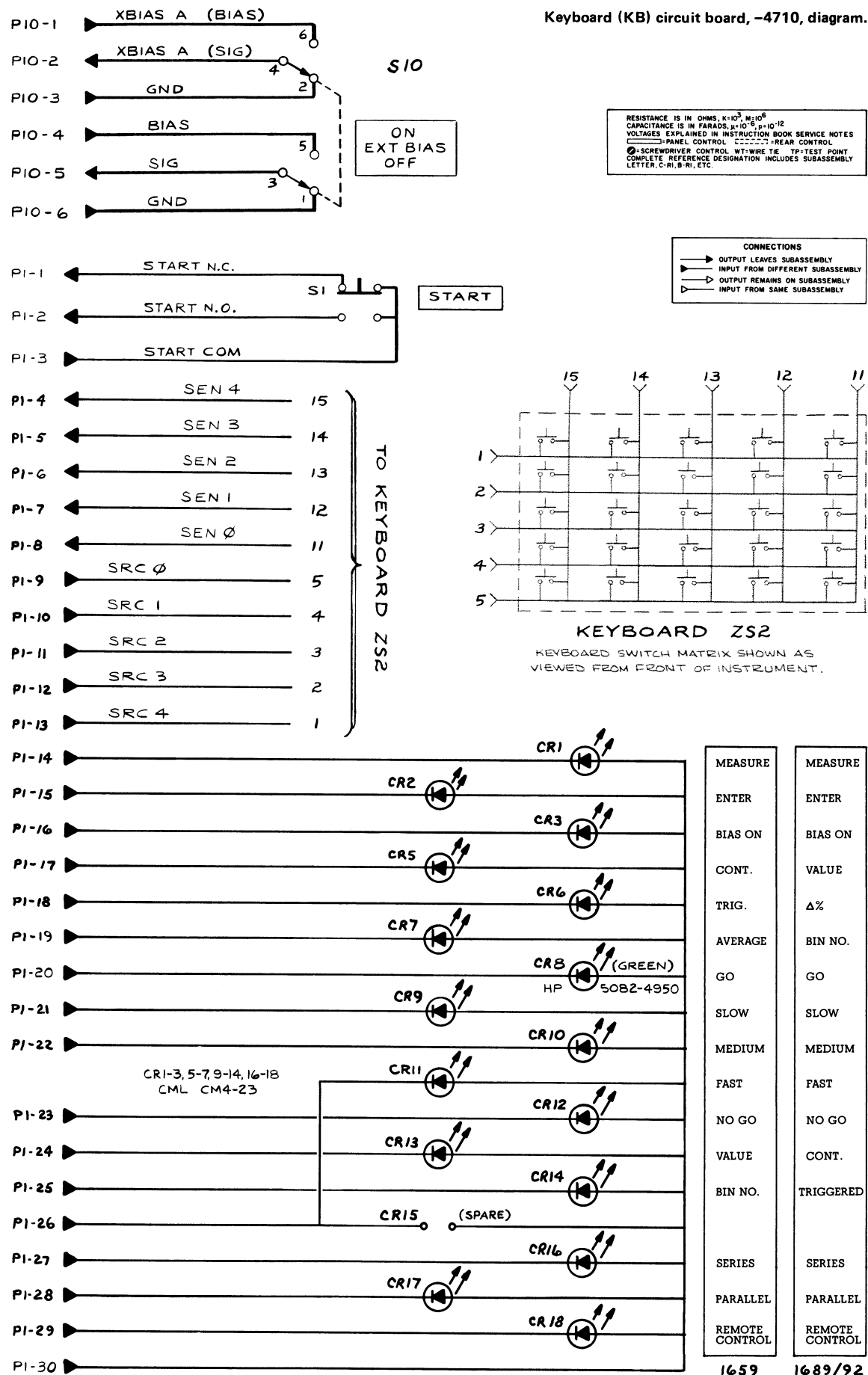


Display Board, schematic, sheet 1, 1689-4705-2D

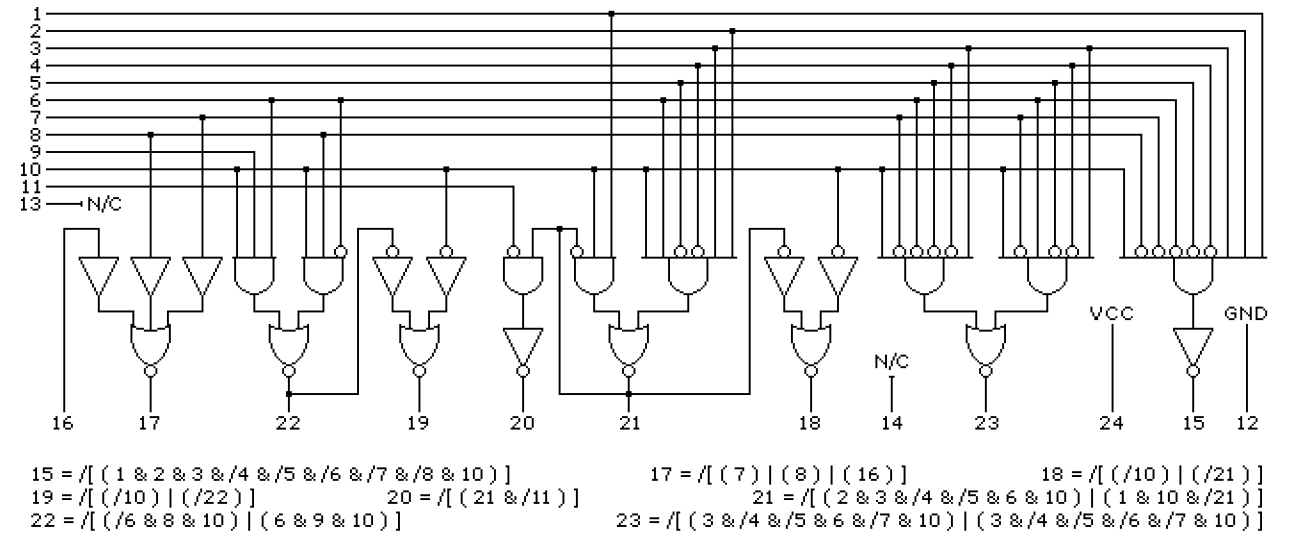


1659	1692
"1" (for RLC)	"1" (for RLC)
"1" (for DQR)	"1" (for DQR)
Ω	Ω
kΩ	kΩ
MΩ	MΩ
(not used)	CONST
(not used)	.3V
(not used)	100 KHZ
10 KHZ	10 KHZ
100 HZ	100 HZ
(not used)	Δ
BIN	BIN
(not used)	%
R	R
L	L
C	C
(not used)	(not used)
(not used)	(not used)
(not used)	(not used)
D	D
Q	Q
(not used)	R
RANGE HELD	RANGE HELD
(not used)	(not used)

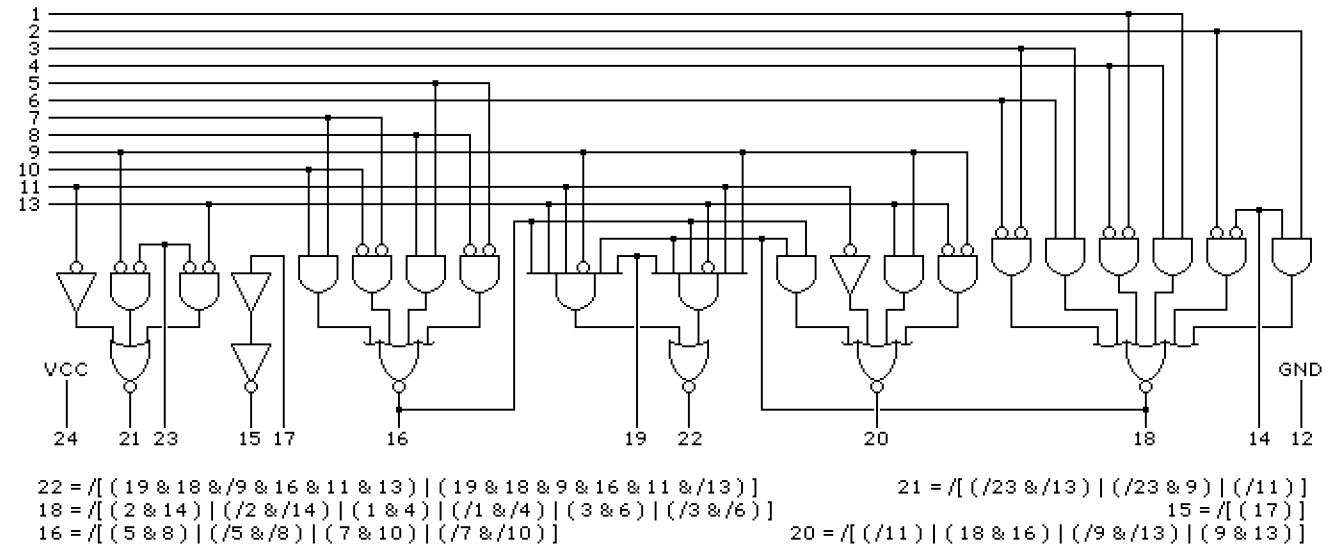
Display Board, schematic, sheet 2, 1689-4705-2D



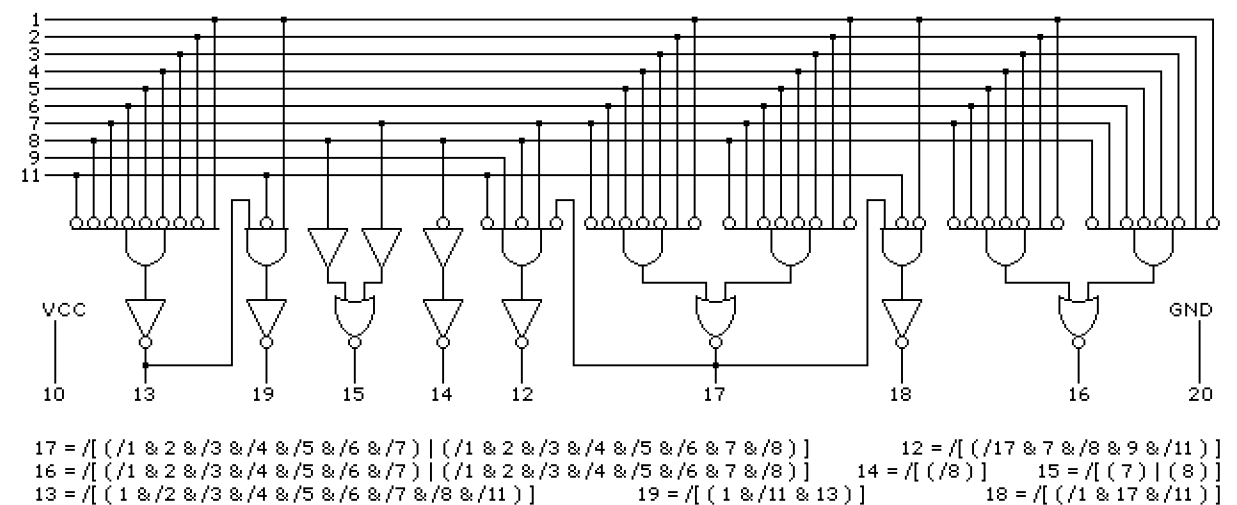
INTERNAL LOGIC AND BOOLEAN EQUATIONS OF PAL20L10 INTEGRATED CIRCUIT U7 IN THE 16XX DIGIBRIDGE

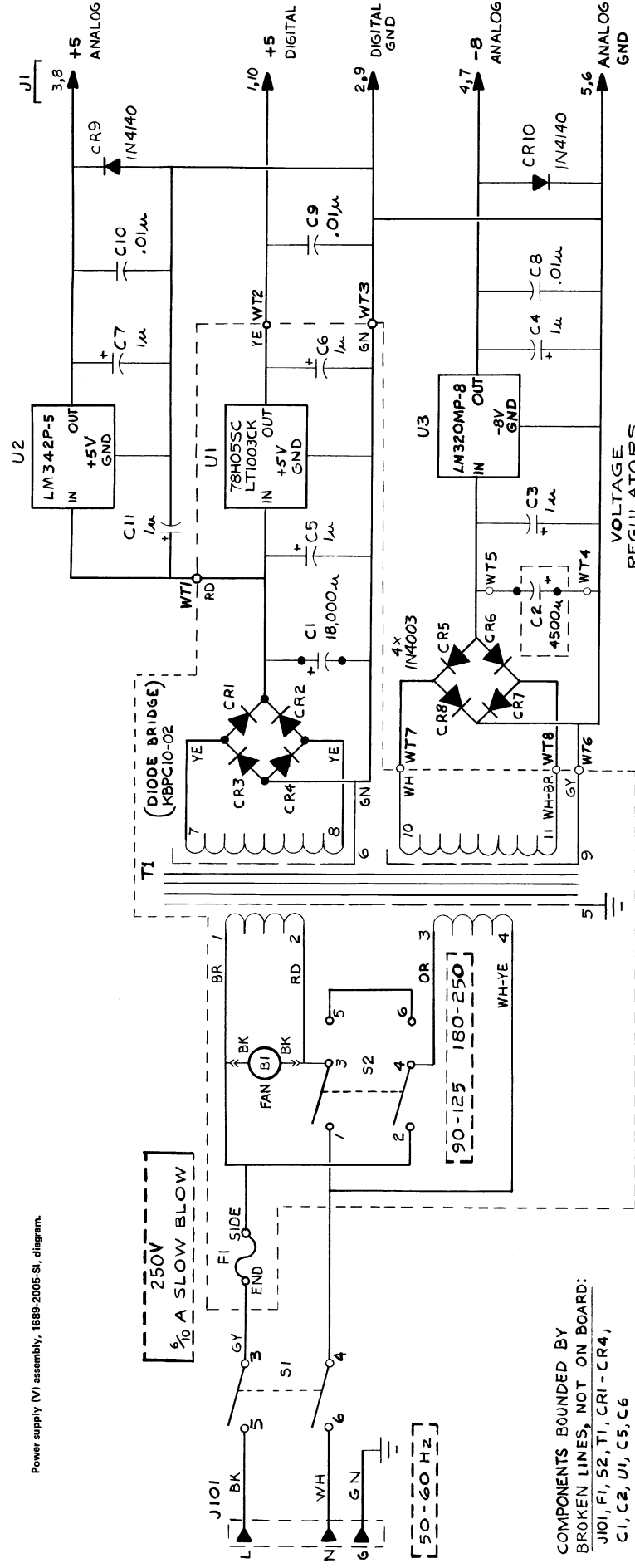


INTERNAL LOGIC AND BOOLEAN EQUATIONS OF PAL20L8A(20V8) INTEGRATED CIRCUIT U16 IN THE 16XX DIGIBRIDGE

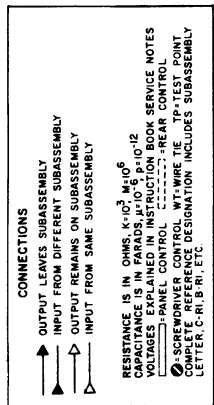
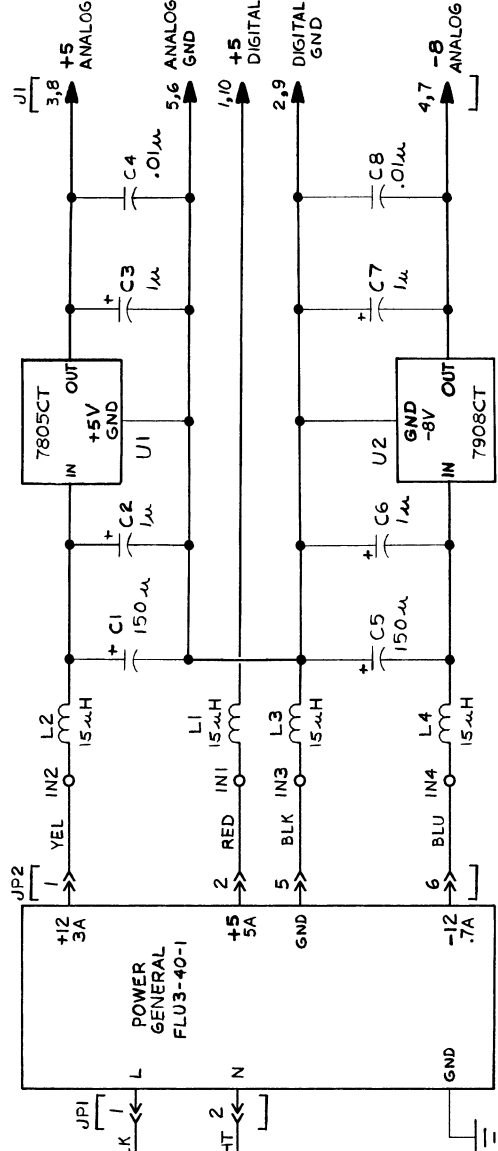
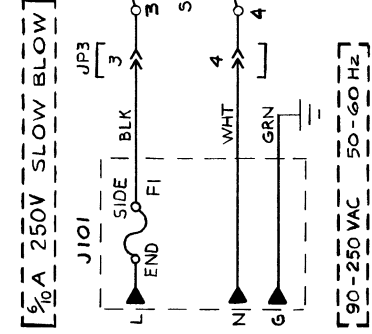
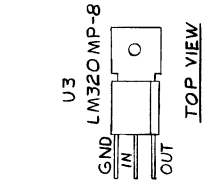
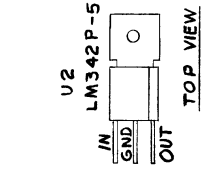
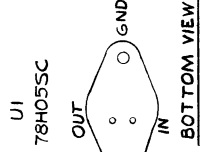
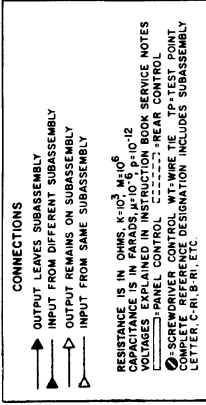


INTERNAL LOGIC AND BOOLEAN EQUATIONS OF PAL16L8 INTEGRATED CIRCUIT U28 IN THE 16XX DIGIBRIDGE





COMPONENTS BOUNDED BY
BROKEN LINES, NOT ON BOARD:
J101, F1, S2, T1, CR1 - CR4,
C1, C2, U1, C5, C6



VOLTAGE REGULATORS

CONNECTIONS
 ▲ OUTPUT LEAVES SUBASSEMBLY
 ◀ INPUT FROM DIFFERENT SUBASSEMBLY
 ▷ INPUT REMAINS ON SUBASSEMBLY
 ◁ INPUT FROM SAME SUBASSEMBLY

RESISTANCE IS IN OHMS, $K=10^3$, $M=10^6$
 CAPACITANCE IS IN FARADS, $\mu=10^{-6}$, $p=10^{-12}$
 VOLTAGES ARE IN VOLTS, UNLESS OTHERWISE NOTED
 VOLTAGES EXPLAINED IN INSTRUCTION BOOK SERVICE NOTES
 ○ SCREWDRIVER CONTROL WIRE TIE-TP-TEST POINT
 ⊕ SCREWDRIVER CONTROL WIRE TIE-TP-TEST POINT
 * SCREWDRIVER CONTROL WIRE TIE-TP-TEST POINT
 COMPLETE REFERENCE DESIGNATION INCLUDES SUBASSEMBLY
 LETTER, C-R, B-R, ETC.