OPERATING INSTRUCTIONS

Peter Di Muro

# TYPE 1391-B

# PULSE, SWEEP, AND TIME-DELAY GENERATOR

1391-B

GENERAL RADIO COMPANY

937-D

OPERATING INSTRUCTIONS

# TYPE 1391-B

# PULSE, SWEEP, AND TIME-DELAY GENERATOR

Form 937-D
May, 1960

GENERAL RADIO COMPANY
WEST CONCORD, MASSACHUSETTS, USA

## TABLE OF VOLTAGES AND RESISTANCES (Cont.)

| TUBE (TYPE) | PIN | DC VOLTS TO GND | RES TO GND |
|---|---|---|---|
| V502 (12AX7) | 1 | 40 | 280k |
| | 2 | -24 | 210k |
| | 3 | -23 | 330k |
| | 6 | 55 | 280k |
| | 7 | -24 | 210k |
| | 8 | -23 | 330k |
| V503 (6AV5GA) | 1 | 40 | 180k |
| | 3 | 55 | 750 |
| | 5 | 145 | 600 |
| | 8 | 120 | 6.8k |
| V504 (6AV5GA) | 1 | 55 | 180k |
| | 3 | 55 | 750 |
| | 5 | 105 | 600 |
| | 8 | 120 | 6.8k |
| V505 (6AV5GA) | 1 | -195 | 620k |
| | 3 | -195 | 51 |
| | 5 | -175 | 840 |
| | 8 | -90 | 5k |
| V506 (6AV5GA) | 1 | -235 | 620k |
| | 3 | -195 | 51 |
| | 5 | -155 | 840 |
| | 8 | -75 | 5k |
| V507 (6550) | 3 | 0 | 150 |
| | 4 | 26 | 25k |
| | 5 | -175 | 890 |
| | 8 | -155 | 600 |
| V508 (6550) | 3 | -26 | 150 |
| | 4 | 26 | 25k |
| | 5 | -155 | 890 |
| | 8 | -155 | 600 |

| TUBE (TYPE) | PIN | DC VOLTS TO GND | RES TO GND |
|---|---|---|---|
| V509 (12AX7) | 1 | -190 | 620k |
| | 2 | -315 | 280k |
| | 3 | -315 | 135k |
| | 6 | -230 | 620k |
| | 7 | -315 | 280k |
| | 8 | -315 | 135k |
| V510 (OA2) | 1 | -170 | 51 |
| | 4 | -340 | 11.9k |
| | 5 | -190 | 51 |
| | 7 | -340 | 11.9k |
| V511 (12BH7) | 1 | 145 | 100 |
| | 2 | -13 | 1.1M |
| | 3 | -7 | 25k |
| | 6 | 145 | 0 |
| | 7 | -13 | 1.1M |
| | 8 | -7 | 25k |
| V601 (6AS7G) | 1 | 225 | 180k |
| | 2 | 455 | 450 |
| | 3 | 300 | 0 |
| | 4 | 225 | 180k |
| | 5 | 455 | 450 |
| | 6 | 300 | 0 |
| V602 (6AK5) | 1 | 145 | 43k |
| | 2 | 145 | 15k |
| | 5 | 225 | 180k |
| | 6 | 250 | 5.1k |
| | 7 | 145 | 15k |
| V603 (OD3) | 2 | 0 | 0 |
| | 5 | 145 | 15k |

| | TERMINAL | AC VOLTS | RES TO GND |
|---|---|---|---|
| POWER XFMR T601 | 1-2 | 115 | |
| | 3-4 | 115 | |
| | 30-31 | 6.7 | |
| | 12-23 | 6.7 | |
| | 9-13 | 6.8 | |
| | 25-26 | 6.7 | |
| | 32-33 | 6.7 | |
| | 10-11 | 70 | |
| | 7-8 | 140 | |
| | 6-16 | 140 | |
| | 27-28 | 100 | |
| | 17-18 | 300 | |
| PL101 | 3 | | ∞ |
| | 4 | | ∞ |
| | 5 | 75 | >50k |
| | 6 | 75 | >50k |
| | 7 | | 50 |
| | 8 | | 50 |
| | 9 | | 50 |
| | 10 | | 50 |
| | 11 | -150 | >10k |
| | 12 | -150 | >10k |
| T201 | 3-5 | | 5 |
| | 2-6 | | 5 |
| | 1-7 | | 5 |

CHANGE NOTICE
for
Operating Instructions for the
Type 1391-B Pulse, Sweep, and Time-Delay Generator
(Form 937-D)

Please make the following corrections in your manual:

page 2, paragraph 1.2.4, line 2: Delete "(30, Figure 1.1)"

page 2, paragraph 1.2.4, line 4: Delete "(31)."

page 10, paragraph 2.6j, line 2: change "SWEEP POS" to read "SWEEP NEG."

pages 28, 29: Substitute new Table of Voltages and Resistances.

pages 32 et seq: Note the following Parts List changes:

All Type COC-63 capacitors are changed to Type COC-62.

GENERAL RADIO COMPANY
West Concord, Massachusetts

October, 1960 Printed in USA

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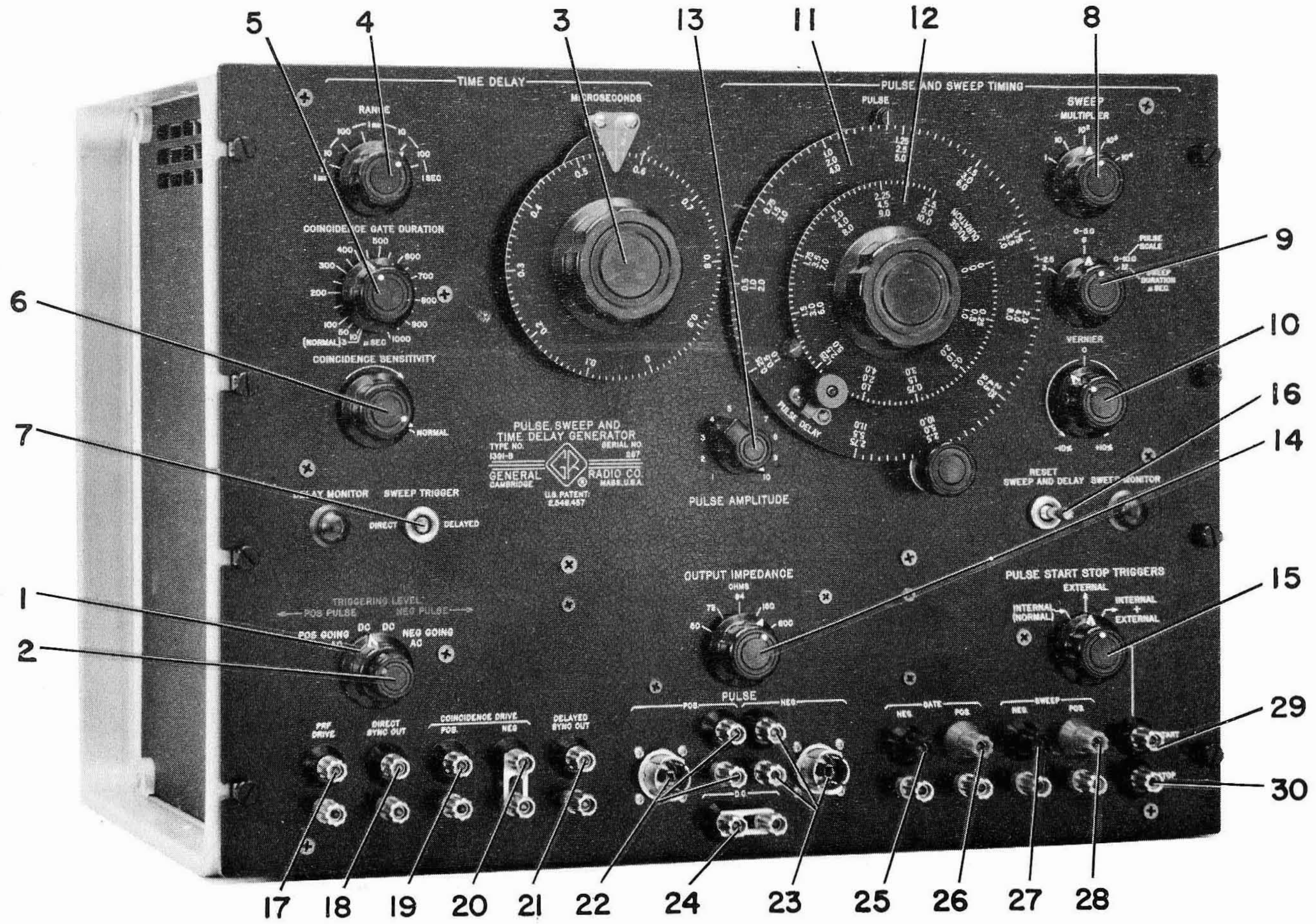


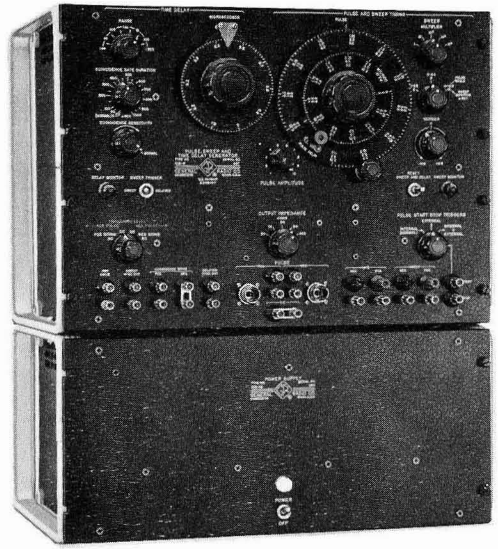



Figure 1.1.
Type 1391-B Pulse, Sweep, and Time-Delay Generator.

# TYPE 1391-B
# PULSE, SWEEP, AND TIME-DELAY GENERATOR

## Section 1 INTRODUCTION

**1.1 PURPOSE.** The Type 1391-B Pulse, Sweep, and Time-Delay Generator (Figure 1.1) is a versatile laboratory instrument designed to generate (1) push-pull pulses, of durations from 0.025 $\mu$sec to 1.1 sec and at repetition rates up to 250 kc; (2) linear sweep voltages of durations from 3 $\mu$sec to 0.12 sec; (3) time delays from 1 $\mu$sec to 1.1 sec; and (4) direct and delayed trigger pulses, which can be used independently or to delay the initiation time of the sweep and main pulse relative to the input driving signal. Transition times of the output pulses (0.015 $\mu$sec rise time) are compatible with most present-day oscilloscopes. The internal sweep circuit makes possible the use of an inexpensive oscilloscope by direct connection to the deflection plates.

**1.2 DESCRIPTION.**

1.2.1 GENERAL. The Type 1391-B is available in either relay-rack or bench mounting, and is housed in two units. The upper unit shown in Figure 1.1 is the generator itself, with all operating controls at the front panel. Below this unit is the power supply, with the main POWER switch and pilot light.

1.2.2 CONTROLS. The following table lists the controls on the front panel of the Type 1391-B Pulse, Sweep, and Time-Delay Generator (index numbers refer to Figure 1.1):

| No. | Name | Type | Function |
|---|---|---|---|
| 1 | TRIGGER SELECTOR | 4-pos selector switch | Selects direction of input-signal zero-crossing to produce direct synchronizing signal, and provides for ac or dc coupling of input signal. |
| 2 | TRIGGERING LEVEL | Concentric rotary control | Sets dc level at which input circuits trigger. |
| | TIME DELAY | | |
| 3 | MICROSECONDS | Continuous rotary control | Determines interval between delayed and direct synchronizing |
| 4 | RANGE | 6-pos selector switch | pulses over the range from 1 $\mu$sec to 1.1 sec. |
| 5 | COINCIDENCE GATE DURATION | Continuous rotary control | Determines duration of coincidence gate from 3 to 1000 $\mu$sec. |
| 6 | COINCIDENCE SENSITIVITY | Continuous rotary control | Selects threshold at which coincidence driving signals will produce delayed sync signals. |
| 7 | SWEEP TRIGGER | 2-pos toggle switch | Selects either direct or delayed sync signal to start sweep. |
| | PULSE AND SWEEP TIMING | | |
| 8 | SWEEP MULTIPLIER | 5-pos selector switch | Determine sweep duration from 3 to 120,000 $\mu$sec in decimal |
| 9 | Sweep Duration Selector | 3-pos selector switch | multiples of 3, 6, and 12 $\mu$sec. |
| 10 | VERNIER | Continuous rotary control | Adjusts sweep duration by ±10% from nominal value. |
| 11 | PULSE DELAY | 6-in. rotary control and dial | Sets duration of pulse. |
| 12 | PULSE DURATION | 4-in. rotary control and dial | Sets pulse duration. |
| 13 | PULSE AMPLITUDE | 10-position selector switch | Sets pulse amplitude. |
| 14 | OUTPUT IMPEDANCE | 5-pos selector switch | Selects any one of five load resistances for pulse current source. |
| 15 | PULSE START STOP TRIGGERS | 3-pos selector switch | Routes internally produced or externally applied triggering signals to determine pulse duration. |
| 16 | RESET SWEEP AND DELAY | 2-pos spring-return toggle switch | Provides artificial reset pulse to restore sweep and delay circuit action. |

**DEFINITIONS:** Terms used in this manual are defined as follows: DRIVES are input signals used to synchronize the generator with external sources. SYNCHRONIZING signals are output signals from the generator, used to synchronize the external system to the generator. TRIGGERS are signals circulating within the instrument to synchronize the various internal circuits. PULSE is generally the main output pulse; other rectangular waves generated within instrument are called gates to distinguish them from the main pulse. Timing signals produced by the delay circuit and occurring at a time indicated by the delay control settings are called DELAYED. Timing signals occurring after start of sweep by a time indicated by PULSE DELAY setting are called START signals, while those occurring after START by a time indicated by the PULSE DURATION setting are called STOP signals.

1.2.3 TERMINALS. The following terminals are on the front panel of the Type 1391-B Pulse, Sweep, and Time-Delay Generator (index numbers refer to Figure 1.1):

| No. | Name | Type | Function |
|---|---|---|---|
| 17 | PRF DRIVE | Binding post pair | To external prf-determining signal source. |
| 18 | DIRECT SYNC OUT | Binding post pair | To external device to be synchronized by direct pulse. |
| | COINCIDENCE DRIVE | | |
| 19 | POS | Binding post pair | Positive or negative pulses to coincidence circuits. |
| 20 | NEG | Binding post pair | |
| 21 | DELAYED SYNC OUT | Binding post pair | To external device to be synchronized after delay interval. |
| | PULSE | | |
| 22 | POS | Binding post pair and coaxial connector | Positive pulse output. |
| 23 | NEG | Binding post pair and coaxial connector | Negative pulse output. |
| 24 | D-C | Binding post pair | Upon removal of link, permits insertion of d-c voltage to adjust pulse d-c component. |
| | GATE | | |
| 25 | NEG | Binding post pair | Output of pulses occurring simultaneously with sweep. |
| 26 | POS | Binding post pair | |
| | SWEEP | | |
| 27 | NEG | Binding post pair | Output of sawtooth signals of duration determined by SWEEP controls. |
| 28 | POS | Binding post pair | |
| 29 | START | Binding post pair | Terminals at which are available internally generated pulse-timing triggers or to which are applied external triggers to time pulse, depending on setting of PULSE START STOP TRIGGERS switch. |
| 30 | STOP | Binding post pair | |

1.2.4 INDICATOR LAMPS. Also on the front panel are the DELAY MONITOR lamp (30, Figure 1.1), which indicates the presence of delayed synchronizing pulses at the DELAYED SYNC OUT terminals, and the SWEEP MONITOR lamp (31), which indicates the presence of the sweep signal at the SWEEP output terminals.

1.2.5 BASIC CIRCUITS.

1.2.5.1 Input Circuits. The input circuits produce direct trigger signals and direct synchronizing signals from an input drive signal. By means of the TRIGGER SELECTOR switch, either a positive- or negative-going zero crossing of the input signal can be selected to produce the direct trigger and the accompanying direct synchronizing signal, available at the DIRECT SYNC OUT terminals. This switch also provides for ac or dc connection of the input signal to the trigger circuits.

1.2.5.2 Delay Circuits. The delay circuits produce delayed triggers and delayed synchronizing signals whose time of occurrence relative to the direct trigger is controlled by the DELAY MICROSECONDS and RANGE controls over a total range of 1 $\mu$sec to 1.1 seconds. The coincidence system, consisting of a monostable coincidence-gate circuit and a gating amplifier of adjustable sensitivity, is not used in "normal" operation (i.e., with the COINCIDENCE GATE DURATION and COINCIDENCE SENSITIVITY controls at NORMAL settings). When the coincidence system is used, two inputs are required to produce the delayed synchronizing signal. The first operates the delay circuits through the input circuit PRF DRIVE terminals to open the coincidence gate; the second, a brief pulse fed into the COINCIDENCE DRIVE terminals, will cause the formation of the delayed trigger and synchronizing signal only when the gate is open.

1.2.5.3 Sweep Circuit. The sweep circuits are started by either the direct or the delayed trigger, depending on the position of the SWEEP TRIGGER switch. These circuits produce (1) a linearly rising waveform that attains an amplitude of 135 volts in 3, 6, or 12 $\mu$sec or decimal multiples thereof up to a maximum time of 120,000 $\mu$sec, and (2) a gate signal with the same duration as the sweep. There are three controls for the sweep circuit: the 3, 6, or 12-$\mu$sec switch, a SWEEP MULTIPLIER, and a VERNIER, affording about $\pm$10-percent variation of the sweep duration. Outputs from the sweep circuits are SWEEP, positive and negative, and GATE, positive and negative.

1.2.5.4 Pulse-Timing Circuits. These circuits are adjusted by the PULSE DURATION and PULSE DELAY controls, which determine the formation times of the START and STOP triggers relative to the sweep. These triggers are used to start and stop the main pulse.

The pulses produced in the timing circuits are connected through the PULSE START STOP TRIGGERS switch to the

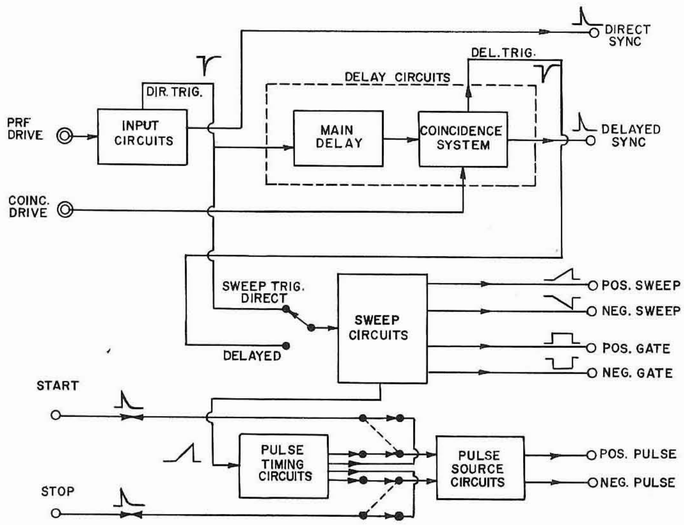



Figure 1.2. System Block Diagram.

pulse-generating circuits. This switch, shown schematically in Figure 1.2, will:

a. when in the INTERNAL (NORMAL) position, start and stop the pulse at the time set on the DURATION and DELAY controls. (In this position, marker pulses corresponding to start and stop times are fed to the START and STOP terminals.)

b. when in the EXTERNAL position, provide for externally generated pulses to start and stop the pulse.

c. when in the INTERNAL + EXTERNAL position, permits the internally produced start and stop triggers to be added to externally generated pulses to start and stop the pulse. Thus the delay circuits and the pulse trigger circuits can be used simultaneously to produce a double pulse.

1.2.5.5 Pulse Source Circuits. These circuits form a bistable system that responds to start and stop triggers generated either internally or externally to produce the push-pull pulse of adjustable amplitude, with an adjustable output impedance.

1.2.6 GENERAL CIRCUIT DESCRIPTIONS.

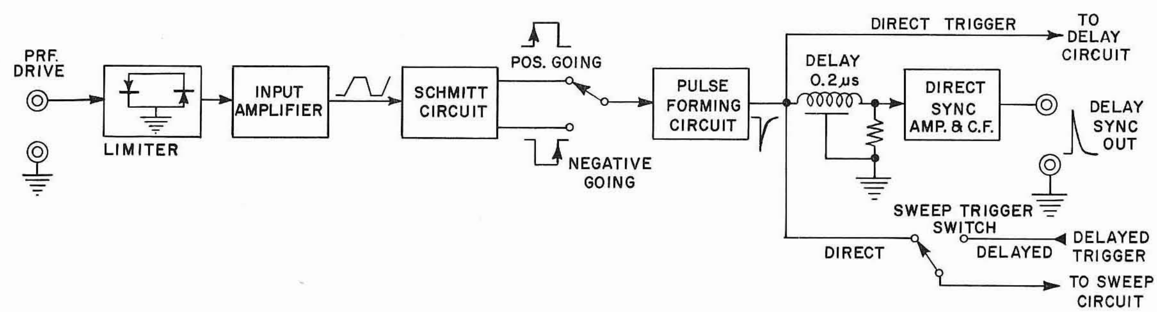
1.2.6.1 Input Circuits. (See Figures 1.3 a, b.) The input circuits consist of an input amplifier, Schmitt circuit, pulse-forming circuit, amplifier, and output cathode follower. The Schmitt circuit is driven by the direct-coupled amplifier, and in turn drives the direct-trigger pulse-forming circuit to produce the direct triggers at prf's to 500 kc. This direct trigger synchronizes the remainder of the circuit groups within the instrument. It can be formed on whichever zero-crossing the user selects. For sine- and square-wave inputs, the trigger-generating system requires about 0.3 volt peak; for brief pulses of either polarity, about 1 volt.

The sweep and delay circuits can be started simultaneously by the direct trigger, or the sweep circuit can be triggered by the delayed trigger. These two modes of operation, selected by the SWEEP TRIGGER switch, either make the delay and sweep circuits completely independent or make use of the delay circuit to delay the sweep with respect to the direct trigger.

The direct synchronizing signal is a 100-volt, 1-$\mu$sec positive pulse fed from a cathode follower to the DIRECT SYNC OUT binding posts on the front panel. Lagging slightly behind the direct trigger, it can be used to synchronize auxiliary equipment such as oscilloscopes and counters. It can also be used to initiate the main pulse when the pulse duration is to be determined by the delay circuit (refer to paragraph 2.8.2).

When the generator is driven by a brief, rapidly rising input pulse, there is a time delay of 0.4 $\mu$sec between this pulse and the direct synchronizing signal. This time delay permits (1)

Figure 1.3a. Block Diagram of Input Circuits.



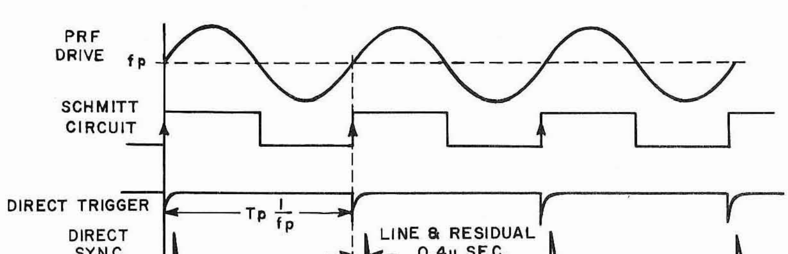




Figure 1.3b. Time Relationships in Input Circuits.

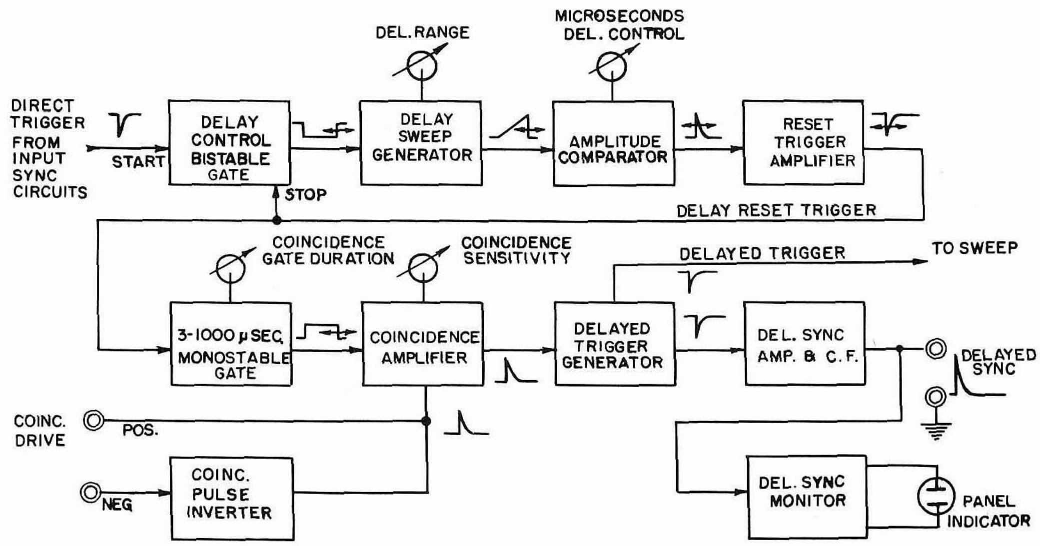



Figure 1.4a. Block Diagram of Delay Circuits.

the establishment of an accurately predetermined minimum delay, and (2) the observation of the direct synchronizing signal on almost any oscilloscope triggered by the input signal.

1.2.6.2 Delay Circuits. (See Figure 1.4a.) The direct trigger starts the delay circuit by opening the bistable gate. The opening of the gate starts a sweep generator, which produces a rising voltage whose slope is determined by an r-c circuit selected by the DELAY RANGE control. The DELAY MICROSECONDS control, a 10-turn potentiometer, provides a voltage reference for an amplitude comparator. When the sweep voltage reaches the level set by the delay control, the amplitude comparator operates a reset trigger generator that closes the bistable gate.

The dial for the 10-turn potentiometer is calibrated linearly in 1000 divisions so that the delay can be read with high incremental resolution. Delay is direct-reading in microseconds, with the basic range from 1 to 11 microseconds. A six-decade range switch selects R-C time constants in the sweep generator to produce multipliers from 1 to $10^5$.

1.2.6.3 Coincidence System. A monostable coincidence gate, adjustable from about 3 to 1000 $\mu$sec, is a part of the delay circuit. The reset trigger produced by the main delay circuit opens this gate 1 $\mu$sec to 1.1 second after the direct trigger. The coincidence gate permits time-selection operations. (See Figures 1.4b, c, and d.)

In normal operation, the opening of the coincidence gate produces the delayed synchronizing signal (Figure 1.4b). However, with reduced sensitivity of the coincidence amplifier, the circuit can no longer be operated by the opening of the coincidence gate alone, and the circuits are prepared for coincidence operation. In this condition, during the intervals in which the gate is open, the injection of a positive or negative pulse at the appropriate COINCIDENCE DRIVE terminals will cause the coincidence amplifier to operate, resulting in the formation of the delayed synchronizing signal and delayed trigger. While the coincidence gate is open, as many delayed synchronizing signals and triggers will be produced as there are driving pulses to the coincidence circuit (Figure 1.4c).

Multiple delayed synchronizing pulses can be produced by means of the delay and coincidence circuits, as shown in Figure 1.4d. The delay circuit can divide the input prf by any number up to about 20, depending on the setting of the delay time controls. Direct synchronizing pulses are fed to the POS COINCIDENCE DRIVE terminal. Any direct synchronizing pulse that exists while the coincidence gate is open will cause a delayed synchronizing pulse to be generated.

1.2.6.4 Sweep Circuit. The sweep circuit (Figure 1.5a), similar in form to the main delay circuit, consists of a bistable gate, a sweep generator and amplitude comparator, and a reset trigger amplifier, which produces the reset signal to close the gate. In this system, however, the sweep generator is a "bootstrap" circuit. It consists of a pentode switching tube, which is turned off by the sweep gate to start the sweep, a cathode follower with a gain of nearly unity, a feedback diode, and a gated clamp circuit to control the initial sweep voltage. The linearly rising voltage waveform in this circuit is fed to the sweep-amplitude-comparator circuit, which switches when the sweep voltage reaches a preset 135 volts to form the reset trigger. In addition, the positive sweep voltage is fed (1) to the pulse-timing circuit, (2) to a cathode follower to provide positive sweep, and (3) through an inverter-cathode-follower to produce the negative sweep. The bistable sweep gate drives a phase-splitter, producing a push-pull waveform at the gate output terminals. The negative sweep at the output terminal drives a stage operating a neon indicator lamp to show that the sweep circuits are operating.

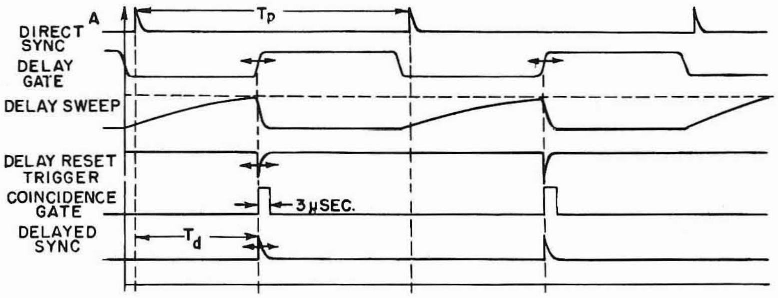



Figure 1.4b.
Delay-Circuit Timing, Coincidence Circuit Set for Normal Operation.

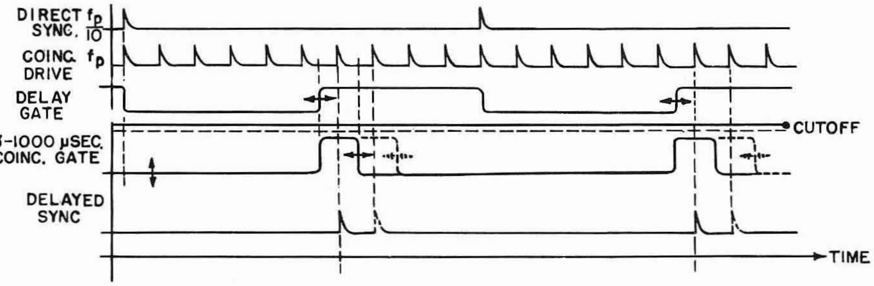
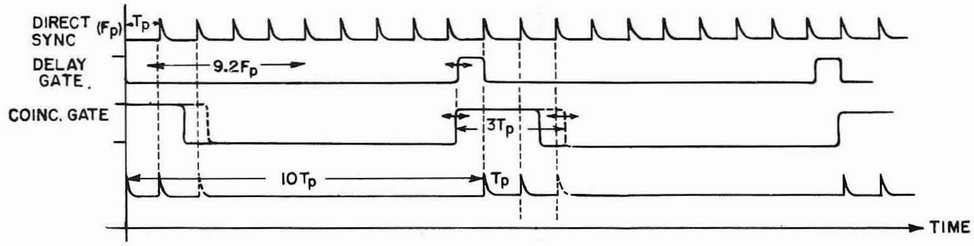



Figure 1.4c.
Timing of Multiple Pulses.

Figure 1.4d. Time Relationships When Delay Circuit Is Used as a PRF Divider. Coincidence Circuit Driven by Direct Synchronizing Pulse.



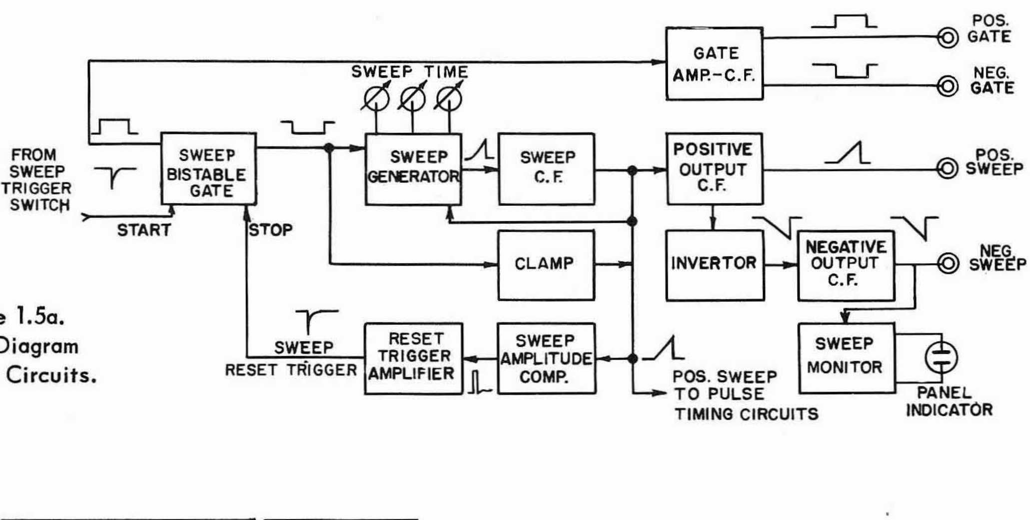




Figure 1.5a.
Block Diagram of Sweep Circuits.

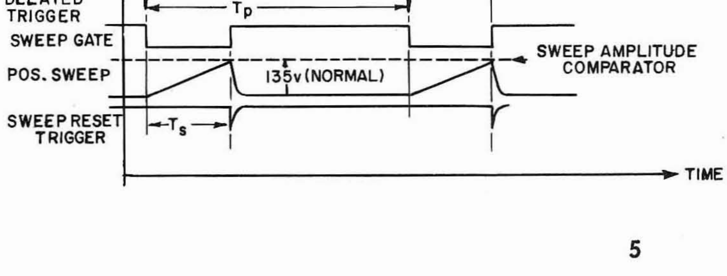



Figure 1.5b.
Time Relationships in the Sweep Circuit.

1.2.6.5 Pulse-Timing Circuits. The sweep voltage operates two amplitude comparators (Figure 1.6a). The comparator at the lower voltage level produces the start trigger (Figure 1.6b), while that at the higher voltage produces the stop trigger. The d-c control voltages for these comparators are set by the concentric panel controls for pulse duration and pulse delay (Figure 1.7). The triggers produced by the changes of state of the comparator circuits are differentiated and fed through a pair of cathode followers to the PULSE START STOP TRIGGERS switch, where they are fed to the pulse generator circuit to time the pulse and to the START and STOP panel terminals. When the PULSE START STOP TRIGGERS switch is set to INTERNAL CIRCUITS (NORMAL), these triggers operate a pair of amplifier stages, which shape them to drive the bistable multivibrator circuit of the pulse source.

1.2.6.6 Main Pulse-Generating Circuits. (See Figure 1.6a.) The START and STOP triggers operate a high-speed, bistable gate circuit. This circuit drives a pair of amplifiers, which in turn operate a pair of drivers for the output stage. The push-pull output stage is a pair of beam tubes used as a current source with switched load resistors, across which the pulse of voltage is

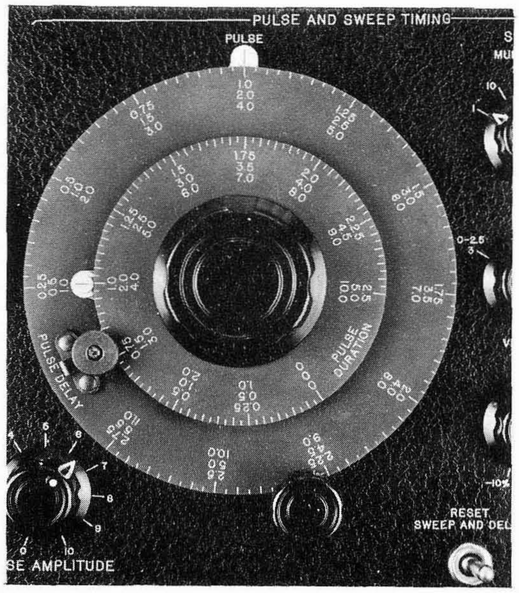



Figure 1.7. Close-up of Pulse-Delay and Duration Dials.

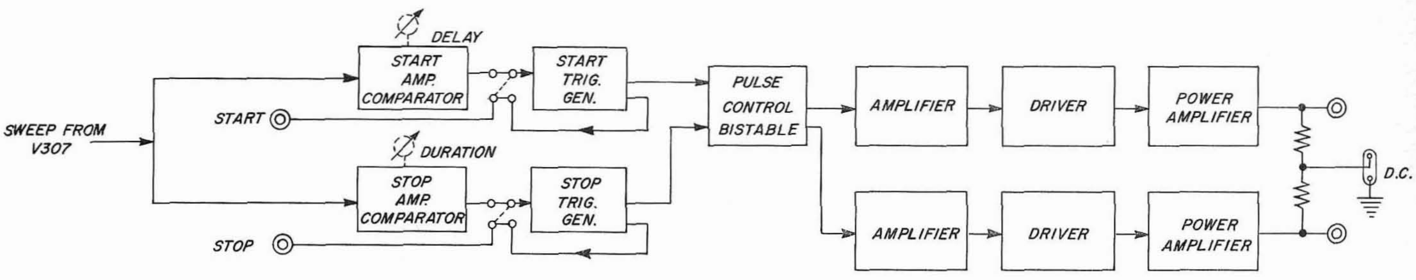



Figure 1.6a. Block Diagram of Pulse-Timing and Output Circuits.

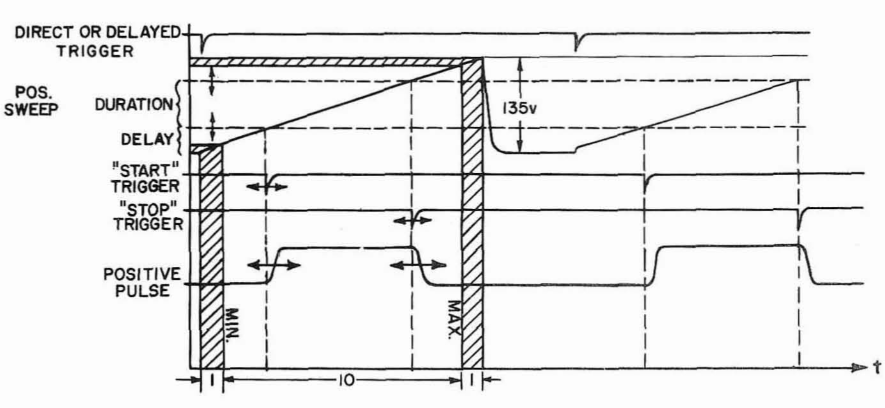



Figure 1.6b.
Pulse Timing Diagram.

developed. The conducting output tube produces a current of 150 ma. Screen voltage on this stage is varied to control pulse amplitude.

The output system is balanced, and the push-pull pulses appear at coaxial connectors and parallel binding posts. The low-potential side of the load resistors is connected to an additional binding post normally grounded to the panel through a shorting link. Under these conditions the output pulses contain an a-c component negative with respect to ground. If the shorting link is removed, the d-c component of an external voltage (from any low-voltage laboratory supply or battery able to furnish 150 ma) can be varied by about ±25 volts.

# Section 2
# OPERATING PROCEDURE

2.1 GENERAL. The Type 1391-B Pulse, Sweep, and Time-Delay Generator can, for instructional purposes, be considered four separate instruments. If a thorough familiarity with all controls is neither desired or needed, study merely those paragraphs that apply to the circuits being used, as listed below:

- 2.2 Auxiliary Equipment
- 2.3 Initial Control Settings
- 2.4 Synchronization
- 2.5 Delay Circuit
  - 2.5.1 Normal Use
  - 2.5.2 Time Selection
- 2.6 Sweep Circuit and Pulse Duration-Delay System
- 2.7 Pulse-Generating Circuit
- 2.8 Use of the PULSE START STOP TRIGGERS switch

2.2 AUXILIARY EQUIPMENT. A few auxiliary instruments are usually needed as components of the external system. First, a source of a timing waveform is needed to determine the repetition rate of the pulser. This can be a simple audio-ultrasonic oscillator, such as the General Radio Type 1210-C Unit R-C Oscillator, Type 1301-A Low-Distortion Oscillator, Type 1302 Oscillator, or Type 1304-B Beat-Frequency Oscillator, or it can be a crystal oscillator with frequency dividers to produce any frequency up to the 100-200-kc region. More complex sources of time-coherent pulses are needed for the time-selection operations described in paragraph 2.5.2. For these operations a timing generator such as the Tektronix Type 180, Dumont Type 300 or equivalent can be used.

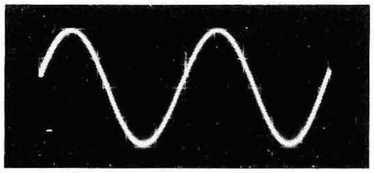
Choice of oscilloscope will depend on the application. An oscilloscope with broadband video amplifier is, of course, necessary to permit observation of short-duration pulses. In order to view the output pulse without degradation of rise time or shape, the pulse must be amplified with a bandwidth in excess of 20 Mc, or else the pulse must be presented by direct connection to the oscilloscope deflection plates. Many applications, of course, do not require that the ultimate rise times be attained, and for these tests less complicated oscilloscopes can be used.

The waveforms shown in this section (Figures 2.1 through 2.7) are oscillograms taken directly from the screen of a Tektronix Type 551 oscilloscope. Throughout the following sections, the prf set by the timing oscillator will be 10 kc (100-$\mu$sec period). The operator should at first keep the dial settings in the delay and sweep circuits considerably less than this value. When the delay or sweep-duration settings equal or exceed the period, the oscilloscope patterns can become unstable or difficult to interpret.

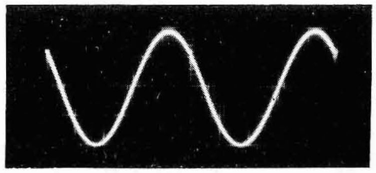
2.3 INITIAL CONTROL SETTINGS. Before turning the instrument on, set the following controls as indicated:

| Control | Setting | |
|---|---|---|
| TIME DELAY RANGE | 10-100 $\mu$sec | 50-$\mu$sec |
| TIME DELAY MICRO-SECONDS | 5.00 | |
| COINCIDENCE GATE DURATION | NORMAL - 3 $\mu$sec | |
| COINCIDENCE SEN-SITIVITY | NORMAL | |
| SWEEP TRIGGER | DIRECT | |
| TRIGGER SELECTOR | POS GOING AC | |
| TRIGGERING LEVEL | CENTER | |
| PULSE AMPLITUDE | 10 | |
| OUTPUT IMPEDANCE | 50 | |
| PULSE DURATION | 5.0 on center scale (50-$\mu$sec pulse) | |
| PULSE DELAY | 0.5 on center scale (5-$\mu$sec delay) | |
| SWEEP MULTIPLIER | 10 (60-$\mu$sec sweep) | |

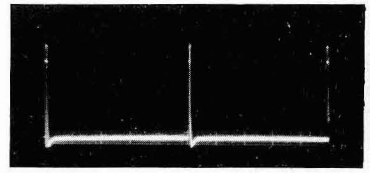
**FIGURE 2.1. 10-kc PRF, 20$\mu$sec/cm**



A. INPUT SIGNAL, TRIGGER SELECTOR AT POSITIVE

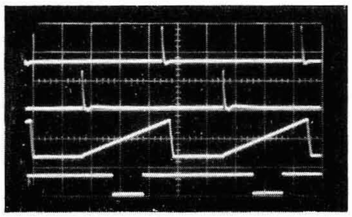


B. INPUT SIGNAL, TRIGGER SELECTOR AT NEGATIVE



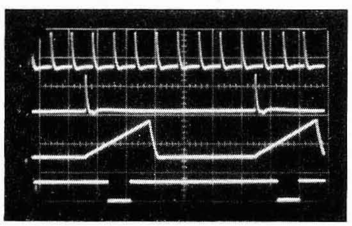
C. DIRECT SYNC PULSE

**FIGURE 2.2. 10-kc PRF 40$\mu$sec DELAY 20$\mu$sec/cm**



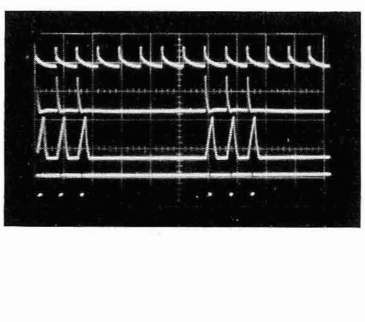
A. DIRECT SYNC
B. DELAY SYNC, 40$\mu$sec DELAY
C. POSITIVE SWEEP, 60$\mu$sec
D. NEGATIVE PULSES, DELAY 20, DURATION 20

**FIGURE 2.3. 100 kc PRF DELAY SET FOR 70$\mu$sec SWEEP SET FOR 30$\mu$sec**



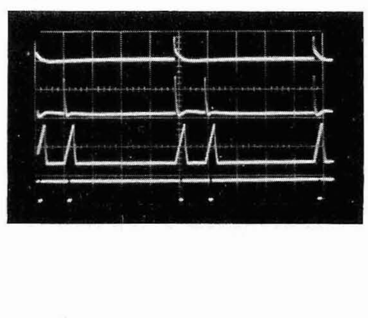
A. DIRECT SYNC
B. DELAY SYNC
C. SWEEP, 30$\mu$sec
D. PULSE, 10$\mu$sec PULSE, 10$\mu$sec DELAY ON SWEEP

**FIGURE 2.4. DELAY SET FOR 72$\mu$sec, PRF 100 kc TRIPLE SWEEP AND PULSE BY INTERNAL-MULTIPLE-PULSE METHOD**



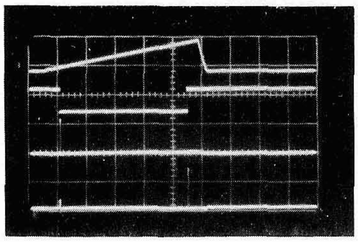
A. DIRECT SYNC
B. DELAY SYNC
C. SWEEP
D. PULSE

**FIGURE 2.5. PULSE PAIR, PRF 10 kc, DELAY 20$\mu$sec DIRECT SYNC TO POS COINC DRIVE TO PRODUCE DOUBLE PULSE**



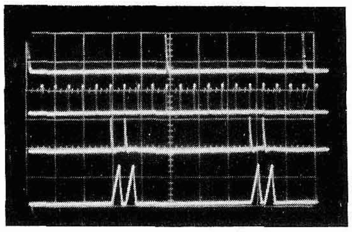
A. DIRECT SYNC
B. DELAY SYNC
C. SWEEP
D. PULSE

FIGURE 2.6.



A. POS SWP, 10 kc 60$\mu$sec, 10$\mu$sec/cm
B. NEG PULSE 50$\mu$sec 10$\mu$sec/cm
C. START PULSE
D. STOP PULSE

FIGURE 2.7. MULT PULSING, EXTERNAL METHOD (20$\mu$sec/cm)



A. 10 kc DIRECT SYNC PULSE
B. 100-kc PULSES TO POS COINC DRIVE
C. DELAYED SYNC
D. 6-$\mu$sec SWEEP (SWEEP TRIGGER SWITCH IN DELAYED POSITION)

2.3 INITIAL CONTROL SETTINGS. (Cont)

| Control | | Setting |
|---|---|---|
| SWEEP DURATION $\mu$SEC | 6 | 60-$\mu$sec sweep |
| VERNIER | 0 | |
| PULSE START STOP TRIGGERS | INTERNAL (NORMAL) | |

2.4 SYNCHRONIZATION PROCEDURE.

a. Connect an audio oscillator (output at least one volt) to the PRF DRIVE binding posts, and set the oscillator for a frequency of 10 kc.

b. Connect an oscilloscope (prepared to write at about 20 $\mu$sec per division) as follows:

(1) Connect the oscilloscope ground to the ground of the Type 1391-B.

(2) Connect the oscilloscope external synchronizing or trigger input to the Type 1391-B DIRECT SYNC OUT.

(3) Set the oscilloscope to accept a positive-going external synchronizing signal.

(4) Connect the oscilloscope vertical amplifier to the Type 1391-B PRF DRIVE binding posts.

c. Turn all equipment on. After a warm-up time of about a minute, both neon indicators on the Type 1391-B should glow. If either indicator does not light, flip the RESET switch to start the sweep or delay circuit.

d. Adjust oscilloscope to give a stable presentation and observe the input waveform on the oscilloscope. It should appear as shown in Figure 2.1A.

e. Set the TRIGGER SELECTOR switch to NEG GOING AC. The oscilloscope pattern should change phase by about 180 degrees, and should appear as shown in Figure 2.1b.

f. Connect the oscilloscope input to the Type 1391-B DIRECT SYNC OUT terminals and observe the 75-volt, 1.5-$\mu$sec positive synchronizing pulse. It should appear as shown in Figure 2.1C or 2.2A.

2.5 DELAY CIRCUIT.

2.5.1 NORMAL USE.

a. Leave the input circuits connected as in paragraph 2.4, with the TRIGGER SELECTOR switch set for either positive- or negative-going triggering. Input oscillator frequency should be set at 10 kc.

b. Move the oscilloscope vertical input to the DELAYED SYNC OUT terminals. The positive delayed synchronizing pulse should appear as shown in Figure 2.2A.

c. Move the TIME DELAY MICROSECONDS dial to 2.00 and observe the motion of the delayed synchronizing pulse. It should appear as in Figure 2.2B. Change the setting of the TIME DELAY RANGE switch to 1-10 $\mu$sec, and again observe the pulse.

d. Set the TIME DELAY RANGE switch to the 10-100-$\mu$sec range, and increase the MICROSECONDS dial setting from 5.00 to 11.00 (fully clockwise). This produces a delay of 110 $\mu$sec. If the delay indicator lamp goes out, flip the RESET switch to start the delay.

e. Remember that the period set by the timing oscillator was only 100 $\mu$sec. The delay circuit is now "counting down," and the output period from the delay circuit is 5kc or 200 $\mu$sec. Figure 2.3 illustrates this principle.

f. Return the DELAY MICROSECONDS dial to 5.00.

2.5.2 TIME SELECTION. There are two methods of using the delay circuits for time selection. The method described in paragraph 2.5.2.1 (Figure 1.4d) does not require an external timing source, but uses the direct sync to produce internal multiple pulses. The second method, described in paragraph 2.5.2.2, requires the use of a timing-pulse generator.

2.5.2.1 Internal Multiple Pulse Method.

a. Connect an external audio oscillator (set for 10 kc) to PRF DRIVE.

b. Set the TRIGGER SELECTOR switch to POS GOING AC.

c. Set the COINCIDENCE SENSITIVITY control fully counterclockwise.

d. Set the COINCIDENCE GATE DURATION control to 250.

e. Set the TIME DELAY RANGE switch to the 100 $\mu$sec-1 msec range.

f. Set the TIME DELAY MICROSECONDS dial to 9.20.

g. Connect the oscilloscope vertical-amplifier input to the DELAYED SYNC OUT terminals.

h. Set the oscilloscope writing rate at 200 $\mu$sec per division.

i. Set the oscilloscope for internal positive sync (or external positive sync and connect sync input to the Type 1391-B DELAYED SYNC OUT).

j. Connect a wire lead from the DIRECT SYNC OUT terminal to the POS COINCIDENCE DRIVE terminal.

k. It may be necessary to advance the COINCIDENCE SENSITIVITY control clockwise if the DELAY MONITOR lamp does not come on when the SYNC and DRIVE terminals are connected.

l. The DELAY MONITOR lamp may go out when the TIME DELAY MICROSECONDS dial is moved over each 100-$\mu$sec point. The delay circuit can be started by means of the RESET switch.

m. The oscilloscope pattern should be similar to that shown in Figure 2.3B. A timing diagram showing the action of the input and delay coincidence circuit is shown in Figure 1.4d, and the action is explained in paragraph 1.2.6.3. At this point it may be necessary to readjust carefully the oscilloscope synchronizing controls to obtain a stable pattern since the waveform is complex.

2.5.2.2 Time Selection, with an External Timing Generator.

a. Connect a 1-kc (1000-$\mu$sec) pulse output from the timing generator (amplitude over 10 volts) to the PRF DRIVE terminals.

b. Set the TRIGGER SELECTOR switch to SINGLE PULSE, and for the appropriate polarity.

c. Connect 100-$\mu$sec pulse of either polarity from the timing generator to the appropriate COINCIDENCE DRIVE terminals.

d. Connect the oscilloscope vertical-amplifier input to the Type 1391-B DELAYED SYNC OUT terminals.

e. Connect the oscilloscope sync input to the PRF DRIVE terminals.

f. Set the oscilloscope synchronizing controls for the polarity of the input pulse, and set the oscilloscope writing rate at 200 $\mu$sec per division.

g. Set the TIME DELAY RANGE switch to the 100-$\mu$sec – 1-msec range.

h. Set the TIME DELAY MICROSECONDS dial to 5.50.

i. Set the COINCIDENCE GATE DURATION control to 200.

j. Increase the setting of the COINCIDENCE SENSITIVITY control from its counterclockwise limit until the indicator lamp glows.

k. Experiment with the COINCIDENCE SENSITIVITY control to obtain maximum amplitude from the two delayed synchronizing pulses that appear. Note that all 100-$\mu$sec pulses appear when the control is in the NORMAL (clockwise) position. Correct setting should yield a pattern similar to that shown in Figure 2.7C.

l. The TIME DELAY MICROSECONDS and COINCIDENCE GATE DURATION controls can now be varied to study the circuit action. The basic principles of operation of this circuit are presented in paragraph 1.2.6.3, and Figure 1.4c shows an idealized time diagram illustrating the time selection system.

m. Now obtain two delayed synchronizing pulses (as in step k), and move the oscilloscope vertical amplifier input connection to the SWEEP POS terminals.

n. With the SWEEP TRIGGER switch at DIRECT, note that there is one 60-$\mu$sec sweep sawtooth for each 1000-$\mu$sec pulse to the PRF DRIVE terminals.

o. Set the SWEEP TRIGGER switch to DELAYED, and note that there is a sweep for each 100-$\mu$sec timing pulse selected (Figure 2.2D).

p. Repeat step l, observing the sweep instead of the delayed synchronizing signals.

## 2.6 SWEEP CIRCUIT.

a. Set all controls to the positions given in paragraph 2.3.

b. Connect the prf drive oscillator, set at 10 kc to give a 100-$\mu$sec time base, to the PRF DRIVE terminals.

c. Connect the oscilloscope vertical amplifier input to the SWEEP POS terminals.

d. Connect the oscilloscope sync (or trigger) input to the Type 1391-B DIRECT SYNC OUT terminals. Set the oscilloscope for a positive synchronizing signal.

e. Set the oscilloscope writing rate to 20 $\mu$sec per division.

f. With all equipment on and warmed up, check that the DELAY MONITOR and SWEEP MONITOR indicator lamps are on. If either indicator does not glow, flip the RESET switch. If both lamps still do not glow, recheck the control settings against those given in paragraph 2.3.

g. Note that one 60-$\mu$sec sweep is generated for each input cycle. The oscilloscope pattern should appear as shown in Figure 2.2C.

h. Change the sweep duration to 30 by setting the SWEEP DURATION $\mu$SEC control to 3 (with the SWEEP MULTIPLIER switch still at 10). Then generate 3-, 6-, and 12-$\mu$sec pulses by setting the SWEEP MULTIPLIER switch to 1 and switching the SWEEP DURATION $\mu$SEC control to 3, 6, and 12.

i. Return the SWEEP MULTIPLIER switch to 10 and the SWEEP DURATION $\mu$SEC switch to 6.

j. Connect the oscilloscope vertical amplifier input to the SWEEP POS, GATE POS, and GATE NEG terminals and observe the negative sweep and the positive and negative gates. Then return the oscilloscope connection to the SWEEP POS terminals.

k. Place the SWEEP TRIGGER switch in the DELAYED position to delay the start of the sweep 50 $\mu$sec.

l. Move the TIME DELAY MICROSECONDS dial to move the sweep in time relative to the direct synchronizing pulse. The delayed trigger may be lost if the delay setting exceeds 100 $\mu$sec. If it is lost, flip the RESET switch.

m. If the sweep controls are set for a duration in excess of 100 $\mu$sec, the sweep circuit will ignore the triggers that occur during sweep time and thereby reduce the sweep recurrence rate. Observe this effect as directed in steps n and o.

n. Set the SWEEP DURATION $\mu$SEC control to 12 and the SWEEP MULTIPLIER to 10 to produce a 120-$\mu$sec sweep. The sweep recurrence rate is now 5 kc. If the SWEEP MONITOR lamp goes out, flip the RESET switch.

o. Reset the sweep controls for 60 $\mu$sec (SWEEP DURATION $\mu$SEC to 6, SWEEP MULTIPLIER to 10), and vary the input timing frequency from 10 kc at the audio generator. Note that as the frequency is increased toward 16 kc, the sweep becomes instable. The vernier control can be set to either + or − 10% to restore stability.

## 2.7 PULSE-GENERATING CIRCUIT.

a. Set all controls to the positions listed in paragraph 2.3.

b. Connect the oscilloscope vertical amplifier input to the PULSE POS terminals. If either brief pulses or a fast rise time is desired, use a coaxial cable for this connection.

c. Connect the oscilloscope ext sync to the Type 1391-B DIRECT SYNC terminals.

d. Observe the output positive 50-$\mu$sec pulse. Experiment with the DELAY and DURATION controls, setting DELAY to 20, DURATION to 20. The negative pulse should appear as in Figure 2.2D.

e. Move the oscilloscope connection to the PULSE POS terminals and observe the positive 40-$\mu$sec pulse.

f. Reduce the pulse duration from 50 to 25 $\mu$sec by switching the SWEEP DURATION $\mu$SEC control to 3. Observe the pulse duration and delay and return the SWEEP DURATION $\mu$SEC switch to 6.

g. Reduce the pulse duration to 25 $\mu$sec by resetting the PULSE DURATION (inner) dial.

h. Reposition this 25-$\mu$sec pulse to start 25 $\mu$sec after the sweep by rotating the PULSE DELAY dial counterclockwise. Note that the three rings of numbers on the PULSE DURATION and PULSE DELAY dials correspond to the three settings of the PULSE SCALE switch.

i. Now pulses of 2.5 $\mu$sec can be obtained with the SWEEP MULTIPLIER switch set at 1. Various other pulse durations and delays can be set by means of the sweep switches, PULSE DURATION, and PULSE DELAY controls.

j. Short Pulses: Decrease the sweep duration to 3 $\mu$sec. Then decrease the PULSE DURATION setting until a pulse of minimum duration is produced. Note that this pulse can be reduced even beyond the usual amplitude, and that the pulse polarity will reverse suddenly at a DURATION setting below zero. This is characteristic, since it is not possible to produce a mechanical stop of sufficient accuracy to stop the motion of the DURATION dial at exactly zero.

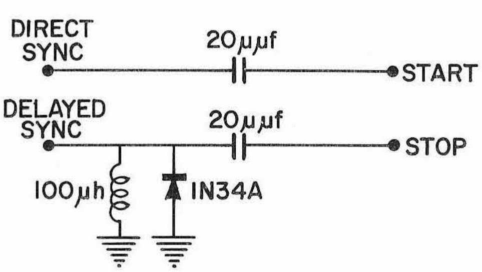



Figure 2.8. Adding Network for Multiple Pulsing.

k. Set up a 1-$\mu$sec pulse and experiment with the OUTPUT IMPEDANCE and PULSE AMPLITUDE controls. Some defects might appear in the pulse due to impedance mismatch as the OUTPUT IMPEDANCE setting is varied. Note also that the PULSE AMPLITUDE control adversely affects the pulse shape when the pulse is set to greatly reduced values. The PULSE AMPLITUDE control is generally satisfactory for pulses of long duration and over a 10- or 20-db range, but for best pulse shape an attenuator or a pad of the proper impedance is recommended.

## 2.8 USE OF THE PULSE START STOP TRIGGERS SWITCH.

### 2.8.1 INTERNAL (NORMAL) POSITION.

a. Set all controls to the positions listed in paragraph 2.3.

b. Set the oscilloscope horizontal controls for a writing rate of 20 $\mu$sec per division.

c. Connect the oscilloscope vertical amplifier input to the PULSE NEG terminals.

d. Connect the oscilloscope sync to the Type 1391-B DIRECT SYNC terminals.

e. Observe the 50-$\mu$sec negative pulse on the oscilloscope. It should appear as shown in Figure 2.6B.

f. Now move the oscilloscope vertical input connection to the START terminal. Note the presence of a 5-volt positive start pulse corresponding to the leading edge of the main pulse (Figure 2.6C).

g. Move the oscilloscope vertical input connection to the STOP terminal, and note the presence of a 5-volt positive stop pulse as shown in Figure 2.6D. Note at both START and STOP terminals a negative pulse at the end of the sweep. Move the PULSE DURATION dial and note the motion of the stop pulse corresponding to the dial reading. The start pulse moves when the PULSE DELAY dial is moved.

### 2.8.2 EXTERNAL POSITION.

a. Move the oscilloscope vertical input connection back to the PULSE POS terminal, and, if possible, set the oscilloscope for d-c input.

b. Set the PULSE START STOP TRIGGERS switch to the EXT position.

c. Tap first the START and then the STOP terminal with a piece of metal held in the hand. The pulse should start and stop with each tap. In this manner, pulses can be produced by any external trigger generator.

d. To use the delay circuit to time the main pulse, proceed as directed in steps e through h below.

e. Set the oscilloscope and PULSE START STOP TRIGGERS switch as indicated in steps a and b above.

f. Connect a jumper wire from the DIRECT SYNC OUT terminal to the START terminal and another from DELAYED SYNC to STOP terminal.

g. Note that a 50-$\mu$sec pulse, corresponding to the 50-$\mu$sec delay interval, is produced (Figure 2.5B). Now vary the time delay settings from 1 $\mu$sec up to about 90 $\mu$sec and note that pulse duration is controlled by delay.

h. This connection, in which the delay circuit is used to control pulse duration, permits the production of pulses up to 1.1 seconds in duration. To produce such a pulse, set (if possible) the oscilloscope writing rate at 0.2 sec per division. Disconnect the driving oscillator from the PRF DRIVE terminals. Set the TIME DELAY MICROSECONDS dial to 11.00, and the TIME DELAY RANGE switch to 100 $\mu$sec – 1 sec. Now either flip the RESET switch or tap the PRF DRIVE terminal quickly, and note the production of the long pulse.

2.8.3 INTERNAL + EXTERNAL POSITION. This position permits externally produced trigger pulses to be added to the start and stop triggers generated in the pulse timing circuits. To test the operation of this switch position, generate a double pulse as follows:

a. Build and connect the adder circuit shown in Figure 2.8.

b. Set the SWEEP TRIGGER switch to DELAYED.

c. Connect the oscilloscope vertical deflection input to the PULSE POS terminals.

d. Connect the oscilloscope synchronizing terminal to the DIRECT SYNC OUT terminals.

e. Set the PULSE START STOP TRIGGERS switch to EXTERNAL and move the DELAY MICROSECONDS dial from its standard position, noting that the delay circuit controls the duration of the pulse.

f. Set the PULSE START STOP TRIGGERS switch to INTERNAL + EXTERNAL, with the pulse timing controls in standard positions. Note the presence of a double pulse. The delay and duration of the second pulse can be varied by means of the PULSE DELAY and DURATION controls.

# Section 3
# CALIBRATION PROCEDURE

3.1 INTRODUCTION. Calibration and readjustment procedures are given in the order of signal progression through the instrument. Paragraph 3.2 lists the test equipment necessary to carry out the calibration of the various circuits, and paragraphs 3.3 through 3.6 discuss the calibration and readjustment procedures necessary in each circuit.

It is hardly likely that a complete calibration, such as that given every new instrument in the General Radio laboratory, will ever be necessary. Usually few, if any, adjustments are necessary when a tube or circuit component is replaced because of failure. Gradual degradation in tube characteristics with use may require retouching of the screwdriver adjustment common to all ranges in the sweep or delay circuit. Also, some unpredictable shift in the values of resistors or capacitors in range timing circuits will generally appear as a change in the calibration of one range. Only the adjustment for that range must be set, and only the relevant paragraph must be consulted, along with paragraph 3.2.

A common adjustment is the range minimum adjustment (R238) in the delay circuit, which may require readjustment when V203 is replaced. This adjustment, discussed in paragraph 3.4, is common to all delay ranges. An equivalent adjustment may be necessary in the sweep circuits to restore the calibration of the pulse-delay dial when either V303 or V309 is replaced. The controls requiring readjustment are the pulse duration and delay minimums R412 and R411. (Refer to paragraph 3.5.2.) Other adjustments are those used to correct for component tolerances in the R-C time constants. Such adjustments must be made only when the components themselves drift (unlikely) or are replaced.

3.2 TEST EQUIPMENT. The type and quantity of auxiliary test equipment necessary for recalibration depend entirely on the accuracy desired, the complexity of the recalibration, and, to some extent, on the range being recalibrated. This equipment can range from a cathode-ray oscilloscope, audio oscillator, and ac-dc multirange meter to the full series of time-measuring equipment listed below. The equipment listed below is adequate for complete recalibration of the instrument.

(1) Oscilloscope - Tektronix 530 or 540 series, or equivalent.

(2) Crystal-controlled time-marker generator - Tektronix 180, Dumont 300, or equivalent producing time markers from 1 to 10,000 $\mu$sec. All of these timing markers should be simultaneously available at the panel terminals of the marker generator.

(3) Time-interval measuring system – While not an absolute necessity in the recalibration of the instrument, a time-interval meter simplifies the calibration of the longer sweeps, delay intervals, and pulse durations. This time-interval meter should operate from two triggers, one to start and one to stop the time-interval measurement. Ideally, it should resolve 1- or 0.1-$\mu$sec input pulses. The time-interval meter will facilitate the measurement of the longer delays, sweeps, and pulses, without the necessity of viewing the very slow transients arising from the long delays on an oscilloscope. Possible instruments for use in this application, if available, are the Berkeley 5571 and 5510, Hewlett-Packard 521-A, 522-B, or 524-B plus 526-B, or the LFE 501.

Additional test equipment includes an audio oscillator (General Radio Type 1210, 1302, or equivalent) needed to set the prf, and an a-c vacuum-tube voltmeter to measure either the rms or peak value of the input voltage.

3.3 CALIBRATION AND ADJUSTMENT OF INPUT CIRCUITS.

3.3.1 ADJUSTMENT OF R104.

a. Connect the audio oscillator (set to 10 kc, output at least 1 volt) to the PRF DRIVE terminals.

b. Connect the oscilloscope vertical amplifier input to the DIRECT SYNC OUT terminals.

c. Center the TRIGGERING LEVEL control.

d. Set the TRIGGER SELECTOR switch to POS GOING AC, and observe the direct synchronizing signal as the audio oscillator gain-control setting is decreased.

e. Adjust R104 so that the direct synchronizing pulse is formed with minimum voltage input. With correct adjustment, the input voltage will be less than 0.3 volt rms.

3.3.2 ADJUSTMENT OF C102.

a. Set the TRIGGER SELECTOR switch to POS GOING AC.

b. Set the SWEEP TRIGGER switch to DIRECT.

c. Connect the oscilloscope probe to the center (output) terminal of S203, the SWEEP TRIGGER switch.

d. Adjust C102 for a trigger amplitude of 5 to 6 volts peak-to-peak.

## 3.4 DELAY CIRCUITS.

3.4.1 ADJUSTMENT OF THE TIME DELAY MICROSECONDS DIAL MINIMUM AND MAXIMUM. This adjustment should be necessary only when either V203, V204, or V205 has been replaced. The time delay between the direct and delayed synchronizing pulses must be measured accurately, and should be within 0.3 percent.

There are three different ways to measure the time delay between the direct and delayed synchronizing pulse. The first two ways require the use of only the high-speed oscillograph and the precision time-marker generator. The third method, most convenient for the three longer delay ranges, requires the use of the time-interval measuring device (refer to paragraph 3.2).

3.4.1.1 First Method. In this method, the time-marker generator is used to set the prf of the Type 1391-B at a rate considerably slower than the period corresponding to the delay range to be checked. A second output from the time-marker generator is presented to calibrate the oscilloscope sweep. An electronic switch that will simultaneously present the delayed synchronizing signal and the timing markers to the oscilloscope is recommended. Timing markers can also be presented if they are placed on the oscilloscope gate input terminals either to brighten or to blank the oscilloscope sweep to display the marker interval. The position of the direct synchronizing pulse relative to the timing markers is carefully determined and the oscilloscope probe is moved to the DELAYED SYNC terminal. The delay dial calibration can then be checked at the cardinal points represented by the timing markers. This procedure is the only effective means for calibration of the lower two delay ranges, 1-10 and 10-100 $\mu$sec.

3.4.1.2 Second Method. In the second method, the timing-marker generator is used to set the prf of the Type 1391-B as in the first method, but the higher-frequency timing markers corresponding to the cardinal points on the delay dial are fed to the appropriate COINCIDENCE DRIVE terminals and the coincidence system is adjusted so that coincidence is established only when the coincidence gate is produced at the same time as one of the marker pulses. Since there is a finite rise time of about 0.2 $\mu$sec at the early edge of the coincidence gate, the correct alignment of the early edge of this gate with a given marker pulse to light the DELAY MONITOR lamp will permit sufficiently accurate calibration only above 100 $\mu$sec, and therefore this method becomes effective only on the third range and above. If, for example, it is desired to calibrate the 100-$\mu$sec-to-1-$\mu$sec range at 100-$\mu$sec cardinal points, the timing-marker generator should set the prf at 100 cps, and 100-$\mu$sec calibration markers should be fed to the COINCIDENCE DRIVE terminal corresponding to marker polarity. The COINCIDENCE GATE DURATION control should be set at a value considerably less than 100 $\mu$sec, say 20. Now suppose the TIME DELAY MICROSECONDS dial is rotated so that the actual delay is 190 $\mu$sec. The second 100-$\mu$sec marker pulse from the timing generator will lie in the center of the coincidence gate, and the DELAY MONITOR lamp will glow. As the delay dial setting is increased to exactly 200 $\mu$sec, the leading edge of the coincidence gate will move out from under the 100-$\mu$sec marker and the lamp will go out. It is apparent, therefore, that the accurate calibration point is attained when the delay dial is moved from higher to lower delay reading at the point where the DELAY MONITOR lamp just lights. For the calibration of longer delay ranges, correspondingly longer time-duration coincidence-gate settings can be used. The accuracy, determined by rise time of the coincidence gate and the ignition voltage of the DELAY MONITOR lamp, increases.

3.4.1.3 Third Method. A time-interval measuring system, capable of being operated by the direct and delayed synchronizing signals, provides a convenient method of calibration. Suppose the time-interval meter is capable of resolving and counting 1-$\mu$sec pulses. The delay circuit can be calibrated to an accuracy of 0.1 percent at 1 msec by the plus or minus one-count limitation. Four decade registers are necessary for this precision at the low end of a range. The procedure is to connect the start terminals of the time-interval meter to the DIRECT SYNC OUT terminals of the Type 1391-B, and the stop terminal to the DELAYED SYNC OUT terminal of the Type 1391-B. A simple trigger, derived on the longer ranges simply by the tapping of a finger against the PRF DRIVE terminal or by the use of a switch and a battery, initiates a "single stroke" delay-circuit action and opens and closes the timing gate of the time-interval meter at the delay period. The delay then reads directly in the decade registers of the interval counter.

By any one of the above three methods, the accuracy at both ends of the TIME DELAY MICROSECONDS dial should first be established for two or three ranges. If the minimum or maximum is consistently off on all these ranges, then either the delay minimum control (R238) and/or the delay maximum control (R236) should be readjusted. This readjustment should be accomplished on the 10-100-msec range. It is necessary to set both the minimum and the maximum controls for correct value at dial readings of 200 for the minimum and 1000 for the maximum. Having calibrated the 10-100-msec range in this manner, check overall dial linearity by checking the delay at cardinal dial points, and test the other ranges to establish their accuracy. If only one range deviates from the correct readings, adjust the appropriate potentiometer (R228 to R233). Note that the 100 msec-to-1-sec range has two adjustments: R233 adjusts the time constant correctly to produce the accurate maximum delay at 1 sec and R232 adjusts the amplitude of the initial voltage step for the correct dial reading at 100 msec. If V203 has been replaced, it may be necessary to readjust C222 of the 1-10-$\mu$sec range to restore dial calibration due to small changes in stray capacitance.

3.4.2 COINCIDENCE GATE ADJUSTMENTS. If, upon replacement of V206, it is found that either the minimum or maximum coincidence gate duration departs intolerably far from 3 or 1000 $\mu$sec, adjust R255, the 1000-$\mu$sec adjustment, or R249, the 3-$\mu$sec adjustment. Usually only a cathode-ray oscillograph connected at TP204 is necessary to establish the desired measurement accuracy. Of course, a more precise adjustment of either the minimum, maximum, or any point between can be made if higher accuracy is desired. It is necessary to repeat the 3- and

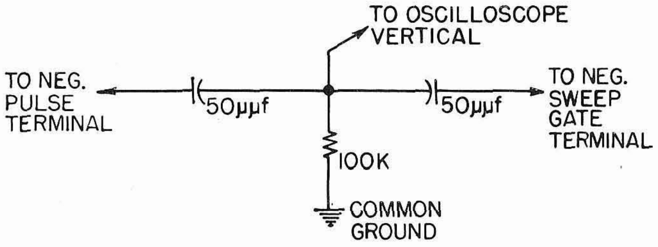



Figure 3.1 Adder Circuit Diagram

then the 1000-μsec adjustments more than once to establish both accurately, since there is a slight interaction.

## 3.5 SWEEP- AND PULSE-TIMING ADJUSTMENTS.

3.5.1 GENERAL. The sweep- and pulse-timing adjustments are discussed together here because the characteristics of the sweep control, the accuracy of the pulse-timing scales, and the controls corresponding to the previously described delay minimum and maximum controls are the calibration controls that determine the minimum pulse delay and the maximum pulse duration and delay.

The sweep and pulse-timing adjustments can all be made by the time-measuring techniques described in paragraph 3.4.1. Here it is necessary to measure both sweep duration and pulse duration, and the easiest way to do this is to build a differentiator and adder network for the oscilloscope to present the sweep gate and pulse transitions simultaneously. The adder and its connections are shown in Figure 3.1. Pulse duration, delay, and sweep duration can be adjusted by observation of the pulses produced at the beginning and end of the sweep gate and main pulse. In order to register the marker showing the beginning of the sweep with the timing-markers, the sweep can be triggered by the delay circuit and made coincident with a specific timing marker.

3.5.2 OVER-ALL SWEEP AND PULSE-TIMING ADJUSTMENT. The 600-μsec sweep range is used for the initial adjustment of sweep duration and for synchronization of the readings of the delay and duration dials. Make sure that the duration and delay readings have a common error on several ranges before readjusting those calibration controls common to all ranges. An error in pulse duration or delay appearing on only one range can be eliminated by adjustment of that range's sweep time constant only. If an error in pulse duration or delay appears on all ranges, proceed as follows:

a. Construct the R-C network shown in Figure 3.1.

b. Connect this network to the PULSE NEG and GATE NEG terminals.

c. Mix the output from the R-C network with 100-μsec timing markers by means of an additional network or a dual-channel oscilloscope attachment.

d. Synchronize the Type 1391-B with the 10,000-μsec timing-marker output and obtain a coherent pattern on the oscilloscope.

e. Using the DELAY controls, align the start of the sweep with one 100-μsec timing pulse.

f. Set the PULSE DELAY to 1.0 and the PULSE DURATION to 4.0.

g. Center R408 (DURATION MAX).

h. Adjust R333 (600 μsec) to set the end of the pulse to the 500-μsec mark.

i. Adjust R352 (SWP AMP) to set the end of the sweep to 600 μsec.

j. Adjust R411 (POS MIN) to set the start of the pulse to the 100-μsec mark, and then rotate the PULSE DURATION dial to exactly zero, without disturbing the PULSE DELAY dial.

k. Adjust R412 (DUR MIN) to set the end of the pulse to coincide with the start of the pulse at the 100-μsec mark. (Both pulses will disappear.)

l. Now set the PULSE DURATION dial to 5.00 and advance the TIME DELAY MICROSECONDS dial to read 5.50.

m. Adjust R407 (POSITION MAX) to set the end of the pulse to coincide with the start of the pulse at 500 μsec. (Both pulses will disappear.)

n. If any adjustments required extensive resetting, repeat the procedure; maximum adjustments have a second-order effect on the minimum voltage and vice versa.

3.5.3 300-μSEC SWEEP ADJUSTMENT. Having calibrated or checked the 600-μsec range calibration, set the end of the 300-μsec sweep to the 300-μsec mark by adjusting R332 (300 μsec). Use an oscilloscope writing rate of 50 μsec per division.

3.5.4 1200-μSEC ADJUSTMENT. As in paragraph 3.5.3, adjust R334 (1200 μsec) to set the end of the sweep to coincide with the twelfth 100-μsec mark after the start of the sweep.

Main sweep- and pulse-timing adjustments are now complete, and the tracking of the x10, x$10^3$, and x$10^4$ ranges can be checked by means of a marker generator or, for the longer ranges, a time-interval counter operated by the pulse or sweep gates. A failure on the part of either the x10, x$10^3$, or x$10^4$ range to track the x$10^2$ range within two percent indicates that the value of a timing capacitor has changed, and the capacitor of the faulty range should be padded or replaced. If all three ranges fail to track by about the same amount, the timing capacitor of the x$10^2$ range (C323) should be replaced or padded.

3.5.5 CALIBRATION OF THE 3-, 6-, AND 12-μSEC RANGES.

a. First make tests to establish the accuracy of pulse timing on the 600-μsec range (refer to paragraph 3.5.2).

b. Set the controls as follows:

| Set | To |
|---|---|
| SWEEP MULTIPLIER | 1 |
| SWEEP DURATION MICROSECONDS | 6 |
| PULSE DURATION | 4.00 μsec (Center Scale) |

c. Connect a 10-kc signal from the marker generator to the PRF DRIVE terminals, and use 1-μsec oscilloscope markers from the marker generator.

d. Center R330 (6 μsec) and adjust C321 to obtain a pulse duration of 4.00 μsec at half amplitude.

e. Set the SWEEP DURATION to 3 and adjust for a 2-μsec pulse using R329 (3 μsec).

f. Set the SWEEP DURATION control to 12.00 and adjust the half-amplitude pulse duration to 8 μsec with R331 (12 μsec).

g. Set SWEEP DURATION MICROSECONDS control to 3. Set PULSE DURATION dial to zero, and adjust C417 for zero-duration pulse.

NOTE

If the 6-μsec sweep cannot be adjusted to produce a 4-μsec pulse with C321, or if R332 and R329 are far from center, reset C321 and repeat the 6-$\mu$sec adjustment (R330), and readjust the 3-$\mu$sec and 12-$\mu$sec ranges.

Generally, when V303 is replaced, only C321 must be retouched to restore proper operation to the 3-, 6- and 12-$\mu$sec ranges.

## 3.6 POWER-SUPPLY ADJUSTMENTS.

3.6.1 TEST EQUIPMENT. The minimum test equipment necessary for the correct adjustment of the power supply includes:

a. a 300-v battery or regulated power supply set for 300v,

b. a 5- or 10-amp Variac® autotransformer or equivalent,

c. an accurate a-c voltmeter to set line voltage,

d. a wattmeter with 500-watt scale,

e. a volt-ohmmeter with 20,000-ohm/volt sensitivity (Weston 772 Analyzer or equivalent).

f. additional apparatus, useful though not absolutely necessary, includes either a wave analyzer (General Radio Type 736-A or equivalent) or a Distortion and Noise Meter (General Radio Type 1932-A or equivalent).

3.6.2 INPUT POWER CHECK. The Type 1391-B requires 420 watts at 115 volts, 60 cycles.

3.6.3 300-VOLT REGULATOR ADJUSTMENT.

a. Measure the 300-volt power supply at pin 2 of plug PL401 or SO602 (yellow wire). It should read 300 ± 1 volts; if not, adjust R612.

b. To check the compensation adjustment, buck most of the 300 volts out with either a 300-volt battery or a second 300-volt regulated power supply. This will permit the voltmeter to be used in differential connection on its 1- or 5-volt scale. (The ±300-volt Type 1391-B supply can be offset by either 1 or 2 volts to permit the meter to read upscale.)

Now vary the line voltage to the Type 1391-B over the 105-125 (210-250) volt range. Note that as line voltage increases 10 percent the regulator output decreases by 0.5 to 1 volt and vice versa. If the compensation curve is not symmetrical about the 300-volt center, readjust R607 to make it so. R612 might need readjustment to maintain correct output voltage.

3.6.4 –150-VOLT ADJUSTMENT. R618 should be set to produce -150 volts output at pin 6 of plug PL401, with input voltage set at 115 volts.

3.6.5 -400-VOLT ADJUSTMENT. Adjust the PULSE DURATION and sweep timing controls to produce a 25-millisecond pulse at a 20-cps repetition rate. Set the PULSE AMPLITUDE control to maximum and set the output impedance for the highest-amplitude negative pulse whose negative edge can be seen on the screen. Set R618 for minimum line-frequency ripple on the "bottom" of this pulse as the line voltage is varied from 105 to 125 volts.

# Section 4
# DETAILED CIRCUIT DESCRIPTIONS

4.1 GENERAL. The following circuit descriptions are presented in much the same order as that taken by a signal, beginning with the input circuits. For convenience in maintenance, the components in each circuit group are numbered in the same series, as shown in the following list:

| Circuit | Tubes and Components No. | Schematic Diagram |
|---|---|---|
| Input Circuits | 100's | Figure 5.1 |
| Delay Circuits | 200's | Figure 5.2 |
| Sweep Circuits | 300's | Figure 5.3 |
| Pulse-Timing Circuits | 400's | Figure 5.4 |
| Pulse-Generating Circuits | 500's | Figure 5.5 |
| Power Supply | 600's | Figure 5.6 |

4.2 INPUT CIRCUITS. (See Figure 5.1.) The trigger circuit consisting of dc amplifier V101A and Schmitt circuit V102 produces the brief direct trigger pulse, and maintains its slope and amplitude constant irrespective of the rate of change of input voltage at the PRF DRIVE terminals. The amplifier V101A is connected to the PRF DRIVE binding post through blocking capacitor C111 and the symmetrical limiter circuit R101, D102, and D103. For dc operation, C111 is shorted out by S101. V101A serves as a d-c amplifier for the Schmitt circuit, V102. If V102A is in conduction, its plate current will maintain the cathode voltage for both sides at about 95 volts. If the plate voltage of V101A is below 90 volts, the circuit is stable and V102A remains in conduction. Now suppose the plate voltage of V101A is increased until V102B begins to conduct. The decreasing plate voltage of V102B reduces grid voltage on V102A and therefore reduces the cathode voltage, making V102B conduct even more heavily. This positive feedback quickly turns V102A off and V102B on. When the plate voltage of V101A is again reduced to below 95 volts, V102A is sufficiently below its cutoff voltage so that the grid voltage of V102B must be reduced to below 90 volts before V102 switches back to the original state. Therefore the circuit exhibits a hysteresis effect.

The bias establishing the quiescent plate current for V101A is normally set in the center of this hysteresis loop. A positive-going voltage at the grid of V101 is amplified and swings V102B into its regenerative region, turning it off and producing a positive transition at its plate. The TRIGGER SELECTOR switch is shown in the positive-going position, so that this wave front is differentiated by C103 and R112 to a positive trigger that momentarily switches V103A on.

R103 and R104 control the bias on V101A, establishing the center of the hysteresis loop. An adjustment of R103, the TRIGGERING LEVEL control, can:

a. permit V102 to switch on either a small positive or a negative input pulse. (Note that in the optimum sensitivity adjustment, the a-c component of a brief input pulse may not be adequate to cause the hysteresis loop to be traversed.)

b. optimize the sensitivity of the trigger for small signal inputs. (This is the normal setting.)

c. select an exact voltage at which V102 will switch, thus permitting the exact sensing of zero crossing for large signals.

The pentode section of V103 is turned on by the positive trigger generated by the Schmitt circuit on the selected zero crossing, either positive- or negative-going. A network in the plate of V103A produces the 0.10-μsec, 20-volt negative direct trigger. A longer-duration negative trigger of somewhat higher amplitude, developed across L101 and R113, is capacitively coupled through the 0.2-μsec delay line DL101 to the grid of V103B. V103B is normally conducting at zero bias, and, when turned off by the negative trigger, produces a 100-volt positive sync, about 1 μsec in duration, which is fed to V104A, a cathode follower capacitively coupled to the DIRECT SYNC OUT terminals. DL101 provides a 0.2-μsec time delay in the direct sync channel. The total delay accumulated between the PRF DRIVE and DIRECT SYNC OUT terminals is about 0.4 μsec. This delay permits the delay and sweep circuits to be precisely calibrated at their minimum values.

4.3 DELAY CIRCUITS.

4.3.1 GENERAL. For convenience, the delay circuits can be divided into two groups; the main delay circuit, across the top of Figure 5.2, and the coincidence circuit system, the line of circuits at the bottom of Figure 5.2. Idealized waveforms are shown in the time diagram accompanying the block diagram for these circuits (Figure 1.4).

The main delay circuit is a loop with a monostable characteristic. The loop action is started by the direct trigger, which opens a bistable gate and starts a sweep circuit. When the sweep voltage equals the d-c voltage set by the TIME DELAY MICROSECONDS control, the amplitude comparator circuit switches, generating a trigger. The trigger is amplified and resets the bistable gate, ending the sweep. The loop then remains quiescent until another direct trigger is received. Since the delay sweep lasts from 1 μsec (minimum) to one second (maximum), the circuits up to the amplitude comparator are direct coupled.

4.3.2 DELAY GATE. The delay gate is a bistable circuit. One gate tube (V201) is normally on, the other (V202) normally off. The supply voltage for the gate is +55 volts and -150 volts with respect to ground; therefore the plate potential of the conducting gate tube is negative with respect to ground by about 15 volts. The gate is opened by the negative direct trigger from the input circuit, and switches regeneratively to turn V201 off and V202 on. The fall in voltage at the plate of V202 turns V203 off and starts the sweep.

4.3.3 DELAY SWEEP GENERATOR. V203 is normally in conduction, with its grid slightly positive. Plate load resistors, ranging from 500 kilohms to five megohms, selected by the DELAY RANGE switch, drop almost the entire power-supply voltage at the plate of V203 when it is on. When V203 goes off, the timing capacitor appropriate to the delay range charges through the selected resistor. Thus the delay sweep is a portion of the exponential voltage produced by the charging of a capacitor through its associated resistor toward the supply voltage. The slope is correctly set for the selected range by a potentiometer, for all ranges except one. R232 provides an adjustable step of initial plate voltage on the 1-sec range to compensate for the lower starting plate voltage due to the five-megohm charging resistor on this range. R283 provides a step to speed up the beginning of the 1-10-$\mu$sec range to overcome the effects of stray capacitance, while on the same range C222 provides an adjustment to permit exact duplication of capacitance in the presence of strays for each instrument. The rising exponential voltage produced by the switching action of V203 is coupled by a cathode follower (V204A) to the grid (pin 2) of V205A, the delay amplitude comparator.

4.3.4 DELAY AMPLITUDE COMPARATOR. V205 is a Schmitt amplitude-comparison circuit. A d-c reference voltage, established by the DELAY MICROSECONDS control, is used to translate its triggering d-c level from a minimum of about 15 volts over a hundred-volt span. When the DELAY MICROSECONDS control is set at mimimum, the sweep must rise only about 10 volts before the amplitude comparator triggers; however, with the control at maximum, the voltage must rise to over 100 volts. The minimum and maximum voltages are set by R236 and R238 to give the correct delay readings on the 10-$\mu$sec-100-$\mu$sec range. Obviously, if the delay sweep were linear and if the voltage established by the DELAY MICROSECONDS control were linear as a function of angle, the DELAY dial reading would be linear. It is apparent that the delaying sweep is not linear, being one third of a complete exponential change curve at its maximum value. Due to the current drawn by V205 and R219 from the arm of the delay potentiometer R237, the change in voltage with angle is nonlinear and closely matches the exponential, resulting in a linear delay scale.

4.3.5 DELAY RESET TRIGGER STAGE. After the lapse of time determined by the sweep and the amplitude-comparison reference voltage, V205 triggers, the left side goes on and the right side goes off. The regenerative rise in voltage at the right-hand plate of V205 causes V204B, the reset trigger amplifier, to conduct, producing a negative trigger, which is fed to the grid of V202, turning V202 off and terminating the sweep. This reset pulse is also fed through C234 to start the coincidence gate. The monostable character of the main delay loop should now be apparent. If, for some reason, the delay reset trigger produced by the amplitude comparator fails to reach and reset the gate, no second trigger can be produced by the amplitude comparator, and the sweep voltage will rise to a maximum value set by the grid current in V204A. The loop will be quiescent in this "locked out" position. The action of the circuit can then be initiated only by artificial reset trigger injected at the grid of V202. This is done by means of the RESET switch, S202, which momentarily removes the bias from V204B, producing the negative pulse to restore the loop to its normal state. The circumstances under which the "lock out" conditions usually occur are:

a. upon warmup, if V202 comes on first. (This can be permanently remedied by reversal of V201 and V202.)

b. when the delay circuit is used as a frequency divider and/or when the delay control is set to produce a delay nearly equal to the input period.

## 4.4 COINCIDENCE CIRCUITS.

4.4.1 GENERAL. The 3-1000-$\mu$sec monostable gate is opened by the negative delay reset trigger. In normal operation the positive early transition of this gate turns on the coincidence amplifier.

The pulse of plate current of the coincidence amplifier is inverted by T201 to drive the delay trigger generator stage into conduction. The delay trigger generator develops the delayed trigger in an inductor-diode pulse-forming network in its plate. This circuit, the following pulse amplifier, and cathode follower are identical in design to the equivalent circuits of the input system explained in paragraph 4.2. The delayed trigger is fed to one side of the SWEEP TRIGGER switch (S203), and the direct trigger to the other. Operation of this switch causes the sweep to be started by either the delayed or the direct trigger.

When the coincidence system is to be used for time selection as described in paragraph 1.3.3, the sum of the 3-1000-$\mu$sec gate from V206 and an input pulse from J201 (POS) or J205 (NEG) is required to turn the coincidence amplifier stage on. The coincidence amplifier bias is increased as the COINCIDENCE SENSITIVITY control (R256) is turned counterclockwise. The 3-1000-$\mu$sec gate alone can not switch V207A into conduction when the sensitivity is reduced. The combination of the gate and positive pulses at the junction of R289 and R290 will switch V207A on and produce the delayed synchronizing signal.

4.4.2 COINCIDENCE GATE CIRCUIT. The right-hand side of the 3-1000-$\mu$sec monostable gate, V206B, is normally conducting with its cathode near -80 volts and its grid slightly positive with respect to cathode. The plate current of this tube, flowing through R256, R257, and R249 to ground, produces a bias voltage, which normally keeps the left-hand side of V206A off. With this tube off, its cathode is slightly negative with respect to ground because of the forward drop of D205. The negative delay reset trigger starts the regenerative action of the monostable gate, during which the right-hand side of V206B goes off, turning the left-hand side on. After switching, the grid of the left-hand side is at ground potential and its cathode is slightly positive with respect to ground; thus D205 is a high resistance, and R251 is a feedback resistor, which stabilizes the plate current of V206-left. The "off" time of V206-left depends on its plate swing and the r-c time constant controlled primarily by C235, R254, and R255. The "off" time of V206-right is controlled as R253 varies the plate swing. C253 and R288 alter the initial shape of the timing grid waveform for V206-right to permit smooth timing down to 3 microseconds. When the timing r-c combination has discharged enough for the right-hand tube again to go into conduction, its plate voltage begins to fall, lowering the grid voltage on the right-hand side, and the circuit regenerates and returns to its original stable state, terminating the gate. The gate is directly coupled to the grid of the coincidence amplifier through R289. The resistive adder is compensated by C254.

4.4.3 COINCIDENCE AMPLIFIER. When the 3-1000-$\mu$sec gate is off, grid 2 of V207A is about -10 volts; while it is on, the grid is near ground potential. R265 in the cathode of V207A is the COINCIDENCE SENSITIVITY control, producing from 3 to 33 volts of additional bias for this stage. In the NORMAL position, the 3 volts of bias alone will not hold the stage in cutoff when its grid rises to ground. When the COINCIDENCE SENSITIVITY control is moved counterclockwise away from the NORMAL position, the circuit is prepared for coincidence operation. During coincidence operation, the same rapid rise of plate current in V207A as that produced by the early transition of the 3-1000-$\mu$sec gate must be obtained; thus fast triggers are necessary to operate the coincidence circuit. Their duration is relatively unimportant but their rise time should exceed 0.2 $\mu$sec over a 5-volt interval.

4.4.4 DELAY TRIGGER AND SYNC GENERATORS. The network in the plate of V208A shapes the negative delayed trigger. This pulse is amplified and inverted in V208B to form a positive sync applied to V207B, the cathode-follower output stage. The presence of the delayed sync at the output terminal is indicated by a stage comprising half of V104B. The positive delayed synchronizing pulse causes this stage to draw grid current, charging C251. The discharge of C251 through R279 in the time between pulses keeps V104B off and causes V209, the DELAY MONITOR lamp, to light.

## 4.5 SWEEP CIRCUITS.

4.5.1 GENERAL. The sweep circuits consist of a bistable control multivibrator, sweep generator, amplitude comparator, and reset trigger amplifier. This loop is identical in configuration to that in the delay circuits. The only difference is that the sweep is generated by a bootstrap-type sweep circuit, which produces a linearly rising sawtooth rather than the simple exponential form produced in the delay circuits. The bootstrap-type sweep generator produces a positive-going, linearly rising sawtooth, which is fed through a cathode follower to the positive sweep output terminals, and from this cathode follower through an amplifier inverter to a negative-output cathode follower for the negative phase. Also, a single-tube amplifier-inverter stage is provided to produce negative and positive gates during the sweep time.

4.5.2 SWEEP CONTROL GATE AND SWEEP GENERATOR. The sweep gate multivibrator comprises V301 and V302 and their associated components. The low plate voltage of V301, which is normally on, keeps V302 beyond cutoff. The plate voltage of V302 is very nearly equal to the positive power supply voltage (55 volts). Therefore, both V303, the sweep generator, and V309, the keyed clamp, are in conduction.

When a negative sweep trigger is received, V301 is turned off and the resulting regenerative action causes V302 to switch on rapidly. When V302 comes on, V303 and V309 are turned off, and the sweep is started. Sweep timing is controlled by the r-c networks in the plate circuit of V303. Resistance is controlled by S301, the SWEEP DURATION switch. Capacitance is controlled by the SWEEP MULTIPLIER switch, S302. In Figure 5.3, the SWEEP MULTIPLIER switch is shown set to 1, the SWEEP DURATION switch to 3 $\mu$sec. Thus the sweep-timing r-c network is C321, R323, and R329. Initially, with V303 in zero-bias conduction, its plate voltage is very nearly at ground. The voltage at grid 2 of V304A is low and its cathode voltage is only slightly positive with respect to the grid. When V303 goes off, the selected sweep-range capacitor begins to charge through its associated resistance network towards +300 volts. The grid voltage of the cathode follower rises and the cathode follows. The cathode resistance of V304 with V309 off is very high, so that the gain of this stage as a cathode follower approaches unity. The rising cathode voltage is coupled through C330 and drives the cathode of D303 positive. D303 opens, and the plate-timing networks for V303 are carried up along with the cathode of V304. If the gain of V304 were exactly unity, a rise of 1 volt at the grid of V304 would cause the same rise at the cathode of V304 and an equivalent increase in B-plus, and the current through the timing resistor would be constant. If this happened, the sweep would be ideally linear. The small departures of the sweep with linearity are due to small departures from a cathode-follower gain of unity. A very large resistance is thus needed in the cathode of V304 during the active portion of this cycle. The linearly rising sweep voltage always attains an amplitude of about 140 volts at the grid of V306, the sweep amplitude comparator. The d-c reference voltage for this stage is fixed to establish the correct sweep amplitude. When the sweep has attained the 140-volt amplitude, V306 triggers, producing a voltage rise at the plate. This causes V305A to conduct, producing the negative reset trigger that turns V302 off and V301 on. The sweep gate is now reset to its normal condition. The sweep generator is brought back into conduction, the keyed clamp is turned on, and the sweep-timing capacitor is discharged. The conducting sweep generator can quickly reduce the voltage across the sweep-timing capacitor to a small value, but the voltage at the cathode of the cathode follower, V304, must be reduced by the discharge of strays and by the replacement of charge on the bootstrap coupling capacitor (C330) by V309. To increase recovery time, this voltage must be brought back to its quiescent value as quickly as possible; therefore, the plate current of V309 is increased during the discharge period by V307A, the reset cathode follower. The grid of V307A is driven positive by differentiation of the negative sweep voltage at V308B. This voltage spike causes V307 to conduct, and momentarily increases the screen voltage on V309, increasing its plate current during the discharge interval.

The positive sweep at the cathode of V304 is connected to the pulse-timing amplitude comparators to provide timing triggers to start and stop the main pulse. V308A is the output cathode follower for the positive sweep phase. Part of the positive sweep voltage from the cathode of V308 is amplified and inverted by V307B, producing the negative sweep fed to the SWEEP NEG output terminals through cathode follower V308B.

The trailing edge of the negative sweep drives the grid of V310B through C331 to cause the spike of positive voltage at the grid of V310. Grid current charges C331, and the discharge of C331 through R369 cuts V310B off. The rise in plate voltage of V310B ionizes the SWEEP MONITOR lamp V311 and indicates the presence of the sweep at the output terminal.

The grid of V305B is directly connected to the plate of V301 and is thus positive during sweep time. The positive sweep gate is present at the cathode, and an equal negative gate is present at the plate. This push-pull gate waveform is connected through 1-$\mu f$ coupling capacitors C339 and C338 to the GATE output terminals on the panel.

4.5.3 SWEEP RESET SYSTEM AND SWEEP PROTECTIVE CIRCUIT. The sweep-generating loop has the same monostable characteristic as the delay generating loop; that is, when the gate is opened by the sweep trigger, the sweep rises until the amplitude comparator triggers and feeds back a stop trigger to close the gate. If, because of rapid warmup of V302 or simultaneous triggering of both sides of the sweep gate, the sweep fails to reset, this loop will come to an equilibrium condition, where the sweep voltage is high and the sweep amplitude comparator is stable and "locked out". Under these conditions, an artificial reset trigger must be given the sweep control gate multivibrator. This is accomplished by the momentary grounding of the cathodes of V301 and V302 through the RESET switch S202, which causes the sweep gate to reverse its state.

In case of a "lock out" or a failure of V303, V304 will drive the grid of V308A to a high positive value, and the cathode resistors of V308 will be damaged. If V303 fails with V309 conducting, a high current could be drawn through V304 and V309 in series, damaging these tubes. Because of these possibilities, the cathode voltage of V304 must be prevented from remaining in a highly positive condition for a very long time. Protection is afforded by a system in which a network consisting of R319, C337, and R320 establishes a grid voltage normally negative on V310A. If the sweep circuit fails to reset, C337 charges to a voltage sufficiently positive to cause V310 to conduct. When V310 conducts it decreases the grid voltage of V304 and lowers the cathode voltage sufficiently to protect all tubes and components.

**4.6 PULSE-TIMING CIRCUITS.** The pulse is normally timed by start and stop triggers produced by amplitude comparators V401 and V402 (see Figure 5.4). These comparison circuits are provided with d-c reference voltages derived from bleeders in the 300-volt regulated supply. A calibrated voltage along R409 supplies V401, the start comparator, while an equivalent voltage from R410 supplies the stop comparator, V402. The rising sweep voltage from V304 is connected through precision attenuators to the left-hand grids of V401 and V402, and these stages trigger in turn as the sweep voltage rises to become equal to the reference voltages. Since the sweep is linear, it is necessary that the amplitude comparators draw a constant current from the reference voltage potentiometer. Hence, both the plate and cathode of the comparator circuit are connected to ganged potentiometers, maintaining the supply potential for the comparators constant regardless of the potentiometer setting. The amplitude comparison take-off voltages are calibrated at both the minimum and maximum voltages for both the PULSE DELAY and DURATION controls by R407, R408, R411, and R412. A small amount of unregulated power-supply voltage is fed across the amplitude comparison voltage pickoff network through R428 and R429. This connection causes a minute variation in the d-c amplitude comparison potentials with line voltage, and serves to compensate for small shifts of pulse position due to line-voltage (and therefore heater-potential) changes. As an example of the operation of two amplitude comparators (see Figure 1.6b), suppose the input sweep voltage is 120 volts in amplitude and that the sweep duration is 3 $\mu$sec. Also, suppose it is desired to start the output pulse with 1 $\mu$sec of delay from the leading edge of the sweep and with a 1-$\mu$sec duration. Under these circumstances, the PULSE DELAY control will be set at a potential of 40 volts and the PULSE DURATION control 40 volts above the PULSE DELAY control, or at a potential of 80 volts. The start amplitude comparator would then trigger one-third of the way along the sweep at 1-$\mu$sec, and the stop amplitude comparator two-thirds of the way along the sweep at 2 $\mu$sec, resulting in a time between triggers produced by these two circuits of 1 $\mu$sec, the desired pulse duration.

V401 and V402 are Schmitt circuit amplitude comparators similar in form to the equivalent comparators of the delay and sweep circuits. The left-hand section of each tube is normally off, the right-hand section on. When the rising sweep voltage reaches the critical level at which the left-hand side will conduct, the circuit regenerates, turning the right-hand side off and producing a fast-rising positive trigger. This positive trigger is coupled in the start channel via C403 and R421 to the start-channel half of S401, and applied to the grid of buffer tube V403. The resulting negative pulse at the plate of V403 is inverted by T401 and further amplified and shaped by V405, the start amplifier, to a fast negative pulse. This pulse flips V501 over to initiate the pulse. The function of S401 has been described in Section 1. Note that the positive trigger pulse marking the beginning of the pulse is produced across R427 by the plate current of V405, and connected via S401 to the START binding post. The circuit action and connections of V404 and V406, the stop-channel buffer and amplifier, are identical with those of the start channel.

## 4.7 PULSE-GENERATING CIRCUITS.

4.7.1 GENERAL. The pulse-generating circuits consist of a bistable multivibrator, identical to those in the sweep and delay circuits. This multivibrator is started and stopped by the triggers derived from the pulse-timing circuits or by externally generated triggers. The bistable multivibrator controls the state of a bistable push-pull pulse amplifier consisting of two power amplifier pentodes, which in turn are directly coupled to a pair of driver amplifiers. These amplifiers drive the output-pulse power output stage. Since the system is both push-pull and direct coupled throughout, the entire circuit is bistable, and the current drawn from all power supplies is constant. The fact that the output-power amplifier is itself direct coupled to the panel terminals necessitates the use of a number of different power-supply voltages. These voltages are all unregulated, so there would normally be a variation in pulse amplitude with line voltage; however, V511 regulates the screen-to-cathode potential of the output tubes to decrease the effects of line-voltage variation.

4.7.2 The right-hand side of V501 is normally in conduction so that its plate voltage is about +140 volts with respect to ground. This voltage is translated negative 100 volts by the current flowing in V502, so V501-left is in plate-current cutoff. Since V501-left is off, the grid of driver V503 is positive and V503 is on.

When on, V503 draws about 60 ma, producing a drop of 36 volts across R507 and R545. The plate voltage of V503 is translated negative by the current flowing in V509-left, and driver V505 is held in cutoff. Since amplifier V504 is off, the translated plate voltage of this stage due to plate current in V509-right causes V506 to conduct. The plate current of V506 through R528 and R530 holds the grid of output tube V508 about 25 volts negative with respect to its cathode, and this tube is off. Since V505 is off, V507 will be at zero bias and conducting. These are the quiescent conditions before a start pulse is fed via D501 to turn V501-left on. When this happens, all tubes on both sides reverse their conduction states. Thus V507 will be turned off and V508 will go on to produce a negative pulse. DC connections throughout cause the entire system to be bistable.

With the pulse amplitude switch set for a maximum, output tubes V507 and V508 conduct about 160 ma of plate current. Voltage produced by this current in R548 through R557 constitutes the output pulse. Negative pulses are, for example, produced when the plate current of V508 is turned on in R548 (50 ohms) to produce -7.5 volts with respect to ground (J507) behind 50 ohms. S501 controls output impedance, and consequently output voltage. Note that the link between J507 and J508 can be opened to insert a battery or dc power supply to translate the dc component of the pulse away from ground.

When V507 and V508 are conducting with full screen voltage (maximum pulse amplitude), about 100 ma of the current in the "on" output tube flows through the "on" driver tube. Under "normal" conditions there will be 160 ma in V507 and 100 ma in V506. The additional 60 ma flows in R537.

If pulse amplitude is decreased, means must be provided for maintaining plate voltage on the driver tubes (normally maintained by conduction of the output tubes). Therefore, as the PULSE AMPLITUDE switch setting is decreased, resistors R567 through R575 are switched in from ground to cathodes of V507 and V508, reducing screen voltages and thereby maintaining plate voltages.

Pulse amplitude is reduced by reduction of the screen voltage of the output stage. The screen resistance (R558 through R566) for V507 and V508 is increased to decrease screen voltage. The pulse current is stabilized against line variations and transients by V511, which controls the screen voltage supplied to the amplitude control network. V511 is essentially a cathode follower, whose grid voltage is supplied by the network consisting of R578, R579, V512, V513, and V514 with this network between +300 volts regulated and -550 volts. Suppose, for example, that the line voltage decreases. The -200 volt supply feeding the cathodes of V507 and V508 becomes less negative and the screen voltage on these stages tends to decrease, decreasing plate current. Actually the -550-volt supply becomes less negative by an amount which, when referred to the cathode of V511, exactly equals the change in cathode voltage on V507 and V508. Thus the plate current at these stages tends to remain constant, and is, in fact, affected only by changes in heater voltage.

## 4.8 POWER SUPPLIES.

4.8.1 GENERAL. All necessary power supplies are in the Type 1391-P2 Power Supply Unit. This supply provides the four 6.3-volt heater supplies and the nine d-c power supplies required. One 10-conductor cable carries the four heater pairs and the 115-volt conductors required to operate the blower. The four heaters are identified by the letters P for positive, A for amplitude comparator, G for ground, and N for negative. The A bus is a shielded, low-noise winding that provides heater voltage for the various amplitude comparators of the input, delay, sweep, and pulse-timing circuits. The ground bus is a heater winding at ground potential for tubes whose cathodes are close to ground, and the N bus supplies those tubes whose heaters normally run at 150 to 200 volts negative. The heater connection of each tube is identified by the key letter printed on the heater terminals of that tube in the circuit diagrams, Figures 5.1 through 5.6.

4.8.2 PLATE SUPPLIES.

4.8.2.1 General. All supplies use silicon rectifier circuits. Those providing appreciable power are full-wave doublers, while the low-drain bias supplies are half-wave rectifiers. The plate supplies, in the order shown from top to bottom of the elementary diagram on the back of Figure 5.6, are:

a. a 110-volt 200-ma doubler supply added to a 300-volt doubler supply to produce +410 volts unregulated. This supply provides plate voltage for the +300-volt regulator.

b. a second 300-volt doubler providing +140 volts for V503 and V504 in the pulse-generating section and +55 and -150 volts for the bistable gate circuits.

c. a -200-volt doubler for the pulse output stage.

d. a half-wave rectifier supplying additional 340-v bias to V509 for the pulse output stage and pulse amplitude regulator.

4.8.2.2 Regulator. A Type 6AS6 series tube (V601) is biased to the proper operating point to produce a 300-volt output by means of the plate current of V602 flowing through R605. The level of this plate current is controlled by the grid voltage on V602, controlled by R612. R612 therefore determines the regulated output voltage. The 150-volt reference voltage for the cathode of V602 is produced by V603. Some unregulated voltage from the 410-volt supply is developed across R607 and is added to the grid network of V602. This provides compensation for changing input voltage. When the output voltage tends to rise due to an increase in line voltage, the grid voltage on V602 increases, increasing the bias on V601 and lowering the output voltage. This compensation produces a negative slope of output voltage with increasing line voltage over the range from 100 to 130 volts. From 105 to 125 volts, the output voltage from the supply changes by less than one-half volt.

# Section 5
# SERVICE AND MAINTENANCE

5.1 GENERAL. The two-year warranty given with every General Radio instrument attests the quality of materials and workmanship in our products. When difficulties do occur, our service engineers will assist in any way possible.

In case of difficulties that cannot be eliminated by the use of these service instructions, please write or phone our Service Department, giving full information of the trouble and of steps taken to remedy it. Be sure to mention the serial and type numbers of the instrument.

Before returning an instrument to General Radio for service, please write to our Service Department or nearest district office (see back cover), requesting a Returned Material Tag. Use of this tag will insure proper handling and identification. For instruments not covered by the warranty, a purchase order should be forwarded to avoid unnecessary delay.

## 5.2 SERVICE.

5.2.1 GENERAL. The Type 1391-B Pulse, Source, and Time-Delay Generator is designed for easy servicing. There are many front-panel connections to the circuits, and test points are provided for oscillographic presentation of stage performance wherever there is no panel connection for the stage. The following notes are based on signal-tracing methods in order of increasing difficulty in required measurements. First isolate the trouble by front-panel observation, using an oscilloscope. Then use Table 5.2 and paragraph 5.2.2 to isolate the defective stage or stages.

Troubles in operation can be divided into two classes: faulty or erroneous operation of a circuit (or perhaps of one range of one circuit), and complete failure of a group of circuits or of the whole system. Troubles in the first category are obviously easy to remedy. Faulty or erroneous operation of one range alone points to the components actually switched on in that range. Faulty operation on all ranges of a multirange circuit usually points to fixed components, tubes, a power supply common to that circuit, etc. Such trouble can usually be remedied by direct investigation of the tubes or components involved and reference to the service data on waveforms and voltages.

CAUTION

When replacing a component on an etched board, be careful not to destroy the bond between board and etched wiring by heat or by force. When removing the defective component, firmly grab the wire at the component side (the component may be clipped off first), and then, pulling on the wire, apply just enough heat to the solder to free it. Before inserting the new component, make certain that an unobstructed passage exists, either by carefully drilling through the component side or by removing the solder from the hole. When using the soldering iron to remove solder, draw the solder back along the conductor from the tab with quick strokes. Never apply the soldering iron to the etched board for more than five seconds at a time.

If the position of the board prohibits the above procedure, many components can be replaced as follows: destroy the old component, preserving enough wire to attach the replacement, then solder the new component in place.

5.2.2 ISOLATION OF TROUBLES.

5.2.2.1 General. Set all controls to the standard positions listed in paragraph 2.3. Be sure that the power is on and that all cables are plugged in on the rear panels of power supply and main unit. Also be certain, by measurement at the PRF DRIVE terminals, that an adequate signal (1 to 10 volts) is present.

Using Table 5.2, observe output signals and monitor lamps to determine which signals are missing or not functioning properly. The 13 columns of signals and indications of signals present (P) or absent (A) will isolate the circuit action at fault. After finding the defective section, use an oscilloscope to observe the waveforms at the test points of the defective section. Proceed in order of increasing numerical value through the circuit to isolate the defective stage. Then measure voltages and check them against Table 5.3.

5.2.2.2 All Signals Absent and Indicators Do Not Light. This is an indication that the defect is either in the input circuit generating the direct trigger (V101A, V102, or V103A), or else is a failure of the power supply feeding these stages. Either possibility can be checked first. Remove the cover and left side pan of the instrument. Voltages can be checked at input power plugs or at the rear skirt of the instrument. (See Figure 5.5.)

5.2.2.3 Direct Sync Present, DELAY MONITOR Lamp Lights Only When Direct Sync Pulse is Connected to POS COINC DRIVE Terminals. This indicates that neither sweep control multivibrator will operate. The only common connections between the circuits are the +55 -150, and -200-volt power supplies. Check the +55 and -150-volt supplies first. The -200-volt supply provides the bias for the direct trigger pulse amplifier. Failure of this supply could cause the trigger amplitude to decrease enough to cause failure of the control multivibrator. Check the direct trigger amplitude (at AT205) if the -150- and +55-volt supplies are satisfactory.

5.2.2.4 Direct Sync Pulse Absent or Low, Balance of Instrument Functions Properly. This symptom points to a weak tube or defective component in the direct sync output circuit. Check the direct sync amplifier tubes V103B and V104A and components.

5.2.2.5 Delay Circuit Does Not Function When RESET Switch is Flipped. Determine whether it is the coincidence-gate circuit, the main delay group, or the output circuit that has failed. Remove the cover of the instrument and check for the presence of a positive delay gate at TP201 (flip RESET switch after connecting oscilloscope). If the gate exists there, the difficulty is in V206 (coincidence gate monostable) or its associated components. As a first check, make sure that the delay reset pulse has the correct amplitude by checking the pulse from TP203 against Figure 5.7.

Since the main delay circuit is a feedback loop in which all circuits (V201 through V205) must be functioning, a special procedure can be used to isolate the defective component. (Refer to paragraph 5.3.1.)

5.2.2.6 No Delay Sync Pulse Present When Direct Sync Pulse Is Connected to POS COINC DRIVE Terminals. Throw the SWEEP TRIGGER switch to DELAYED. If the sweep circuit does not start, the difficulty is in the delay sync amplifier (V208B) or cathode follower (V207B) or their components.

5.2.2.7 Delay and Direct Triggers Normal; Sweeps, Gates and Pulses Missing. This indicates that the sweep loop (V301, V302, V303, V304, V309, V305A, and V306) is defective. Since the reset pulse must be present to reset the bistable gate, the loop can "lock out", as can the delay circuit. Troubles are most easily isolated by means of the special procedure outlined in paragraph 5.3.

5.2.2.8 Defective or Missing Negative Sweep Only. Check V307B, V308B, and their components. If only the SWEEP MONITOR lamp functions, check V310B and associated components.

5.2.2.9 No Main Pulse, No Output Pulse From START Trigger Terminal When PULSE START STOP TRIGGER Switch is in INTERNAL (NORMAL) Position. This indicates a failure in the start channel (V401, V403, or V405). First look for the positive start trigger at TP401 shown in Figure 5.7. If the trigger exists, the trouble must be in V403, V405, or associated components.

5.2.2.10 No Main Pulse, No Output Pulse From STOP Trigger Terminal When PULSE START STOP TRIGGER Switch is in INTERNAL (NORMAL) Position. This indicates failure in V402, V404, or V406. First check TP402 for the positive stop trigger as shown in Figure 5.7. If the trigger exists, the difficulty is with V404 or V406.

5.2.2.11 No Main Pulse, Both Start and Stop Triggers Present When PULSE START STOP TRIGGER Switch is in INTERNAL (NORMAL) Position. This usually indicates a failure in the pulse source itself. First check the operation of V404 and V405 by checking their waveforms at TP403 and TP404. If these pulses are as shown in Figure 5.7, proceed to a detailed check of the pulse source (paragraph 5.3.2).

5.2.2.12 All Signals Present Except Sweep Gate. Since the sweep gate output system consists only of a simple pulse-splitter from the sweep-gate bistable multivibrator, which must be operated to produce the sweep, the trouble can only be in V305B or associated components.

5.2.2.13 Negative Sweep and Positive Sweep Both Missing, Pulse-Timing Circuit Normal. The only circuit common to both negative and positive sweep phases after the pulse-timing sweep is taken out is that of V308A and its associated components. Check this circuit.

## 5.3 SPECIAL TECHNIQUES FOR TROUBLE-SHOOTING DELAY, SWEEP, AND PULSE-TIMING CIRCUITS.

The possible bistable characteristic of the delay and sweep loops when a failure occurs, and the definite bistable characteristic of the pulse generator make trouble-shooting these circuits somewhat more complex than the straightforward signal-tracing techniques that suffice for the other circuits. Paragraph 5.3.1 below outlines the techniques for the sweep and delay circuits, and paragraph 5.3.2 that for the pulse generator.

5.3.1 DELAY AND SWEEP LOOP TROUBLE-SHOOTING. Assume that the delay reset pulse amplifier V204B should fail by burnout. The first direct trigger received by V201 of the bistable control circuit upon warmup will flip V202 on and cut off V203. The delay sweep will rise and cause V205 to switch to generate the driving pulse for V204B, which cannot produce the reset pulse. The loop is now stable, with V201 off, V202 on, V203 off, V204A in grid current, V205A on, and V205B off. The same condition could obviously be caused by a defective V204, V205, etc.

Several procedures can be used to isolate the defective components. Since it is probable that the failure is caused by a weak or failed vacuum tube, it would be advisable to replace tubes, one by one, with tubes known to be good. Voltages can, of course, be measured and checked against those given in Table 5.3, after making sure of the state of the delay gate (V201 on, V202 off).

The following is a rapid and effective means of locating difficulties in each loop:

a. Connect an oscilloscope set for d-c operation to TP201 (or POS GATE).

b. Set DELAY (or SWEEP) RANGE switch to the longest range, 1 second (120,000 $\mu$sec sweep range).

c. Connect a low-frequency (10-20 cps) source to the PRF DRIVE terminals.

d. Now flip the RESET switch. V201 (301) should go on and be turned back off by the next low-frequency direct trigger. If V201 or V301 does not switch on, the control bistable gate is defective. The defect can be remedied either by tube replacement or voltage measurement. In the delay circuit, the manual reset pulse is actually produced by the momentary grounding of the cathode of V204B by a discharged capacitor (C221); so that if the delay circuit is involved, V204 and its associated components must also be suspect. If the delay circuit fails to change state, produce a reset pulse by touching a grounded, discharged 100-$\mu\mu$f capacitor on TP203. This will produce a negative pulse to turn V202 off. If the bistable switches when this is done, V204B or one of its components is faulty.

If the bistable gate of the defective circuit is functioning, the trouble can easily be located by the substitution of a reset pulse for that of the defective loop. The procedure is as follows:

(1) Delay Circuit: The falling edge of the positive output is substituted for the missing reset pulse.

(a) Set the SWEEP TRIGGER switch to DIRECT so that the sweep and delay circuits are started simultaneously.

(b) Set up a 10-kc repetition rate, set the DELAY RANGE control to 10-100 $\mu$sec, and set the sweep and pulse controls to produce a 50-$\mu$sec pulse on the 60-$\mu$sec sweep range.

(c) Connect the PULSE POS output terminal to TP203 (DELAY RESET PULSE) through a jumper and 100-$\mu\mu$f capacitor.

(d) Flip the RESET switch and check for gate waveform at TP202. The delay sweep will reset simultaneously with the trailing edge of the positive pulse, and the delay sweep can now be checked at TP202. If the gate still does not function, test the bistable gate as directed in the beginning of this section.

(2) Sweep Loop: The delay reset pulse can be substituted for the sweep reset pulse by means of a jumper containing a 100-$\mu\mu$f capacitor connected between TP203 and TP305.

(a) Set the SWEEP TRIGGER switch to DIRECT.

(b) Set up a 10-kc repetition rate, set the DELAY controls for 60 $\mu$sec. The sweep will be started by the direct trigger and will stop at the setting of the delay control. Check for the sweep gate at its output terminals.

(c) The sweep can now be traced through TP302-TP305, and the defective stage isolated by signal-tracing methods. In order to check the sweep amplitude selector, V306, the delay control must be advanced beyond 60 $\mu$sec, the point where the sweep amplitude selector should trigger.

e. The following symptoms are possible:

(1) Delay Circuit: The normal condition with the DELAY controls set for maximum is a sawtooth waveform rising to 150 volts, where V204A draws grid current. A steady low voltage at TP202 indicates a defective V203 (grid, cathode, or screen short) on a nonconducting V204. A steady high voltage could be caused either by a defective V203 or an open R234. An open R234 or a grid-cathode short in V205A will produce a voltage at TP202 that varies as the DELAY control setting is varied.

(2) Sweep Circuit: In the sweep circuit, there are two tubes, V303 and V309, that must be turned off by the gate. If V303 fails to go off, the sweep voltage will not rise. If V309 does not shut off, there will be a small step until V304 begins to draw grid current.

5.3.2 TROUBLE-SHOOTING THE PULSE SOURCE. A pulse can be absent for either of two reasons: (1) the control multivibrator is defective, or (2) power-supply voltage is incorrect or missing. Proceed as follows to isolate the difficulty:

a. Having determined that both start and stop pulses are present (paragraph 5.2.2.11), using an oscilloscope, compare the waveforms at TP501 and TP502 with those shown in Figure 5.7.

b. If the multivibrator is operating correctly, place the PULSE START STOP TRIGGER switch in the EXTERNAL OUT position, and, using a 20,000-ohm-per-volt voltmeter (or VTVM), measure the quiescent d-c voltages at the points in Table 5.4. This is a quick check on both tube and power-supply performance. (Voltages given in the table are typical for 115-volt line and should not vary by more than 10 percent.) Note that at TP501 and TP506 the first voltage given is for the normal quiescent position, and the second is the active pulse interval. If the gate is in the pulse-on state (V502 on), then the second voltage listed applies and the voltage states at all succeeding test points and at pulse output terminals will reverse. Any abnormal voltages indicate difficulties that can be remedied by replacement of tubes or components.

5.4 SETUP PROCEDURE FOR THE PULSE DURATION AND POSITION DIAL ASSEMBLY. The following procedure will be necessary only when a potentiometer is replaced or a part of the mechanical assembly is damaged and must be replaced. The object is to adjust the potentiometer blades so that all mechanical stopping action is accomplished by panel stops external to the potentiometers, and so that the DURATION dial can never be set to produce a "negative" pulse duration.

The four potentiometers are R409, R403, R410, and R404, in order from the front panel toward the rear of the instrument (see Figure 5.9). R409 and R403 are the two pulse delay controls, and R410 and R404 are the pulse duration adjustments.

a. Loosen the interlocking collars (A, B, C) between R403 and R410.

b. Connect an ohmmeter between the center and counterclockwise (facing from the panel) terminals of R409 and, by means of the DELAY dial, set the potentiometer to give a reading of between 20 and 100 ohms.

c. Check the synchronization of R403 by connecting the ohmmeter between the center and counterclockwise terminals of R403. The reading should be between 20 and 100 ohms. Adjust, if necessary, by loosening and rotating collar A (Figure 5.9). Retighten collar A.

d. Loosen the set screws (just behind the front panel) that hold the DELAY dial to the shaft, and set the DELAY dial to the etched 2.75-5.50-11.00 point. Tighten the set screws to secure the dial to the shaft, and move the DELAY dial to exactly 0.25-0.5-1.0.

e. By means of the DURATION dial, set R410 to read between 20 and 100 ohms on an ohmmeter connected between its center and counterclockwise terminals. Check R404 for synchronization with R410 by reading the resistance between its center and counterclockwise terminals. Adjust, if necessary, by loosening and rotating the rear collar (D, Figure 5.9) for a reading of between 20 and 100 ohms. Retighten D.

f. Rotate the rear interlocking collar (C, Figure 5.9) against the fixed stop (S) and tighten it to the shaft.

g. Loosen the DURATION dial from the shaft by loosening the set screws on the knob. Then, without disturbing the position of the shaft, set this dial exactly to the 2.5-5.0-10.0 point and tighten the set screws. (Do not disturb the DELAY dial setting; it must be set to the 0.25-0.5-1.0 point.)

h. Without disturbing the DELAY dial setting, move the DURATION dial to its exact zero point. Rotate the front interlocking collar (B, Figure 5.9) counterclockwise until it engages the pin on the rear interlocking collar C. Then tighten collar B to the outer shaft.

i. Check results as follows:

(1) With the DELAY dial exactly at 0.25-0.5-1.00, the DURATION dial can be set to any calibrated point within its range, but cannot be set outside its range in either direction.

(2) With the DELAY dial exactly at 2.75-5.50-11.00, the DURATION delay will indicate exactly zero and will be immovable.

5.5 TROUBLE-SHOOTING CHART. The following is a tabulation of some of the more likely causes of malfunction, together with suggested adjustments and replacements.

TABLE 5.1 TROUBLE-SHOOTING CHART

| | |
|---|---|
| | PULSE |
| a. Ringing | Incorrectly terminated transmission lines, causing stray inductance. 300-ohm twin lead properly terminated produces a clean pulse. |
| b. Overshoot | Improperly adjusted oscilloscope and/or poor termination (see a., above). |
| c. Pulse with two distinct levels. | Incorrect bias supply adjustment (400-v supply) or abnormally low line voltage. Readjust bias voltage by R616 on rear skirt of power supply. Adjust for pulse flatness. Or replace V503 and/or V504. |
| d. Hum on pulse | V505 or V506 weak, or incorrect adjustment of -150, +55-v supply. Adjust R618. |
| e. Ramp-off | Check that oscilloscope has adequate low-frequency response. Check compensation of oscilloscope probe, if one is used. Calculate coupling time constant; it must be at least 10 times as large as pulse transmitted to produce less than 10% rampoff. |
| f. Inadequate rise time | Check typical rise times in Specifications. Remember that system tolerance to stray capacitance decreases as output impedance increases. Check oscilloscope bandwidth, remembering that observed rise time is that given by over-all system response. $T_{obs} = \sqrt{T_{pulse}^2 + T_{sys}^2}$ |
| | SWEEP CIRCUIT |
| g. Positive sweep and pulse timing nonlinear (sweep slope decreases). | Incorrect adjustment of +55-, -150-v supply so that V503 is not completely off. Make -150-v supply more negative or replace V503. |
| h. Negative sweep nonlinear. | Readjust R340 (this might be necessary when V307 is replaced). |
| i. Poor recovery time (over 2 μsec for 3-μsec sweep). | Replace defective V309 or V307. |
| j. V304 weak or defective and R335 and R336 excessively hot. | Check V310, sweep protective tube and circuit, and repair if necessary. To test circuit, pull V303 out of its socket and:<br>(1) Check that plate voltage of V302 is positive with respect to ground. If this voltage is negative, flip the RESET button.<br>(2) With V302 off, measure voltage at TP303. It should be about 125 volts. If it is higher, check V310 and associated circuits. |
| | DELAY CIRCUIT |
| k. Delay nonlinear at top of scale, period longer than dial reading. | Nonlinearity of delay sweep due to:<br>(1) V203 not shutting completely off. Check +55-, -150-v supply and V203.<br>or<br>(2) V204 drawing excessive grid current. Replace tube. |

| | |
|---|---|
| | DELAY CIRCUIT (Cont.) |
| l. Excessive jitter on delay synchronizing pulse. | Check line and noise on +300-v regulated supply. Check V204 and V205 for heater cathode leakage. |
| m. Large drift in delay sync. pulse (over 1:1000) for 10% line change. | Occurs only when V205 is replaced. Replace R219 with value necessary to compensate completely for a line change with DELAY MICROSECONDS dial at a minimum. To establish value, replace R219 with a 200-k resistor in series with a 1-megohm potentiometer and establish correct compensation by inserting resistance for minimum drift as line voltage is varied ±10% from normal. |
| | INPUT CIRCUIT |
| n. Loss of input sensitivity. | V101 weak or R104 incorrectly adjusted. In either case, adjust R104 to restore normal operation. |
| o. Direct trigger amplitude low (less than 5 volts). | Check V103 for grid current by replacing it with a tube known to be good. (V103 can be interchanged with V207.) |
| | POWER SUPPLY |
| CAUTION: Be careful when servicing power supplies. The high-voltage supplies are dangerous. | |
| p. Short circuit in a power-supply component or a burned-out rectifier. | (1) Try to find source of overload with ohmmeter check. The damaged rectifier is easy to find by visual inspection. Refer to rectifier layout in Figure 5.13.<br>(2) Replace the defective components (or component).<br>(3) Then replace the defective rectifier.<br>(4) Carefully test repaired supply by measuring the output voltage at very low input voltages. (If possible, use a Variac® to increase input voltage slowly.) The power supply output should be slightly higher at very low input voltages than the proportional normal voltage. |
| q. Power-supply about half its normal value. | Defective rectifier or half-wave rectifier operation. Replace defective rectifier and then check associated filter capacitor. |
| r. Low output voltage. | Measure voltage across entire input capacitor in doubler supplies, then across each half of doubler. Check (1) electrolytic capacitors and (2) rectifiers associated with low side. |
| s. Burned-out or overheated resistors in filter networks. | Trouble must be isolated to either power-supply filter or main unit. Hence:<br>(1) Break connection at either SO602 or PL401 and insert milliammeter between open connections.<br>(2) Turn on power and gradually increase line voltage, observing current. If current value is too high, repair defective circuit in the main unit. See Table 5.6.<br>(3) If current is still low, check electrolytic capacitors of associated filter. If too high, check associated circuit in main unit. |

| | POWER SUPPLY (Cont.) |
|---|---|
| t. 300-v output not regulated, too high. | Check V602 and V603. Component may be causing V602 to be nonconducting. Check V601 for a grid cathode short. |
| u. 300-v output not regulated, too low. | Check V601 and the +450-v supply. After replacing any tubes in regulator, check output voltage and compensation in accordance with paragraph 3.7.3. |

5.6 TROUBLE-SHOOTING PROCEDURE. Table 5.2 should enable the user to pinpoint the circuit in which the trouble exists. Columns 1 through 13 contain various sets of conditions, in which indications as listed in the left-hand column are either present or absent. Simply determine the vertical column corresponding to the conditions present on the instrument, and refer to the information in the lower part of that column.

TABLE 5.2 TROUBLE-SHOOTING PROCEDURE

(Control settings as listed in paragraph 2.3)

| Initial Test Measurement | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Direct Sync Pulse | A | P | A | P | P | P | P | P | P | P | P | P | P |
| Delay Sync (DELAY MONITOR lamp) | A | A | P | A | A | P | P | P | P | P | P | P | A |
| DELAY MONITOR lamp, Direct Sync at POS COINC DRIVE terminals | A | P | P | P | A | P | P | P | P | P | P | P | A |
| Positive Sweep (SWEEP MONITOR lamp) | A | A | P | P | P | A | P | P | P | P | P | A | P |
| Negative Sweep (SWEEP MONITOR lamp) | A | A | P | P | P | A | A | P | P | P | P | A | P |
| Sweep Gate | A | A | P | P | P | A | P | P | P | P | A | P | P |
| Start Trigger (PSST in INT NORMAL) | A | A | P | P | P | A | P | A | P | P | P | P | P |
| Stop Trigger (PSST in INT NORMAL) | A | A | P | P | P | A | P | P | A | P | P | P | P |
| Main Pulse | A | A | P | P | P | A | P | A | A | A | P | P | P |
| Probable Failure | 300-v (reg or unreg) pwr sup or input circuit (V101, V102, V103) | +55, -150, -190, or -180-v pwr supply; V103 weak | Direct sync out, V103 or V104 | Main delay circuit loop, V201 thru V205, or V206 | Coincidence system V207, V208, V101B, V104B | Sweep Circuit loop | Neg swp output V307, V308, V310 | Start amp comparator V401, V403 V405 | Stop amp comparator V402, V404 V406 | Pulse source | Swp gate amp V305 | Neg and pos swp V308 | Delay sync output V208B, V207B |
| Reference Paragraph | 5.2.2.2 | 5.2.2.3 | 5.2.2.4 | 5.2.2.5 | 5.2.2.6 | 5.2.2.7 | 5.2.2.6 | 5.2.2.9 | 5.2.2.10 | 5.2.2.11 | 5.2.2.12 | 5.2.2.13 | 5.2.2.6 |
| Test Points for systematic check | 101, 102 | | | 201, 202, 203 | 204, 205, 206 | 301, 302, 303, 304 | | 401 | 402 | 403, 404, 501 thru 506 | | | |
| Measure Voltage | 300 (reg, unreg) -190 | +55, -150 heater bus "N" | | | | | | | | at 50-ohm output terminals | | | |
| NOTES | | | | Check V206 first by observing at TP201. | | | | | | Defects in output pulse (Par. 5.4) | | | |

| TUBE (TYPE) | PIN | D-C VOLTS | RES TO GND |
|---|---|---|---|
| V101 | 1 | + 88 | 120k |
| (5965) | 2 | 0 | 10k |
| | 3 | + 3.2 | 8.5k |
| | 6 | +244 | 6.6k |
| | 7 | 0 | 100k |
| | 8 | + 3.2 | 320 |
| V102 | 1 | +300 | 5k |
| (6BQ7) | 2 | + 78 | 37k |
| | 3 | + 90 | 6.8k |
| | 6 | +245 | 3.7k |
| | 7 | + 90 | 120k |
| | 8 | + 90 | 6.8k |
| V103 | 1 | +120 | 10k |
| (6U8) | 2 | - 12.8 | 11k |
| | 3 | +190 | 17k |
| | 6 | +300 | 1.1k |
| | 7 | 0 | 0 |
| | 8 | 0 | 0 |
| | 9 | 0 | 1k |
| V104 | 1 | +300 | 0 |
| (5963) | 2 | 0 | 230k |
| | 3 | + 17 | 10k |
| | 6 | + 48 | 95k |
| | 7 | 0 | 18M |
| | 8 | 0 | 0 |
| V201 | 1 | -120 | 6.8k |
| (6485) | 2 | -110 | 3.3k |
| | 3 | + 40 | 6.8k |
| | 6 | - 55 | 47k |
| | 7 | -110 | 3.3k |
| V202 | 1 | -120 | 6.8k |
| (6485) | 2 | -110 | 3.3k |
| | 3 | + 40 | 6.8k |
| | 6 | - 55 | 47k |
| | 7 | -110 | 3.3k |
| V203 | 1 | + 15 | 107k |
| (6AN5) | 2 | + 17 | 500k |
| | 6 | + 25 | 16k |
| | 7 | + 15 | 1.8k |
| V204 | 1 | + 20 | 22k |
| (6AW8) | 2 | + 17 | 500k |
| | 3 | +300 | 0 |
| | 6 | + 5 | 1k |
| | 7 | 0 | 33k |
| | 8 | +190 | 100k |
| | 9 | +275 | 4.7k |
| V205 | 1 | +270 | 42k |
| (12AX7) | 2 | + 20 | 22k |
| | 3 | + 35 | 7.8k |
| | 6 | +280 | 5.6k |
| | 7 | + 34 | 27k |
| | 8 | + 35 | 7.8k |
| V206 | 1 | +300 | 0.7k |
| (5965) | 2 | - 25 | >3k |
| | 3 | - 0.5 | >0.2k |

| TUBE (TYPE) | PIN | D-C VOLTS | RES TO GND |
|---|---|---|---|
| | 6 | - 33 | 5k |
| | 7 | -100 | >2M |
| | 8 | -100 | 3.3k |
| V207 | 1 | +300 | 0.1k |
| (6U8) | 2 | - 20 | 55k |
| | 3 | +300 | 47k |
| | 6 | +300 | 1k |
| | 7 | + 2.5 | 1k |
| | 8 | + 10 | 10k |
| | 9 | 0 | 220k |
| V208 | 1 | +130 | 10k |
| (6U8) | 2 | - 5 | 5.3k |
| | 3 | +140 | 13k |
| | 6 | +300 | 1.1k |
| | 7 | 0 | 0 |
| | 8 | 0 | 0 |
| | 9 | 0 | 33k |
| V301 | 1 | -108 | 6.1k |
| (6485) | 2 | -110 | 3.3k |
| | 5 | - 23 | 6.8k |
| | 6 | - 55 | 47k |
| | 7 | -110 | 3.3k |
| V302 | 1 | -115 | >5k |
| (6485) | 2 | -110 | 3.3k |
| | 5 | + 40 | 6.8k |
| | 6 | - 55 | 47k |
| | 7 | -110 | 3.3k |
| V303 | 1 | + 6.3 | 107k |
| (6AN5) | 2 | 0 | 0 |
| | 5 | + 2.5 | >300k |
| | 6 | + 14 | 16k |
| | 7 | 0 | 0 |
| V304 | 1 | +298 | 100 |
| (12BH7) | 2 | + 2.5 | >300k |
| | 3 | + 15 | 20k |
| | 6 | +300 | 0 |
| | 7 | + 2.5 | >300k |
| | 8 | + 15 | 20k |
| V305 | 1 | +250 | 10k |
| (5965) | 2 | 0 | 33k |
| | 3 | + 5 | 1k |
| | 6 | +300 | 5.6k |
| | 7 | - 22 | 6.8k |
| | 8 | 0 | 5.6k |
| V306 | 1 | +295 | 5.6k |
| (12AX7) | 2 | +150 | 40k |
| | 3 | +150 | 22k |
| | 6 | +290 | 47k |
| | 7 | + 14 | 20k |
| | 8 | +150 | 22k |
| V307 | 1 | +300 | 0 |
| (5965) | 2 | + 21 | 35k |
| | 3 | + 38 | 12k |
| | 6 | +250 | 12k |
| | 7 | + 1 | 12.4k |

| TUBE (TYPE) | PIN | D-C VOLTS | RES TO GND |
|---|---|---|---|
| | 8 | + 10 | 3.5k |
| V308 | 1 | +410 | 0 |
| (5687) | 2 | +168 | 10M |
| | 3 | +180 | 10.7k |
| | 6 | + 31 | 19k |
| | 7 | + 15 | 20k |
| | 9 | +300 | 0 |
| V309 | 1 | + 0.6 | 107k |
| (6AN5) | 2 | 0 | 0 |
| | 5 | + 14 | 20k |
| | 6 | + 38 | 12k |
| | 7 | 0 | 0 |
| V310 | 1 | + 2 | 280k |
| (5965) | 2 | - 48 | 650k |
| | 3 | 0 | 0 |
| | 6 | + 33 | 470k |
| | 7 | - 0.6 | 3M |
| | 8 | 0 | 0 |
| V401 | 1 | +191 | 48k |
| (12AX7) | 2 | + 9.3 | 46.5k |
| | 3 | + 23.3 | 8k |
| | 6 | +215 | 8k |
| | 7 | + 24 | 26k |
| | 8 | + 23.3 | 8k |
| V402 | 1 | +188 | 48k |
| (12AX7) | 2 | + 9.5 | 46k |
| | 3 | + 23.5 | 8k |
| | 6 | +218 | 8k |
| | 7 | + 22.2 | 26k |
| | 8 | + 23.5 | 8k |
| V403 | 1 | - 3.4 | 18k |
| (6485) | 2 | + 0.3 | 32 |
| | 5 | +265 | 10k |
| | 6 | +210 | 34k |
| | 7 | + 0.3 | 32 |
| V404 | 1 | - 3.5 | 18k |
| (6485) | 2 | 0 | 0 |
| | 5 | +233 | 10k |
| | 6 | +210 | 34k |
| | 7 | 0 | 0 |
| V405 | 1 | - 31 | 23k |
| (6485) | 2 | 0 | 32 |
| | 5 | +142 | 1 |
| | 6 | +305 | 33k |
| | 7 | 0 | 32 |
| V406 | 1 | - 42.5 | 33k |
| (6485) | 2 | + 0.3 | 32 |
| | 5 | +144 | 9.5k |
| | 6 | +305 | 33k |
| | 7 | + 0.3 | 32 |
| V501 | 1 | +131 | 500 |
| (5687) | 2 | + 52 | 180k |
| | 3 | + 52 | 2.35k |
| | 6 | + 52 | 2.35k |
| | 7 | + 41 | 180k |

| TUBE (TYPE) | PIN | D-C VOLTS | RES TO GND |
|---|---|---|---|
| | 9 | +143 | 500 |
| V502 (12AX7) | 1 | + 52 | 180k |
| | 2 | - 21 | 220k |
| | 3 | - 20 | 340k |
| | 6 | + 41 | 180k |
| | 7 | - 21 | 220k |
| | 8 | - 20 | 340k |
| V503 (6AV5GA) | 1 | + 52 | 175k |
| | 3 | + 54 | 7.5k |
| | 5 | +109 | 5.6k |
| | 8 | +120 | 6.5k |
| V504 (6AV5GA) | 1 | + 40 | 175k |
| | 3 | + 54 | 7.5k |
| | 5 | +135 | 5.6k |
| | 8 | +120 | 6.5k |
| V505 (6AV5GA) | 1 | -216 | 600k |
| | 3 | -185 | 50 |
| | 5 | -135 | 850 |
| | 8 | - 90 | 5k |
| V506 (6AV5GA) | 1 | -185 | 600k |
| | 3 | -180 | 50 |
| | 5 | -158 | 850 |
| | 8 | - 90 | 5k |
| V507 (6550) | 1 | | 600 |
| | 3 | - 23.5 | |
| | 4 | | 145 |
| | 5 | -135 | ∞ |
| | 8 | -135 | |
| V508 (6550) | 1 | | 600 |
| | 3 | - 0.3 | |
| | 4 | | 145 |

| TUBE (TYPE) | PIN | D-C VOLTS | RES TO GND |
|---|---|---|---|
| | 5 | -155 | ∞ |
| | 8 | -135 | |
| V509 (12AX7) | 1 | -210 | 600k |
| | 2 | -315 | 230k |
| | 3 | -315 | 130k |
| | 6 | -185 | 600k |
| | 7 | -315 | 230k |
| | 8 | -315 | 130k |
| V510 (OA2) | 1 | -185 | 50 |
| | 4 | -340 | 11.5k |
| | 5 | -185 | 50 |
| | 7 | -340 | 11.5 |
| V511 (12BH7) | 1 | +142 | 950 |
| | 2 | + 4.5 | 1M |
| | 3 | + 9 | ∞ |
| | 6 | +143 | 0 |
| | 7 | + 5 | 1M |
| | 8 | + 9 | ∞ |
| V601 (6AS7G) | 1 | +235 | 180k |
| | 2 | +430 | 0.45k |
| | 3 | +300 | 0 |
| | 4 | +235 | 180k |
| | 5 | +430 | 0.45k |
| | 6 | +300 | 0 |
| V602 (6AK5) | 1 | +147 | 43k |
| | 2 | +150 | 15k |
| | 5 | +235 | 180k |
| | 6 | +265 | 5.1k |
| | 7 | +150 | 15k |
| V603 (OD3) | 2 | 0 | 0 |
| | 5 | +150 | 15k |

| | TERMINAL | VOLTS | RES TO GND |
|---|---|---|---|
| POWER XFMR T601 | 1-2 | 115 | |
| | 3-4 | 115 | |
| | 5-6 | 197 | |
| (all voltages are ac) | 30-31 | 6.8 | |
| | 12-23 | 6.8 | |
| | 9-13 | 6.8 | |
| | 25-26 | 6.6 | |
| | 32-33 | 6.9 | |
| | 10-11 | 68 | |
| | 7-8 | 140 | |
| | 6-16 | 135 | |
| | 27-28 | 97 | |
| | 17-18 | 290 | |
| PL101 | 3 | | ∞ |
| | 4 | | ∞ |
| | 5 | | >50k |
| | 6 | | >50k |
| | 7 | | 50 |
| | 8 | | 50 |
| | 9 | | 50 |
| | 10 | | 50 |
| | 11 | | >10k |
| | 12 | | >10k |
| PL401 | 1 | +440 | |
| | 4 | +310 | |
| | 5 | + 60 | |
| | 7 | -190 | |
| | 9 | -540 | |
| | 10 | +150 | |
| T201 | 3-5 | | 5 |
| | 2-6 | | 5 |
| | 1-7 | | 5 |

NOTES:

(1) Input resistance of d-c voltmeter must be several times value listed in RES column.

(2) Panel controls should be set as follows:

TIME DELAY RANGE: 10-100 ms
COINCIDENCE GATE DURATION: CCW
COINCIDENCE SENSITIVITY: CW
MICROSECONDS: 1.00
PULSE AMPLITUDE: CW
OUTPUT IMPEDANCE: 150
PULSE DELAY: CW
PULSE DURATION: CW
SWEEP MULTIPLIER: $10^2$
SWEEP SCALE: 6

(3) Measure voltages with no input signal.

(4) Voltage conditions in push-pull stages of pulse-forming circuits (V501 to V507) may be the reverse of those listed. (i. e., V501 voltages may apply to V502, and vice versa.)

(5) Operate RESET switch before making voltage measurements.

(6) All resistances are in ohms unless otherwise indicated by k (kilohms) or M megohms).

(7) Resistance measurements were made with all terminals of PL401 grounded in the Type 1391-B, and all terminals of SO401 grounded in the Type 1391-P2. Resistances at PL401 terminals were measured with Type 1391-P2 disconnected.

## TABLE 5.4

## VOLTAGES IN THE PULSE SOURCE

| Measurement Point | Volts dc | |
|---|---|---|
| | Quiescent | Active |
| TP501 | + 53 | + 41 |
| TP502 | + 41 | + 55 |
| TP503 | -212 | -182 |
| TP504 | -185 | -218 |
| TP505 | -135 | -158 |
| TP506 | -155 | -135 |
| PULSE POS | - 23 | 0 |
| PULSE NEG | 0 | - 24 |

NOTES

1. Voltages in column labeled "Quiescent" are for the normal position, those in the "Active" column for the active pulse interval. If the gate is in the pulse-on state (V502 on), then the "Active" voltage applies and the voltage stated of all succeeding test points and at pulse output terminals reverse roles.
2. Voltages should be measured with no input signal.
3. Switch settings:
   OUTPUT IMPEDANCE: 150
   PULSE AMPLITUDE: CW
4. Any abnormal voltages indicate troubles that can be remedied by replacement of tubes or components.

## TABLE 5.5

## POWER-SUPPLY-CIRCUIT CONNECTIONS

| SUPPLY | PL401 PIN NO. | TUBES |
|---|---|---|
| +410 | 1 | V308B |
| +300 | 2 | V101A, V102, V104B, V203, V204A, V205, V207A, V208, V303, V304, V309, V306, V307B |
| +300 (±10%) | 4 | V101B, V103, V104A, V204B, V206A, V207B, V308A, V307A, V305, V310B |
| + 55 | 5 | V201, V202, V301, V302, V501, V502 |
| -150 | 6 | V201, V202, V301, V302, V501, V502, V206 |
| -190 | 7 | Bias V103A, bias V208A, V507 |
| -290 | 9 | V505, V506 |
| +140 | 10 | V503, V504 |
| -425 | 12 | Bias V505, bias V506 |

## TABLE 5.6

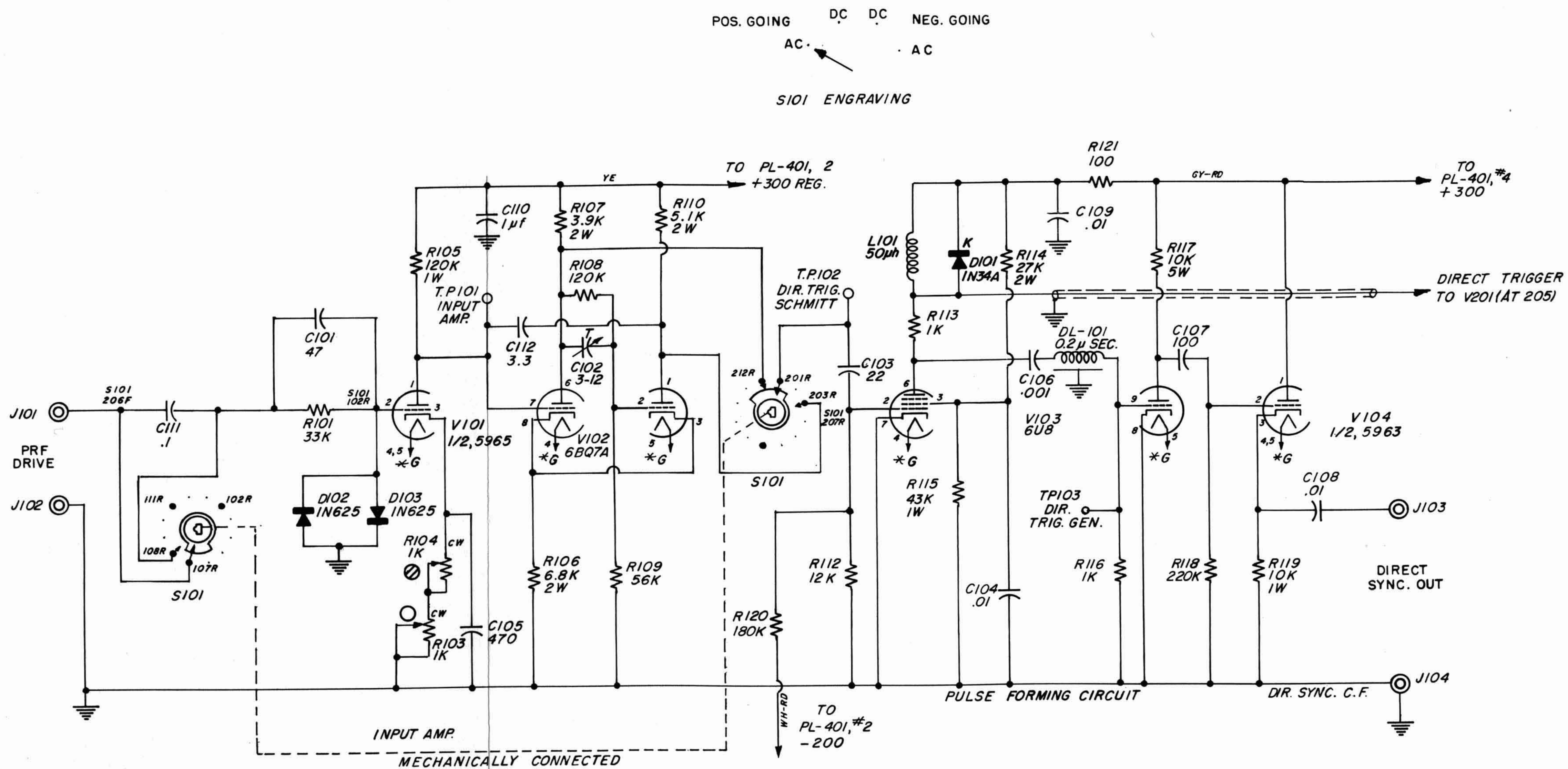
## TABLE OF D-C OUTPUTS (Measured at SO602)

| PL602 | Volts | Ma |
|---|---|---|
| 1 | +435 | 17 |
| 2 | +300 | 120 |
| 4 | +310 | 92 |
| 5 | + 55 | 29 |
| 6 | -150 | 46 |
| 7 | -190 | 207 |
| 9 | -540 | 0.3 |
| 10 | +150 | 170 |
| 12 | -430 | 7 |

## PARTS LIST

| Section | Ref. | Value | Tolerance | Rating | GR No. (NOTE A) |
|---|---|---|---|---|---|
| RESISTORS (NOTE B) | R101 | 33 k | ± 5% | 1/2 w | REC-20BF |
| | R103 | 1 k | ± 5% | 1/2 w | 971-410 |
| | R104 | 1 k | ±10% | | POSW-3 |
| | R105 | 120 k | ± 5% | 1 w | REC-30BF |
| | R106 | 6.8 k | ± 5% | 2 w | REC-41BF |
| | R107 | 3.9 k | ± 5% | 2 w | REC-41BF |
| | R108 | 120 k | ± 5% | 1/2 w | REC-20BF |
| | R109 | 56 k | ± 5% | 1/2 w | REC-20BF |
| | R110 | 5.1 k | ± 5% | 2 w | REC-41BF |
| | R112 | 12 k | ± 5% | 1/2 w | REC-20BF |
| | R113 | 1 k | ± 5% | 1/2 w | REC-20BF |
| | R114 | 27 k | ± 5% | 2 w | REC-41BF |
| | R115 | 43 k | ± 5% | 1 w | REC-30BF |
| | R116 | 1 k | ± 5% | 1/2 w | REC-20BF |
| | R117 | 10 k | ±10% | 5 w | REPO-43 |
| | R118 | 220 k | ± 5% | 1/2 w | REC-20BF |
| | R119 | 10 k | ±10% | 1 w | REC-30BF |
| | R120 | 180 k | ± 5% | 1/2 w | REC-20BF |
| | R121 | 100 k | ± 5% | 1/2 w | REC-20BF |
| CAPACITORS (NOTE C) | C101 | 47 | ±10% | 500dcwv | COC-21(N750) |
| | C102 | 3-12 | | | COT-23 |
| | C103 | 22 | ±10% | 500dcwv | COM-20B |
| | C104 | 0.01µf | | 500dcwv | COC-63 |
| | C105 | 470 | ±10% | 500dcwv | COM-20B |
| | C106 | 0.001µf | ±10% | 300dcwv | COM-20B |
| | C107 | 100 | ±10% | 500dcwv | COM-20B |
| | C108 | 0.01µf | ±10% | 500dcwv | COL-71 |
| | C109 | 0.01µf | | 500dcwv | COC-63 |
| | C110 | 1µf | ±10% | 400dcwv | COW-25 |
| | C111 | 0.1µf | ±10% | 600dcwv | COL-71 |
| | C112 | 3.3 | ±10% | 500dcwv | COC-1 |
| MISCELLANEOUS | BL101 | BLOWER | | | FA-1 |
| | D101 | CRYSTAL DIODE | | | 1N34-A |
| | D102 | CRYSTAL DIODE | | | 1N625 |
| | D103 | CRYSTAL DIODE | | | 1N625 |
| | DL101 | DELAY LINE, 0.2µsec | | | 1391-326 |
| | F101 | SNAP CONTROL, Thermo | | | FUC-13 |
| | L101 | AIR CHOKE, 50µh | | | CHA-3-2 |
| | PL101 | PLUG | | | CDMP-11-10 |
| | S101 | SWITCH, Rotary | | | SWRW-175 |
| | V101 | TUBE | | | 5965 |
| | V102 | TUBE | | | 6BQ7-A |
| | V103 | TUBE | | | 6U8 |
| | V104 | TUBE | | | 5963 |

For explanation of NOTES, refer to page 42.




○ PANEL CONTROL

⊘ SCREW DRIVER ADJUSTMENT

RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED

RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED
K = 1000 OHMS M = 1 MEGOHM

CAPACITANCE VALUES ONE AND OVER IN MICRO MICROFARADS, LESS THAN ONE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED

* HEATER CABLE CONNECTIONS SHOWN IN FIGURE 5.5b.

TP USED: 101, 102, 103

## BLOCK DIAGRAM

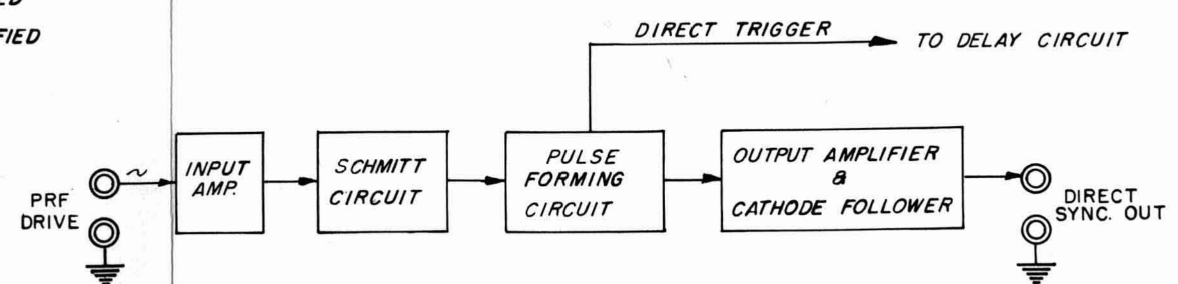



Figure 5.1. Schematic Diagram for Input Trigger Generator Circuits.

PARTS LIST

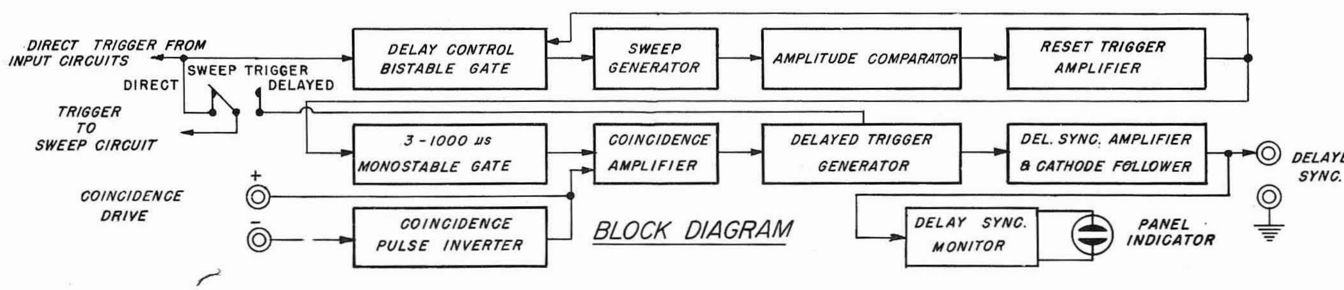
| | | | | | GR No. (NOTE A) |
|---|---|---|---|---|---|
| RESISTORS (NOTE B) | R201 | 1 k | ± 5% | 1/2 w | REC-20BF |
| | R202 | 4.7 k | ± 5% | 1/2 w | REC-20BF |
| | R203 | 6.8 k | ± 5% | 1 w | REC-30BF |
| | R204 | 6.8 | ± 5% | 1 w | REC-30BF |
| | R205 | 100 k | ± 1% | 1/2 w | REF-70 |
| | R206 | 100 k | ± 1% | 1/2 w | REF-70 |
| | R207 | 30 k | ± 1% | 1/2 w | REF-70 |
| | R208 | 30 k | ± 1% | 1/2 w | REF-70 |
| | R209 | 3 k | ± 5% | 1/2 w | REC-20BF |
| | R210 | 36 k | ± 5% | 1/2 w | REC-20BF |
| | R211 | 100 k | ± 5% | 1/2 w | REC-20BF |
| | R212 | 47 k | ± 5% | 2 w | REC-41BF |
| | R213 | 24 k | ± 5% | 1 w | REC-30BF |
| | R218 | 10 k | ± 5% | 1/2 w | REC-20BF |
| | R219 | 270 k | ± 5% | 1/2 w | REC-20BF |
| | R220 | 47 k | ± 5% | 1/2 w | REC-20BF |
| | R221 | 10 k | ± 5% | 1/2 w | REC-20BF |
| | R222 | 450 k | ± 1% | 1/2 w | REF-70 |
| | R223 | 450 k | ± 1% | 1/2 w | REF-70 |
| | R224 | 450 k | ± 1% | 1/2 w | REF-70 |
| | R225 | 450 k | ± 1% | 1/2 w | REF-70 |
| | R226 | 500 k | ± 1% | 1/2 w | REF-75 |
| | R227 | 4.5 M | ± 1% | 1 w | REF-2-2 |
| | R228 | 250 k | ±10% | | POSC-11 |
| | R229 | 100 k | ±10% | | POSC-11 |
| | R230 | 100 k | ±10% | | POSC-11 |
| | R231 | 100 k | ±10% | | POSC-11 |
| | R232 | 100 k | ±10% | | POSC-11 |
| | R233 | 1 M | ±20% | | POSC-11 |
| | R234 | 22 k | ± 5% | 2 w | REC-41BF |
| | R235 | 24 k | ± 5% | 5 w | REPO-43 |
| | R236 | 5 k | ±10% | | POSW-3 |
| | R237 | 10 k | ± 5% | | 1391-42 |
| | R238 | 500 | ±10% | | POSW-3 |
| | R239 | 27 k | ± 1% | 1/2 w | REF-70 |
| | R240 | 6.8 k | ±10% | 2 w | REC-41BF |
| | R241 | 330 k | ± 1% | 1/2 w | REF-70 |
| | R242 | 47 k | ±10% | 1 w | REC-30BF |
| | R243 | 5.6 k | ± 5% | 1/2 w | REC-20BF |
| | R244 | 33 k | ± 5% | 1/2 w | REC-20BF |
| | R245 | 1 k | ± 5% | 1/2 w | REC-20BF |
| | R246 | 4.7 k | ± 5% | 1/2 w | REC-20BF |
| | R247 | 100 k | ± 5% | 1/2 w | REC-20BF |
| | R248 | 100 k | ± 5% | 1 w | REC-30BF |
| | R249 | 1 k | ±10% | | POSW-3 |
| | R250 | 2.2 k | ± 5% | 1/2 w | REC-20BF |
| | R251 | 15 k | ± 5% | 2 w | REC-41BF |
| | R252 | 510 | ± 5% | 1/2 w | REC-20BF |
| | R253 | 10 k | ± 5% | | 973-N |
| | R254 | 2 M | ± 5% | 1/2 w | REC-20BF |
| | R255 | 1 M | ±20% | | POSC-11 |
| | R256 | 3 k | ± 5% | 1/2 w | REC-30BF |
| | R257 | 1.2 k | ± 5% | 1/2 w | REC-20BF |
| | R258 | 3.3 k | ± 5% | 1 w | REC-30BF |

| | | | | | GR No. (NOTE A) |
|---|---|---|---|---|---|
| RESISTORS (NOTE B) | R259 | 220 | ± 5% | 1/2 w | REC-20BF |
| | R260 | 100 k | ± 5% | 1/2 w | REC-20BF |
| | R261 | 330 | ± 5% | 1/2 w | REC-20BF |
| | R262 | 6.8 k | ±10% | 2 w | REC-41BF |
| | R263 | 1 k | ± 5% | 1/2 w | REC-20BF |
| | R264 | 100 k | ±10% | 1 w | REC-30BF |
| | R265 | 10 k | ± 5% | | 973-N |
| | R266 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R267 | 1 k | ± 5% | 1 w | REC-30BF |
| | R268 | 47 | ± 5% | 1/2 w | REC-20BF |
| | R269 | 47 k | ± 5% | 1/2 w | REC-20BF |
| | R270 | 180 k | ± 5% | 1/2 w | REC-20BF |
| | R271 | 5.1 k | ± 5% | 1/2 w | REC-20BF |
| | R272 | 1 k | ± 5% | 1/2 w | REC-20BF |
| | R273 | 27 k | ± 5% | 1 w | REC-30BF |
| | R274 | 27 k | ± 5% | 1 w | REC-30BF |
| | R275 | 33 k | ± 5% | 1/2 w | REC-20BF |
| | R276 | 10 k | ± 5% | 5 w | REPO-43 |
| | R277 | 220 k | ± 5% | 1/2 w | REC-20BF |
| | R278 | 10 k | ±10% | 1 w | REC-30BF |
| | R279 | 18 M | ± 5% | 1/2 w | REC-20BF |
| | R280 | 100 k | ±10% | 1 w | REC-30BF |
| | R281 | 1 M | ± 5% | 1/2 w | REC-20BF |
| | R282 | 560 | ± 5% | 1/2 w | REC-20BF |
| | R283 | 62 k | ± 5% | 1/2 w | REC-20BF |
| | R284 | 1200 | ± 5% | 1/2 w | REC-20BF |
| | R285 | 1.8 k | ± 5% | 1/2 w | REC-20BF |
| | R286 | (Note F) | ± 5% | 1/2 w | REC-20BF |
| | R287 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R288 | 100 k | ± 5% | 1/2 w | REC-20BF |
| | R289 | 100 k | ± 5% | 1/2 w | REC-20BF |
| | R290 | 100 k | ± 5% | 1/2 w | REC-20BF |
| CAPACITORS (NOTE C) | C201 | 100 | ±10% | 500dcwv | COC-21 |
| | C202 | 100 | ±10% | 500dcwv | COC-21 |
| | C203 | 22 | ±10% | 500dcwv | COC-21(N750) |
| | C204 | 22 | ±10% | 500dcwv | COC-21(N750) |
| | C205 | 47 | ±10% | 500dcwv | COC-21(N750) |
| | C206 | 0.001μf | ±10% | 300dcwv | COM-20B |
| | C207 | 0.01μf | ±10% | 600dcwv | COL-71 |
| | C208 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C209 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C219 | 0.0047μf | ±10% | 200dcwv | COW-16 |
| | C220 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C221 | 0.47μf | ±10% | 100dcwv | COW-17 |
| | C222 | 7-45 | | | COT-12 |
| | C223 | 470 | ± 2% | 500dcwv | COM-20E |
| | C224 | 0.0047μf | ± 2% | 500dcwv | COM-35E |
| | C225 | 0.047μf | ± 2% | 150dcwv | ZCOP-8 |
| | C226 | 0.47μf | ± 2% | 150dcwv | ZCOP-6-2 |
| | C227 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C229 | 3.3 | ±0.5μμf | 500dcwv | COC-21(N750) |
| | C230 | 47 | ±10% | 500dcwv | COM-20B |

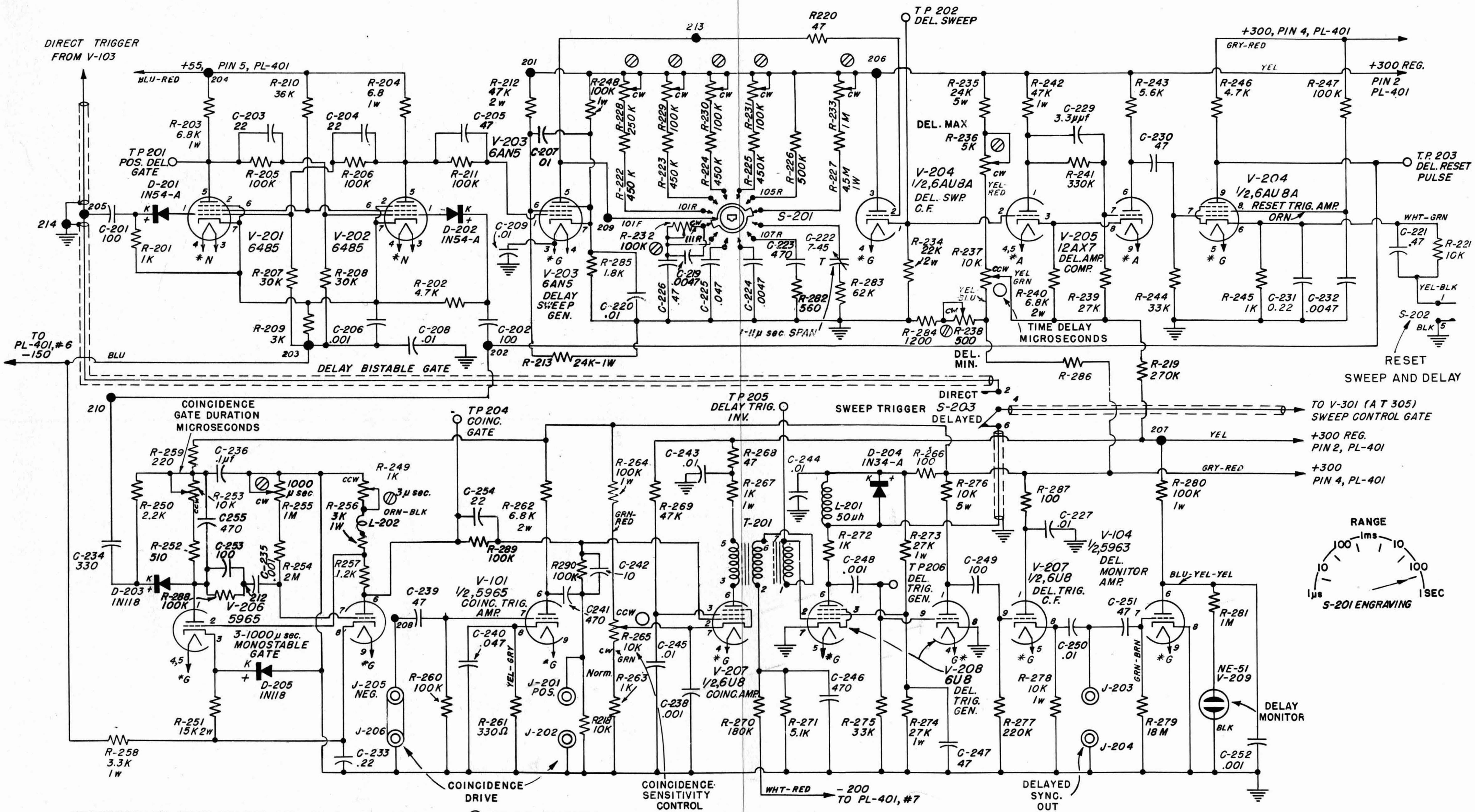
| CAPACITORS (NOTE C) | | | | GR No. (NOTE A) |
|---|---|---|---|---|
| C231 | 0.22µf | ±10% | 100dcwv | COW-17 |
| C232 | 0.0047µf | ±10% | 600dcwv | COL-71 |
| C233 | 0.22µf | ±10% | 200dcwv | COW-16 |
| C234 | 330 | ±10% | 500dcwv | COM-20B |
| C235 | 0.001µf | ± 2% | 300dcwv | COM-20E |
| C236 | 0.1µf | ±10% | 400dcwv | COW-25 |
| C238 | 0.001µf | ±10% | 500dcwv | COM-20B |
| C239 | 47 | ±10% | 500dcwv | COC-21 (N750) |
| C240 | 0.047µf | ±10% | 100dcwv | COW-17 |
| C241 | 470 | ±10% | 500dcwv | COM-20B |
| C242 | 10 | ±0.5µµf | 500dcwv | COC-21 (N750) |
| C243 | 0.01µf | ±10% | 600dcwv | COL-71 |
| C244 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| C245 | 0.001µf | ±10% | 300dcwv | COM-20B |
| C246 | 470 | ±10% | 500dcwv | COM-20B |
| C247 | 47 | ±10% | 500dcwv | COC-21(N750) |
| C248 | 0.001µf | ±10% | 300dcwv | COM-20B |
| C249 | 100 | ±10% | 500dcwv | COM-20B |
| C250 | 0.01µf | ±10% | 600dcwv | COL-71 |
| C251 | 47 | ±10% | 500dcwv | COC-21(N750) |
| C252 | 0.001µf | ±10% | 300dcwv | COM-20B |
| C253 | 100 | ±10% | 500dcwv | COC-21 |
| C254 | 22 | ±10% | 500dcwv | COC-21(N750) |
| C255 | 470 | ±10% | 500dcwv | COM-20B |

| MISCELLANEOUS | | GR No. (NOTE A) |
|---|---|---|
| D201 | CRYSTAL DIODE | 1N54-A |
| D202 | CRYSTAL DIODE | 1N54-A |
| D203 | CRYSTAL DIODE | 1N118 |
| D204 | CRYSTAL DIODE | 1N34-A |
| D205 | CRYSTAL DIODE | 1N118 |
| L201 | AIR CHOKE, 50 µh | CHA-3-2 |
| L202 | AIR CHOKE, 100µh | CHA-3-3 |
| S201 | SWITCH | SWRW-113 |
| S202 | SWITCH | SWT-8 |
| S203 | SWITCH | SWT-320 |
| T201 | TRANSFORMER | 1391-44 |
| V201 | TUBE | 6485 |
| V202 | TUBE | 6485 |
| V203 | TUBE | 6AN5 |
| V204 | TUBE | 6AU8A |
| V205 | TUBE | 12AX7 |
| V206 | TUBE | 5965 |
| V207 | TUBE | 6U8 |
| V208 | TUBE | 6U8 |
| V209 | TUBE | NE-51 |

For explanation of NOTES, refer to page 42.




Block Diagram for Delay Circuits.




RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED

RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED
K = 1000 OHMS   M = 1 MEGOHM

CAPACITANCE VALUES ONE AND OVER IN MICRO MICRO-FARADS, LESS THAN ONE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

○ PANEL CONTROL

⊘ SCREW DRIVER ADJUSTMENT

* HEATER CABLE CONNECTIONS SHOWN IN FIGURE 5.5b.

Figure 5.2. Schematic Diagram for Delay Circuits.

PARTS LIST

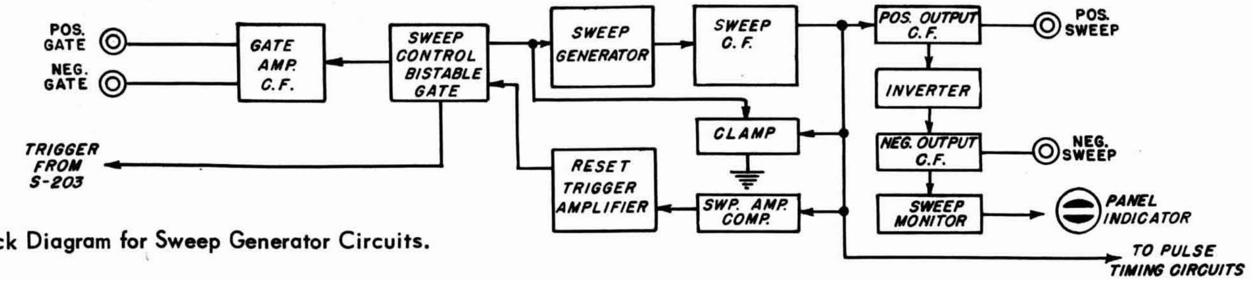
| | | | | | GR No. (NOTE A) |
|---|---|---|---|---|---|
| RESISTORS (NOTE B) | R301 | 1 k | ± 5% | 1/2 w | REC-20BF |
| | R302 | 4.7 k | ± 5% | 1/2 w | REC-20BF |
| | R303 | 6.8 k | ± 5% | 1 w | REC-30BF |
| | R304 | 6.8 k | ± 5% | 1 w | REC-30BF |
| | R305 | 100 k | ± 1% | 1/2 w | REF-70 |
| | R306 | 100 k | ± 1% | 1/2 w | REF-70 |
| | R307 | 30 k | ± 1% | 1/2 w | REF-70 |
| | R308 | 30 k | ± 1% | 1/2 w | REF-70 |
| | R309 | 3 k | ± 5% | 1/2 w | REC-20BF |
| | R310 | 36 k | ± 5% | 1/2 w | REC-20BF |
| | R311 | 100 k | ± 5% | 1/2 w | REC-20BF |
| | R312 | 47 k | ± 5% | 2 w | REC-41BF |
| | R313 | 24 k | ± 5% | 1 w | REC-30BF |
| | R317 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R318 | 33 k | ± 5% | 1/2 w | REC-20BF |
| | R319 | 1.2 M | ± 5% | 1/2 w | REC-20BF |
| | R320 | 1.5 M | ± 5% | 1/2 w | REC-20BF |
| | R321 | 10 k | ± 5% | | 973-N |
| | R322 | 47 k | ± 5% | 2 w | REC-41BF |
| | R323 | 91 k | ± 5% | 1/2 w | REC-20BF |
| | R324 | 200 k | ± 5% | 1/2 w | REC-20BF |
| | R325 | 390 k | ± 5% | 1/2 w | REC-20BF |
| | R326 | 91 k | ± 5% | 1/2 w | REC-20BF |
| | R327 | 200 k | ± 5% | 1/2 w | REC-20BF |
| | R328 | 390 k | ± 5% | 1/2 w | REC-20BF |
| | R329 | 25 k | ±10% | | POSC-11 |
| | R330 | 100 k | ±10% | | POSC-11 |
| | R331 | 250 k | ±10% | | POSC-11 |
| | R332 | 100 k | ±10% | | POSC-11 |
| | R333 | 250 k | ±10% | | POSC-11 |
| | R334 | 250 k | ±10% | | POSC-11 |
| | R335 | 12 k | ± 5% | 2 w | REC-41BF |
| | R336 | 6.8 k | ± 5% | 2 w | REC-41BF |
| | R337 | 10 M | ± 5% | 1/2 w | REC-20BF |
| | R338 | 680 | ± 5% | 1/2 w | REC-20BF |
| | R339 | 10 k | ±10% | 5 w | 1391-40 |
| | R340 | 1 k | ±10% | | POSW-3 |
| | R341 | 15 k | ± 5% | 1/2 w | REC-20BF |
| | R342 | 22 k | ± 5% | 1 w | REC-30BF |
| | R343 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R344 | 100 k | ± 5% | 1/2 w | REC-20BF |
| | R345 | 470 k | ± 5% | 1/2 w | REC-20BF |
| | R346 | 100 k | ± 5% | 1/2 w | REC-20BF |
| | R347 | 10 M | ± 5% | 1/2 w | REC-20BF |
| | R348 | 10 k | ±10% | 2 w | REC-41BF |
| | R349 | 8.2 k | ±10% | 2 w | REC-41BF |
| | R350 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R351 | 22 k | ±10% | 2 w | REC-41BF |
| | R352 | 10 k | ±10% | | POSW-3 |
| | R353 | 10 k | ±10% | 1 w | REC-30BF |
| | R354 | 6.8 k | ±10% | 1 w | REC-30BF |
| | R355 | 47 k | ±10% | 1/2 w | REC-20BF |
| | R356 | 330 k | ± 5% | 1/2 w | REC-20BF |
| | R357 | 27 k | ± 5% | 1/2 w | REC-20BF |

| | | | | | GR No. (NOTE A) |
|---|---|---|---|---|---|
| RESISTORS (NOTE B) | R358 | 5.6 k | ± 5% | 1/2 w | REC-20BF |
| | R359 | 33 k | ± 5% | 1/2 w | REC-20BF |
| | R360 | 1 k | ± 5% | 1/2 w | REC-20BF |
| | R361 | 10 k | ±10% | 2 w | REC-41BF |
| | R362 | 7.5 k | ± 5% | 1/2 w | REC-20BF |
| | R363 | 5.6 k | ± 5% | 1 w | REC-30BF |
| | R364 | 5.6 k | ± 5% | 1 w | REC-30BF |
| | R365 | 10 M | ± 5% | 1/2 w | REC-20BF |
| | R366 | 10 M | ± 5% | 1/2 w | REC-20BF |
| | R367 | 10 M | ± 5% | 1/2 w | REC-20BF |
| | R368 | 10 M | ± 5% | 1/2 w | REC-20BF |
| | R369 | 2.7 M | ± 5% | 1/2 w | REC-20BF |
| | R370 | 150 k | ± 5% | 1/2 w | REC-20BF |
| | R371 | 5.6 k | ± 5% | 1/2 w | REC-20BF |
| | R372 | 12 k | ± 5% | 2 w | REC-41BF |
| | R373 | 3.3 k | ± 5% | 1/2 w | REC-20BF |
| | R374 | 22 k | ± 5% | 1/2 w | REC-20BF |
| CAPACITORS (NOTE C) | C301 | 100 | ±10% | 500dcwv | COC-21 |
| | C302 | 100 | ±10% | 500dcwv | COC-21 |
| | C303 | 22 | ±10% | 500dcwv | COC-21(N750) |
| | C304 | 22 | ±10% | 500dcwv | COC-21(N750) |
| | C305 | 47 | ±10% | dcwv | COC-21(N750) |
| | C306 | 0.001µf | ±10% | 300dcwv | COM-20B |
| | C307 | 0.01µf | ±10% | 600dcwv | COL-71 |
| | C321 | 3-12 | | | COT-23 |
| | C322 | 430 | ± 2% | 500dcwv | COM-20E |
| | C323 | 0.0047µf | ± 2% | 500dcwv | COM-35E |
| | C324 | 0.047µf | ± 2% | 150dcwv | ZCOP-8 |
| | C325 | 0.47µf | ± 2% | 150dcwv | ZCOP-6-2 |
| | C326 | 0.1 µf | ±10% | 100dcwv | COW-25 |
| | C327 | 1 µf | ±10% | 400dcwv | COW-25 |
| | C328 | 1 µf | ±10% | 400dcwv | COW-25 |
| | C329 | 47 | ±10% | 500dcwv | COC-21(N750) |
| | C330 | 30 µf | | 350dcwv | COE-53 |
| | C331 | 0.001µf | ±10% | 300dcwv | COM-20B |
| | C332 | 220 | ±10% | 500dcwv | COM-20B |
| | C333 | 47 | ±10% | 500dcwv | COM-20B |
| | C334 | 10 | ±0.5µµf | 500dcwv | COC-21(N750) |
| | C335 | 47 | ±10% | 500dcwv | COM-20B |
| | C336 | 0.1 µf | +100-0% | 300dcwv | COC-63 |
| | C337 | 1 µf | ±10% | 100dcwv | COW-17 |
| | C338 | 1 µf | ±10% | 400dcwv | COW-25 |
| | C339 | 1 µf | ±10% | 400dcwv | COW-25 |
| | C340 | 16 µf | | 150dcwv | COE-4 |
| | C341 | 100 | ±10% | | COC-21 |
| MISC. | D301 | CRYSTAL DIODE | | | 1N54-A |
| | D302 | CRYSTAL DIODE | | | 1N54-A |
| | D303 | CRYSTAL DIODE | | | HD6008 |
| | S301 | SWITCH | | | SWRW-80 |
| | S302 | SWITCH | | | SWRW-81 |

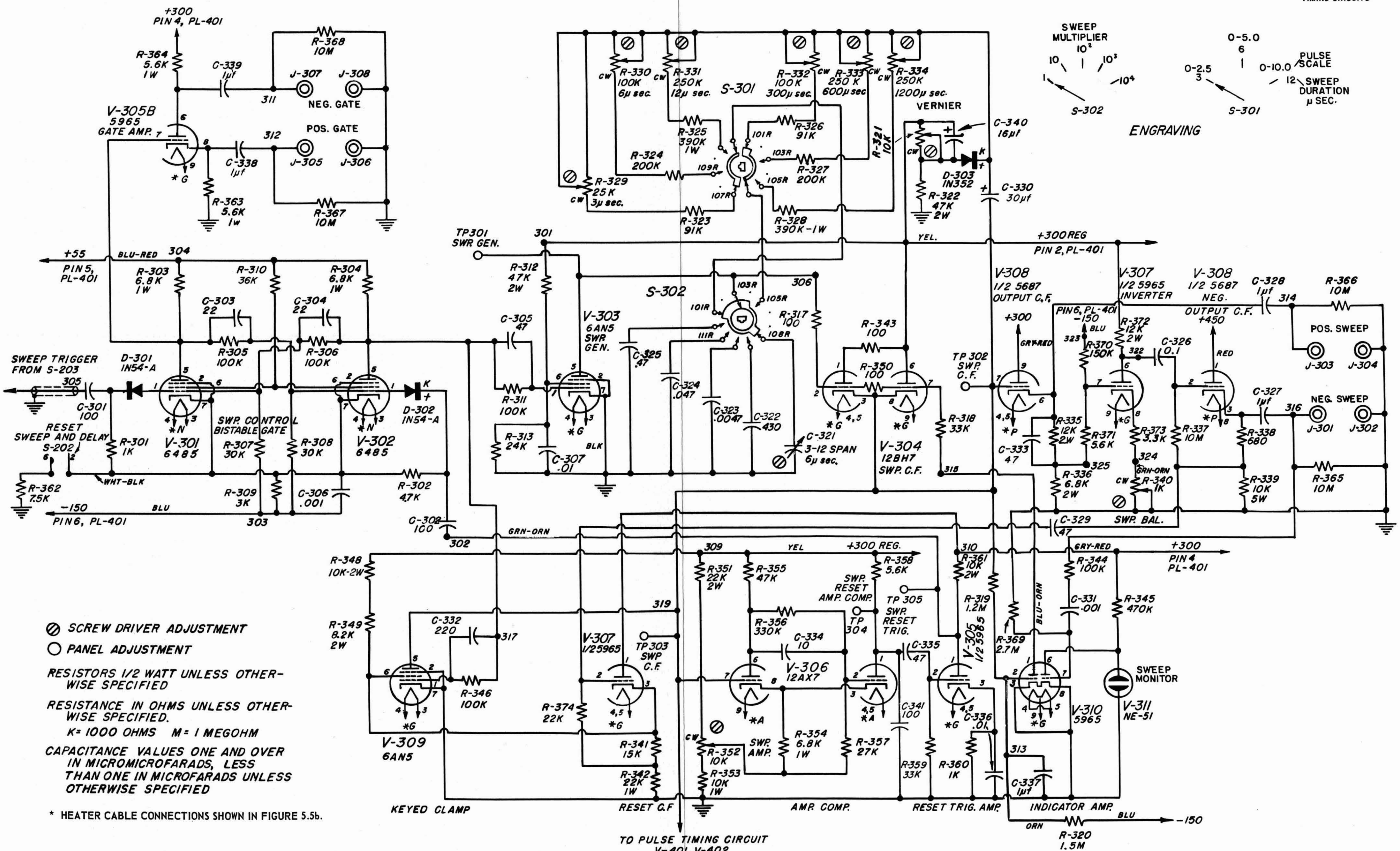
For explanation of NOTES, refer to page 42.

| | | GR No. (NOTE A) |
|---|---|---|
| V301 | TUBE | 6485 |
| V302 | TUBE | 6485 |
| V303 | TUBE | 6AN5 |
| V304 | TUBE | 12BH7 |
| V305 | TUBE | 5965 |
| V306 | TUBE | 12AX7 |
| V307 | TUBE | 5965 |
| V308 | TUBE | 5687 |
| V309 | TUBE | 6AN5 |
| V310 | TUBE | 5965 |
| V311 | TUBE | NE-51 |

Figure 5.3. Schematic Diagram for Sweep Generator Circuits.




Block Diagram for Sweep Generator Circuits.




⊘ SCREW DRIVER ADJUSTMENT

○ PANEL ADJUSTMENT

RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED

RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED.
K = 1000 OHMS M = 1 MEGOHM

CAPACITANCE VALUES ONE AND OVER IN MICROMICROFARADS, LESS THAN ONE IN MICROFARADS UNLESS OTHERWISE SPECIFIED

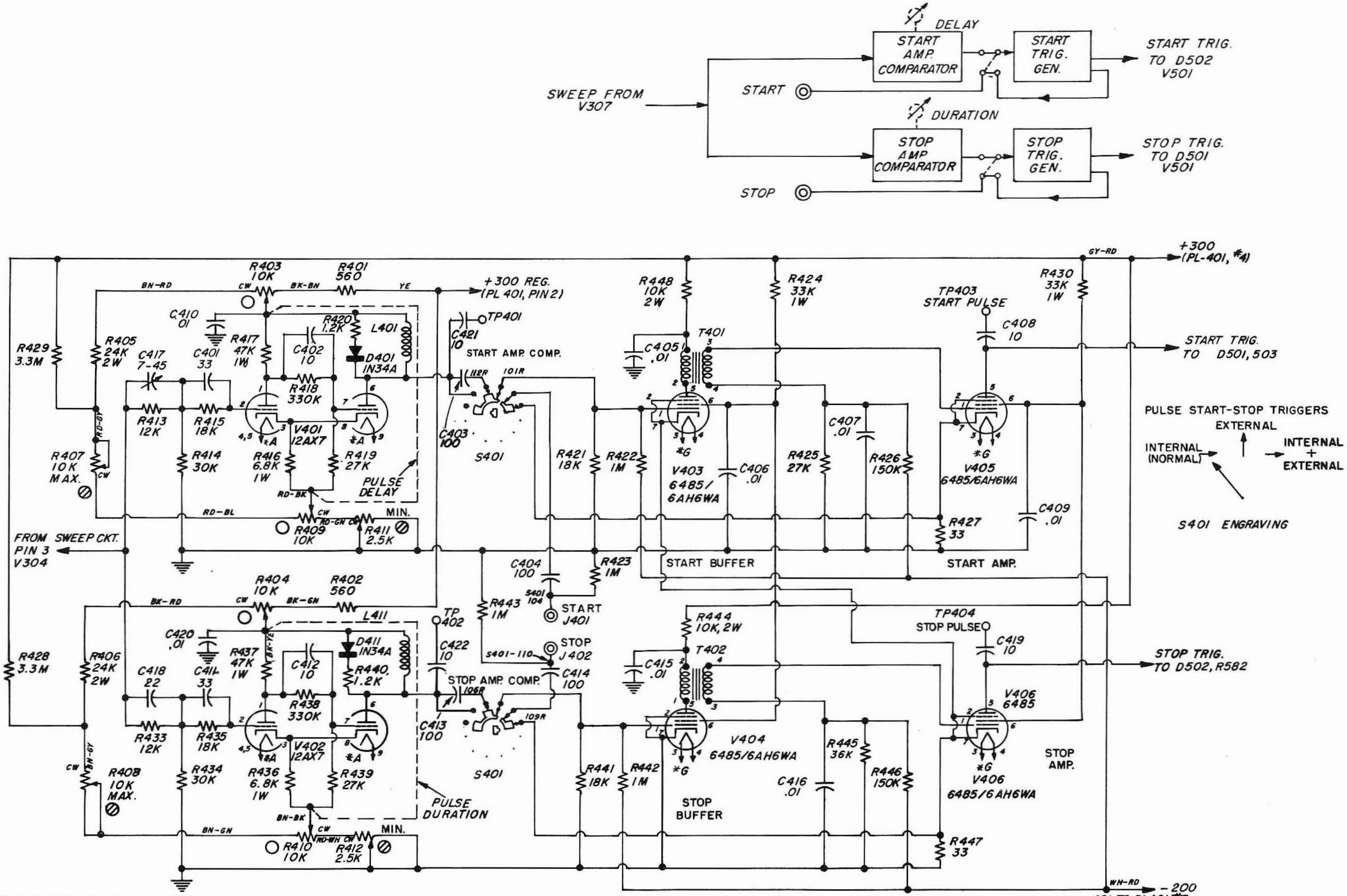
* HEATER CABLE CONNECTIONS SHOWN IN FIGURE 5.5b.

# PARTS LIST

| | | PART NO. (NOTE A) | | | |
|---|---|---|---|---|---|
| RESISTORS (NOTE B) | R401 | 560 | ±5% | 1/2w | REC-20BF |
| | R402 | 560 | ±5% | 1/2w | REC-20BF |
| | R403 | 10k | ±5% | | 1391-210 |
| | R404 | 10k | ±5% | | 1391-210 |
| | R405 | 24k | ±5% | 2 w | REC-41BF |
| | R406 | 24k | ±5% | 2 w | REC-41BF |
| | R407 | 10k | ±10% | | POSW-3 |
| | R408 | 10k | ±10% | | POSW-3 |
| | R409 | 10k | ±5% | | 1391-210 |
| | R410 | 10k | ±5% | | 1391-210 |
| | R411 | 2.5k | ±10% | | POSW-3 |
| | R412 | 2.5k | ±10% | | POSW-3 |
| | R413 | 12k | ±1% | 1/2w | REF-70 |
| | R414 | 30k | ±1% | 1/2w | REF-70 |
| | R415 | 18k | ±5% | 1/2w | REC-20BF |
| | R416 | 6.8k | ±5% | 1 w | REC-30BF |
| | R417 | 47k | ±5% | 1 w | REC-30BF |
| | R418 | 330k | ±5% | 1/2w | REC-20BF |
| | R419 | 27k | ±5% | 1/2w | REC-20BF |
| | R420 | 1.2k | ±10% | 1/2w | REC-20BF |
| | R421 | 18k | ±5% | 1/2w | REC-20BF |
| | R422 | 1M | ±5% | 1/2w | REC-20BF |
| | R423 | 1M | ±5% | 1/2w | REC-20BF |
| | R424 | 33k | ±5% | 1 w | REC-30BF |
| | R425 | 27 | ±5% | 1/2w | REC-20BF |
| | R426 | 150k | ±5% | 1/2w | REC-20BF |
| | R427 | 33 | ±5% | 1/2w | REC-20BF |
| | R428 | 3.3M | ±5% | 1/2w | REC-20BF |
| | R429 | 3.3M | ±5% | 1/2w | REC-20BF |
| | R430 | 33k | ±5% | 1 w | REC-30BF |
| | R433 | 12k | ±1% | 1/2w | REF-70 |
| | R434 | 30k | ±1% | 1/2w | REF-70 |
| | R435 | 18k | ±5% | 1/2w | REC-20BF |
| | R436 | 6.8k | ±5% | 1 w | REC-30BF |
| | R437 | 47k | ±5% | 1 w | REC-30BF |
| | R438 | 330k | ±5% | 1/2w | REC-20BF |
| | R439 | 27k | ±5% | 1/2w | REC-20BF |
| | R440 | 1.2k | ±5% | 1/2w | REC-20BF |
| | R441 | 18k | ±5% | 1/2w | REC-20BF |
| | R442 | 1M | ±5% | 1/2w | REC-20BF |
| | R443 | 1M | ±5% | 1/2w | REC-20BF |
| | R444 | 10k | ±5% | 2 w | REC-41BF |
| | R445 | 36k | ±5% | 1/2w | REC-20BF |

| | | PART NO. (NOTE A) | | | |
|---|---|---|---|---|---|
| | R446 | 150k | ±5% | 1/2w | REC-20BF |
| | R447 | 33 | ±5% | 1/2w | REC-20BF |
| | R448 | 10k | ±5% | 2 w | REC-41BF |
| CAPACITORS (NOTE C) | C401 | 33 | ±10% | 500dcwv | COC-21(N750) |
| | C402 | 10 | ±0.5μμf | 500dcwv | COC-21(N750) |
| | C403 | 100 | ±10% | 500dcwv | COM-20B |
| | C404 | 100 | ±10% | 300dcwv | COM-20B |
| | C405 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C406 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C407 | 0.01μf | +100-0% | 300dcwv | COC-63 |
| | C408 | 10 | ±0.5μμf | 500dcwv | COC-21(N750) |
| | C409 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C410 | 0.01μf | +100-0% | 1000dcwv | COC-63 |
| | C411 | 33 | ±10% | 500dcwv | COC-21(N750) |
| | C412 | 10 | ±0.5μμf | 500dcwv | COC-21(N750) |
| | C413 | 100 | ±10% | 500dcwv | COM-20B |
| | C414 | 100 | ±10% | 500dcwv | COM-20B |
| | C415 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C416 | 0.01μf | +100-0% | 500dcwv | COC-63 |
| | C417 | 7-45 | ±10% | 500dcwv | COT-12 |
| | C418 | 22 | ±10% | 500dcwv | COM-20B |
| | C419 | 10 | ±0.5μμf | 500dcwv | COC-21(N750) |
| | C420 | 0.01μf | +100-0% | 1000dcwv | COC-63 |
| | C421 | 10 | ±0.5μμf | 500dcwv | COC-21(N750) |
| | C422 | 10 | ±0.5μμf | 500dcwv | COC-21(N750) |
| | D401 | CRYSTAL DIODE | | | 1N34-A |
| | D402 | CRYSTAL DIODE | | | 1N34-A |
| | L401 | CHOKE 500μh | | | CHA-597A |
| | L411 | CHOKE 500μh | | | CHA-597A |
| | PL401 | PLUG | | | CDMP-11-12 |
| | S401 | SWITCH | | | SWRW-176 |
| | T401 | TRANSFORMER | | | 1391-45 |
| | T402 | TRANSFORMER | | | 1391-45 |
| | V401 | TUBE | | | 12AX7 |
| | V402 | TUBE | | | 12AX7 |
| | V403 | TUBE | | | 6485 or 6AH6WA |
| | V404 | TUBE | | | 6485 or 6AH6WA |
| | V405 | TUBE | | | 6485 or 6AH6WA |
| | V406 | TUBE | | | 6485 or 6AH6WA |

For explanation of NOTES, refer to page 42.




RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED
RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED
K = 1000 OHMS M = 1 MEGOHM
CAPACITANCE VALUES ONE AND OVER IN MICRO MICROFARADS, LESS THAN ONE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED

○ PANEL CONTROL
⊘ SCREW DRIVER ADJUSTMENT
* HEATER CABLE CONNECTIONS SHOWN IN FIGURE 5.5b.

**Figure 5.4. Schematic Diagram for Pulse-Timing Circuits.**

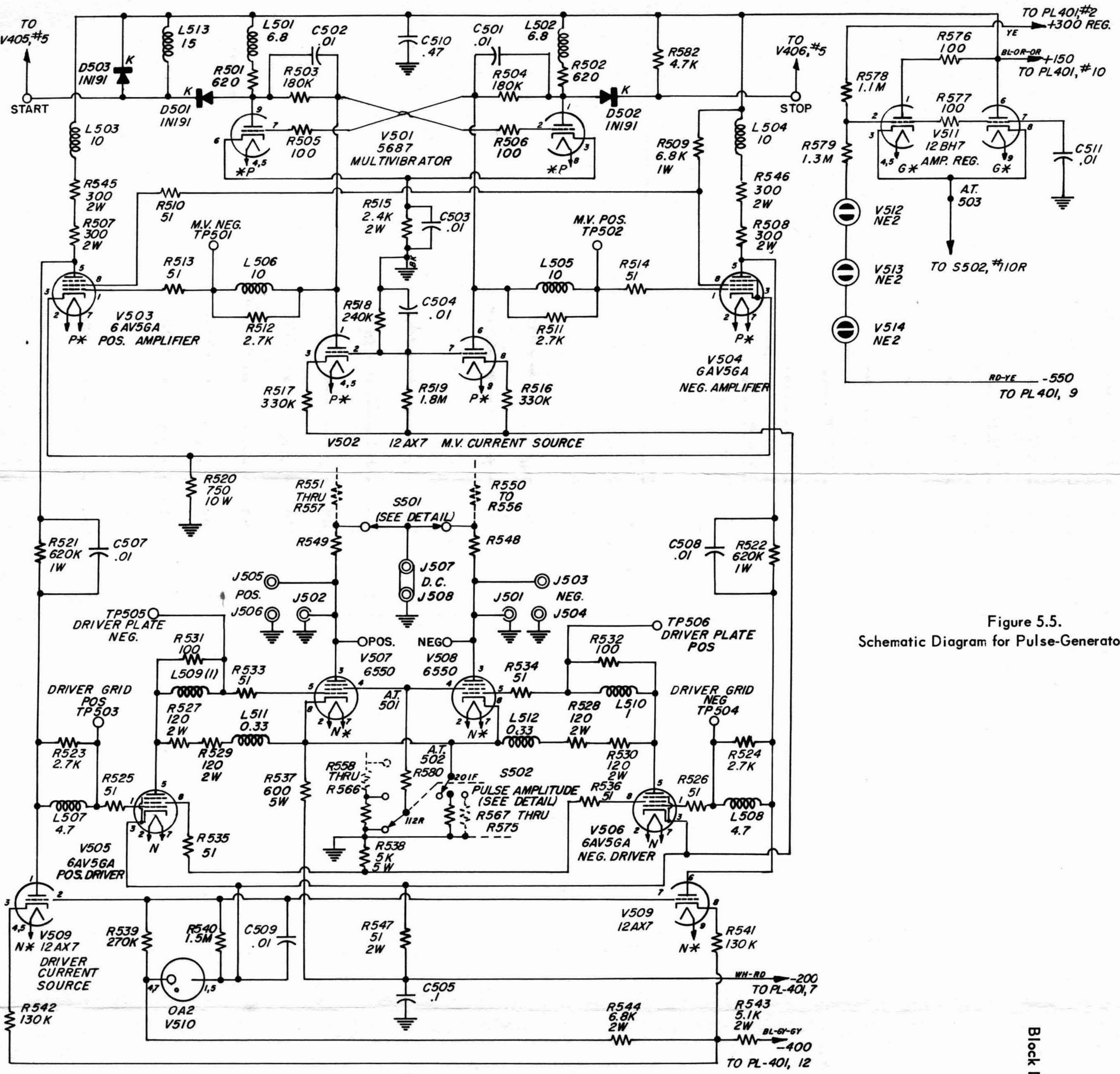
PARTS LIST

| | | PART NO. (NOTE A) | | | |
|---|---|---|---|---|---|
| RESISTORS (NOTE B) | R501 | 620 | ±5% | 1/2w | REC-20BF |
| | R502 | 620 | ±5% | 1/2w | REC-20BF |
| | R503 | 180k | ±1% | 1/2w | REF-70 |
| | R504 | 180k | ±1% | 1/2w | REF-70 |
| | R505 | 100 | ±5% | 1/2w | REC-20BF |
| | R506 | 100 | ±5% | 1/2w | REC-20BF |
| | R507 | 300 | ±5% | 2 w | REC-41BF |
| | R508 | 300 | ±5% | 2 w | REC-41BF |
| | R509 | 6.8k | ±5% | 1 w | REC-30BF |
| | R510 | 51 | ±5% | 1/2w | REC-20BF |
| | R511 | 2.7k | ±5% | 1/2w | REC-20BF |
| | R512 | 2.7k | ±5% | 1/2w | REC-20BF |
| | R513 | 51 | ±5% | 1/2w | REC-20BF |
| | R514 | 51 | ±5% | 1/2w | REC-20BF |
| | R515 | 2.4k | ±5% | 2 w | REC-41BF |
| | R516 | 330k | ±1% | 1/2w | REF-70 |
| | R517 | 330k | ±1% | 1/2w | REF-70 |
| | R518 | 240k | ±1% | 1/2w | REF-70 |
| | R519 | 1.8M | ±1% | 1/2w | REF-70 |
| | R520 | 750 | ±5% | 10 w | REPO-44 |
| | R521 | 620k | +1% | 1 w | REF-75 |
| | R522 | 620k | ±1% | 1 w | REF-75 |
| | R523 | 2.7k | ±5% | 1/2w | REC-20BF |
| | R524 | 2.7k | ±5% | 1/2w | REC-20BF |
| | R525 | 51 | ±5% | 1/2w | REC-20BF |
| | R526 | 51 | ±5% | 1/2w | REC-20BF |
| | R527 | 120 | ±5% | 2 w | REC-41BF |
| | R528 | 120 | ±5% | 2 w | REC-41BF |
| | R529 | 120 | ±5% | 2 w | REC-41BF |
| | R530 | 120 | ±5% | 2 w | REC-41BF |
| | R531 | 100 | ±5% | 1/2w | REC-20BF |
| | R532 | 100 | ±5% | 1/2w | REC-20BF |
| | R533 | 51 | ±5% | 1/2w | REC-20BF |
| | R534 | 51 | ±5% | 1/2w | REC-20BF |
| | R535 | 51 | ±5% | 1/2w | REC-20BF |
| | R536 | 51 | ±5% | 1/2w | REC-20BF |
| | R537 | 600 | ±5% | 5 w | REPO-42 |
| | R538 | 5k | ±5% | 5 w | REPO-42 |
| | R539 | 270k | ±1% | 1/2w | REF-70 |
| | R540 | 1.5M | ±1% | 1/2w | REF-70 |
| | R541 | 130k | ±1% | 1/2w | REF-70 |
| | R542 | 130k | ±1% | 1/2w | REF-70 |
| | R543 | 5.1k | ±5% | 2 w | REC-41BF |
| | R544 | 6.8k | ±5% | 2 w | REC-41BF |
| | R545 | 300 | ±5% | 2 w | REC-41BF |
| | R546 | 300 | ±5% | 2 w | REC-41BF |
| | R547 | 51 | ±5% | 2 w | REC-41BF |
| | R548 | 51 | ±5% | 2 w | REC-41BF |
| | R549 | 51 | ±5% | 2 w | REC-41BF |
| | R550 | 22 | ±5% | 1 w | REC-30BF |
| | R551 | 22 | ±5% | 1 w | REC-30BF |
| | R552 | 22 | ±5% | 1 w | REC-30BF |
| | R553 | 22 | ±5% | 1 w | REC-30BF |
| | R554 | 56 | ±5% | 2 w | REC-41BF |
| | R555 | 56 | ±5% | 2 w | REC-41BF |
| | R556 | 470 | ±5% | 10 w | REPO-42-2 |
| | R557 | 470 | ±5% | 10 w | REPO-42-2 |
| | R558 | 680 | ±5% | 1/2w | REC-20BF |
| | R559 | 750 | ±5% | 1/2w | REC-20BF |
| | R560 | 1k | ±5% | 1/2w | REC-20BF |
| | R561 | 1.5k | ±5% | 1/2w | REC-20BF |

| | | PART NO. (NOTE A) | | | |
|---|---|---|---|---|---|
| | R562 | 2.2k | ±5% | 1/2w | REC-20BF |
| | R563 | 2.7k | ±5% | 1/2w | REC-20BF |
| | R564 | 3k | ±5% | 1/2w | REC-20BF |
| | R565 | 3.6k | ±5% | 1/2w | REC-20BF |
| | R566 | 3.9k | ±5% | 1/2w | REC-20BF |
| | R567 | 8.2k | ±5% | 5 w | REPO-43 |
| | R568 | 10k | ±5% | 5 w | REPO-43 |
| | R569 | 10k | ±5% | 5 w | REPO-43 |
| | R570 | 7.5k | ±5% | 5 w | REPO-43 |
| | R571 | 6.2k | ±5% | 5 w | REPO-43 |
| | R572 | 5.6k | ±5% | 5 w | REPO-43 |
| | R573 | 13k | ±5% | 2 w | REC-41BF |
| | R574 | 13k | ±5% | 2 w | REC-41BF |
| | R575 | 13k | ±5% | 2 w | REC-41BF |
| | R576 | 100 | ±5% | 1/2w | REC-20BF |
| | R577 | 100 | ±5% | 1/2w | REC-20BF |
| | R578 | 1.1M | ±5% | 1/2w | REC-20BF |
| | R579 | 1.3M | ±5% | 1/2w | REC-20BF |
| | R580 | 22 | ±5% | 1/2w | REC-20BF |
| | R581 | 5.1k | ±5% | 1/2w | REC-20BF |
| | R582 | 4.7k | ±5% | 1/2w | REC-20BF |
| CAPACITORS (NOTE C) | C501 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| | C502 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| | C503 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| | C504 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| | C505 | 0.1µf | ±10% | 400dcwv | COW-25 |
| | C507 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| | C508 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| | C509 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| | C510 | 0.47µf | ±10% | 200dcwv | COW-16 |
| | C511 | 0.01µf | +100-0% | 500dcwv | COC-63 |
| | D501 | CRYSTAL DIODE | | | 1N191 |
| | D502 | CRYSTAL DIODE | | | 1N191 |
| | D503 | CRYSTAL DIODE | | | 1N191 |
| | L501 | 6.8 µh | ±10% | | CHM-1 |
| | L502 | 6.8 µh | ±10% | | CHM-1 |
| | L503 | 10 µh | ±10% | | CHM-1 |
| | L504 | 10 µh | ±10% | | CHM-1 |
| | L505 | 10 µh | ±10% | | CHM-1 |
| | L506 | 10 µh | ±10% | | CHM-1 |
| | L507 | 4.7 µh | ±10% | | CHM-1 |
| | L508 | 4.7 µh | ±10% | | CHM-1 |
| | L509 | 1 µh | ±10% | | CHM-1 |
| | L510 | 1 µh | ±10% | | CHM-1 |
| | L511 | 0.33 µh | ±10% | | CHM-1 |
| | L512 | 0.33 µh | ±10% | | CHM-1 |
| | L513 | 15 µh | ±10% | | CHM-1 |
| | L514 | 4.7 µh | ±10% | | CHM-1 |
| | L515 | 4.7 µh | ±10% | | CHM-1 |
| | S501 | SWITCH, Rotary | | | SWRW-83 |
| | S502 | SWITCH, Rotary | | | SWRW-177 |

| | | | | |
|---|---|---|---|---|
| TUBES | V501 | 5687 | V508 | 6550 |
| | V502 | 12AX7 | V509 | 12AX7 |
| | V503 | 6AV5GA | V510 | OA2 |
| | V504 | 6AV5GA | V511 | 12BH7 |
| | V505 | 6AV5GA | V512 | NE-2 |
| | V506 | 6AV5GA | V513 | NE-2 |
| | V507 | 6550 | V514 | NE-2 |

For explanation of NOTES, refer to page 42.



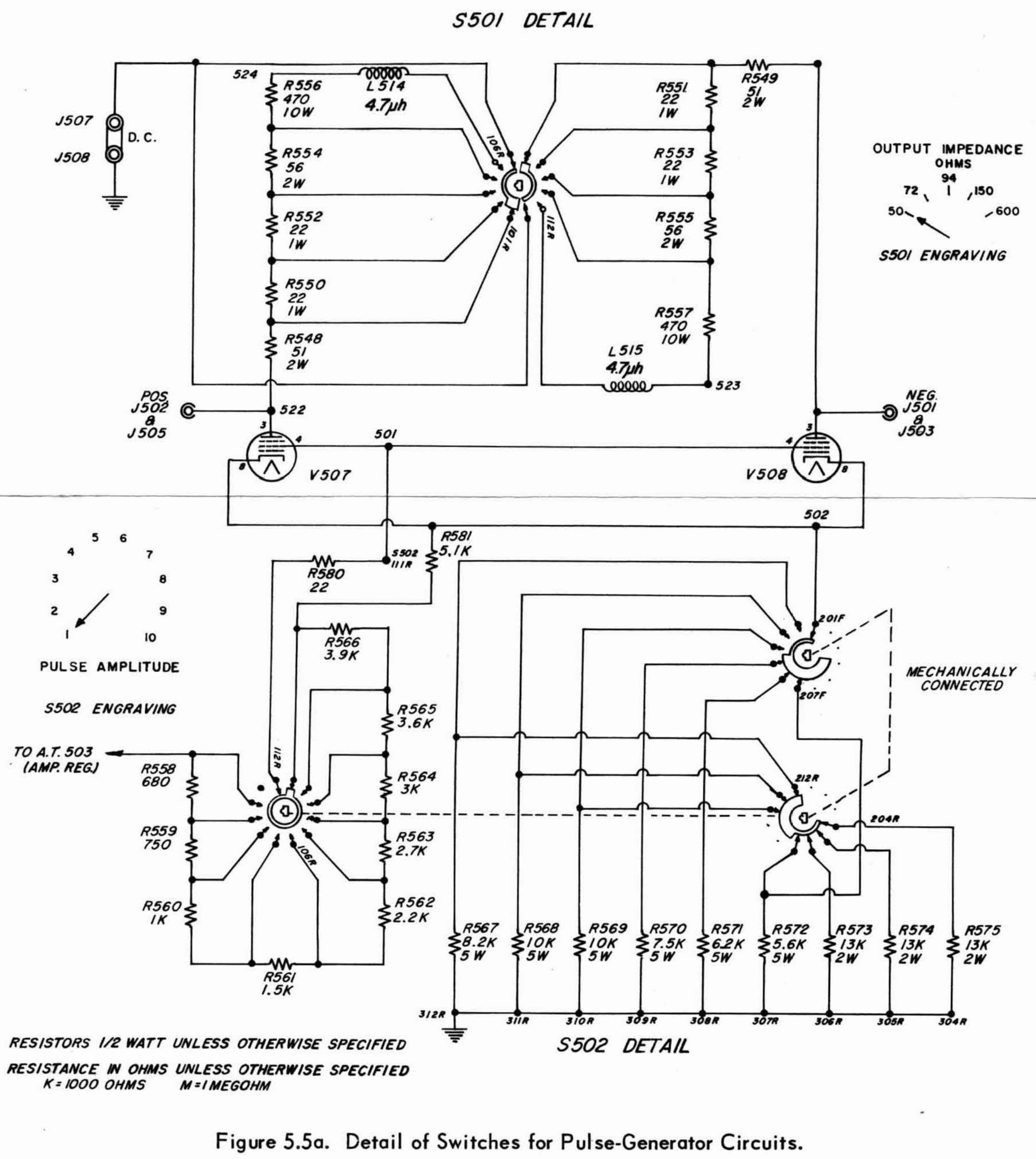

RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED

RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED
K= 1000 OHMS M = 1 MEGOHM

CAPACITANCE VALUES ONE AND OVER IN MICRO MICROFARADS, LESS THAN ONE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

HEATER CABLE CONNECTIONS SHOWN IN FIGURE 5.5b.

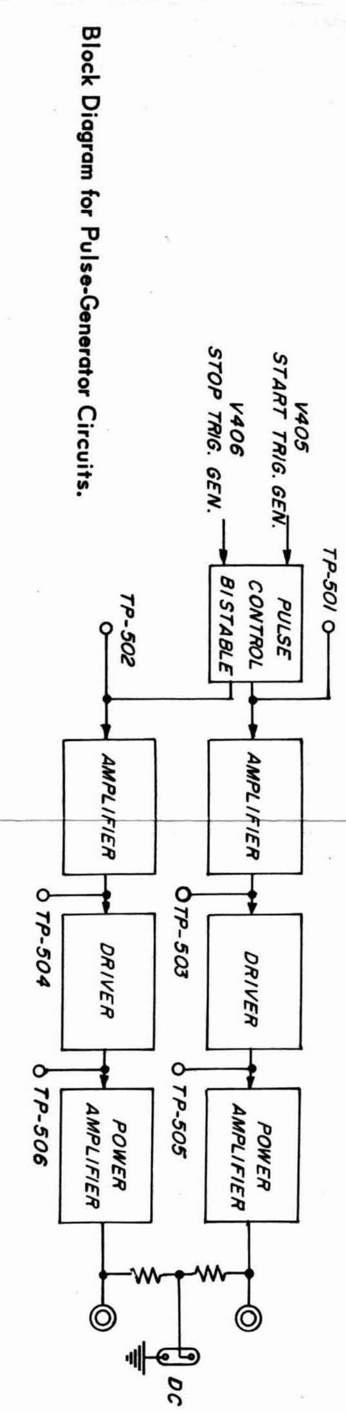
Figure 5.5.
Schematic Diagram for Pulse-Generator Circuits.




RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED

RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED
K=1000 OHMS M=1 MEGOHM

Figure 5.5a. Detail of Switches for Pulse-Generator Circuits.




Block Diagram for Pulse-Generator Circuits.

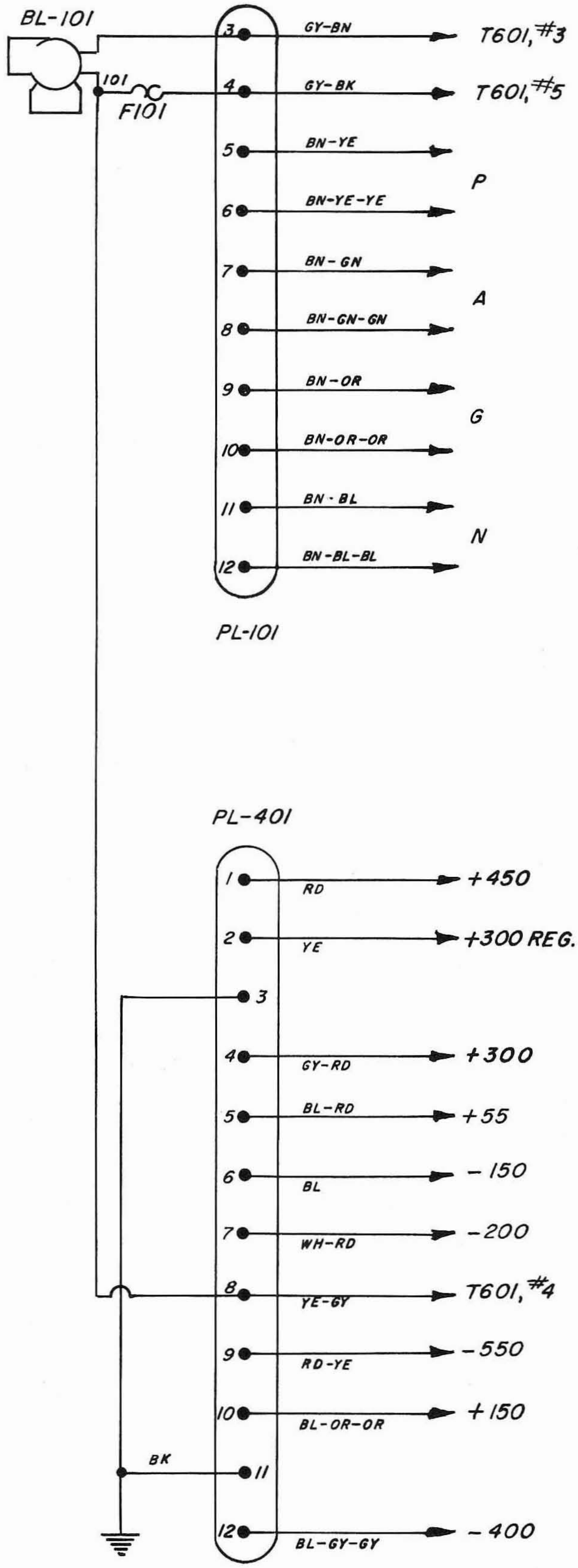


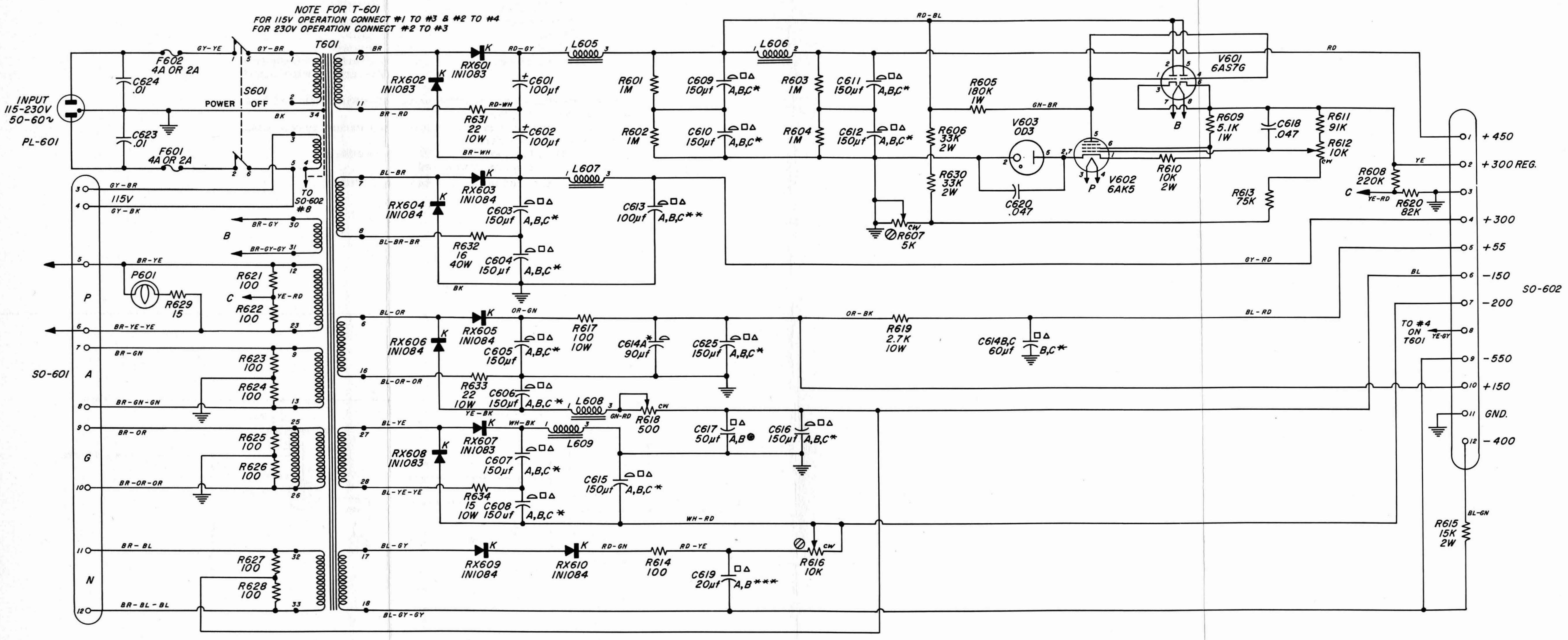

Figure 5.5b.
Detail of Plugs for Power Supply.

## PARTS LIST

| | | | | | PART NO. (NOTE A) |
|---|---|---|---|---|---|
| RESISTORS (NOTE B) | R601 | 1 M | ± 5% | 1/2 w | REC-20BF |
| | R602 | 1 M | ± 5% | 1/2 w | REC-20BF |
| | R603 | 1 M | ± 5% | 1/2 w | REC-20BF |
| | R604 | 1 M | ± 5% | 1/2 w | REC-20BF |
| | R605 | 180 k | ±10% | 1 w | REC-30BF |
| | R606 | 33 k | ±10% | 2 w | REC-41BF |
| | R607 | 5 k | ±10% | | POSW-3 |
| | R608 | 220 k | ± 5% | 1/2 w | REC-20BF |
| | R609 | 5.1 k | ± 5% | 1 w | REC-30BF |
| | R610 | 10 k | ± 5% | 2 w | REC-41BF |
| | R611 | 91 k | ± 1% | 1/2 w | REF-70 |
| | R612 | 10 k | ±10% | | POSW-3 |
| | R613 | 75 k | ± 1% | 1/2 w | REF-70 |
| | R614 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R615 | 15 k | ±10% | 2 w | REC-41BF |
| | R616 | 10 k | ±10% | | POSW-3 |
| | R617 | 100 | ± 5% | 10 w | REPO-22 |
| | R618 | 500 | ±10% | | POSW-3 |
| | R619 | 2.7 k | ± 5% | 10 w | REPO-22 |
| | R620 | 82 k | ± 5% | 1/2 w | REC-20BF |
| | R621 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R622 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R623 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R624 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R625 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R626 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R627 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R628 | 100 | ± 5% | 1/2 w | REC-20BF |
| | R629 | 15 | ±10% | 1/2 w | REW-3C |
| | R630 | 33 k | ±10% | 2 w | REC-41BF |
| | R631 | 22 | ±10% | 10 w | REPO-22 |
| | R632 | 16 | ±10% | 40 w | REPO-21P |
| | R633 | 22 | ±10% | 10 w | REPO-22 |
| | R634 | 15 | ±10% | 10 w | REPO-22 |
| CAPACITORS (NOTE C) | C601 | 100 | | 150 dcwv | COE-45 |
| | C602 | 100 | | 150 dcwv | COE-45 |
| | C603A | 90 | | | |
| | C603B | 30 | | 300 dcwv | COE-52 |
| | C603C | 30 | | | |
| | C604A | 90 | | | |
| | C604B | 30 | | 300 dcwv | COE-52 |
| | C604C | 30 | | | |
| | C605A | 90 | | | |
| | C605B | 30 | | 300 dcwv | COE-52 |
| | C605C | 30 | | | |
| | C606A | 90 | | | |
| | C606B | 30 | | 300 dcwv | COE-52 |
| | C606C | 30 | | | |
| | C607A | 90 | | | |
| | C607B | 30 | | 300 dcwv | COE-52 |
| | C607C | 30 | | | |
| | C608A | 90 | | | |
| | C608B | 30 | | 300 dcwv | COE-52 |
| | C608C | 30 | | | |
| | C609A | 90 | | | |
| | C609B | 30 | | 300 dcwv | COE-52 |
| | C609C | 30 | | | |
| | C610A | 90 | | | |
| | C610B | 30 | | 300 dcwv | COE-52 |
| | C610C | 30 | | | |

| | | | | PART NO. (NOTE A) |
|---|---|---|---|---|
| C611A | 90 | | | |
| C611B | 30 | | 300 dcwv | COE-52 |
| C611C | 30 | | | |
| C612A | 90 | | | |
| C612B | 30 | | 300 dcwv | COE-52 |
| C612C | 30 | | | |
| C613A | 50 | | | |
| C613B | 25 | | 450 dcwv | COE-10 |
| C613C | 25 | | | |
| C614A | 90 | | | |
| C614B | 30 | | 300 dcwv | COE-52 |
| C614C | 30 | | | |
| C615A | 90 | | | |
| C615B | 30 | | 300 dcwv | COE-52 |
| C615C | 30 | | | |
| C616A | 90 | | | |
| C616B | 30 | | 300 dcwv | COE-52 |
| C616C | 30 | | | |
| C617A | 25 | | 200 dcwv | COE-51 |
| C617B | 25 | | | |
| C618 | 0.047 | ±10% | 200 dcwv | COW-16 |
| C619A | 10 | | 450 dcwv | COE-5 |
| C619B | 10 | | | |
| C620 | 0.047 | ±10% | 400 dcwv | COW-25 |
| C623 | 0.01 | ±10% | 600 dcwv | COL-71 |
| C624 | 0.01 | ±10% | 600 dcwv | COL-71 |
| C625A | 90 | | | |
| C625B | 30 | | 300 dcwv | COE-52 |
| C625C | 30 | | | |
| F601 | FUSE, 4 amp, Slo-Blo Type 3AG (for 115-v input) | | | FUF-1 |
| F601 | FUSE, 2 amp, Slo-Blo Type 3AG (for 230-v input) | | | FUF-1 |
| F602 | FUSE, 4 amp, Slo-Blo Type 3AG (for 115-v input) | | | FUF-1 |
| F602 | FUSE, 2 amp, Slo-Blo Type 3AG (for 230-v input) | | | FUF-1 |
| L605 | CHOKE | | | 485-406 |
| L606 | CHOKE | | | 485-456 |
| L607 | CHOKE | | | 485-406 |
| L608 | CHOKE | | | 485-406 |
| L609 | CHOKE | | | 485-406 |
| P601 | PILOT LAMP, 6.3 v, Mazda #44 | | | 2LAP-939 |
| PL601 | PLUG, Input | | | ZCDPP-10 |
| RX601 | RECTIFIER | | | 1N1083 |
| RX602 | RECTIFIER | | | 1N1083 |
| RX603 | RECTIFIER | | | 1N1084 |
| RX604 | RECTIFIER | | | 1N1084 |
| RX605 | RECTIFIER | | | 1N1084 |
| RX606 | RECTIFIER | | | 1N1084 |
| RX607 | RECTIFIER | | | 1N1083 |
| RX608 | RECTIFIER | | | 1N1083 |
| RX609 | RECTIFIER | | | 1N1084 |
| RX610 | RECTIFIER | | | 1N1084 |
| S601 | SWITCH, dpst | | | SWT-333NP |
| T601 | TRANSFORMER | | | 565-419 |
| V601 | TUBE | | | 6AS7-G |
| V602 | TUBE | | | 6AK5 |
| V603 | TUBE | | | OD3 |

For explanation of NOTES, refer to page 42.




RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED

RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED
K=1000 OHMS M= 1 MEGOHM

CAPACITANCE VALUES ONE AND OVER IN MICRO MICROFARADS, LESS THAN ONE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

⊘ SCREWDRIVER ADJUSTMENT

* A SECTION 90uf, B & C SECTIONS 30μf — 300WV

** A SECTION 50uf, B & C SECTIONS 25μf — 450WV

*** A & B SECTIONS 10μf — 450 WV

⊗ A & B SECTIONS 25μf — 200WV

Figure 5.6. Schematic Diagram for Type 1391-B Power Supply.

NOTES

(A) Type designations for resistors and capacitors are as follows:

| Capacitors | Resistors |
|---|---|
| COC-ceramic | REC-composition |
| COL-oil | REF-film |
| COM-mica | REPO-power |
| COP-polystyrene | POSC-variable composition |
| | POSW-variable wire-wound |

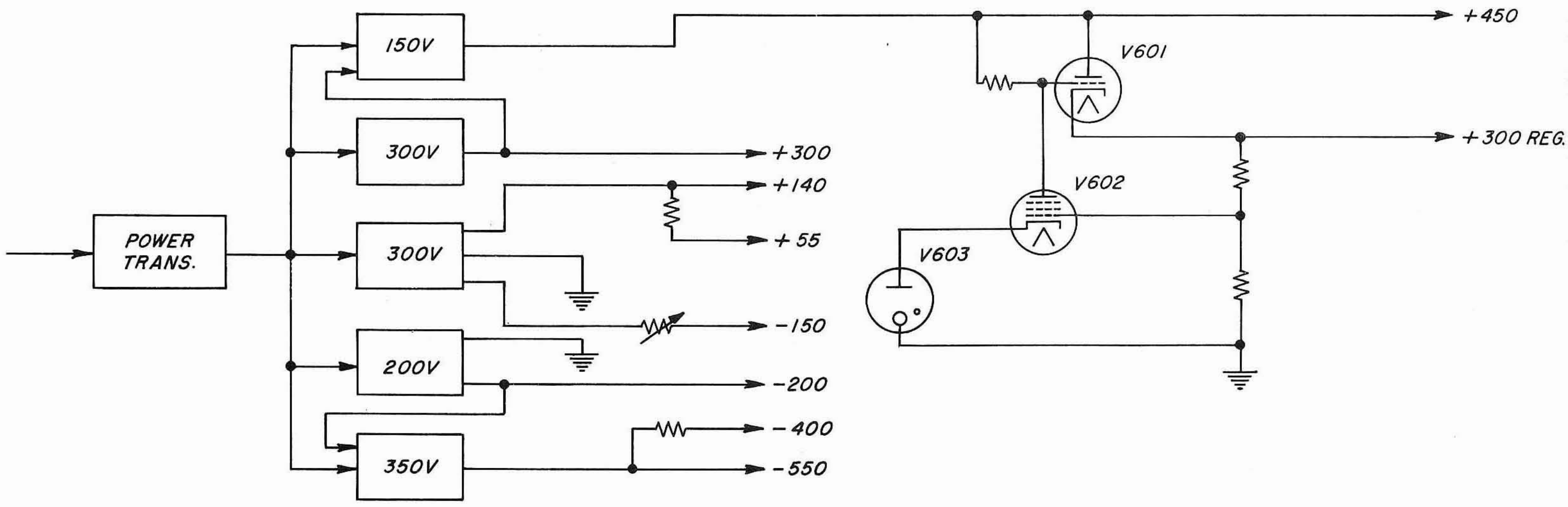
(B) All resistances are in ohms unless otherwise indicated by k (kilohms) or M (megohms).

(C) Capacitances are in micromicrofarads except as otherwise indicated by µf (microfarads).

(D) Sections A, B, C, are 90, 30, 30 µf, respectively.

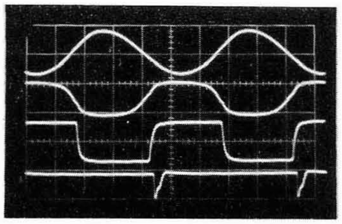
(E) Capacitances are in microfarads.

(F) Value determined in General Radio laboratory.



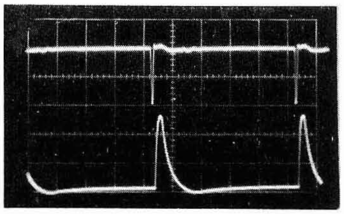

Elementary Schematic Diagram for Type 1391-P2 Power Supply.

Figure 5.7. Test Waveforms



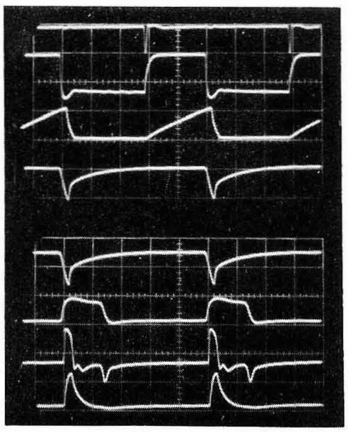
**1. INPUT CIRCUITS 100 kc 2$\mu$sec/cm**

A. INPUT SIGNAL 5v/cm
B. TP101 (INPUT AMP) 20v/cm
C. TP102 (DIR TRIG SCHMITT) 50v/cm
D. TP103 (DIR TRIG GEN) 20v/cm



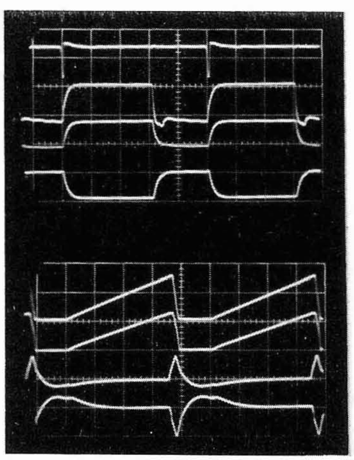
**2. INPUT CIRCUITS**

A. DIRECT TRIG 5v/cm (8-$\mu\mu$f probe)
B. DIR SYNC PULSE 50v/cm



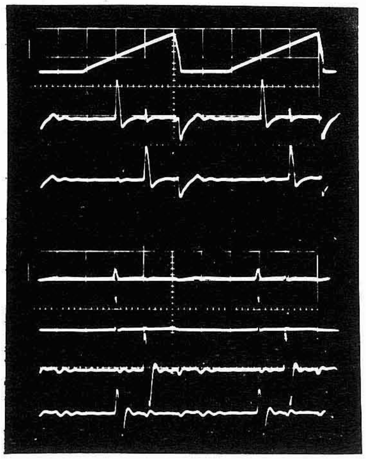
**3. DELAY CIRCUITS 100 kc 2$\mu$sec/cm, DELAY SET FOR 4$\mu$sec.**

A. DIRECT TRIG 10v/cm
B. TP201 (POS DEL GATE) 50v/cm
C. TP202 (DEL SWEEP) 50v/cm
D. TP203 (DEL RESET PULSE) 50v/cm
E. TP203 (DEL RESET PULSE) 50v/cm
F. TP204 (COINC GATE) 50v/cm (3$\mu$sec)
G. TP205 (DELAY TRIG INV) 5v/cm
H. DELAYED SYNC 100v/cm



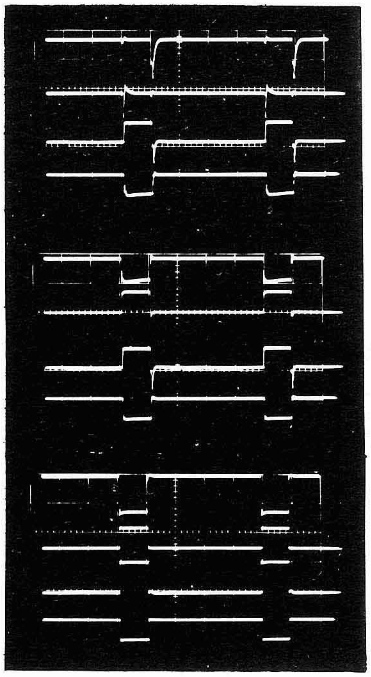
**4. SWEEP CIRCUITS 100 kc 6$\mu$sec/cm**

A. SWEEP TRIGGER (DELAYED 4$\mu$sec) 10v/cm
B. GRID (7) V305 50v/cm
C. POS GATE 50v/cm
D. NEG GATE 50v/cm
E. TP301 (SWP GEN) 100v/cm
F. TP302, 303 (SWP CF) 100v/cm
G. TP304 (SWP RESET AMP COMP) 5v/cm
H. TP305 (SWP RESET TRIG) 20v/cm



**5. PULSE TIMING, 6-$\mu$sec SWEEP, 2-$\mu$sec DELAY, 2-$\mu$sec PULSE**

A. TP303 (SWP CF) 100v/cm
B. TP401 (START AMP COMP) 5v/cm
C. TP402 (STOP AMP COMP) 5v/cm
D. TP403 START PULSE 5v/cm
E. TP404 STOP PULSE 5v/cm
F. V405 GRID (PIN 1) 50v/cm
G. V406 GRID (PIN 1) 50v/cm



**6. PULSE GENERATOR**

A. STOP PULSE
B. START PULSE
C. V501 PLATE (PIN 9)
D. V501 PLATE (PIN 1)
E. TP501 (MV NEG) 20v/cm
F. TP503 (DRIVER GRID POS) 50v/cm
G. TP502 (MV POS) 20v/cm
H. TP504 (DRIVER GRID NEG) 50v/cm
I. TP505 (DRIVER PLATE NEG) 20v/cm
J. POS PULSE (94Ω) 20v/cm
K. TP506 (DRIVER PLATE POS) 20v/cm
L. NEG PULSE (94Ω) 20v/cm

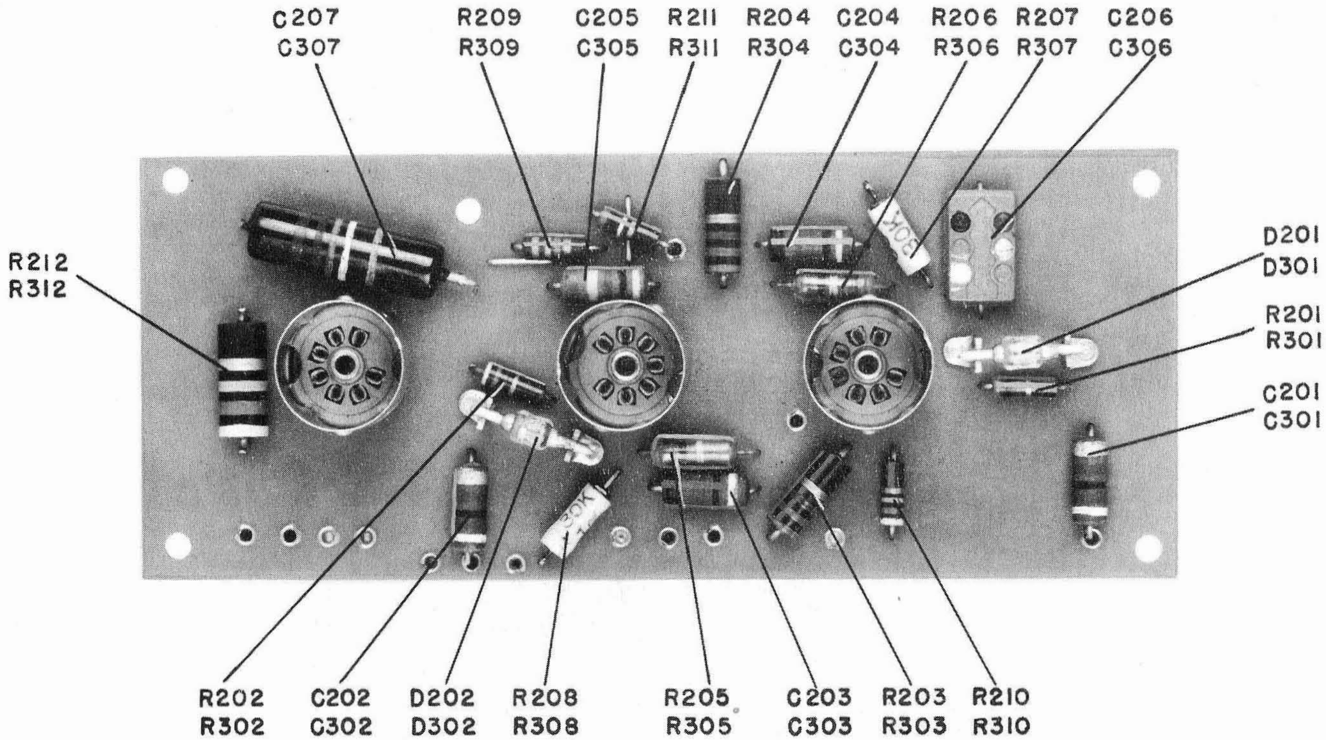



Figure 5.8. Multivibrator Shelf.

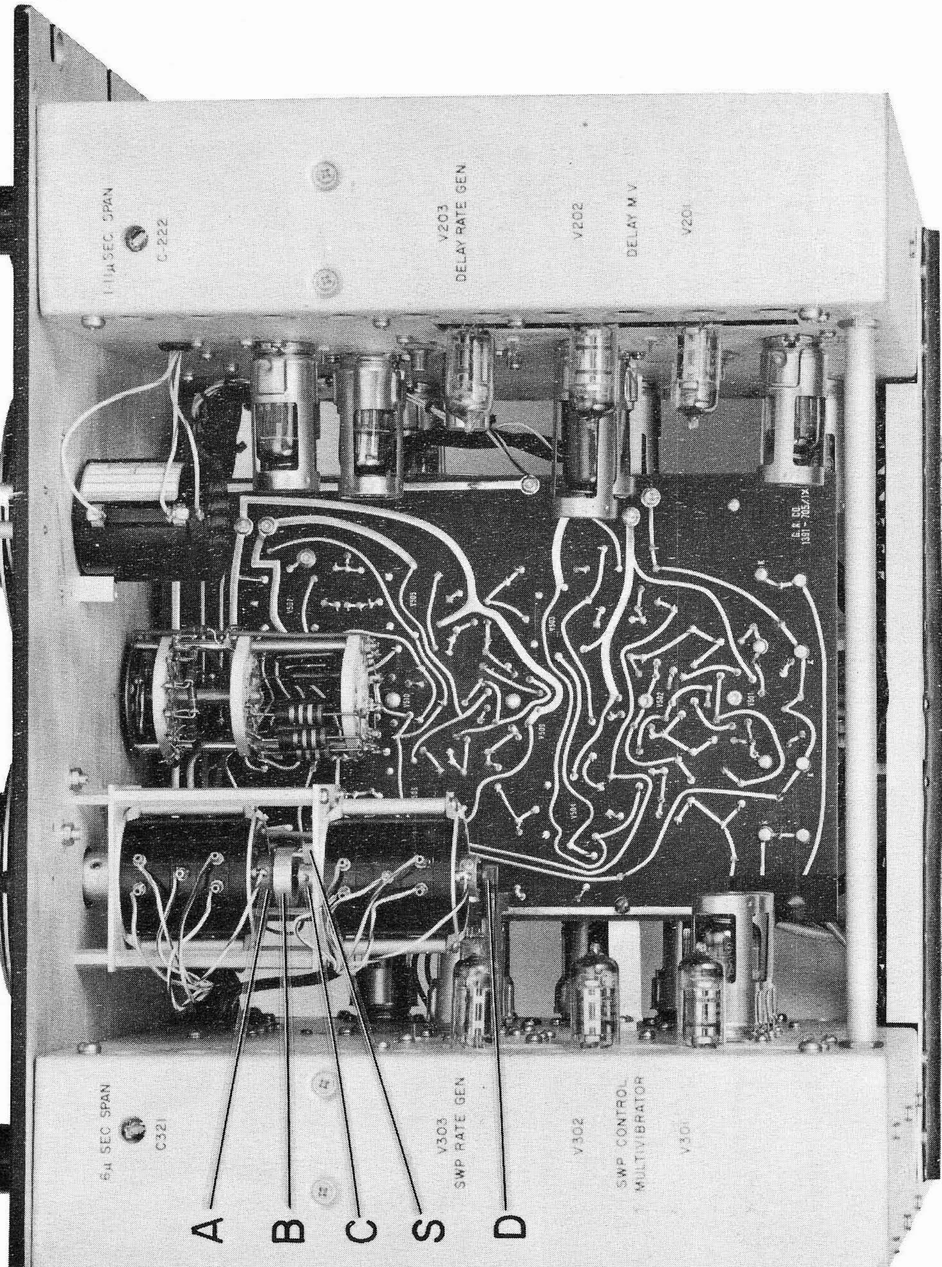



Figure 5.9. Top Interior View.

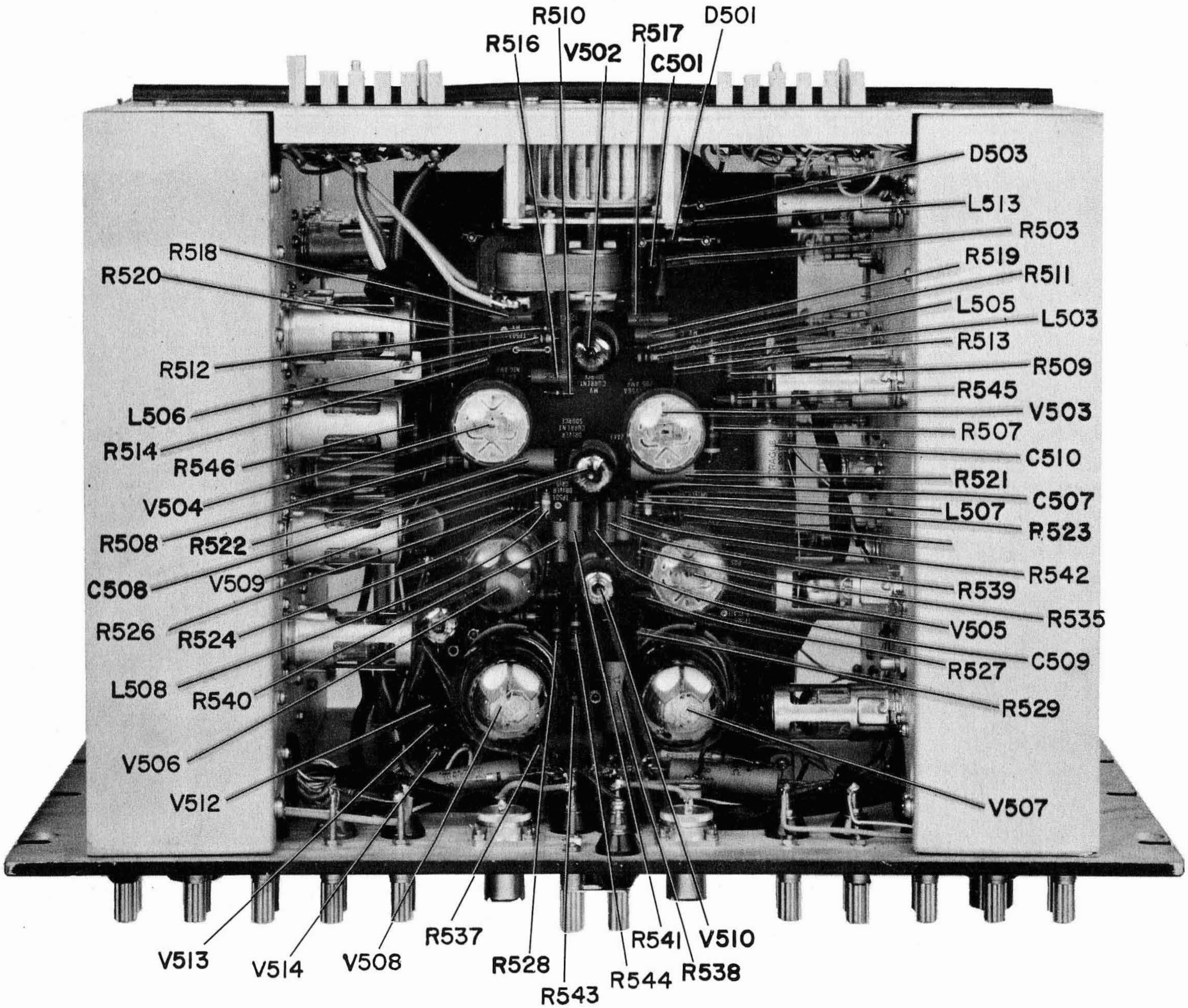
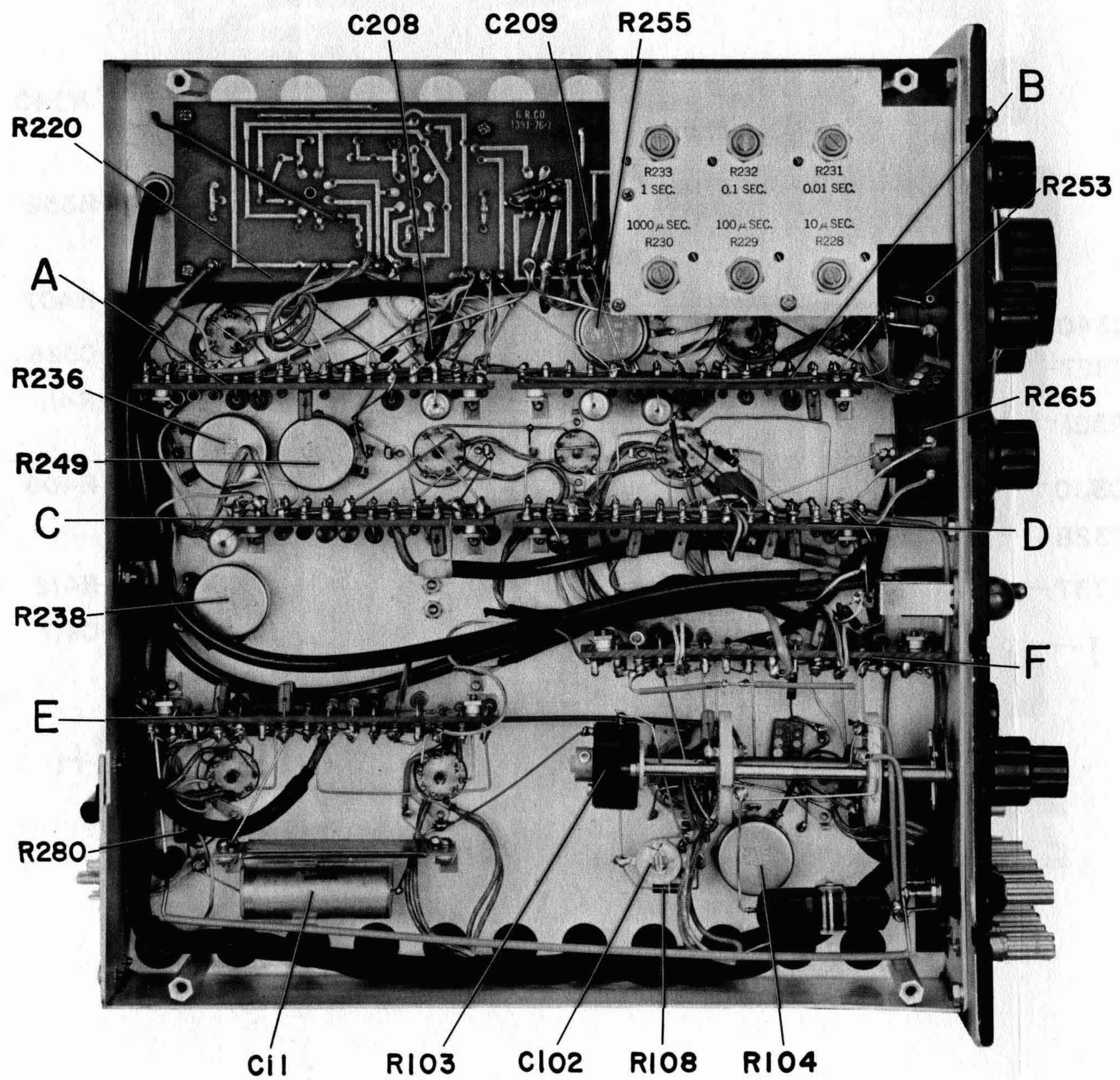



Figure 5.10. Bottom Interior View.



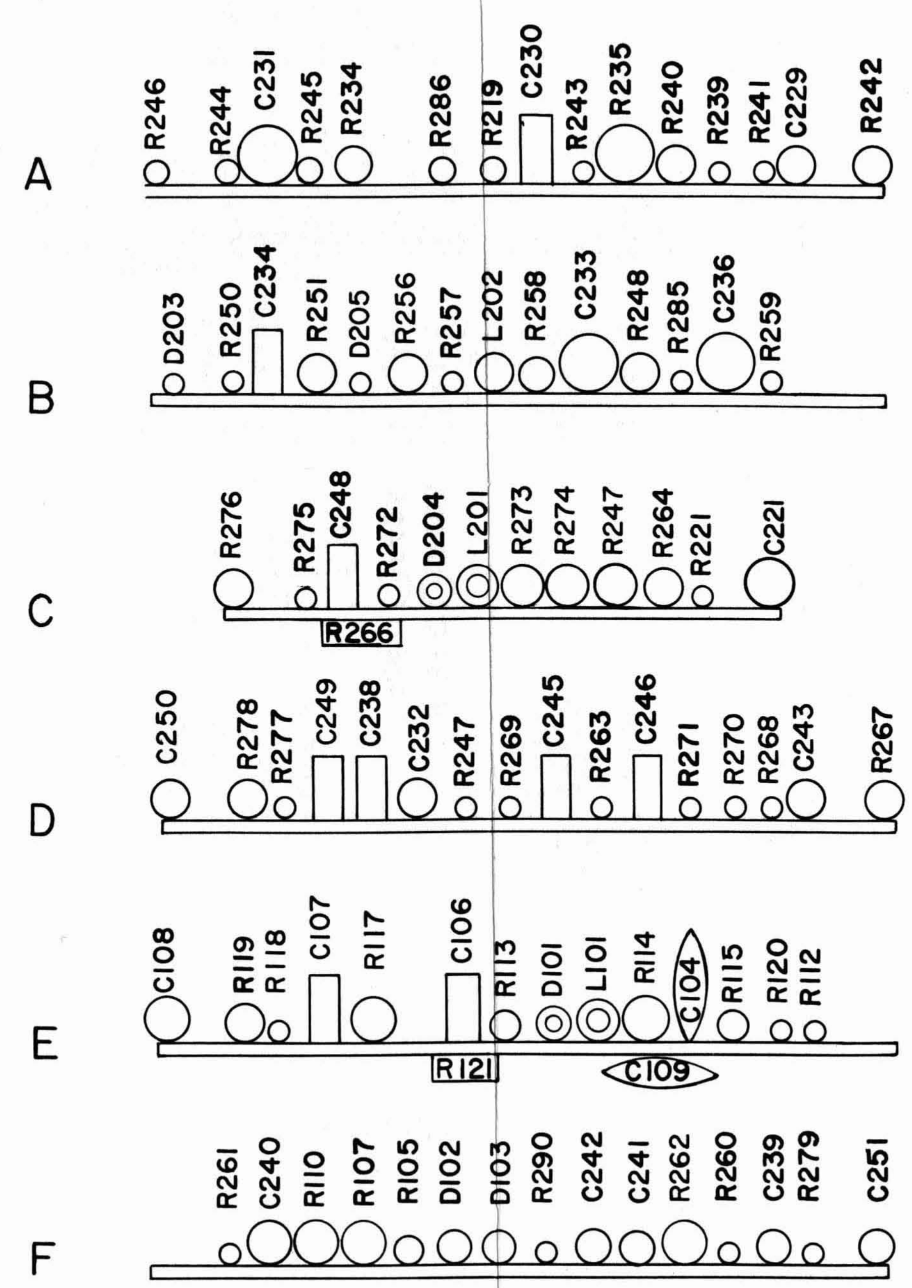




Figure 5.11. Left Side Interior View.

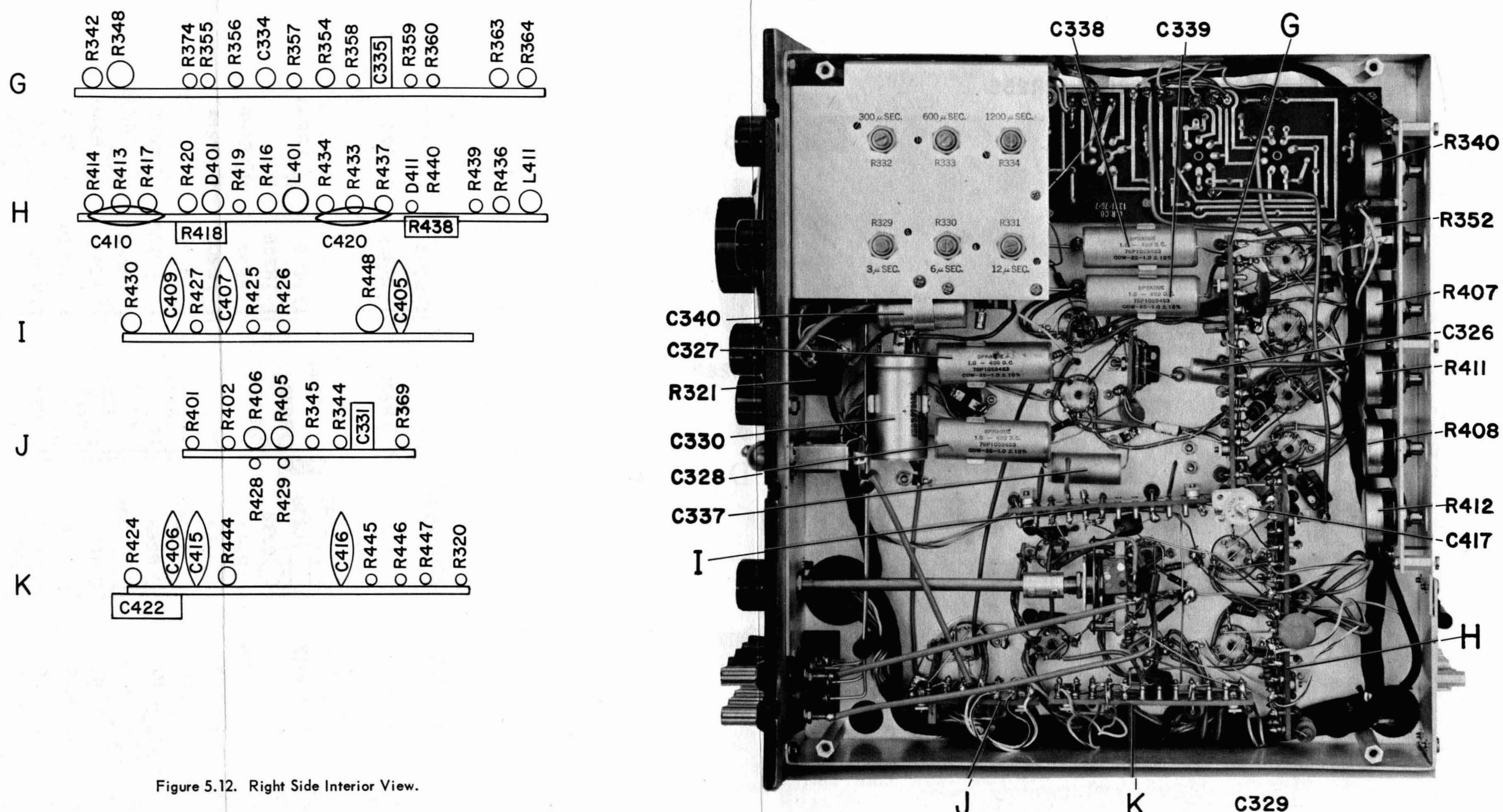



Figure 5.12. Right Side Interior View.

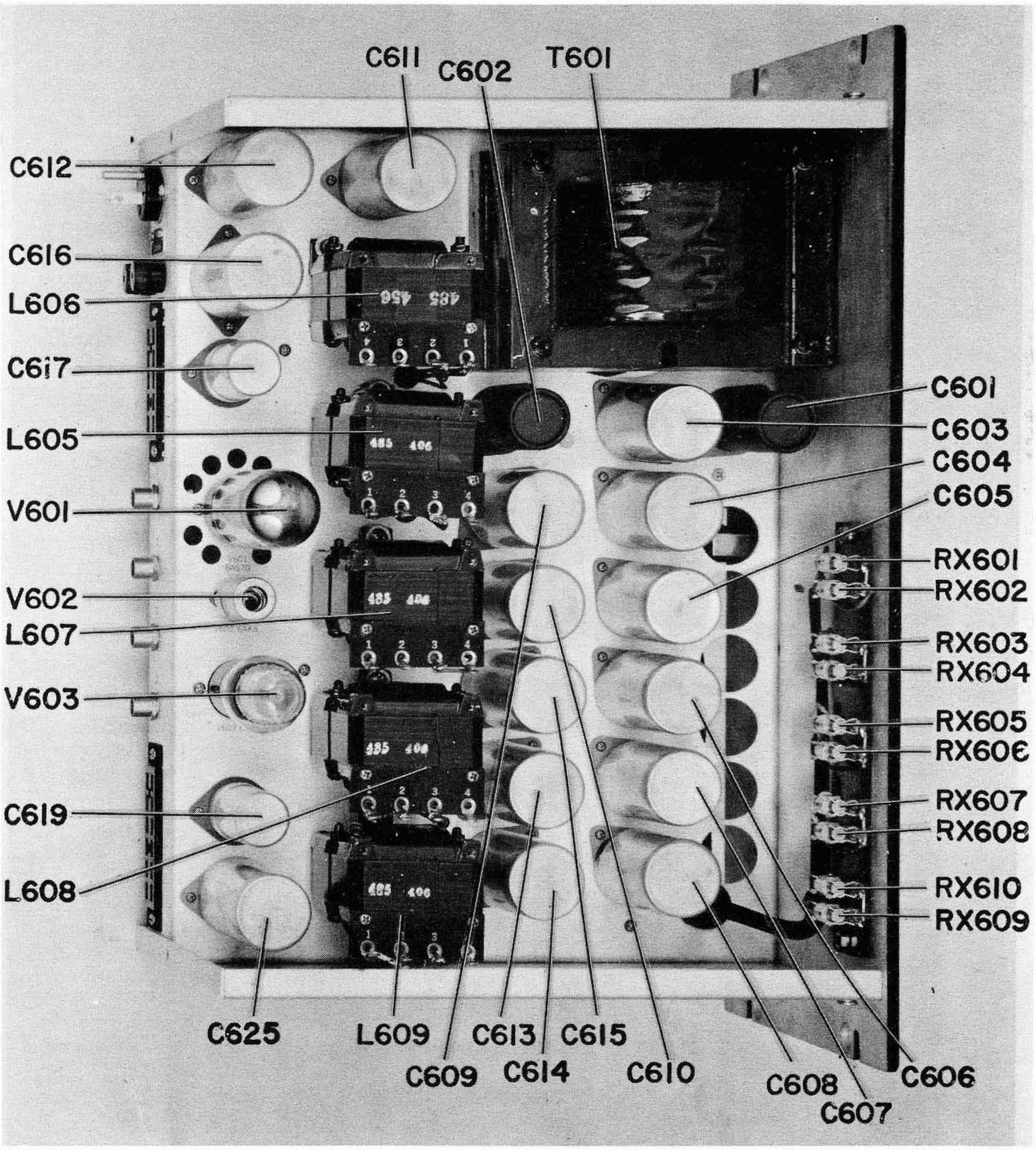



Figure 5.13. Top Interior View of Power Supply.

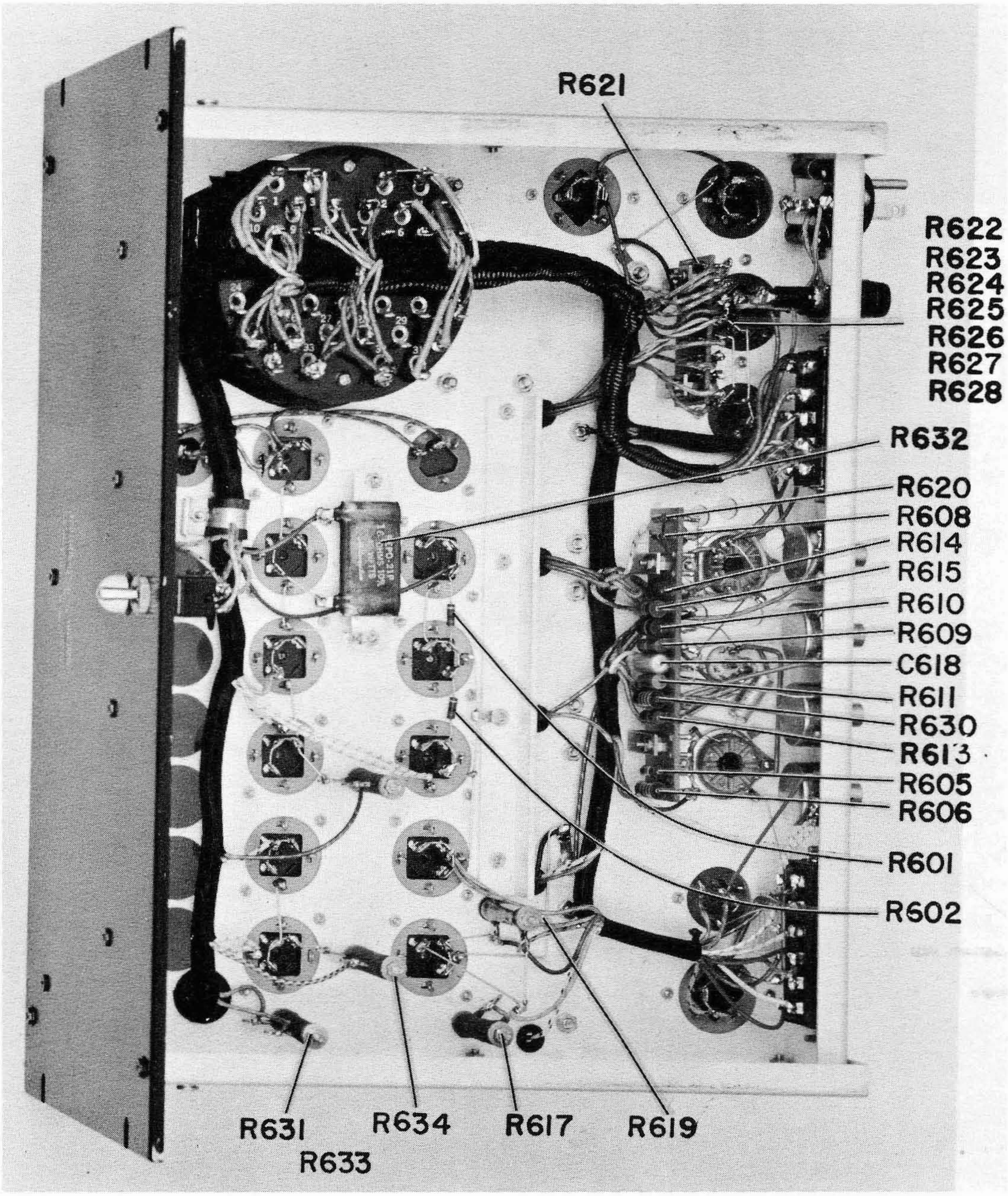



Figure 5.14. Bottom Interior View of Power Supply.

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