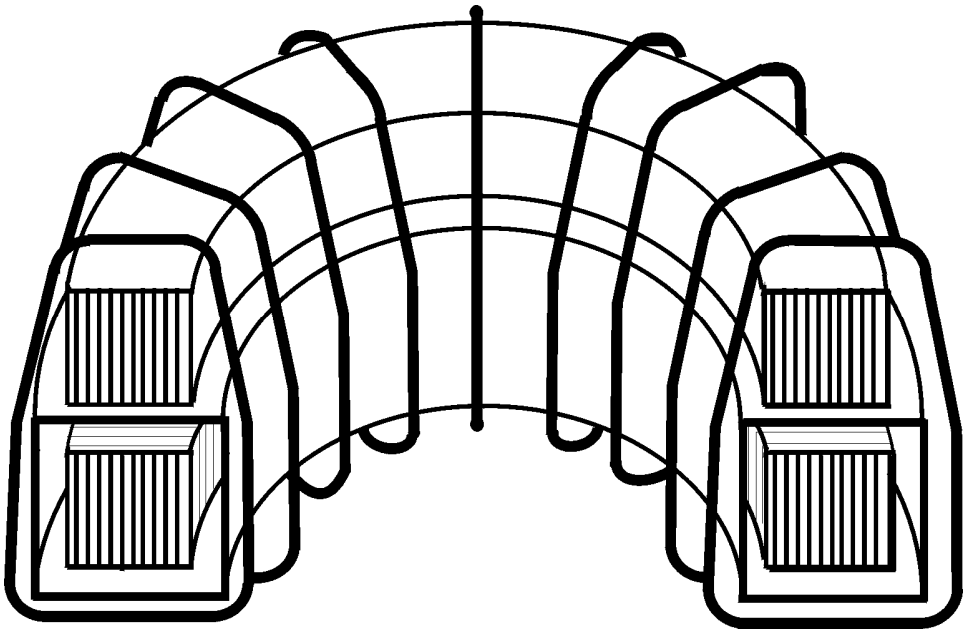
NIST Technical Note 1473

Transformer-Like Devices for High-Accuracy AC Current Measurements

T. M. Souders



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James M. Turner, Deputy Director

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FOREWORD

Between 1967 and 1975, the author conducted the calibration services for instrument current transformers at the National Bureau of Standards (now National Institute of Standards and Technology), and upgraded the facilities used in those services. In addition, he developed and implemented a new measurement service for low-value ac resistors. Much of the material included in this Technical Note derives from work during that period. Remarkably, the field has not changed dramatically over the intervening years.

The period from about 1958 to 1970 saw renewed interest in transformer-like devices as solutions to a variety of electrical measurement problems, and development programs were undertaken at a number of national laboratories and universities. Many of these led to new types of devices having vastly improved accuracy, making it possible to scale and measure impedances, ac voltage and current, and power and energy, with unprecedented accuracy. During this period, an ongoing collaboration between P. N. Miljanic of the Institut Nikola Tesla in Belgrade, Yugoslavia and N. L. Kusters and W. J. M. Moore of the National Research Council (NRC) in Ottawa, Canada, led to the development of the modern current comparator. This represented a new class of transformer-like devices with remarkably increased accuracy over conventional current transformers. O. Petersons, also with NRC during part of that time, extended and applied the work of that group, particularly to the field of high voltage measurements. Many of these developments were available to the author as he began the design of the new measurement services at NBS. Around 1968 Petersons left NRC to take a position at NBS and the author was fortunate to have him as a mentor during the first few years of his career. Many of the ideas and approaches set forth in this document, especially regarding magnetic shielding and the use of equivalent circuits, can be traced to his influence. The work was performed under the supervision of B. L. Dunfee, who provided a supportive, nurturing work environment for which the author has ever since been thankful. In addition, colleagues D. Flach and R. Kahler were partners during part of this work, and contributed their own diligence and insights. Of course, any errors or omissions in this document are solely the author's responsibility.

TRANSFORMER-LIKE DEVICES FOR HIGH-ACCURACY AC CURRENT MEASUREMENTS

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ABSTRACT

A theoretical and practical framework is presented to aid in the design, fabrication, and testing of transformer-like devices for use in high-accuracy ac current metering applications. Current transformers, two-stage current transformers, and current comparators are discussed, as well as related devices that use passive and active error correction techniques. Transformer theory is developed in terms of simple electromagnetic theory and practical equivalent circuits. Magnetic design equations are presented and the measurement of relevant magnetic properties is discussed. Sources of error and their mitigation are covered in detail, including errors caused by magnetizing currents, winding and core inhomogenieties (so-called magnetic errors), and circulating capacitive currents. Calibration methods and current transformer testing are also covered.

KEY WORDS: ac current measurement; current comparators; current transformers; current transformer testing; error sources; equivalent circuits; magnetic shielding; transformer design

1. INTRODUCTION

Instrument current transformers are used to scale ac currents to levels that are most appropriate for measurement. Today, most modern electronic instrumentation is voltage-based: Current is measured by first passing it through an impedance of known value, and the resulting voltage drop becomes the quantity that is actually measured (see fig. 1). Most often the impedance is a low inductance four-terminal resistor, although mutual inductors and even capacitors are occasionally used for ac measurements. To achieve the highest accuracy, the impedance value is generally selected to give an rms voltage level in the range of 0.1 V to 1 V. However at current levels greater than about 1 A, it becomes increasingly difficult to use resistors because of problems of power dissipation and residual inductance. For example, if the voltage drop is maintained at 1 V, then one watt of power dissipation is required for every ampere of measured current. Furthermore, the residual inductance associated with any resistor design causes phase errors (between input current and output voltage) that become unacceptably large at high currents (i.e., low resistance values) and high frequencies. Fortunately, pre-scaling the current to be measured can minimize these problems.

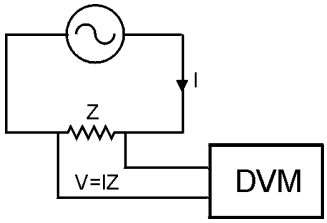


Figure 1.1. Current Measurement Using Voltage-Based Instrumentation

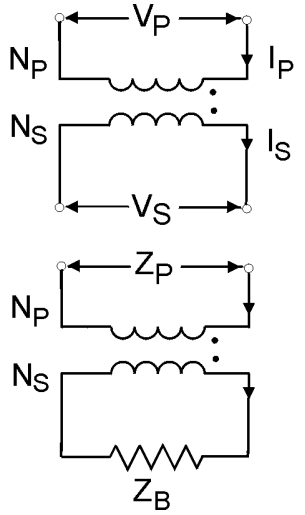
Current transformers are typically used for this purpose since they are capable of reasonably high ratio accuracies with relatively low power dissipation over a wide range of current ratios. The current flowing in a load (or *burden*, Z_B) connected to the secondary winding of a current transformer is nominally equal to the current in the primary or driven winding, times the inverse turns ratio. Consequently, under the conditions given above, a current transformer having an inverse turns ratio of N will reduce the power dissipation in the resistor by a factor of 1/N for a fixed voltage. Even higher accuracies are achievable using feedback amplifier techniques or transformers with two or more stages. For the special case in which the current in question is being compared with a standard, known current of the same frequency, then current comparators can be used.

This technical note presents a theoretical and practical framework to aid in the design, fabrication and testing of current transformers and current comparators for use in high accuracy metering applications.

1.1 The Ideal Transformer

Real transformers are designed to approximate the properties of an ideal transformer as represented in fig. 1.2. The ideal transformer is a device having two magnetically coupled but galvanically isolated windings designated primary and secondary, with N_P and N_S turns

respectively. The windings themselves of the ideal transformer have zero impedance, and are perfectly coupled, so that the ratios of the voltages (or currents) appearing at the terminals are exactly equal to the turns ratio (or inverse turns ratio) as indicated in the figure. When impedance, Z_B, is connected to the secondary winding, it follows then that the impedance as measured from the primary terminals is multiplied by the square of the turns ratio.



$$I_P N_P = I_S N_S$$

$$V_P N_S = V_S N_P$$

$$Z_P = Z_B \left(\frac{N_P}{N_S} \right)^2$$

Figure 1.2. The Ideal Transformer

1.2 Transformer Error and its Representation

The error, ε, of a current transformer is a complex quantity that expresses the degree to which the true primary-to-secondary current ratio differs from the inverse turns ratio:

$$\frac{I_P}{I_S'} = \frac{N_S}{N_P}(1-\varepsilon) = \frac{N_S}{N_P}(1-\alpha - j\beta), \tag{1.1}$$

where α and β are the in-phase and quadrature error components, respectively. The notation I'_S is used to indicate that the actual secondary current differs from the idea secondary current, I_S, that is shown in fig. 1.2.

In real transformers, the driving voltage that supports the secondary current is induced by the ac flux in the magnetic core linking the windings. However, to sustain the ac flux a *magnetizing current* must link the core; i.e., the net difference between the primary and secondary ampere-turns must not be zero. By definition though, the net ampere-turns of an ideal transformer is zero ($I_P N_P - I_S N_S = 0$) as stated above; consequently it is this residual magnetizing current that is responsible for the major error associated with current transformers. By using toroidal cores with high magnetic permeability, the magnetizing current can usually be kept small, but it cannot be reduced to zero. The equivalent circuit shown in fig. 1.3 can be used to accurately represent this error source, along with other characteristics of real transformers such as finite winding impedances. Here Z_P and Z_S represent the so-called leakage impedances that characterize the primary and secondary windings, and Z_m is the magnetizing impedance, a characteristic of the

core and winding that ultimately determines the size of the magnetizing current, I_m. Note that the magnetizing current is shunted away and current I'_S is the actual current delivered to the secondary burden. In practical designs, Z_m is large compared to Z_S and Z_B, so that I_m is small compared to I_S, and the resulting transformer error is small. These concepts will be developed more fully in subsequent chapters, and the quantities Z_m and I_m will be related to the underlying physics involved.

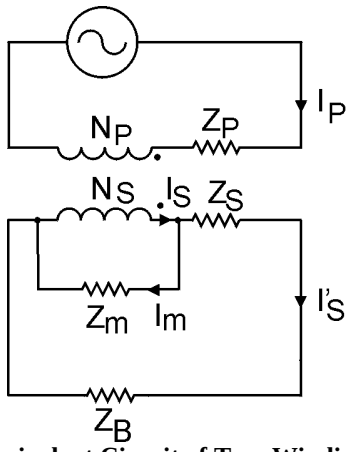


Figure 1.3. Equivalent Circuit of Two-Winding Transformer

For now, we can solve the circuit equations from fig. 1.3 to obtain the transformer error as defined in (1.1) above, in terms of the circuit parameters. Thus we have

$$I_S^{'} = I_S\left(\frac{1}{1+\dfrac{Z_S+Z_B}{Z_m}}\right) \approx I_S\left(1-\frac{Z_S+Z_B}{Z_m}\right) \qquad (\text{for } Z_m >> Z_S+Z_B), \tag{1.2}$$

and combining (1.2) with (1.1) we get the transformer error as

$$\varepsilon \approx -\frac{Z_S+Z_B}{Z_m}\ . \tag{1.3}$$

1.3 Other Error Sources

While the magnetizing current is the predominant source of error in a simple current transformer, it is not the only source. So-called magnetic errors arise when the windings link the core unequally (see chapter 7), and capacitive errors arise when capacitance between or across windings shunts part of the current away from the core (see chapter 8). For current comparators and multistage current transformers, these become the dominant sources of error. Subsequent chapters will explore these error sources in depth, and will present approaches for their mitigation. Note however that the type of equivalent circuit shown in fig. 1.3 cannot easily represent either of these error sources, and it will only be used to represent errors caused by magnetizing currents.

1.4 Notation

Fig. 1.4 shows the notation that will be used throughout this document to indicate the relative placement of windings and cores, and the polarity of windings designated by dots placed at one end of each winding. There are two governing rules:

1. Only windings shown above a given core link that core.
2. Polarity: For all currents entering corresponding terminals of windings linking a common core, the direction of flux induced in the core is the same. This causes all characteristic impedances to be positive.

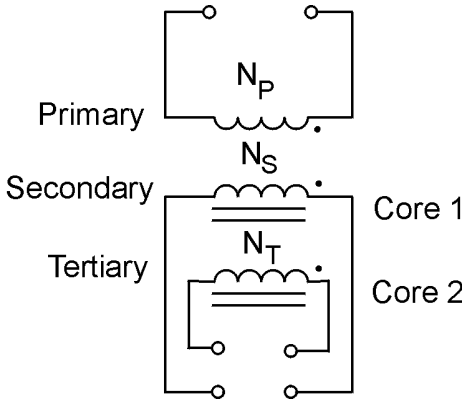


Figure 1.4. Notation of Cores and Windings

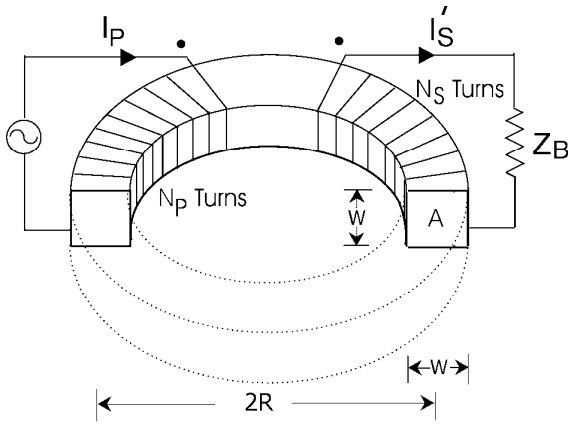
Therefore, in fig. 1.4, the primary, secondary and tertiary windings all link core 2, but only the primary and secondary windings link core 1.

2. PHYSICAL INTERPRETATION OF TRANSFORMER ERROR

Two laws of electromagnetic theory govern the fundamental principles of current transformers and current comparators: Faraday's Law of Induction and Ampere's Circuital Law. Together with the common formula for the inductance of a winding on a toroidal core of square cross section, Faraday's law can be used to calculate the error of a current transformer caused by magnetizing current. Fig. 2.1 represents a current transformer consisting of a magnetic core wound with a primary winding of N_P turns and a secondary winding of N_S turns connected to a burden. The supplied primary current enters the marked primary terminal, and in accordance with Le Chatelier's principle of least action, the resulting secondary current leaves the marked secondary terminal, thus minimizing the net flux in the core and the net ampere-turns linking the core. If we think of the net ampere-turns as a net current, i_m, flowing in the secondary winding, then we have

$$i_m = (i_P N_P - i_S' N_S) / N_S . \tag{2.1}$$

In a current transformer, i_m is called the magnetizing current.



$$L_S \approx \frac{k_m \mu_0 N_S^{\,2} A}{2\pi R} \quad (R >> w)$$

Figure 2.1. Current Transformer with Square-Cross-Section Toroidal Core (1/2 shown)

From Faraday's law, the voltage induced in the secondary winding is given by

$$v_S = \oint E_S \cdot dl = -N_S \frac{d\phi}{dt} = -L_S \frac{di_m}{dt}, \tag{2.2}$$

where v_S is the induced voltage (V),
E_S is the electric field intensity along path of the winding (V/m),
dl is an element of length of the path of the winding (m),
ϕ is the magnetic flux in the core (Wb), and
L_S is the inductance of winding (H).

The standard units of measurement are shown in parentheses, and the lower case notation used in (2.1) and (2.2) denotes time-domain variables. Transforming to the frequency domain, (2.2) becomes

$$V_S = -j\omega L_S I_m. \tag{2.3}$$

In a current transformer, the induced secondary winding voltage, V_S, supports the voltage drop across the burden impedance and the secondary winding leakage impedance, Z_S. (The leakage impedance of a winding consists of the winding resistance, and the component of inductive reactance whose flux does not link other windings). Therefore,

$$V_S = -I_S'(Z_B + Z_S). \tag{2.4}$$

Combining (2.3) and (2.4) gives the following expression for the magnetizing current:

$$I_m = \frac{I_S^{'}(Z_B + Z_S)}{j\omega L_S} \tag{2.5}$$

From (2.5), the transformer ratio is then given by

$$\frac{I_P}{I_S^{'}} = \frac{I_S(N_S / N_P)}{I_S^{'}} = \frac{(I_S^{'} + I_m)(N_S / N_P)}{I_S^{'}} = \frac{N_S}{N_P}\left(1 + \frac{Z_S + Z_B}{j\omega L_S}\right), \tag{2.6}$$

and comparing (2.6) with (1.1) we see that

$$\varepsilon = -\frac{Z_S + Z_B}{j\omega L_S}. \tag{2.7}$$

If we call impedance $j\omega L_S$ the magnetizing impedance, Z_m, then we arrive at the same error expression that is given by the equivalent circuit, i.e., (1.3). Furthermore, we see that the magnetizing impedance can be calculated from the simple formula for the inductance of a winding on a toroidal core as shown in fig. 2.1:

$$L_S \approx \frac{k_m \mu_0 N_S^2 A}{2\pi R} \quad (R >> w), \tag{2.8}$$

where L_S is the inductance of the winding (H),
k_m is the relative permeability of the core material (dimensionless),
μ_0 is the permeability of free space ($4\pi 10^{-7}$ Wb/A-m),
N_S is the number of turns of the secondary winding,
A is ithe effective cross sectional core area (m^2),
R is the mean radius of the core (m), and
w is the width and height of the core (m).

In practice, the magnetizing impedance is not a pure inductance but includes a resistive component that reflects the losses in the core material. At low frequencies, the losses are typically small and (2.7) gives a good approximation for the error.

From a practical standpoint, the formula given in (2.8) can be used for most common core configurations since it is reasonably accurate for any rectangular core cross section in which the ratio of height to width is at least 0.5.

Before moving on to the next section, note that the transformer error given in (2.7) is only dependent on the parameters of the secondary circuit.

3. THE CURRENT COMPARATOR

In many applications, it is useful to be able to accurately compare a current with a reference current when the two currents are of different magnitudes. Such needs arise, for example, in

many types of bridge circuits as well as in apparatus for testing current transformers. The simple current comparator shown in figs. 3.1a and 3.1b is often used in these applications. Historically, the current comparator was described as early as 1917 by Baker [27], and was later rediscovered and improved upon by Obradovic, Miljanic and Spiridonovic in 1957 [25] and by Kusters and Moore in 1961 [23]. Subsequent collaborations between Miljanic, Kusters and Moore led to many further developments and improvements (see [4] for a thorough description of this work).

The currents being compared are carried by two ratio windings as shown, with opposing polarities, and a third *detection* winding is used to indicate when ampere-turn balance is achieved, i.e, when the complex ratio of the two currents is exactly equal to the inverse turns ratio of the comparator. Under this condition, the flux in the core is zero, and therefore no voltage is induced in the detection winding. In some applications, one of the currents is adjusted by known amounts to bring about the null condition, while in other applications the number of turns in one or both windings is adjusted for the same purpose. Since there is no flux in the core at balance, there are no voltages induced in the windings and no magnetizing current is present; consequently, no power is transferred from primary to secondary circuit, as is the case with current transformers. Instead, the power dissipated in the secondary circuit of a simple current comparator is totally supplied by the source of the secondary current.

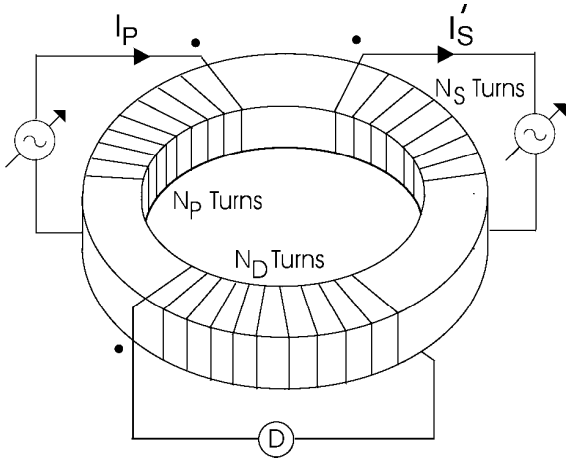


Figure 3.1a. Simple Current Comparator

These principles are embodied in the equivalent circuit shown in fig. 3.2. This circuit is similar to the current transformer equivalent circuit of fig. 1.3 with the addition of another ideal transformer to represent the placement and action of the detection winding. Since the detection winding is used to detect the presence of a magnetizing current, the upper winding of the second ideal transformer is connected across the magnetizing impedance, and the turns ratio of this transformer represents the ratio of the secondary winding to the detection winding. When the voltage at the detector is zero, the voltage across the magnetizing impedance, and consequently the magnetizing current, must also be zero. Under these conditions, the actual secondary current, I'_S, equals the ideal secondary current, I_S. As noted earlier however, magnetic and capacitive errors also contribute to the overall accuracy of a current comparator, and these error sources are considered in detail in subsequent chapters.

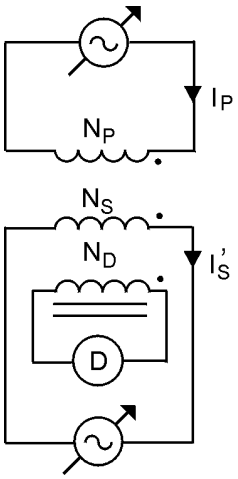


Figure 3.1b. Schematic Representation of Simple Current Comparator

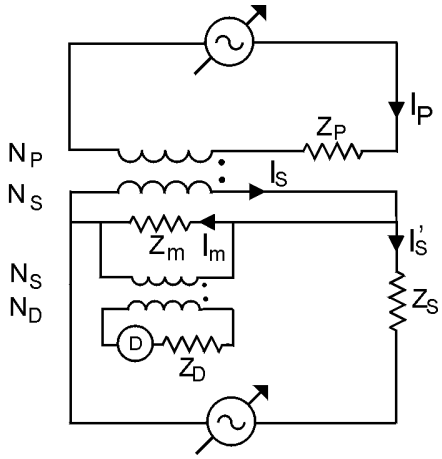


Figure 3.2. Equivalent Circuit of a Simple Current Comparator

Physically, the current comparator is often thought of as an embodiment of Ampere's Circuital Law: The line integral of the magnetic field intensity, *H*, around a closed path is equal to the sum of the currents that are enclosed by that path. Although the rationale is a bit tenuous, it proceeds as follows. If the path taken is that of the magnetic core, and the currents are the primary- and secondary-winding currents flowing in opposition through N_P and N_S turns, respectively, this gives

$$\oint H \cdot d\ell = \sum_S I = N_P I_P - N_S I_S , \tag{3.1}$$

where $d\ell$ is an element of length of the path (m) and
s indicates summation over any surface enclosed by the line integral.

In a current comparator, the line integral is estimated via a detection winding that densely and uniformly covers the core (unlike that illustrated in fig. 3.1a, where, for clarity, the detection winding is shown covering only a portion of the core).

If it is assumed that the flux density, $B = k_m \mu_0 H$, is constant over the core's cross section, then (3.1) can be written in terms of magnetic flux as

$$\frac{1}{k_m \mu_0 A} \oint \phi \cdot dl = \sum_S I \,, \tag{3.2}$$

where k_m is the relative permeability,
μ_0 is the permeability of free space,
A is the cross sectional area of core, and
ϕ Is the magnetic flux.

For regular toroidal cores and uniformly distributed windings, we can make the further simplifying assumption that the flux is constant over the path of the core, giving

$$\frac{2 \pi R \phi}{k_m \mu_0 A} = \sum_S I \,, \tag{3.3}$$

where R is the radius of the toroidal core.

Meanwhile, the detection winding voltage can be expressed in terms of the magnetic flux in the core from Faraday's law as

$$v_D = \oint E_D \cdot dl = -N_D \frac{d\phi}{dt} \,. \tag{3.4}$$

(Note that the line integral in (3.4) follows the path of the detection winding around and around the core cross-section N_D times. Although this path eventually traverses the core, it is not the same as the line integral of (3.1) which for simplicity is assumed to follow the core path itself. If the same path were used in both, a less restrictive argument could be made, however with the expense of greater complexity.)

For sinusoidal signals (3.4) becomes

$$V_D = -j\omega N_D \Phi \,, \tag{3.5}$$

and combining (3.5) with the frequency-domain counterpart of (3.3), we get

$$V_D = -j \frac{k_m \mu_0 A \omega N_D}{2\pi R} \sum_S I \,. \tag{3.6}$$

Therefore, the detection winding voltage is directly proportional to the net ampere-turns that link the core, i.e., that pass through the core window. The condition of ampere-turn balance that occurs in simple current comparators when the primary and secondary ampere-turns are equal and opposite, is indicated by a null voltage at the detection winding.

From the equivalent circuit of fig. 3.2, we can see that the open-circuit voltage at the detector is given by

$$V_D = I_m Z_m \frac{N_D}{N_S} = (I_S - I_S^{'}) Z_m \frac{N_D}{N_S} = \left(I_P \frac{N_P}{N_S} - I_S^{'} \right) \frac{Z_m N_D}{N_S} = (I_P N_P - I_S^{'} N_S) \frac{Z_m N_D}{N_S^2}. \qquad (3.7)$$

Substituting into (3.7) the formula for magnetizing impedance derived previously (see (2.8)) gives the same expression for detection winding voltage as shown in (3.6). Therefore the equivalent circuit is consistent with the physical interpretation given above. The quantity $(Z_m N_D)/N_S^2$ in (3.7) is called the *sensitivity* of the detection winding. Under the various assumptions made above, the sensitivity to ampere-turns in the primary winding is the same as the sensitivity to ampere-turns in the secondary winding, as (3.7) and (3.6) suggest; and in fact the accuracy of the current comparator depends on this equality. However, so-called magnetic errors can arise when the assumptions are not strictly valid, and the result is that the sensitivity is somewhat different for the primary and secondary windings. The subject of magnetic error and its mitigation is treated in chapter 7.

3.1 The Compensated Current Comparator

One drawback of the simple current comparator is that the leakage impedances of both ratio windings can be significant loads for the respective current sources. If the current comparator is being used to calibrate a current transformer for example, the source of secondary current is actually the secondary winding of the transformer under test, and the secondary leakage impedance of the current comparator adds a significant burden to the test transformer that will affect its error.

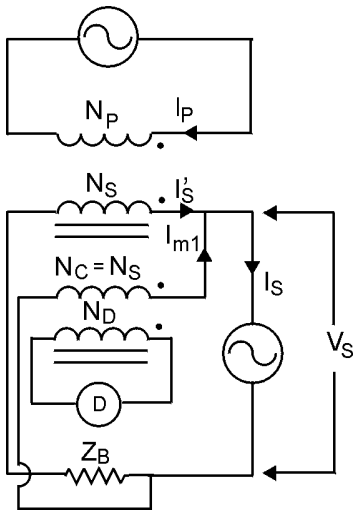


Figure 3.3 Compensated Current Comparator

The so-called compensated current comparator [11] shown in fig. 3.3 minimizes this problem for the secondary circuit. This circuit has an additional core that creates a transformer stage capable of transferring power across the core from the primary to secondary circuit. In operation, a compensation winding added to the detection core carries the magnetizing current, I_{m1}, of the transformer stage as shown, so that the voltage, V_S, of the secondary current source at detector balance is given by:

$$V_S = I_{m1} Z_C , \tag{3.8}$$

where Z_C is the leakage impedance of the compensation winding. This is more apparent from the equivalent circuit shown in fig. 3.4. When the secondary current source is adjusted to achieve a null on the detector, no current flows through the magnetizing impedance, Z_{m2}, of the detection core. Therefore, current I'_{m1} that flows through the leakage impedance, Z_C, of the compensation winding, exactly equals the magnetizing current I_{m1}, and the secondary current I'_S exactly equals the ideal secondary current, I_S.

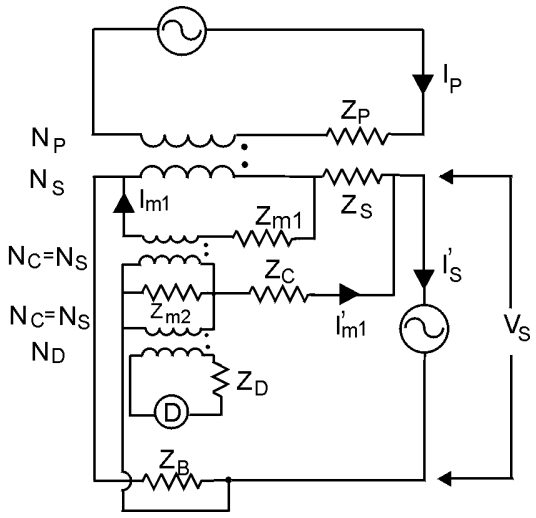


Figure 3.4 Compensated Current Comparator: Equivalent Circuit

At detector balance, the equivalent load seen by the secondary current source is:

$$Z_L = \frac{V_S}{I_S} = \frac{I_{m1} Z_C}{I_S} \approx \frac{(Z_S + Z_B) Z_C}{Z_{m1}} , \tag{3.9}$$

which is normally quite small as compared to a load of Z_S which would exist for a simple, uncompensated current comparator. Applications of the compensated current comparator will be discussed in chapters 6 and 9.

4. MAGNETIC DESIGN EQUATIONS AND THE MEASUREMENT OF MAGNETIC PROPERTIES

4.1 Hysteresis, Permeability and Core Loss

The so-called hysteresis loop of a magnetic core reveals several important characteristics that must be considered when selecting the cores to be used in transformers or current comparators. The magnetic field intensity, H, in a magnetic core is a memoryless linear function of the current linking the core. However, the magnetic flux density, B, is only linearly proportional to the current when the core is a non-magnetic material, i.e., when the permeability is that of free space, μ_0. Otherwise, depending on the type of magnetic material used, the magnetic flux density is a nonlinear and non-unique function of current (or magnetic field intensity).

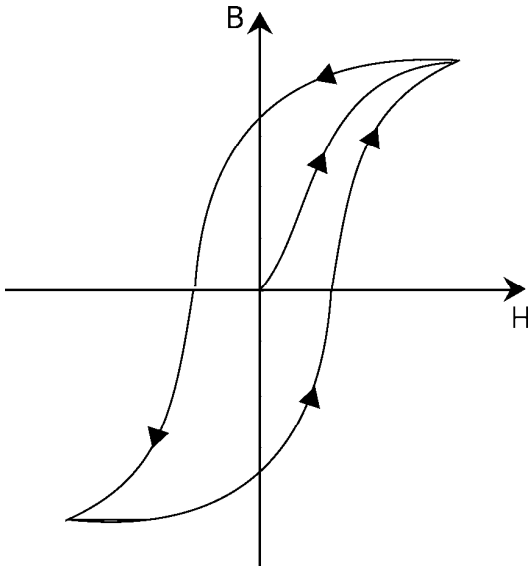


Figure 4.1 Hysteresis Loop

These relationships are illustrated with the B/H curve or hysteresis loop shown in fig. 4.1, which is typical of the magnetic cores used in most current transformers and current comparators. By definition, the slope of the curve, i.e., B/H, is the magnetic permeability, $k_m\mu_0$, where k_m is the relative permeability. As the current increases from zero, the permeability has an initial value that increases as the current gets larger, until a point at which it begins to decrease, ultimately reaching a value of μ_0 as the current becomes very large. If the current is then cycled back through zero to a large negative value, and so on for a periodic signal, the memory effect of the hysteresis loop is manifested.

Several important points are illustrated here. First, since the permeability is a nonlinear function of current, we can expect the resulting magnetizing current of a transformer (as described in (2.5)) to contain harmonic components even when the primary current is strictly a single tone sinusoid. However, because of the symmetry of the hysteresis loop, only odd harmonics will normally appear. (If the core has residual dc magnetization though, the loop will become asymmetric and even harmonics will also be generated.) Second, the relative size of the magnetizing current, and hence the error, varies depending on the flux density in the core (see section 4.2). Third, if the peak flux density becomes too large, the core "saturates," the permeability plummets and the error increases dramatically (see section 4.2). Fourth, the hysteretic property of the B/H curve suggests that energy is being used to magnetize the core, which results in core loss. In fact, for repetitive signals, e.g., sinusoids, the total energy per unit core volume per cycle is equal to the area enclosed by the loop. The resulting core loss is represented in an equivalent circuit as a parallel loss component of the magnetizing impedance. Finally, the initial state of magnetization affects the overall size and symmetry of the B/H curve (and the harmonic content as noted above) and demagnetization may be required to achieve the initial state of zero magnetization that is assumed in fig. 4.1 (see section 4.5).

4.2 Magnetic Flux Density and Saturation Flux Density

In order to estimate the size of magnetizing currents in transformer designs and hence the errors that result, it is necessary to know the magnetic flux density that can be expected in the cores. For toroidal cores, the magnetic flux density may be calculated in terms of the secondary current, secondary leakage impedance and burden, as follows. From (2.2), the frequency domain relationship between secondary winding voltage, V_S, flux, Φ, and flux density is given by

$$V_S = -N_S\, j\omega \Phi = -N_S\, j\omega\, B\, A, \tag{4.1}$$

where N_S is the number of turns in the secondary winding and
A is the effective cross sectional area of the core.

Rearranging (4.1) yields

$$B = j\frac{V_S}{2\pi f N_S A}, \tag{4.2}$$

and combining this with (2.4) gives the magnetic flux density as

$$B = -j\frac{I_S^{'}(Z_S + Z_B)}{2\pi f N_S A}. \tag{4.3}$$

With I_S expressed in amperes, the impedances in ohms, and A in squared meters, B is given in tesla or Wb/m^2. Note that 1T equals 10^4 gauss, with gauss being the unit more commonly used by manufacturers of magnetic cores.

If V_S is assumed to be the rms value of the secondary voltage and B_{sat} is the saturation flux density, then the largest secondary voltage that can be sustained, V_{Smax}, is obtained from (4.2) as

$$V_{S\max} = \frac{j2\pi f N_S A B_{sat}}{\sqrt{2}}. \tag{4.4}$$

4.3 Magnetizing Impedance and Magnetizing Impedance per Turn-Squared

As noted in chapter 2, the principal component of the magnetizing impedance, Z_m, associated with a winding on a core is the self-inductance of the winding. So again, for toroidal cores the magnetizing impedance is given by:

$$Z_m \approx j\omega L = j\frac{\omega k_m \mu_0 N^2 A}{2\pi R} = j\frac{f k_m \mu_0 N^2 A}{R}. \tag{4.5}$$

This expression ignores the contribution of core loss, which is typically rather small at low frequencies.

The impedance given in (4.5) corresponds to a particular number of turns, *N*, of the winding. For design purposes, it is usually more convenient to characterize the core itself by its magnetizing impedance per turn-squared, given by:

$$\frac{Z_m}{N^2} \approx j\frac{f k_m \mu_0 A}{R}. \tag{4.6}$$

While the expressions of (4.5) or (4.6) are critical to the selection of cores and the number of turns to use in a transformer design, they only provide approximate estimates of device performance. As noted above, they ignore contributions such as core loss, and the values for the parameters on which they depend are usually typical values taken from data sheets. To get a more accurate estimate of the performance one is likely to achieve once a core has been selected, it is certainly advisable to measure the magnetizing impedance per turn-squared directly. Such a measurement is simple to perform with the setup shown in fig. 4.2.

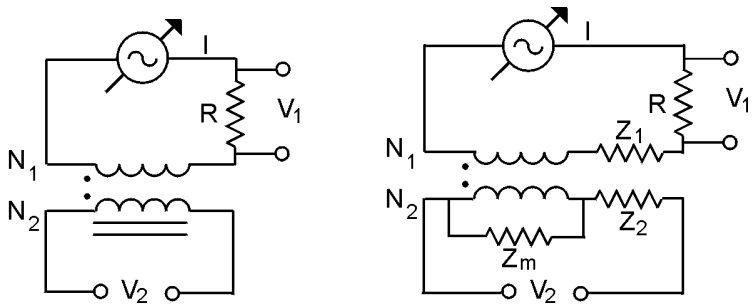


Figure 4.2 Test Setup to Measure Magnetizing Impedance per Turn-Squared (left), and its Equivalent Circuit (right)

With this setup, two windings are placed on the core under test. The first, with N_1 turns, carries the excitation current that is measured in terms of voltage V_1 across the series ac resistor. The second winding of N_2 turns, produces the induced voltage, V_2. The current is adjusted to give the desired magnetic flux density test condition, which is indicated per (4.2) by voltage, $V_S = V_2$, and then the two voltages are recorded. The magnetizing impedance per turn-squared is given as:

$$\frac{Z_m}{N_2^2} = \frac{1}{N_1 N_2} \times \frac{V_2 R}{V_1}. \tag{4.7}$$

By using two windings, this approach makes it possible to measure the impedance per turn-squared independent of the leakage impedance of either winding. The values for N_1 and N_2 are selected for convenience of measurement, but some care should be taken to distribute each uniformly around the core.

4.4 Detection Sensitivity for Current Comparators, and Tuned Detection

The function of a current comparator is to detect the condition of ampere-turn balance among the ratio windings. As discussed in chapter 3, ampere-turn balance is sensed by a detection winding

placed on the detection core. The main parameter of interest in selecting the detection core and number of detection winding turns is the detection sensitivity, i.e., the detection winding voltage produced per ampere-turn of unbalance. Referring to fig. 3.2, any ampere-turn unbalance gives rise to the magnetizing current, I_m, which flows through the magnetizing impedance, Z_m. Therefore, the detection voltage, V_D, is given by:

$$V_D = \frac{N_D I_m Z_m}{N_S}. \tag{4.8}$$

The detection sensitivity, $Z_{D\text{-}S}$, is then:

$$Z_{D-S} = \frac{V_D}{I_m N_S} = \frac{N_D Z_m}{N_S^2}, \tag{4.9}$$

since $I_m N_S$ is the ampere-turn unbalance. For toroidal cores, we combine (4.9) with (4.6) to yield:

$$Z_{D-S} \approx j \frac{N_D f k_m \mu_0 A}{R}. \tag{4.10}$$

If 4.10 is expressed in terms of winding density, i.e., the number of turns in the detection winding per unit length of core circumference, D_T, then we have [4]:

$$Z_{D-S} \approx j\omega D_T k_m \mu_0 A, \tag{4.11}$$

where $D_T = N_D/(2\pi R)$. Expressed in this way, we see that the sensitivity does not depend on the diameter of the core, but only on the winding density and the cross sectional area of the core.

As previously noted, the magnetizing impedance is primarily inductive at lower frequencies, and so the detection sensitivity is also primarily inductive as the imaginary term in (4.10) implies. This makes it possible to increase the detection sensitivity by tuning the circuit with a capacitor across the detection winding as shown in fig. 4.3.

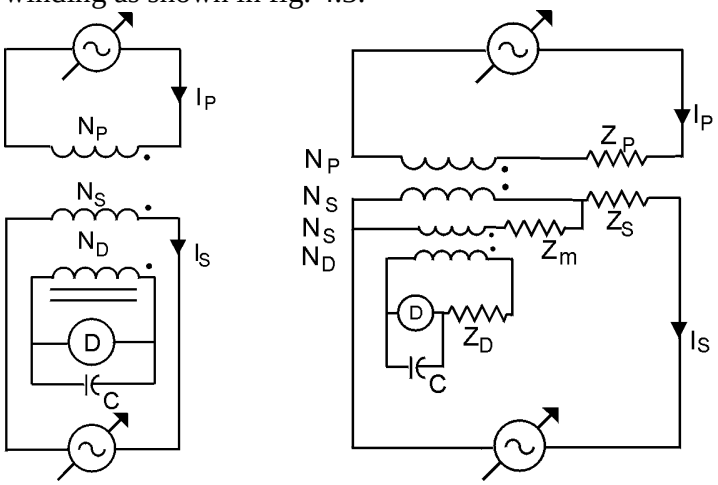


Figure 4.3 Tuned Detection Circuit (left), and Equivalent Circuit (right)

The sensitivity is greatest when the capacitance is given by

$$C = \frac{L}{(\omega L)^2 + Z_D^2}, \tag{12}$$

where L is the inductance of the detection winding, $(k_m \mu_0 N_D^2 A)/(2\pi R)$, and the leakage impedance, Z_D, is assumed to be resistive [4].

4.5 Core Demagnetization

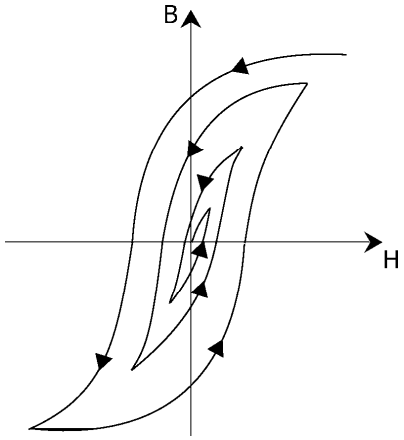


Figure 4.4 Core Demagnetization

At the beginning of this chapter, it was noted that dc magnetization of a core affects the size and shape of the B/H curve, which in turn can affect the overall error performance of the device. To remove residual magnetization, it is necessary to raise the ac winding voltage to the point that the core saturates, and then reduce the voltage slowly to zero. This process is indicated in fig. 4.4. The voltage must not be switched off before it reaches zero, since the resulting transient may remagnetize the core.

5. WINDING TECHNIQUES AND THE ESTIMATION OF LEAKAGE IMPEDANCES

There are three basic choices to be made in designing the windings of a current transformer or current comparator: the number of turns, the wire size, and the winding layout. These choices directly affect the winding's magnetizing impedance, its current carrying capacity and leakage impedance, as well as the resulting magnetic and capacitive errors.

5.1 Number of Turns and Wire Size

The first consideration when selecting the number of turns and wire size to use must be the current carrying capacity required of the winding. Generally, for windings that carry little or no current such as detection, compensation or tertiary windings, self-heating is of little concern; however for the main ratio windings it becomes paramount. While the amount of power generated in a winding is of course the square of the winding current times the winding resistance, the temperature buildup is more difficult to calculate since it depends on how readily heat can be removed from the winding. However, for most practical cases a rule-of-thumb of

240 amperes per cm^2 of wire cross-section should be acceptable. This applies to devices with multiple windings in a reasonably ventilated space maintained at room temperature. Table 5.1 presents the approximate current carrying capacity of several wire sizes based on this rule. Of course, a heavier wire (i.e, smaller wire gage) than shown in Table 5.1 can be used, and may be appropriate to achieve the desired resistance for the winding.

Table 5.1
Approximate Current Carrying Capacity of Selected Wire Sizes

Wire Size (AWG)	Current Carrying Capacity (A)
#12	7.9
#15	4.0
#18	2.0
#20	1.2
#24	0.49

The number of turns to use for a winding depends on the type of winding. For a detection winding, the required sensitivity dictates the number of turns needed, as discussed in section 4.4. For tertiary or compensation windings, the number of turns is usually selected to match that of the secondary winding, and the wire size for these is usually selected to give the lowest resistance that can be achieved in a single-layer winding, although in some cases multi-layer windings may be required. The effects of the resistances of these windings on the device error are given in chapter 6. For the secondary windings of transformer stages, the required magnetizing impedance sets the lower bound for the number of turns (see sections 1.2, 3.1, 4.3 and chapter 6), but other considerations such as saturation flux density can dictate a larger number (see section 4.2). Of course, the number of turns selected for the secondary winding must give an integer number of turns for the primary winding, to achieve the desired turns ratio.

5.2 Winding Layout

As seen in previous chapters, the error of a transformer stage that results from magnetizing current is only dependent on the number of turns of the secondary winding. Therefore, it is usually preferable to have a fixed number of turns for the secondary winding since this practice keeps the error constant over all available ratios. Multiple ratios are then accommodated via the primary winding. In chapter 7, we will see that winding uniformity is important in minimizing so-called magnetic errors, so it is also important to distribute the turns of a winding uniformly around the core, preferably in one layer. This also makes it easier to calculate errors due to circulating capacitive currents as discussed in chapter 8. The preference for single-layer windings has two reasons: interwinding capacitance is greatly increased in multi-layer windings, leading to larger capacitive errors; and the leakage inductance of a winding increases substantially with multiple layers since flux between the layers does not link all of the turns. The leakage inductance is also greater in the outer winding, since the flux in the space between windings does not link the inner one at all. Therefore, it is common practice to make the secondary the inner winding, thus minimizing its leakage impedance and the resulting error that it causes in conjunction with the magnetizing impedance. The reactance of a single layer secondary winding is then usually negligible at lower frequencies. For multi-layer windings though, the reactance can be the dominant source of leakage impedance, especially at higher

frequencies. Also, the leakage reactance of the primary (outer) winding is relatively larger. Note that it is experimentally difficult to measure the individual leakage impedances of each winding, except for their dc resistive components. Therefore they must be estimated analytically whenever it is likely that the reactances will be significant. Of course, the resistive components can be readily estimated from the resistance per unit length of the wire (available from wire tables) and the length of wire in the winding. Formulae for calculating leakage reactances can be found in [1,19].

For multi-ratio devices, a series-parallel arrangement of the primary winding as illustrated in fig. 5.1 can be used to advantage. The winding is divided into P individual sections of Q turns each, with the sections wound side-by-side such that the core circumference is filled by the P sections. To achieve the lowest available ratio, N_S/N_P, all P sections are connected in series. Higher ratios are available by connecting the sections in series-parallel combinations as shown in the figure. For the example in the figure, P is 8 and Q is 30. If the secondary winding has 240 turns, then the arrangement in the figure can give four ratios: 1/1 (240/240), 2/1 (240/120), 4/1 (240/60), and 8/1 (240/30). Note that for a fixed secondary current level, the primary current increases in proportion to the turns ratio, but the current flowing in each of the P sections is constant regardless of ratio and the power dissipation in the winding is also constant. Furthermore, the ampere-turn current distribution in the winding does not change from ratio to ratio, so that any magnetic error (see chapter 7) that exists should be independent of ratio as well. This method minimizes the total number of turns required in the primary winding, and requires wire of only one size. In addition, the primary leakage impedance simply scales inversely with the square of the ratio. The drawbacks of the series-parallel approach are that the available ratios are limited, and procedures used to make the necessary connections are more complicated than is otherwise required.

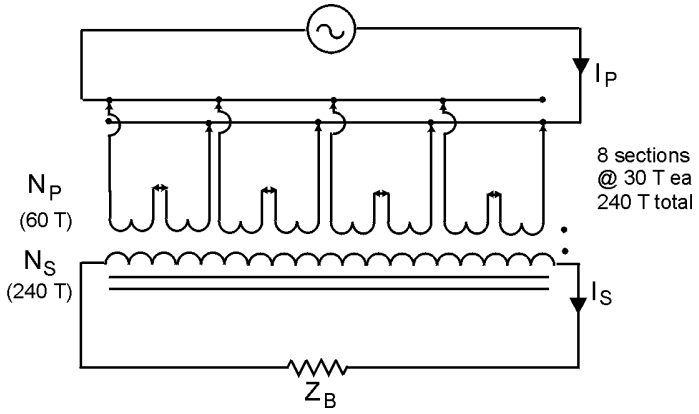


Figure 5.1 Series-Parallel Arrangement for Primary Winding (one example)

5.3 The "Single-Turn" Problem

As an N-turn winding progresses around the circumference of the core, it not only links the flux in the core N times, but it also links once any flux in the window of the core. Flux in this region is extraneous and will induce an additional voltage in the winding that is unwanted. Such flux often represents spurious mutual coupling to external circuit elements, e.g., currents in

conductors leading to or from the device in question, and as such will induce a voltage that is coherent with the flux in the core. For ratio windings, an induced voltage is usually inconsequential if it is small with respect to the normal voltage appearing across the burden (for secondary windings) or at the source (for primary windings). However, for the detection winding of a current comparator, the voltage represents a direct error, and for tertiary and compensation windings that operate at low voltages, it can create problems as well. The solution to the problem is to add a single return loop around the window that cancels the single turn of the winding, as illustrated in fig. 5.2.

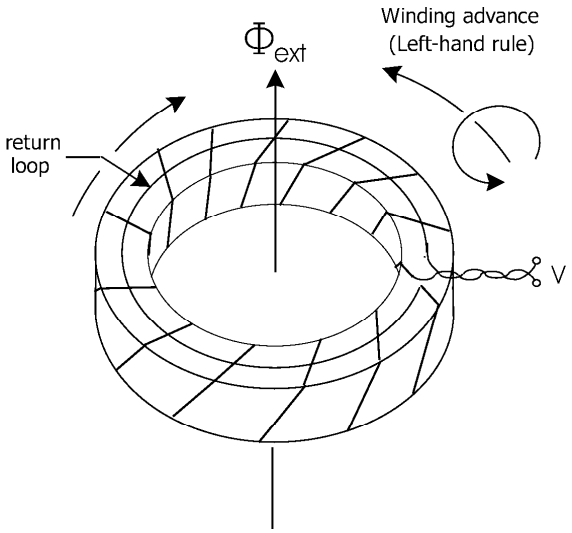


Figure 5.2 Solution for "Single-Turn" Problem

5.4 Turns Counting

Somewhat surprisingly, it isn't necessarily easy to make an error-free count of the number of turns that are being manually applied to a core. Ten turns are easy to count, but 100 turns requires some care, and 1000 turns is even more difficult. After the turns are applied, it is important to verify the count or else the device may be useless. The setup shown in fig. 5.3 is useful for this purpose.

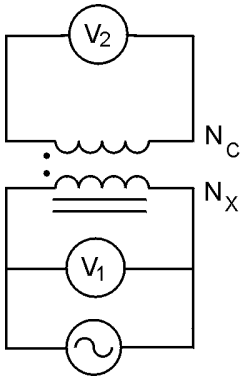


Figure 5.3 Turns Counting Circuit

In the figure, N_X represents the number of turns in the winding to be counted and N_C represents the number of turns, presumed known, of another winding placed on the same core. The winding under test is excited by a source, and the voltage across each winding is accurately measured. For the results to be accurate, N_C should be readily countable, but no smaller than 10; the test frequency should be chosen such that

$$Z_{mx} \geq 10 N_X Z_X , \tag{5.1}$$

where Z_{mx} is the magnetizing impedance of the winding under test at that frequency
Z_x is the leakage impedance of the winding under test,

and V_1 should be set high enough that V_2 is readily measurable with uncertainty less than $1/(10N_X)$. The number of turns in the test winding is then given by:

$$N_X = \text{round}\left[N_C \frac{V_1}{V_2} \right] , \tag{5.2}$$

where round[*] represents the nearest integer value of *. Clearly, as N_X approaches 1000 or more, the demands on the voltmeter's accuracy become critical. If a voltmeter with sufficient accuracy is not available, then it becomes necessary to create a bridge circuit in which the voltage ratio is compared with the programmable voltage ratio of an accurate, inductive voltage divider.

6. PASSIVE AND ACTIVE CORRECTION TECHNIQUES

As we saw in earlier chapters, the ratio accuracy of a simple two-winding current transformer is limited by the inherent magnetizing impedance of the secondary winding. The result is that a small portion of the secondary current is shunted away from the burden. A number of approaches have been proposed to minimize this error, and these are generally based on adding "corrective" cores and windings, or on the use of feedback amplifiers, or more often, on combinations of both approaches.

6.1 Passive Two-Stage Current Transformers

The addition of a second core and winding as illustrated in fig. 6.1 creates a so-called two-stage transformer [10, 26]. As the figure illustrates, the primary and secondary windings link both cores, but the tertiary winding only links core 2. The second stage consisting of core 2 and the tertiary winding, senses the ampere-turn difference of the first stage, i.e., the magnetizing current, and under the proper conditions produces a tertiary current that is very nearly equal to it. Therefore, the sum of the secondary and tertiary winding currents is very nearly equal to the ideal secondary current. For the second stage to produce an accurate correction however, the two stages must have separate burdens, or the common burden must be very small. The equivalent circuit of fig. 6.2 illustrates the case in which there are two separate burdens, designated Z_{B1} and Z_{B2}. Note that the equivalent circuit is simply the equivalent circuit of a simple current

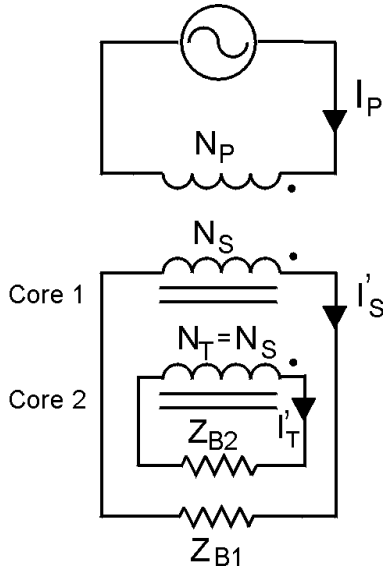


Figure 6.1 Two-Stage Current Transformer with Separate Burdens

transformer (stage 2) embedded in the equivalent circuit of another simple current transformer (stage 1), and the primary current of stage 2 is the magnetizing current of stage 1. A solution of the network equations for fig. 6.2 gives the following expression for the transformer ratio, defined as the ratio of the primary current to the sum of the actual secondary and tertiary currents:

$$\frac{I_P}{I_S^{'} + I_T^{'}} \approx \frac{N_S}{N_P}\left(1 + \varepsilon_1 \cdot \varepsilon_2\right), \tag{6.1}$$

where

$$\varepsilon_1 \approx -\frac{Z_S + Z_{B1}}{Z_{m1}} \quad \text{and} \quad \varepsilon_2 \approx -\frac{Z_T + Z_{B2}}{Z_{m2}} \quad \text{and} \, (Z_S + Z_{B1}) << Z_{m1}\,, (Z_T + Z_{B2}) << Z_{m2}\,. \tag{6.2}$$

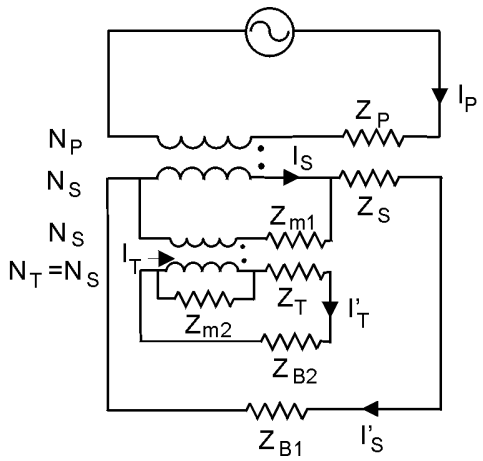


Figure 6.2 Two-Stage Transformer with Separate Burdens: Equivalent Circuit

Therefore, the ratio error as defined in section 1.2 is approximately equal to minus the product of the ratio errors of the individual stages. Brooks and Holtz first described the two-stage current transformer [26] in 1922. In their application, two separate windings of a wattmeter constituted

the two burdens, and the wattmeter responded to the sum of the two currents, thus providing a more accurate reading than was attainable with a conventional wattmeter and single-stage transformer.

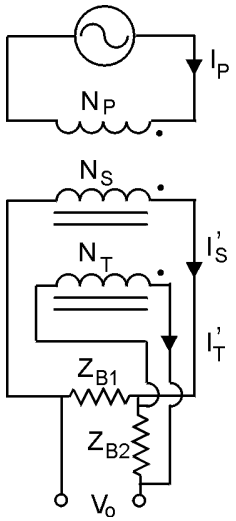


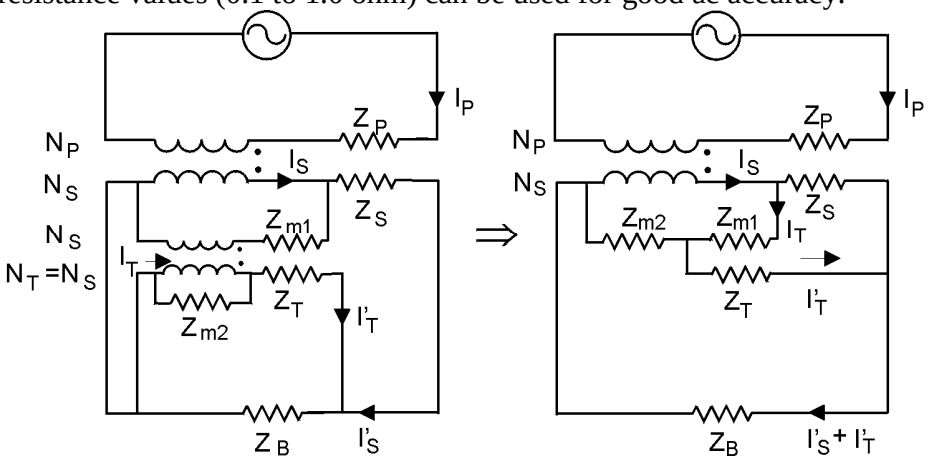
Figure 6.3 Two-Stage Transformer-Scaled Resistor

Fig. 6.3 illustrates another application of the two-stage transformer with separate burdens that has been used successfully by the author and others. For the case in which Z_{B2} is approximately equal to Z_{B1}, this is a simple but very accurate way to produce a lower-valued trans-resistance from a larger-valued 4-terminal resistor. Here, the output voltage is given by:

$$V_O \approx \frac{N_P}{N_S} I_P Z_{B1}\left(1+\varepsilon_1 \cdot \varepsilon_2 - \varepsilon_1 \mu\right), \tag{6.3}$$

where $Z_{B2} = Z_{B1}\left(1+\mu\right)$ and ε_1 and ε_2 are as defined above.

Although simple, this circuit can be quite accurate and exhibit wide bandwidth; furthermore, reasonable resistance values (0.1 to 1.0 ohm) can be used for good ac accuracy.



Figures 6.4a and 6.4b Two-Stage Transformer with Single Burden: Equivalent Circuits

Also, the power dissipated in the output resistor is only *Np/Ns* times the power dissipated in an un-scaled resistor of the same value. The accuracy of a two-stage transformer degrades usually

when a single burden is shared by both stages. The corresponding equivalent circuit is shown in figs. 6.4a and in a reduced form in 6.4b.

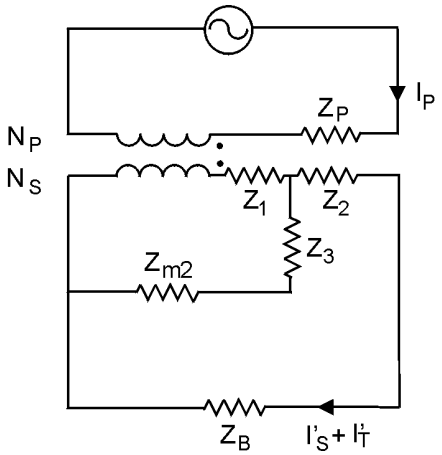


Figure 6.4c Two-Stage Transformer with Single Burden: Final Equivalent Circuit

Finally, following a $\nabla \rightarrow$ Y transformation, the equivalent circuit in fig. 6.4b yields that shown in fig. 6.4c,

$$\text{where} \quad Z_1 = \frac{Z_{m1} Z_S}{Z_{m1} + Z_S + Z_T}, \quad Z_2 = \frac{Z_S Z_T}{Z_{m1} + Z_S + Z_T}, \text{ and} \quad Z_3 = \frac{Z_{m1} Z_T}{Z_{m1} + Z_S + Z_T}.$$

With the usual assumption that the burden and leakage impedances are small with respect to the magnetizing impedances, the circuit of fig. 6.4c yields the following transformer ratio:

$$\frac{I_P}{I_S^{'} + I_T^{'}} \approx \frac{N_S}{N_P}\left(1 + \frac{Z_2 + Z_B}{Z_{m2}}\right) \approx \frac{N_S}{N_P}\left(1 + \frac{Z_S Z_T}{Z_{m1} Z_{m2}} + \frac{Z_B}{Z_{m2}}\right) \approx \frac{N_S}{N_P}\left(1 + \frac{Z_B}{Z_{m2}}\right). \tag{6.4}$$

Note that the effect of the second stage in this case is to essentially eliminate the contribution of the secondary winding leakage impedance to the error, while leaving the contribution due to the burden untouched. Therefore, unless the burden impedance is very small, the two-stage transformer with common burden is not in itself a very useful circuit.

6.2 Active Two-Stage Transformers

The use of feedback amplifiers can minimize the previously discussed errors in two-stage transformers caused by the burden impedance. A simple example is shown in fig. 6.5. Here, the effective burden as seen by the transformer is reduced by the amplifier gain, G, and the output voltage is given by:

$$V_O \approx \left(I_S^{'} + I_T^{'}\right) Z_B \left(1 - \frac{1}{G}\right) \approx I_S Z_B \left(1 - \frac{1}{G} - \frac{Z_B}{G Z_{m2}}\right). \tag{6.5}$$

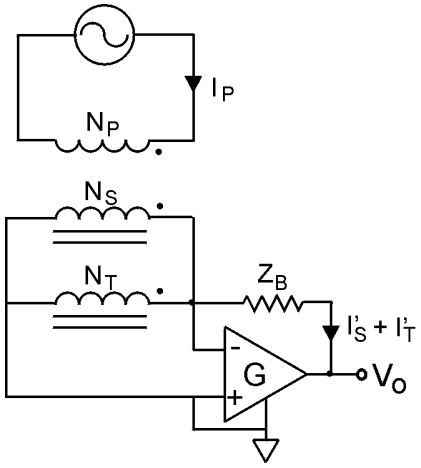


Figure 6.5 Two-Stage Transformer with Feedback Amplifier

For high-accuracy applications, this circuit requires that the amplifier gain be quite high at the frequencies of interest. Furthermore, the amplifier must be capable of handling the full secondary current as well as the full power dissipated in the burden. These requirements are not often easy to meet in practice.

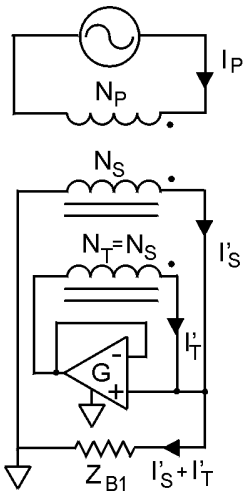


Figure 6.6 Amplifier-Aided Two-Stage Transformer

The amplifier-aided two-stage transformer circuit shown in fig. 6.6 minimizes all of these problems [10]. In this case, the first stage supplies the main current and power to the burden, while the amplifier is used to reduce the burden as seen by the second stage, and to sum the tertiary current with the secondary current in the burden. The value of the current delivered to the burden is given (with the usual assumptions) by:

$$I_S^{'} + I_T^{'} \approx I_S\left[1-\varepsilon_1\varepsilon_2\right] = I_S\left[1-\frac{Z_S+Z_{B1}}{Z_{m1}}\times\frac{Z_T+Z_{B2}}{Z_{m2}}\right], \tag{6.6}$$

where the second stage burden, Z_{B2}, is:

$$Z_{B2} \approx \frac{Z_{B1}}{\varepsilon_1 G} \approx \frac{Z_{B1}Z_{m1}}{(Z_S+Z_{B1})G}. \tag{6.7}$$

The resulting transformer ratio is then:

$$\frac{I_P}{I_S^{'} + I_T^{'}} \approx \frac{N_S}{N_P}\left[1 + \frac{(Z_S + Z_{B1})Z_T}{Z_{m1}Z_{m2}} + \frac{Z_{B1}}{G\,Z_{m2}}\right]. \tag{6.8}$$

Both of the error terms are of second order, so there is no first-order dependence on the amplifier gain, unlike the example of fig. 6.5. In addition, the last error term should be essentially constant over a wide range of frequencies since the magnetizing impedance, Z_{m2}, increases as the amplifier gain is rolling off with frequency. Because the feedback of this design is directly coupled rather than magnetically coupled as with some other designs, it is inherently quite stable at large open loop gains. A potential drawback however is that any dc offset in the amplifier will produce an unwanted dc current in the burden.

6.3 Active Current-Comparator Correction Circuits

Other correction circuits are based on the current comparator. For example, the self-balancing current comparator developed by O. Petersons [16] combines a feedback amplifier with the compensated current comparator of section 3.1 to produce a nearly ideal transformer ratio. The circuit is shown in fig. 6.7 and its equivalent circuit is given in fig. 6.8. Here, the amplifier produces a compensation winding current, I_C, that balances the current comparator. The current I_C is summed with the secondary current, I'_S, in the burden, establishing a nearly ideal current ratio. A solution of the network equations derived from fig. 6.8 gives the following transformer ratio (see [16]):

$$\frac{I_P}{I_S^{'} + I_C} \approx \frac{N_S}{N_P}\left(1 + \frac{Z_B}{Z_{m2}(G+1)}\right). \tag{6.9}$$

Note that in designs where the first error component of (6.8) is negligibly small, (6.8) becomes essentially the same as (6.9). The magnetically coupled feedback of this design requires care in stabilizing the amplifier, and a wideband operation is difficult to achieve.

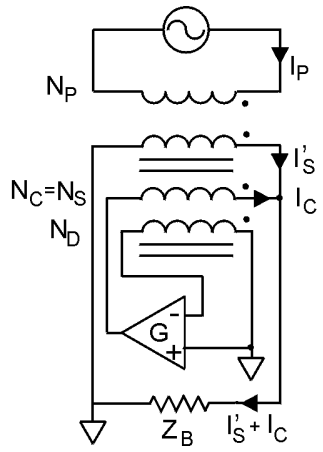


Figure 6.7 Self-Balancing Current Comparator

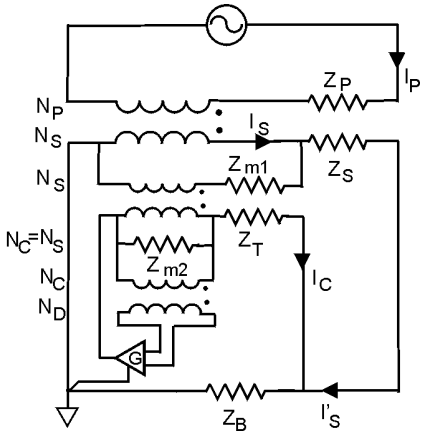


Figure 6.8 Self-Balancing Current Comparator: Equivalent Circuit

The next example, the Miljanic-So-Moore circuit [3], looks at first like the self-balancing current comparator; however, the feedback is via an excitation winding on the core of the first - or transformer – stage as seen in fig. 6.9. With sufficient gain, this winding provides just the right magnetizing current to the first stage to cause a nearly perfect secondary current to be developed. The feedback current is returned with the opposite polarity through the detection winding. Since the detection winding has the same number of turns as the excitation winding, the excitation current produces no flux in the detection core, and the only source of flux in that core is any imbalance in the primary and secondary ampere-turns. The equivalent circuit of fig. 6.10 is rather complicated, but serves to illustrate the operation of the circuit. For sufficient high amplifier gain, the only remaining error in this circuit is caused by the flow of the excitation current through the leakage impedance of the detection winding. The resulting voltage drop must be offset by a slight error in I'_S that flows through Z_{m2}, the magnetizing impedance of the detection winding. This error is given by:

$$\varepsilon = -\frac{Z_D\left(Z_S + Z_B\right)}{Z_{m1}Z_{m2}}. \tag{6.10}$$

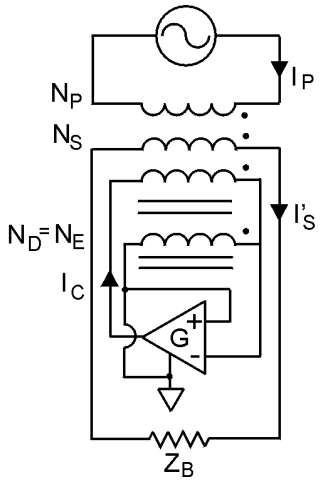


Figure 6.9 Miljanic-So-Moore Circuit

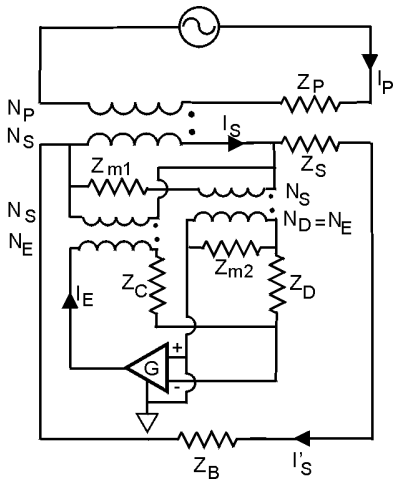


Figure 6.10 Miljanic-So-Moore Equivalent Circuit

As (6.10) indicates, the error is inversely proportional to the magnetizing impedance of the detection winding and directly proportional to the detection winding leakage impedance. Since the former is proportional to N_D^2 and the later to N_D, it is reasonable to make the number of turns of the detection winding, and hence the excitation winding also, as high as practicable. This circuit has the advantage that no dc current is introduced into the burden.

6.4 Construction of Two-Stage Transformers and Compensated Current Comparators

A typical physical arrangement of the cores and windings for two-stage transformers as well as compensated current comparators is illustrated in fig. 6.11.

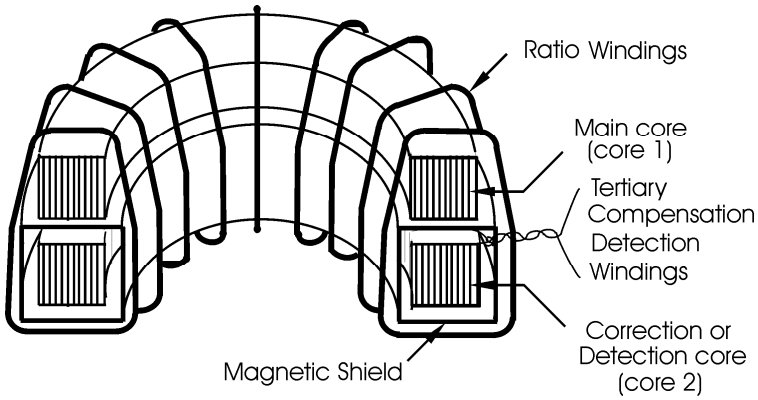


Figure 6.11 Construction of Two-Stage Transformers and Compensated Current Comparators

Note that core 2 is shown enclosed in a magnetic shield. The purpose of this is discussed in detail in the following chapter. Although this general method of construction is the most widely used today, the early papers of Miljanic, Kusters and Moore [4, 17, 18, 20] propose another method which combines the function of core 1 with that of the magnetic shield. Most today agree that the construction shown in the fig. 6.11 leads to more effective magnetic shielding.

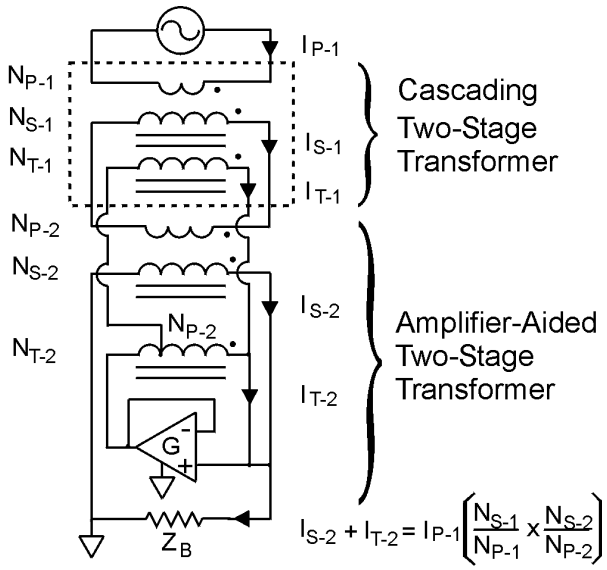


Figure 6.12 Cascading Two-Stage and Amplifier-Aided Two-Stage Transformers

6.5 Ratio Cascading

In some cases where large ratios are needed, it is preferable to achieve the desired ratio by cascading two (or more) devices as illustrated in fig. 6.12. The benefit of this approach is that fewer turns are required for the windings of each device, resulting in smaller physical size and lower capacitive errors. In the example shown, a simple two-stage transformer with a ratio of N_{S1}/N_{P1} is cascaded into an amplifier-aided two-stage transformer having a ratio of N_{S2}/N_{P2}, and the resulting composite ratio is the product of the two: $(N_{S1}N_{S2})/(N_{P1}N_{P2})$. Note that the tertiary winding of the upper transformer cascades into a tapped section of N_{P2} turns of the tertiary winding of the lower transformer. This assures that the equivalent burden on the second stage of the upper transformer is appropriately small, and that the correction current of that stage is weighted appropriately in the lower transformer. Similar cascading approaches can be used when the lower device is a current comparator, either simple or compensated.

7. MAGNETIC ERROR: ITS MEASUREMENT AND MITIGATION

In previous chapters, it was assumed that the primary and secondary windings couple equally to the tertiary winding of a two-stage transformer, or to the detection winding of a current comparator. In fact, this is never quite true: the coupling is dependent on the physical distribution of windings, and on the homogeneity of the magnetic properties of the core. For devices in which care has been taken to make the windings uniform, and high quality cores are used, the magnetic error can usually be held to a level of about 10^{-5}. To achieve higher accuracies, some type of magnetic error mitigation must be employed. As a result of magnetic error, the sensitivity of a detection winding is somewhat different to ampere-turns in the primary winding as it is to ampere-turns in the secondary winding, as illustrated in fig. 7.1. Therefore, under the simple conditions shown in fig. 7.2, the detector voltage will not be zero, i.e.,

$$V_D = I_P N_P Z^P_{D-S} - I_S N_S Z^S_{D-S} = IN_P\left(Z^P_{D-S} - Z^S_{D-S}\right) \neq 0\,. \qquad (7.1)$$

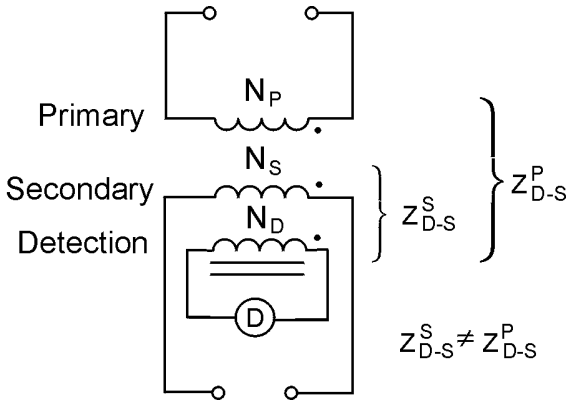


Figure 7.1 Unequal Sensitivities Due to Magnetic Error

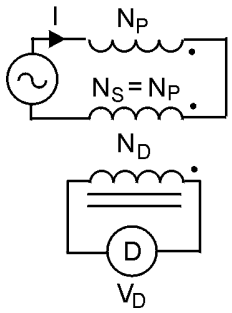


Figure 7.2 Manifestation of Magnetic Error

7.1 Source of Magnetic Error

The cause of magnetic error is illustrated in fig. 7.3, which shows a section of a magnetic core with detection winding, and another concentrated winding represented by a single turn.

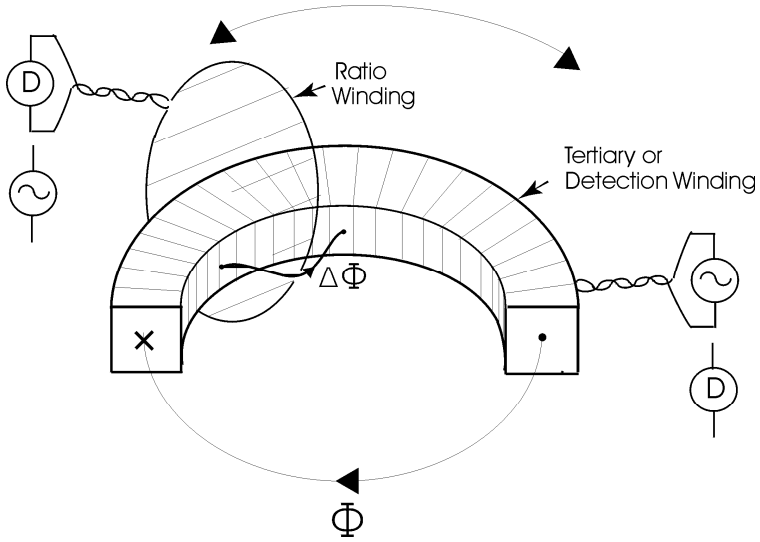


Figure 7.3 Source of Magnetic Error

Although a detection winding is used in this example, the same principles hold for the tertiary winding of a two-stage transformer, or for that matter, any third winding that is intended to be linked equally with the main (primary and secondary) ratio windings.

In a current comparator, the detection winding would normally be connected to a detector, and the single-turn winding would represent a section of either of the ratio windings through which a current would pass. To understand magnetic error though, it is conceptually easier to imagine the reciprocal network in which the detectors and sources are interchanged as indicated in fig. 7.3. (Although reciprocity does not strictly hold for magnetic devices based on nonlinear core materials, it is a reasonable approximation for our purposes here). Imagine then that a sinusoidal current is passed through the detection winding, causing magnetic flux in the core as shown. If the core and detection winding are reasonably uniform along the path of the core, nearly all of the flux is contained within the core; however, because of small non-uniformities, small amounts of flux may leave and reenter the core as illustrated by $\Delta\Phi$. When the loop is positioned as shown, it does not link this leakage flux; but when the loop is rotated to another position on the core, all of the flux is linked. Thus from Faraday's law the difference in induced voltage between the two positions is:

$$\Delta V_D = \oint E \cdot dl = -\frac{d}{dt}\int_S B \cdot da = -\frac{d}{dt}(\Delta\Phi). \qquad (7.2)$$

Invoking the reciprocity theorem, if the current is instead passed through the loop and the loop is moved around the core, then the same voltage change, ΔV_D, as given in (7.2) will appear across the detection winding. This suggests that two windings carrying the same but opposing current will not necessarily produced the hoped-for null at the detection winding, indicating the presence of magnetic error.

7.2 Test Method for Magnetic Error

The arguments just presented suggest a simple and quite effect test method for magnetic error, as illustrated in fig. 7.4.

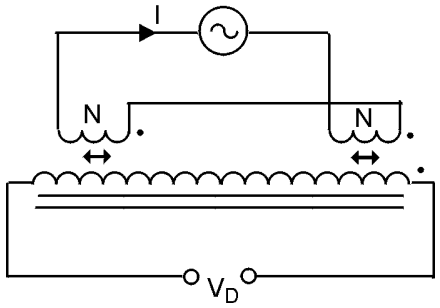


Figure 7.4 Test Method for Assessing Magnetic Error

It is implemented as follows: After the detection (or tertiary) winding is in place (with or without a magnetic shield as discussed below), two concentrated bundles of wire, each with the same number of turns, are loosely wound on the core, so that they can be moved along the core independent of each other. They are then connected in series opposition and energized by a current source. The current is set so that the ampere-turns of each winding (*I N* in the figure) is the same as will exist in the ratio windings of the completed transformer or current comparator.

As the detection winding voltage is monitored, the two bundles are moved independently to different positions around the core to find the maximum voltage, V_D, that occurs. The magnetic error is then given by:

$$\varepsilon_m = \frac{V_D}{I\,N\,Z_{D-S}}, \tag{7.3}$$

where $Z_{D\text{-}S}$ is the sensitivity of the detection winding as discussed in chapter 4. This measurement will almost surely give a worst-case estimate of the magnetic that will be encountered when the ratio windings are applied, assuming some minimal care is taken to distribute the windings uniformly. Much has been written on the subject of magnetic error [4, 9, 21], and numerous test methods have been described, but in the author's view this simple test is the most relevant and effective one available. For completeness however, it is worth noting that another, less significant mechanism for magnetic error has been described by O. Petersons [9], and this source requires a different type of test for detection and measurement.

7.3 Magnetic Shielding to Reduce Magnetic Error

If the level of magnetic error thus measured exceeds the design requirements, the error can be substantially reduced by the use of a magnetic shield. The concept of magnetic shielding of cores to reduce the errors in transformer-like devices was first described by A. M. Thompson in his classic paper of 1958 [24]. The idea seems to have been discovered independently but somewhat later by Miljanic, Kusters and Moore [21], and it was this group that led to its widespread use in current comparators.

As illustrated in fig. 7.5, a magnetic shield consists of a hollow toroidal box of high-permeability magnetic material that encloses the detection winding. By intercepting the errant elements of magnetic flux that were shown in fig. 7.3, a magnetic shield ensures that loops representing the ratio windings always link the entire flux, Φ, regardless of orientation around the core.

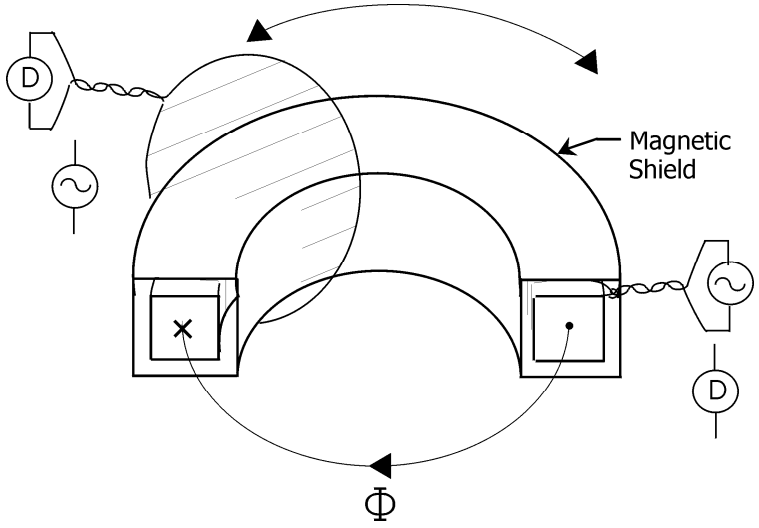


Figure 7.5 Use of Magnetic Shield to Reduce Magnetic Error

The requirements for a magnetic shield are as follows: (1) All closed loops on the Toroidal surface must be low reluctance, and (2) All closed loops penetrated by the core must be high impedance. Therefore, toroidal half-shells (fig. 7.6) must have an electrically insulated barrier between them, and the barrier must be thin and widely overlapping to minimize the reluctance between them.

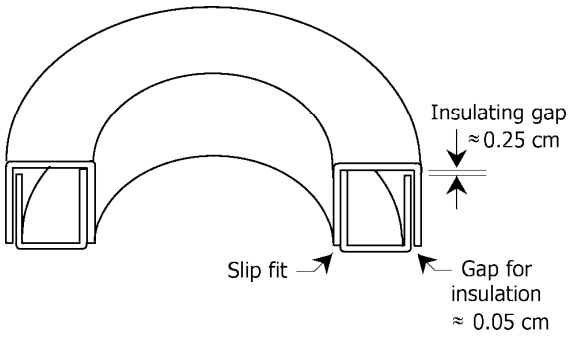


Figure 7.6 Magnetic Shield – ½ of Shield Shown to Illustrate Cross Section

The shield design shown in fig. 7.6 meets these requirements and is quite effective. (Note that only half of the shield is shown to reveal the cross section.)

The material forming the box is typically 0.125 cm mumetal, with mumetal-welded seams. After fabrication, the box should be annealed to achieve the maximum permeability. An insulating gap of about 0.05 cm is left at the outer overlap of the two half-boxes, and it should be filled with a flexible insulator to ensure that no contact is possible between these two sides. Otherwise, closed loops around the minor circumference of the core could be short-circuited and rule 2 above would be violated. On the other hand, the gaps should be kept small so that rule 1 is obeyed. If the height of the overlapping region is very large with respect to the dimension of the gap, then the reluctance around the minor circumference of the toroid will be low. Such a shield remains effective for all frequencies at which the permeability remains high. Eventually however, eddy current losses in the material reduce the effective permeability of such shields to the point that they are no longer useful.

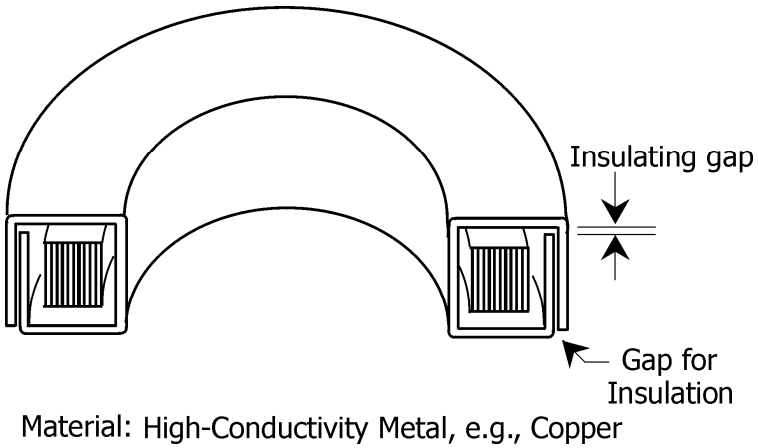


Figure 7.7 Eddy Current Shield – ½ of Shield Shown to Illustrate Cross Section

To achieve useful magnetic shielding at higher frequencies, eddy current shields can be used. As shown in fig. 7.7, these are toroidal boxes made of high-conductance, non-magnetic metals, and work by excluding flux penetration. Flux entering a high-conductivity shield with thickness greater than the skin depth of the material generates eddy currents that oppose the flux, and this phenomenon is responsible for their effectiveness. In this case, all closed loops on the toroidal surface should ideally have low resistance, and like the magnetic shields previously considered, all closed loops penetrated by the core must be of high resistance. These two requirements are of course in conflict for loops around the minor core circumference. The second requirement must be strictly met to avoid a shorted turn which would be totally unacceptable; therefore the first requirement can only be met for most but not all loops. By allowing a large overlap region however, such shields are still quite effective at higher frequencies.

The skin depth, δ, for non-magnetic metals is given by:

$$\delta = \left(\frac{2\rho}{2\pi f \mu_0} \right)^{1/2}, \tag{7.5}$$

where f is the frequency, and ρ is the resistivity in Ω - m. For copper, this gives a skin depth of 0.065 m/s$^{1/2}$ per root Hertz. At 60 Hz, the skin depth for copper is 0.84 cm, which requires a fairly bulky shield to be effective; however at 10 kHz it is only 0.65 mm, and reasonably lightweight shields are effective at that frequency. Fortunately, many magnetic shields remain effective at frequencies of 1 kHz or higher.

Eddy current shields like that shown in fig. 7.7 present some construction difficulties because at least one seam must be joined after the shield parts are assembled around the core. While three of the seams can be welded (e.g., with copper) before final assembly, the last seam must be sealed afterwards, with a lower temperature procedure. Either low-temperature lead-tin solders or other solders such as Wood's metal can be used.

Table 7.1 lists approximate values for the lowest magnetic error achievable with different configurations. In all cases, it is assumed that the windings are each uniformly distributed in one layer on a high permeability core (except for the last case in which an air core is usually used).

Table 7.1 Lowest Achievable Magnetic Error for Different Configurations

Configuration	**Minimum Magnetic Error, ε_m**
No Shielding	10^{-5}
Single Magnetic Shield	10^{-7}
Eddy Current Shield	10^{-6}
Magnetic and Eddy Current Shields	10^{-8}
Superconducting Shield (dc only)	10^{-10}

Note that exceptional shielding can be achieved with a combination of magnetic and eddy current shields. For a thorough discussion of shielding and the use of combination shields, see [4, 9].

8. Calculation and Management of Capacitive Errors

Because capacitance is unavoidably associated with the windings of transformer-like devices, small amounts of current are shunted away from windings, and are directed from one winding to another. One effect is that the current entering one terminal of a winding is generally not the same as the current leaving the other terminal. Another effect is that the current ratio of the device is changed by the flow of capacitance currents. Both of these effects are dependent on the driving voltages behind the capacitive currents, which in turn are dependent on the network impedances and particularly the burden. It is apparent then that precision measurements will require that the current ratio be well-defined. This means:

1. Specifying the terminals where the currents are defined,
2. Specifying the terminal voltages, and
3. Specifying the burden.

If the current ratio is thus defined and if the winding geometries are relatively simple, then it is possible to calculate the expected capacitive errors. The general approach, first outlined by P. Miljanic [19], is as follows:

1. First, assume that the principle of superposition is valid,
2. Locate a likely source of capacitance and estimate its value,
3. Express the voltage across the capacitance as the product of a winding current and impedance,
4. Calculate the resulting capacitive current and multiply by the number of turns it links (when it is not included in the defined current) or shunts (when it is included),
5. Divide the results by the main ampere-turns to get the component of capacitive error, and
6. Evaluate the sign of the error (i.e., via factor k_C, below).

In some cases, it is useful to incorporate electrostatic shields in transformer designs to help manage capacitive errors. Such shields, made from metal foil or conducting paint or epoxy, help in defining and redirecting capacitive currents. Once capacitive errors have been calculated or measured, it is almost always possible to minimize the error by introducing another (discrete) capacitance in the network that produces an equal and opposite effect.

8.1 Evaluation of Sign Factor, k_C

To begin the process of calculating capacitive errors, we will start with the last item in the list above, evaluating the sign of the error. Once a capacitive current has been identified, the sense of its effect on the overall ratio error of the device is determined by the turns that it links or bypasses. Although it is a good practice for the designer to work this out to his or her own satisfaction, we reduce the problem here to a selection of four possibilities listed in Table 8.1. For a current to be included in the defined current, it must flow into (or out of) the defining terminal for that defined current. Some examples given below will help to clarify this point.

Table 8.1 Evaluation of Sign Factor, k_C

Winding	Conditions	k_C
Secondary	Capacitance current is included in the defined I_S but does not flow through all N_S turns	+1
	Capacitance current is not included in the defined I_S but links at least some of secondary turns	-1
Primary	Capacitance current is included in the defined I_P but does not flow through all N_P turns	-1
	Capacitance current is not included in the defined I_P but links at least some of primary turns	+1

8.2 Calculating Capacitive Errors: Examples

The following examples illustrate how the six steps given above are used to calculate capacitive errors. In Miljanic's paper [19], examples of simple current comparators with unshielded windings are given, and the reader should consult that paper for those applications. Most of the examples given here represent devices with transformer stages, i.e., two-stage transformers and compensated current comparators, and in many cases electrostatic shields are used, with the shields being at different potentials with respect to that of the defining terminal. Such conditions can occur in some transformer-ratio-arm bridge applications, as well as in current transformer testing. In all of the examples, the winding in question is assumed to be uniformly distributed in one layer, and the dotted terminal is assumed to be the terminal where the current is defined. The examples do not include compensation windings, detection windings or tertiary windings since in operation these winding are usually at zero, or at least constant potential everywhere, and are therefore rather easy to shield to prevent the flow of capacitive currents. Of course, the designer should verify this for the particular circuit in question before dismissing these windings as sources of capacitive error. When electrostatic shields are used, capacitive currents can flow between shields, or from the shields to ground. This needs to be considered by the designer also, since it could cause additional currents to be directed to or from the defined terminals. If all of the shields are at ground or virtual ground potential, this problem is eliminated since the voltage differences between shields and to ground are then all zero.

8.2.1 Transformer or Compensated Current Comparator: Secondary Shield Connected to Defined Terminal

This example is illustrated in fig. 8.1. The capacitive error considered here is due to the distributed capacitance between the winding and the shield. Differential elements of capacitance, *dC*, are illustrated along with differential elements of the resulting capacitive current, *dI*. These are given by:

$$dC = \frac{C_{SS}}{N_S} dN \quad \text{and} \quad dI = |V_N| j\omega dC \quad , \tag{8.1}$$

where C_{SS} is the total capacitance between the secondary winding and its shield, which is readily measured if the shield is disconnected.

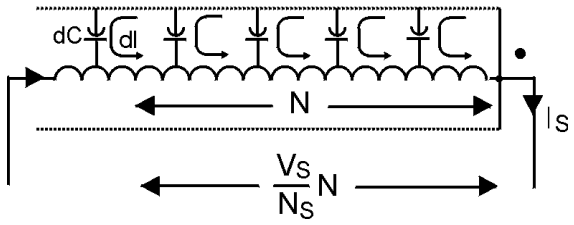


Figure 8.1 Capacitive Current in Secondary Winding of a Transformer or Compensated Current Comparator, with a Shield Connected to the Defined Terminal

Since this example involves the secondary winding of a device that transfers power to a burden, the voltage, V_S, at the unmarked terminal (with respect to the voltage at the marked) is $-I_S Z_B$. At any point along the winding, the voltage is given by:

$$V_N = \frac{N}{N_S}\left[-I_S\left(Z_S + Z_B\right) + I_S Z_S\right]. \tag{8.2}$$

The first term within the brackets represents the voltage induced in the winding, and the second term represents the voltage drop caused by the flow of the current through the distributed leakage impedance of the winding. Since the winding is assumed to be uniform, the resulting voltage diminishes linearly from the unmarked to the marked terminal. The absolute value of V_N is used in (8.1) because the sign information is applied separately via factor k_C. Note that the capacitive current flows from the shield to the winding and returns to the shield at the marked terminal. Since the current links some of the winding but never enters or leaves the marked terminal to be included in the defined current, the value for k_C is –1, which in (8.4) is represented as k_C^-. The net ampere-turns that excites the core is increased (adding to the effective excitation current), and as a result the secondary current is reduced by the same amount. In equation (8.3), the effective ampere-turns produced by the capacitive current is calculated by integrating the product of the differential currents and the number of turns they each link. (The use of a simple integration is of course an approximation because the turns have both discrete and continuous properties.)

$$\begin{aligned}(I \cdot N)_{EQ} &= \int_{N=0}^{N_S} N dI = j\omega I_S Z_B C_{SS} \int_{N=0}^{N_S} \frac{N^2}{N_S^2} dN = \frac{j\omega I_S Z_B C_{SS}}{N_S^2}\frac{N^3}{3}\Bigg]_{N=0}^{N_S} \\ &= \frac{j\omega I_S Z_B C_{SS} N_S}{3}.\end{aligned} \tag{8.3}$$

If we divide the results from (8.3) by the ideal secondary current, I_S, and include the sign factor we have

$$\varepsilon_{SS} = \frac{k_c^-(I \cdot N)_{EQ}}{I_S N_S} = -\frac{j\omega Z_B C_{SS}}{3}. \tag{8.4}$$

Therefore, the current ratio is given by

$$\frac{I_P}{I_S} = \frac{N_S}{N_P}\left(1 - \varepsilon_{SS}\right) = \frac{N_S}{N_P}\left(1 + \frac{j\omega Z_B C_{SS}}{3}\right). \tag{8.5}$$

In this case, the capacitive current causes additional ampere-turns to excite the core, and in response the secondary winding current is reduced by the same amount, causing the current ratio to increase.

8.2.2 Transformer or Compensated Current Comparator: Secondary Shield Grounded; Marked Terminal at Virtual Ground

This example illustrates how a simple modification of the last example causes a significant change in the size of the error, as well as a reversal of the polarity. In this case shown in fig. 8.2, the shield is connected to ground while the marked terminal is brought to a virtual ground as often occurs when a compensated current comparator is used. Although the capacitive currents appear to flow just as in fig. 8.1, there is an important difference: The current flows from ground into the winding while shunting parts of it, and exits the marked terminal to return to ground elsewhere in the circuit. Therefore, the conditions in the first row of Table 8.1 apply, and the sign factor, k_C, is +1.

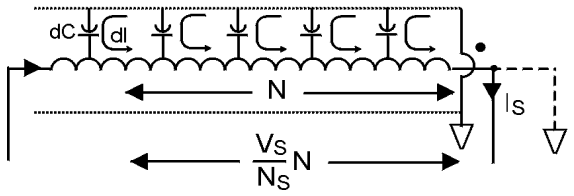


Figure 8.2 Capacitive Current in Secondary Winding of a Transformer or Compensated Current Comparator, with a Grounded Shield and Marked Terminal at Virtual Ground

The values for *dC*, *dI* and V_N are as before in (8.1) and (8.2). Since in this example the capacitive current is part of the defined secondary current but does not link all N_S turns, we calculate the ampere-turns that are lost. Therefore, the net ampere-turns is given by

$$(I\cdot N)_{EQ} = \int_{N=0}^{N_s}(N_S - N)dI = j\omega I_S Z_B C_{SS}\int_{N=0}^{N_s}\frac{(N_S-N)N}{N_S^2}dN = \frac{j\omega I_S Z_B C_{SS}}{N_S^2}\left(\frac{N^2}{2}-\frac{N^3}{3}\right)\Bigg]_{N=0}^{N_s} \quad (8.6)$$
$$= \frac{j\omega I_S Z_B C_{SS} N_S}{6},$$

and

$$\varepsilon_{SS} = \frac{k_c^+ (I\cdot N)_{EQ}}{I_S N_S} = +\frac{j\omega Z_B C_{SS}}{6}\ . \quad (8.7)$$

This gives the current ratio as

$$\frac{I_P}{I_S} = \frac{N_S}{N_P}(1-\varepsilon_{SS}) = \frac{N_S}{N_P}\left(1-\frac{j\omega Z_B C_{SS}}{6}\right). \quad (8.8)$$

8.2.3 Transformer or Compensated Current Comparator: Turn-to-Turn Capacitance of Secondary Winding

In the previous two examples, the winding-to-shield capacitive error was evaluated, but another source of capacitive error also exists for these two examples.

All windings have capacitance between the individual turns as indicated in fig. 8.3, and the resulting error must also be evaluated. If the windings are uniformly distributed and the capacitance, $C_{S\text{-}T}$, between turns is constant, then it is easy to show that the equivalent circuit at the bottom of fig. 8.3 is valid, in which a lumped $C_{S\text{-}T}$ appears across the winding terminals.

In this case, the capacitance $C_{S\text{-}T}$ is not readily measured directly, but it can be estimated by measuring the capacitance between two isolated turns having the same geometry and spacing.

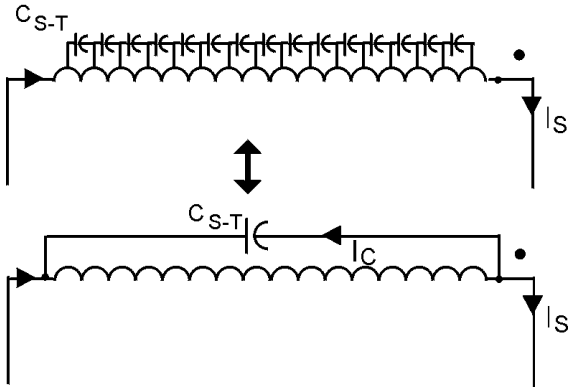


Figure 8.3 Turn-to-Turn Capacitance of Secondary Winding

For this example, k_C is –1 since the current is not included in the defined I_S, and the secondary winding voltage is

$$V_S = \left[- I_S \left(Z_S + Z_B \right) + I_S Z_S \right], \tag{8.9}$$

and the equivalent net ampere-turns is given by

$$\left(IN \right)_{EQ} = \left| V \right| j\omega C_{S-T} N_S . \tag{8.10}$$

The resulting error is:

$$\varepsilon_{S-T} = \frac{k_c^- \left(IN \right)_{EQ}}{I_S N_S} = - j\omega Z_B C_{S-T} . \tag{8.11}$$

Note that shunt capacitance causes a negative ratio error. This means that it is possible to offset positive capacitive errors as in the example of section 8.2.2 by introducing additional shunt capacitance across the winding.

8.2.4 Transformer or Compensated Current Comparator: Primary Shield Grounded; Marked Primary Terminal at Virtual Ground

This example is the primary-winding equivalent of the example shown in section 8.2.2, and is illustrated in fig. 8.4.

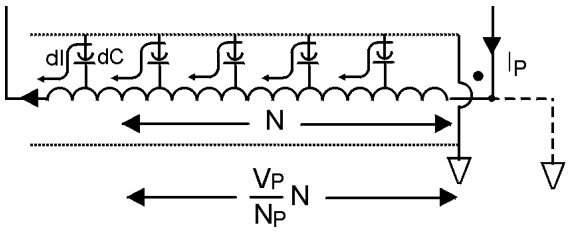


Figure 8.4 Capacitive Current in Primary Winding of a Transformer or Compensated Current Comparator, with a Grounded Shield and Marked Terminal at Virtual Ground

Note that the capacitive current flows from the shield to the winding and returns to the shield via a ground elsewhere in the circuit. Additional ampere-turns are added, and the current is not included in the defined primary current; therefore, from the last row of 8.1 we see that k_C is +1. As before, the differential current and capacitance are:

$$dC = \frac{C_{PS}}{N_P} dN \quad \text{and} \quad dI = \left|V_N\right| j\omega dC \ . \tag{8.12}$$

The voltage drop along the winding includes a component due to the primary leakage impedance, Z_P, and one due to the reflected impedance of the secondary circuit, Z_X, as follows:

$$V_N = \frac{N}{N_P} I_P \left[Z_P + \left(\frac{N_P}{N_S} \right)^2 \left(Z_S + Z_B \right) \right] = \frac{N I_P Z_X}{N_P} \ . \tag{8.13}$$

The equivalent ampere-turns linking the core is:

$$\begin{aligned} (I \cdot N)_{EQ} &= \int_{N=0}^{N_P} \left(N_P - N\right) dI = j\omega I_P Z_X C_{PS} \int_{N=0}^{N_P} \frac{N\left(N_P - N\right)}{N_P^2} dN \\ &= j\omega I_P C_{PS} Z_X \left(\frac{N^2}{2N_P} - \frac{N^3}{3N_P^2} \right) \Bigg]_{N=0}^{N_P} = \frac{j\omega I_P C_{PS} Z_X N_P}{6}, \end{aligned} \tag{8.14}$$

and the resulting error is:

$$\varepsilon_{PS} = \frac{k_c^+ (I \cdot N)_{EQ}}{I_P N_P} = + \frac{j\omega Z_X C_{PS}}{6} \ . \tag{8.15}$$

Therefore, the current ratio is similar to that of the corresponding example with the secondary winding treated in section 8.2.2. Likewise, when the shield is connected to the marked primary terminal, the resulting error is:

$$\varepsilon_{PS} = \frac{k_C^-(I \cdot N)_{EQ}}{I_P N_P} = -\frac{j\omega Z_X C_{PS}}{3}\ , \tag{8.16}$$

which also corresponds to the secondary winding example in section 8.2.1.

8.2.5 Transformer or Compensated Current Comparator: Turn-to-Turn Capacitance of Primary Winding

In this last example, the effect of turn-to-turn capacitance associated with the primary winding is considered, as illustrated in fig. 8.5.

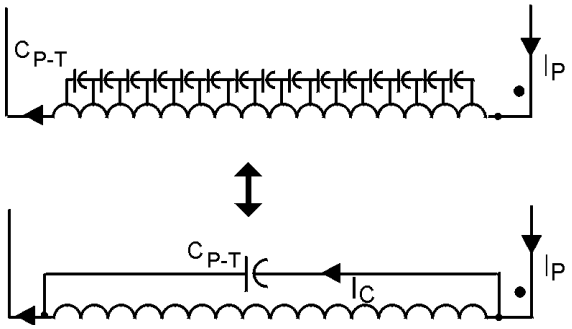


Figure 8.5 Turn-to-Turn Capacitance of Primary Winding

Here, the voltage, V, across the winding, and thus across the lumped capacitance, $C_{P\text{-}T}$, is:

$$V = I_P Z_X\ , \tag{8.17}$$

where Z_X is the same as in the previous example above. Since the capacitive current is included in the defined primary current but shunts some (or in this case all) of the primary turns, the sign factor, k_C, is –1 from Table 8.1, and the equivalent ampere-turns is:

$$(IN)_{EQ} = |V| j\omega C_{P-T} N_P\ . \tag{8.18}$$

This gives an error of:

$$\varepsilon_{S-T} = \frac{k_C^-(IN)_{EQ}}{I_P N_P} = -j\omega Z_X C_{P-T}\ , \tag{8.19}$$

which is also similar to the corresponding case involving the secondary winding.

8.3 Trimming of Capacitive Errors in Transformers or Compensated Current Comparators

As suggested previously, some capacitive errors can be trimmed by adding shunt capacitance across the winding. In almost all cases, a similar approach can be found, possibly using an inverting amplifier, to trim the errors. In any case, the value of the trimming capacitance can be calculated using the formula given in the examples above, or in some cases the value can be

determined directly via a measurement as illustrated in fig. 8.6. In the author's experience, the calculated values can be relied upon with an uncertainty of better than 10 percent, assuming that the windings and shields are reasonably uniform around the core.

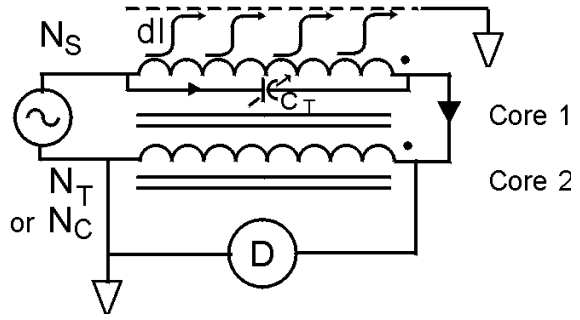


Figure 8.6 Trimming Capacitive Error in a Two-Stage Transformer or Compensated Current Comparator

The figure shows a procedure for trimming the capacitive error discussed in section 8.1, in which the secondary marked terminal is at virtual ground and the secondary shield is grounded. As noted before, such an error can be trimmed with the appropriate capacitance connected across the secondary winding, as indicated by trimmer capacitance, C_T, in the figure. The procedure is to connect the secondary winding in series opposition with the tertiary (or compensation) winding, as shown, and to excite the windings with an appropriate voltage source. (Since the winding is being excited from an external voltage source in this case, the capacitive currents flow differently than in the example of section 8.1; nevertheless, the resulting errors are the same.) The outer core (core 1), will be excited and the magnetizing current flowing in the secondary winding returns through the tertiary or compensation winding. If no capacitive currents flow, then core 2 will experience zero net ampere-turns, and thus no flux will be present. However, the excitation of the first core will cause capacitive error current to flow to the shield, returning via the ground connection. The net ampere-turns of the capacitive error current will then create an imbalance in core 2, inducing voltage in the tertiary (or compensation winding) that is detected as shown. If the trimmer capacitance is connected, then compensating ampere-turns are created, and a value can be found that balances the detector. This method requires that the tertiary or compensation winding have the same number of turns as the secondary winding, which is usually the case. As show, the accuracy of the method is limited by the voltage drop in the tertiary or compensation winding caused by the magnetizing current flowing through the tertiary or compensation winding leakage impedance, Z_T or Z_C. Since the source voltage is equivalent to the secondary winding voltage in operation, the magnetizing current can be expressed as:

$$I_m \approx I_S \frac{Z_S + Z_B}{Z_{m1}} \ , \tag{8.20}$$

and the voltage drop across the tertiary winding is:

$$I_m Z_T \approx I_S \frac{(Z_S + Z_B)Z_T}{Z_{m1}} \ . \tag{8.21}$$

The voltage induced in the tertiary winding by the capacitive error current, $\varepsilon_C I_S$, is:

$$V_{Det} = \varepsilon_C I_S N_S Z_{Sens}\,, \tag{8.22}$$

where Z_{Sens} is the sensitivity of the tertiary winding. Equating (8.21) with (8.22), we get the minimum detectable capacitive error:

$$\varepsilon_C = \frac{(Z_S + Z_B)Z_T}{N_S Z_{m1} Z_{sens}}\,. \tag{8.23}$$

Since (8.23) is inversely proportional to test frequency until leakage inductances and eddy current losses begin to dominate, it is usually possible to perform the test at a frequency for which ε_C is no greater than 10^{-6}. This source of uncertainty can be eliminated if the test device is a compensated current comparator, and the detector is connected across the detection winding instead of the compensation winding.

Once the capacitive error from the secondary winding has been compensated with the method just discussed, the primary winding can be compensated with a similar procedure. See [10] for more details.

8.5 Additional Comments on Capacitive Errors

As noted in section 8.2, both the sign and magnitude of capacitive errors may be different for simple current comparators versus the examples given here. In addition, the errors of unshielded windings will also differ. The methods given here and in [19] however should allow the designer to evaluate the errors for many different configurations, so long as the geometry is simple and well known. It should also be reiterated that careful attention be paid to the exact way in which the device will be used, since the complete circuit in which the device will be embedded determines the voltages that will appear at different terminals. Finally, great care should be taken to avoid capacitive coupling from the ratio windings to sources of power-line voltage. The currents thus generated can cause large errors if the circuit itself is being operated at power-line frequency, and can cause “beating” at the difference frequency if another operating frequency is used. A characteristic of these errors is that they are inversely proportional to the level of the test current, being proportionately larger at low test currents.

9. CURRENT TRANSFORMER TESTING

An important application of current comparators and two-stage transformers is in the testing of simple instrument current transformers that are used for metering purposes. When used for this purpose, the two-stage transformer or current comparator serves as a standard device whose ratio is compared to that of the transformer-under-test.

Today, most standards that are used for testing current transformers fall into two different categories: transformer-like standards, and compensated current comparators. They both have the advantage that they impose very little burden on the transformer under test. This is important because the errors of simple transformers are quite dependent on the burden that they supply (as indicated in (1.2)), so it is customary to test them with the same burden that they experience in the field. Therefore, the residual burden imposed by the test circuit must be smaller than any

burden that may be specified by the test requirements. The two types of standard devices are not interchangeable however. Each type requires a different measuring circuit to make the comparison between the standard device and transformer under test. The two approaches are discussed below.

9.1 Transformer Testing Using a Standard Transformer

Transformer-like standards are devices that can maintain high accuracy while supporting a burden. Examples include the active two-stage transformers and active current-comparator correction circuits discussed in section 6.2 and 6.3, respectively. The normal two-stage transformer can also be used so long as the tertiary winding is only connected across the measuring resistor, R, in fig. 9.1. In all cases, the ratio of the standard transformer is chosen to be nominally equal to that of the test transformer, i.e.,

$$\frac{N_{SS}}{N_{PS}} \approx \frac{N_{SX}}{N_{PX}}. \tag{9.1}$$

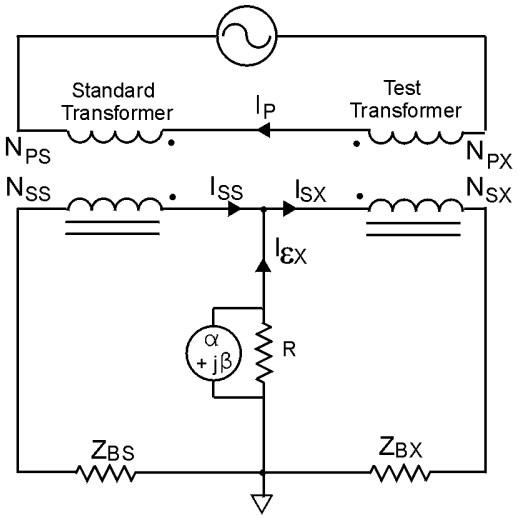


Figure 9.1 Transformer Testing with a Transformer-Like Standard

Under this condition, the difference between the two secondary currents, $I_{\varepsilon X}$ is small and flows through a low impedance circuit where its in-phase and quadrature components are measured with respect to the standard secondary current, I_{SS}. The equivalent burden, Z_B', imposed by the measuring circuit on both the standard and test transformers is

$$Z_B^{'} \approx \frac{\Delta V}{I_S} = \frac{I_{\varepsilon X} R}{I_S}, \tag{9.2}$$

where R is the impedance of the measuring circuit.

Many different types of measuring circuits can be used for this application, and a few possibilities are considered next.

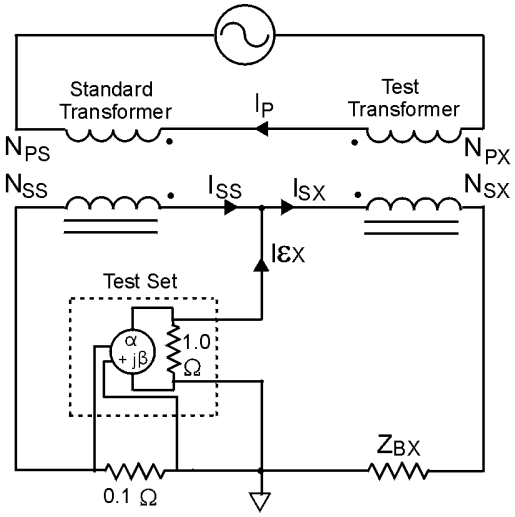


Figure 9.2 Test Set Based on Measurement of Error Current Through a Small Resistance

In fig. 9.2, the error current flows through a low valued (1 Ω) resistor, and the voltage drop across the resistor is measured in terms of the voltage drop across another low valued (0.1 Ω) resistor that carries the secondary current of the standard transformer. An electronic vector voltmeter circuit is used to resolve the in-phase (α) and quadrature (β) components of the error voltage. Although the accuracy of the two resistors has only second order importance, they must have reasonably low reactance at the operating frequencies of interest.

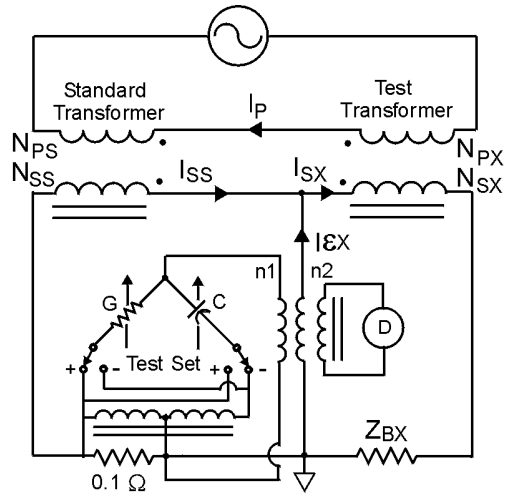


Figure 9.3 Test Set Based on Measurement of Error Current in a Current Comparator Winding

The circuit shown in fig. 9.3 illustrates another way in which the error current can be measured. It incorporates a simple current comparator and a G-C current injection network [4, 11, 18]. Here the error current is directed into a low-impedance winding of a simple, unshielded current comparator where it is compared with the adjustable current set by the programmable conductance, G, and capacitance, C. Complementary, selectable reference voltages across these elements assure that the adjustable current is proportional to the secondary current, $I_{SS,}$ and that

both polarities are accommodated. The current is adjusted to reach a null on the detector. Assuming that the standard transformer has negligible error, that $0.1(G+j\omega C)<<1$, and that the leakage impedance of winding n1 is negligibly small, the transformer error is then given by:

$$\varepsilon_X = -\frac{I_{\varepsilon x}}{I_{SS}} = 0.1\frac{n_1}{n_2}\left[\pm G \pm j\omega C\right] = \alpha + j\beta\,. \tag{9.3}$$

At detector balance, the voltages across the windings n1 and n2 are small, assuring that the burden imposed by the test circuit is small, and that the expression in (9.3) remains accurate. By providing selectable turns ratios, n_1/n_2, via additional windings, the circuit can accommodate different ranges of transformer error.

Other test set designs suitable for use in the example of fig. 9.3, as well as the compensated current comparator example discussed next, can be found in [6, 11].

9.2 Transformer Testing Using a Compensated Current Comparator

As noted in section 3.1, the compensated current comparator [20] is used to detect ampere-turn balance among its primary, secondary and compensation windings while imposing minimal burden on the external circuit. To bring this condition about in a transformer test circuit, the error current must be injected from a current source as shown in the example of fig. 9.4.

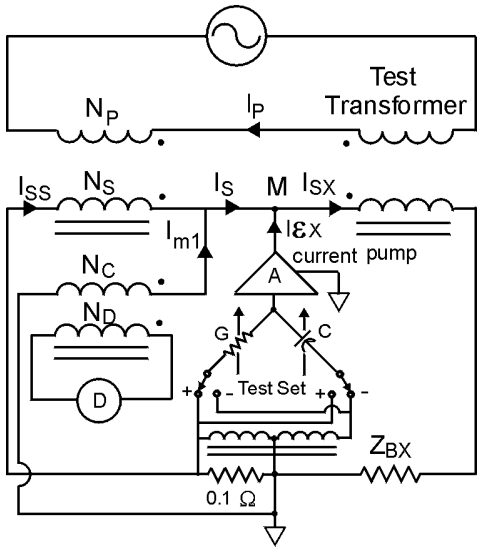


Figure 9.4 Transformer Testing with a Compensated Current Comparator

In this example, the current from a G-C network of the type shown above is pumped into node M to balance the detector. With sufficiently high output impedance and compliance voltage, the current pump can overcome the voltage that exists at node M while the current comparator is still unbalanced. Assuming that the current comparator has negligibly small error, the error of the transformer under test is given by:

$$\varepsilon_X = 0.1A\left[\pm G + j\omega C\right], \tag{9.4}$$

where *A* is the current gain of the current pump.

As noted previously, other balancing networks such as those described in [6, 11] can be used in place of the G-C network and current pump shown here.

9.3 Secondary Feed with a Compensated Current Comparator

As previously noted, the voltage across the compensation winding of a compensated current comparator is effectively zero when the comparator is balanced, thus eliminating the comparator circuit as a source of burden for the test transformer. No power is transferred between the two secondary circuits; instead, the power required to energize the secondary circuit of the current comparator is supplied via the comparator's transformer stage. Alternatively, the power supply can be placed in the secondary circuit of the current comparator, and the transformer stage can be used as a supply transformer to provide the primary current for both devices. This is illustrated in fig. 9.5. With this approach, a separate, high current supply transformer is not needed; however, the transformer stage must be designed so that it can support the large secondary winding voltage that is usually required in this application for large turns ratio, N_S/N_P. This voltage is given by:

$$V_S \approx I_S \left[\left(\frac{N_S}{N_P} \right)^2 \left(Z_{PX} + Z_{PL} + Z_{PS} \right) + \left(Z_{SX} + Z_{BX} + Z_{SS} + Z_{BS} \right) \right], \tag{9.5}$$

where Z_{PX} and Z_{PS} are the primary leakage impedances of the current comparator and test transformer respectively, Z_{SX} and Z_{SS} are the respective secondary leakage impedances, and Z_{PL} is the impedance of the external primary circuit. For large ratios where the primary current is high, the inductive component of Z_{PL} becomes the dominant term in (9.5). For example, if the turns ratio is 200 and the inductance of the primary circuit is 2 μH, the voltage due to this term alone will exceed 150 V at 60 Hz with a primary current of 1000 A.

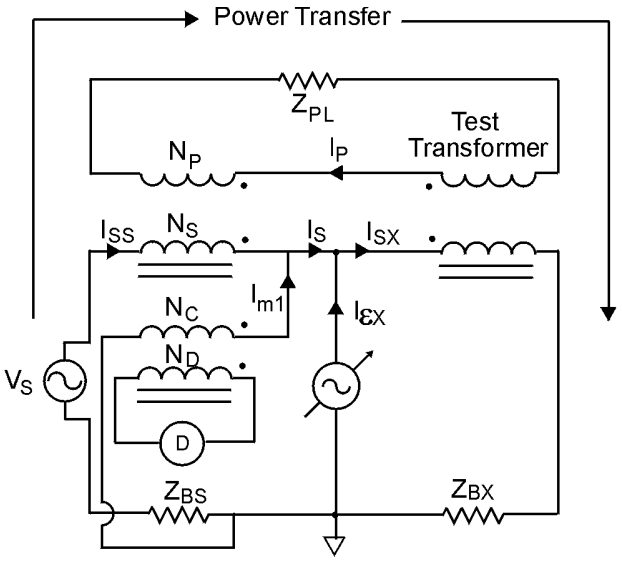


Figure 9.5 Transformer Testing with Compensated Current Comparator Using Secondary Feed

It should also be noted that a larger voltage will increase the capacitive errors associated with the secondary winding, as noted in chapter 8.

9.4 Testing Transformers with Ratios Less Than Unity

Some commercial multi-range transformers can accommodate ratios as low as 0.05 (e.g., 0.25 A/5 A). A standard transformer or compensated current comparator with matching ratios faces serious capacitive errors: Since the secondary windings must have enough turns to support a reasonable burden, the primary windings have an unusually large number of turns to accommodate the low ratios. Whether primary or secondary feed is used, a large voltage can be expected across the primary winding of a conventional current comparator because the reflected secondary circuit impedance is multiplied by the square of the turns ratio. This, in conjunction with the large number of turns, can produce unusually large capacitive errors. For this reason, a special comparator circuit has been designed to accommodate low-ratio test transformers [12]. In that design, the test set is moved from the secondary to the primary circuit in an effort to minimize the secondary circuit impedance. An alternative design shown in fig. 9.6 was developed many years ago by the author, but not hitherto published. In this design, the transformer stage of the current comparator is physically separated from the current comparator function, so that they no longer share common windings. With this approach, it is possible to use far fewer turns for the current comparator itself, noting only that the ratios must match, i.e., $N_{PT}/N_{ST}=N_{PC}/N_{SC}$. Because the job of transferring power falls only on the separated current transformer, nearly all of the required voltage appears across its primary winding and not that of the current comparator. With shields placed as shown, all of the resulting capacitive currents are captured and measured by the current comparator windings. By grounding the primary circuit, virtually no current flows between the shields.

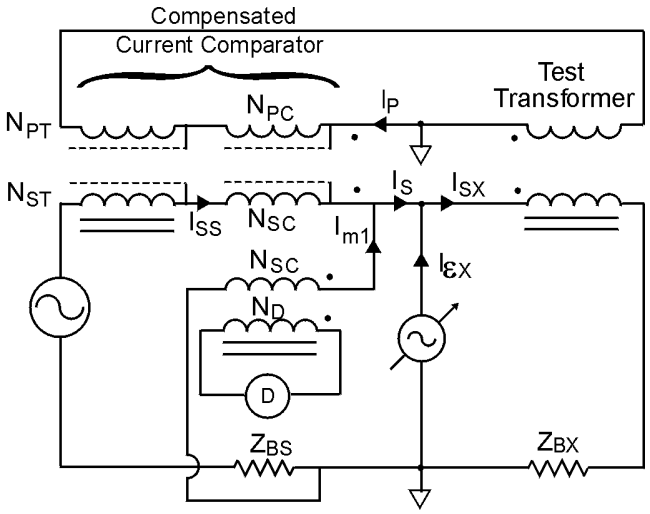


Figure 9.6 Special Purpose Compensated Current Comparator for Ratios Less Than Unity

9.5 Measuring the Test Transformer Burden

Since the errors of current transformers are dependent on the burdens they encounter, a measurement of the test burden is important in transformer testing. The standard approach for

this measurement is to connect a resistor of known value across the secondary terminals of the test transformer and to note the change in indicated error as the test circuit is rebalanced. The resistor shunts a portion of the test secondary current away from the measurement node, which is proportional to the burden. Assuming that the resistor, r, is large enough that it has negligible effect on the burden, this measurement gives:

$$Z_B = -r\Delta\varepsilon\,, \tag{9.6}$$

where $\Delta\varepsilon$ is the change in complex ratio error. A resistance value of 1000 Ω is usually suitable for most measurements.

10. CALIBRATION METHODS AND DETERMINATION OF UNCERTAINTIES

There are three general methods for determining the errors of current transformer-like devices. First, the errors can be estimated using the design equations presented in earlier chapters, along with measurement or estimation of the relevant parameters such as leakage and magnetizing impedances, maximum magnetic errors, and capacitive errors. Second, the errors can be measured directly in terms of a reference standard device, using comparison techniques like those discussed in chapter 9 and in [5]. For comparison techniques appropriate for current comparators, see [4, 18]. Finally, absolute calibrations of transformers and current comparators can be made using various step-up techniques. These require two or more devices and usually bootstrap from simple calibrations of their 1/1 ratios to build up the calibrations of all the higher ratios in multiple steps. Examples of these approaches can be found in [2, 4, 10, 18].

A typical circuit for calibrating the base 1/1 ratio of a current transformer is illustrated in fig.10.1. The same circuit can be used for two-stage transformers and for active correction devices that behave as current transformers, e.g., the devices discussed in section 6.2 and 6.3. Related circuits can be used for current comparators, although auxiliary sources are usually required [4, 18].

As shown in the figure, the difference between the primary and secondary currents flows through winding n2 of the measuring circuit, where it is balanced with the current generated from the admittance network of the test set.

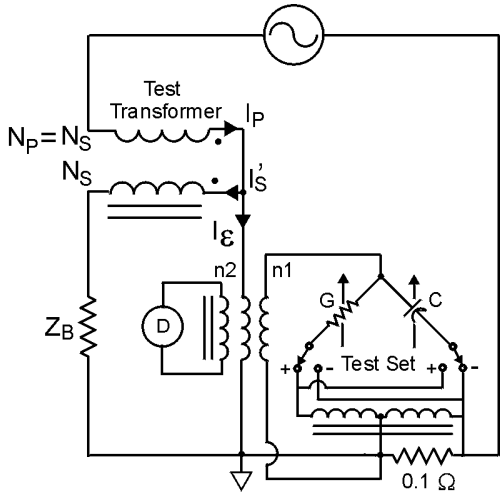


Figure 10.1 Calibration of the 1/1 Base Ratio of a Transformer

By placing the 0.1 Ω resistor of the test set on the primary side of the ground connection, it does not contribute to the burden seen by the test transformer.

The calibration of the 1/1 ratio can be used as the starting point for a step-up calibration procedure as previously noted, or it can be used to corroborate error calculations made via the design equations. For devices that have fixed secondary windings, the errors due to magnetizing impedance and secondary-winding capacitances should not change with changes in ratio. Similarly, for devices that use the series-parallel configuration for the primary windings discussed in section 5.2, or devices that have very effective magnetic shielding, the magnetic errors should also remain unchanged with changes in ratio. Under these conditions, the capacitive errors associated with the primary windings should be the only errors that change when the ratio is changed. Therefore, the measurement of the 1/1 ratio is indicative of the major error contributions at all ratios. In [2], Corney presents a formula to estimate the change in capacitive error when switching from the series to the parallel connection for transformers using a series-parallel primary configuration.

For many applications, error calculations that have been corroborated with 1/1 ratio measurements are sufficient. However, when the highest level of certainty is required, step-up procedures must be used. These are typically rather difficult and tedious to perform, and require additional test devices and equipment. The simpler step-up procedures require two multi-ratio test devices with appropriate ratios, and intercomparison circuitry [2, 10], while still relying on certain minimal assumptions. For example, in [10] the two test devices are compared using a simple current comparator having only three ratios (1/1, 2/2 and 2.5/1). Strong arguments can be made that its errors are negligibly small. The most rigorous step-up procedures require at least three test devices, along with multiple sources and balances [4, 18], and are rarely warranted.

11. REFERENCES

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