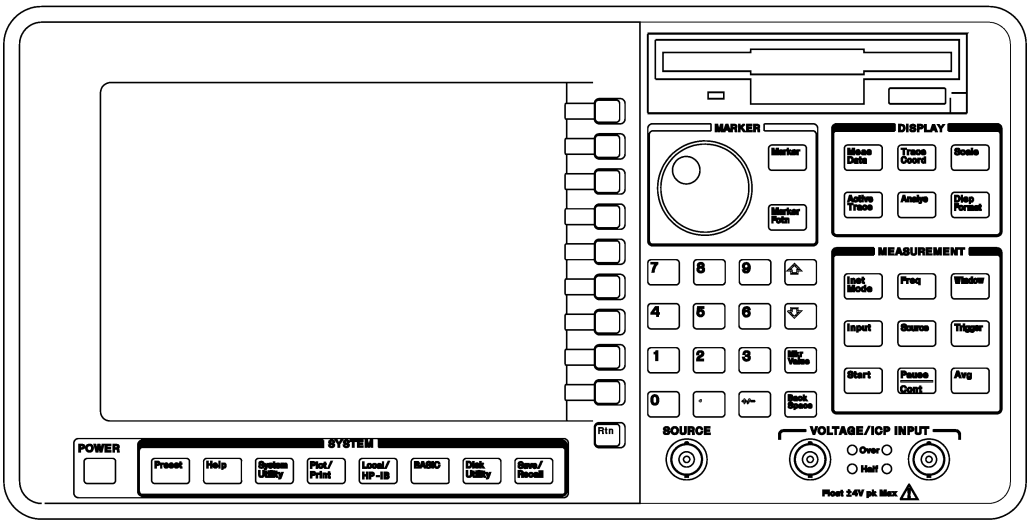
Agilent 35670A Service Guide



Agilent Technologies

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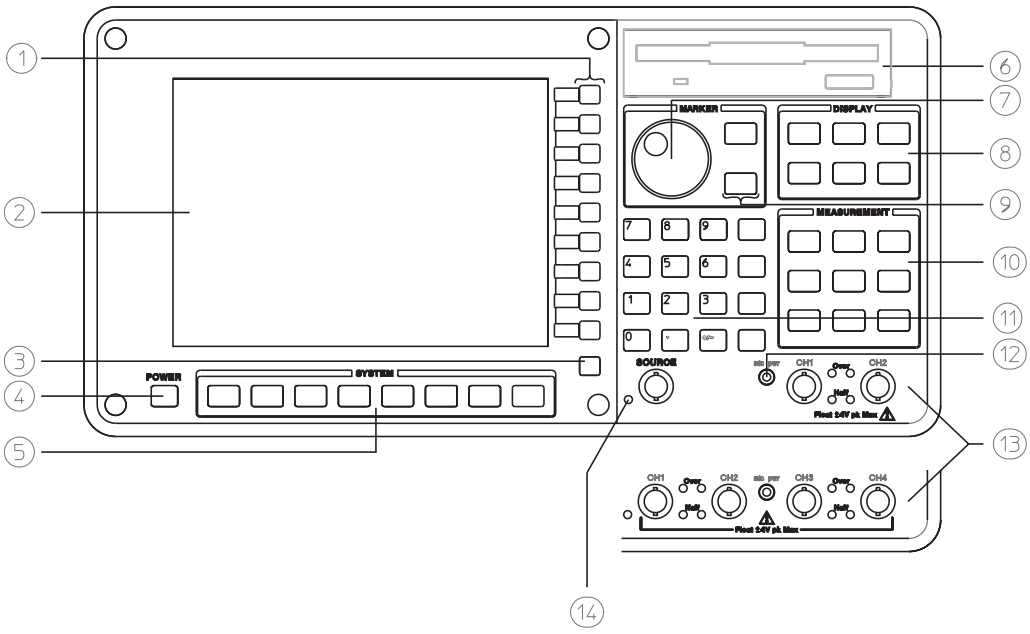
The Agilent 35670A at a Glance (Front Panel)



Agilent 35670A Front Panel

1-Use the softkeys to select items from the current menu. A softkey's function is indicated by a video label on the analyzer's screen. Throughout this book, softkeys are printed like this: [FFT ANALYSIS].

Hardkeys are front-panel buttons whose functions are always the same. They have a label printed directly on the key itself. Throughout this book, hardkeys are printed like this: [**Inst Mode**].

2-The analyzer's screen is divided into the menu area and the display area. The menu area displays video labels for the softkeys. The data area displays measurement data and information about the parameter settings.

3-The [**Rtn**] key returns the menu to the previous level.

4 -The POWER switch turns on the analyzer.

5 -Use the SYSTEM keys to control various system-level functions. These functions include saving files, plotting measurement data, and accessing online help.

6 -Use the disk drive to save your work on 3.5 inch flexible disks.

7-The knob moves the markers and the cursor. It also steps through numeric values and scrolls through online help.

8 -Use the DISPLAY keys to control what appears on the analyzer's traces. They only affect how data is displayed; DISPLAY keys do not change measurement parameters. *You can press keys in the DISPLAY menus without losing measurement parameters.*

9 -Use the MARKER keys to select a variety of marker features.

10-Use the MEASUREMENT keys to control the analyzer's source and inputs. They also control measurement parameters. *You must make a new measurement if you change a MEASUREMENT parameter.*

11-Use the numeric-entry keys to enter a numeric value.

12-The microphone power connector provides power (8 Vdc) for the Microphone Adapter Kit (Option UK4).

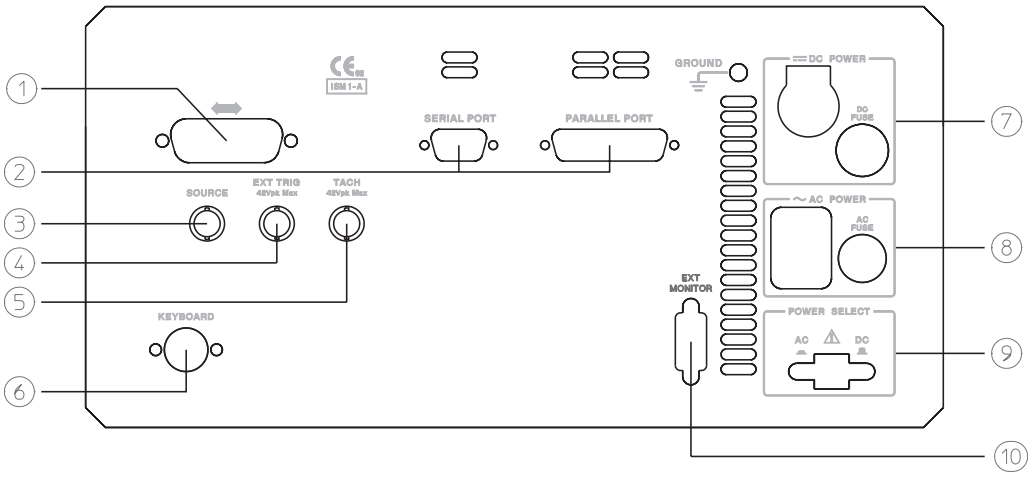
13-The connector area of the front panel has two different configurations. The standard analyzer has a source output connector and two input connectors. The 4-channel analyzer (Option AY6) has four input connectors.

Range indicators are located next to each input connector. The upper LED is the over-range indicator (the signal level exceeds the current range setting). The lower LED is the half range indicator (the signal level exceeds half the current range setting).

14-A source on/off indicator is located at the left edge of the connector area.

The standard Agilent 35670A (2-channel) has a source connector on the front panel.

The Agilent 35670A at a Glance (Rear Panel)



Agilent 35670A Rear Panel

1-The GPIB connector links the Agilent 35670A to other GPIB devices. GPIB parameters are set in the [**Local/GPIB**] and [**Plot/Print**] menus.

2-The SERIAL PORT and the PARALLEL PORT link the analyzer to plotters and printers. These parameters are set in the [**Plot/Print**] menu.

3-The SOURCE connector outputs the analyzer's source signal. An LED on the front panel indicates if the source is on or off. The source parameters are set in the [Source] menu.

The standard Agilent 35670A (2-channel) also has a source connector on the front panel.

4-The EXT TRIG connector links the analyzer to an external trigger signal. The external trigger parameters are set in the **[**Trigger] menu.

5-The TACH connector links the analyzer to a tachometer. The tachometer parameters are set in the [Input] menu.

6-The KEYBOARD connector attaches an optional keyboard to the analyzer.

7-The DC POWER connector accepts DC power levels from 12 - 28 Vdc (nominal).

8-The AC POWER connector accept a wide range of ac voltage levels.

9-The POWER SELECT switch determines whether the analyzer is powered via the AC POWER connector or the DC POWER connector.

10-The EXT MONITOR port links the analyzer to multi-sync monitors.

Safety Summary

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Agilent Technologies, Inc. assumes no liability for the customer's failure to comply with these requirements.

GENERAL

This product is a Safety Class 1 instrument (provided with a protective earth terminal). The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

All Light Emitting Diodes (LEDs) used in this product are Class 1 LEDs as per IEC 60825-1.

ENVIRONMENTAL CONDITIONS

This instrument is intended for indoor use in an installation category II, pollution degree 2 environment. It is designed to operate at a maximum relative humidity of 95% and at altitudes of up to 4600 meters. Refer to the specifications tables for the ac mains voltage requirements and ambient operating temperature range.

BEFORE APPLYING POWER

Verify that the product is set to match the available line voltage, the correct fuse is installed, and all safety precautions are taken. Note the instrument's external markings described under Safety Symbols.

GROUND THE INSTRUMENT

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

FUSES

Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes.

DO NOT REMOVE THE INSTRUMENT COVER

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made only by qualified service personnel.

Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

Caution

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Safety Symbols

 Warning, risk of electric shock

 Caution, refer to accompanying documents

 Alternating current

 Both direct and alternating current

 Earth (ground) terminal

 Protective earth (ground) terminal

 Frame or chassis terminal

 Terminal is at earth potential.

 Standby (supply). Units with this symbol are not completely disconnected from ac mains when this switch is off

Regulatory Markings

	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australian EMC Framework regulations under the terms of the Radio Communications Act of 1992.
	The CE mark is a registered trademark of the European Community. ICES/NMB-001 indicates that this ISM device complies with the Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.
	Contains one or more of the six hazardous substances above the maximum concentration value (MCV), 40 Year EPUP.
	The CSA mark is a registered trademark of the CSA-International.
	This instrument complies with the WEEE Directive (2002/96/EC) marketing requirement. The affixed product label indicates that you must not discard this electrical/electronic product in domestic household waste.

Accessories

The accessories listed in the following table are supplied with the Agilent 35670A.

Supplied Accessories	Part Number
Line Power Cable	See page 2-4
Standard Data Format Utilities	HP 5061-8042
Agilent 35670A Operator's Guide	Agilent 35670-90053
Agilent 35670A Quick Start	Agilent 35670-90056
Agilent 35670A Installation and Verification Guide	Agilent 35670-90054
Agilent 35670A GPIB Command Reference	Agilent 35670-90057
GPIB Programmer's Guide	Agilent 5960-5708
Agilent 35670A GPIB Commands: Quick Reference	Agilent 35670-90048

The accessories listed in the following table are available for the Agilent 35670A.

Available Accessories	Part Number
DC Power Cable, 3 meter	HP 35250A
DC Power Cable with Cigarette Lighter Adapter	HP 35251A
Box of ten 3.5-inch double-sided, double-density disks	HP 92192A
Using Instrument BASIC with the Agilent 35670A	Agilent 35670-90049
Instrument BASIC User's Handbook	HP E2083-90000
HP Thinkjet Printer	HP 2225A
HP Quietjet Printer	HP 2227A
HP Jet Paper, 2500 sheets	HP 92261N
GPIB Cable, 1 meter	HP 10833A
GPIB Cable, 2 meter	HP 10833B
GPIB Cable, 4 meter	HP 10833C
GPIB Cable, 0.5 meter	HP 10833D

In This Book

This guide provides instructions for installing, verifying performance, and repairing the Agilent 35670A Dynamic Signal Analyzer.

Chapter 1, ''Specifications,'' lists the specifications for the Agilent 35670A and the specifications for the required test equipment.

Chapter 2, ''Preparing the Analyzer for Use,'' provides step-by-step instructions for getting the analyzer ready to use and instructions on cleaning the screen, storing, and transporting.

Chapter 3, ''Verifying Specifications,'' provides step-by-step instructions for installing and running the semiautomated performance test software. This chapter also provides illustrations that show the equipment set up for each test and a copy of the test records.

Chapter 4, ''Troubleshooting the Analyzer,'' provides step-by-step instructions for isolating most failures to the faulty assembly.

Chapter 5, ''Adjusting the Analyzer,'' provides step-by-step instructions for adjusting the analyzer.

Chapter 6, ''Replacing Assemblies,'' provides step-by-step instructions to follow before and after replacing an assembly. This chapter also provides step-by-step instructions for disassembling the analyzer.

Chapter 7, ''Replaceable Parts,'' provides ordering information and lists the replaceable parts.

Chapter 8, ''Circuit Descriptions,'' provides the overall instrument description and individual assembly descriptions.

Chapter 9, ''Voltages and Signals,'' shows where the signals and voltages are used in the analyzer and describes each signal.

Chapter 10, ''Internal Test Descriptions,'' describes the power-on test, calibration routine, fault log messages, and self tests.

Chapter 11, ''Backdating,'' provides information necessary to modify this manual for instruments that differ from those currently being produced.

Chapter 12, ''Quick Reference,'' shows assembly locations, cable connections, and all the block diagrams.

Table of Contents

2 Preparing the Analyzer for Use

3 Verifying Specifications

4 Troubleshooting the Analyzer

5 Adjusting the Analyzer

6 Replacing Assemblies

7 Replaceable Parts

8 Circuit Descriptions

1

Specifications

Specifications

This chapter contains the specifications for the Agilent 35670A Dynamic Signal Analyzer and the critical specifications for the equipment required to test the Agilent 35670A.

Instrument specifications apply after 15 minutes warm-up and within 2 hours of the last self-calibration. When the internal cooling fan has been turned OFF, specifications apply within 5 minutes of the last self-calibration. All specifications are with 400 line frequency resolution unless stated otherwise. Four channel instruments are unspecified in the one channel mode where alias protection filters are not connected.

Abbreviations

dBVrms = dB relative to 1 Volt rms.

dBfs = dB relative to full scale amplitude range. Full scale is approximately 2 dB below ADC overload.

FS or fs Full scale; synonymous with input range.

Real Time or Online = Refer to the collecting and displaying of information with no dropouts or missing information.

Rload = Load resistance connected to the analyzer's source.

Typical = Typical, non-warranted, performance specification included to provide general product information.

Vpk = Peak of the ac voltage.

Frequency

Maximum range	
1 channel mode	102.4 kHz, 51.2 kHz (option AY6†)
2 channel mode	51.2 kHz
4 channel mode (option AY6 only)	25.6 kHz
Spans	
1 channel mode	195.3 mHz to 102.4 kHz
2 channel mode	97.7 mHz to 51.2 kHz
4 channel mode (option AY6 only)	48.8 mHz to 25.6 kHz
Minimum resolution	
1 channel mode	122 mHz (1600 line display)
2 channel mode	61 mHz (1600 line display)
4 channel mode (option AY6 only)	61 mHz (800 line display)
Maximum real-time bandwidth (FFT span for continuous data acquistion) (preset, fast averaging)	
1 channel mode	25.6 kHz
2 channel mode	12.8 kHz
4 channel mode (option AY6 only)	6.4 kHz
Measurement rate (typical) (preset, fast averaging)	
1 channel mode	≥70 averages/second (≥170 with 100 line display)
2 channel mode	≥33 averages/second
4 channel mode (option AY6 only)	≥15 averages/second
Display update rate (typical) (preset, fast average off)	5 updates/second 9 updates/second (single channel, single display, undisplayed traces set with static data: e.g., data register)
Accuracy	±30 ppm (±0.003%)

† Option AY6 single channel maximum range extends to 102.4 kHz without anti-alias filter protection.

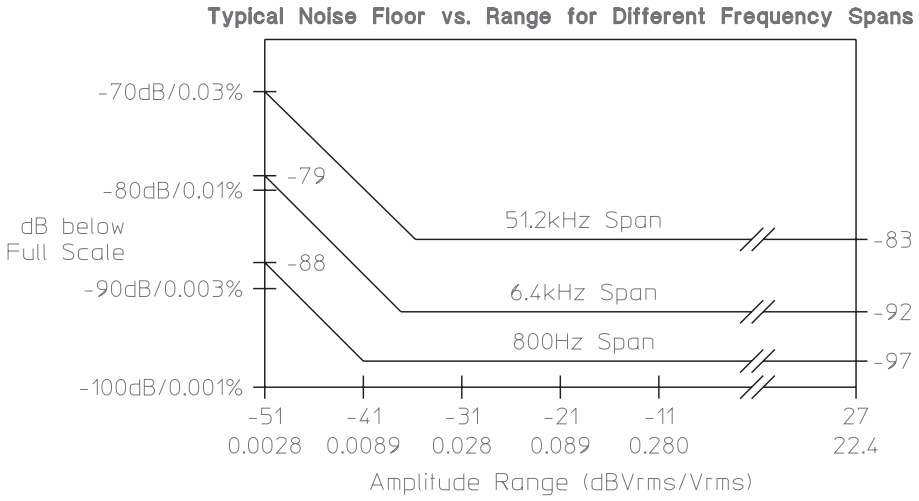
Single Channel Amplitude

Absolute amplitude accuracy (FFT) (A combination of full scale accuracy, full scale flatness, and amplitude linearity.)	±2.92% (0.25 dB) of reading ±0.025% of full scale
FFT full scale accuracy at 1 kHz (0 dBfs)	±0.15 dB (1.74%)
FFT full scale flatness (0 dBfs) relative to 1 kHz	±0.2 dB (2.33%)
FFT amplitude linearity at 1 kHz Measured on +27 dBVrms range with time average, 0 to –80 dBfs.	±0.58% (0.05 dB) of reading ±0.025% of full scale
Amplitude resolution (16 bits less 2 dB over-range) with averaging	0.0019% of full scale (typical)
Residual dc response FFT mode frequency display (excludes A-weight filter)	<–30 dBfs or 0.5 mVdc (whichever is greater)

FFT Dynamic Range

Spurious free dynamic range (Includes spurs, harmonic distortion, intermodulation distortion, alias products) Excludes alias responses at extremes of span. Source impedance = 50 Ω	<–80 dBfs (90 dB typical)

FFT noise floor (typical)
Flat top window, 64 RMS averages



Harmonic distortion Single tone (in band), ≤0 dBfs	<–80 dBfs
Post-filter harmonic distortion (alias responses) of a single tone ≤102.4 kHz, ≤0 dBfs	<–80 dBfs
Intermodulation distortion Two tones (in-band), each ≤–6.02 dBfs	<–80 dBfs
Spurious and residual responses Source impedance = 50 Ω	<–80 dBfs
Frequency alias responses Single tone (out of displayed range), ≤0 dBfs, ≤1 MHz (≤200 kHz with ICP on) 2.5% to 97.5% of the frequency span Lower and upper 2.5% of frequency span	 <–80 dBfs <–65 dBfs

Input Noise

Input noise level
Flat top window, −51 dBVrms range, source impedance = 50 Ω, 32 rms averages

Above 1280 Hz	<–140 dBVrms/√Hz
160 Hz to 1.28 kHz (6.4 kHz span)	<–130 dBVrms/√Hz< % 0 >

Note: To calculate noise as dB below full scale:
Noise [dBfs] = Noise [dBVrms/$\sqrt{Hz}$] + 10LOG(NEBW) – Range [dBVrms].
See ''Window Parameters,'' below, for noise equivalent bandwidths (NEBW).

Window Parameters

	Uniform	Hann	Flat Top
–3 dB bandwidth †	0.125% of span	0.185% of span	0.450% of span
Noise equivalent bandwidth †	0.125% of span	0.1875% of span	0.4775% of span
Attenuation at ± 1/2 bin	4.0 dB	1.5 dB	0.01 dB
Shape factor (–60 dB BW/–3 dB BW)	716	9.1	2.6

† For 800 line displays. With 400, 200, or 100 line displays, multiply bandwidths by 2, 4, and 8, respectively. With 1600 line displays (only available in 1 or 2 channel mode), divide bandwidths by 2.

Single Channel Phase

Phase accuracy relative to external trigger 16 RMS averages, center of bin, dc coupled, 0 dBfs to –50 dBfs, 0 Hz < freq ≤ 10.24 kHz only	±4.0 degree

For Hann and flat top windows, phase is referenced to a cosine wave at the center of the time record. For the uniform, force, and exponential windows, phase is referenced to a cosine wave at the beginning of the time record.

Cross Channel Amplitude

FFT cross channel gain accuracy
Frequency response mode, same amplitude range
(AC coupled, Peroidic Chirp, Uniform Window, < =4Hz)

At full scale: Tested with 10 rms averages on the −11 to +27 dBvrms ranges, and 100 rms averages on the −51 dBVrms range	±0.04 dB (0.46%)
At −20 dBfs: Tested with 200 rms averages on the −11 to +27 dBVrms ranges, and 2000 rms averages on the −51 dBVrms range	±0.08 dB (0.92%)

Cross Channel Phase

Cross channel phase accuracy (same conditions as cross-channel amplitude)	±0.5 degree

Input

Input ranges (full scale) (auto-range capability)	+27 dBVrms (31.7 Vpk) to –51 dBVrms (3.99 mVpk) in 2 dB steps
Maximum input levels	42 Vpk
Input impedance	1 MΩ ±10%, 90 pF nominal
Low side to chassis impedance	
Floating mode Grounded mode	1 MΩ ±30%, <0.010 µF (typical) ≤100 Ω
AC coupling rolloff	<3 dB rolloff at 1 Hz
Common mode rejection ratio Single tone at or below 1 kHz	
–51 dBVrms to –11 dBVrms ranges –9 dBVrms to +9 dBVrms ranges +11 dBVrms to +27 dBVrms ranges	>75 dB typical >60 dB typical >40 dB typical
Note: CM dBfs = CM signal input [dBVrms] – CMRR [dB] – range [dBVrms]	
Common mode range (floating mode)	±4 Vpk
Amplitude over-range detection	+3 dB typical
ICP signal conditioning	
Current source Open circuit voltage	4.25 ±1.5 mA +26 to +32 Vdc
A-weight filter Conforms to ANSI Standard S1.4-1983; and to IEC 651-1979; 10 Hz to 25.6 kHz	Type 0 Tolerance
Crosstalk Between input channels, and source-to-input (receiving channel source impedance = 50 Ω)	<–135 dB below signal or <–80 dBfs of receiving channel, whichever response is greater in amplitude

Time Domain

Specifications apply in histogram/time mode, unfiltered time display	
DC amplitude accuracy	±5.0 % fs
Rise time of –1 V to 0 V test pulse	<11.4 ms
Settling time of –1 V to 0 V test pulse	<16 ms to 1%
Pulse aberrations (peak overshoot) of –1 V to 0 V test pulse Peak aberration relative to the mode-to-mode difference (most common values)	<3 %
Sampling period	
1 channel mode 2 channel mode 4 channel mode (option AY6 only)	3.815 ms (1/262144 Hz) to 2 s in 2× steps 7.629 ms (1/131072 Hz) to 4 s in 2× steps 15.26 ms (1/65536 Hz) to 8 s in 2× steps

Trigger

Trigger modes	Internal trigger External trigger Source trigger GPIB trigger
Maximum trigger delay	
Post trigger Pre trigger No two channels can be further than ±7168 samples from each other.	8191 seconds 8191 sample periods
External trigger maximum input	±42 Vpk
External trigger range	
Low range High range	–2 V to +2 V –10 V to +10 V
External trigger resolution	
Low range High range	15.7 mV 78 mV

Tachometer

Pulses per revolution	0.5 to 2048
RPM accuracy	±100 ppm (0.01%) (typical)
Tachometer level range	
Low range High range	–4 V to +4 V –20 V to +20 V
Tachometer level resolution	
Low range High range	100 mV 500 mV
Tachometer level accuracy (as a % of tachometer range setting)	±10% of range
Maximum tachometer input level	±42 Vpk
Minimum tachometer pulse width	600 ns
Maximum tachometer pulse rate	400 kHz

Source Output

Source types	Sine, random noise, chirp, pink noise, burst random, burst chirp
Amplitude range	ac: ±5 V peak † dc: ±10 V † † Vac_{pk} + |Vdc| ≤10 V
AC amplitude resolution	
Voltage ≥ 0.2 Vrms Voltage < 0.2 Vrms	2.5 mVpk 0.25 mVpk
DC offset accuracy	±15 mV±3% of (|Vdc| +Vac_{pk}) settings
Pink noise adder	Add 600 mV typical when using pink noise
Output impedance	< 5 Ω
Maximum loading	
Current Capacitance	±20 mA peak 0.01 mF
Sine amplitude accuracy at 1 kHz Rload >250 Ω 0.1 Vpk to 5 Vpk	±4% (0.34 dB) of setting
Sine flatness (relative to 1 kHz) 0.1 V to 5 V peak, 0 Hz to 102.4 kHz	±1 dB
Harmonic and sub-harmonic distortion and spurious signals (in band) 0.1 Vpk to 5 Vpk sine wave	
Fundamental <30 kHz Fundamental ≥30 kHz	<–60 dBc <–40 dBc

Digital Interfaces

External keyboard	Compatible with PC-style 101-key keyboard model number HP C1405A (#ABA) (DIN connector) and HP keyboard cable part number 5081-2249.
GPIB	Conforms to the following standards: IEEE 488.1 (SH1, AH1, T6, TEO, L4, LE0, RS1, RL1, PP0, DC1, DT1, C1, C2, C3, C12, E2) IEEE 488.2-1987 Complies with SCPI 1992 Factory set address: 11
Data transfer rate (REAL 64 Format)	<45 ms for a 401 point trace
Serial port (printing, plotting)	300 baud to 9600 baud
Parallel port (printing, plotting)	

General Specifications

Safety Standards	IEC61010-1:2001/EN61010-1:2001 (2nd Edition) Canada: CAN/CSA-C22.2 No. 61010.1-2004 USA: ANSI/UL 61010-1:2004
EMC Standards	Canada: ICES-001:2004 IEC 61326-1:2005/EN61326-1:2006 Australia/New Zealand: AS/NZS CISPR11:2004
Acoustics	LpA <55 dB (cooling fan at high speed setting) LpA <45 dB (auto speed setting at 25 °C)

Fan speed setting of high, automatic, and off are available. The fan off setting can be enabled for a short period of time, except at higher ambient temperatures where the fan will stay on.

Environmental Operating Restrictions	Operating: Disk in Drive	Operating: No Disk in Drive	Storage and Transport
Ambient Temperature	4 °C to 45 °C	0 °C to 55 °C	–40 °C to 70 °C
Relative Humidity (non-condensing)			
Minimum	20%	15%	5%
Maximum	80% at 32 °C	95% at 40 °C	95% at 50 °C
Vibration (5 – 500 Hz)	0.6 Grms	2.1 Grms	3.41 Grms
Shock	5 G (10 ms 1/2 sine)	5 G (10 ms 1/2 sine)	40 G (3 ms 1/2 sine)
Maximum Altitude	4600 meters (15,000 feet)		
AC Power	100 Vrms to 240 Vrms (47 Hz to 440 Hz) 350 VA maximum		
DC Power	12 Vdc to 28 Vdc nominal 200 VA maximum		
DC Current at 12V (typical)	10 A (standard) 12 A (4 Channel, Option AY6)		
Warm-Up Time	15 minutes		
Weight	15 kg (33 lbs) net 29 kg (64 lbs) shipping		
Dimensions (excluding bail handle and impact cover)	Height: 190 mm (7.5 in) Width: 340 mm (13.4 in) Depth: 465 mm (18.3 in)		

IEC 801-3 (Radiated Immunity): Performance degradation may occur at Security Level 2.

Order Tracking — Option 1D0

$$\frac{Max\ Order \times Max\ RPM}{60} \leq$$

Real time (online)	
1 channel mode	25,600 Hz
2 channel mode	12,800 Hz
4 channel mode	6,400 Hz
Capture playback †	
1 channel mode	102,400 Hz
2 channel mode	51,200 Hz
4 channel mode	25,600 Hz

Specified for
5 ≤ RPM ≤ 60,000 (online), 5 ≤ RPM ≤ 491,519 (capture playback); and
number of orders ≤ 200

† Signals are captured online and then postprocessed in capture playback mode.

Delta order	1/128 to 1/1
Resolution (maximum order)/(delta order)	≤200
Maximum RPM ramp rate 1000 to 10,000 RPM run up maximum order = 10 delta order = 0.1 RPM step = 30 (1 channel) = 60 (2 channel) = 120 (4 channel)	750 RPM/second (typical for real time)
Order track amplitude accuracy	±1 dB (typical)

Swept Sine Measurements —Option 1D2

Dynamic range Default span: 51.2 Hz to 51.2 kHz Fast average ON, 101 point log sweep Tested with 11 dBVrms source level at 100 ms integration (approximately 60 second sweep)	130 dB typical

Arbitrary Waveform Source—Option 1D4

Amplitude Range	Arb: ±5 Vpk † dc: ±10 V † † V_{pk} +|Vdc| ≤10 V
Record Length Depends on measurement resolution (100, 200, 400, 800, and 1600 lines)	# of points = 2.56 x lines of resolution, or # of complex points = 1.28 x lines of resolution
Point spacing	Matches the measurement sample rate.
DAC Resolution	
0.2828 Vpk to 5 Vpk <0.2828 Vpk	2.5 mV 0.25 mV

Real Time Octave Analysis — Option 1D1

Standards	Conforms to ANSI Standard S1.11 - 1986, Order 3, Type 1-D, Extended and Optional Frequency Ranges Conforms to IEC 651-1979 Type 0 Impulse, and ANSI S1.4

Frequency ranges (at centers)

Online (real time)

	1 channel	2 channel	4 channel
1/1 octave	0.063 Hz to 16 kHz	0.063 Hz to 8 kHz	0.063 Hz to 4 kHz
1/3 octave	0.08 Hz to 40 kHz	0.08 Hz to 20 kHz	0.08 Hz to 10 kHz
1/12 octave	0.0997 Hz to 12.338 kHz	0.0997 Hz to 6.169 kHz	0.0997 Hz to 3.084 kHz

Capture playback

	1 channel	2 channel	4 channel
1/1 octave	0.063 Hz to 16 kHz	0.063 Hz to 16 kHz	0.063 Hz to 16 kHz
1/3 octave	0.08 Hz to 31.5 kHz	0.08 Hz to 31.5 kHz	0.08 Hz to 31.5 kHz
1/12 octave	0.0997 Hz to 49.35 kHz	0.0997 Hz to 49.35 kHz	0.0997 Hz to 49.35 kHz

1 to 12 octaves can be measured and displayed.

1/1, 1/3, and 1/12 octave true center frequencies related by the formula:

$$\frac{f(i+1)}{f(i)} = 2^{1/n}; n = 1,\ 3 \text{ or } 12;$$

Where 1000 Hz is the reference for 1/1, 1/3 octave, and 1000 x$2^{(1/24)}$Hz is the reference for 1/12 octave. The marker returns the ANSI standard preferred frequencies.

Accuracy 1 second stable average single tone at band center	±0.2 dB

Readings are taken from the linear total power spectrum bin. It is derived from sum of each filter.

1/3 octave dynamic range 2 second stable average, limited by input noise level	>80 dB (typical) per ANSI S1.11 - 1986

Recommended Test Equipment

The following table lists the recommended equipment needed to test the performance of the Agilent 35670A Dynamic Signal Analyzer. The table on page 1-20 lists additional equipment needed to adjust and troubleshoot the analyzer. Other equipment may be substituted for the recommended model if it meets or exceeds the listed critical specifications. When substitutions are made, you may have to modify the procedures to accommodate the different operating characteristics.

Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model
AC Calibrator	10 Hz to 102.4 kHz; 1 mV to 10 V Amplitude Amplitude Accuracy: ±0.1% phase locking capability	Fluke 5700A † Alternate Fluke 5200A † Datron 4200, 4700, or 4708 ‡ HP 745A
Frequency Synthesizer	Frequency Range: 10 Hz to 1 MHz Frequency Accuracy: ≤5 ppm Amplitude Accuracy: 0.2 dB from 1 Hz to 100 kHz 1 dB from 100 kHz to 1 MHz Harmonic Distortion: ≤–70 dBc Spurious: ≤–70 dBc <±1 deg phase shift between output and sync	HP 3326A Alternate (2) HP 3325A/B Opt 001
Low Distortion Oscillator	Frequency Range: 10 Hz to 100 kHz Harmonic Distortion: ≤–93 dB, 10 Hz to 20 kHz	HP 339A †† Alternate HP 3326A with notch filter †† HP 3325A/B with notch filter††
Digital Multimeter	5 1/2 digit True rms ac Voltage: 30 Hz to 100 kHz; 0.1 to 500 V; ±0.1%; ≥1 MΩ input impedance dc Voltage: 1 V to 300 V; ±0.1%	HP 3458A Alternate HP 3456A , HP 3455A HP 3478A
Feedthrough Termination (2) (4 for option AY6)	50 Ω: ±2% at dc	Pomona Elect Model 4119-50 ‡‡ Alternate HP 11048C, HP 10100C

† John Fluke Manufacturing Co., Inc., PO Box C9090, Everett, WA 98206 U.S.A. (206) 347-6100
‡ Wavetek, 5808 Churchman Bypass, Indianapolis, IN 46203 U.S.A.
†† This equipment is not required for Operation Verification. The parts and schematic for the notch filter are shown on page 1-19.
‡‡ ITT Pomona Electronics, 1500 East Ninth Street, Pomona, CA 91769 U.S.A. (714) 469-2900 FAX (206) 629-3317

Recommended Test Equipment (continued)

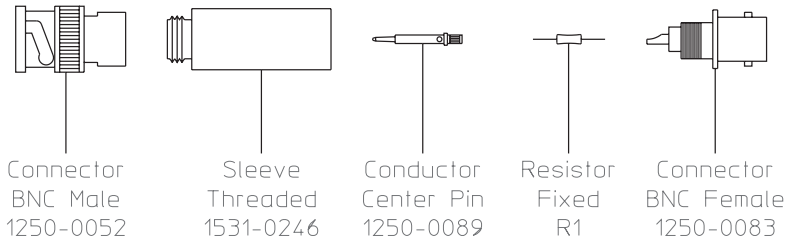
Instrument	Critical Specifications	Recommended Model
Cables	BNC-to-Dual Banana (6) BNC-to-BNC 30 cm BNC-to-BNC 122 cm	HP 11001-60001 HP 8120-1838 HP 8120-1840
Adapters	BNC(m)-to-Dual Banana Plug BNC(f)-to-Dual Banana Plug BNC(f)-to-BNC (f) (4) BNC Tee (m)(f)(f)	HP 10110B HP 1251-2277 HP 1250-0080 HP 1250-0781
Resistor (2)†	Value: 1 kΩ Accuracy: 1% Power: 0.25W	HP 0757-0280

† See the following for suggested assembly.

Suggested Assembly for Series Resistor

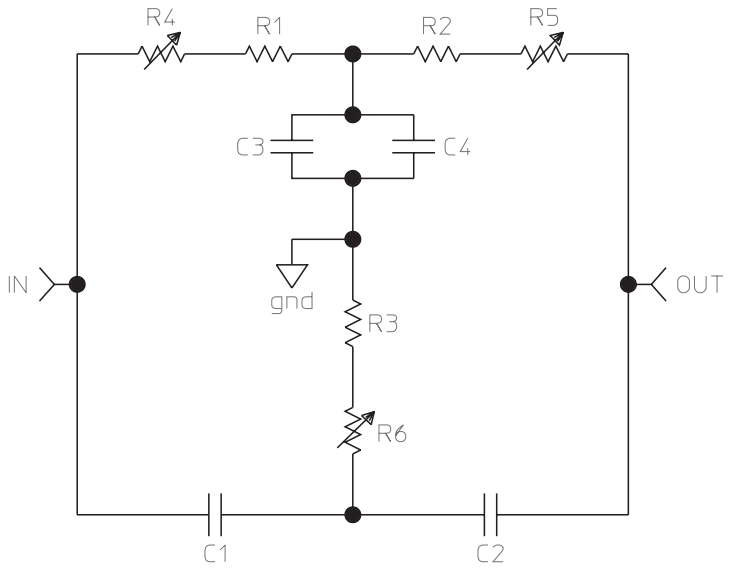
The following is a suggested assembly for the 1 kΩ series resistor. Two 1 kΩ series resistors are required for the Intermodulation Distortion performance test.

- **Cut resistor leads to 12 mm on each end.**
- **Solder one resistor lead to the center conductor of the BNC female connector.**
- **Solder the conductor center pin to the other lead of the resistor.**
- **Screw the sleeve and the BNC male connector into place. Tighten securely.**



Schematic and Parts List for Notch Filter

The Harmonic Distortion performance test requires either an HP 339A or an HP 3326A or HP 3325A/B with notch filter. The following shows the schematic and parts list for the notch filter.



Reference	Description	Agilent Part Number
C1 - C4	0.025 µF ±2.5%, 100 V polypropelene-metalized	HP 0160-6809
R1 - R2	249 Ω ±1% metal film, 0.125 W	HP 0698-4421
R3	118 Ω ±1% metal film, 0.125 W	HP 0698-4407
R4 - R6	20 Ω trimmer, 1 turn	HP 2100-3409

Additional Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model
Frequency Counter	Frequency Range: 0 Hz to 100 MHz Frequency Accuracy: 7.5 ppm or better at 20 MHz	HP 5350B Alternate HP 5351B, HP 5335A
Oscilloscope	Bandwidth: >50 MHz Two Channel; External Trigger; 1 MΩ Input	HP 54111D Alternate HP 1980B, HP 1740
Oscilloscope Probe	Impedance: ≥1 MΩ Division Ratio: 10:1 Maximum Voltage: ≥20 Vdc	HP 10431A
Oscilloscope Probe	Impedance: ≥ 1 MΩ Division Ratio: 1:1	HP 10438A
Spectrum Analyzer	Frequency Range: 10 Hz to 100 kHz Dynamic Range: ≥70 dB	HP 3562A Alternate HP 3561A, HP 3585A/B
Logic Probe	TTL	HP 545A Alternate HP 5006A, HP5005A/B
Patch Cord	Minigrabber test clips	Pomona 3781-8-7
Cable	BNC(m)-to-SMB(f)	HP 03585-61616
Adapter	SMB(m)-to-SMB(m)	HP 1250-0669

2

Preparing the Analyzer for Use

Preparing the Analyzer for Use

This chapter contains instructions for inspecting and installing the Agilent 35670A Dynamic Signal Analyzer. This chapter also includes instructions for cleaning the screen, transporting and storing the analyzer.

DC Power Requirements

The analyzer can operate from a dc power source supplying a true range of 10.8 to 30.8 Vdc. With all options installed, power consumption is less than 200 VA. The following table shows typical current requirements at different operating voltages for the standard two-channel analyzer and for the optional four-channel analyzer.

Operating Voltage	**Typical Current**	
	Standard 2 channel Agilent 35670A	Optional 4 channel Agilent 35670A
12 Vdc	8.0 amps	11.0 amps
24 Vdc	4.0 amps	5.5 amps

AC Power Requirements

The analyzer can operate from a 47 to 440 Hz, single-phase, ac power source supplying 90 to 264 Vrms. With all options installed, power consumption is less than 350 VA.

Warning **Only a qualified service person, aware of the hazards involved, should measure the line voltage.**

DC Power Cable and Grounding Requirements

The negative side of the dc input connector is not connected to chassis ground. In dc mode operation, the chassis will float. The chassis ground lug on the rear panel and the negative side of the dc input connector should both be connected to a known reference potential.

Two dc power cables are available—the HP 35250A dc power cable and the HP 35251A dc power cable with cigarette lighter adapter. Both cables contain a 30 amp, 32 volt fuse (HP 2110-0920).

Warning **The tip of the cigarette lighter adapter may get hot during use. After unpluging the adapter, be careful of the heat from the adapter's tip.**

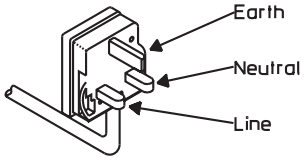
Caution Although shorter cables may reduce dc voltage loss, use the standard cables. The dc inrush current may pit the connector contacts in shorter cables.

AC Power Cable and Grounding Requirements

On the GPIB connector, pin 12 and pins 18 through 24 are tied to chassis ground and the GPIB cable shield. The instrument frame, chassis, and covers are connected to chassis ground. The input BNCs are floating unless ground mode is selected.

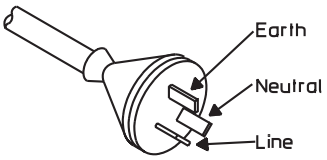
The analyzer is equipped with a three-conductor power cord that grounds the analyzer when plugged into an appropriate receptacle. The type of power cable plug shipped with each analyzer depends on the country of destination. The following figure shows available power cables and plug configurations.

United Kingdom
Option 900



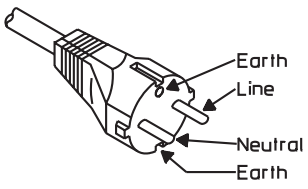
PLUG*: BS 1363A
CABLE*: HP 8120-1703
220V-5A
OPERATION

Australia/New Zealand
Option 901



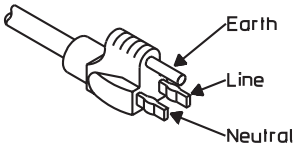
PLUG*: NZSS 198/AS C112
CABLE*: HP 8120-0696
220V-6A
OPERATION

Continental Europe
Option 902



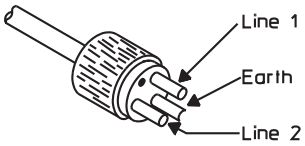
PLUG*: CEE7-V11
CABLE*: HP 8120-1692
220V-6A
OPERATION

North America
Option 903



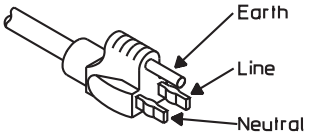
PLUG*: NEMA 5-15P
CABLE*: HP 8120-1521
125V-10A**
OPERATION

North America
Option 904



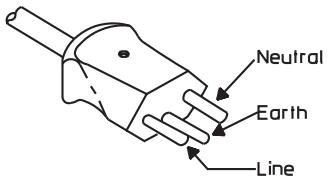
PLUG*: NEMA-G-15P
CABLE*: HP 8120-0698
250V-6A**
OPERATION

Japan
Option 918



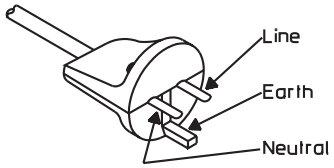
PLUG*: MITI 41-9692
CABLE*: HP 8120-4754
125V-12A
OPERATION

Switzerland
Option 906



PLUG*: SEV 1011.1959-24507
TYPE 12
CABLE*: HP 8120-2296
220V-6A
OPERATION

Denmark
Option 912



PLUG*: DHCR 107
CABLE*: HP 8120-2957
220V-6A
OPERATION

*The number shown for the plug is the industry identifier for the plug only, the number shown for the cable is an HP part number for a complete cable including the plug.

**UL listed for use in the United States of America.

Warning **The power cable plug must be inserted into an outlet provided with a protective earth terminal. Defeating the protection of the grounded analyzer cabinet can subject the operator to lethal voltages.**

To do the incoming inspection

The Agilent 35670A Dynamic Signal Analyzer was carefully inspected both mechanically and electrically before shipment. It should be free of marks or scratches, and it should meet its published specifications upon receipt.

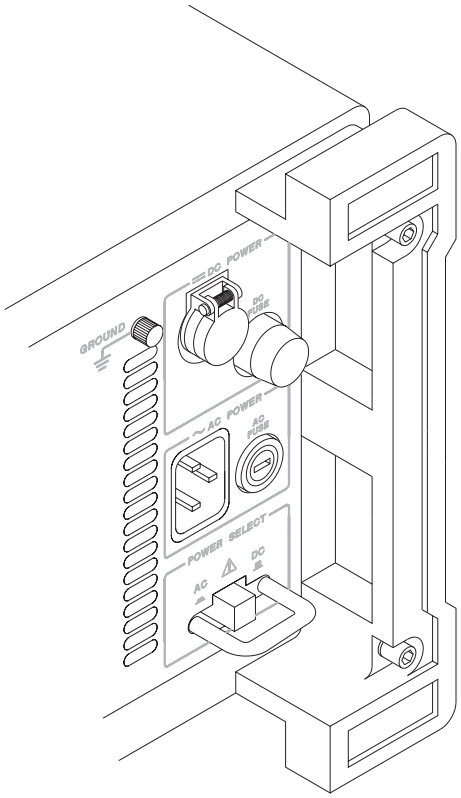
- **Inspect the analyzer for physical damage incurred in transit. If the analyzer was damaged in transit, do the following:**
- Save all packing materials.
- File a claim with the carrier.
- Call your Agilent Technologies sales and service office.

Warning

If the analyzer is mechanically damaged, the integrity of the protective earth ground may be interrupted. Do not connect the analyzer to power if it is damaged.

- **Check that the POWER SELECT switch on the analyzer's rear panel is set to the AC position.**

The switch is in the AC position when in the ''in'' position.



- **Check that the correct fuses are installed in the fuse holders.**

An 8 amp, 250 volt, normal blow fuse is required for ac operation. A 30 amp, 32 volt, normal blow fuse is required for dc operation. Both fuses are installed at the factory. For instructions on removing the fuses or fuse part numbers, see ''To change the fuses.''

- **Using the supplied power cord, connect the analyzer to an appropriate receptacle.**

The analyzer is shipped with a three-conductor power cord that grounds the analyzer when plugged into an appropriate receptacle. The type of power cable plug shipped with each analyzer depends on the country of destination.

- **Set the analyzer's power switch to on.**

Press the switch located on the analyzer's lower left-hand corner. The switch is in the on (|) position when in the ''in'' position. The analyzer requires about 20 seconds to complete its power-on routine.

- **Test the electrical performance of the analyzer using the operation verification or the performance tests in chapter 3, ''Verifying Specifications.''**

The operation verification tests verify the basic operating integrity of the analyzer; these tests take about 1 ½ hours to complete and are a subset of the performance tests. The performance tests verify that the analyzer meets all the performance specifications; these tests take about 2 ½ hours to complete.

To install the analyzer

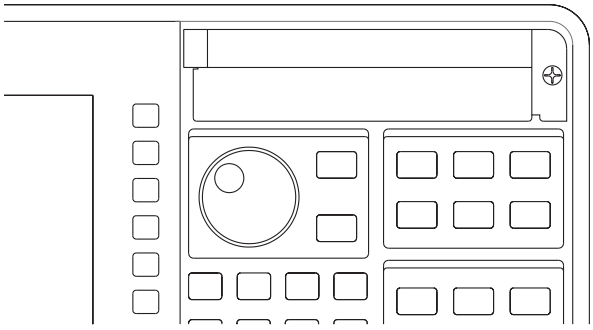
The analyzer is shipped with rubber feet and bail handle in place, ready for use as a portable or bench analyzer.

- Install the analyzer to allow free circulation of cooling air.
  Cooling air enters the analyzer through the right side and exhausts through the left side and rear panel.
- To install the analyzer in an equipment cabinet, follow the instructions shipped with the rack mount kit.

Warning **To prevent potential fire or shock hazard, do not expose the analyzer to rain or other excessive moisture.**

- Protect the analyzer from moisture and temperatures or temperature changes that cause condensation within the analyzer.
  The operating environment specifications for the analyzer are listed in chapter 1, ''Specifications.''
- Protect the analyzer's disk drive from dirt and dust.
  Remove the screw to the right of the disk drive and use it to attach the supplied disk drive cover. The disk drive cover is located inside the front-panel impact cover.

Caution Use of the equipment in an environment containing dirt, dust, or corrosive substances will drastically reduce the life of the disk drive and the flexible disks. To minimize damage, use the disk drive cover and store the flexible disks in a dry, static-free environment.



To connect the analyzer to a dc power source

In applications requiring a portable dc power source, use a properly protected dc power system. The dc system should contain a deep cycle battery rather than a standard automobile battery. A standard automobile battery will fail prematurely if repeatedly discharged. Also, select a battery that provides the best compromise between operation time and portability.

- **Set the analyzer's power switch to off (O).**
- **Set the analyzer's POWER SELECT switch to the DC position.**

The switch is in the DC position when in the ''out'' position.

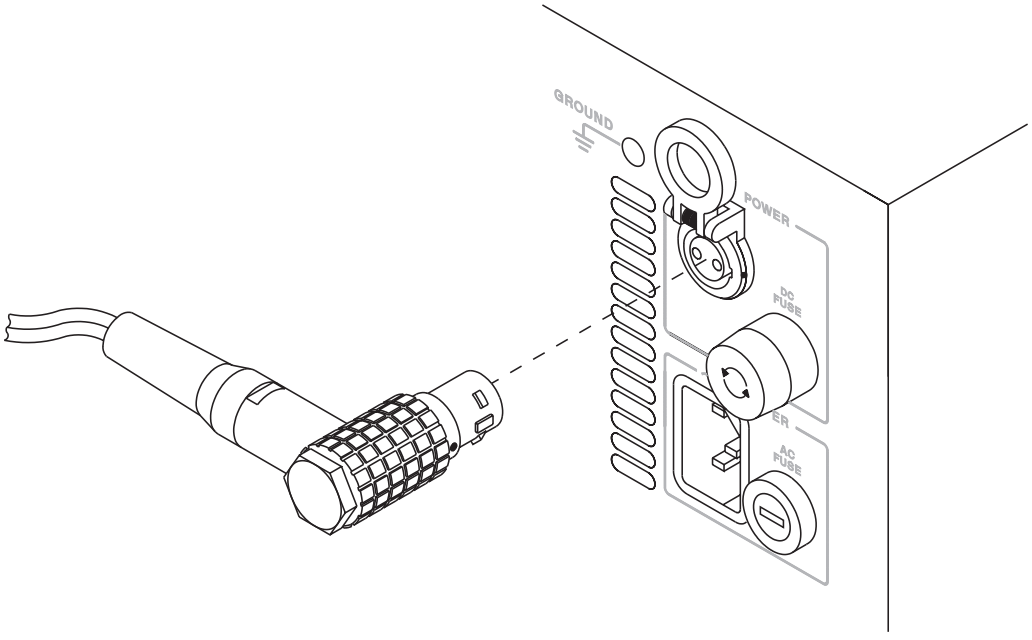
- **Connect the dc power cable to the dc power source.**

Using the dc power cable (HP 35250A), attach the black cable to the common terminal and the red cable to the positive terminal of the dc power source. Using the dc power cable with cigarette lighter adapter (HP 35251A), plug the cigarette lighter adapter into an automotive cigarette lighter receptacle.

- **Connect the analyzer's ground terminal to the same reference potential as the common terminal of the dc power source.**

Using a wire, connect the analyzer's GROUND terminal to the common terminal of the dc source. If you are using the dc power cable with cigarette lighter adapter, connect the GROUND terminal to the automobile chassis.

- **Plug the dc power cable into the analyzer's DC POWER receptacle. Make sure to align the red dot on the plug with the red dot on the receptacle.**



- **Turn on the dc power source.**

If the dc power source is supplied by an automobile, start the automobile. The automobile must be running to provide adequate dc power.

Warning **The tip of the cigarette lighter adapter may get hot during use. After unpluging the adapter, be careful of the heat from the adapter's tip.**

- **Set the analyzer's power switch to on (|).**

If the analyzer will not power up or operates intermittently on dc power, see ''If the analyzer will not power up'' or ''If the analyzer operates intermittently on dc power'' at the end of this chapter.

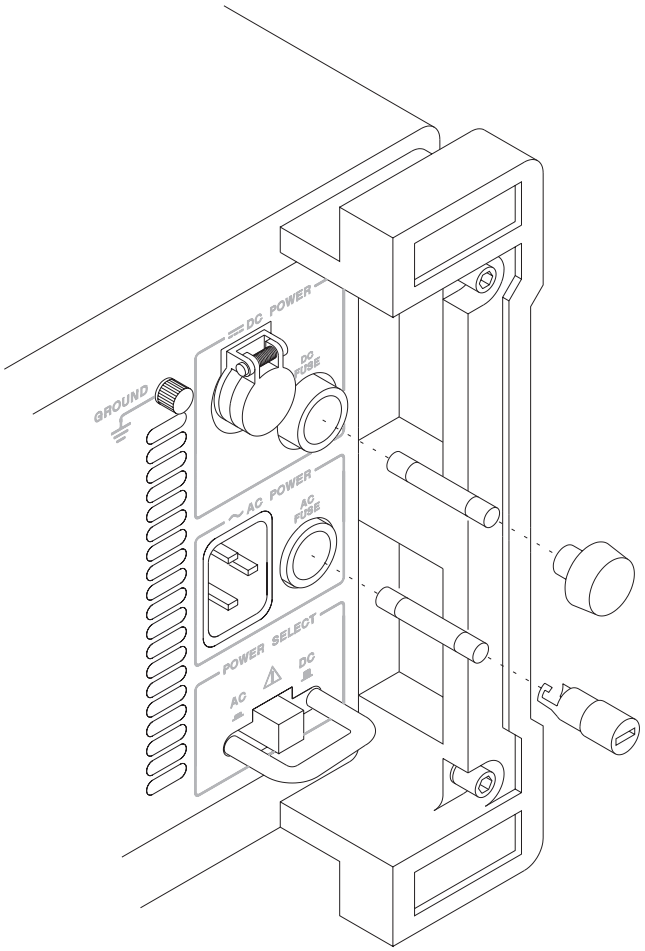
To change the fuses

Both fuses are installed at the factory.

- **Unplug the power cord from the analyzer.**
- **Press in and turn the appropriate fuse holder cap counter-clockwise (use a small screw driver for the ac fuse). Remove when the fuse cap is free from the housing.**
- **Pull the fuse from the fuse holder cap.**
- **To reinstall, select the proper fuse and place in the fuse holder cap.**

DC Fuse	AC Fuse
HP 2110-0920 30 A 32 V Normal Blow	HP 2110-0342 8 A 250 V Normal Blow

- **Place the fuse holder cap in the housing. Press in and turn clockwise.**



To connect the analyzer to a serial device

The Serial Port is a 9-pin, EIA-574 port that is only available using option 1C2, Instrument Basic. The total allowable transmission path length is 50 feet.

- Connect the analyzer's rear panel SERIAL PORT to a serial device using a 9-pin female to 25-pin RS-232-C cable.

Part Number	Cable Description
HP 24542G	9-pin female to 25-pin male RS-232
HP 24542H	9-pin female to 25-pin female RS-232

For additional information, see chapter 9 in the *Agilent 35670A Service Guide*.

To connect the analyzer to a parallel device

The Parallel Port is a 25-pin, Centronics port. The Parallel Port can interface with PCL printers or HP-GL plotters.

- Connect the analyzer's rear panel PARALLEL PORT connector to a plotter or printer using a Centronics interface cable.

Part Number	Cable Description
HP 92284A	25-pin male to 36-pin male 2-meter Centronics
HP C2912B	25-pin male to 36-pin male 3-meter Centronics

For additional information, see chapter 9 in the *Agilent 35670A Service Guide*.

To connect the analyzer to an GPIB device

The analyzer is compatible with the Agilent Technologies Interface Bus (GPIB). The GPIB is Agilent Technologies's implementation of IEEE Standard 488.1. Total allowable transmission path length is 2 meters times the number of devices or 20 meters, whichever is less. Operating distances can be extended using an GPIB Extender.

GPIB peripherals include HP-GL plotters, PCL printers, and SS-80 external disks.

- **Connect the analyzer's rear panel GPIB connector to an GPIB device using an GPIB interface cable.**

Caution

The analyzer contains metric threaded GPIB cable mounting studs as opposed to English threads. Use only metric threaded GPIB cable lockscrews to secure the cable to the analyzer. Metric threaded fasteners are black, while English threaded fasteners are silver.

For GPIB programming information, see the *Agilent 35670A GPIB Programming Reference*.

To connect the analyzer to an external monitor

The External Monitor connector is a 9-pin D female miniature connector that can interface with an external, multisync monitor. The monitor must be compatible with the 24.8 kHz line rate, 55 Hz frame rate, and TTL signals provided by the Agilent 35670A. A SONY CPD-1302 monitor and a NEC Multisync 3D monitor with EZPIXpc† driver has been checked and found compatible with the Agilent 35670A external monitor mode operation.

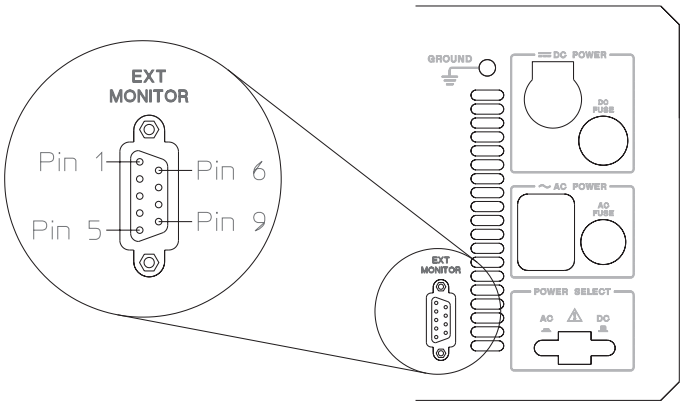
- **Set the analyzer's power switch to on (|).**
- **Set the monitor's power switch to on and configure the input and timing mode if necessary.**

See the manual supplied with the monitor for information on configuring the monitor's input and timing mode.

- **Connect the external monitor's input cable to the analyzer's rear panel EXT MONITOR connector.**

A cable with a 9-pin connector option or an adapter to a 9-pin connector is required to connect the monitor to the Agilent 35670A.

- **Press the following keys to enable external mode:**
  [Disp Format]
  [MORE **]**
  [MORE **]**
  [EXT MON **ON OFF]**



Pin Number	Signal Name	Pin Number	Signal Name
3	R	8	HSYNC
4	G	9	VSYNC
5	B	1, 2, 6	GND

† The EZPIXpc driver converts TTL video signals into RGB analog signals, drives 75 ohm coax cable, provides RGB composite sync or RGB sync on green, for monitors with RGB input capability. EZPIXpc, Covid, Inc., 1725 West 17th St, Tempe, Arizona 85281, 800-638-6104

To connect the optional keyboard

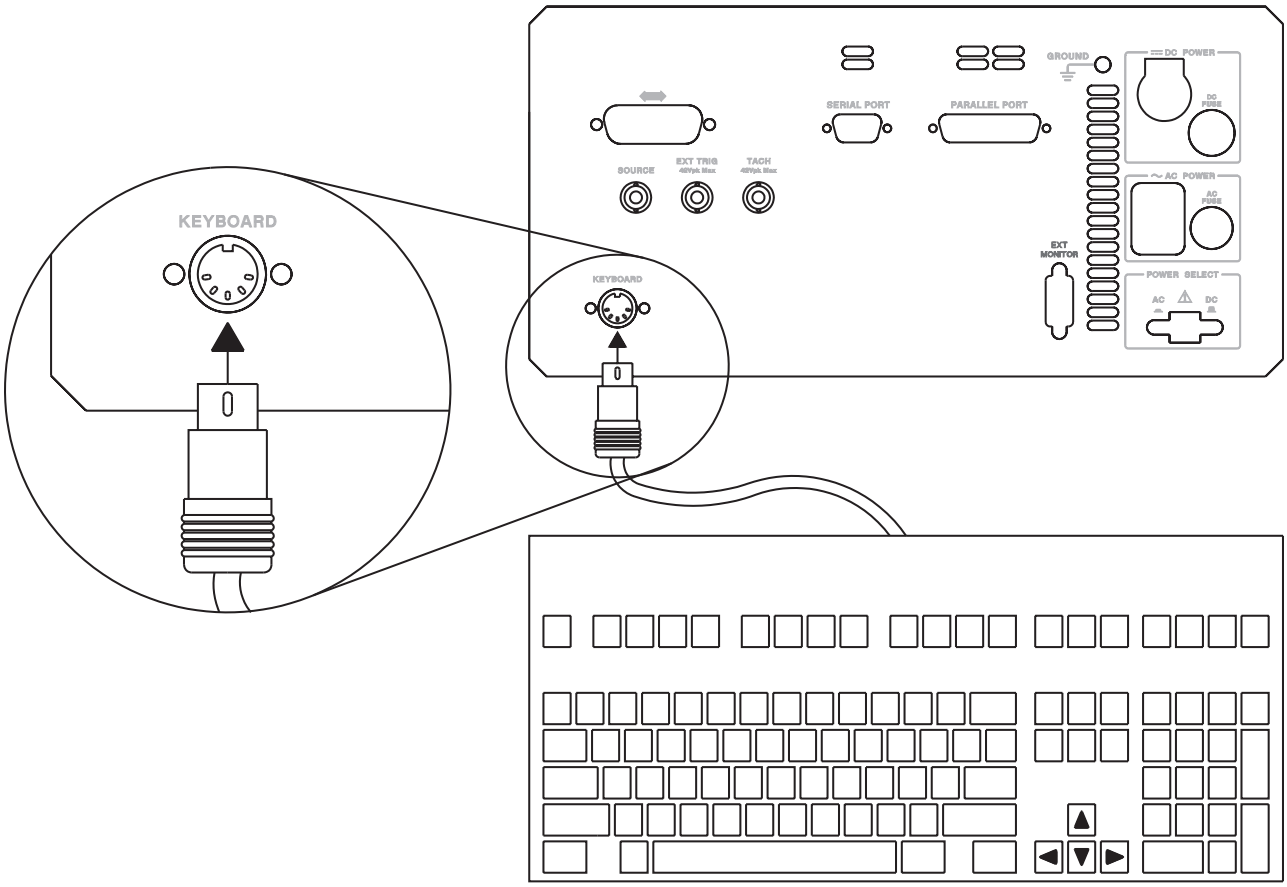
The analyzer may be connected to an optional external keyboard. The keyboard remains active even when the analyzer is not in alpha entry mode. This means that you can operate the analyzer using the external keyboard rather than the front panel. Pressing the appropriate keyboard key does the same thing as pressing a hardkey or a softkey on the analyzer's front panel.

- **Set the power switch to off (O).**

Caution

Do not connect or disconnect the keyboard cable with the line power turned on (I). Connecting or disconnecting the keyboard while power is applied may damage the keyboard or the analyzer.

- **Connect the round plug on the keyboard cable to the KEYBOARD connector on the analyzer's rear panel. Make sure to align the plug with the connector pins.**



- **Connect the other end of the keyboard cable to the keyboard.**

Caution

In addition to the U.S. English keyboard, the Agilent 35670A Dynamic Signal Analyzer supports U.K. English, German, French, Italian, Spanish, and Swedish. Use only the Agilent Technologies approved keyboard for this product. Agilent Technologies does not warrant damage or performance loss caused by a non-approved keyboard. See the beginning of this guide for part numbers of approved Agilent Technologies keyboards.

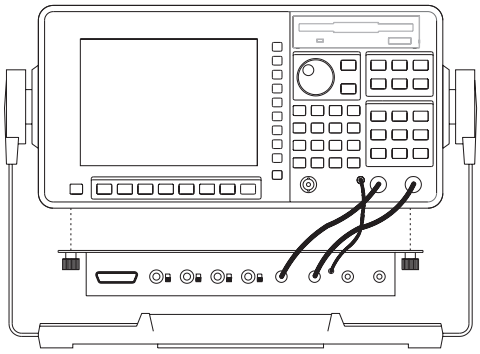
- **To configure your analyzer for a keyboard other than U.S. English, press [** System Utility **] [** KEYBOARD SETUP **]. Then press the appropriate softkey to select the language.**

Configuring your analyzer to use a keyboard other than U.S. English only ensures that the analyzer recognizes the proper keys for that particular keyboard. Configuring your analyzer to use another keyboard *does not* localize the on-screen annotation or the analyzer's online HELP facility.

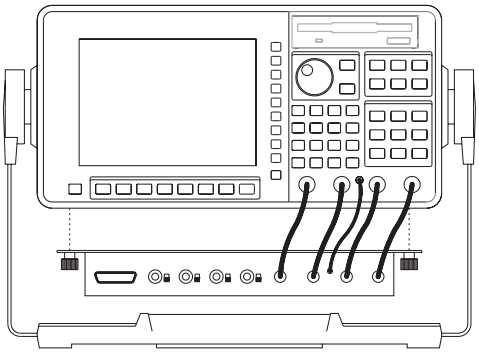
To connect the microphone adapter

The Microphone Adapter and Power Supply (option UK4) simplifies microphone connections. The mic connector on the analyzer's front panel provides 8 Vdc to power the adapter. The adapter's internal power supply uses a step-up converter to provide 28 V and 200 V on the seven-pin input connectors. The 28 V pins power the microphone pre-amplifiers. The 200 V pins polarize the condenser microphone cartridges.

- **Flip the bail handle down to support the front of the analyzer.**
- **Insert the threaded ends of the adapter's two knurled knobs into the standoffs on the bottom of the analyzer's case, then tighten the knobs with your fingers.**
- **Attach the adapter's mic cable to mic connector on the analyzer's front panel.**
- **Connect the adapter's BNCs to the corresponding BNCs on the analyzer's front panel.**



Standard 2 channel Agilent 35670A
Agilent 35670A



Optional 4 channel

To clean the screen

The analyzer's display is covered with a plastic diffuser screen (this is not removable by the operator). Under normal operating conditions, the only cleaning required will be an occasional dusting. However, if a foreign material adheres itself to the screen, do the following:

- **Set the power switch to off (○).**
- **Remove the power cord.**
- **Dampen a soft, lint-free cloth with a mild detergent mixed in water.**
- **Carefully wipe the screen.**

Caution

Do not apply any water mixture directly to the screen or allow moisture to go behind the front panel. Moisture behind the front panel will severely damage the instrument.

To prevent damage to the screen, do not use cleaning solutions other than the above.

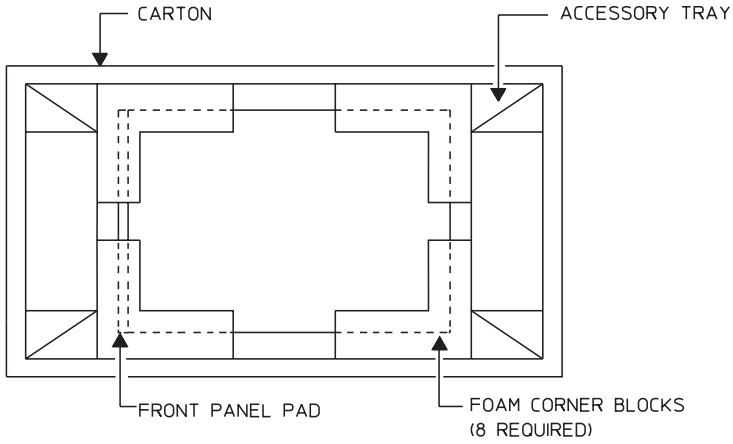
To store the analyzer

- **Store the analyzer in a clean, dry, and static free environment.**
  For other requirements, see environmental specifications in chapter 1, ''Specifications.''

To transport the analyzer

- Package the analyzer using the original factory packaging or packaging identical to the factory packaging.

  Containers and materials identical to those used in factory packaging are available through Agilent Technologies offices.
- If returning the analyzer to Agilent Technologies for service, attach a tag describing the following:
  - Type of service required
  - Return address
  - Model number
  - Full Serial number
  - In any correspondence, refer to the analyzer by model number and full serial number
- Mark the container FRAGILE to ensure careful handling.
- If necessary to package the analyzer in a container other than original packaging, observe the following (use of other packaging is not recommended):
  - Snap the impact cover in place to protect the front panel.
  - Wrap the analyzer in heavy paper or anti-static plastic.
  - Use a double-wall carton made of at least 350-pound test material.
  - Cushion the analyzer to prevent damage.



Caution

Do not use styrene pellets in any shape as packing material for the analyzer. The pellets do not adequately cushion the analyzer and do not prevent the analyzer from shifting in the carton. In addition, the pellets create static electricity which can damage electronic components.

If the analyzer will not power up

- ❑ Check that the power cord is connected to the Agilent 35670A and to a live power source.
- ❑ Check that the front-panel switch is on (|).
- ❑ Check that the rear-panel AC/DC power select switch is properly set.
- ❑ Check that the fuse is good.
  See ''To change the fuses'' on page 2-10.
- ❑ Check that the analyzer's air circulation is not blocked.
  Cooling air enters the analyzer through the right side and exhausts through the left side and rear panel. If the analyzer's air circulation is blocked, the analyzer powers down to prevent damage from excessive temperatures. The analyzer remains off until it cools down and its power switch is set to off (O) then to on (|).
- ❑ Obtain Agilent service, if necessary. See ''Need Assistance?'' at the end of this guide.

If the analyzer operates intermittently on dc power

The analyzer powers down when operating on dc power if no measurement has been made within 30 minutes.

- ❑ Check that the dc power source can supply the required power.

  The dc power source must have a true range of 10.8 to 30.8 Vdc. At the minimum voltage of 10.8 Vdc, the dc power source must be able to supply approximately 8.7 amps for a two-channel analyzer and 12.2 amps for a four-channel analyzer. The voltage loss through an automotive cigarette lighter system can cause the dc voltage to go below 10.8 Vdc.
- ❑ Check that power transients are not causing the dc voltage to go below 10.8 Vdc.

  The dc voltage provided by an automobile is susceptible to power transients. For example, power transients may occur when lights or fans turn on or off, when power door locks engage or disengage, and when windshield wipers operate. If the dc supply voltage falls below 10.8 V, the analyzer automatically turns off. However, the analyzer is not affected by power transients that occur within the range of 10.8 to 30.8 Vdc.
- ❑ Check that the cable connections are not loose.
- ❑ Obtain Agilent service, if necessary. See ‘’Need Assistance?’’ at the end of this guide.

3

Verifying Specifications

Verifying Specifications

This chapter tells you how to use the *Agilent 35670A Semiautomated Performance Test Disk*. The performance test disk contains a program that semiautomates the operation verification tests and performance tests.

After you review this chapter, follow the directions in ''To load the program'' then continue with one of the following:

- ''To run the program in semiautomated mode''
- ''To run the program without a printer''
- ''To run the program in manual mode''

Caution

Before applying line power to the analyzer or testing its electrical performance, see chapter 2, ''Preparing the Analyzer for Use.''

Overview

The *Semiautomated Performance Test Disk* contains a program (ITM_35670A) and two procedure files (OP_VERIFY and PERFORMAN). ITM_35670A is the test manager program. OP_VERIFY is the operation verification procedure file and PERFORMAN is performance test procedure file. The procedure files contain an ordered list of tests, and each test contains one or more measurements. Since ITM_35670A reads the procedure files, the disk must remain in the disk drive during testing.

If you do not have a keyboard connected to the analyzer, use the numeric key pad and the alpha keys when the program prompts you to type in information. See the analyzer's help text for a description of the alpha keys.

If a test fails, contact your local Agilent Technologies sales and service office or have a qualified service technician see chapter 4, ''Troubleshooting the Analyzer,'' in the *Agilent 35670A Service Guide*.

Features of the Program

- The program can automatically create a printout similar to the test records at the back of this chapter.
- The program can beep when equipment connections need to be changed.
- The program can start the test sequence at any test in the operation verification or performance test list.
- The program can stop after each measurement or alternatively, only if a failure occurs.
- The program can be run in manual mode.

Test Duration

In semiautomated mode, the operation verification tests require approximately 1½ hours and the performance tests require approximately 2½ hours.

Calibration Cycle

To verify the Agilent 35670A Dynamic Signal Analyzer is meeting its published specifications, do the performance tests every 12 months.

Recommended Test Equipment

The equipment needed for operation verification and performance tests is listed on page 1-18. Other equipment may be substituted for the recommended model if it meets or exceeds the listed critical specifications.

Also, if you want the test record to be automatically printed, you need an GPIB printer. If you want the printer to automatically leave top and bottom margins on every page, enable perforation skip mode (see your printer's manual for directions). If you do not have an GPIB printer you must record the results of each test in the test records. These test records may be reproduced without written permission of Agilent Technologies.

Program Controlled Test Equipment

This program automatically controls the instruments listed in the following table using GPIB commands. If you use a test instrument other than those shown in the table, the program prompts you to set the instrument state during testing.

Test Equipment	Program Controlled Model
AC Calibrator	Fluke 5700A Alternate Fluke 5200A Datron 4200, 4707, 4708
Frequency Synthesizer	HP 3326A Alternate (2) HP 3325A/B
Digital Multimeter	HP 3458A Alternate HP 3455A HP 3456A HP 3478A

Measurement Uncertainty

A table starting on page 3-56 lists the measurement uncertainty and ratio for each performance test using the recommended test equipment. Except for the External Trigger test, the ratios listed for the recommended test equipment meet or exceed the measurement uncertainty ratio required by U.S. MIL-STD-45662A. The table also provides a place to record the measurement uncertainty and ratio for each performance test using equipment other than the recommended test equipment. The table may be reproduced without written permission of Agilent Technologies.

Operation Verification and Performance Tests

The operation verification tests give a high confidence level (>90%) that the Agilent 35670A Dynamic Signal Analyzer is operating properly and within specifications. The operation verification tests are a subset of the performance tests. The operation verification tests should be used for incoming and after-repair inspections. The performance tests provide the highest level of confidence and are used to verify that the Agilent 35670A Dynamic Signal Analyzer conforms to its published specifications. Some repairs require a performance test to be done after the repair (see chapter 6, ‘’Replacing Assemblies’’ in the *Agilent 35670A Service Guide* for this information). The following table lists the operation verification and performance tests.

Operation Verification Tests	Performance Tests
Self Test	Self Test
DC Offset	DC Offset
Noise	Noise
Spurious Signals	Spurious Signals
Amplitude Accuracy	Amplitude Accuracy
Flatness	Flatness
Amplitude Linearity	Amplitude Linearity
A-Weight Filter	A-Weight Filter
Channel Match	Channel Match
Frequency Accuracy	Frequency Accuracy
Single Channel Phase Accuracy	Anti-Alias Filter
Tach Function	Input Coupling
ICP Supply	Harmonic Distortion
Source Amplitude Accuracy	Intermodulation Distortion
Source Flatness	Cross Talk
Source Distortion	Single Channel Phase Accuracy
	External Trigger
	Tach Function
	Input Resistance
	ICP Supply
	Source Amplitude Accuracy
	Source Output Resistance
	Source DC Offset
	Source Flatness
	Source Distortion

Specifications and Performance Tests

The following table lists specifications and the performance test or tests that verify each specification.

Specification	Performance Test
Frequency	
Accuracy	Frequency Accuracy
Single Channel Amplitude	
Residual dc response	DC Offset
FFT full scale accuracy at 1 kHz	Amplitude Accuracy
FFT full scale flatness	Flatness
FFT amplitude linearity at 1 kHz	Amplitude Linearity
FFT Dynamic Range	
Frequency alias responses	Anti-Alias Filter
Harmonic distortion	Harmonic Distortion
Intermodulation distortion	Intermodulation Distortion
Spurious and residual responses	Spurious Signals
Input Noise	Noise
Single Channel Phase	Single Channel Phase Accuracy
Cross Channel Amplitude	Channel Match
Cross Channel Phase	Channel Match
Input	
ac coupling rolloff	Input Coupling
Cross talk	Cross Talk
Input impedance	Input Resistance
ICP signal conditioning	ICP Supply
A-weight filter	A-Weight Filter
Trigger	
External trigger	External Trigger
Tachometer	
Tachometer level accuracy	Tach Function
Source Output	
Sine flatness	Source Flatness
Harmonic and sub-harmonic distortion	Source Distortion
Sine amplitude accuracy at 1 kHz	Source Amplitude Accuracy
Resistance	Source Output Resistance
dc offset accuracy	Source DC Offset

To load the program

For information about the program's softkeys, see the menu descriptions starting on page 3-51.

- **Set the Agilent 35670A Dynamic Signal Analyzer's power switch to off (O), then connect the analyzer, test instruments, and printer using GPIB cables.**
- **If you have the PC Style Keyboard, option 1CL, connect the keyboard to the analyzer using the keyboard cable (see ''To connect the optional keyboard'' in chapter 2).**
- **Insert the *Semiautomated Performance Test Disk* into the analyzer's disk drive, then set the power switch to on (|).**
- **After the analyzer finishes its power-up calibration routine, press the following keys:**

[**Local/GPIB**]
[SYSTEM CONTROLLR]
[**System Utility**]
[MEMORY USAGE]
[REMOVE WATERFALL]
[CONFIRM REMOVE]
[RETURN]
[MORE]
[SERVICE TESTS]
[PERFRMANC TEST]

- **Now go to one of the following procedures to continue:**
- ''To run the program in semiautomated mode''
- ''To run the program without a printer''
- ''To run the program in manual mode''

To run the program in semiautomated mode

You must have an GPIB printer connected to your system to run the program in semiautomated mode. If you do not have a printer, see ''To run the program without a printer'' later in this chapter.

- **Press the following keys and when the program prompts you, type in the information for the title page of the test record and press [** ENTER **]:**

[TITLE PAGE]
[TEST FACILITY]
[FACILITY ADDRESS]
[TESTED BY]
[REPORT NUMBER]
[CUSTOMER]
[MORE]
[TEMP]
[HUMIDITY]
[LINE FREQUENCY]
[RETURN]

- **Press the following keys and when the program prompts you, type in the equipment configuration information:**

[EQUIP CONFIG]
[AC CALIBRATO]
[SYNTH. 1]
[SYNTH. 2] (If needed)
[LOW-D OSCILLATO] (If needed)
[MULTIMETER]
[RETURN]

The GPIB address is 100 x (interface select code) + (primary address). The interface select code for the test equipment and printer is 7 (for example, if the primary address is 8, the GPIB address is 708).

When entering the calibration due date, only four characters are displayed on the screen. However, you can enter up to nine characters and they will be printed.

- **Press the following keys and type in the printer address when the program prompts you:**

[TEST CONFIG]
[PRINTER ADDRESS]
[PROCEDURE]
[OP_VERIFY] or [PERFORMAN]
[STOP AFTER]
[LIMIT FAILURE] or [NONE]
[RETURN]

- **Press the following keys to start the test:**

[START TESTING]
[START BEGINNING]

When you select [START BEGINNING], the data is written to a file on the disk and printed only after all tests are done. When you select [START MIDDLE] or [ONE TEST], the data is printed immediately after each measurement.

- **Follow the directions on the display.**

Warning

During the test, the program prompts you to change the test equipment connections. Always turn the ac calibrator output to OFF or STANDBY before changing test equipment connections. The ac calibrator can produce output voltages that could result in injury to personnel.

The directions on the display briefly tell you how to connect test equipment. For detailed illustrations of equipment setup, see the setup illustrations starting on page 3-13.

If you want to pause the program and return the Agilent 35670A Dynamic Signal Analyzer to front panel control, press [**BASIC**]. To continue the program, press [**BASIC**] [DISPLAY SETUP] [LOWER] [RETURN] [CONTINUE]. If you changed any instrument setup states, press [RESTART TEST] instead of [CONTINUE]to ensure accurate measurement results.

To run the program without a printer

Use this procedure if you do not have an GPIB printer connected to yout system.

- **Write in the information needed on the title page of the selected test record.**

The test records are located near the back of this chapter and may be copied without written permission of Agilent Technologies.

- **Press the following keys and when the program prompts you, type in the model number and GPIB address:**

[EQUIP CONFIG]
[AC CALIBRATO]
[SYNTH. 1]
[SYNTH. 2] (If needed)
[LOW-D OSCILLATO] (If needed)
[MULTIMETER]
[RETURN]

The GPIB addresses equals 100 ⟩(interface select code) + (primary address). The interface select code for the test equipment is 7 (for example, if the primary address is 8, the GPIB address is 708).

- **Press the following keys:**

[TEST CONFIG]
[PROCEDURE]
[OP_VERIFY] or [PERFORMAN]
[STOP AFTER]
[EACH MEASUREMENT]
[RETURN]

- **Press the following keys to start the test:**

[START TESTING]
[START BEGINNING]

- **Now follow the directions on the display and record every measurement result in the selected test record.**

Warning

During the test, the program prompts you to change the test equipment connections. Always turn the ac calibrator output to OFF or STANDBY before changing test equipment connections. The ac calibrator can produce output voltages that could result in injury to personnel.

The directions on the display briefly tell you how to connect test equipment. For detailed illustrations of equipment setup, see the setup illustrations starting on page 3-13.

If you want to pause the program and return the Agilent 35670A Dynamic Signal Analyzer to front panel control, press [**BASIC**]. To continue the program, press [**BASIC**] [DISPLAY SETUP] [LOWER] [RETURN] [CONTINUE]. If you changed any instrument setup states, press [RESTART TEST] instead of [CONTINUE] to ensure accurate measurement results.

To run the program in manual mode

Use this procedure if you want to run the program in manual mode. You will be prompted to set up all test equipment and you can check the analyzer's setup state after each measurement.

- **Write in the information needed on the title page of the selected test record.**

The test records are located near the back of this chapter and may be copied without written permission of Agilent Technologies.

- **Press the following keys and when the program prompts you, set all GPIB addresses to 0:**

[EQUIP CONFIG]
[AC CALIBRATO]
[SYNTH. 1]
[SYNTH. 2] (If needed)
[LOW-D OSCILLATO] (If needed)
[MULTIMETER]
[RETURN]

- **Press the following keys:**

[TEST CONFIG]
[PROCEDURE]
[OP_VERIFY] or [PERFORMAN]
[STOP AFTER]
[EACH MEASUREMENT]
[RETURN]

- **Press the following keys to start the test:**

[START TESTING]
[START BEGINNING]

- **Now follow the directions on the display and record the measurement result in the selected test record after every measurement.**

If you want to view the analyzer's setup state, press [**BASIC**] [**Disp Format**] [MEASURMNT STATE] or [INPUT STATE]. To continue the program, press [**BASIC**] [DISPLAY SETUP] [LOWER] [RETURN] [CONTINUE]. If you changed any instrument setup states, press [RESTART TEST] instead of [CONTINUE] to ensure accurate measurement results.

Warning

During the test, the program prompts you to change the test equipment connections. Always turn the ac calibrator output to OFF or STANDBY before changing test equipment connections. The ac calibrator can produce output voltages that could result in injury to personnel.

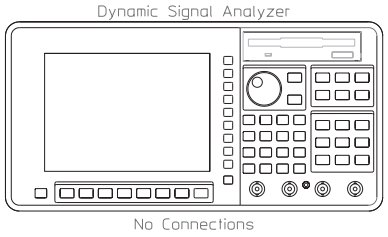
The directions on the display briefly tell you how to connect test equipment. For detailed illustrations of equipment setup, see the setup illustrations starting on the next page.

To set up the self test

Performance Test and Operation Verification

This test checks the measurement hardware in the Agilent 35670A. No performance tests should be attempted until the analyzer passes this test. This test takes approximately one minute to complete, and requires no external equipment.

1

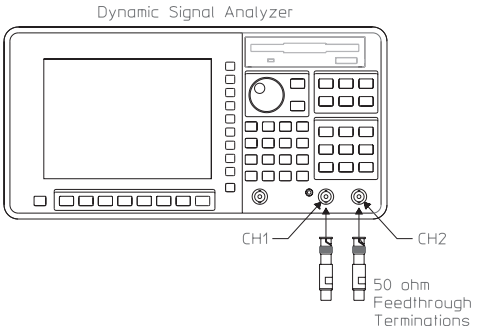


To set up the dc offset test

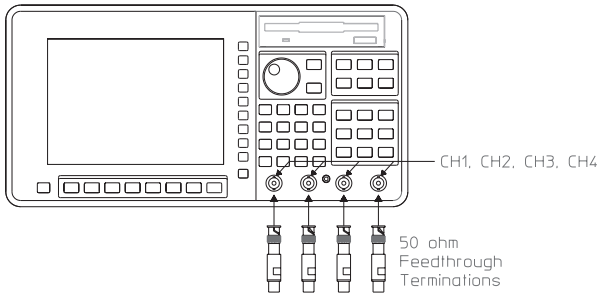
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its single channel amplitude specification for residual dc responses. In this test, the Agilent 35670A measures its internal residual dc offset at two amplitudes.

1 2 ch



1 4 ch

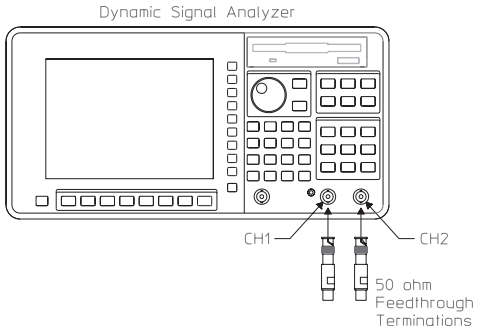


To set up the noise test

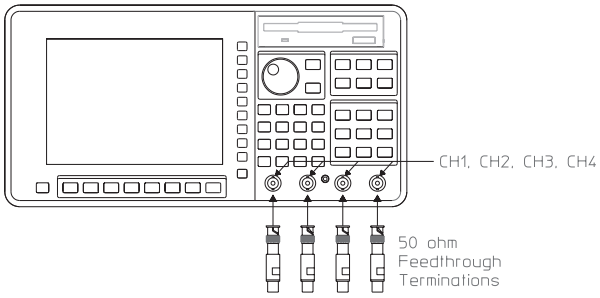
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its input noise specification. In this test, the Agilent 35670A measures its internal noise level.

1 2 ch



1 4 ch

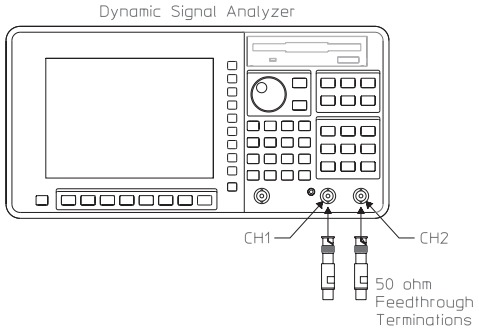


To set up the spurious signals test

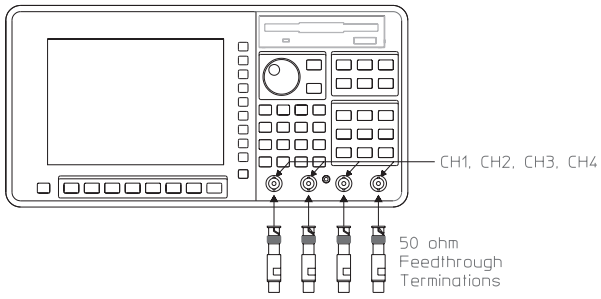
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its FFT dynamic range specification for spurious and residual responses. In this test, the Agilent 35670A measures its internal spurious signals. The test records at the end of this chapter list the frequencies that are checked.

1 2 ch



1 4 ch

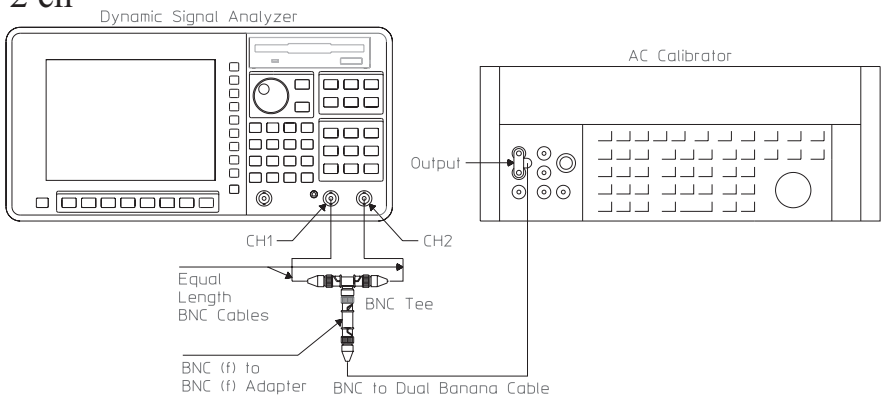


To set up the amplitude accuracy test

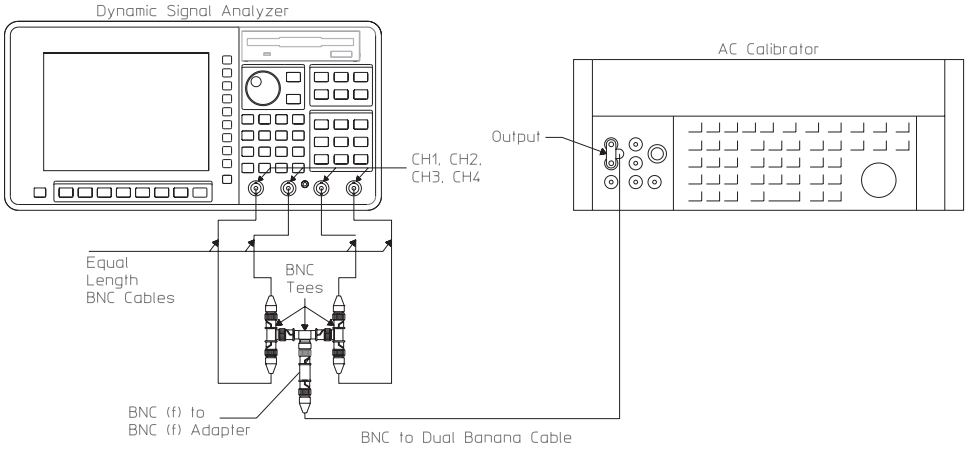
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its single channel amplitude specification for FFT full scale accuracy at 1 kHz. In this test, an ac calibrator outputs a 1 kHz signal with an exact amplitude to all channels. This test checks amplitude accuracy at 27, 19, 9, 1, –11, –27, –35, –43, and –51 dBVrms.

1 2 ch



1 4 ch

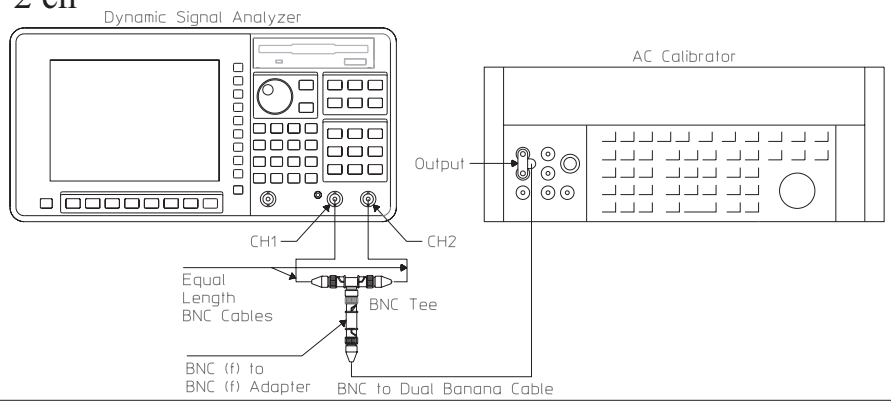


To set up the flatness test

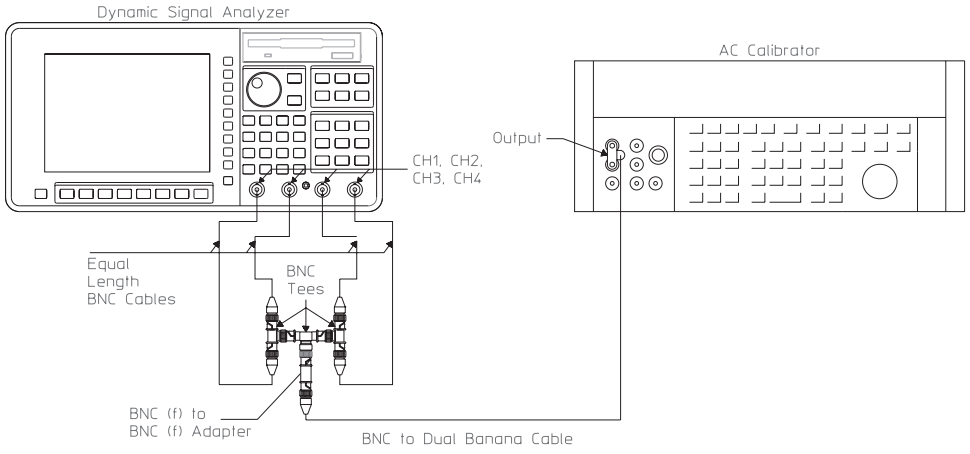
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its single channel amplitude specification for FFT full scale flatness relative to 1 kHz. In this test, the ac calibrator outputs a signal with an exact amplitude to all channels. The test records at the end of this chapter list the amplitudes and frequencies that are checked.

1 2 ch



1 4 ch

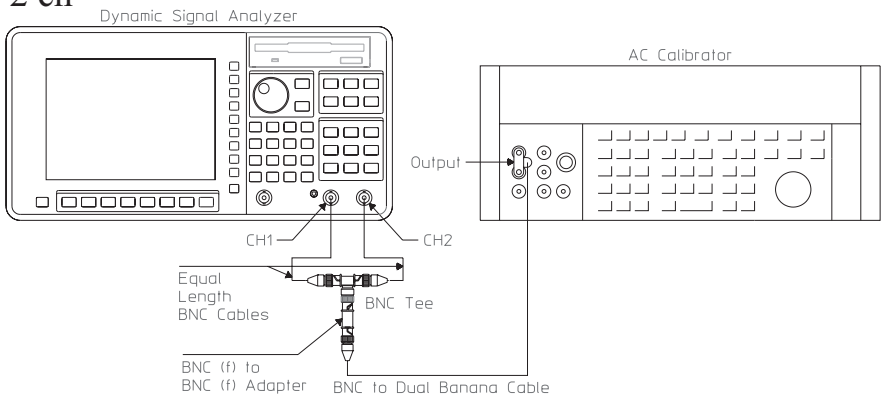


To set up the amplitude linearity test

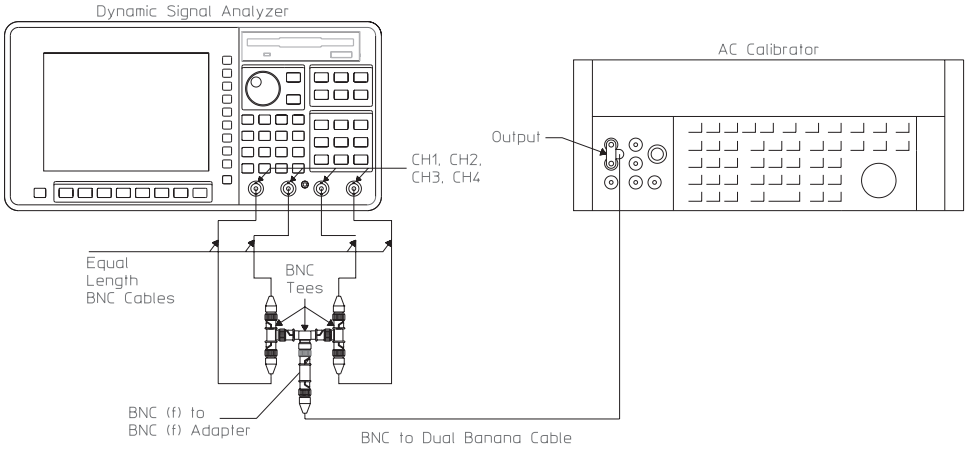
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its single channel amplitude specification for FFT amplitude linearity at 1 kHz. In this test, the ac calibrator outputs a 1 kHz signal with an an exact amplitude to all channels. This test checks amplitude linearity at 27, 13, –1, –15, –29, –43, and –53 dBVrms.

1 2 ch



1 4 ch

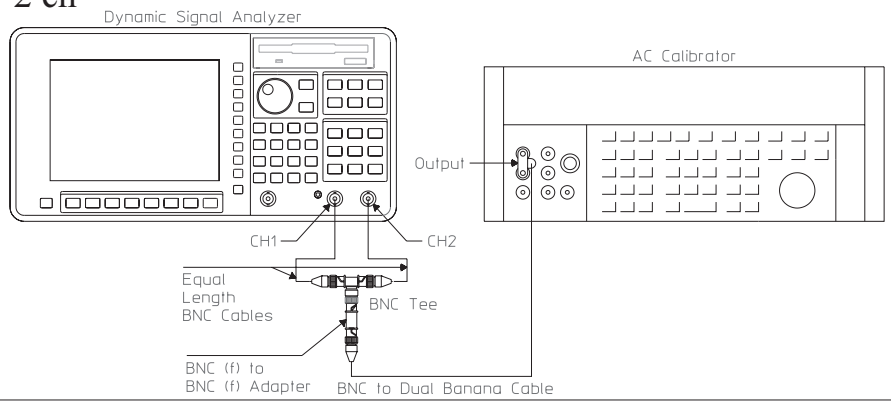


To set up the A-weight filter test

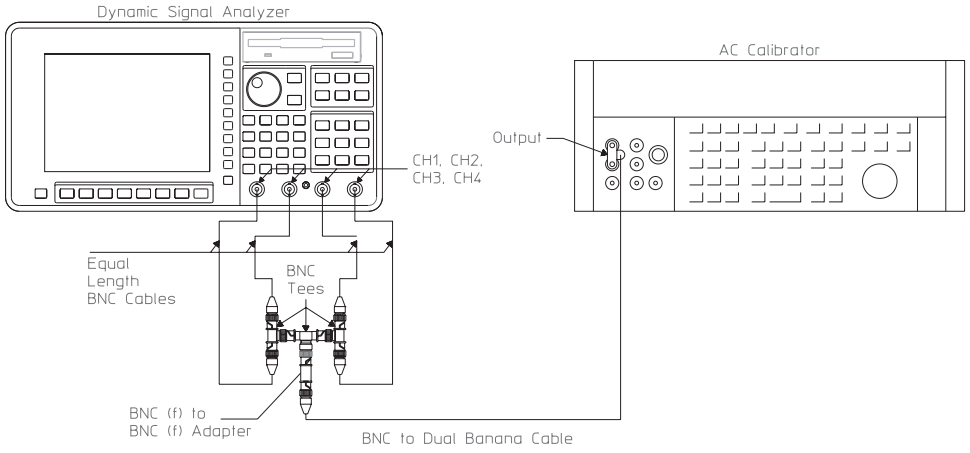
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its input specification for A-weight filter. In this test, an ac calibrator outputs a 1 dBVrms signal with an exact amplitude to all channels. The test records at the end of this chapter list the frequencies that are checked.

1 2 ch



1 4 ch

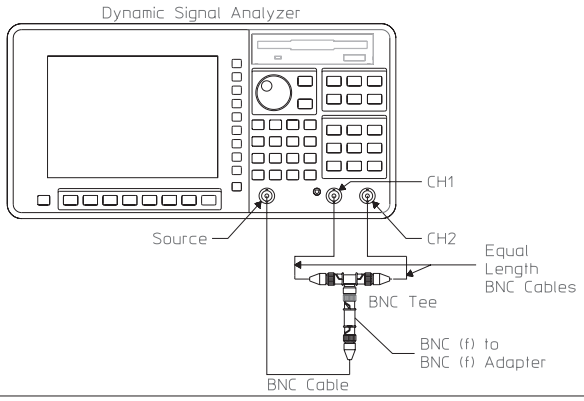


To set up the channel match test

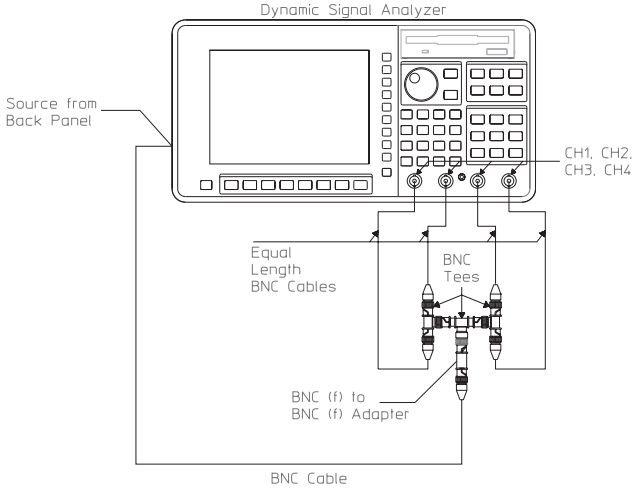
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its cross channel amplitude and cross channel phase specification. In this test, the Agilent 35670A's source outputs an identical signal to all channels. The Agilent 35670A measures the amplitude and phase of the signal and compares the values measured on one channel to the values measured on another channel.

1 2 ch



1 4 ch

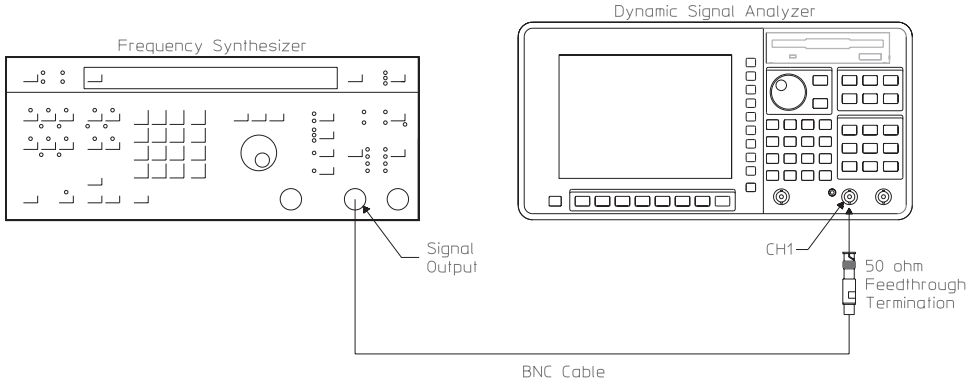


To set up the frequency accuracy test

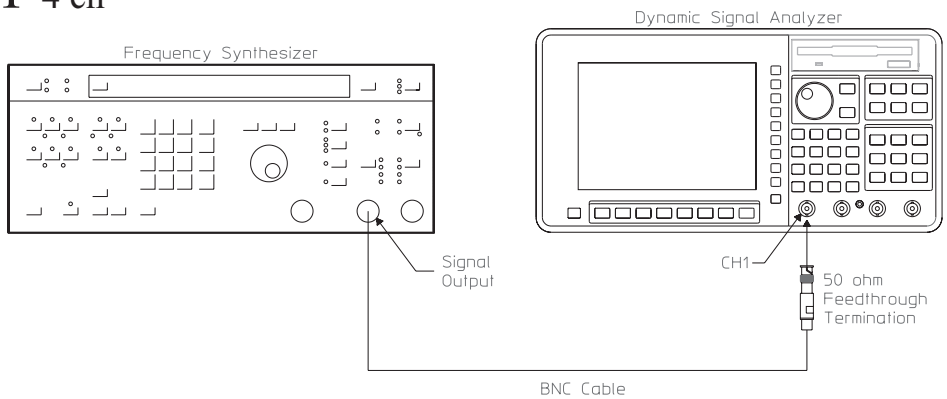
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its frequency accuracy specification. In this test, the analyzer measures the frequency of an accurate 50 kHz signal.

1 2 ch



1 4 ch

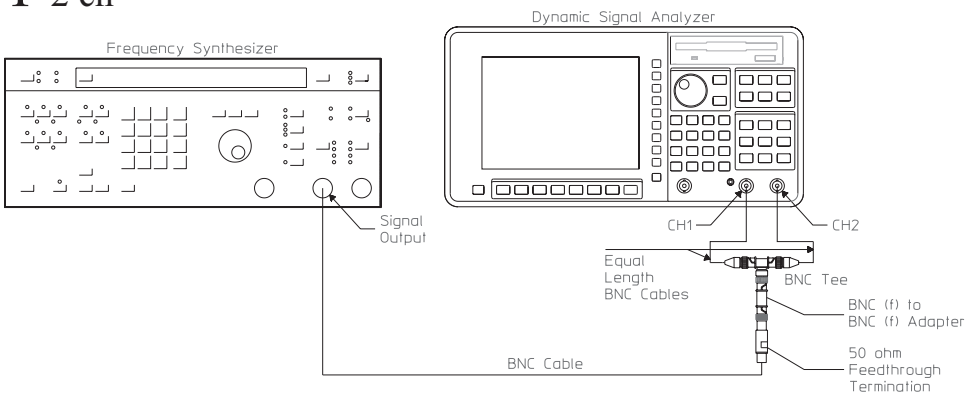


To set up the anti-alias filter test

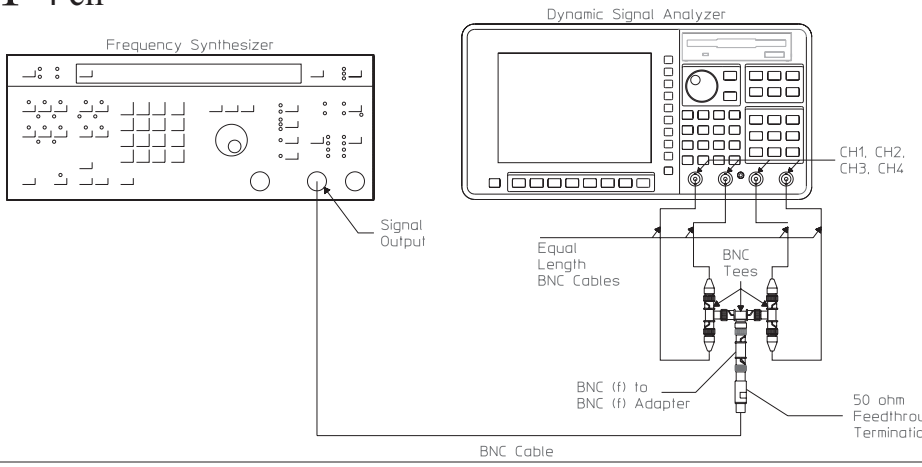
Performance Test only

This test verifies that the Agilent 35670A meets its FFT dynamic range specification for frequency alias responses. In this test, a frequency synthesizer outputs a –9 dBVrms signal known to cause an alias frequency to all channels. The Agilent 35670A then measures the alias frequency to determine how well the alias frequency was rejected. The test records at the end of this chapter list the frequencies that are checked.

1 2 ch



1 4 ch

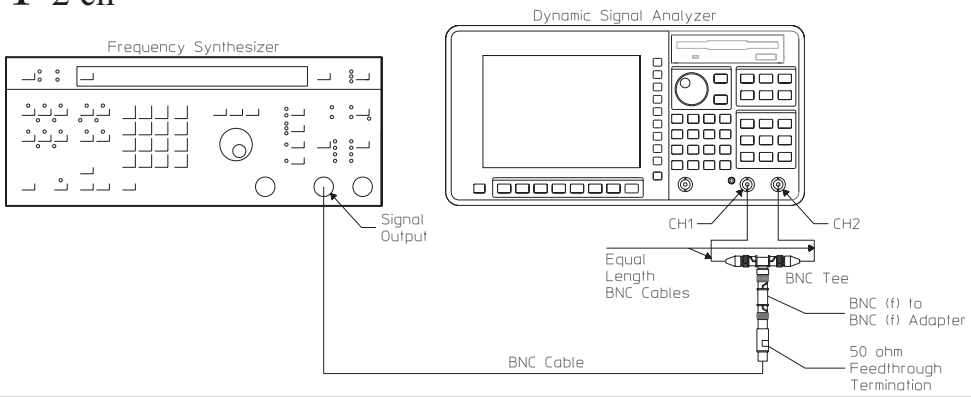


To set up the input coupling test

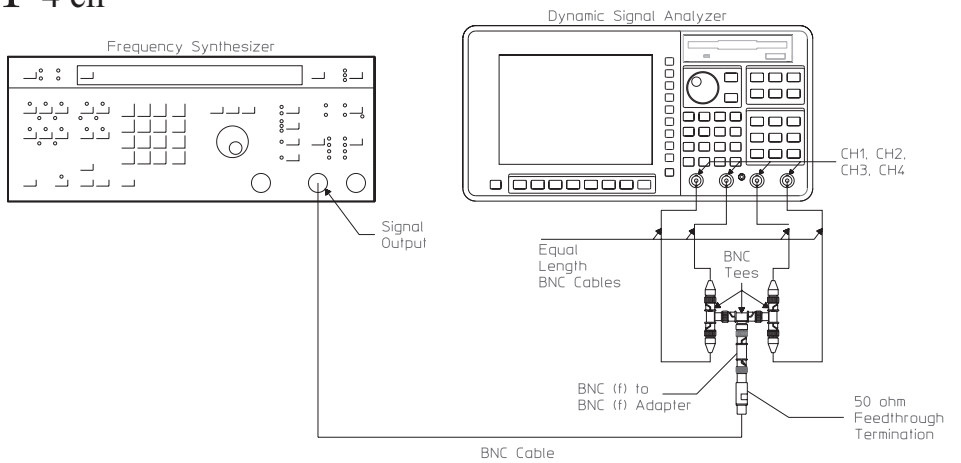
Performance Test only

This test verifies that the Agilent 35670A meets its input specification for ac coupling rolloff. In this test, a frequency synthesizer outputs a 1 Hz signal to all channels. The signal is measured in both ac and dc coupled modes. The value measured in ac coupled mode is subtracted from the value measured in dc coupled mode to determine the ac coupling rolloff.

1 2 ch



1 4 ch

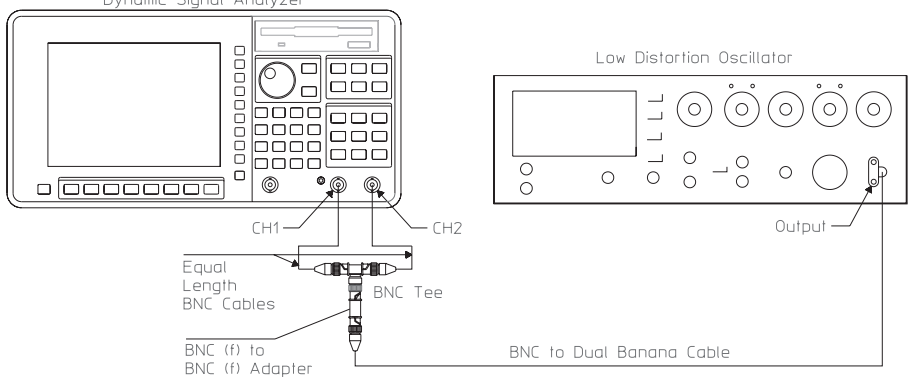


To set up the harmonic distortion test

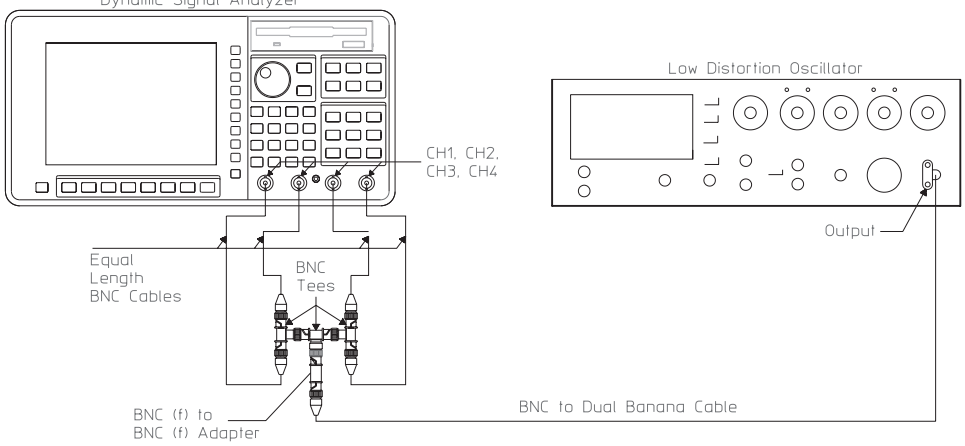
Performance Test only

This test verifies that the Agilent 35670A meets its FFT dynamic range specification for harmonic distortion. In this test, a low distortion oscillator or a frequency synthesizer and 24.5 kHz notch filter outputs a signal to all channels. The second, third, fourth, or fifth harmonic is then measured. If the harmonic falls outside the analyzer's frequency range, the analyzer measures the alias frequencies. The test records at the end of this chapter list the fundamental frequencies. If you are using the synthesizer and notch filter, the frequencies listed in the test record are approximate.

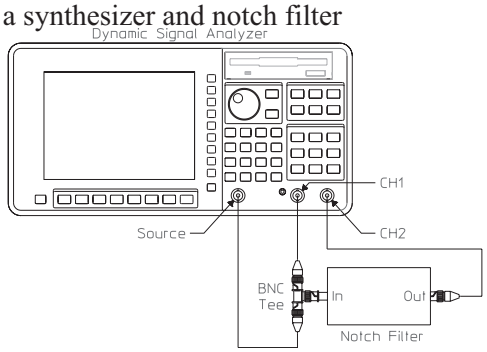
1 2 ch Using an HP339A



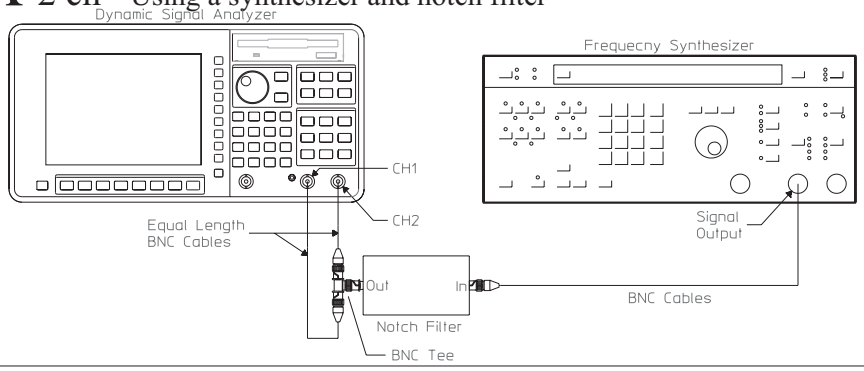
1 4 ch Using an HP 339A



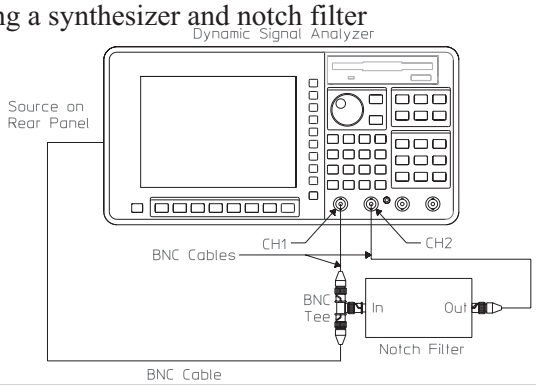
1A 2 ch Using a synthesizer and notch filter

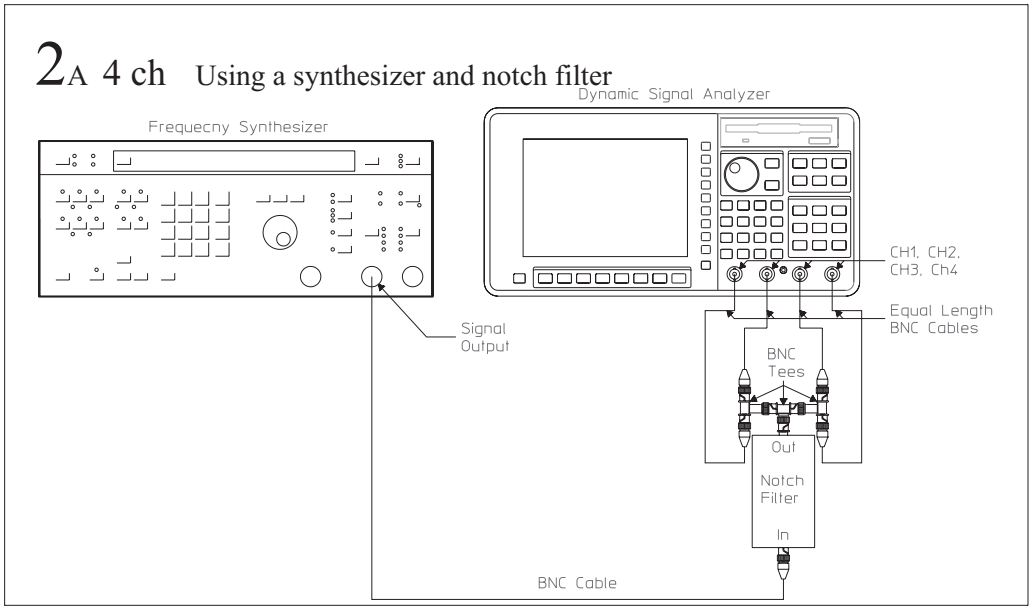


2A 2 ch Using a synthesizer and notch filter



1A 4 ch Using a synthesizer and notch filter



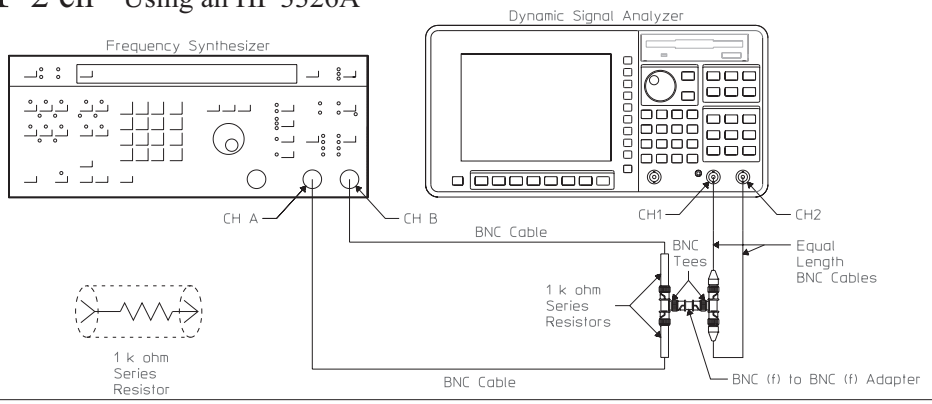

2A 4 ch Using a synthesizer and notch filter
Frequecny Synthesizer
Dynamic Signal Analyzer
CH1, CH2,
CH3, Ch4
Equal Length
BNC Cables
Signal
Output
BNC
Tees
Out
Notch
Filter
In
BNC Cable

To set up the intermodulation distortion test

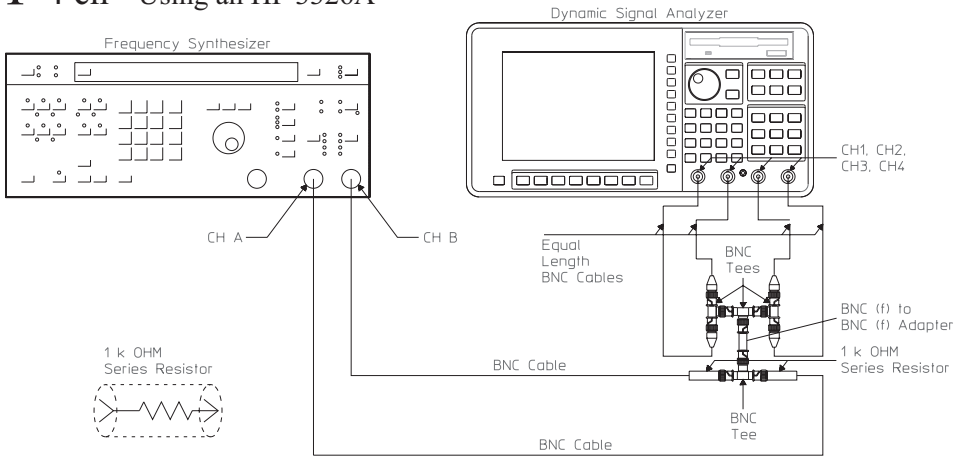
Performance Test only

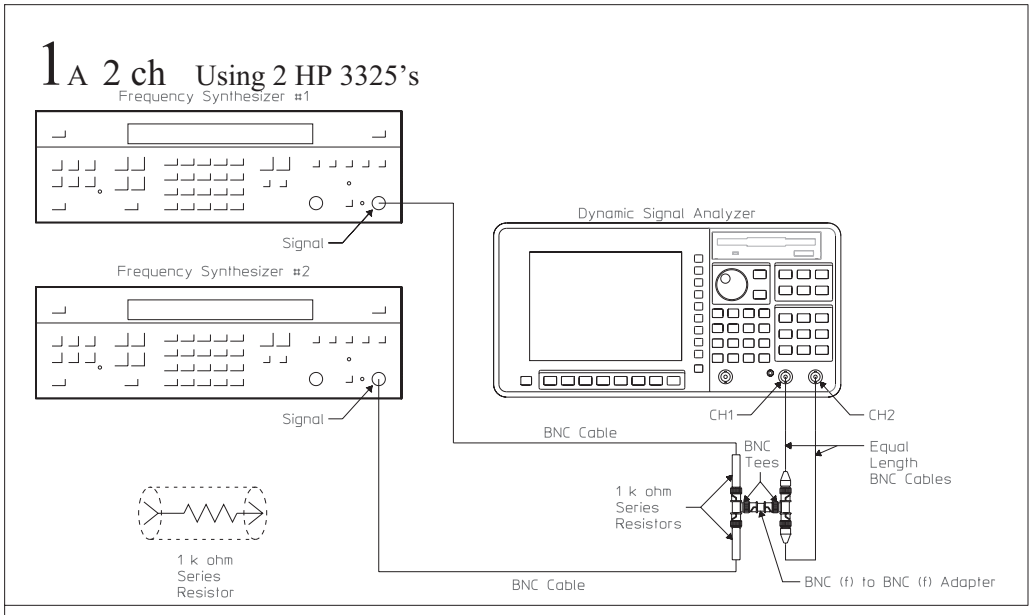
This test verifies that the Agilent 35670A meets its FFT dynamic range specification for intermodulation distortion. In this test, two signals are combined to provide a composite signal to all channels. The intermodulation products are found at the sum (F1 + F2) and difference (F1 – 2F2) frequencies. The analyzer measures the amplitude of each intermodulation product.

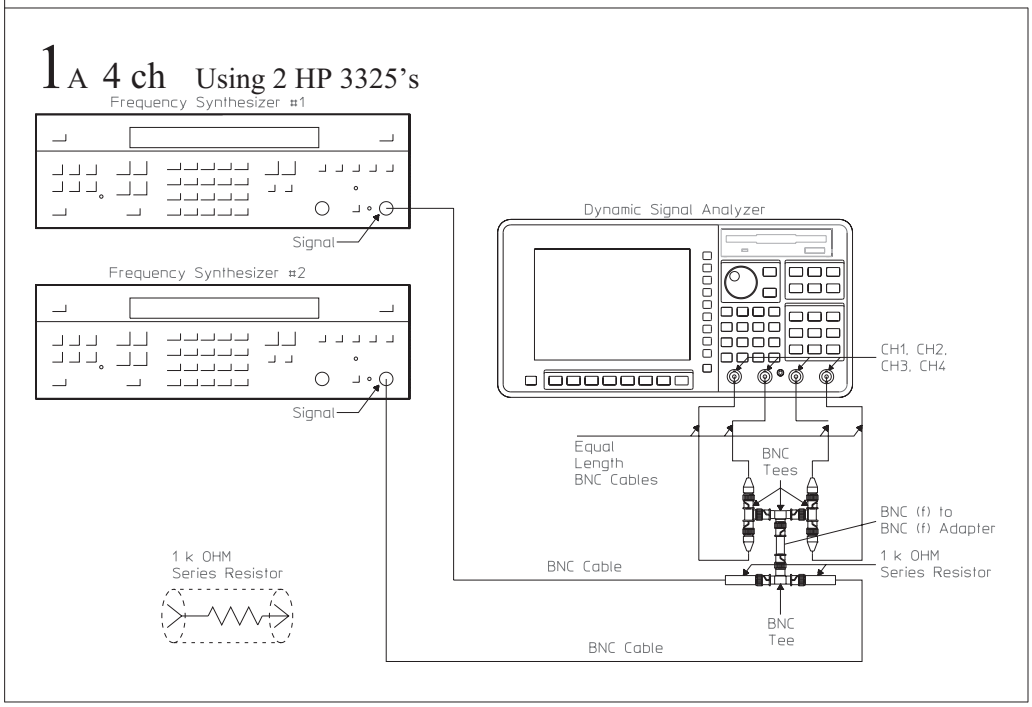
1 2 ch Using an HP 3326A



1 4 ch Using an HP 3326A




1A 2 ch Using 2 HP 3325's
Frequency Synthesizer #1
Signal
Frequency Synthesizer #2
Signal
Dynamic Signal Analyzer
CH1
CH2
BNC Cable
BNC Tees
Equal Length BNC Cables
1 k ohm Series Resistors
1 k ohm Series Resistor
BNC Cable
BNC (f) to BNC (f) Adapter

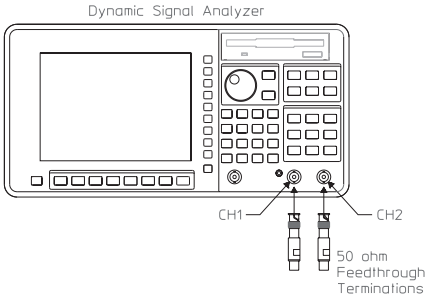

1A 4 ch Using 2 HP 3325's
Frequency Synthesizer #1
Signal
Frequency Synthesizer #2
Signal
Dynamic Signal Analyzer
CH1, CH2, CH3, CH4
Equal Length BNC Cables
BNC Tees
BNC (f) to BNC (f) Adapter
1 k OHM Series Resistor
1 k OHM Series Resistor
BNC Cable
BNC Tee
BNC Cable

To set up the cross talk test

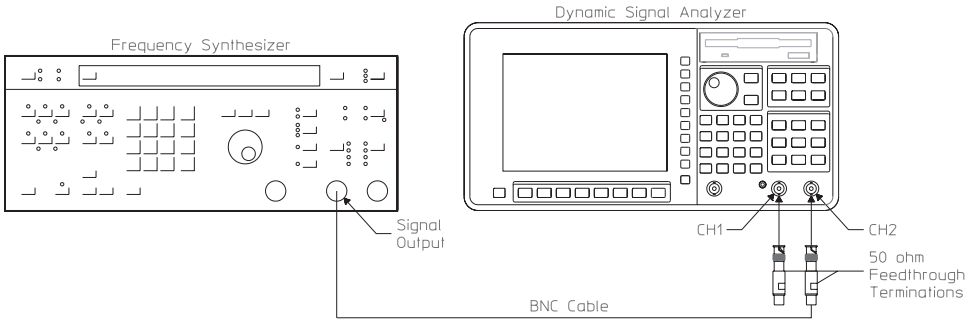
Performance Test only

This test verifies that the Agilent 35670A meets its input specification for channel-to-channel and channel-to-source cross talk. In this test, the Agilent 35670A measures the amount of energy induced from the source or input channel to another input channel. For source-to-channel crosstalk, the analyzer's source is set for 25.6 kHz, 9 dBVrms and the signal level at the input channels is measured. For channel-to-channel crosstalk, the frequency synthesizer outputs a 25.6 kHz or 51.2 kHz, 9 dBVrms signal to all but one input channel and the signal level at the unused input channel is measured.

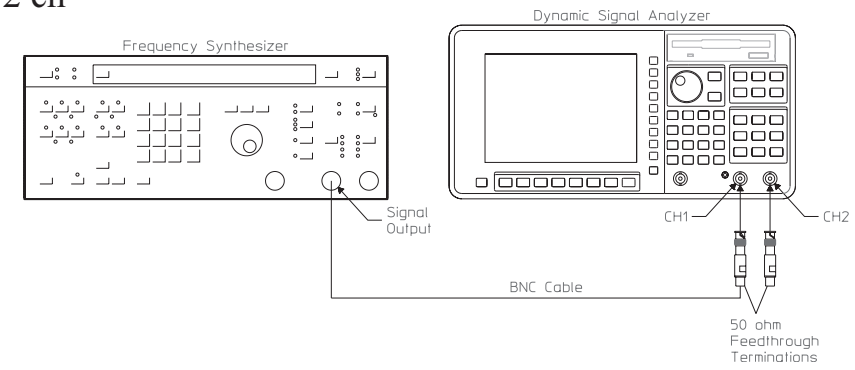
1 2 ch



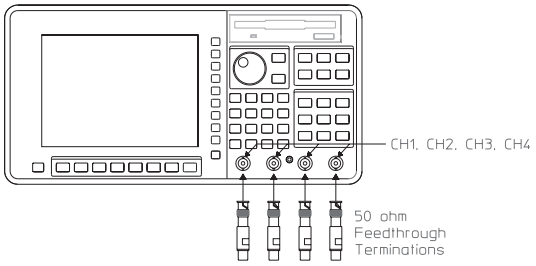
2 2 ch



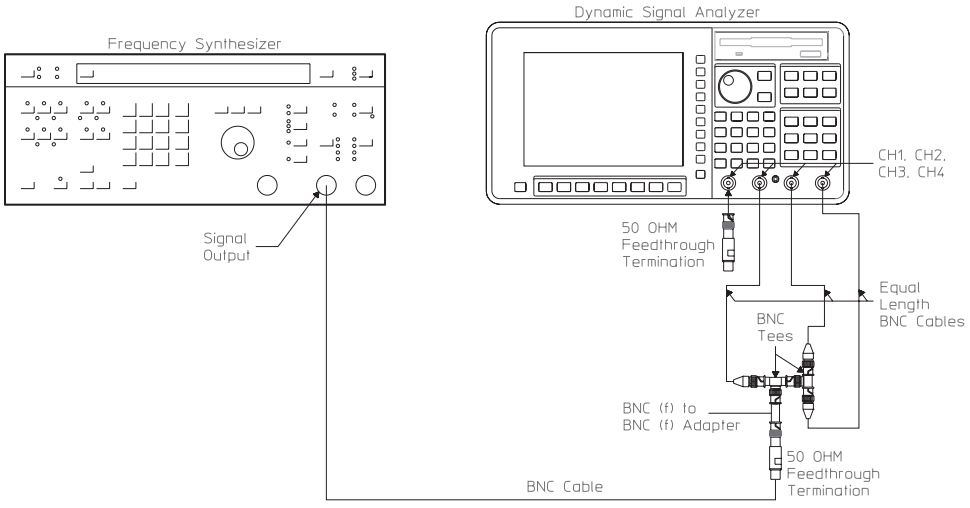
3 2 ch



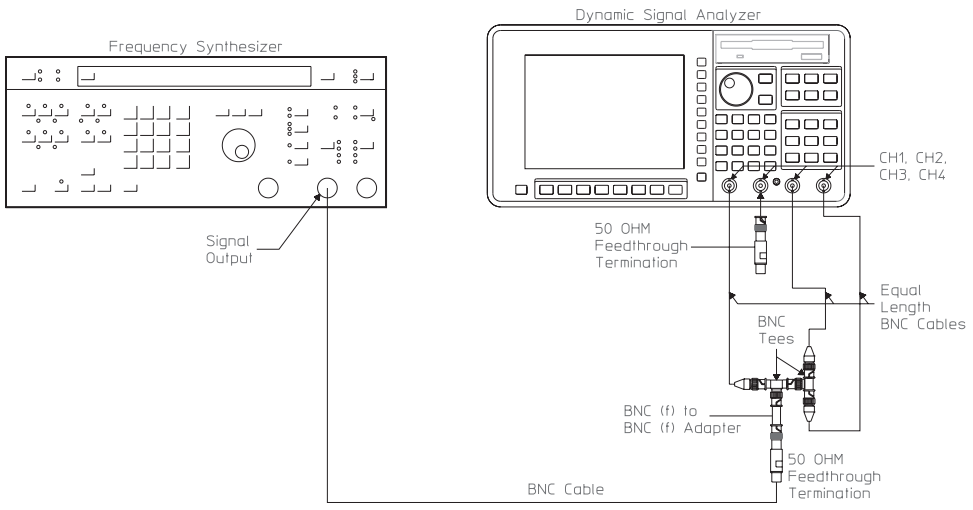
1 4 ch



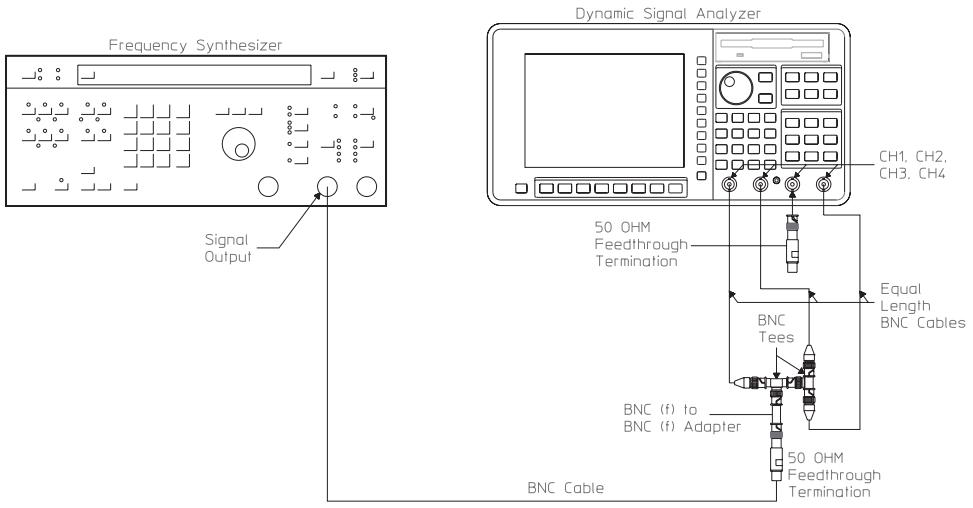
2 4 ch

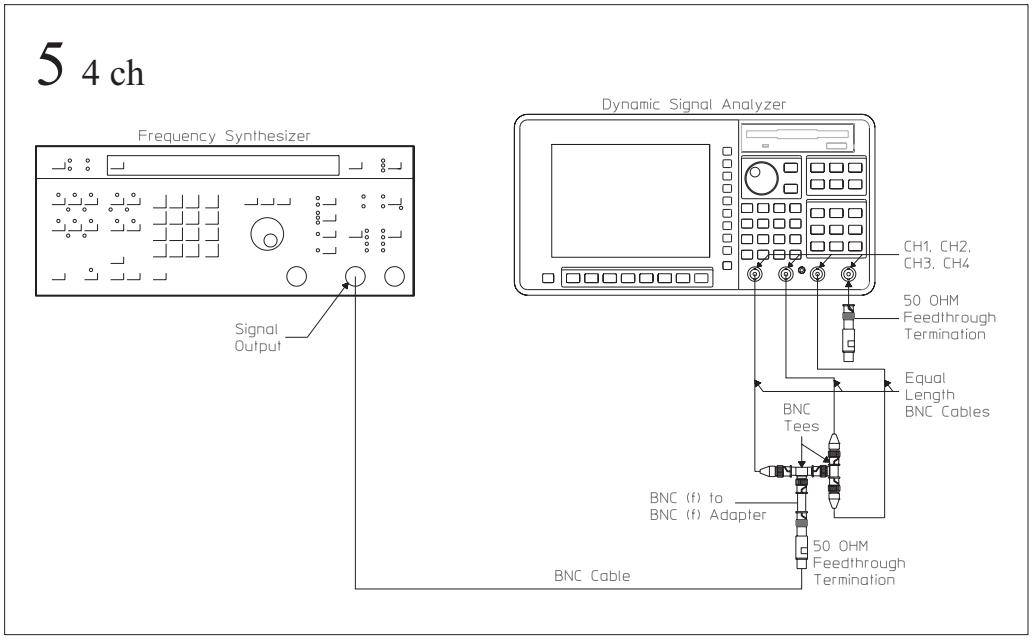


3 4 ch


Frequency Synthesizer
Dynamic Signal Analyzer
CH1, CH2,
CH3, CH4
Signal
Output
50 OHM
Feedthrough
Termination
Equal
Length
BNC Cables
BNC
Tees
BNC (f) to
BNC (f) Adapter
50 OHM
Feedthrough
Termination
BNC Cable

4 4 ch


Frequency Synthesizer
Dynamic Signal Analyzer
CH1, CH2,
CH3, CH4
Signal
Output
50 OHM
Feedthrough
Termination
Equal
Length
BNC Cables
BNC
Tees
BNC (f) to
BNC (f) Adapter
50 OHM
Feedthrough
Termination
BNC Cable

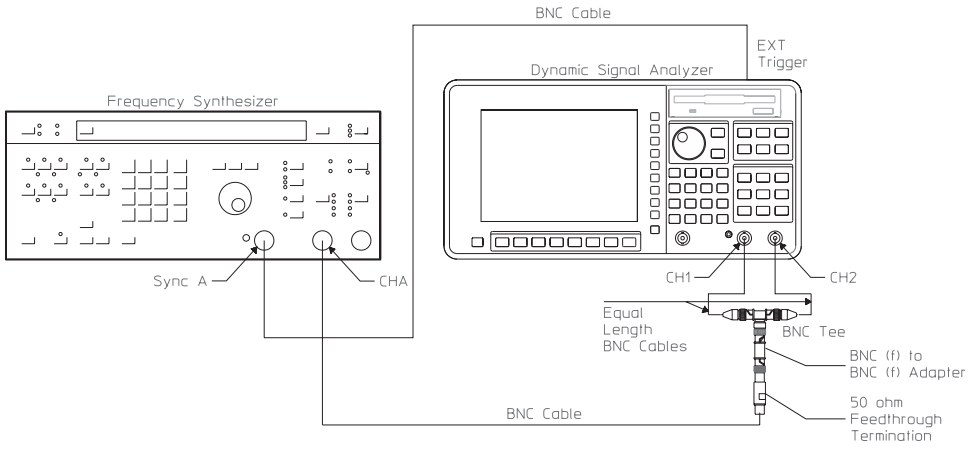

5 4 ch
Frequency Synthesizer
Dynamic Signal Analyzer
CH1, CH2,
CH3, CH4
50 OHM
Feedthrough
Termination
Signal
Output
Equal
Length
BNC Cables
BNC
Tees
BNC (f) to
BNC (f) Adapter
50 OHM
Feedthrough
Termination
BNC Cable

To set up the single channel phase accuracy test

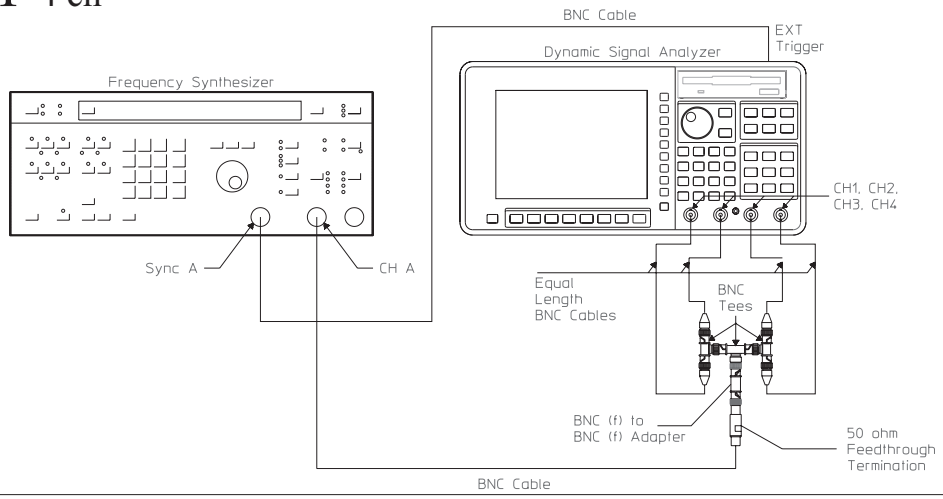
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its single channel phase accuracy specification. In this test, a frequency synthesizer outputs an identical square wave to all channels and a synchronized TTL-level signal to the trigger input. The phase difference between the trigger and each channel is measured to determine phase accuracy.

1 2 ch



1 4 ch

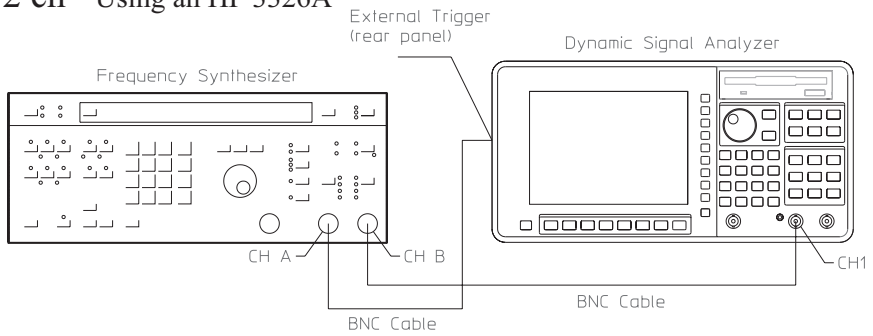


To set up the external trigger test

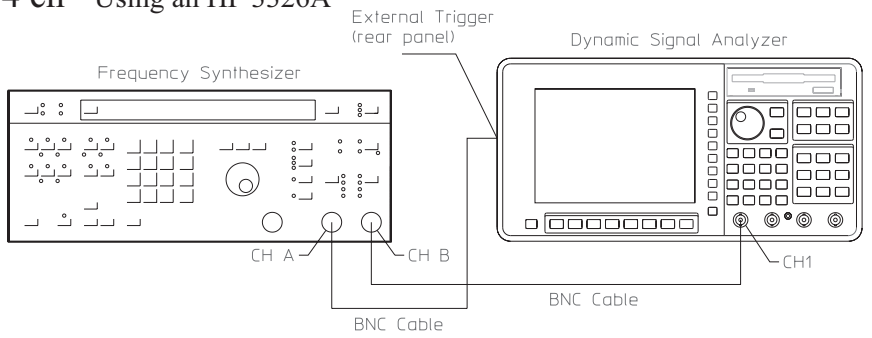
Performance Test only

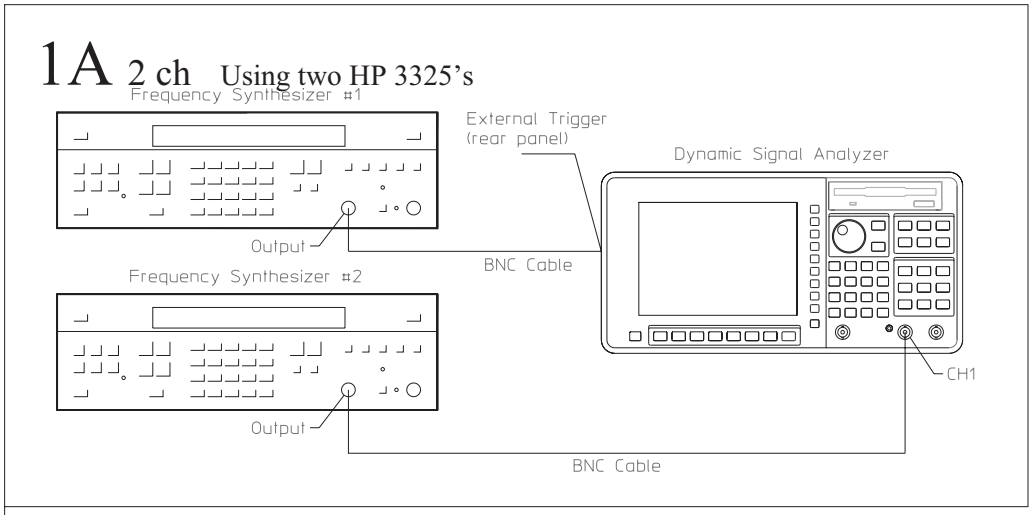
This test verifies that the Agilent 35670A meets its trigger specification for external trigger level accuracy. In this test, a frequency synthesizer outputs a 1 kHz signal to the external trigger input and a 12.8 kHz signal to channel 1. The analyzer makes an accurate triggered measurement on channel 1 to verify the trigger level and slope.

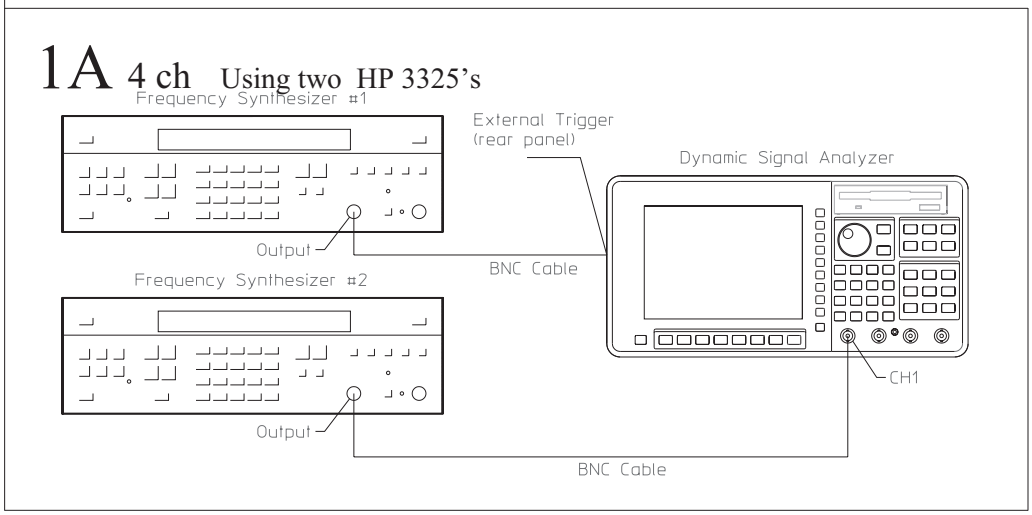
1 2 ch Using an HP 3326A



1 4 ch Using an HP 3326A




1A 2 ch Using two HP 3325's
Frequency Synthesizer #1
External Trigger
(rear panel)
Dynamic Signal Analyzer
Output
BNC Cable
Frequency Synthesizer #2
CH1
Output
BNC Cable

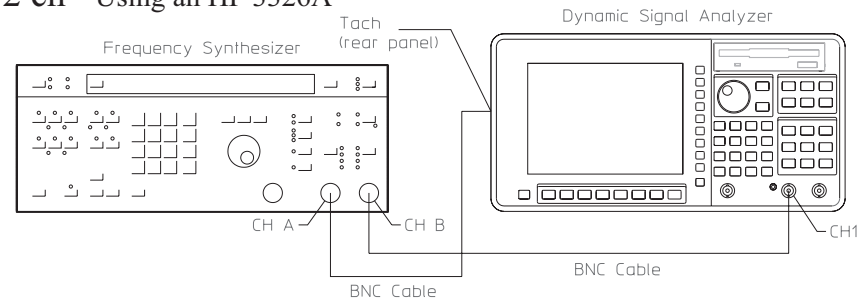

1A 4 ch Using two HP 3325's
Frequency Synthesizer #1
External Trigger
(rear panel)
Dynamic Signal Analyzer
Output
BNC Cable
Frequency Synthesizer #2
CH1
Output
BNC Cable

To set up the tach function test

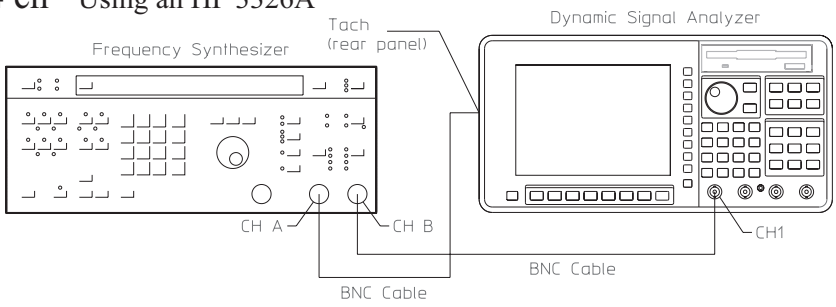
Performance Test and Operation Verification

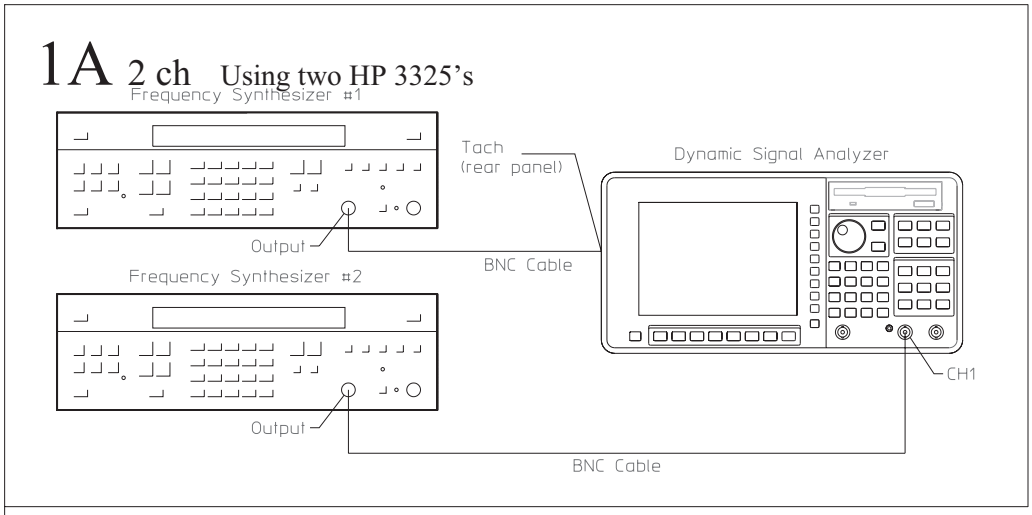
This test is only for Agilent 35670A's with option 1D0, computed order tracking. This test verifies that the Agilent 35670A meets its tachometer specification for trigger level accuracy. In this test, a frequency synthesizer outputs a signal to the tachometer input and to channel 1. The analyzer makes an accurate order measurement on channel 1 to verify the trigger level and slope.

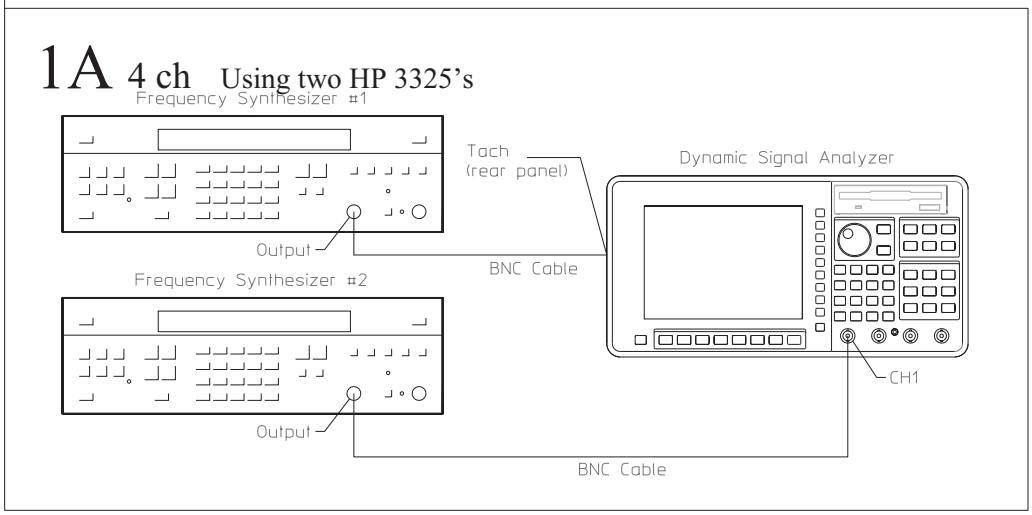
1 2 ch Using an HP 3326A



1 4 ch Using an HP 3326A




1A 2 ch Using two HP 3325's
Frequency Synthesizer #1
Tach
(rear panel)
Dynamic Signal Analyzer
Output
BNC Cable
Frequency Synthesizer #2
CH1
Output
BNC Cable

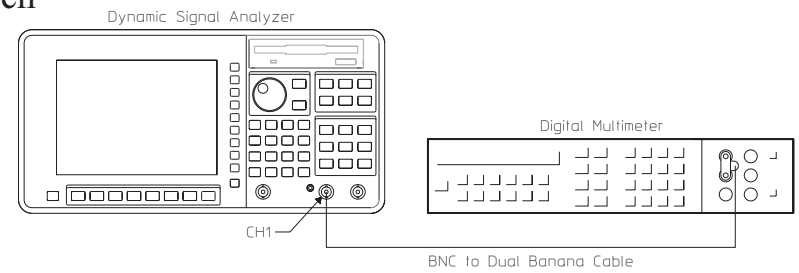

1A 4 ch Using two HP 3325's
Frequency Synthesizer #1
Tach
(rear panel)
Dynamic Signal Analyzer
Output
BNC Cable
Frequency Synthesizer #2
CH1
Output
BNC Cable

To set up the input resistance test

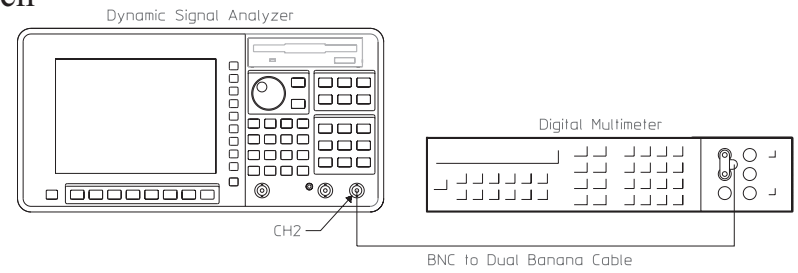
Performance Test only

This test verifies that the Agilent 35670A meets its input resistance specification. In this test, a digital multimeter directly measures the input resistance of each channel. The digital multimeter is set to the 1 MΩ range.

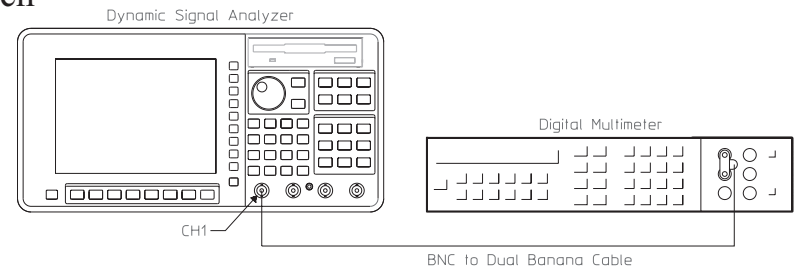
1 2 ch



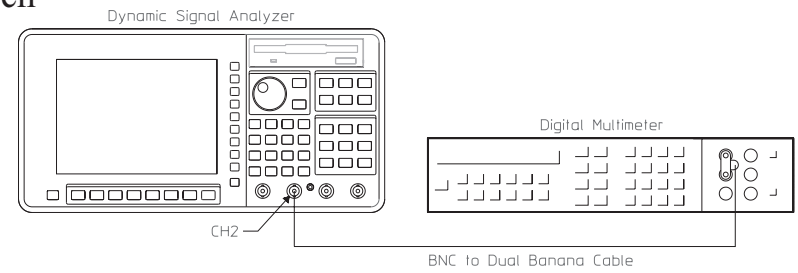
2 2 ch



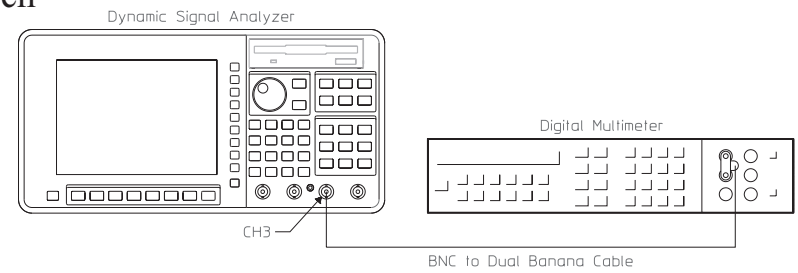
1 4 ch



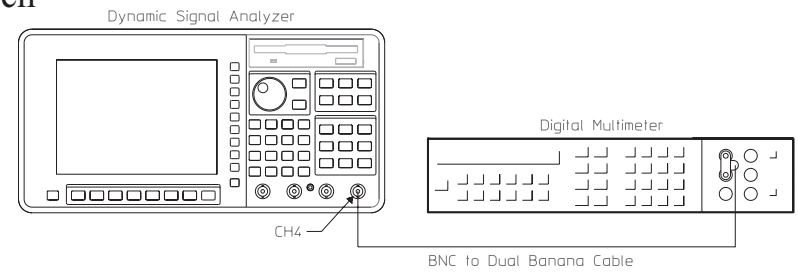
2 4 ch



3 4 ch



4 4 ch

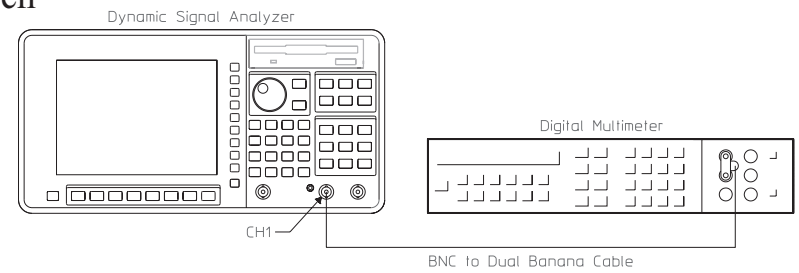


To set up the ICP supply test

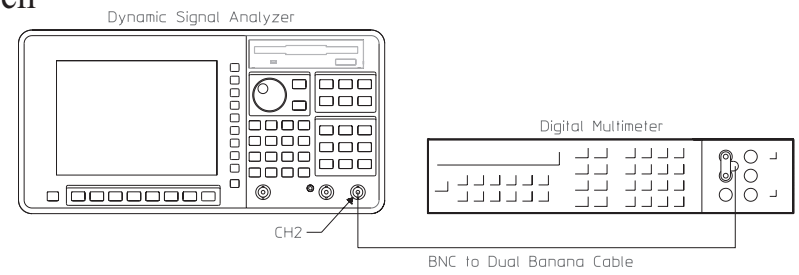
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its input specification for ICP signal conditioning. In this test, a digital multimeter directly measures the open circuit voltage of each channel. The digital multimeter measures the current souce of each channel by measuring the voltage across a 50 Ω feedthrough termination. The digital multimeter is set to the 100 V range to measure open circuit voltage and set to the 1 V range to measure the current source.

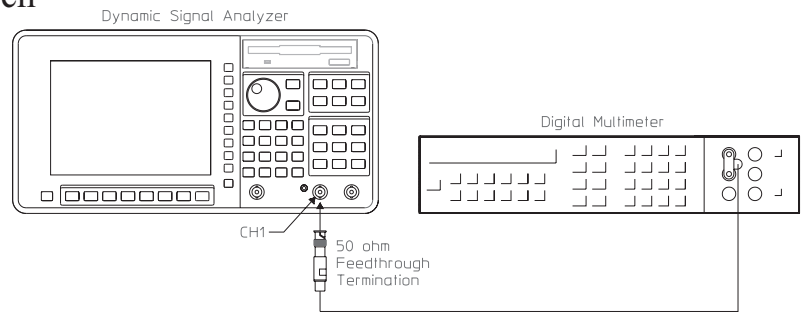
1 2 ch



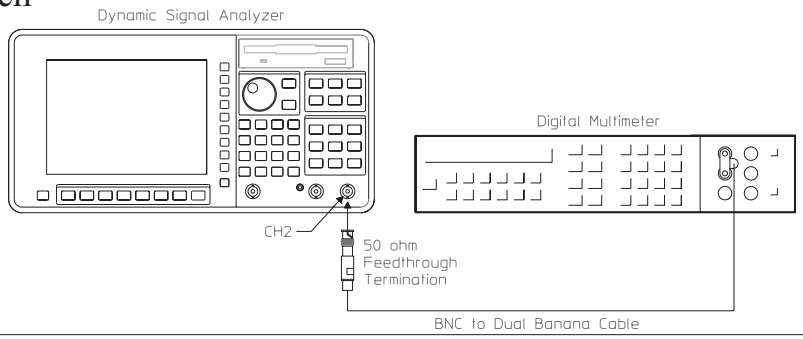
2 2 ch



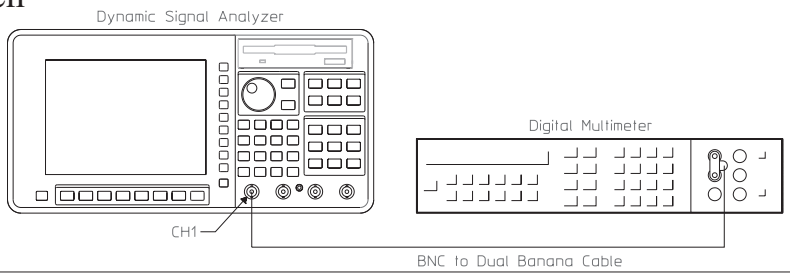
3 2 ch



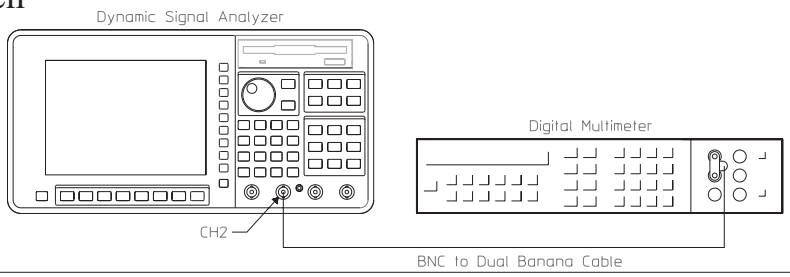
4 2 ch



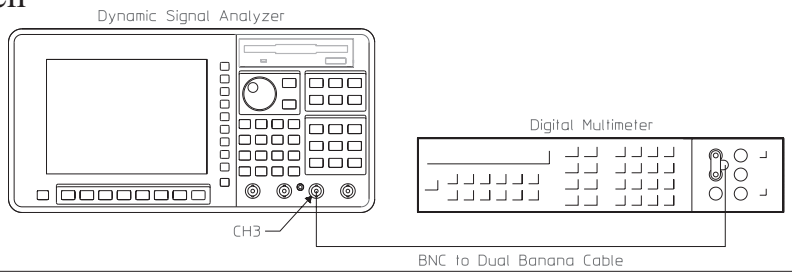
1 4 ch



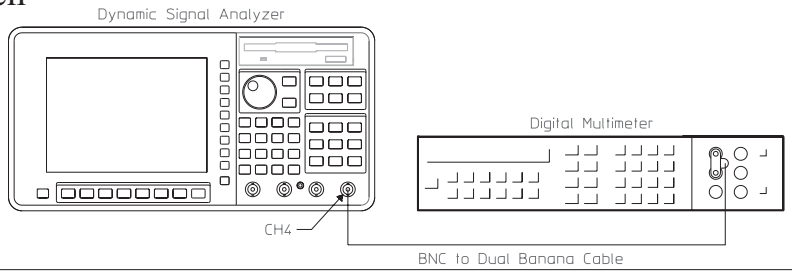
2 4 ch



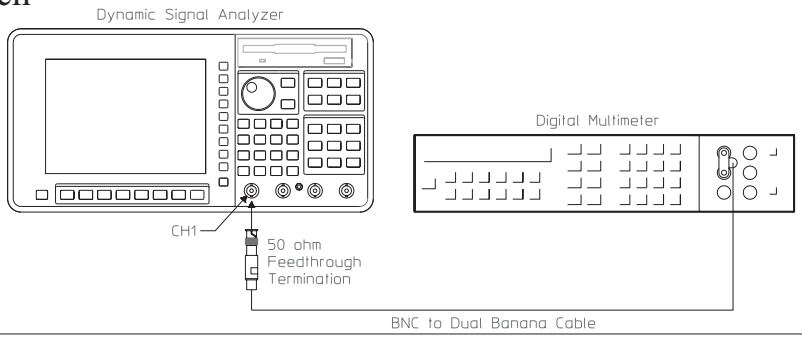
3 4 ch



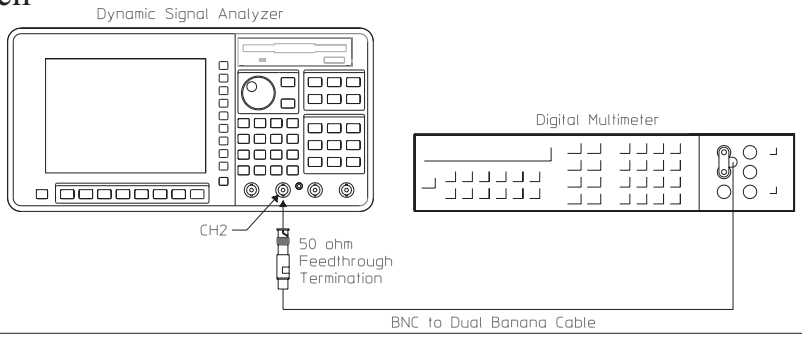
4 4 ch



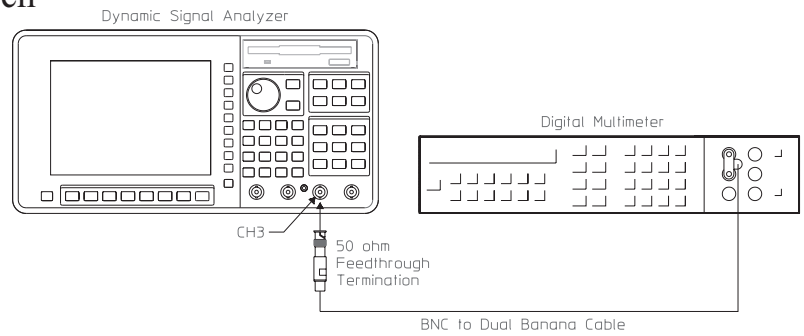
5 4 ch



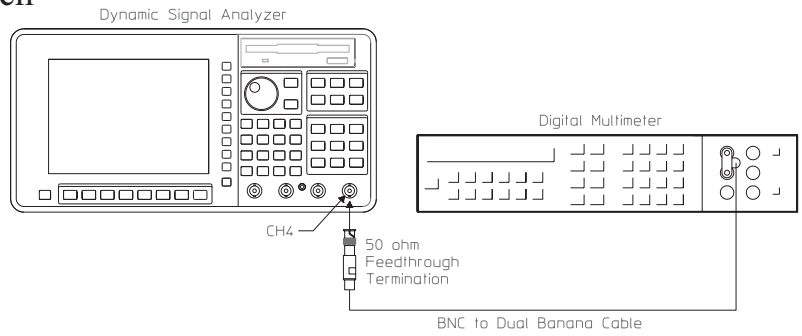
6 4 ch



7 4 ch


Dynamic Signal Analyzer
Digital Multimeter
CH3
50 ohm
Feedthrough
Termination
BNC to Dual Banana Cable

8 4 ch

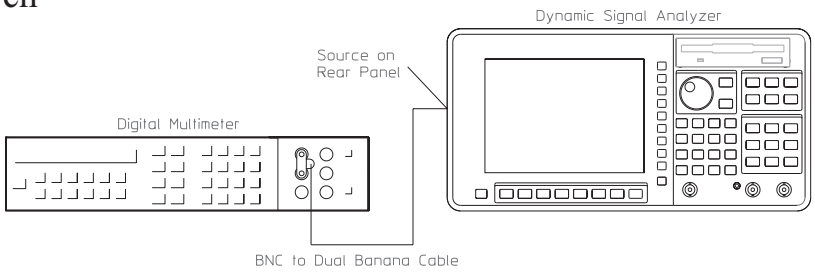

Dynamic Signal Analyzer
Digital Multimeter
CH4
50 ohm
Feedthrough
Termination
BNC to Dual Banana Cable

To set up the source amplitude accuracy test

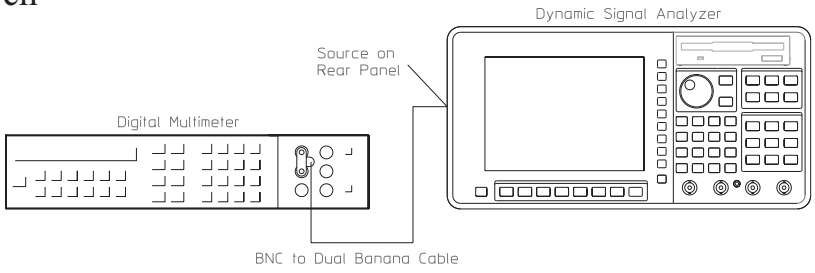
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its source output specification for sine amplitude accuracy at 1 kHz. In this test, a digital multimeter measures the amplitude accuracy of the source. Source amplitude accuracy is checked at 0.1 Vpk with the digital multimeter set to the 100 mVrms range and at 3.0 and 5.0 Vpk with the digital multimeter set to the 10 Vrms range. For the standard two channel analyzer, the digital multimeter is connected to the rear panel source connector instead of the front panel source connector. This is the only test that verifies the rear panel source port on the standard two channel analyzer.

1 2 ch



1 4 ch



To set up the source output resistance test

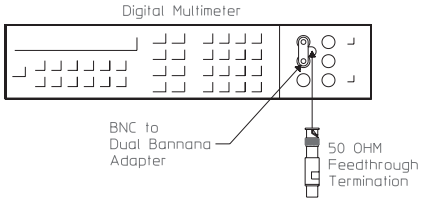
Performance Test only

This test verifies that the Agilent 35670A meets its source output specification for resistance. In this test, a digital multimeter measures the 50 Ω feedthrough termination. The channel 1 input then measures the source output across the feedthrough termination, then in an open circuit condition. The resistance is calculated using the following formula:

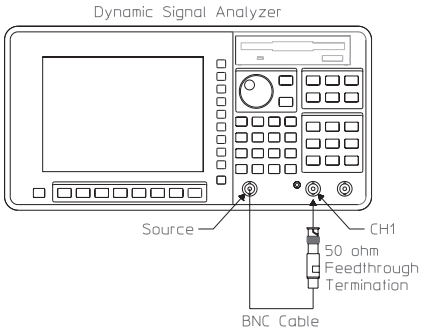
Rs = R1((Vopen - Vload)/Vload)

Note: Use the same 50 Ω feedthrough termination for steps 1 and 2.

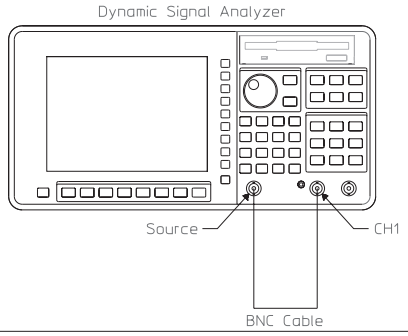
1 2 ch



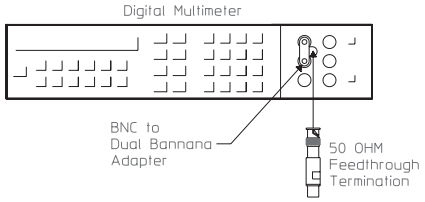
2 2 ch



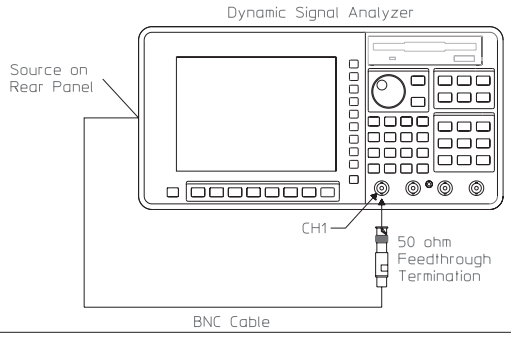
3 2 ch



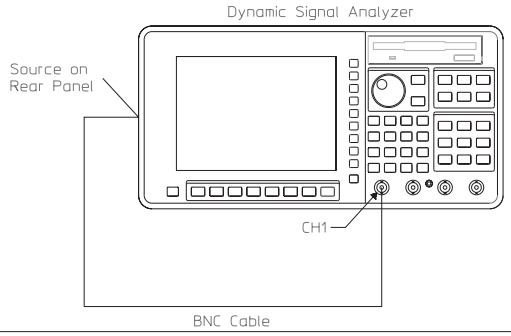
1 4 ch



2 4 ch



3 4 ch

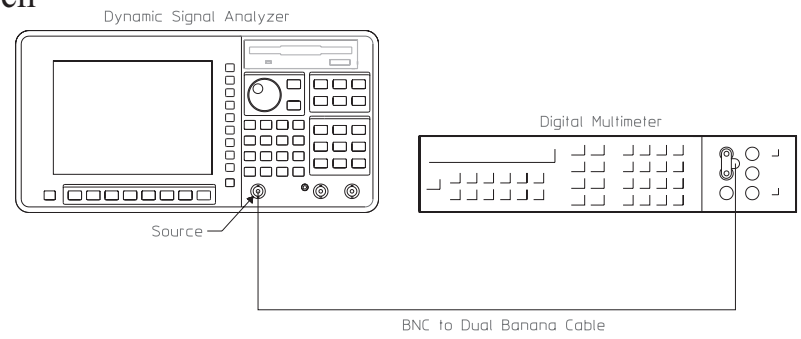


To set up the source dc offset test

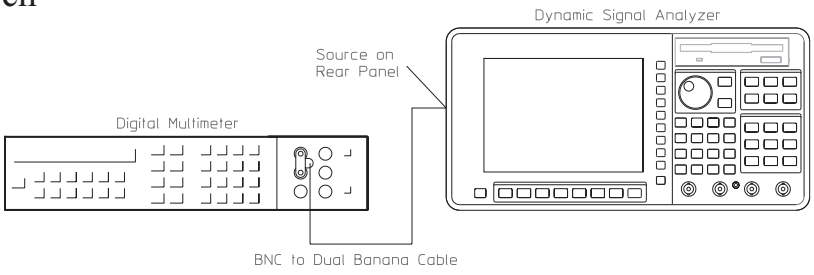
Performance Test only

This test verifies that the Agilent 35670A meets its source output specification for dc offset accuracy. In this test, a digital multimeter measures the dc offset voltage of the source with and without an ac component. The frequency of the ac component is 96 kHz. The test records at the end of this chapter list the voltages that are checked.

1 2 ch



1 4 ch

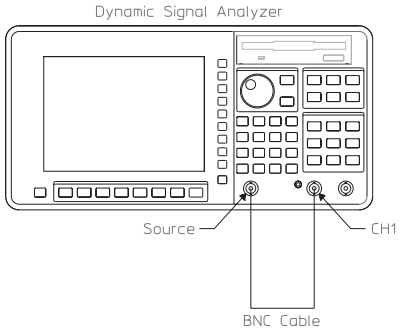


To set up the source flatness test

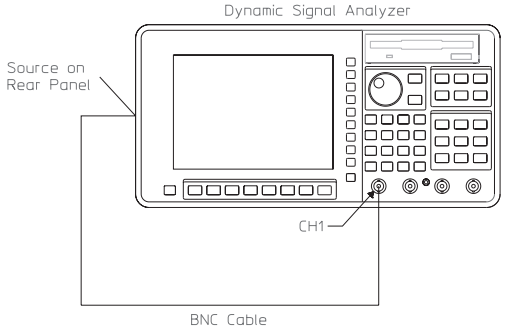
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its source output specification for sine flatness. In this test, the analyzer's channel 1 input measures the flatness of its source.

1 2 ch



1 4 ch

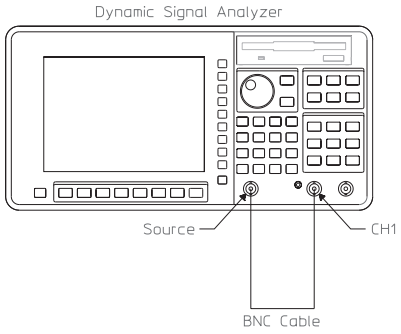


To set up the source distortion test

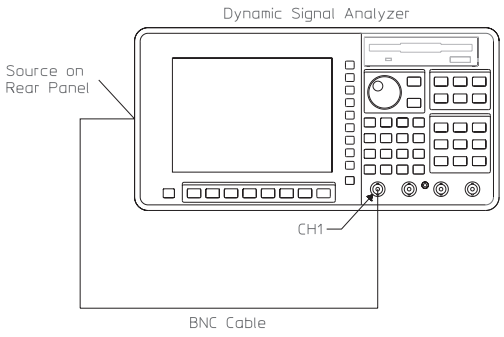
Performance Test and Operation Verification

This test verifies that the Agilent 35670A meets its source output specification for harmonic and sub-harmonic distortion and spurious signals. In this test, the analyzer's source is connected to its channel 1 input. The source is set for a maximum output level (5 Vpk) and the input range is set equal to the source level. The fundamental and harmonic is measured. The test records at the end of this chapter list the fundamental frequencies that are checked.

1 2 ch



1 4 ch



ITM_35670A Main Menu Descriptions

If you do not have a keyboard connected to the analyzer, use the numeric key pad and the alpha keys to enter names or numbers. See the analyzer's help text for a description of the alpha keys.

Load and run the ITM_35670A program to display the following softkeys:

[START TESTING]

Displays a menu that allows you to start testing with any test or to select just one test in the list. Before pressing this softkey, use [TEST CONFIG] and [EQUIP CONFIG].

[TEST CONFIG]

Displays the test configuration and a menu that allows you to enter the procedure, stop conditions, beeper prompt, and GPIB address for the analyzer and printer.

[EQUIP CONFIG]

Displays the test equipment configuration and a menu that allows you to enter the model number, calibration due date, serial number, and GPIB address for each test instrument.

[TITLE PAGE]

Displays the test record title page information and a menu that allows you to enter information for the analyzer.

[STOP ITM]

Stops the ITM_35670A program.

Start Testing Menu Descriptions

Press [START TESTING] to display the following softkeys:

[START BEGINNING]

Prints the test record title page information and starts the selected test procedure at the beginning. When you select [START BEGINNING], the data is written to a file on the disk and printed only after all tests are done.

[START MIDDLE]

Displays a list of all the tests in the selected procedure. Testing starts with the test you select and continues through the remainder of the tests in the list. When you select [START MIDDLE], the data is printed immediately after each measurement.

[ONE TEST]

Displays all the tests in the selected procedure. The test you select is the only test performed. When you select [ONE TEST], the data is printed immediately after each measurement.

[RETURN]

Returns to the ITM_35670A main menu.

Start a test to display the following softkeys:

[STOP TESTING]

Stops the test and returns to the ITM_35670A main menu.

[RESTART TEST]

Starts the current test over. Any connection prompts are repeated.

[RESTART MEAS]

Starts the current measurement over.

The following softkeys also appear when the program is waiting for you to press [CONTINUE]:

[STOP BEEPING]

Turns off the beeper prompt for the remainder of this measurement.

[CONTINUE]

Continues the test. Press this key after following the directions on the display.

Test Configuration Menu Descriptions

Press [TEST CONFIG] to display the test configuration and the following softkeys:

[Agilent 35670A ADDRESS]

Prompts you to enter the GPIB address for the Agilent 35670A Dynamic Signal Analyzer.

The GPIB addresses equals 100 \ (interface select code) + (primary address). The interface select code for the printer and test equipment is 7 (for example, if the primary address is 8, the GPIB address is 708).

[PRINTER ADDRESS]

Prompts you to enter the GPIB address for the printer. To disable the printer, set the printer address to 0.

[PROCEDURE]

Prompts you to select the operation verification procedure (OP_VERIFY) or the performance test procedure (PERFORMAN).

[BEEPER]

Toggles the beeper on and off. When the beeper is on, the program beeps approximately every 2 minutes while waiting for you to follow the directions on the display and press [CONTINUE].

[RETURN]

Returns to the ITM_35670A main menu.

[STOP AFTER]

Prompts you to select stop after limit failure, stop after each measurement, or do not stop after a limit failure or measurement. If [Limit Failure] is selected, the program stops after the failing measurement is displayed but before it is printed. At this point you can continue on and print the failing measurement or restart the measurement.

Equipment Configuration Menu Descriptions

Press [EQUIP CONFIG] to display the test equipment configuration and the following softkeys:

[AC CALIBRATO]

Prompts you to enter the model, serial number, GPIB address, and calibration due date for the ac calibrator.

If you select [Other] for model, the program prompts you to type in a model, serial number, and calibration due date but not an GPIB address.

When entering the calibration due date, only four characters are displayed on the screen. However, you can enter up to nine characters and they will be printed.

[SYNTH. 1]

Prompts you to enter the model, serial number, GPIB address, and calibration due date for the synthesizer.

[SYNTH. 2]

Prompts you to enter the model, serial number, GPIB address, and calibration due date for the second synthesizer. If the first synthesizer is an Agilent 3326A or if you are only performing the operation verification tests, you do not need a second synthesizer.

[LOW-D. OSCILLATO]

Prompts you to enter the model, serial number, and calibration due date for the low-distortion oscillator. If you have a 24.5 kHz notch filter or if you are only performing the operation verification tests, you do not need a low-distortion oscillator.

[MULTIMETER]

Prompts you to enter the model, serial number, GPIB address, and calibration due date for the multimeter.

[SAVE SETUP]

Saves the current equipment configuration to a file for future recall.

[RECALL SETUP]

Recalls an equipment configuration that was previously saved using [SAVE SETUP].

[RETURN]

Returns to the ITM_35670A main menu.

Title Page Menu Descriptions

Press [TITLE PAGE] to display the title page information and the following softkeys:

[TEST FACILITY]

Prompts you to enter the name or number of the testing entity.

[FACILITY ADDRESS]

Prompts you to enter the address of the testing entity.

[TESTED BY]

Prompts you to enter the name or number of the person performing the test.

[REPORT NUMBER]

Prompts you to enter the analyzer's report number.

[CUSTOMER]

Prompts you to enter the name or number of the person requesting the test.

[SERIAL NUMBER]

Prompts you to enter the analyzer's serial number.

[MORE]

Displays the next page.

[RETURN]

Returns to the ITM_35670A main menu.

[OPTIONS]

Prompts you to enter the analyzer's options.

[DATE]

Prompts you to enter the test date.

[TEMP]

Prompts you to enter the temperature of the environment during the test.

[HUMIDITY]

Prompts you to enter the humidity of the environment during the test.

[LINE FREQUENCY]

Prompts you to enter the power line frequency.

[MORE]

Displays the first page.

[RETURN]

Returns to the ITM_35670A main menu.

The title page information is printed at the beginning of the test procedure.

Measurement Uncertainty

The following table lists the measurement uncertainty and ratio for each performance test using the recommended test equipment. Except for the External Trigger test, the ratios listed for the recommended test equipment meet or exceed the measurement uncertainty ratio required by U.S. MIL-STD-45662A.

- If you are using equipment other than the recommended test equipment, you may calculate and record the measurement uncertainty and ratio for each performance test. The table may be reproduced without written permission of Agilent Technologies.

Performance Test	Using Recommended Test Equipment		Using Other Test Equipment	
	Measurement Uncertainty	**Ratio**	**Measurement Uncertainty**	**Ratio**
Self Test	NA	NA	NA	NA
DC Offset	NA	NA	NA	NA
Noise	NA	NA	NA	NA
Spurious Signals	NA	NA	NA	NA
Amplitude Accuracy				
−51 dBVrms	±0.020 dB	7.7:1		
−43 dBVrms	±0.0084 dB	>10:1		
−35 dBVrms	±0.004 dB	>10:1		
−27 dBVrms	±0.003 dB	>10:1		
−11 dBVrms	±0.001 dB	>10:1		
1 dBVrms	±0.0008 dB	>10:1		
9 dBVrms	±0.001 dB	>10:1		
19 dBVrms	±0.00081 dB	>10:1		
27 dBVrms	±0.00117 dB			
Flatness				
25.6 kHz, 27 dBVrms	±0.01487 dB	>10:1		
25.6 kHz, 9 dBVrms	±0.01277 dB	>10:1		
25.6 kHz, −11 dBVrms	±0.01277 dB	>10:1		
51.2 kHz, 27 dBVrms	±0.02025 dB	10:1		
51.2 kHz, 9 dBVrms	±0.01460 dB	>10:1		
51.2 kHz, −11 dBVrms	±0.01583 dB	>10:1		
99.84 kHz, 27 dBVrms	±0.02025 dB	10:1		
99.84 kHz, 9 dBVrms	±0.01460 dB	>10:1		
99.84 kHz, −11 dBVrms	±0.01583 dB	>10:1		

NA (not applicable) internal test

Performance Test	Using Recommended Test Equipment		Using Other Test Equipment	
	Measurement Uncertainty	Ratio	Measurement Uncertainty	Ratio
Amplitude Linearity 13 dBVrms –1 dBVrms –15 dBVrms –29 dBVrms –43 dBVrms –53 dBVrms	 ±0.0020 dB ±0.0020 dB ±0.0026 dB ±0.0046 dB ±0.0096 dB ±0.0255 dB	 >10:1 >10:1 >10:1 >10:1 >10:1 >10:1		
A-Weight Filter 10 Hz 31.62 Hz 100 Hz 1 kHz 10 kHz 25.120 kHz	 0.016 dB 0.012 dB 0.012 dB 0.011 dB 0.011 dB 0.012 dB	 >10:1 >10:1 >10:1 >10:1 >10:1 >10:1		
Channel Match magnitude phase	 ±0.00001 dB ±0.01 mdeg	 >10:1 >10:1		
Frequency Accuracy	±6.25 ppm	4.8:1		
Anti-Alias Filter <100 kHz <1 MHz	 ± 0.1 dB ± 0.3 dB	 >10:1 >10:1		
Input Coupling	± 0.001 dB	>10:1		
Harmonic Distortion using HP 339A using HP 3326A with filter	 ±0.184 dB ±0.92 dB	 4.46:1 10:1		
Intermodulation Distortion	±0.83 dB	10:1		
Cross Talk channel to channel source to input	 ± 0.1 dB ±1.34 dB	 >10:1 6:1		
Single Channel Phase Accuracy	± 0.25 deg †	>10:1		
External Trigger	280 mVpk	3.6:1 ‡		
Tach Function	330 mV	6:1		
Input Resistance	±17Ω	>10:1		
ICP Supply oven circuit voltage current	17Ω ±320 mV ±132<M > mA	 >10:1 >10:1		

† The sync output to signal output phase error was determined to be less than 0.25 degrees.
‡ If measured value is within ⌠3% of specification, verify synthesizer level accuracy. Note: Without 50 Ω termination, observed levels are twice the setting into high impedance.

Performance Test	Using Recommended Test Equipment		Using Other Test Equipment	
	Measurement Uncertainty	Ratio	Measurement Uncertainty	Ratio
Source Amplitude Accuracy				
0.1 Vpk	± 9.83 mVpk	>10:1		
3.0 Vpk	± 492.9 mVpk	>10:1		
5.0 Vpk	± 633.0 mVpk	>10:1		
Source Output Resistance	±0.15 Ω	>10:1		
Source DC Offset				
0 Vdc, 0 Vac-pk	± 238 nV	>10:1		
±10 Vdc, 0 Vac-pk	± 84 mV	>10:1		
0 Vdc, 5 Vac-pk	± 2.123 mV	>10:1		
±5 Vdc, 5 Vac-pk	± 43 mV	>10:1		
Source Flatness	± 0.2 dB	5.24:1		
Source Distortion				
fundamental <30 kHz	±0.5 dB	6.3:1		
fundamental ≥30 kHz	±0.5 dB	>10:1		

Performance Test Record - Two Channel

Test Facility _____

Facility Address _____

Tested By _____

Report Number_____

Customer Name_____

Serial Number_____

Installed Options _____

Date _____

Temperature_____

Humidity _____

Power Line Frequency _____

Test Instruments Used

Instrument	Model	ID or Serial Number	Calibration Due
AC Calibrator			
Synthesizer 1			
Synthesizer 2			
Low-D Oscillator			
Multimeter			

Serial Number:_____Report Number:_____
Test Date:___/___/___

Self Test

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Long Confidence				

DC Offset

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
–51 dBVrms, Ch 1		–30		
–51 dBVrms, Ch 2		–30		
–35 dBVrms, Ch 1		–30		
–35 dBVrms, Ch 2		–30		

Noise

Measurement	Lower Limit	Upper Limit ($^{dBV}/_{\sqrt{Hz}}$)	Measured Value ($^{dBV}/_{\sqrt{Hz}}$)	Pass/Fail
Two Ch, 6.4 kHz Span, Ch 1		–130		
Two Ch, 6.4 kHz Span, Ch 2		–130		
Two Ch, 51.2 kHz Span, Ch 1		–140		
Two Ch, 51.2 kHz Span, Ch 2		–140		
One Ch, 102.4 kHz Span, Ch 1		–140		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Spurious Signals

Two Ch, 0 Hz Start, Ch 1	–80
Two Ch, 0 Hz Start, Ch 2	–80
Two Ch, 200 Hz Start, Ch 1	–80
Two Ch, 200 Hz Start, Ch 2	–80
Two Ch, 400 Hz Start, Ch 1	–80
Two Ch, 400 Hz Start, Ch 2	–80
Two Ch, 600 Hz Start, Ch 1	–80
Two Ch, 600 Hz Start, Ch 2	–80
Two Ch, 800 Hz Start, Ch 1	–80
Two Ch, 800 Hz Start, Ch 2	–80
Two Ch, 1000 Hz Start, Ch 1	–80
Two Ch, 1000 Hz Start, Ch 2	–80
Two Ch, 1200 Hz Start, Ch 1	–80
Two Ch, 1200 Hz Start, Ch 2	–80
Two Ch, 1400 Hz Start, Ch 1	–80
Two Ch, 1400 Hz Start, Ch 2	–80
Two Ch, 1600 Hz Start, Ch 1	–80
Two Ch, 1600 Hz Start, Ch 2	–80
Two Ch, 3200 Hz Start, Ch 1	–80
Two Ch, 3200 Hz Start, Ch 2	–80
Two Ch, 4800 Hz Start, Ch 1	–80
Two Ch, 4800 Hz Start, Ch 2	–80
Two Ch, 6400 Hz Start, Ch 1	–80
Two Ch, 6400 Hz Start, Ch 2	–80
Two Ch, 8000 Hz Start, Ch 1	–80
Two Ch, 8000 Hz Start, Ch 2	–80
Two Ch, 9600 Hz Start, Ch 1	–80
Two Ch, 9600 Hz Start, Ch 2	–80
Two Ch, 11200 Hz Start, Ch 1	–80
Two Ch, 11200 Hz Start, Ch 2	–80
Two Ch, 12800 Hz Start, Ch 1	–80
Two Ch, 12800 Hz Start, Ch 2	–80
Two Ch, 14400 Hz Start, Ch 1	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Two Ch, 14400 Hz Start, Ch 2	–80
Two Ch, 16000 Hz Start, Ch 1	–80
Two Ch, 16000 Hz Start, Ch 2	–80
Two Ch, 17600 Hz Start, Ch 1	–80
Two Ch, 17600 Hz Start, Ch 2	–80
Two Ch, 19200 Hz Start, Ch 1	–80
Two Ch, 19200 Hz Start, Ch 2	–80
Two Ch, 20800 Hz Start, Ch 1	–80
Two Ch, 20800 Hz Start, Ch 2	–80
Two Ch, 22400 Hz Start, Ch 1	–80
Two Ch, 22400 Hz Start, Ch 2	–80
Two Ch, 24000 Hz Start, Ch 1	–80
Two Ch, 24000 Hz Start, Ch 2	–80
Two Ch, 25600 Hz Start, Ch 1	–80
Two Ch, 25600 Hz Start, Ch 2	–80
Two Ch, 27200 Hz Start, Ch 1	–80
Two Ch, 27200 Hz Start, Ch 2	–80
Two Ch, 28800 Hz Start, Ch 1	–80
Two Ch, 28800 Hz Start, Ch 2	–80
Two Ch, 30400 Hz Start, Ch 1	–80
Two Ch, 30400 Hz Start, Ch 2	–80
Two Ch, 32000 Hz Start, Ch 1	–80
Two Ch, 32000 Hz Start, Ch 2	–80
Two Ch, 33600 Hz Start, Ch 1	–80
Two Ch, 33600 Hz Start, Ch 2	–80
Two Ch, 35200 Hz Start, Ch 1	–80
Two Ch, 35200 Hz Start, Ch 2	–80
Two Ch, 36800 Hz Start, Ch 1	–80
Two Ch, 36800 Hz Start, Ch 2	–80
Two Ch, 38400 Hz Start, Ch 1	–80
Two Ch, 38400 Hz Start, Ch 2	–80
Two Ch, 40000 Hz Start, Ch 1	–80
Two Ch, 40000 Hz Start, Ch 2	–80
Two Ch, 41600 Hz Start, Ch 1	–80
Two Ch, 41600 Hz Start, Ch 2	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Two Ch, 43200 Hz Start, Ch 1	–80
Two Ch, 43200 Hz Start, Ch 2	–80
Two Ch, 44800 Hz Start, Ch 1	–80
Two Ch, 44800 Hz Start, Ch 2	–80
Two Ch, 46400 Hz Start, Ch 1	–80
Two Ch, 46400 Hz Start, Ch 2	–80
Two Ch, 48000 Hz Start, Ch 1	–80
Two Ch, 48000 Hz Start, Ch 2	–80
Two Ch, 49600 Hz Start, Ch 1	–80
Two Ch, 49600 Hz Start, Ch 2	–80
One Ch, 79200 Start, Ch 1	–80
One Ch, 80800 Start, Ch 1	–80
One Ch, 85600 Start, Ch 1	–80
One Ch, 87200 Start, Ch 1	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Spurious Signals (continued)

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
One Ch, 88800 Start, Ch 1		–80		
One Ch, 97000 Start, Ch 1		–80		
One Ch, 98600 Start, Ch 1		–80		
One Ch, 100200 Start, Ch 1		–80		
One Ch, 101800 Start, Ch 1		–80		

Amplitude Accuracy

Measurement	Lower Limit (dBVrms)	Upper Limit (dBVrms)	Measured Value (dBVrms)	Pass/Fail
–51 dBVrms, Ch 1	–51.15	–50.85		
–51 dBVrms, Ch 2	–51.15	–50.85		
–43 dBVrms, Ch 1	–43.15	–42.85		
–43 dBVrms, Ch 2	–43.15	–42.85		
–35 dBVrms, Ch 1	–35.15	–34.85		
–35 dBVrms, Ch 2	–35.15	–34.85		
–27 dBVrms, Ch 1	–27.15	–26.85		
–27 dBVrms, Ch 2	–27.15	–26.85		
–11 dBVrms, Ch 1	–11.15	–10.85		
–11 dBVrms, Ch 2	–11.15	–10.85		
1 dBVrms, Ch 1	0.85	1.15		
1 dBVrms, Ch 2	0.85	1.15		
9 dBVrms, Ch 1	8.85	9.15		
9 dBVrms, Ch 2	8.85	9.15		
19 dBVrms, Ch 1	18.85	19.15		
19 dBVrms, Ch 2	18.85	19.15		
27 dBVrms, Ch 1	26.85	27.15		
27 dBVrms, Ch 2	26.85	27.15		

Flatness

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
27 dBVrms, 99.84 kHz, One Ch, Ch 1	–0.2	0.2		
9 dBVrms, 99.84 kHz, One Ch, Ch 1	–0.2	0.2		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
–11 dBVrms, 99.84 kHz, One Ch, Ch 1	–0.2	0.2		
27 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
27 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
9 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
9 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
–11 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		

Amplitude Linearity

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
13 dBVrms, Ch 1	–0.0615	0.061		
13 dBVrms, Ch 2	–0.0615	0.061		
–1 dBVrms, Ch 1	–0.105	0.104		
–1 dBVrms, Ch 2	–0.105	0.104		
–15 dBVrms, Ch 1	–0.33	0.318		
–15 dBVrms, Ch 2	–0.33	0.318		
–29 dBVrms, Ch 1	–1.551	1.316		
–29 dBVrms, Ch 2	–1.551	1.316		
–43 dBVrms, Ch 1	–13.823	5.088		
–43 dBVrms, Ch 2	–13.823	5.088		
–53 dBVrms, Ch 1	–30.116	10.896		
–53 dBVrms, Ch 2	–30.116	10.896		

Serial Number:_____Report Number:_____
Test Date:___/___/___

A-Weight Filter

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Ch 1, 10 Hz	–5	2		
Ch 2, 10 Hz	–5	2		
Ch 1, 31.62 Hz	–1	1		
Ch 2, 31.62 Hz	–1	1		
Ch 1, 100 Hz	–0.7	0.7		
Ch 2, 100 Hz	–0.7	0.7		
Ch 1, 1000 Hz	–0.7	0.7		
Ch 2, 1000 Hz	–0.7	0.7		
Ch 1, 10000 Hz	–3	2		
Ch 2, 10000 Hz	–3	2		
Ch 1, 25120 Hz	–4.5	2.4		
Ch 2, 25120 Hz	–4.5	2.4		

Channel Match

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Two Ch, 2/1, 7 dBV FS Mag	–0.04 dB	0.04 dB	dB	
Two Ch, 2/1, 7 dBV FS Phs	–0.5 deg	0.5 deg	deg	
Two Ch, 2/1, –13 dBV FS Mag	–0.04 dB	0.04 dB	dB	
Two Ch, 2/1, –13 dBV FS Phs	–0.5 deg	0.5 deg	deg	
Two Ch, 2/1, –33 dBV FS Mag	–0.04 dB	0.04 dB	dB	
Two Ch, 2/1, –33 dBV FS Phs	–0.5 deg	0.5 deg	deg	
Two Ch, 2/1, 7 dBV –20dBfs Mag	–0.08 dB	0.08 dB	dB	
Two Ch, 2/1, 7 dBV –20dBfs Phs	–0.5 deg	0.5 deg	deg	

Serial Number:_____Report Number:_____
Test Date:___/___/___

Frequency Accuracy

Measurement	Lower Limit (kHz)	Upper Limit (kHz)	Measured Value (kHz)	Pass/Fail
50 kHz	49.9985	50.0015		

Anti-Alias Filter

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
One Ch, Ch 1, 102.4 kHz		–80		
Two Ch, Ch 1, 51.2 kHz		–80		
Two Ch, Ch 2, 51.2 kHz		–80		

Input Coupling

Measurement	Lower Limit	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
dc - ac, Ch 1		3		
dc - ac, Ch 2		3		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Harmonic Distortion

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
Single, 12.25 kHz 2nd, Ch 1		–80		
Two Ch, 12.25 kHz 2nd, Ch 1		–80		
Two Ch, 12.25 kHz 2nd, Ch 2		–80		
Single, 8.167 kHz 3rd, Ch 1		–80		
Two Ch, 8.167 kHz 3rd, Ch 1		–80		
Two Ch, 8.167 kHz 3rd, Ch 2		–80		
Single, 6.125 kHz 4th, Ch 1		–80		
Two Ch, 6.125 kHz 4th, Ch 1		–80		
Two Ch, 6.125 kHz 4th, Ch 2		–80		
Single, 4.9 kHz 5th, Ch 1		–80		
Two Ch, 4.9 kHz 5th, Ch 1		–80		
Two Ch, 4.9 kHz 5th, Ch 2		–80		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Intermodulation Distortion

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
One Ch, F1+F2, 102.4 kHz, Ch 1		–80		
One Ch, F1+F2, 64.096 kHz, Ch 1		–80		
One Ch, F1-2F2, 99.096 kHz, Ch 1		–80		
Two Ch, F1+F2, 1952 Hz, Ch 1		–80		
Two Ch, F1+F2, 1952 Hz, Ch 2		–80		
Two Ch, F1-2F2, 1048 Hz, Ch 1		–80		
Two Ch, F1-2F2, 1048 Hz, Ch 2		–80		
Two Ch, F1+F2, 48.048 kHz, Ch 1		–80		
Two Ch, F1+F2, 48.048 kHz, Ch 2		–80		
Two Ch, F1+F2, 33.024 kHz, Ch 1		–80		
Two Ch, F1+F2, 33.024 kHz, Ch 2		–80		
Two Ch, F1-2F2, 49.096 kHz, Ch 1		–80		
Two Ch, F1-2F2, 49.096 kHz, Ch 2		–80		

Cross Talk

Measurement	Lower Limit	Upper Limit (dBVrms)	Measured Value (dBVrms)	Pass/Fail
Source-to-Ch 1		–126		
Source-to-Ch 2		–126		
Receiver Ch 1, Driver Ch 2		–126		
Receiver Ch 2, Driver Ch 1		–126		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Single Ch Phase Accuracy

Measurement	Lower Limit (deg)	Upper Limit (deg)	Measured Value (deg)	Pass/Fail
Positive slope, Ch 1	–4	4		
Positive slope, Ch 2	–4	4		
Negative slope, Ch 1	–4	4		
Negative slope, Ch 2	–4	4		

External Trigger

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
8 V Pos	–10	10		
8 V Neg	–10	10		
–8 V Pos	–10	10		
–8 V Neg	–10	10		

Tach Function (option D01 only)

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
Trigger level +8V Pos	–10	10		
Trigger level +8V Neg	–10	10		
Trigger level –8V Pos	–10	10		
Trigger level –8V Neg	–10	10		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Input Resistance

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
27 dBVrms, Ch 1	–10	10		
9 dBVrms, Ch 1	–10	10		
–11 dBVrms, Ch 1	–10	10		
27 dBVrms, Ch 2	–10	10		
9 dBVrms, Ch 2	–10	10		
–11 dBVrms, Ch 2	–10	10		

ICP Supply

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Ch 1 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 2 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 1 Current	2.75 mA	5.75 mA	mA	
Ch 2 Current	2.75 mA	5.75 mA	mA	

Source Amplitude Accuracy

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
1 kHz, 0.1 Vpk	–4	4		
1 kHz, 3.0 Vpk	–4	4		
1 kHz, 5.0 Vpk	–4	4		

Source Output Resistance

Measurement	Lower Limit	Upper Limit (ohm)	Measured Value (ohm)	Pass/Fail
Resistance		5		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Source DC Offset

Measurement	Lower Limit (mVdc)	Upper Limit (mVdc)	Measured Value (mVdc)	Pass/Fail
0 Vdc, 0 Vac(pk)	–15	15		
–10 Vdc, 0 Vac(pk)	–315	315		
+10 Vdc, 0 Vac(pk)	–315	315		
–5 Vdc, 5 Vac(pk)	–315	315		
+5 Vdc, 5 Vac(pk)	–315	315		
0 Vdc, 5 Vac(pk)	–165	165		

Source Flatness

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
12.8 kHz	–1	1		
25.6 kHz	–1	1		
51.2 kHz	–1	1		
102.4 kHz	–1	1		

Source Distortion

Measurement	Lower Limit	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
12.8 kHz		–60		
51.2 kHz		–40		
102.4 kHz		–40		

Performance Test Record - Four Channel

Test Facility _____

Facility Address _____

Tested By _____

Report Number_____

Customer Name_____

Serial Number_____

Installed Options _____

Date _____

Temperature_____

Humidity _____

Power Line Frequency _____

Test Instruments Used

Instrument	Model	ID or Serial Number	Calibration Due
AC Calibrator			
Synthesizer 1			
Synthesizer 2			
Low-D Oscillator			
Multimeter			

Serial Number:_____Report Number:_____
Test Date:___/___/___

Self Test

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Long Confidence				

DC Offset

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
–51 dBVrms, Ch 1		–30		
–51 dBVrms, Ch 2		–30		
–51 dBVrms, Ch 3		–30		
–51 dBVrms, Ch 4		–30		
–35 dBVrms, Ch 1		–30		
–35 dBVrms, Ch 2		–30		
–35 dBVrms, Ch 3		–30		
–35 dBVrms, Ch 4		–30		

Noise

Measurement	Lower Limit	Upper Limit ($^{dBV}/_{\sqrt{Hz}}$)	Measured Value ($^{dBV}/_{\sqrt{Hz}}$)	Pass/Fail
Four Ch, 6.4 kHz Span, Ch 1		–130		
Four Ch, 6.4 kHz Span, Ch 2		–130		
Four Ch, 6.4 kHz Span, Ch 3		–130		
Four Ch, 6.4 kHz Span, Ch 4		–130		
Four Ch, 25.6 kHz Span, Ch 1		–140		
Four Ch, 25.6 kHz Span, Ch 2		–140		
Four Ch, 25.6 kHz Span, Ch 3		–140		
Four Ch, 25.6 kHz Span, Ch 4		–140		
Two Ch, 51.2 kHz Span, Ch 1		–140		
Two Ch, 51.2 kHz Span, Ch 2		–140		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Spurious Signals

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
Four Ch, 0 Hz Start, Ch 1		–80		
Four Ch, 0 Hz Start, Ch 2		–80		
Four Ch, 0 Hz Start, Ch 3		–80		
Four Ch, 0 Hz Start, Ch 4		–80		
Four Ch, 200 Hz Start, Ch 1		–80		
Four Ch, 200 Hz Start, Ch 2		–80		
Four Ch, 200 Hz Start, Ch 3		–80		
Four Ch, 200 Hz Start, Ch 4		–80		
Four Ch, 400 Hz Start, Ch 1		–80		
Four Ch, 400 Hz Start, Ch 2		–80		
Four Ch, 400 Hz Start, Ch 3		–80		
Four Ch, 400 Hz Start, Ch 4		–80		
Four Ch, 600 Hz Start, Ch 1		–80		
Four Ch, 600 Hz Start, Ch 2		–80		
Four Ch, 600 Hz Start, Ch 3		–80		
Four Ch, 600 Hz Start, Ch 4		–80		
Four Ch, 800 Hz Start, Ch 1		–80		
Four Ch, 800 Hz Start, Ch 2		–80		
Four Ch, 800 Hz Start, Ch 3		–80		
Four Ch, 800 Hz Start, Ch 4		–80		
Four Ch, 1000 Hz Start, Ch 1		–80		
Four Ch, 1000 Hz Start, Ch 2		–80		
Four Ch, 1000 Hz Start, Ch 3		–80		
Four Ch, 1000 Hz Start, Ch 4		–80		
Four Ch, 1200 Hz Start, Ch 1		–80		
Four Ch, 1200 Hz Start, Ch 2		–80		
Four Ch, 1200 Hz Start, Ch 3		–80		
Four Ch, 1200 Hz Start, Ch 4		–80		

Spurious Signals (continued)

Four Ch, 1400 Hz Start, Ch 1		–80		
Four Ch, 1400 Hz Start, Ch 2		–80		
Four Ch, 1400 Hz Start, Ch 3		–80		
Four Ch, 1400 Hz Start, Ch 4		–80		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Four Ch, 1600 Hz Start, Ch 1	–80
Four Ch, 1600 Hz Start, Ch 2	–80
Four Ch, 1600 Hz Start, Ch 3	–80
Four Ch, 1600 Hz Start, Ch 4	–80
Four Ch, 3200 Hz Start, Ch 1	–80
Four Ch, 3200 Hz Start, Ch 2	–80
Four Ch, 3200 Hz Start, Ch 3	–80
Four Ch, 3200 Hz Start, Ch 4	–80
Four Ch, 4800 Hz Start, Ch 1	–80
Four Ch, 4800 Hz Start, Ch 2	–80
Four Ch, 4800 Hz Start, Ch 3	–80
Four Ch, 4800 Hz Start, Ch 4	–80
Four Ch, 6400 Hz Start, Ch 1	–80
Four Ch, 6400 Hz Start, Ch 2	–80
Four Ch, 6400 Hz Start, Ch 3	–80
Four Ch, 6400 Hz Start, Ch 4	–80
Four Ch, 8000 Hz Start, Ch 1	–80
Four Ch, 8000 Hz Start, Ch 2	–80
Four Ch, 8000 Hz Start, Ch 3	–80
Four Ch, 8000 Hz Start, Ch 4	–80
Four Ch, 9600 Hz Start, Ch 1	–80
Four Ch, 9600 Hz Start, Ch 2	–80
Four Ch, 9600 Hz Start, Ch 3	–80
Four Ch, 9600 Hz Start, Ch 4	–80
Four Ch, 11200 Hz Start, Ch 1	–80
Four Ch, 11200 Hz Start, Ch 2	–80
Four Ch, 11200 Hz Start, Ch 3	–80
Four Ch, 11200 Hz Start, Ch 4	–80
Four Ch, 12800 Hz Start, Ch 1	–80
Four Ch, 12800 Hz Start, Ch 2	–80
Four Ch, 12800 Hz Start, Ch 3	–80
Four Ch, 12800 Hz Start, Ch 4	–80
Four Ch, 14400 Hz Start, Ch 1	–80
Four Ch, 14400 Hz Start, Ch 2	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Four Ch, 14400 Hz Start, Ch 3	–80
Four Ch, 14400 Hz Start, Ch 4	–80
Four Ch, 16000 Hz Start, Ch 1	–80
Four Ch, 16000 Hz Start, Ch 2	–80
Four Ch, 16000 Hz Start, Ch 3	–80
Four Ch, 16000 Hz Start, Ch 4	–80
Four Ch, 17600 Hz Start, Ch 1	–80
Four Ch, 17600 Hz Start, Ch 2	–80
Four Ch, 17600 Hz Start, Ch 3	–80
Four Ch, 17600 Hz Start, Ch 4	–80
Four Ch, 19200 Hz Start, Ch 1	–80
Four Ch, 19200 Hz Start, Ch 2	–80
Four Ch, 19200 Hz Start, Ch 3	–80
Four Ch, 19200 Hz Start, Ch 4	–80
Four Ch, 20800 Hz Start, Ch 1	–80
Four Ch, 20800 Hz Start, Ch 2	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Spurious Signals (continued)

Four Ch, 20800 Hz Start, Ch 3	–80
Four Ch, 20800 Hz Start, Ch 4	–80
Four Ch, 22400 Hz Start, Ch 1	–80
Four Ch, 22400 Hz Start, Ch 2	–80
Four Ch, 22400 Hz Start, Ch 3	–80
Four Ch, 22400 Hz Start, Ch 4	–80
Four Ch, 24000 Hz Start, Ch 1	–80
Four Ch, 24000 Hz Start, Ch 2	–80
Four Ch, 24000 Hz Start, Ch 3	–80
Four Ch, 24000 Hz Start, Ch 4	–80
Two Ch, 25600 Hz Start, Ch 1	–80
Two Ch, 25600 Hz Start, Ch 2	–80
Two Ch, 27200 Hz Start, Ch 1	–80
Two Ch, 27200 Hz Start, Ch 2	–80
Two Ch, 28800 Hz Start, Ch 1	–80
Two Ch, 28800 Hz Start, Ch 2	–80
Two Ch, 30400 Hz Start, Ch 1	–80
Two Ch, 30400 Hz Start, Ch 2	–80
Two Ch, 32000 Hz Start, Ch 1	–80
Two Ch, 32000 Hz Start, Ch 2	–80
Two Ch, 33600 Hz Start, Ch 1	–80
Two Ch, 33600 Hz Start, Ch 2	–80
Two Ch, 35200 Hz Start, Ch 1	–80
Two Ch, 35200 Hz Start, Ch 2	–80
Two Ch, 36800 Hz Start, Ch 1	–80
Two Ch, 36800 Hz Start, Ch 2	–80
Two Ch, 38400 Hz Start, Ch 1	–80
Two Ch, 38400 Hz Start, Ch 2	–80
Two Ch, 40000 Hz Start, Ch 1	–80
Two Ch, 40000 Hz Start, Ch 2	–80
Two Ch, 41600 Hz Start, Ch 1	–80
Two Ch, 41600 Hz Start, Ch 2	–80
Two Ch, 43200 Hz Start, Ch 1	–80
Two Ch, 43200 Hz Start, Ch 2	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Two Ch, 44800 Hz Start, Ch 1	–80
Two Ch, 44800 Hz Start, Ch 2	–80
Two Ch, 46400 Hz Start, Ch 1	–80
Two Ch, 46400 Hz Start, Ch 2	–80
Two Ch, 48000 Hz Start, Ch 1	–80
Two Ch, 48000 Hz Start, Ch 2	–80
Two Ch, 49600 Hz Start, Ch 1	–80
Two Ch, 49600 Hz Start, Ch 2	–80

Amplitude Accuracy

Measurement	Lower Limit (dBVrms)	Upper Limit (dBVrms)	Measured Value (dBVrms)	Pass/Fail
–51 dBVrms, Ch 1	–51.15	–50.85		
–51 dBVrms, Ch 2	–51.15	–50.85		
–51 dBVrms, Ch 3	–51.15	–50.85		
–51 dBVrms, Ch 4	–51.15	–50.85		
–43 dBVrms, Ch 1	–43.15	–42.85		
–43 dBVrms, Ch 2	–43.15	–42.85		
–43 dBVrms, Ch 3	–43.15	–42.85		
–43 dBVrms, Ch 4	–43.15	–42.85		
–35 dBVrms, Ch 1	–35.15	–34.85		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Amplitude Accuracy (continued)

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
–35 dBVrms, Ch 2	–35.15	–34.85		
–35 dBVrms, Ch 3	–35.15	–34.85		
–35 dBVrms, Ch 4	–35.15	–34.85		
–27 dBVrms, Ch 1	–27.15	–26.85		
–27 dBVrms, Ch 2	–27.15	–26.85		
–27 dBVrms, Ch 3	–27.15	–26.85		
–27 dBVrms, Ch 4	–27.15	–26.85		
–11 dBVrms, Ch 1	–11.15	–10.85		
–11 dBVrms, Ch 2	–11.15	–10.85		
–11 dBVrms, Ch 3	–11.15	–10.85		
–11 dBVrms, Ch 4	–11.15	–10.85		
1 dBVrms, Ch 1	0.85	1.15		
1 dBVrms, Ch 2	0.85	1.15		
1 dBVrms, Ch 3	0.85	1.15		
1 dBVrms, Ch 4	0.85	1.15		
9 dBVrms, Ch 1	8.85	9.15		
9 dBVrms, Ch 2	8.85	9.15		
9 dBVrms, Ch 3	8.85	9.15		
9 dBVrms, Ch 4	8.85	9.15		
19 dBVrms, Ch 1	18.85	19.15		
19 dBVrms, Ch 2	18.85	19.15		
19 dBVrms, Ch 3	18.85	19.15		
19 dBVrms, Ch 4	18.85	19.15		
27 dBVrms, Ch 1	26.85	27.15		
27 dBVrms, Ch 2	26.85	27.15		
27 dBVrms, Ch 3	26.85	27.15		
27 dBVrms, Ch 4	26.85	27.15		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Flatness

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
27 dBVrms, 51.2 kHz, One Ch, Ch 1	–0.2	0.2		
9 dBVrms, 51.2 kHz, One Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 51.2 kHz, One Ch, Ch 1	–0.2	0.2		
27 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
27 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
9 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
9 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
–11 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
27 dBVrms, 25.6 kHz, Four Ch, Ch 1	–0.2	0.2		
27 dBVrms, 25.6 kHz, Four Ch, Ch 2	–0.2	0.2		
27 dBVrms, 25.6 kHz, Four Ch, Ch 3	–0.2	0.2		
27 dBVrms, 25.6 kHz, Four Ch, Ch 4	–0.2	0.2		
9 dBVrms, 25.6 kHz, Four Ch, Ch 1	–0.2	0.2		
9 dBVrms, 25.6 kHz, Four Ch, Ch 2	–0.2	0.2		
9 dBVrms, 25.6 kHz, Four Ch, Ch 3	–0.2	0.2		
9 dBVrms, 25.6 kHz, Four Ch, Ch 4	–0.2	0.2		
–11 dBVrms, 25.6 kHz, Four Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 25.6 kHz, Four Ch, Ch 2	–0.2	0.2		
–11 dBVrms, 25.6 kHz, Four Ch, Ch 3	–0.2	0.2		
–11 dBVrms, 25.6 kHz, Four Ch, Ch 4	–0.2	0.2		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Amplitude Linearity

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
13 dBVrms, Ch 1	–0.0615	0.061		
13 dBVrms, Ch 2	–0.0615	0.061		
13 dBVrms, Ch 3	–0.0615	0.061		
13 dBVrms, Ch 4	–0.0615	0.061		
–1 dBVrms, Ch 1	–0.105	0.104		
–1 dBVrms, Ch 2	–0.105	0.104		
–1 dBVrms, Ch 3	–0.105	0.104		
–1 dBVrms, Ch 4	–0.105	0.104		
–15 dBVrms, Ch 1	–0.33	0.318		
–15 dBVrms, Ch 2	–0.33	0.318		
–15 dBVrms, Ch 3	–0.33	0.318		
–15 dBVrms, Ch 4	–0.33	0.318		
–29 dBVrms, Ch 1	–1.551	1.316		
–29 dBVrms, Ch 2	–1.551	1.316		
–29 dBVrms, Ch 3	–1.551	1.316		
–29 dBVrms, Ch 4	–1.551	1.316		
–43 dBVrms, Ch 1	–13.823	5.088		
–43 dBVrms, Ch 2	–13.823	5.088		
–43 dBVrms, Ch 3	–13.823	5.088		
–43 dBVrms, Ch 4	–13.823	5.088		
–53 dBVrms, Ch 1	–30.116	10.896		
–53 dBVrms, Ch 2	–30.116	10.896		
–53 dBVrms, Ch 3	–30.116	10.896		
–53 dBVrms, Ch 4	–30.116	10.896		

Serial Number:_____Report Number:_____
Test Date:___/___/___

A-Weight Filter

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Ch 1, 10 Hz	–5	2		
Ch 2, 10 Hz	–5	2		
Ch 3, 10 Hz	–5	2		
Ch 4, 10 Hz	–5	2		
Ch 1, 31.62 Hz	–1	1		
Ch 2, 31.62 Hz	–1	1		
Ch 3, 31.62 Hz	–1	1		
Ch 4, 31.62 Hz	–1	1		
Ch 1, 100 Hz	–0.7	0.7		
Ch 2, 100 Hz	–0.7	0.7		
Ch 3, 100 Hz	–0.7	0.7		
Ch 4, 100 Hz	–0.7	0.7		
Ch 1, 1000 Hz	–0.7	0.7		
Ch 2, 1000 Hz	–0.7	0.7		
Ch 3, 1000 Hz	–0.7	0.7		
Ch 4, 1000 Hz	–0.7	0.7		
Ch 1, 10000 Hz	–3	2		
Ch 2, 10000 Hz	–3	2		
Ch 3, 10000 Hz	–3	2		
Ch 4, 10000 Hz	–3	2		
Ch 1, 25120 Hz	–4.5	2.4		
Ch 2, 25120 Hz	–4.5	2.4		
Ch 3, 25120 Hz	–4.5	2.4		
Ch 4, 25120 Hz	–4.5	2.4		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Channel Match

Two Ch, 2/1, 7 dBV FS Mag	–0.04	0.04
Two Ch, 2/1, 7 dBV FS Phs	–0.5	0.5
Two Ch, 2/1, –13 dBV FS Mag	–0.04	0.04
Two Ch, 2/1, –13 dBV FS Phs	–0.5	0.5
Two Ch, 2/1, –33 dBV FS Mag	–0.04	0.04
Two Ch, 2/1, –33 dBV FS Phs	–0.5	0.5
Two Ch, 2/1, 7 dBV –20 dBfs Mag	–0.08	0.08
Two Ch, 2/1, 7 dBV –20 dBfs Phs	–0.5	0.5
Four Ch, 2/1, 7 dBV FS Mag	–0.04	0.04
Four Ch, 2/1, 7 dBV FS Phs	–0.5	0.5
Four Ch, 2/1, –13 dBV FS Mag	–0.04	0.04
Four Ch, 2/1, –13 dBV FS Phs	–0.5	0.5
Four Ch, 2/1, –33 dBV FS Mag	–0.04	0.04
Four Ch, 2/1, –33 dBV FS Phs	–0.5	0.5
Four Ch, 2/1, 7 dBV –20 dBfs Mag	–0.08	0.08
Four Ch, 2/1, 7 dBV –20 dBfs Phs	–0.5	0.5
Four Ch, 3/1, 7 dBV FS Mag	–0.04	0.04
Four Ch, 3/1, 7 dBV FS Phs	–0.5	0.5
Four Ch, 3/1, –13 dBV FS Mag	–0.04	0.04
Four Ch, 3/1, –13 dBV FS Phs	–0.5	0.5
Four Ch, 3/1, –33 dBV FS Mag	–0.04	0.04
Four Ch, 3/1, –33 dBV FS Phs	–0.5	0.5
Four Ch, 3/1, 7 dBV –20 dBfs Mag	–0.08	0.08
Four Ch, 3/1, 7 dBV –20 dBfs Phs	–0.5	0.5
Four Ch, 4/1, 7 dBV FS Mag	–0.04	0.04
Four Ch, 4/1, 7 dBV FS Phs	–0.5	0.5
Four Ch, 4/1, –13 dBV FS Mag	–0.04	0.04
Four Ch, 4/1, –13 dBV FS Phs	–0.5	0.5
Four Ch, 4/1, –33 dBV FS Mag	–0.04	0.04
Four Ch, 4/1, –33 dBV FS Phs	–0.5	0.5
Four Ch, 4/1, 7 dBV –20 dBfs Mag	–0.08	0.08
Four Ch, 4/1, 7 dBV –20 dBfs Phs	–0.5	0.5
Four Ch, 4/3, 7 dBV FS Mag	–0.04	0.04

Serial Number:_____Report Number:_____
Test Date:___/___/___

Four Ch, 4/3, 7 dBV FS Phs	–0.5	0.5
Four Ch, 4/3, –13 dBV FS Mag	–0.04	0.04
Four Ch, 4/3, –13 dBV FS Phs	–0.5	0.5
Four Ch, 4/3, –33 dBV FS Mag	–0.04	0.04
Four Ch, 4/3, –33 dBV FS Phs	–0.5	0.5
Four Ch, 4/3, 7 dBV –20 dBfs Mag	–0.08	0.08
Four Ch, 4/3, 7 dBV –20 dBfs Phs	–0.5	0.5

Serial Number:_____Report Number:_____
Test Date:___/___/___

Frequency Accuracy

Measurement	Lower Limit (kHz)	Upper Limit (kHz)	Measured Value (kHz)	Pass/Fail
50 kHz	49.9985	50.0015		

Anti-Alias Filter

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
One Ch, Ch 1, 51.2 kHz		–80		
Two Ch, Ch 1, 51.2 kHz		–80		
Two Ch, Ch 2, 51.2 kHz		–80		
Four Ch, Ch 1, 25.6 kHz		–80		
Four Ch, Ch 2, 25.6 kHz		–80		
Four Ch, Ch 3, 25.6 kHz		–80		
Four Ch, Ch 4, 25.6 kHz		–80		

Input Coupling

Measurement	Lower Limit	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
dc - ac, Ch 1		3		
dc - ac, Ch 2		3		
dc - ac, Ch 3		3		
dc - ac, Ch 4		3		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Harmonic Distortion

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
Two Ch, 12.25 kHz 2nd, Ch 1		–80		
Two Ch, 12.25 kHz 2nd, Ch 2		–80		
Four Ch, 12.25 kHz 2nd, Ch 1		–80		
Four Ch, 12.25 kHz 2nd, Ch 2		–80		
Four Ch, 12.25 kHz 2nd, Ch 3		–80		
Four Ch, 12.25 kHz 2nd, Ch 4		–80		
Two Ch, 8.167 kHz 3rd, Ch 1		–80		
Two Ch, 8.167 kHz 3rd, Ch 2		–80		
Four Ch, 8.167 kHz 3rd, Ch 1		–80		
Four Ch, 8.167 kHz 3rd, Ch 2		–80		
Four Ch, 8.167 kHz 3rd, Ch 3		–80		
Four Ch, 8.167 kHz 3rd, Ch 4		–80		
Two Ch, 6.125 kHz 4th, Ch 1		–80		
Two Ch, 6.125 kHz 4th, Ch 2		–80		
Four Ch, 6.125 kHz 4th, Ch 1		–80		
Four Ch, 6.125 kHz 4th, Ch 2		–80		
Four Ch, 6.125 kHz 4th, Ch 3		–80		
Four Ch, 6.125 kHz 4th, Ch 4		–80		
Two Ch, 4.9 kHz 5th, Ch 1		–80		
Two Ch, 4.9 kHz 5th, Ch 2		–80		
Four Ch, 4.9 kHz 5th, Ch 1		–80		
Four Ch, 4.9 kHz 5th, Ch 2		–80		
Four Ch, 4.9 kHz 5th, Ch 3		–80		
Four Ch, 4.9 kHz 5th, Ch 4		–80		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Intermodulation Distortion

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
Two Ch, F1+F2, 1952 Hz, Ch 1		–80		
Two Ch, F1+F2, 1952 Hz, Ch 2		–80		
Two Ch, F1–2F2, 1048 Hz, Ch 1		–80		
Two Ch, F1–2F2, 1048 Hz, Ch 2		–80		
Two Ch, F1+F2, 48.048 kHz, Ch 1		–80		
Two Ch, F1+F2, 48.048 kHz, Ch 2		–80		
Two Ch, F1+F2, 33.024 kHz, Ch 1		–80		
Two Ch, F1+F2, 33.024 kHz, Ch 2		–80		
Two Ch, F1–2F2, 49.096 kHz, Ch 1		–80		
Two Ch, F1–2F2, 49.096 kHz, Ch 2		–80		
Four Ch, F1+F2, 1952 Hz, Ch 1		–80		
Four Ch, F1+F2, 1952 Hz, Ch 2		–80		
Four Ch, F1+F2, 1952 Hz, Ch 3		–80		
Four Ch, F1+F2, 1952 Hz, Ch 4		–80		
Four Ch, F1–2F2, 1048 Hz, Ch 1		–80		
Four Ch, F1–2F2, 1048 Hz, Ch 2		–80		
Four Ch, F1–2F2, 1048 Hz, Ch 3		–80		
Four Ch, F1–2F2, 1048 Hz, Ch 4		–80		
Four Ch, F1+F2, 24048 Hz, Ch 1		–80		
Four Ch, F1+F2, 24048 Hz, Ch 2		–80		
Four Ch, F1+F2, 24048 Hz, Ch 3		–80		
Four Ch, F1+F2, 24048 Hz, Ch 4		–80		
Four Ch, F1+F2, 17488 Hz, Ch 1		–80		
Four Ch, F1+F2, 17488 Hz, Ch 2		–80		
Four Ch, F1+F2, 17488 Hz, Ch 3		–80		
Four Ch, F1+F2, 17488 Hz, Ch 4		–80		
Four Ch, F1–2F2, 24096 Hz, Ch 1		–80		
Four Ch, F1–2F2, 24096 Hz, Ch 2		–80		
Four Ch, F1–2F2, 24096 Hz, Ch 3		–80		
Four Ch, F1–2F2, 24096 Hz, Ch 4		–80		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Cross Talk

Measurement	Lower Limit	Upper Limit (dBVrms)	Measured Value (dBVrms)	Pass/Fail
Source-to-Ch 1		–126		
Source-to-Ch 2		–126		
Source-to-Ch 3		–126		
Source-to-Ch 4		–126		
Receiver Ch 1, Driver Ch 2, 3, 4		–126		
Receiver Ch 2, Driver Ch 1, 3, 4		–126		
Receiver Ch 3, Driver Ch 1, 2, 4		–126		
Receiver Ch 4, Driver Ch 1, 2, 3		–126		

Single Ch Phase Accuracy

Measurement	Lower Limit (deg)	Upper Limit (deg)	Measured Value (deg)	Pass/Fail
Positive slope, Ch 1	–4	4		
Positive slope, Ch 2	–4	4		
Positive slope, Ch 3	–4	4		
Positive slope, Ch 4	–4	4		
Negative slope, Ch 1	–4	4		
Negative slope, Ch 2	–4	4		
Negative slope, Ch 3	–4	4		
Negative slope, Ch 4	–4	4		

Serial Number:_____Report Number:_____
Test Date:___/___/___

External Trigger

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
8 V Pos	–10	10		
8 V Neg	–10	10		
–8 V Pos	–10	10		
–8 V Neg	–10	10		

Tach Function (option D01 only)

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
Trigger level +8V Pos	–10	10		
Trigger level +8V Neg	–10	10		
Trigger level –8V Pos	–10	10		
Trigger level –8V Neg	–10	10		

Input Resistance

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
27 dBVrms, Ch 1	–10	10		
9 dBVrms, Ch 1	–10	10		
–11 dBVrms, Ch 1	–10	10		
27 dBVrms, Ch 2	–10	10		
9 dBVrms, Ch 2	–10	10		
–11 dBVrms, Ch 2	–10	10		
27 dBVrms, Ch 3	–10	10		
9 dBVrms, Ch 3	–10	10		
–11 dBVrms, Ch 3	–10	10		
27 dBVrms, Ch 4	–10	10		
9 dBVrms, Ch 4	–10	10		
–11 dBVrms, Ch 4	–10	10		

ICP Supply

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Ch 1 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 2 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 31 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 4 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 1 Current	2.75 mA	5.75 mA	mA	

Serial Number:_____Report Number:_____
Test Date:___/___/___

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Ch 2 Current	2.75 mA	5.75 mA	mA	
Ch 3 Current	2.75 mA	5.75 mA	mA	
Ch 4 Current	2.75 mA	5.75 mA	mA	

Source Amplitude Accuracy

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
1 kHz, 0.1 Vpk	–4	4		
1 kHz, 3.0 Vpk	–4	4		
1 kHz, 5.0 Vpk	–4	4		

Source Output Resistance

Measurement	Lower Limit	Upper Limit (ohm)	Measured Value (ohm)	Pass/Fail
Resistance		5		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Source DC Offset

Measurement	Lower Limit (mVdc)	Upper Limit (mVdc)	Measured Value (mVdc)	Pass/Fail
0 Vdc, 0 Vac(pk)	–15	15		
–10 Vdc, 0 Vac(pk)	–315	315		
+10 Vdc, 0 Vac(pk)	–315	315		
–5 Vdc, 5 Vac(pk)	–315	315		
+5 Vdc, 5 Vac(pk)	–315	315		
0 Vdc, 5 Vac(pk)	–165	165		

Source Flatness

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
12.8 kHz	–1	1		
25.6 kHz	–1	1		
51.2 kHz	–1	1		

Source Distortion

Measurement	Lower Limit	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
12.8 kHz		–60		
51.2 kHz		–40		

Operation Verification Test Record - Two Channel

Test Facility _____

Facility Address _____

Tested By _____

Report Number _____

Customer Name _____

Serial Number _____

Installed Options _____

Date _____

Temperature _____

Humidity _____

Power Line Frequency _____

Test Instruments Used

Instrument	Model	ID or Serial Number	Calibration Due
AC Calibrator			
Synthesizer 1			
Synthesizer 2			
Low-D Oscillator			
Multimeter			

Serial Number:_____Report Number:_____
Test Date:___/___/___

Self Test

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Long Confidence				

DC Offset

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
–51 dBVrms, Ch 1		–15		
–51 dBVrms, Ch 2		–15		
–35 dBVrms, Ch 1		–30		
–35 dBVrms, Ch 2		–30		

Noise

Measurement	Lower Limit	Upper Limit ($^{dBV}/_{\sqrt{Hz}}$)	Measured Value ($^{dBV}/_{\sqrt{Hz}}$)	Pass/Fail
Two Ch, 6.4 kHz Span, Ch 1		–130		
Two Ch, 6.4 kHz Span, Ch 2		–130		
Two Ch, 51.2 kHz Span, Ch 1		–140		
Two Ch, 51.2 kHz Span, Ch 2		–140		
One Ch, 102.4 kHz Span, Ch 1		–140		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Spurious Signals

Two Ch, 0 Hz Start, Ch 1	–80
Two Ch, 0 Hz Start, Ch 2	–80
Two Ch, 200 Hz Start, Ch 1	–80
Two Ch, 200 Hz Start, Ch 2	–80
Two Ch, 400 Hz Start, Ch 1	–80
Two Ch, 400 Hz Start, Ch 2	–80
Two Ch, 600 Hz Start, Ch 1	–80
Two Ch, 600 Hz Start, Ch 2	–80
Two Ch, 800 Hz Start, Ch 1	–80
Two Ch, 800 Hz Start, Ch 2	–80
Two Ch, 1000 Hz Start, Ch 1	–80
Two Ch, 1000 Hz Start, Ch 2	–80
Two Ch, 1200 Hz Start, Ch 1	–80
Two Ch, 1200 Hz Start, Ch 2	–80
Two Ch, 1400 Hz Start, Ch 1	–80
Two Ch, 1400 Hz Start, Ch 2	–80
Two Ch, 1600 Hz Start, Ch 1	–80
Two Ch, 1600 Hz Start, Ch 2	–80
Two Ch, 3200 Hz Start, Ch 1	–80
Two Ch, 3200 Hz Start, Ch 2	–80
Two Ch, 4800 Hz Start, Ch 1	–80
Two Ch, 4800 Hz Start, Ch 2	–80
Two Ch, 6400 Hz Start, Ch 1	–80
Two Ch, 6400 Hz Start, Ch 2	–80
Two Ch, 8000 Hz Start, Ch 1	–80
Two Ch, 8000 Hz Start, Ch 2	–80
Two Ch, 9600 Hz Start, Ch 1	–80
Two Ch, 9600 Hz Start, Ch 2	–80
Two Ch, 11200 Hz Start, Ch 1	–80
Two Ch, 11200 Hz Start, Ch 2	–80
Two Ch, 12800 Hz Start, Ch 1	–80
Two Ch, 12800 Hz Start, Ch 2	–80
Two Ch, 14400 Hz Start, Ch 1	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Two Ch, 14400 Hz Start, Ch 2	–80
Two Ch, 16000 Hz Start, Ch 1	–80
Two Ch, 16000 Hz Start, Ch 2	–80
Two Ch, 17600 Hz Start, Ch 1	–80
Two Ch, 17600 Hz Start, Ch 2	–80
Two Ch, 19200 Hz Start, Ch 1	–80
Two Ch, 19200 Hz Start, Ch 2	–80
Two Ch, 20800 Hz Start, Ch 1	–80
Two Ch, 20800 Hz Start, Ch 2	–80
Two Ch, 22400 Hz Start, Ch 1	–80
Two Ch, 22400 Hz Start, Ch 2	–80
Two Ch, 24000 Hz Start, Ch 1	–80
Two Ch, 24000 Hz Start, Ch 2	–80
Two Ch, 25600 Hz Start, Ch 1	–80
Two Ch, 25600 Hz Start, Ch 2	–80
Two Ch, 27200 Hz Start, Ch 1	–80
Two Ch, 27200 Hz Start, Ch 2	–80
Two Ch, 28800 Hz Start, Ch 1	–80
Two Ch, 28800 Hz Start, Ch 2	–80
Two Ch, 30400 Hz Start, Ch 1	–80
Two Ch, 30400 Hz Start, Ch 2	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Spurious Signals (continued)

Two Ch, 32000 Hz Start, Ch 1	–80
Two Ch, 32000 Hz Start, Ch 2	–80
Two Ch, 33600 Hz Start, Ch 1	–80
Two Ch, 33600 Hz Start, Ch 2	–80
Two Ch, 35200 Hz Start, Ch 1	–80
Two Ch, 35200 Hz Start, Ch 2	–80
Two Ch, 36800 Hz Start, Ch 1	–80
Two Ch, 36800 Hz Start, Ch 2	–80
Two Ch, 38400 Hz Start, Ch 1	–80
Two Ch, 38400 Hz Start, Ch 2	–80
Two Ch, 40000 Hz Start, Ch 1	–80
Two Ch, 40000 Hz Start, Ch 2	–80
Two Ch, 41600 Hz Start, Ch 1	–80
Two Ch, 41600 Hz Start, Ch 2	–80
Two Ch, 43200 Hz Start, Ch 1	–80
Two Ch, 43200 Hz Start, Ch 2	–80
Two Ch, 44800 Hz Start, Ch 1	–80
Two Ch, 44800 Hz Start, Ch 2	–80
Two Ch, 46400 Hz Start, Ch 1	–80
Two Ch, 46400 Hz Start, Ch 2	–80
Two Ch, 48000 Hz Start, Ch 1	–80
Two Ch, 48000 Hz Start, Ch 2	–80
Two Ch, 49600 Hz Start, Ch 1	–80
Two Ch, 49600 Hz Start, Ch 2	–80
One Ch, 79200 Start, Ch 1	–80
One Ch, 80800 Start, Ch 1	–80
One Ch, 85600 Start, Ch 1	–80
One Ch, 87200 Start, Ch 1	–80
One Ch, 88800 Start, Ch 1	–80
One Ch, 97000 Start, Ch 1	–80
One Ch, 98600 Start, Ch 1	–80
One Ch, 100200 Start, Ch 1	–80
One Ch, 101800 Start, Ch 1	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Amplitude Accuracy

Measurement	Lower Limit (dBVrms)	Upper Limit (dBVrms)	Measured Value (dBVrms)	Pass/Fail
–51 dBVrms, Ch 1	–51.15	–50.85		
–51 dBVrms, Ch 2	–51.15	–50.85		
–43 dBVrms, Ch 1	–43.15	–42.85		
–43 dBVrms, Ch 2	–43.15	–42.85		
–35 dBVrms, Ch 1	–35.15	–34.85		
–35 dBVrms, Ch 2	–35.15	–34.85		
–27 dBVrms, Ch 1	–27.15	–26.85		
–27 dBVrms, Ch 2	–27.15	–26.85		
–11 dBVrms, Ch 1	–11.15	–10.85		
–11 dBVrms, Ch 2	–11.15	–10.85		
1 dBVrms, Ch 1	0.85	1.15		
1 dBVrms, Ch 2	0.85	1.15		
9 dBVrms, Ch 1	8.85	9.15		
9 dBVrms, Ch 2	8.85	9.15		
19 dBVrms, Ch 1	18.85	19.15		
19 dBVrms, Ch 2	18.85	19.15		
27 dBVrms, Ch 1	26.85	27.15		
27 dBVrms, Ch 2	26.85	27.15		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Flatness

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
27 dBVrms, 99.84 kHz, One Ch, Ch 1	–0.2	0.2		
9 dBVrms, 99.84 kHz, One Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 99.84 kHz, One Ch, Ch 1	–0.2	0.2		
27 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
27 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
9 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
9 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
–11 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		

Amplitude Linearity

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
13 dBVrms, Ch 1	–0.0615	0.061		
13 dBVrms, Ch 2	–0.0615	0.061		
–1 dBVrms, Ch 1	–0.105	0.104		
–1 dBVrms, Ch 2	–0.105	0.104		
–15 dBVrms, Ch 1	–0.33	0.318		
–15 dBVrms, Ch 2	–0.33	0.318		
–29 dBVrms, Ch 1	–1.551	1.316		
–29 dBVrms, Ch 2	–1.551	1.316		
–43 dBVrms, Ch 1	–13.823	5.088		
–43 dBVrms, Ch 2	–13.823	5.088		
–53 dBVrms, Ch 1	–30.116	10.896		
–53 dBVrms, Ch 2	–30.116	10.896		

A Weight Filter

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Ch 1, 10 Hz	–5	2		
Ch 2, 10 Hz	–5	2		
Ch 1, 31.62 Hz	–1	1		
Ch 2, 31.62 Hz	–1	1		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Ch 1, 100 Hz	–0.7	0.7		
Ch 2, 100 Hz	–0.7	0.7		
Ch 1, 1000 Hz	–0.7	0.7		
Ch 2, 1000 Hz	–0.7	0.7		
Ch 1, 10000 Hz	–3	2		
Ch 2, 10000 Hz	–3	2		
Ch 1, 25120 Hz	–4.5	2.4		
Ch 2, 25120 Hz	–4.5	2.4		

Channel Match

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Two Ch, 2/1, 7 dBV FS Mag	–0.04 dB	0.04 dB	dB	
Two Ch, 2/1, 7 dBV FS Phs	–0.5 deg	0.5 deg	deg	
Two Ch, 2/1, –13 dBV FS Mag	–0.04 dB	0.04 dB	dB	
Two Ch, 2/1, –13 dBV FS Phs	–0.5 deg	0.5 deg	deg	
Two Ch, 2/1, –33 dBV FS Mag	–0.04 dB	0.04 dB	dB	
Two Ch, 2/1, –33 dBV FS Phs	–0.5 deg	0.5 deg	deg	
Two Ch, 2/1, 7 dBV –20dBfs Mag	–0.08 dB	0.08 dB	dB	
Two Ch, 2/1, 7 dBV –20dBfs Phs	–0.5 deg	0.5 deg	deg	

Serial Number:_____Report Number:_____
Test Date:___/___/___

Frequency Accuracy

Measurement	Lower Limit (kHz)	Upper Limit (kHz)	Measured Value (kHz)	Pass/Fail
50 kHz	49.9985	50.0015		

Single Ch Phase Accuracy

Measurement	Lower Limit (deg)	Upper Limit (deg)	Measured Value (deg)	Pass/Fail
Positive slope, Ch 1	–4	4		
Positive slope, Ch 2	–4	4		
Negative slope, Ch 1	–4	4		
Negative slope, Ch 2	–4	4		

Tach Function (option D01 only)

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
Trigger level +8V Pos	–10	10		
Trigger level +8V Neg	–10	10		
Trigger level –8V Pos	–10	10		
Trigger level –8V Neg	–10	10		

Serial Number:_____Report Number:_____
Test Date:___/___/___

ICP Supply

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Ch 1 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 2 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 1 Current	2.75 mA	5.75 mA	mA	
Ch 2 Current	2.75 mA	5.75 mA	mA	

Source Amplitude Accuracy

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
1 kHz, 0.1 Vpk	–4	4		
1 kHz, 3.0 Vpk	–4	4		
1 kHz, 5.0 Vpk	–4	4		

Source Flatness

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
12.8 kHz	–1	1		
25.6 kHz	–1	1		
51.2 kHz	–1	1		
102.4 kHz	–1	1		

Source Distortion

Measurement	Lower Limit	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
12.8 kHz		–60		
51.2 kHz		–40		
102.4 kHz		–40		

Operation Verification Test Record - Four Channel

Test Facility _____

Facility Address _____

Tested By _____

Report Number _____

Customer Name _____

Serial Number _____

Installed Options _____

Date _____

Temperature _____

Humidity _____

Power Line Frequency _____

Test Instruments Used

Instrument	Model	ID or Serial Number	Calibration Due
AC Calibrator			
Synthesizer 1			
Synthesizer 2			
Low-D Oscillator			
Multimeter			

Serial Number:_____Report Number:_____
Test Date:___/___/___

Self Test

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Long Confidence				

DC Offset

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
–51 dBVrms, Ch 1		–15		
–51 dBVrms, Ch 2		–15		
–51 dBVrms, Ch 3		–15		
–51 dBVrms, Ch 4		–15		
–35 dBVrms, Ch 1		–30		
–35 dBVrms, Ch 2		–30		
–35 dBVrms, Ch 3		–30		
–35 dBVrms, Ch 4		–30		

Noise

Measurement	Lower Limit	Upper Limit ($^{dBV}/_{\sqrt{Hz}}$)	Measured Value ($^{dBV}/_{\sqrt{Hz}}$)	Pass/Fail
Four Ch, 6.4 kHz Span, Ch 1		–130		
Four Ch, 6.4 kHz Span, Ch 2		–130		
Four Ch, 6.4 kHz Span, Ch 3		–130		
Four Ch, 6.4 kHz Span, Ch 4		–130		
Four Ch, 25.6 kHz Span, Ch 1		–140		
Four Ch, 25.6 kHz Span, Ch 2		–140		
Four Ch, 25.6 kHz Span, Ch 3		–140		
Four Ch, 25.6 kHz Span, Ch 4		–140		
Two Ch, 51.2 kHz Span, Ch 1		–140		
Two Ch, 51.2 kHz Span, Ch 2		–140		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Spurious Signals

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
Four Ch, 0 Hz Start, Ch 1		–80		
Four Ch, 0 Hz Start, Ch 2		–80		
Four Ch, 0 Hz Start, Ch 3		–80		
Four Ch, 0 Hz Start, Ch 4		–80		
Four Ch, 200 Hz Start, Ch 1		–80		
Four Ch, 200 Hz Start, Ch 2		–80		
Four Ch, 200 Hz Start, Ch 3		–80		
Four Ch, 200 Hz Start, Ch 4		–80		
Four Ch, 400 Hz Start, Ch 1		–80		
Four Ch, 400 Hz Start, Ch 2		–80		
Four Ch, 400 Hz Start, Ch 3		–80		
Four Ch, 400 Hz Start, Ch 4		–80		
Four Ch, 600 Hz Start, Ch 1		–80		
Four Ch, 600 Hz Start, Ch 2		–80		
Four Ch, 600 Hz Start, Ch 3		–80		
Four Ch, 600 Hz Start, Ch 4		–80		
Four Ch, 800 Hz Start, Ch 1		–80		
Four Ch, 800 Hz Start, Ch 2		–80		
Four Ch, 800 Hz Start, Ch 3		–80		
Four Ch, 800 Hz Start, Ch 4		–80		
Four Ch, 1000 Hz Start, Ch 1		–80		
Four Ch, 1000 Hz Start, Ch 2		–80		
Four Ch, 1000 Hz Start, Ch 3		–80		
Four Ch, 1000 Hz Start, Ch 4		–80		
Four Ch, 1200 Hz Start, Ch 1		–80		
Four Ch, 1200 Hz Start, Ch 2		–80		
Four Ch, 1200 Hz Start, Ch 3		–80		
Four Ch, 1200 Hz Start, Ch 4		–80		
Four Ch, 1400 Hz Start, Ch 1		–80		
Four Ch, 1400 Hz Start, Ch 2		–80		
Four Ch, 1400 Hz Start, Ch 3		–80		
Four Ch, 1400 Hz Start, Ch 4		–80		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Four Ch, 1600 Hz Start, Ch 1	–80
Four Ch, 1600 Hz Start, Ch 2	–80
Four Ch, 1600 Hz Start, Ch 3	–80
Four Ch, 1600 Hz Start, Ch 4	–80
Four Ch, 3200 Hz Start, Ch 1	–80
Four Ch, 3200 Hz Start, Ch 2	–80
Four Ch, 3200 Hz Start, Ch 3	–80
Four Ch, 3200 Hz Start, Ch 4	–80
Four Ch, 4800 Hz Start, Ch 1	–80
Four Ch, 4800 Hz Start, Ch 2	–80
Four Ch, 4800 Hz Start, Ch 3	–80
Four Ch, 4800 Hz Start, Ch 4	–80
Four Ch, 6400 Hz Start, Ch 1	–80
Four Ch, 6400 Hz Start, Ch 2	–80
Four Ch, 6400 Hz Start, Ch 3	–80
Four Ch, 6400 Hz Start, Ch 4	–80
Four Ch, 8000 Hz Start, Ch 1	–80
Four Ch, 8000 Hz Start, Ch 2	–80
Four Ch, 8000 Hz Start, Ch 3	–80
Four Ch, 8000 Hz Start, Ch 4	–80
Four Ch, 9600 Hz Start, Ch 1	–80
Four Ch, 9600 Hz Start, Ch 2	–80
Four Ch, 9600 Hz Start, Ch 3	–80
Four Ch, 9600 Hz Start, Ch 4	–80
Four Ch, 11200 Hz Start, Ch 1	–80
Four Ch, 11200 Hz Start, Ch 2	–80
Four Ch, 11200 Hz Start, Ch 3	–80
Four Ch, 11200 Hz Start, Ch 4	–80
Four Ch, 12800 Hz Start, Ch 1	–80
Four Ch, 12800 Hz Start, Ch 2	–80
Four Ch, 12800 Hz Start, Ch 3	–80
Four Ch, 12800 Hz Start, Ch 4	–80
Four Ch, 14400 Hz Start, Ch 1	–80
Four Ch, 14400 Hz Start, Ch 2	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Four Ch, 14400 Hz Start, Ch 3	–80
Four Ch, 14400 Hz Start, Ch 4	–80
Four Ch, 16000 Hz Start, Ch 1	–80
Four Ch, 16000 Hz Start, Ch 2	–80
Four Ch, 16000 Hz Start, Ch 3	–80
Four Ch, 16000 Hz Start, Ch 4	–80
Four Ch, 17600 Hz Start, Ch 1	–80
Four Ch, 17600 Hz Start, Ch 2	–80
Four Ch, 17600 Hz Start, Ch 3	–80
Four Ch, 17600 Hz Start, Ch 4	–80
Four Ch, 19200 Hz Start, Ch 1	–80
Four Ch, 19200 Hz Start, Ch 2	–80
Four Ch, 19200 Hz Start, Ch 3	–80
Four Ch, 19200 Hz Start, Ch 4	–80
Four Ch, 20800 Hz Start, Ch 1	–80
Four Ch, 20800 Hz Start, Ch 2	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Spurious Signals (continued)

Four Ch, 20800 Hz Start, Ch 3	–80
Four Ch, 20800 Hz Start, Ch 4	–80
Four Ch, 22400 Hz Start, Ch 1	–80
Four Ch, 22400 Hz Start, Ch 2	–80
Four Ch, 22400 Hz Start, Ch 3	–80
Four Ch, 22400 Hz Start, Ch 4	–80
Four Ch, 24000 Hz Start, Ch 1	–80
Four Ch, 24000 Hz Start, Ch 2	–80
Four Ch, 24000 Hz Start, Ch 3	–80
Four Ch, 24000 Hz Start, Ch 4	–80
Two Ch, 25600 Hz Start, Ch 1	–80
Two Ch, 25600 Hz Start, Ch 2	–80
Two Ch, 27200 Hz Start, Ch 1	–80
Two Ch, 27200 Hz Start, Ch 2	–80
Two Ch, 28800 Hz Start, Ch 1	–80
Two Ch, 28800 Hz Start, Ch 2	–80
Two Ch, 30400 Hz Start, Ch 1	–80
Two Ch, 30400 Hz Start, Ch 2	–80
Two Ch, 32000 Hz Start, Ch 1	–80
Two Ch, 32000 Hz Start, Ch 2	–80
Two Ch, 33600 Hz Start, Ch 1	–80
Two Ch, 33600 Hz Start, Ch 2	–80
Two Ch, 35200 Hz Start, Ch 1	–80
Two Ch, 35200 Hz Start, Ch 2	–80
Two Ch, 36800 Hz Start, Ch 1	–80
Two Ch, 36800 Hz Start, Ch 2	–80
Two Ch, 38400 Hz Start, Ch 1	–80
Two Ch, 38400 Hz Start, Ch 2	–80
Two Ch, 40000 Hz Start, Ch 1	–80
Two Ch, 40000 Hz Start, Ch 2	–80
Two Ch, 41600 Hz Start, Ch 1	–80
Two Ch, 41600 Hz Start, Ch 2	–80
Two Ch, 43200 Hz Start, Ch 1	–80
Two Ch, 43200 Hz Start, Ch 2	–80

Serial Number:_____Report Number:_____
Test Date:___/___/___

Two Ch, 44800 Hz Start, Ch 1	–80
Two Ch, 44800 Hz Start, Ch 2	–80
Two Ch, 46400 Hz Start, Ch 1	–80
Two Ch, 46400 Hz Start, Ch 2	–80
Two Ch, 48000 Hz Start, Ch 1	–80
Two Ch, 48000 Hz Start, Ch 2	–80
Two Ch, 49600 Hz Start, Ch 1	–80
Two Ch, 49600 Hz Start, Ch 2	–80

Amplitude Accuracy

Measurement	Lower Limit (dBVrms)	Upper Limit (dBVrms)	Measured Value (dBVrms)	Pass/Fail
–51 dBVrms, Ch 1	–51.15	–50.85		
–51 dBVrms, Ch 2	–51.15	–50.85		
–51 dBVrms, Ch 3	–51.15	–50.85		
–51 dBVrms, Ch 4	–51.15	–50.85		
–43 dBVrms, Ch 1	–43.15	–42.85		
–43 dBVrms, Ch 2	–43.15	–42.85		
–43 dBVrms, Ch 3	–43.15	–42.85		
–43 dBVrms, Ch 4	–43.15	–42.85		
–35 dBVrms, Ch 1	–35.15	–34.85		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Amplitude Accuracy (continued)

Measurement	Lower Limit	Upper Limit (dBfs)	Measured Value (dBfs)	Pass/Fail
–35 dBVrms, Ch 2	–35.15	–34.85		
–35 dBVrms, Ch 3	–35.15	–34.85		
–35 dBVrms, Ch 4	–35.15	–34.85		
–27 dBVrms, Ch 1	–27.15	–26.85		
–27 dBVrms, Ch 2	–27.15	–26.85		
–27 dBVrms, Ch 3	–27.15	–26.85		
–27 dBVrms, Ch 4	–27.15	–26.85		
–11 dBVrms, Ch 1	–11.15	–10.85		
–11 dBVrms, Ch 2	–11.15	–10.85		
–11 dBVrms, Ch 3	–11.15	–10.85		
–11 dBVrms, Ch 4	–11.15	–10.85		
1 dBVrms, Ch 1	0.85	1.15		
1 dBVrms, Ch 2	0.85	1.15		
1 dBVrms, Ch 3	0.85	1.15		
1 dBVrms, Ch 4	0.85	1.15		
9 dBVrms, Ch 1	8.85	9.15		
9 dBVrms, Ch 2	8.85	9.15		
9 dBVrms, Ch 3	8.85	9.15		
9 dBVrms, Ch 4	8.85	9.15		
19 dBVrms, Ch 1	18.85	19.15		
19 dBVrms, Ch 2	18.85	19.15		
19 dBVrms, Ch 3	18.85	19.15		
19 dBVrms, Ch 4	18.85	19.15		
27 dBVrms, Ch 1	26.85	27.15		
27 dBVrms, Ch 2	26.85	27.15		
27 dBVrms, Ch 3	26.85	27.15		
27 dBVrms, Ch 4	26.85	27.15		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Flatness

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
27 dBVrms, 51.2 kHz, One Ch, Ch 1	–0.2	0.2		
9 dBVrms, 51.2 kHz, One Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 51.2 kHz, One Ch, Ch 1	–0.2	0.2		
27 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
27 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
9 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
9 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
–11 dBVrms, 51.2 kHz, Two Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 51.2 kHz, Two Ch, Ch 2	–0.2	0.2		
27 dBVrms, 25.6 kHz, Four Ch, Ch 1	–0.2	0.2		
27 dBVrms, 25.6 kHz, Four Ch, Ch 2	–0.2	0.2		
27 dBVrms, 25.6 kHz, Four Ch, Ch 3	–0.2	0.2		
27 dBVrms, 25.6 kHz, Four Ch, Ch 4	–0.2	0.2		
9 dBVrms, 25.6 kHz, Four Ch, Ch 1	–0.2	0.2		
9 dBVrms, 25.6 kHz, Four Ch, Ch 2	–0.2	0.2		
9 dBVrms, 25.6 kHz, Four Ch, Ch 3	–0.2	0.2		
9 dBVrms, 25.6 kHz, Four Ch, Ch 4	–0.2	0.2		
–11 dBVrms, 25.6 kHz, Four Ch, Ch 1	–0.2	0.2		
–11 dBVrms, 25.6 kHz, Four Ch, Ch 2	–0.2	0.2		
–11 dBVrms, 25.6 kHz, Four Ch, Ch 3	–0.2	0.2		
–11 dBVrms, 25.6 kHz, Four Ch, Ch 4	–0.2	0.2		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Amplitude Linearity

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
13 dBVrms, Ch 1	–0.0615	0.061		
13 dBVrms, Ch 2	–0.0615	0.061		
13 dBVrms, Ch 3	–0.0615	0.061		
13 dBVrms, Ch 4	–0.0615	0.061		
–1 dBVrms, Ch 1	–0.105	0.104		
–1 dBVrms, Ch 2	–0.105	0.104		
–1 dBVrms, Ch 3	–0.105	0.104		
–1 dBVrms, Ch 4	–0.105	0.104		
–15 dBVrms, Ch 1	–0.33	0.318		
–15 dBVrms, Ch 2	–0.33	0.318		
–15 dBVrms, Ch 3	–0.33	0.318		
–15 dBVrms, Ch 4	–0.33	0.318		
–29 dBVrms, Ch 1	–1.551	1.316		
–29 dBVrms, Ch 2	–1.551	1.316		
–29 dBVrms, Ch 3	–1.551	1.316		
–29 dBVrms, Ch 4	–1.551	1.316		
–43 dBVrms, Ch 1	–13.823	5.088		
–43 dBVrms, Ch 2	–13.823	5.088		
–43 dBVrms, Ch 3	–13.823	5.088		
–43 dBVrms, Ch 4	–13.823	5.088		
–53 dBVrms, Ch 1	–30.116	10.896		
–53 dBVrms, Ch 2	–30.116	10.896		
–53 dBVrms, Ch 3	–30.116	10.896		
–53 dBVrms, Ch 4	–30.116	10.896		

Serial Number:_____Report Number:_____
Test Date:___/___/___

A Weight Filter

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Ch 1, 10 Hz	–5	2		
Ch 2, 10 Hz	–5	2		
Ch 3, 10 Hz	–5	2		
Ch 4, 10 Hz	–5	2		
Ch 1, 31.62 Hz	–1	1		
Ch 2, 31.62 Hz	–1	1		
Ch 3, 31.62 Hz	–1	1		
Ch 4, 31.62 Hz	–1	1		
Ch 1, 100 Hz	–0.7	0.7		
Ch 2, 100 Hz	–0.7	0.7		
Ch 3, 100 Hz	–0.7	0.7		
Ch 4, 100 Hz	–0.7	0.7		
Ch 1, 1000 Hz	–0.7	0.7		
Ch 2, 1000 Hz	–0.7	0.7		
Ch 3, 1000 Hz	–0.7	0.7		
Ch 4, 1000 Hz	–0.7	0.7		
Ch 1, 10000 Hz	–3	2		
Ch 2, 10000 Hz	–3	2		
Ch 3, 10000 Hz	–3	2		
Ch 4, 10000 Hz	–3	2		
Ch 1, 25120 Hz	–4.5	2.4		
Ch 2, 25120 Hz	–4.5	2.4		
Ch 3, 25120 Hz	–4.5	2.4		
Ch 4, 25120 Hz	–4.5	2.4		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Channel Match

Two Ch, 2/1, 7 dBV FS Mag	–0.04	0.04
Two Ch, 2/1, 7 dBV FS Phs	–0.5	0.5
Two Ch, 2/1, –13 dBV FS Mag	–0.04	0.04
Two Ch, 2/1, –13 dBV FS Phs	–0.5	0.5
Two Ch, 2/1, –33 dBV FS Mag	–0.04	0.04
Two Ch, 2/1, –33 dBV FS Phs	–0.5	0.5
Two Ch, 2/1, 7 dBV –20 dBfs Mag	–0.08	0.08
Two Ch, 2/1, 7 dBV –20 dBfs Phs	–0.5	0.5
Four Ch, 2/1, 7 dBV FS Mag	–0.04	0.04
Four Ch, 2/1, 7 dBV FS Phs	–0.5	0.5
Four Ch, 2/1, –13 dBV FS Mag	–0.04	0.04
Four Ch, 2/1, –13 dBV FS Phs	–0.5	0.5
Four Ch, 2/1, –33 dBV FS Mag	–0.04	0.04
Four Ch, 2/1, –33 dBV FS Phs	–0.5	0.5
Four Ch, 2/1, 7 dBV –20 dBfs Mag	–0.08	0.08
Four Ch, 2/1, 7 dBV –20 dBfs Phs	–0.5	0.5
Four Ch, 3/1, 7 dBV FS Mag	–0.04	0.04
Four Ch, 3/1, 7 dBV FS Phs	–0.5	0.5
Four Ch, 3/1, –13 dBV FS Mag	–0.04	0.04
Four Ch, 3/1, –13 dBV FS Phs	–0.5	0.5
Four Ch, 3/1, –33 dBV FS Mag	–0.04	0.04
Four Ch, 3/1, –33 dBV FS Phs	–0.5	0.5
Four Ch, 3/1, 7 dBV –20 dBfs Mag	–0.08	0.08
Four Ch, 3/1, 7 dBV –20 dBfs Phs	–0.5	0.5
Four Ch, 4/1, 7 dBV FS Mag	–0.04	0.04
Four Ch, 4/1, 7 dBV FS Phs	–0.5	0.5
Four Ch, 4/1, –13 dBV FS Mag	–0.04	0.04
Four Ch, 4/1, –13 dBV FS Phs	–0.5	0.5
Four Ch, 4/1, –33 dBV FS Mag	–0.04	0.04
Four Ch, 4/1, –33 dBV FS Phs	–0.5	0.5
Four Ch, 4/1, 7 dBV –20 dBfs Mag	–0.08	0.08
Four Ch, 4/1, 7 dBV –20 dBfs Phs	–0.5	0.5
Four Ch, 4/3, 7 dBV FS Mag	–0.04	0.04

Serial Number:_____Report Number:_____
Test Date:___/___/___

Four Ch, 4/3, 7 dBV FS Phs	–0.5	0.5
Four Ch, 4/3, –13 dBV FS Mag	–0.04	0.04
Four Ch, 4/3, –13 dBV FS Phs	–0.5	0.5
Four Ch, 4/3, –33 dBV FS Mag	–0.04	0.04
Four Ch, 4/3, –33 dBV FS Phs	–0.5	0.5
Four Ch, 4/3, 7 dBV –20 dBfs Mag	–0.08	0.08
Four Ch, 4/3, 7 dBV –20 dBfs Phs	–0.5	0.5

Frequency Accuracy

Measurement	Lower Limit (kHz)	Upper Limit (kHz)	Measured Value (kHz)	Pass/Fail
50 kHz	49.9985	50.0015		

Serial Number:_____Report Number:_____
Test Date:___/___/___

Single Ch Phase Accuracy

Measurement	Lower Limit (deg)	Upper Limit (deg)	Measured Value (deg)	Pass/Fail
Positive slope, Ch 1	–4	4		
Positive slope, Ch 2	–4	4		
Positive slope, Ch 3	–4	4		
Positive slope, Ch 4	–4	4		
Negative slope, Ch 1	–4	4		
Negative slope, Ch 2	–4	4		
Negative slope, Ch 3	–4	4		
Negative slope, Ch 4	–4	4		

Tach Function (option D01 only)

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
Trigger level +8V Pos	–10	10		
Trigger level +8V Neg	–10	10		
Trigger level –8V Pos	–10	10		
Trigger level –8V Neg	–10	10		

ICP Supply

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Ch 1 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 2 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 3 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 4 Open Circuit Voltage	26 Vdc	32 Vdc	Vdc	
Ch 1 Current	2.75 mA	5.75 mA	mA	
Ch 2 Current	2.75 mA	5.75 mA	mA	
Ch 3 Current	2.75 mA	5.75 mA	mA	
Ch 4 Current	2.75 mA	5.75 mA	mA	

Serial Number:_____Report Number:_____
Test Date:___/___/___

Source Amplitude Accuracy

Measurement	Lower Limit (%)	Upper Limit (%)	Measured Value (%)	Pass/Fail
1 kHz, 0.1 Vpk	–4	4		
1 kHz, 3.0 Vpk	–4	4		
1 kHz, 5.0 Vpk	–4	4		

Source Flatness

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
12.8 kHz	–1	1		
25.6 kHz	–1	1		
51.2 kHz	–1	1		

Source Distortion

Measurement	Lower Limit	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
12.8 kHz		–60		
51.2 kHz		–40		

4

Troubleshooting the Analyzer

Troubleshooting the Analyzer

This chapter contains troubleshooting tests that can isolate most failures to the faulty assembly. The section ''How to troubleshoot the analyzer'' tells you which test to start with based on the failure. The test you start with will either isolate the faulty assembly or send you to another test to continue troubleshooting.

Safety Considerations

The Agilent 35670A Dynamic Signal Analyzer is a Safety Class 1 instrument (provided with a protective earth terminal). Although the instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings that must be followed to ensure safe operation and retain the instrument in safe operating condition. Service must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Warning

Any interruption of the protective (grounding) conductor inside or outside the analyzer, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the Agilent 35670A Dynamic Signal Analyzer. There are no operator controls inside the analyzer.

Only fuses with the required current rating and of the specified type should be used for replacement. The use of repaired fuses or short circuiting the fuse holder is not permitted. Whenever it is likely that the protection offered by the fuse has been impaired, the analyzer must be made inoperative and secured against any unintended operation.

When power is removed from the Agilent 35670A Dynamic Signal Analyzer, +225 volts are present in the display for approximately 5 seconds. Be extremely careful when working in proximity to this area during this time. The high voltage can cause serious personal injury if contacted.

Caution

Do not connect or disconnect ribbon cables with the power switch set to on (|). Power transients caused by connecting or disconnecting a cable can damage circuit assemblies.

Equipment Required

See ''Recommended Test Equipment'' starting on page 1-17 for tables listing recommended equipment. Any equipment which meets the critical specifications given in the tables may be substituted for the recommended model.

Troubleshooting Hints

- Incorrect bias supply voltages can cause false diagnostic messages. In most troubleshooting procedures, the power supply voltages are not checked. If you suspect incorrect supply voltages to an assembly, use the ''Voltages and Signals'' chapter to check the voltages at the assembly.
- Cables can cause intermittent hardware failures.
- Noise or spikes in the power supply can cause the analyzer to fail.
- Measurements in this chapter are only approximate (usually ∫1 dB or 10%) unless stated otherwise.
- Use chassis ground for all measurements in this chapter unless stated otherwise.
- To determine your firmware version code, press [**System Utility**] [MORE] [S/N VERSION].
- Logic levels in this chapter are either TTL level high or TTL level low unless stated otherwise. Toggling signal levels continually change from one TTL level to the other.
- The troubleshooting tests in this chapter assume only one independent failure. Multiple failures can cause false results.
- The troubleshooting procedures do not isolate failures to cables or connectors. If you suspect a cable or connector failure, check the device for continuity.
- If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening press [**Preset**] [DO PRESET] or cycle power after you abort the self test.

How to troubleshoot the analyzer

- **Review ''Safety Considerations'' and ''Troubleshooting Hints.''**

Warning

Service must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

- **See chapter 6, ''Replacing Assemblies,'' to determine how to disassemble and assemble the analyzer.**
- **Determine initial test by comparing the analyzer's symptoms to the symptoms in the following table.**

Symptom	Troubleshooting Test
Screen blank † Screen defective After power up, >3 minutes before keys active No response when key is pressed Incorrect response when key is pressed	Initial verification, page 4-5
Keys are active and screen grid is displayed but screen is defective	Display, page 4-22
Error messages Calibration fails Performance test fails Intermittent failure GPIB fails Mic pwr fails Serial port fails Parallel port fails External monitor does not work	Self tests, page 4-31
External keyboard does not work	DIN connector, page 4-61
External trigger fails	Trigger, page 4-62
Nonvolatile states not saved after power cycled Date display is ''Date: 01-01-BL''	Memory battery, page 4-67

† If the analyzer is failing, the grid may not appear for two minutes. Wait two minutes before assuming that a low level failure occurred.

- **Follow the recommended troubleshooting test until you locate the faulty assembly.**
- **Replace the faulty assembly and follow the directions in ''What to do after replacing an assembly'' in chapter 6, ''Replacing Assemblies.''**

To perform initial verification

Use this test to check signals that are vital to the operation of the analyzer.

❑ Step 1. Check the power select switch and fuse.

- **Check that the POWER SELECT switch on the rear of the analyzer is set to the AC position.**
- **Check that the correct line fuse is installed in the rear panel fuse holder.**

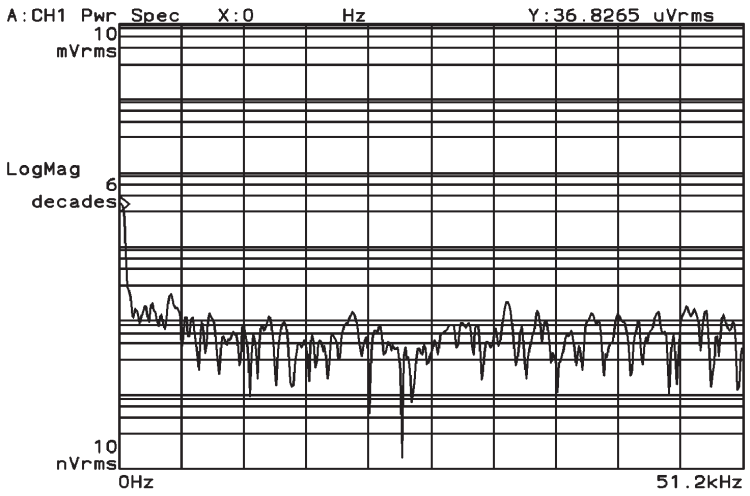
For information on the power select switch and line fuse, see ‘’To do the incoming inspection’’ on page 2-5 and ‘’To change the fuses’’ on page 2-10.

❑ Step 2. If the grid appears after power up but there is no response when keys are pressed, ckeck that the calibration routine is not locking up the analyzer.

- **Set the power switch to off (** O **).**
- **Set the power switch to on (** I **) and as soon as** Booting System **appears on the display, disable the calibration routine by holding [Preset] until** Uncalibrated data **appears.**
- **If the keys are now active, go to page 4-37, ‘’To troubleshoot self-test lockup failures.’’**

❑ Step 3. If the analyzer powers up with failure messages, then locks up, but the grid and lettering appear normal, go to page 4-15, ‘’To troubleshoot power-up failures.’’

❑ Step 4. If the analyzer powers up normally with no error messages (see the following illustration), the screen is continually updating, but the analyzer does not respond to key presses, use the following table to determine the probable faulty assembly.



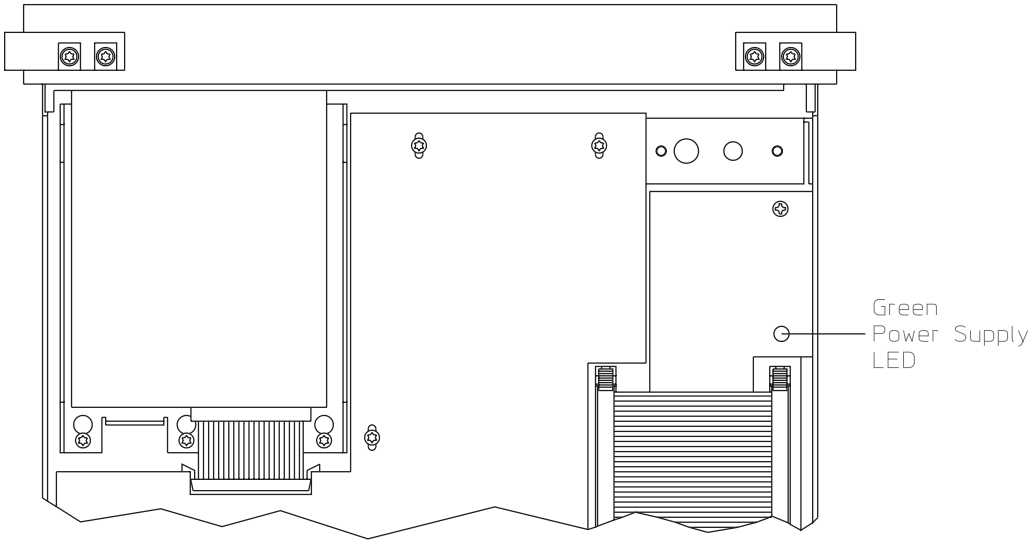
Symptom	Probable Faulty Assembly
SYSTEM keys function but MARKER, DISPLAY, MEASUREMENT, or number keys do not function correctly	A13 or A15 Primary Keypad
MARKER, DISPLAY, MEASUREMENT, and number keys function but SYSTEM keys do not function correctly	A14 Secondary Keypad
No keys function correctly	A11 Keyboard Controller

❑ Step 5. Check the power supply LED and fan.

- **Set the power switch to off (O) and disconnect the power cord from the rear panel.**
- **Remove the cover.**

See ''To remove cover'' on page 6-6.

- **Connect the power cord and set the power switch to on (|).**
- **If the green power supply LED is not lit, go to page 4-11, ''To troubleshoot the power supply.''**



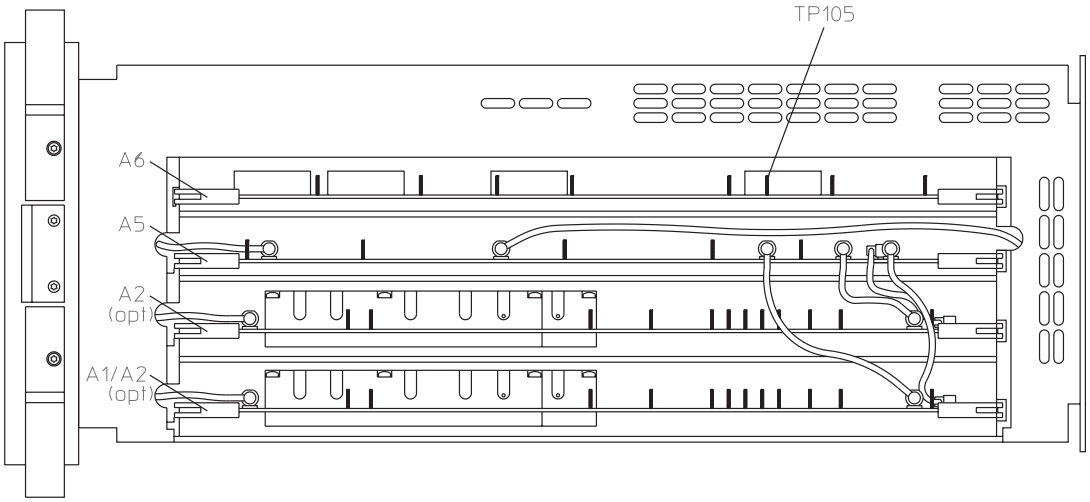
- **Check that the fan is turning at a moderate speed for normal room temperature.**

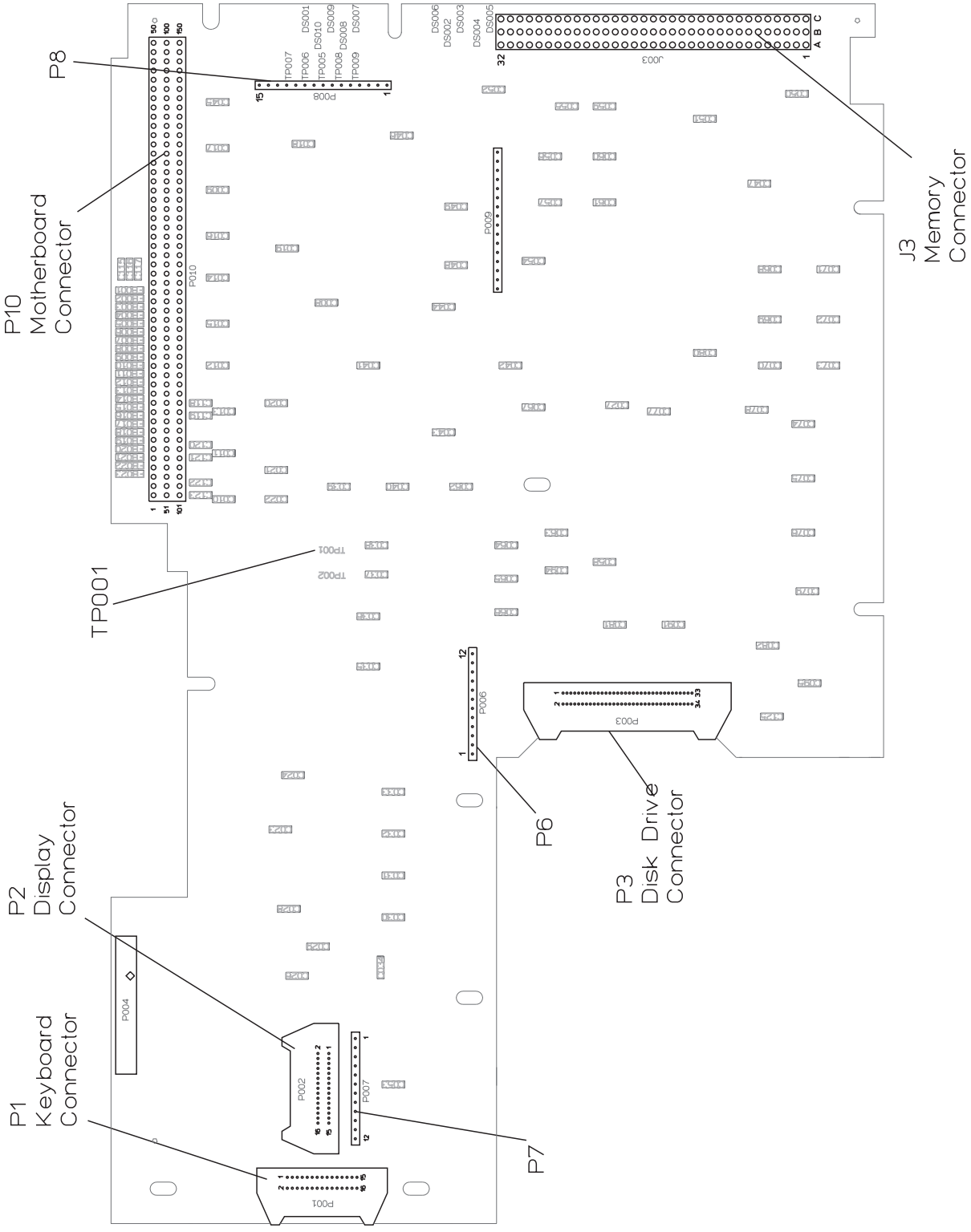
The fan is very quiet. Check air flow before determining that the fan is not turning.

- **If the fan is not turning, go to page 4-11, ''To troubleshoot the power supply.''**

❑ Step 6. Check the following TTL clock signals using an oscilloscope and a 1 MΩ 10:1 probe.

Signal Name	Test Location	Frequency	Probable Faulty Assembly
FREQ REF	A7 TP1	19.923 MHz	A7 CPU
G20MHz	A7 J3 pin 32C	19.923 MHz	A7 CPU
VCLK	A7 P2 pin 13	20 MHz	A7 CPU
SYSCLK	A6 TP105	10 MHz	A6 Digital





A7 Component Locator, Circuit Side

❑ Step 7. Check signals required for power up.

- **Using a logic probe, check the following signals.**

Signal Name	Test Location	TTL State	Probable Faulty Assembly
PVALID	A7 P8 pin 3	High	A98 Power Supply
RSTn	A7 P8 pin 5	High	A7 CPU
CASn	A7 P7 pin 3	Toggling	A7 CPU
RASn	A7 P7 pin 4	Toggling	A7 CPU
VDATA	A7 P7 pin 7	Toggling	A7 CPU
ASn	A7 P6 pin 10	Toggling	A7 CPU

- **Using a logic probe, check that the following TTL signals are toggling just after power up.**

The signals may stop toggling when the CPU assembly finishes the bootrom self tests.

Signal Name	Test Location
PASn	A7 P8 pin 7
PDSACK1n	A7 P8 pin 8
PDSACK0n	A7 P8 pin 9
PRW	A7 P8 pin 10
PDSn	A7 P8 pin 11
PA(26)	A7 P8 pin 12
PA(16)	A7 P8 pin 13

- **If the signals are not correct, the A7 CPU assembly is probably faulty.**
- **Using a logic probe, check that A7 P7 pin 2 (SCL) and A7 P7 pin 1 (SDA) toggle TTL states at least twice just after power up.**
- **If the signals are not correct, the A7 CPU assembly is probably faulty.**
- **If the signals are correct, go to page 4-15, ‘’To troubleshoot power-up failures.’’**

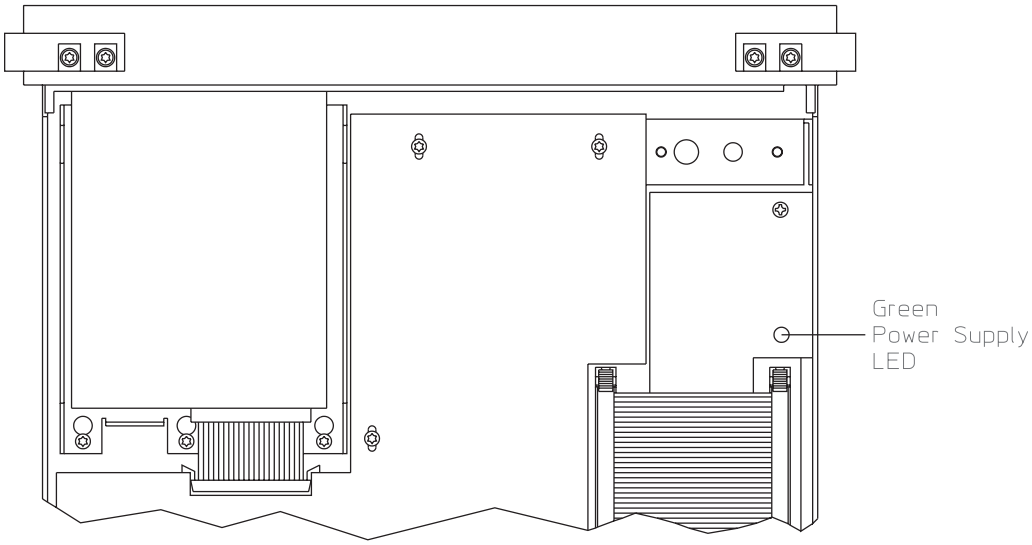
To troubleshoot the power supply

Use this test to check the Power Supply and Fan assemblies. This test can also isolate the assembly causing the Power Supply to shut down.

❑ Step 1. Check the power supply LED.

- **Set the power switch to off (O).**
- **Disconnect the ribbon cable from the A98 Power Supply assembly.**
- **Set the power switch to on (I).**
- **If the green power supply LED is not lit, the A98 Power Supply assembly is probably faulty.**
- **Set the power switch to off (O).**
- **Reconnect the ribbon cable to the Power Supply assembly.**
- **Set the power switch to on (I).**
- **If the power supply LED is on but the fan is not turning, go to Step 7.**

A thermistor on the A10 Rear Panel assembly controls the power to the A90 Fan assembly. As the analyzer's temperature increases, the fan speed increases. Since the fan is very quiet, check air flow before determining that the fan is not turning.

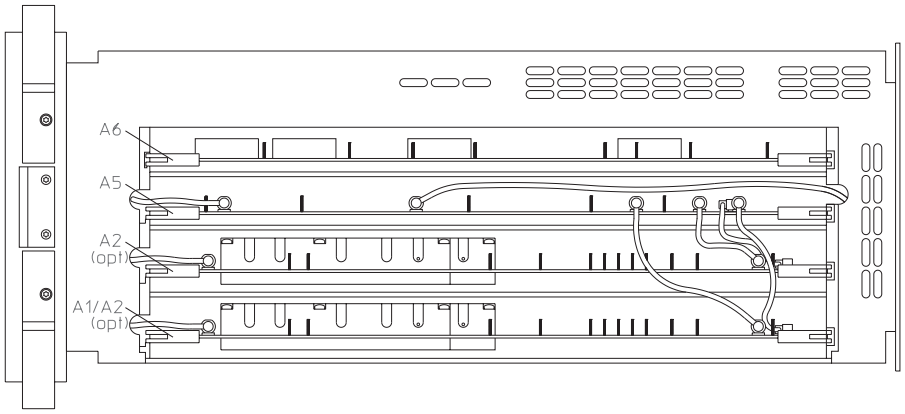


❑ Step 2. Determine if the Digital, Analog, or Input assemblies are causing the Power Supply assembly to shut down.

- **Set the power switch to off (O).**
- **Pull the following assemblies out of the card nest about 1 inch:**

A6 Digital
A5 Analog
A2 Input (optional)
A1/A2 Input

- **Set the power switch to on (I).**
- **If the power supply LED is still off, set the power switch to off (O), reconnect the above assemblies, and go to Step 4.**



❑ Step 3. Repeat the following until the assembly causing the Power Supply assembly to shut down is located.

- **Set the power switch to off (O).**
- **Reconnect one assembly at a time in the following order.**

A6 Digital
A5 Analog
A2 Input (optional)
A1/A2 Input

- **Set the power switch to on (I).**
- **If the green power supply LED is off, the assembly just reconnected is probably faulty.**

The A5 Analog assembly provides over-temperature protection which shuts down the power supply if the analyzer's internal temperature becomes excessive. Before replacing the A5 Analog assembly, check that the fan is turning when the green power supply LED is on and that the air flow is not restricted (cooling air enters from the right side and exhausts through the left side and rear panel). Since the fan is very quiet, check air flow to determine that the fan is turning.

❑ Step 4. Determine if the CPU assembly or one of the assemblies connected to the CPU assembly is causing the power supply to shut down.

- **Remove the A7 CPU assembly.**

See ''To remove CPU'' on page 6-11.

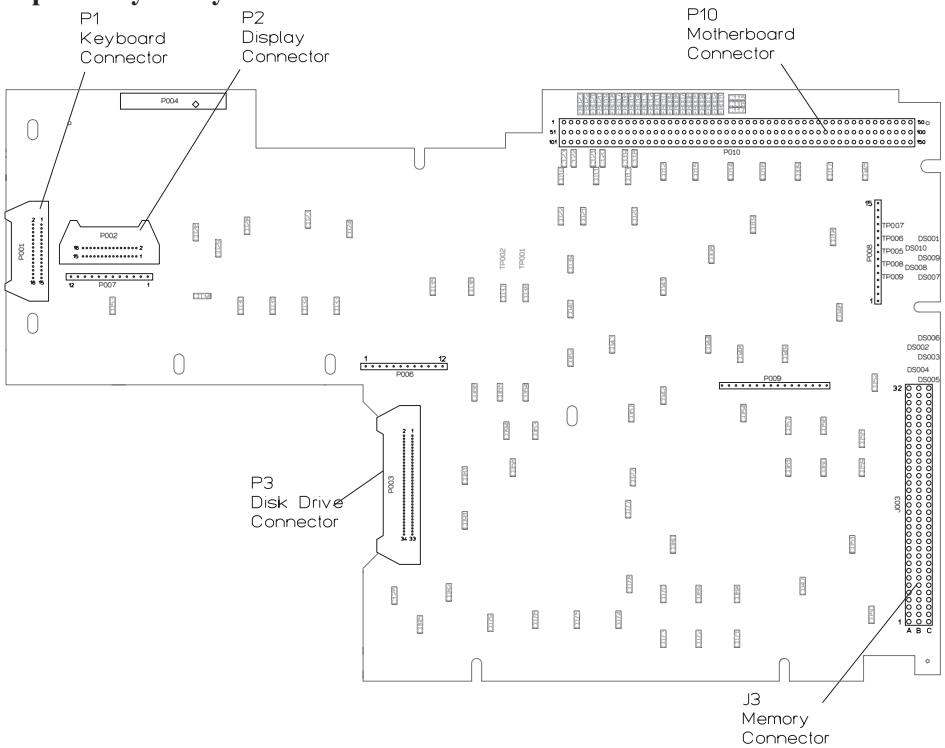
- **Set the power switch to on (|).**
- **If the power supply LED is still off, set the power switch to off (○), reconnect the CPU assembly, and go to Step 6.**

❑ Step 5. Repeat the following steps until the assembly causing the Power Supply assembly to shut down is located.

- **Set the power switch to off (○).**
- **Reconnect one assembly at a time in the following order:**

A7 CPU (A7 P10 to A99 J7)
A8 Memory (A8 P1 to A7 J3)
A102 DC-DC Converter (cable to A7 P2)
A11 Keyboard Controller (cable to A7 P1)
A100 Disk Drive (cable to A7 P3)

- **Set the power switch to on (|).**
- **If the green power supply LED is off, the assembly just reconnected is probably faulty.**



A7 Component Locator, Circuit Side

❑ Step 6. Determine if the Motherboard, Fan, or Rear Panel assembly is causing the Power Supply to shut down.

- **Disconnect the fan cable from A99 P90.**
- **Set the power switch to on (|).**
- **If the power supply LED is now on, the A90 Fan assembly is probably faulty.**
- **Set the power switch to off (O).**
- **Reconnect the fan cable.**
- **Remove the rear panel and disconnect the cable from A10 P100.**

See ''To remove rear panel'' on page 6-7.

- **Set the power switch to on (|).**
- **If the power supply LED is now on, the A10 Rear Panel assembly is probably faulty.**
- **If the Fan or Rear Panel assembly is not causing the Power Supply assembly to shut down, then the A99 Motherboard is probably faulty.**

❑ Step 7. Check the Fan assembly.

- **Set the power switch to off (O).**
- **Remove the A7 CPU assembly.**

See ''To remove CPU'' on page 6-11.

- **Disconnect the fan power cable from A99 P90 (red and black cable).**
- **Connect 5 Vdc to the fan cable. The fan should be turning slowly.**
- **Increase the voltage to 10 Vdc. The fan should turn faster as the voltage increases.**
- **If the fan did not respond correctly, the A90 Fan assembly is probably faulty.**
- **If the fan responded correctly, the A10 Rear Panel assembly is probably faulty.**

To troubleshoot power-up failures

Use this test when the screen is defective, when the analyzer does not respond correctly to the keyboard, or when it takes more than 3 minutes for the keyboard to become active. Any of the following conditions may cause a power-up failure:

- A defective CPU or Memory assembly.
- A defective assembly connected to the CPU assembly causing a bus failure.
- A defective cable between the CPU assembly and another assembly.
- A defective control line.

❑ Step 1. Compare the power-up failure messages to the following table.

- **Set the power switch to on (|).**
- **If the screen is blank or no power-up failure messages are displayed, go to Step 2.**
- **Determine the probable faulty assembly or next test by comparing the power-up test result to the following table.**

If the power-up failure messages match more than one entry in the table, use the entry closest to the beginning of the table.

Failing Power-up Message	Probable Faulty Assembly or Next Test
LEDs MC68030 Processor MC68882 Coprocessor Bootrom Display	A7 CPU
Main RAM Program ROM	CPU, memory, DSP, and buses failures, page 4-18
DSP	A7 CPU
Fast bus	IIC Bus failures, page 4-25
MFP	A7 CPU
GPIB keypress detected, booting to GPIB Monitor	A14 Secondary Keypad
Front Panel failure information: keyboard IIC chip fails: IIC: No Device Acknowledge key stuck: 32	A11 Keyboard Controller
Front Panel failure information: key stuck: *number* *where number is 13, 14, 16, 20, 21, 24, 33, 35, 36, 37, 38, 40, 43, 52, 53, or 54*	A14 Secondary Keypad
Front Panel failure information: key stuck: *number* *all other numbers not listed above*	A13 or A15 Primary Keypad

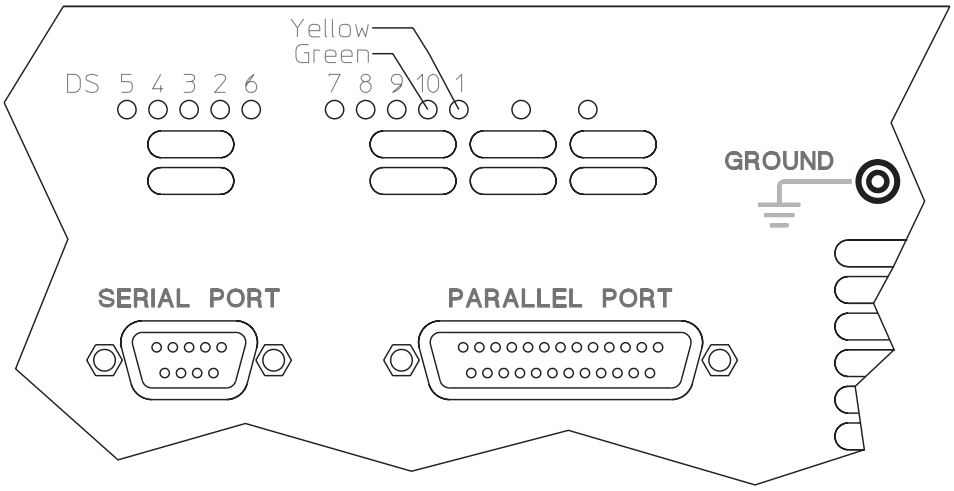
❑ Step 2. Determine if the power-on test passed or failed.

- **Set the power switch to off (O).**
- **Set the power switch to on (I) while watching the power-on LEDs.**

The power-on LEDs are on the A7 CPU assembly and are visible through the rear panel. To see the LEDs easier, remove the seven screws holding the rear panel to the analyzer and lean the rear panel back. This also gives you access to reset switch SW2.

- **If the power-on LEDs responded as follows, the power-on test passed.**

- All power-on LEDs are on momentarily.
- DS1 (yellow, +5 LED) remains on as long as power is applied to the assembly.
- DS10 (green, run LED) comes on just after DS1.
- DS5, DS4, DS3, DS2, DS6, DS7, DS8, and DS9 sequence through the codes listed in the following table.



Binary (DS5) (DS9)	Hexa-decimal	~Time LEDs Visible	Description
1111 1111 0000 0000	FF 00	200 ms on 200 ms off	A7 flashes LEDs
0000 1000	08	†	starting A7 test
0000 0010	02	†	A8 RAM DSACK test
0001 0100	14	†	starting A8 RAM test
0001 0110	16	†	starting A8 refresh test
0001 1100	1C	4s	starting A8 program ROM test
0000 0000	00	4s	clear LEDs
1010 0000	A0	†	A7 MFP test
1010 0001	A1	†	starting A7 DSP test
1010 0010	A2	†	fast bus test
0101 1110	AE	200 ms	front panel test
1111 1111	FF	Remain on	

0 = LED off
1 = LED on
† When no failure occurs, these codes appear for only a very short time and probably won't be visible.

- **If the power-on LEDs display a code for more than 4 seconds, a failure occurred in the core assemblies or on the buses.**

  For additional information on the power-on test, see the ''Power-on Test Descriptions'' on page 10-3.

❑ Step 3. Determine the next step by comparing the power-on test results to the following table.

Power-on LEDs	Next Test
LEDs stop and display a fail code. A7 DS101 (green, run LED) is off.	CPU, memory, and buses, page 4-18
LEDs pass, but the screen is defective.	Display, 4-22
LEDs pass, but it takes more than 3 minutes before the keys are active. LEDs pass and screen appears normal, but keys do not function.	IIC Bus, page 4-25

To troubleshoot CPU, memory, and buses failures

Use this test to isolate the failure when the power-on LEDs show a fail code or the analyzer locks up during the power-up tests.

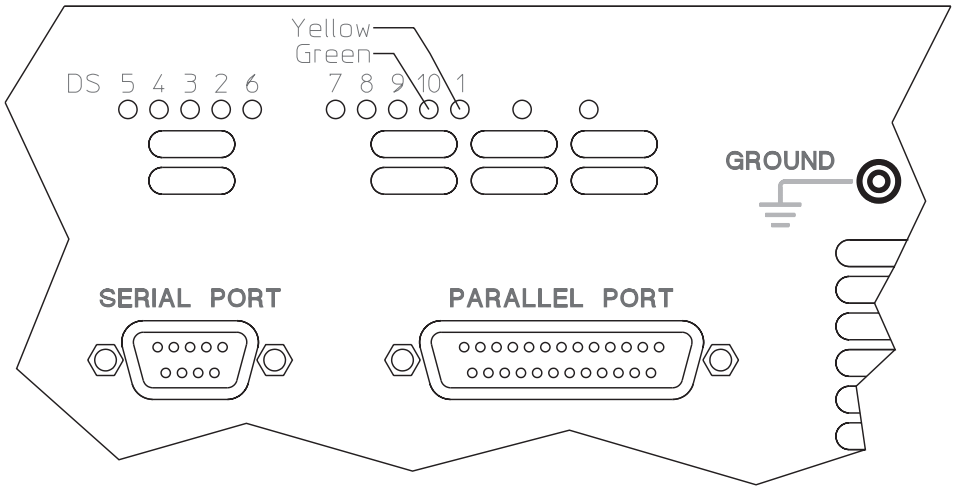
❑ Step 1. Compare the LED fail code to the following table.

- **Set the power switch to off (O).**
- **Set the power switch to on (I) while watching the power-on LEDs.**

The power-on LEDs are on the A7 CPU assembly and are visible through the rear panel. To see the LEDs easier, remove the seven screws holding the rear panel to the analyzer and lean the rear panel back. This also gives you access to reset switch SW2.

- **Determine the probable faulty assembly by comparing the power-on LEDs fail code to the following table.**

The power-on LEDs are showing a fail code when the LEDs display a code for more than 4 seconds.



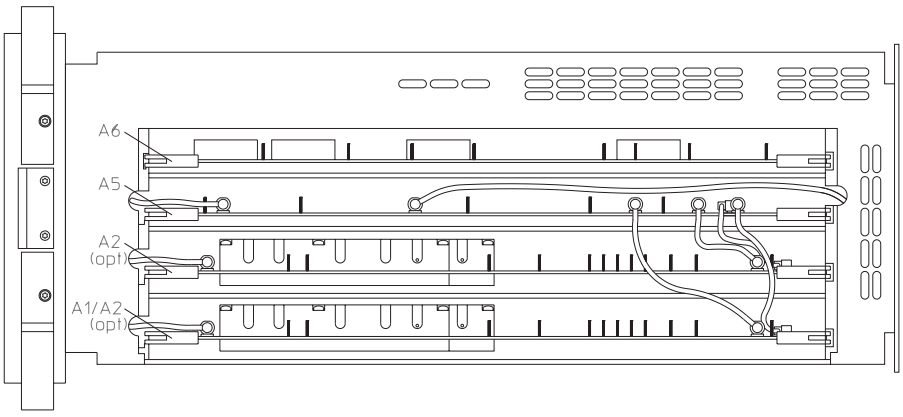
Binary (DS5) (DS9)	Hexadecimal	Probable Faulty Assembly
0000 0100	04	A7 CPU
1111 1111	FF	
0001 0011	13	
0000 0001	01	
0001 0111	17	
0001 1000	18	
0000 1001	09	
0000 1011	0B	
0001 1010	1A	
0001 1001	19	
0000 1000	08	
0001 0010	12	
1010 0000	A0	
0000 0010	02	A8 Memory
0001 1011	1B	
0001 0100	14	
0001 0110	16	
0001 1100	1C	

0 = LED off
1 = LED on

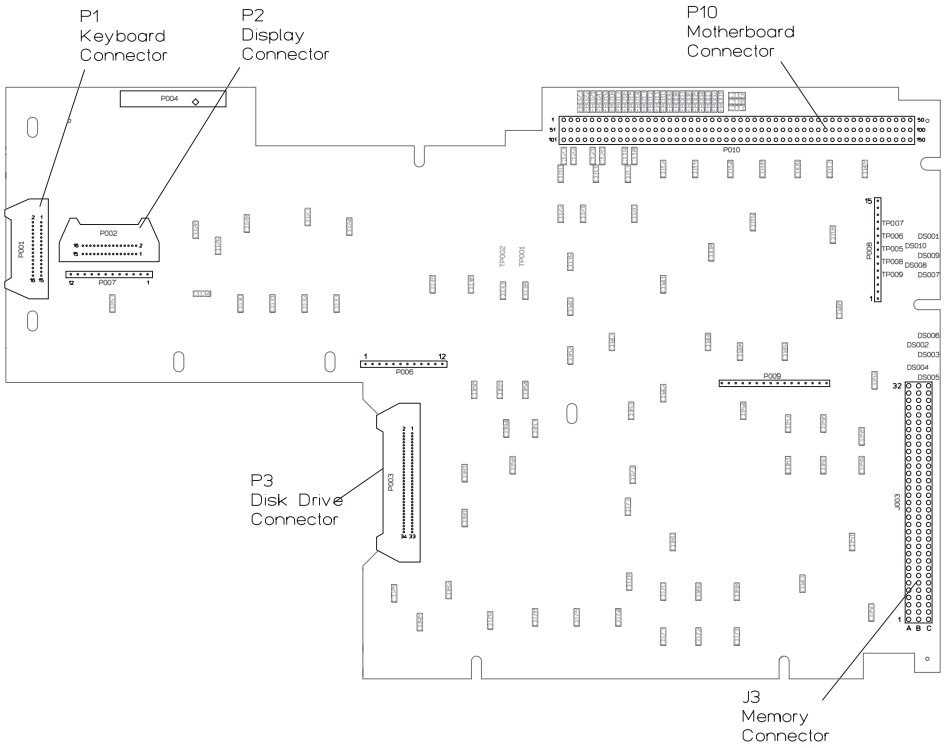
❑ Step 2. Determine if the CPU assembly is causing the failure.

- **Set the power switch to off (○).**
- **Pull the following assemblies out of the card nest about 1 inch:**

A6 Digital
A5 Analog
A2 Input (optional)
A1 or A2 Input



- **Disconnect the A7 CPU assembly from the Motherboard, Memory assembly, and cables.**
- **Reconnect the CPU assembly to the Motherboard (do not connect the Memory assembly or cables to the CPU assembly).**



A7 Component Locator, Circuit Side

- **Set the power switch to on (|) while watching the power-on LEDs.**
- **If the LEDs did not display hexadecimal FF (1111 1111) then hexadecimal 02 (0000 0010), the A7 CPU assembly is probably faulty.**

❑ Step 3. Determine if the Memory or Display assembly is causing the failure.

- **Set the power switch to off (○).**
- **Reconnect the Memory assembly to the CPU assembly.**
- **Set the power switch to on (|) while watching the power-on LEDs.**

The LEDs should sequence through 00 (clear LEDs) with 00 remaining on the LEDs.

- **Set the power switch to off (○).**
- **Reconnect the display cable to A7 P2.**
- **Set the power switch to on (|) while watching the power-on LEDs.**

The LEDs should sequence through 00 (clear LEDs) with 00 remaining on the LEDs. The following is an example of the messages displayed when the CPU and memory power-on tests pass. The numbers in the messages will most likely be different in your analyzer.

Copyright 1988, 1990, 1991, 1992, 1993,
Agilent Technologies Company,
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LEDs
MC68030 Processor
MC68882 Coprocessor
Bootrom revision A.01.17
Main RAM
  Testing 8388608 bytes at 0x06c00000
Program ROM

Copyright 1991, 1992, 1993, Agilent Technologies Company

Booting System

- **If the screen is defective or blank, go to page 4-22, ''To troubleshoot display failures.''**
- **If there is an error message, use the table on page 4-15 in the ''To troubleshoot power-up failures'' procedure to determine the probable faulty assembly.**
- **If the failure still is not isolated, go to page 4-25, ''To troubleshoot IIC bus failures.''**

To troubleshoot display failures

Use this test to isolate display failures to the A101 Display assembly, A102 DC-DC Converter assembly, or A7 CPU assembly.

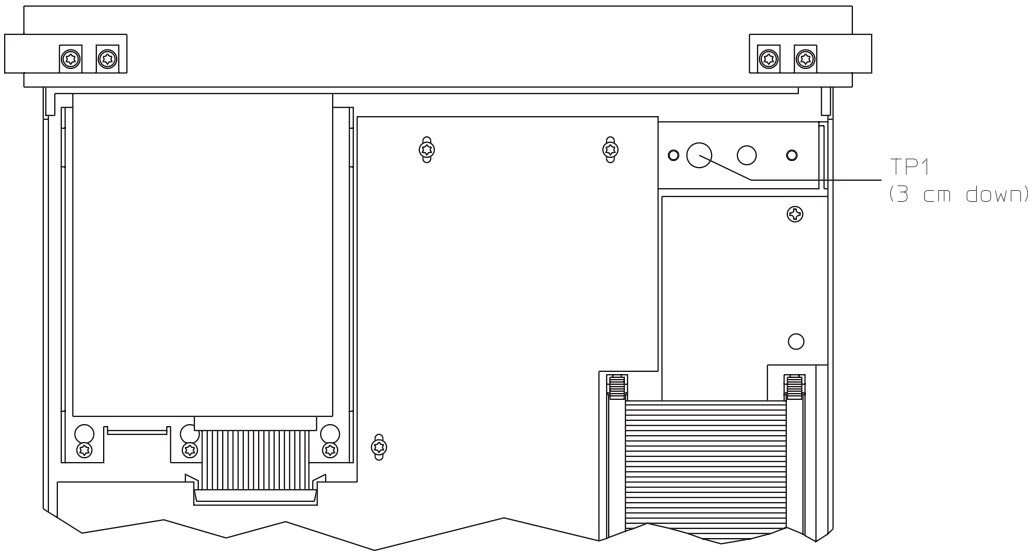
❑ Step 1. Check the DC-DC Converter assembly.

- **Set the power switch to off (O).**
- **Connect the voltmeter to A102 TP1.**
- **Set the power switch to on (I).**
- **Check that the voltage reads is 210 10 Vdc.**

Caution

The Display assembly will be damaged if the voltage is at or above 235 Vdc.

- **If the voltage is incorrect, the A102 DC-DC Converter assembly is probably faulty.**

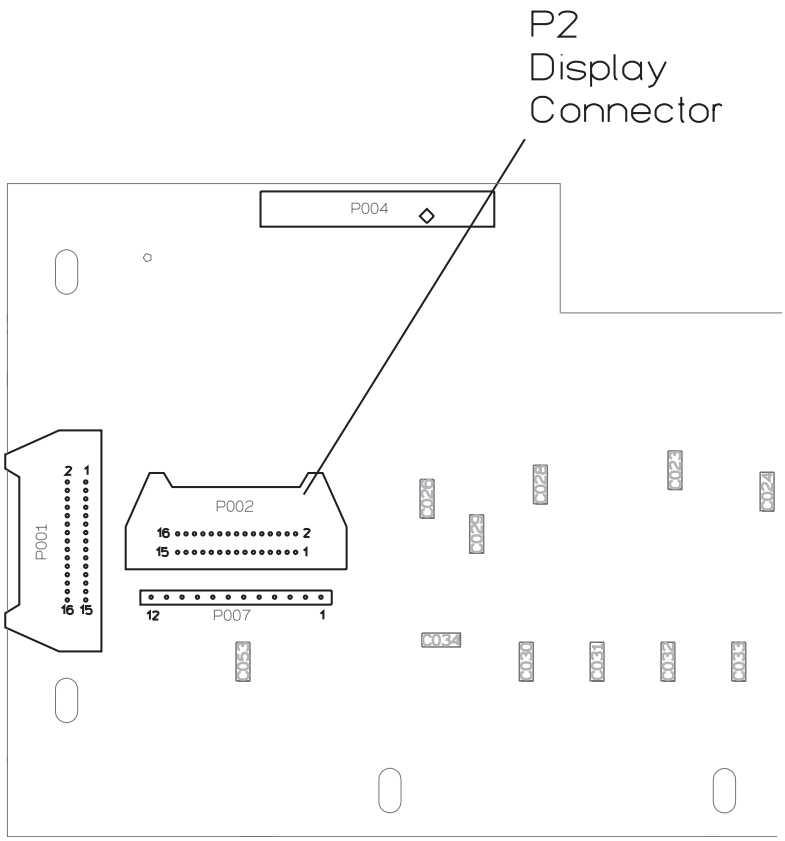


❑ Step 2. Check the CPU signals to the Display assembly.

- **Set the power switch to on (|).**
- **Using a logic probe, check that the following TTL signals are toggling.**

Test Location	Signal Name	In/Out
A7 P2(9)	VSYNCEL	A7 Out
A7 P2(11)	HSYNCELn	A7 Out
A7 P2(13)	VCLK	A7 Out
A7 P2(15)	VID	A7 Out

- **If the signals are incorrect, do the following:**
- **Set the power switch to off (O).**
- **Disconnect the display cable from A7 P2.**
- **Set the power switch to on (|).**
- **Check the signals again.**
- **If the signals are now correct, the A101 Display assembly is probably faulty.**



A7 Component Locator, Circuit Side

❑ Step 3. Determine the probable faulty assembly by comparing the analyzer's symptoms to the following table.

Symptom	Probable Faulty Assembly
Vertical and horizontal scanning is occurring Part of information is missing, for example only half letters Blocks of information are missing Information on the screen is scrambled or mixed up Vertical or horizontal stripes appear across the screen	CPU
Screen is blank Screen is tilted, compressed, or distorted Line across the screen	Display

To troubleshoot IIC bus failures

Use this test to isolate IIC (Inter-IC) bus failures to one of the following assemblies:

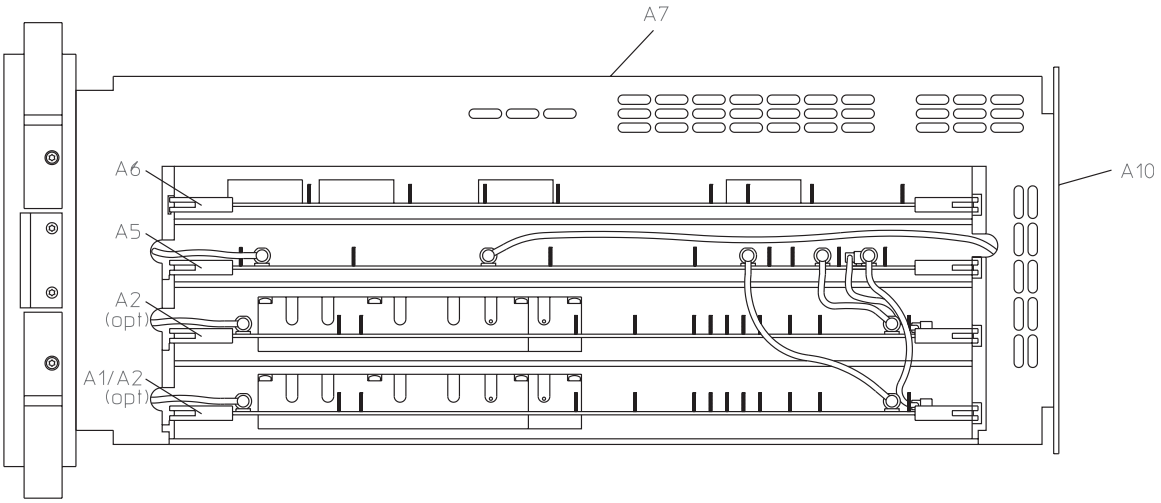
- A7 CPU
- A1/A2 Input
- A5 Analog
- A10 Rear Panel
- A11 Keyboard Controller

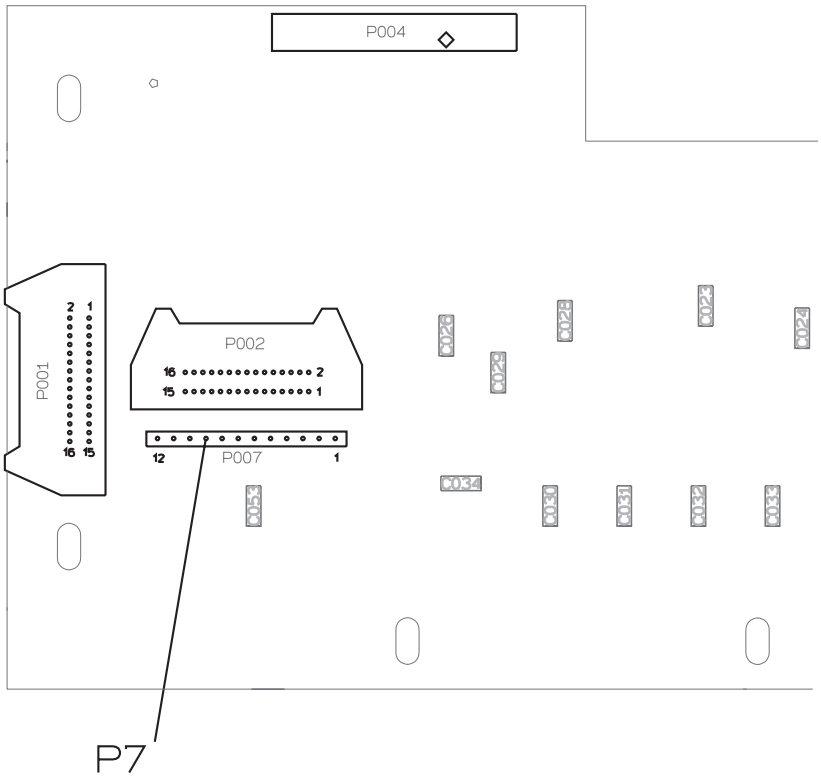
❑ Step 1. Disconnect all assemblies connected to the CPU assembly's IIC bus.

- **Set the power switch to off (○).**
- **Remove the rear panel and disconnect the cable from A10 P100.**
- **Pull the following assemblies out of the card nest about 1 inch:**

A5 Analog
A2 Input (optional)
A1/A2 Input

- **Disconnect the keyboard cable from A7 P1.**





❑ Step 2. Check the serial clock (SCL).

- **Attach a logic probe to A7 P7 pin 2 (SCL).**
- **Set the power switch to on (|).**
- **Press SW2 (reset switch) while monitoring A7 P7 pin 2 (SCL), the power-on LEDs, and the display.**

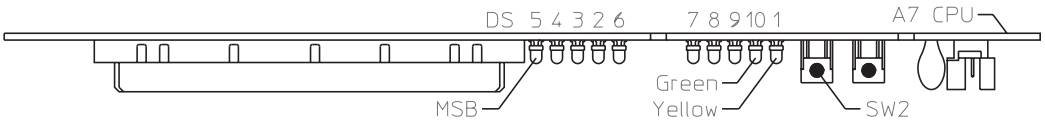
The TTL logic level should toggle when 00 is displayed and toggle continuously when Booting System is displayed. The following failure message should be displayed after Booting System and the display grid should appear about 2 minutes after power up.

Front Panel failure information:
keyboard IIC chip fails:
IIC: No Device Acknowledge
key stuck: 32

A power-on test has failed. Refer servicing to qualified personnel.

Press Start key to attempt to continue power-up.

- **If the signal does not toggle after SW2 is pressed, the A7 CPU assembly is probably faulty.**
- **If no error messages are displayed after** Booting System **or A7 DS101 (green run LED) is off, go to page 4-29, ''To troubleshoot fast bus failures.''**



❑ Step 3. Check the serial data line (SDA).

- **Attach the logic probe to A7 P7 pin 1 (SDA).**
- **Press SW2 while monitoring A7 P7 pin 1 (SDA), the power-on LEDs, and the display.**

The TTL logic level should toggle when 00 is displayed and toggle continuously when Booting System is displayed. The following failure message should be displayed after Booting System and the display grid should appear about 2 minutes after power up.

Front Panel failure information:
keyboard IIC chip fails:
IIC: No Device Acknowledge
key stuck: 32

A power-on test has failed. Refer servicing to qualified personnel.

Press Start key to attempt to continue power-up.

- **If the signal does not toggle after SW2 is pressed or the failure message is not displayed, the A7 CPU assembly is probably faulty.**

❑ Step 4. Check the assemblies on the IIC bus by repeating the following steps for each assembly.

- **Set the power switch to off (O).**
- **Reconnect one assembly at a time in the following order.**

A11 Keyboard Controller (cable to A7 P1)
A10 Rear Panel (cable to A10 P100)
A5 Analog
A1/A2 Input (lower slot)
A2 Input (upper slot)

- **Set the power switch to on (|).**
- **After the softkey menu appears, (about one minute after power up) press any key.**
- **If the analyzer does not respond correctly, the assembly just reconnected is probably faulty.**

❑ Step 5. If the failure still is not isolated, go to page 4-29, ‘’To troubleshoot fast bus failures.’’

To troubleshoot fast bus failures

Use this test to isolate Fast Bus failures to the A7 CPU assembly or A6 Digital assembly.

- **Set the power switch to off (○).**
- **Set the power switch to on (|) while holding in the [System Utility] key.**

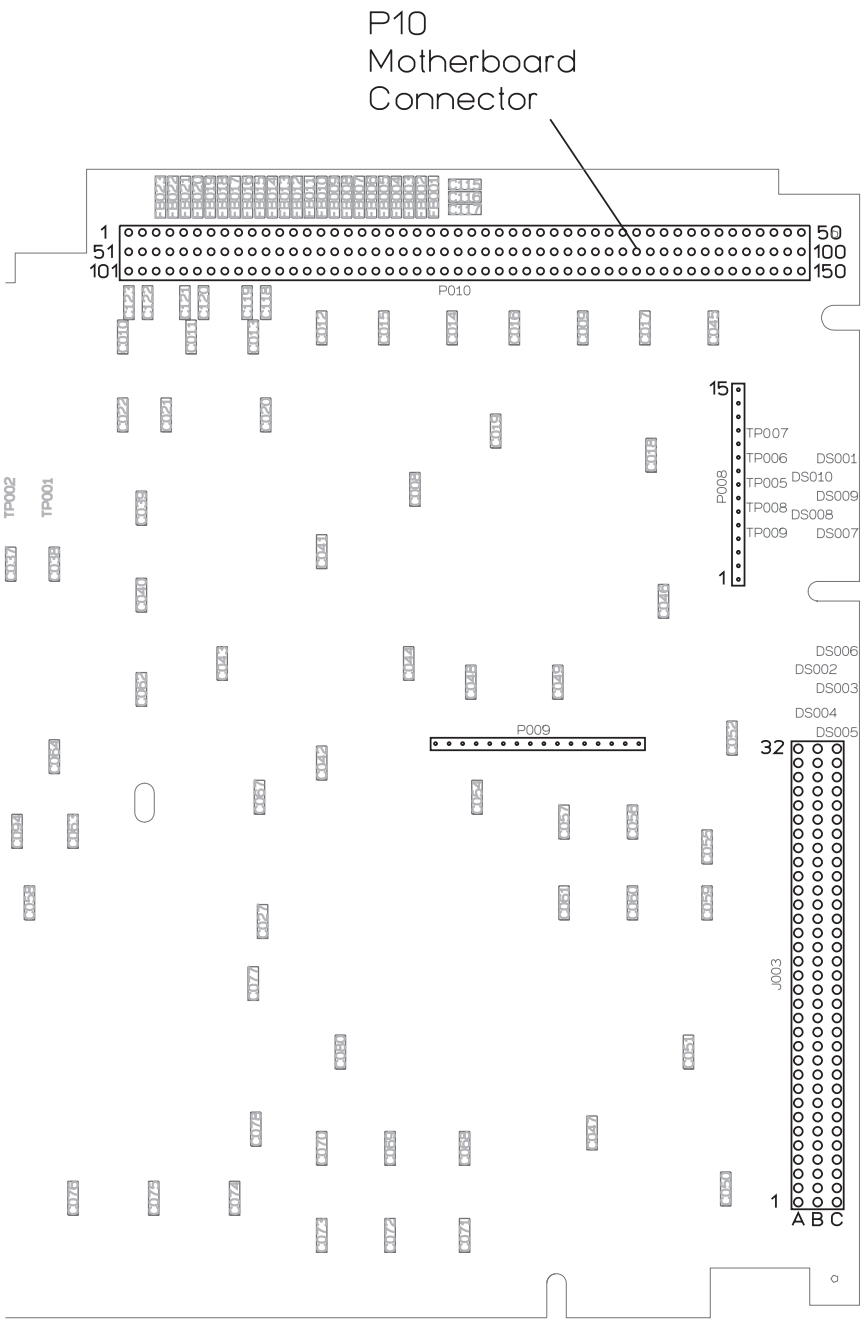
The screen displays Fast Bus Diagnostic Test ... and the power-on LEDs are flashing.

- **If the analyzer did not respond correctly, the A7 CPU assembly is probably faulty.**
- **Using a logic probe, check the following signals.**

A7 P10 Pin	Signal Name	TTL Logic State In Test Mode
64, 114, 65, 115, 66	FA1 to FA5	Toggling
72	ECLK	Toggling
74	FSELAn	Toggling
112	BRESETn	Low
119	FRW	Toggling
123	FIFOENn	High
124	FSELSn	Toggling
7-11, 21-45, 59, 71, 109, 118, 120, 122, 147, 149	GND	Low

- **If the signals are correct, the A6 Digital assembly is probably faulty.**
- **If any signal is incorrect, the A7 CPU assembly is probably faulty.**

This is only a partial check of the fast bus signals between the A7 CPU assembly and the A6 Digital assembly.


P10
Motherboard
Connector
1
51
101
50
100
150
P010
15
1
P008
TP007
TP006
TP005
TP008
TP009
DS001
DS010
DS009
DS008
DS007
TP002
TP001
DS006
DS002
DS003
DS004
DS005
P009
32
1
A B C
J003

To perform self tests

Use this test when one of the following occurs:

- Performance test fails
- Calibration fails
- Trigger fails
- GPIB fails
- Microphone power fails
- Serial port fails
- Parallel port fails
- Failure is intermittent

❑ Step 1. Run all the functional self tests.

- **Connect the rear panel SOURCE output to the rear panel TACH input using a BNC cable.**
- **Remove all cables from the front panel input connectors.**

Caution

The ICP self test outputs approximately 30 Vdc on the input connectors. Before starting the self tests, disconnect all devices connected to the input connectors. Devices left connected during the ICP self test may be damaged.

- **Set the power switch to on (|).**
- **After calibration is complete, press the following keys:**

[**Input**]
  [ALL CHANNELS]
  [CH* FIXED RANGE]
[**System Utility**]
  [CALIBRATN]
  [AUTO CAL **OFF**]
[**Rtn**]
  [MORE]
  [SELF TEST]
  [FUNCTIONL TESTS]
  [ALL]
  [CONTINUE]

❑ Step 2. Compare the analyzer's self-test results to the following table.

- **When the tests have finished, press the following keys:**

[**Rtn**]
[TEST LOG]

- **Press the [** PREVIOUS PAGE **] softkey until the first page of test log is displayed.**

To print the test log to a GPIB printer, press the following keys:
[**Local/GPIB**]
[SYSTEM CONTROLLR]
[PRINTER ADDRESS]
(*printer address*)
[ENTER]
[**System Utility**]
[MORE]
[SELF TEST]
[TEST LOG]
[**Plot/Print**]
[<F"Times""P10 >PLOT/PRNT DEVICE]
(*device type*)
[**Rtn**]
[PLOT/PRNT DESTINATN]
[OUTPUT TO GPIB]
[**Rtn**]
[START PLOT/PRNT]

- **If the analyzer did not complete the tests (analyzer locks up), go to page 4-37 ''To troubleshoot self-test lockup failures.''**
- **If the failure is intermittent and the analyzer passed all self tests, go to page 4-40 ''To troubleshoot intermittent failures.''**
- **If the analyzer completed the tests, compare the analyzer's test log to the following table.**

If the analyzer's test log matches more than one entry on the table, use the entry closest to the beginning of the table. The table lists the probable faulty assembly or assemblies and any recommended adjustment or troubleshooting procedure to do before replacing the assembly. If both an adjustment and a test are recommended, do the adjustment first.

For additional information on the self tests, see ''Self-Test Descriptions'' on page 10-10.

Self-Test Troubleshooting Guide

Failing Self Test	Probable Faulty Assembly	Adjustment	Troubleshooting Test
Interrupt	A7 CPU		CPU, Memory, and Buses, page 4-18.
Mult Fctn Peripheral	A7 CPU		
Front Panel	A11 Keyboard Controller		
GPIB	A10 Rear Panel		
Disk Controller	A7 CPU		
Disk FIFO	A7 CPU		
IIC Bus (If only one assembly is failing)	Assembly failing. See Test Log		
IIC Bus (If multiple assemblies are failing)	See Test Log		IIC bus, page 4-25
Fast Bus	A7 CPU A6 Digital		Fast bus, page 4-29
Trigger Gate Array	A6 Digital †		
LO Gate Array	A6 Digital		
Digital Filter Gate Array	A6 Digital		
FIFO	A6 Digital		
Baseband Zoom ADC Gate Array All other self tests pass	A5 Analog		
Baseband Zoom All other self tests pass	A6 Digital		
Baseband	A5 Analog A6 Digital		Source and calibrator, page 4-45
Zoom	A5 Analog A6 Digital		Source and calibrator, page 4-45
Source through DSP	A6 Digital		
Source LO	A6 Digital		
Source to CPU	A6 Digital		

† Analyers with firmware revision A.00.00 may fail the Trigger Gate Array test when the A1/A2 Input or A5 Analog assemblies fail. Go to page 4-45, ‘’To troubleshoot source and calibrator failures,’’ to determine the probable faulty assembly.

Self-Test Troubleshooting Guide (continued)

Failing Self Test	Probable Faulty Assembly	Adjustment	Troubleshooting Test
Source With LO fails and Source Without LO passes	A6 Digital		
Source Without LO one channel	A1/A2 Input A5 Analog		Input and ADC, page 4-51 Four channel, page 4-54
Source Without LO channel 1 and 3 or channel 2 and 4	A2 Input		
Source With LO one channel	A1/A2 Input A5 Analog		Input and ADC, page 4-51 Four channel, page 4-54
Source With LO channel 1 and 3 or channel 2 and 4	A2 Input		
Input Offset one channel or channel 1 and 3 or channel 2 and 4	A1/A2 Input	Input dc offset, page 5-10	
ADC Gate Array	A5 Analog A6 Digital	ADC gain, offset, and reference, page 5-10	Source and calibrator, page 4-45
Source Without LO all channels	A5 Analog A6 Digital		Source and calibrator, page 4-45
Source With LO all channels	A5 Analog A6 Digital		Source and calibrator, page 4-45
Input Offset all channels	A5 Analog	ADC gain, offset, and reference, page 5-7	
Input Distortion one channel	A1/A2 Input A5 Analog		Input and ADC, page 4-51 Four channel, page 4-54
Input Distortion channel 1 and 3 or channel 2 and 4	A2 Input		
Input Distortion all channels	A5 Analog A6 Digital	ADC Gain, offset, and reference, page 5-7	Source and calibrator, page 4-45
Input Trigger one or more channels fail, but at least one channel passes	A5 Analog		
Input Trigger	A5 Analog A6 Digital		Trigger, page 4-62

Self-Test Troubleshooting Guide (continued)

Failing Self Test	Probable Faulty Assembly	Adjustment	Troubleshooting Test
Input A-Wt Filter one channel or channel 1 and 3 or channel 2 and 4	A1/A2 Input		
Input A-Wt Filter all channels	A6 Digital		
Input AAF/Bypass one channel or channel 1 and 3 or channel 2 and 4	A1/A2 Input	Filter flatness, page 5-17	
Input AAF/Bypass all channels	A6 Digital		
Input ICP Source † one channel or channel 1 and 3 or channel 2 and 4	A1/A2 Input		
Tachometer ‡	A6 Digital A10 Rear Panel		Tachometer, page 4-24
Source Filter	A5 Analog		
Source DC	A5 Analog		
Quick Confidence	A1/A2 Input A5 Analog A6 Digital	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7 Filter flatness, page 5-17	Performance test, page 4-42
All self tests pass		Next Step	

† This test fails if a device is connected to the front panel input connectors.
‡ This test fails if the Source output is not connected to the Tachometer input.

❑ Step 3. Determine the probable faulty assembly and next test by comparing the analyzer's symptoms to the following table.

Failure	Probable Faulty Assembly	Next Test
Disk drive	A100 Disk Drive Flexible disk Disk drive cable A7 CPU	Disk drive, page 4-57
GPIB	A10 Rear Panel †	
Serial port	A10 Rear Panel †	
Parallel	A10 Rear Panel †	
External trigger	A10 Rear Panel A5 Analog	Trigger failures, page 4-62
Tachometer	A10 Rear Panel A6 Digital	Tachometer, page 4-24
Source	A5 Analog A6 Digital	Source and calibrator, page 4-45
Autorange Overrange	A1/A2 Input A5 Analog	Auto-range, page 4-59
External keyboard	A10 F200 fuse External Keyboard A10 Rear Panel	DIN connector, page 4-61
External monitor	A7 CPU	
Microphone power Microphone adapter	A77 Microphone A5 Analog	Microphone power, page 4-69
Performance test		Performance test, page 4-42
Intermittent failure		Intermittent, page 4-40

† The circuits for the output ports are located on the A10 Rear Panel assembly except for a few output buffers on the A7 CPU assembly. If replacing the A10 Rear Panel assembly does not fix the failure, the A7 CPU assembly is probably faulty.

For additional information on the self tests, see ''Self-Test Descriptions'' starting on page 10-10.

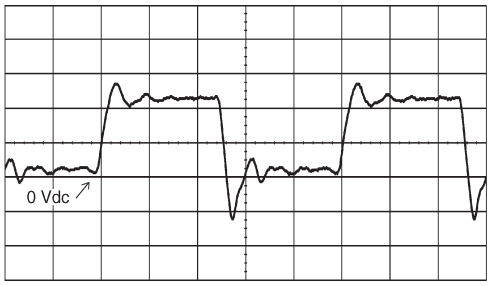
To troubleshoot self-test lockup failures

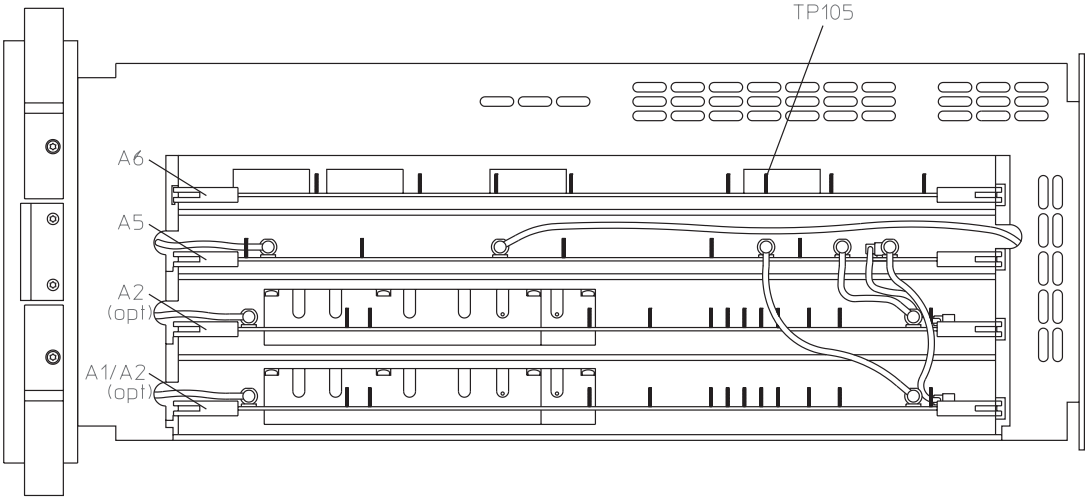
Use this test to continue troubleshooting if the analyzer locked up while running the functional test ALL.

❑ Step 1. Check the clock signal.

- **Set the power switch to on (|).**
- **Using an oscilloscope and a 1 M 10:1 probe, check the following signal.**

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A6 TP105		Time Duty Cycle	
CH1 V/div	2.0 V/div		
Input Impedance	1 MΩ		
CH1 Coupling	dc		
Probe Atten	10		
Display Mode	Repetitive		
Averaging	8		
Time/div	20 ns/div		
Trigger	Trg'd		
Trig Src	Sweep Chan1		





- **If the signal is incorrect, the A6 Digital assembly is probably faulty.**

❑ Step 2. Run the IIC and fast bus self tests.

- **Press the following keys:**

[**System Utility**]
[CALIBRATN]
[AUTO CAL **OFF**]
[**Input**]
[ALL CHANNELS]
[CH* FIXED RANGE]
1
[Vpk]
[**System Utility**]
[MORE]
[SELF TEST]
[TEST LOG]
[**Rtn**]
[FUNCTIONL TESTS]
[I/O]
[IIC BUS]

- **If the keyboard is not active, or the analyzer locks up when a key is pressed, go to page 4-25, ''To troubleshoot IIC bus failures.''**
- **Press the [** FAST BUS **] softkey.**
- **If the analyzer locks up or the digital processor failed the fast bus self test, go to page 4-29, ''To troubleshoot fast bus failures.''**

❑ Step 4. Run the remaining self tests.

- **Connect the rear panel SOURCE output to the rear panel TACH input using a BNC cable.**
- **Remove all cables from the front panel input connectors.**

Caution

The ICP self test outputs approximately 30 Vdc on the input connectors. Before starting the self tests, disconnect all devices connected to the input connectors. Devices left connected during the ICP self test may be damaged.

- **Until a test fails or the analyzer locks up, press the following keys allowing enough time for each test to complete before pressing the next key :**

[**Rtn**]
[OTHER]
[INTER RUPT]
[MULT FCTN PERIPHERL]
[MAIN RAM]
[CONTINUE]
[**Rtn**]
[DIGITAL PROCESSOR]
[ALL]
[**Rtn**]
[SOURCE]
[SOU RCE LO]
[SOURCE TO CPU]
[CONTINUE]
[**Rtn**]
[ADC GATE ARRAY]
[INPUTS]
[<F “Times”>Times"P10ALL]
[CONTINUE<| >]
[**Rtn**]
[TACHOMETR]
[CO NTINUE]

A failure may cause the self tests to run very slow. If the analyzer does not complete a self test within a few minutes (analyzer locks up during the test), consider it equivalent to displaying FAILS in the test log.

- **If any of these self tests fail, locate the test that failed in the ‘’Self-Test Troubleshooting Guide’’ on page 4-33.**
- **If the failure still is not isolated, go to page 4-45, ‘’To troubleshoot source and calibrator failures.’’**

To troubleshoot intermittent failures

Use this test to isolate intermittent failures to the assembly.

- **Determine if your intermittent failure is caused by one of the following common causes.**

Common Reasons	Troubleshooting Procedure
Loose screws and cables	Check that the screws in the analyzer are tight and that the cables are firmly in their sockets. This is especially important since grounding for the analyzer depends on the cables and screws.
Motherboard connectors	Remove each assembly connected to the Motherboard and check the connectors for loose or bent pins.
Power supply voltages	Check for correct power-supply voltages. See ''To perform initial verification'' on page 4-5.
Out-of-adjustment	Do the adjustments for the analyzer in chapter 5.
Low level noise	Do ''To troubleshoot distortion failures'' on page 4-56.
Air flow restricted	Cooling air enters from the right side and exhausts through the left side and rear panel. Check that the air flow was not restricted in these areas when the failure occurred.
External voltage	Verify that the line voltage is within the electrical specification for the analyzer. See chapter 2.

- **Connect the rear panel SOURCE output to the rear panel TACH input using a BNC cable. Remove all cables from the front panel input connectors.**

Caution

The ICP self test outputs approximately 30 Vdc on the input connectors. Before starting the self tests, disconnect all devices connected to the input connectors. Devices left connected during the ICP self test may be damaged.

- **Set the power switch to on (|).**

- **Press the following keys:**

[**Preset**]
  [DO PRESET]
[**System Utility**]
  [CALIBRATN]
  [AUTO CAL **OFF**]
[**Input**]
  [ALL CHANNELS]
  [CH* FIXED RANGE]
  1
  [Vpk]
[**System Utility**]
  [MORE]
  [SELF TEST]
  [TEST LOG]
  [CLEAR TEST LOG]
[**Rtn**]
  [LOOP MODE **ON**]
  [FUNCTIONL TESTS]
  [ALL]
  [C ONTINUE]

- **After this test detects a failure, press the following keys:**

[**Rtn**]
  [LOOP MODE **OFF**]

- **Compare the analyzer's test log to the ''Self Test Troubleshooting Guide'' starting on page 4-33.**

If the analyzer's test log matches more than one entry in the table, use the entry closest to the beginning of the table. The table lists the probable faulty assembly or assemblies and any recommended adjustment or troubleshooting procedure to do before replacing the assembly. If both an adjustment and a test are recommended, do the adjustment first.

All pass and fail messages are displayed on the test log along with the number of times a test passes or fails. When loop mode is activated, the analyzer continually repeats a test until power is cycled or loop mode is aborted by pressing the [LOOP MODE **OFF**] softkey. During some tests, the keyboard is not active and loop mode cannot be turned off. If this occurs, wait for the test to finish.

If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening, press [**Preset**] [DO PRESET] or cycle power after you abort a self test.

To run a specific self test in loop mode, press the keys listed in step 4 except select the specific self test instead of [ALL].

To troubleshoot performance test failures

With the exception of the Quick Confidence test, all functional self tests must pass before the following table is valid.

- ❑ Step 1. If the analyzer failed a performance test, compare the failing performance test to the following table.

  If more than one performance test is failing, use the entry that is closest to the beginning of the table. The table lists the probable faulty assembly or assemblies and any recommended adjustment or troubleshooting procedure to do before replacing the assembly. If both an adjustment and a test are recommended, do the adjustment first.

Failing Performance Test Troubleshooting Guide

Failing Performance Test	Probable Faulty Assembly (in order of probabilty)	Adjustment	Troubleshooting Test
DC offset one channel or channel 1 and 3 or channel 2 and 4	A1/A2 Input	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7	
DC offset all channels	A5 Analog	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7	
Amplitude accuracy one channel	A1/A2 Input A5 Analog	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7	Input and ADC, page 4-51 Four channel, page 4-54
Amplitude accuracy channel 1 and 3 or channel 2 and 4	A2 Input	Input dc offset, page 5-10	
Amplitude accuracy all channels	A5 Analog	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7	
Flatness one channel	A1/A2 Input A5 Analog	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7	Input and ADC, page 4-51 Four channel, page 4-54
Flatness channel 1 and 3 or channel 2 and 4	A2 Input	Input dc offset, page 5-10	
Flatness all channels	A5 Analog	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7	

Failing Performance Test	Probable Faulty Assembly (in order of probabilty)	Adjustment	Troubleshooting Test
Amplitude linearity one channel	A1/A2 Input A5 Analog	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7	Input and ADC, page 4-51 Four channel, page 4-54
Amplitude linearity channel 1 and 3 or channel 2 and 4	A2 Input	Input dc offset, page 5-10	
Amplitude linearity all channels	A5 Analog	Input dc offset, page 5-10 ADC gain, offset, and reference, page 5-7	
Amp_phase match	A1/A2 Input A5 Digital A6 Digital		Source and calibrator, page 4-45
A-weight filter	A1/A2 Input		
Anti-alias filter	A1/A2 Input	Filter flatness, page 5-17	
Frequency accuracy	A7 CPU	Frequency reference, page 5-5	
Input coupling	A1/A2 Input		
Single ch phase accuracy	A10 Rear Panel A5 Analog A6 Digital		Trigger, page 4-62
External trigger	A10 Rear Panel A5 Analog		Trigger, page 4-62
Input resistance	A1/A2 Input		
Input capacitance	A1/A2 Input		
Harmonic distortion one channel	A1/A2 Input A5 Analog		Input and ADC, page 4-51 Four channel, page 4-54
Harmonic distortion channel 1 and 3 or channel 2 and 4	A2 Input		
Harmonic distortion all channels	A5 Analog	ADC gain, offset, and reference, page 5-7	
Intermodulation distortion one channel	A1/A2 Input A5 Analog		Input and ADC, page 4-51 Four channel, page 4-54
Intermodulation distortion channel 1 and 3 or channel 2 and 4	A2 Input		
Intermodulation distortion all channels	A5 Analog	ADC gain, offset, and reference, page 5-7	

Failing Performance Test Troubleshooting Guide

Failing Performance Test	Probable Faulty Assembly (in order of probabilty)	Adjustment	Troubleshooting Test
Spurious signals one channel	A1/A2 Input A5 Analog		Input and ADC, page 4-51 Four channel, page 4-54
Spurious signals channel 1 and 3 or channel 2 and 4	A2 Input		
Spurious signals all channels	A5 Analog mechanical A6 Digital	ADC gain, offset, and reference, page 5-7	Distortion, page 4-56
Noise one channel	A1/A2 Input A5 Analog		Input and ADC, page 4-51 Four channel, page 4-54
Noise channel 1 and 3 or channel 2 and 4	A2 Input		
Noise all channels	A5 Analog mechanical	ADC gain, offset, and reference, page 5-7	Distortion, page 4-56
Cross talk	A1/A2 Input		Distortion, page 4-56
ICP supply	A1/A2 Input		
Source dc offset	A5 Analog		
Source amplitude accuracy	A5 Analog		
Source flatness	A5 Analog		
Source distortion	A5 Analog		
Source output resistance	A5 Analog		

To troubleshoot source and calibrator failures

Use this test to isolate source and calibrator failures to the A6 Digital assembly, the A5 Analog assembly, the A1/A2 Input assembly, the A12 BNC assembly, or the A10 Rear Panel assembly.

❑ Step 1. Check the sine wave output.

- **Set the power switch to on (|).**
- **Connect an oscilloscope to the analyzer's SOURCE connector using a BNC cable.**
- **Set the oscilloscope as follows:**

CH1 V/div	400 mV/div
Input Impedance	50 Ω
CH1 Coupling	dc
Probe Attenuation	1
Display Mode	Repetitive
Time/div	20 µs/div
Trigger	Trg'd Sweep
Trig Src	Chan1
Trigger Level	0 V

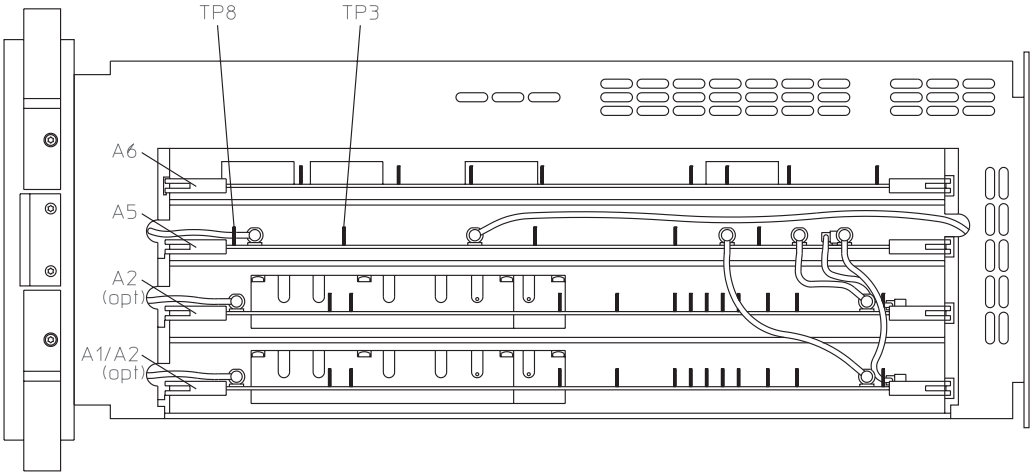
- **Press the following keys:**

[**System Utility**]
[CALIBRATN]
[AUTO CAL **OFF**]
[**Source**]
[SOURCE **ON**]
[LEVEL]
1
[Vpk]

- **If the oscilloscope displays a 10.2 kHz, 2 Vp-p sine wave with no dc offset, go to Step 2.**

This is only a quick check of the source sine wave. If the source is suspected of failing at a specific frequency or amplitude, check the source sine wave at the failing frequency or amplitude.

- **Using an oscilloscope and a 1:1 probe, check that the signal at A5 TP8 is a 10.2 kHz, 2 Vp-p sine wave with no dc offset.**
- **If the signal is correct at A5 TP8 and incorrect at the analyzer's front panel SOURCE connector, the A12 BNC assembly is probably faulty.**
- **If the signal is correct at A5 TP8 and incorrect at the analyzer's rear panel SOURCE connector, the A10 Rear Panel assembly is probably faulty.**
- **If the signal is incorrect, the A5 Analog assembly is probably faulty.**



❑ Step 2. Check the dc offset.

- **Connect the voltmeter to A5 TP3.**
- **Press the following keys:**

  [LEVEL]
  0
  [Vpk]
  [DC OFFSET]

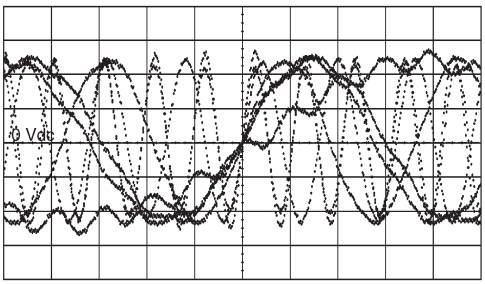
- **Rotate the RPG knob while monitoring the voltmeter.**
- **If the voltmeter's voltage does not change from +2.3 to 2.3 as the dc offset value is varied between 10 and +10 Vdc, the A5 Analog assembly is probably faulty.**

❑ Step 3. Check the periodic chirp output.

- **Press the following keys:**

  [DC OFFSET]
  0
  [V]
  [LEVEL]
  1
  [Vpk]
  [PERIODIC CHIRP]

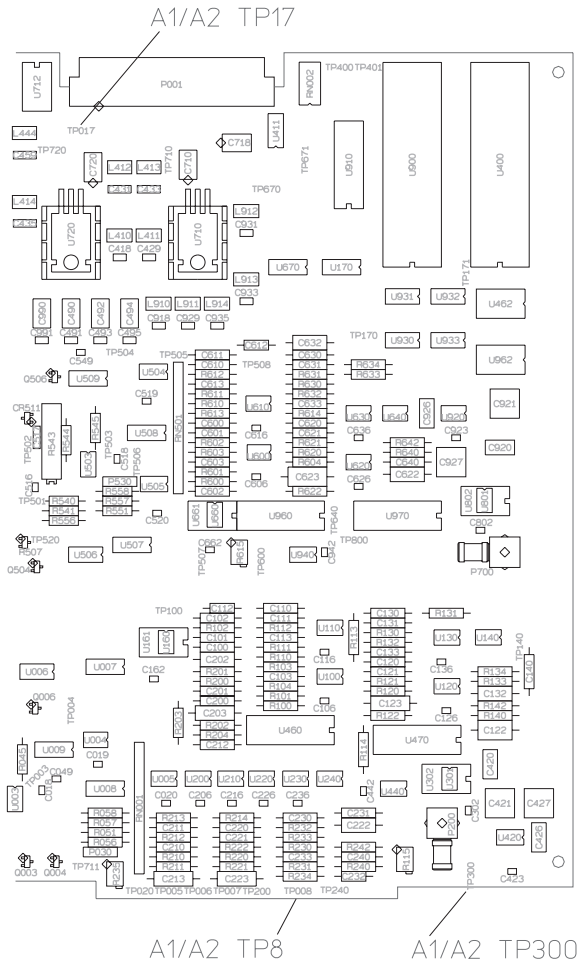
- **Using an an oscilloscope and a 1:1 probe, check the following signal.**

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A5 TP8		Amplitude Time Duty Cycle Pulse shape Time Relationship	
CH1 V/div	300 V/div		
Input Impedance	50 Ω		
CH1 Coupling	dc		
Probe Atten	1		
Display Mode	Repetitive		
Averaging	off		
Time/div	10 µs/div		
Trigger	Trg'd		
Trig Src	Sweep Chan1		
			Periodic Chirp

- **If the signal is incorrect, the A5 Analog assembly is probably faulty.**

❑ Step 4. Check the calibrator output.

- **Set the power switch to off (O).**
- **Remove the A1/A2 Input assembly and attach a test clip patch cord to TP 17. Connect a 10:1 oscilloscope probe to the patch cord and TP 8 (ground).**

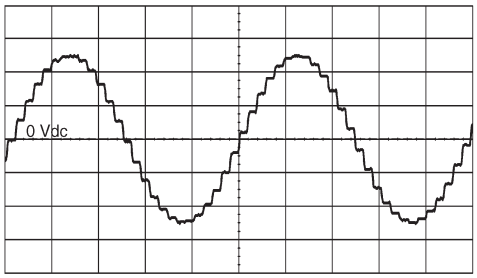


- **Reinstall the Input assembly in the card nest with patch cord and probe attacted.**
- **Set the power switch to on (|).**

- **Press the following keys:**

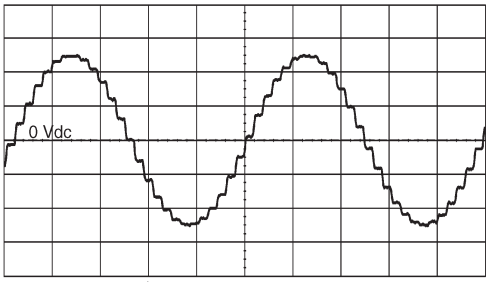
[**System Utility**]
[CALIBRATN]
[AUTO CAL **OFF**]
[**Input**]
[ALL CHANNELS]
[CH* FIXED RANGE]
1
[Vpk]
[**Source**]
[SOURCE **ON**]
[LEVEL]
1
[Vpk]
[**System Utility**]
[MORE]
[SERVICE TESTS]
[SPCL TEST MODES]
[HIGH LEVEL CAL]

- **If the signal does not look like the following figure, the A5 Analog assembly is probably faulty.**

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A1/A2 TP 17		Amplitude Time	
CH1 V/div	2 V/div		
Input Impedance	1 M Ω dc		
CH1 Coupling	10		
Probe Atten	Repetitive		
Display Mode	8		
Averaging	20 ms/div		
Time/div	Trg'd Sweep		
Trigger	Chan1		
Trig Src			

High Level Calibrator

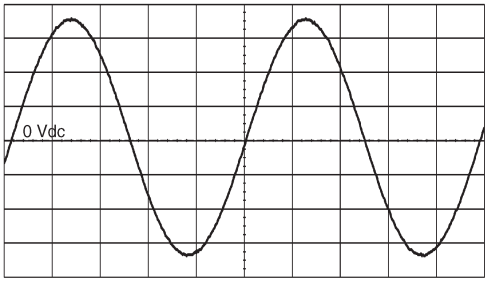
- **Press [** LOW LEVEL CAL **].**
- **If the signal does not look like the following figure, the A5 Analog assembly is probably faulty.**

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A1/A2 TP 17		Amplitude Time	
CH1 V/div	200 mV/div		
Input Impedance	1 M Ω dc		
CH1 Coupling	10		
Probe Atten	Repetitive		
Display Mode	8		
Averaging	20 ms/div		
Time/div	Trg'd Sweep		
Trigger	Chan1		
Trig Src			

Low Level Calibrator

❑ Step 5. Check the Input assembly.

- **Using an oscilloscope and a 10:1 probe, check the following signal.**

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A1/A2 TP 300		Amplitude Time Distortion	
CH1 V/div	200 mV/div		
Input Impedance	1 M Ω		
CH1 Coupling	dc		
Probe Atten	10		
Display Mode	Repetitive		
Averaging	8		
Time/div	20 ms/div		
Trigger	Trg'd Sweep		
Trig Src	Chan1		

Channel 1 Output

- **If the signal is incorrect, the A1/A2 Input assembly is probably faulty.**

❑ Step 6. Compare the analyzer's self-test results to the following table.

- **Press the following keys:**

[**System Utility**]
[MORE]
[SELF TEST]
[FUNCTIONL TESTS]
[DIGITAL PROCESSOR]
[ALL]
[**Rtn**]
[ADC GATE ARRAY]

- **Determine the probable faulty assembly by comparing the analyzer's self-test results to the following table.**

Self-Test Results	Probable Faulty Assembly
Trigger Gate Array fails and ADC Gate Array passes	A6 Digital
Baseband fails, Zoom fails, and ADC Gate Array passes	A6 Digital
ADC Gate Array fails	A5 Analog
All self tests pass through the ADC Gate Array	A5 Analog

This test does not check all the signals from the A6 Digital assembly to the A5 Analog and A1/A2 Input assemblies. All the functions of the A6 Digital assembly are checked by the self tests except for a few output buffers. If replacing the A5 Analog assembly does not fix the failure, the A6 Digital assembly is probably faulty.

To troubleshoot input and ADC failures

Use this test to isolate input failures in two channel analyzers to the A1 Input assembly, A5 Analog assembly, or A12 BNC assembly.

❑ Step 1. Check the input path.

- **Set the frequency synthesizer as follows:**

Frequency	10 kHz
Amplitude	2 Vp-p
Function	Sine Wave

- **Set the oscilloscope as follows:**

CH1 V/div	400 mV/div
Input Impedance	1 MΩ
CH1 coupling	dc
Time/div	20 ns/div
Probe Atten	1

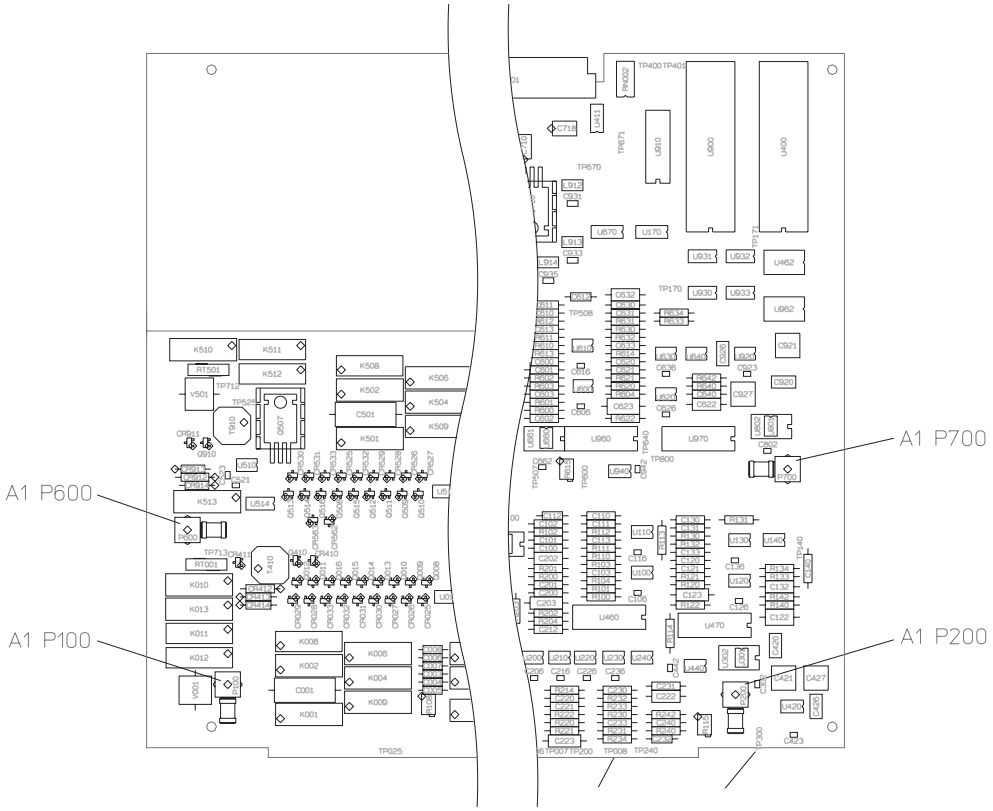
- **Press the following keys:**

[**System Utility**]
  [CALIBRATN]
  [AUTO CAL **OFF**]
[**Input**]
  [ALL CHANNELS]
  [CH* FIXED RANGE]
  1
  [Vpk]

- **Connect the frequency synthesizer to the failing channel's input connector using a BNC cable.**
- **Using the oscilloscope, BNC-to-SMB cable, and SMB-to-SMB adapter, check the following signals for the failing channel:**

Test Location	**Amplitude (** 10%)	**Probable Faulty Assembly**
Channel 1		
A12 P31 (connected to A1 P100)	2 Vp-p	A12 BNC
A1 P200	2.83 Vp-p	A1 Input
Channel 2		
A12 P41 (connected to A1 P600)	2 Vp-p	A12 BNC
A1 P700	2.83 Vp-p	A1 Input

This is only a quick check of the Input assembly. If the Input assembly's amplitude is still suspected of failing, set the analyzer to the failing range, impedance, and frequency. Connect a signal equal to the range setting to the failing channel. When the input level equals the range level, A1 P200 (channel 1) or A1 P700 (channel 2) should be 2.83 ±0.28 Vp-p.



❑ Step 2. Check the dc offset DAC.

- **Using the BNC-to-SMB cable, connect the oscilloscope to A1 P200 to check channel 1 or to A1 P700 to check channel 2.**

If you changed the input signal or range, set the input signal to 2 Vp-p and the range to 1 Vpk.

- **Set the oscilloscope to 700 mV/div.**
- **Press the following keys:**

[**System Utility**]
[MORE]
[SERVICE TESTS]
[SPCL TEST MODES]
[MORE SPCL MODES]
[CHANNEL 1 SPCL MODE] or [CHANNEL 2 SPCL MODE]
[OFFSET DAC]
0
[ENTER]

- **Note the dc offset voltage of the sine wave displayed on the oscilloscope.**
- **Enter numbers between 127 and +128.**

The sine wave dc offset voltage should change about 780 mV for a −127 entry and −780 mV for a +127 entry.

- **If the dc offset function is incorrect, the A1 Input assembly is probably faulty.**
- **If the dc offset function is correct, the A5 Analog assembly is probably faulty.**

To troubleshoot input failures on four channel analyzers

Use this test to isolate the failure when one channel fails in a four channel analyzer.

❑ Step 1. Run the input and quick confidence self tests.

- **Set the power switch to on (|).**
- **When the power-up tests are completed, press the following keys:**

[**System Utility**]
[CALIBRATN]
[AUTO CAL **OFF**]
[**Input**]
[ALL CHANNELS]
[CH* FIXED RANGE]
1
[Vpk]
[**System Utility**]
[MORE]
[SELF TEST]
[TEST LOG]
[**Rtn**]
[FUNCTIONL TESTS]
[INPUTS]
[ALL]
[CONTINUE]
[**Rtn**]
[**Rtn**]
[QUICK CONF TEST]

- **If the self tests fail but do not lockup the analyzer, note the failure messages and go to Step 2.**
- **If the analyzer locks up on the Quick Confidence self test but not on the input self tests, note the failure messages and go to Step 2 but don't run the Quick Confidence self test.**
- **If the analyzer locks up on the input self tests, go to Step 2 to determine if exchanging the Input assemblies will allow the self tests to run.**

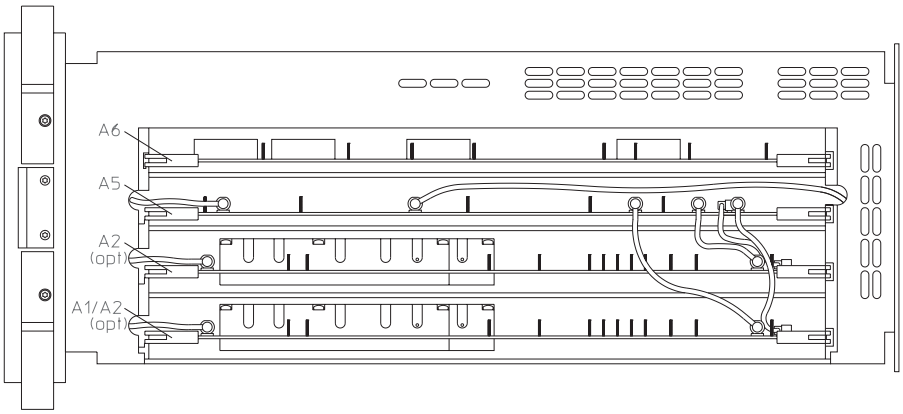
This is most likely to occur when channel 1 and 3 are failing.

- **If the self tests pass, go to Step 2 but substitute the failure symptom for the self tests.**

If the exact failure symptom is not known, use the performance test procedures to isolate the failure symptom.

❑ Step 2. Exchange the Input assemblies.

- **Set the power switch to off (○).**
- **Exchange the Input assembly in the lower slot with the Input assembly in the upper slot.**



- **Reconnect the cables to the A5 Analog assembly.**
- **Set the power switch to on (|).**
- **Press the following keys:**

[**System Utility**]
[CALIBRATN]
[AUTO CAL OFF]
[**Input**]
[ALL CHANNELS]
[CH* FIXED RANGE]
1
[Vpk]
[**System Utility**]
[MORE]
[SELF TEST]
[TEST LOG]
[**Rtn**]
[FUNCTIONL TESTS]
[INPUTS]
[ALL]
[CONTINUE]
[**Rtn**]
[**Rtn**]
[QUICK CONF TEST]

- **If the same channel fails as failed before the exchange, the A5 Analog assembly is probably faulty.**
- **If a different channel now fails, the A2 Input assembly for the failing channel is probably faulty.**

The Input assembly for channel 1 and 3 is in the lower slot. The Input assembly for channel 2 and 4 is in the upper slot.

To troubleshoot distortion failures

Use this test to isolate distortion failures to the A1/A2 Input assembly, the A5 Analog assembly, or to mechanical failures.

❑ Step 1. Check mechanical ground connections.

- **Check that the Digital assembly, Input assembly, and Analog assembly are completely in the card nest and making good contact with the grounding guides at the sides of the card nest.**
- **Check that the screws in the sides, back, and top of the analyzer are tight.**

When grounding is inadequate, feedback from the line power frequency and internal clock frequencies may appear as distortion on the Input assemblies.

❑ Step 2. Check the analyzer's clock signals.

Noisy clock signals can cause noise or spurious signals in the analyzer. To check the analyzer's clocks, go to page 4-5 ''To perform initial verification'' and do Step 6.

❑ Step 3. Do the "Spurious signals" and ''Noise'' performance tests.

- **Run the "Spurious signals" and ''Noise'' performance tests in chapter 3, ''Verifying Specifications.''**
- **If all channels fail, the A5 Analog assembly is probably out of adjustment or faulty.**

Do the ''ADC gain, offset and reference'' adjustment on page 5-7 before replacing the assembly.

- **If only one channel, or channel 1 and 3, or channel 2 and 4 fails, the Input assembly that failed is probably faulty.**
- **If the ''Spurious signals'' and ''Noise'' performance tests pass, but the analyzer appears to power up with a high noise floor, an auto-range circuit may be failing.**

To check the auto-range function and isolate a failure, see ''To troubleshoot auto-range failures'' on page 4-59.

To troubleshoot disk drive failures

This test isolates disk drive failures to the A7 CPU, the A100 Disk Drive assembly, or the flexible disk.

❑ Step 1. Check the disk controller on the A7 CPU assembly.

- **Press the following keys:**

[**System Utility**]
[MORE]
[SELF TEST]
[TEST LOG]
[**Rtn**]
[FUNCTIONL TESTS]
[I/O]
[INTERNAL DISK]
[DISK CONTROLLR]
[DISK FIFO]

- **If the disk controller test aborts and displays the message** Mass Storage Unit not Present!!**, the Disk Drive assembly, or the cable to the Disk Drive assembly is probably faulty. The A7 CPU assembly could also be faulty but it is less probable.**
- **If the disk controller or disk FIFO test fails, the A7 CPU assembly is probably faulty.**

❑ Step 2. Check the Disk Drive assembly.

- **Insert a formatted flexible disk into the Disk Drive assembly and press the following keys:**

[RESTORE]
[RANDOM SEEK]
[SEEK RECORD]
(*any number between 1 and 2771*)
[READ]
[READ/WRITE]

- **If any of the self tests failed, insert a new formatted disk and repeat the previous step.**
- **If the disk drive self tests still fail, the A100 Disk Drive assembly is probably faulty.**

If the self test aborts and displays the message Bad or unformatted media, the most likely cause of the failure is a bad flexible disk. The analyzer can use either LIF (Logical Interchange Format) or a DOS formatted flexible disk.

❑ Step 3. Check that the Disk Drive assembly can read and write to all sectors of a flexible disk.

The read/write self test can take up to 40 minutes to complete if there are no failures.

- **Press the [** READ/WRITE ALL **] softkey.**
- **If the self test aborts and displays the message** Bad or unformatted media**, insert a new formatted disk and repeat the previous step.**
- **If the self test fails a second time, the Disk Drive assembly is probably faulty.**
- **If the self test passes, the Disk Drive assembly and flexible disk are functioning correctly.**

To troubleshoot auto-range failures

Use this test to check the auto-range and overload detector circuits on the A1/A2 Input assembly. This test assumes that calibration and all self tests passed.

- **Set the power switch to on (|).**
- **Press the following keys:**

[**System Utility**]
[CALIBRATN]
[AUTO CAL **OFF**]
[**Inst Mode**]
[CHANNELS 4] or [CHANNELS 2]
[**Input**]
[ALL CHANNELS]
[CH* FIXED RANGE]
1
[dBVrms]
[**Source**]
[SOURCE **ON**]
[LEVEL]
1
[dBVrms]
[**System Utility**]
[MORE]
[SERVICE TESTS]
[SPCL TEST MODES]
[SOURCE LEVEL]

The Half range LEDs for all channels should be on and the Over range LEDs should be off.

- **Press the following keys:**

[**Source**]
[LEVEL]
5
[dBVrms]

The Half range and Over range LEDs for all channels should be on.

- **Press the following keys:**

[**Input**]
[CH* AUTO RANGE]

After the auto-range routine is finished, the Half range LEDs should be on and the Over range LEDs should be off.

- **Press the following keys:**

  [CHANNEL 1]
  [CHANNEL 1 RANGE]

The range should be set to 5 dBVrms.

- **Press [Rtn].**
- **Repeat steps 5 and 6 for each channel.**
- **If only one channel, or channel 1 and 3, or channel 2 and 4 are failing, the A1/A2 Input assembly is probably faulty.**

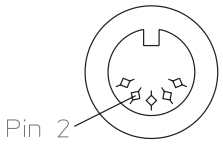
In the two channel analyzer, the A1 Input assembly provides the circuits for channel 1 and 2. In the four channel analyzer, the A2 Input assembly in the lower slot provides the circuits for channel 1 and 3, and the A2 Input assembly in the upper slot provides the circuits for channel 2 and 4.

- **If all channels are failing, the A5 Analog assembly is probably faulty.**

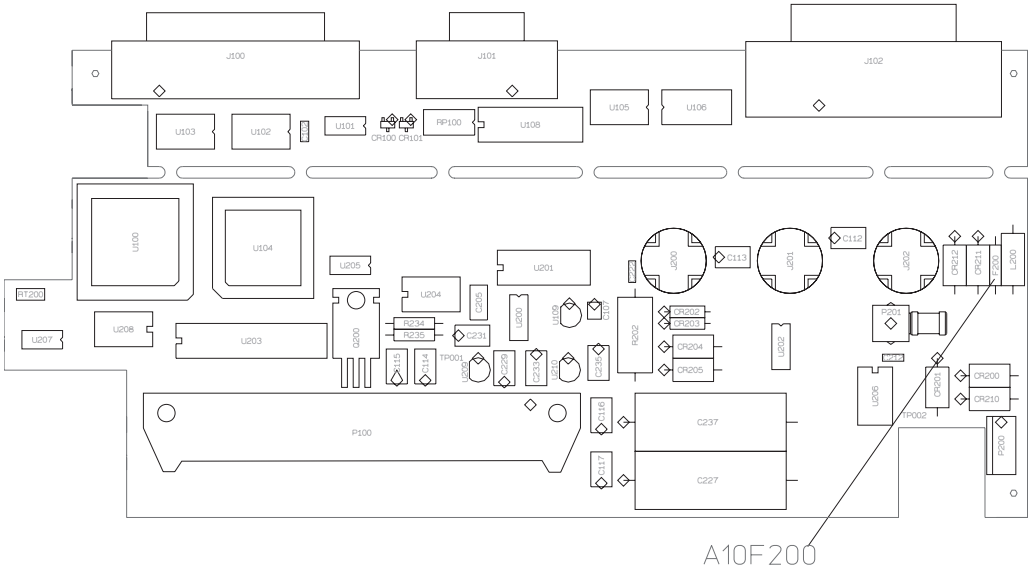
To troubleshoot DIN connector failures

Use this test to determine if the fuse for the DIN connector is failing before replacing the A10 Rear Panel assembly.

- **Set the power switch to on (|).**
- **Check the voltage on pin 2 of the DIN connector for +5V.**



- **If the voltage is correct, the A10 Rear Panel assembly is probably faulty.**
- **If the voltage is incorrect, replace A10 F200.**



To troubleshoot trigger failures

Use this test when the trigger mode is suspected of failing or the Input Trigger self test fails on all channels.

❑ Step 1. Check trigger modes.

- **Set the power switch to on (|).**
- **Press the following keys:**

[System Utility]
  [CALIBRATN]
  [AUTO CAL OFF]
[**Input**]
  [ALL CHANNELS]
  [CH* FIXED RANGE]
  1
  [Vpk]
[**Source**]
  [SOURCE **ON**]
  [LEVEL]
  1
  [Vpk]
  [FIXED SINE]
  [1]
  [kHz]
[**Inst Mode**]
  [4 CHANNEL] or [2 CHANNEL]
  [ACTIVE TRACE]
  [A B C D] or [A B]
[**Meas Data**]
  [ALL CHANNELS]
  [TIME CHANNEL]
[**System Utility**]
  [MORE]
  [SERVICE TESTS]
  [SPCL TEST MODES]
  [SOURCE LEVEL]
[**Trigger**]
  [SOURCE TRIGGER]

- **If the analyzer is not triggering and the message** WAITING FOR SOURCE TRIGGER **is displayed, the A6 Digital assembly is probably faulty.**

Fixed sine wave source triggering occurs at a consistent (but not predictable) point within the time record.

- **Set the frequency synthesizer as follows:**

Frequency	1 kHz
Amplitude	6 Vp-p
Function	Square Wave

- **Connect the frequency synthesizer to the analyzer's rear panel EXT TRIG connector using a BNC cable.**
- **Press the following keys allowing enough time for the analyzer to trigger before pressing the next key. Note which trigger modes are failing:**

[CHANNEL 1]
[CHANNEL 2]
[CHANNEL 3] (option AY6 only)
[CHANNEL 4] (option AY6 only)
[TRIGGER SETUP]
[CHANNEL LEVEL]
200
[mV]
[SLOPE NEG]
[ALL CHANNELS]
[CHANNEL DELAY]
100
[mS]
[0]
[S]
[**Rtn**]
[ARM SETUP]
[MANUAL ARM]
[**Rtn**]
[ARM]
[ARM SETUP]
[AUTOMATIC ARM]
[**Rtn**]
[EXTERNAL TRIGGER]
[TRIGGER SETUP]
[EXT LEVEL TTL]
[EXT LEVEL USER]
[USER EXT LEVEL]
200
[mV]
[EXT RANGE +/– 10]
[USER EXT LEVEL]
0
[V]

The message WAITING FOR mode TRIGGER is displayed when the analyzer is not triggering.

- **Change the frequency synthesizer's amplitude to 0.3 Vp-p.**
- **Press [** EXT RANGE +/ 2 **].**

The analyzer should now trigger.

❑ Step 2. Determine the probable faulty assembly or next step by comparing the trigger failure to the following table.

If the trigger failure matches more than one entry in the table, use the entry closest to the beginning of the table.

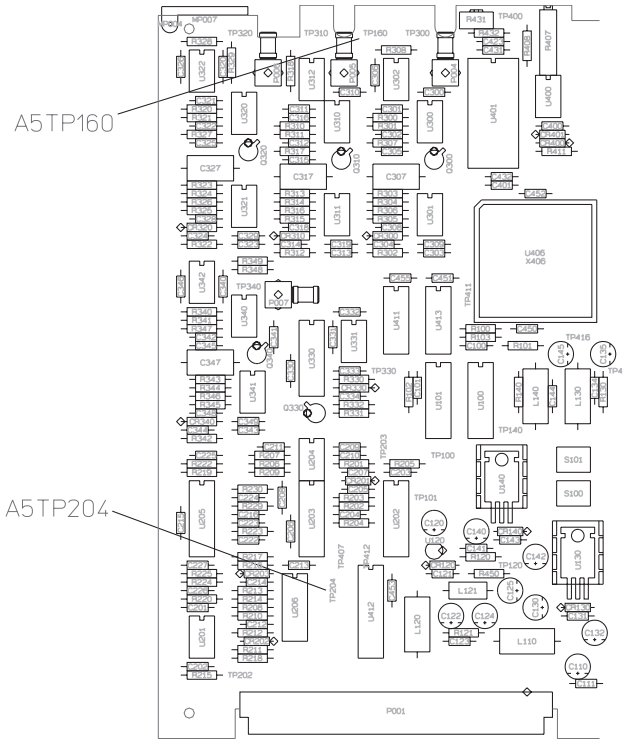
Trigger Mode Failing	Probable Faulty Assembly or Next Step
All channels and external trigger fail all trigger modes	Step 3
All channels trigger but external trigger fails all trigger modes	Step 4
At least one channel or external trigger functions correctly	A5 Analog
Channel level fails Arm fails External trigger fails user level or TTL level	A5 Analog
External trigger fails EXT RANGE	A10 Rear Panel
Trigger delay fails	A6 Digital

❑ Step 3. Check trigger signal to Digital assembly.

- **Set the power switch to off (O).**
- **Remove the A5 Analog assembly and attach a test clip patch cord to TP 204.**
- **Connect a logic probe to the patch cord and TP 160 (ground).**
- **Reinstall the Analog assembly in the card nest with patch cord and probe attached.**
- **Set the power switch to on (I).**
- **Press the following keys:**

[**System Utility**]
  [CALIBRATN]
  [AUTO CAL **OFF**]
[**Input**]
  [ALL CHANNELS]
  [CH* FIXED RANGE]
  1
  [Vpk]
[**Source**]
  [SOURCE ON]
  [LEVEL]
  [1]
  [Vpk]
[**System Utility**]
  [MORE]
  [SERVICE TESTS]
  [SPCL TEST MODES]
  [SOURCE LEVEL]
[**Trigger**]
  [CHANNEL 1]

- **If the signal at A5 TP 204 is toggling, the A6 Digital assembly is probably faulty.**
- **If the signal at A5 TP 204 is not toggling, the A5 Analog assembly is probably faulty.**



❑ Step 4. Check external trigger signal to the Analog assembly.

- **Set the power switch to off (O).**
- **Remove the seven screws holding the rear panel to the analyzer and lean the rear panel back until the A10 Rear Panel assembly is visible. Keep the cables connected.**
- **Set the power switch to on (|).**
- **Change the frequency synthesizer's amplitude to 2 Vp-p.**
- **Set the oscilloscope as follows:**

CH1 V/div	100 mV/div
Input Impedance	1 MΩ
CH1 Coupling	dc
Time/div	200 µs/div
Probe Atten	10

- **Connect the oscilloscope to A10 TP2 using a 10:1 probe.**
- **Press the following keys:**

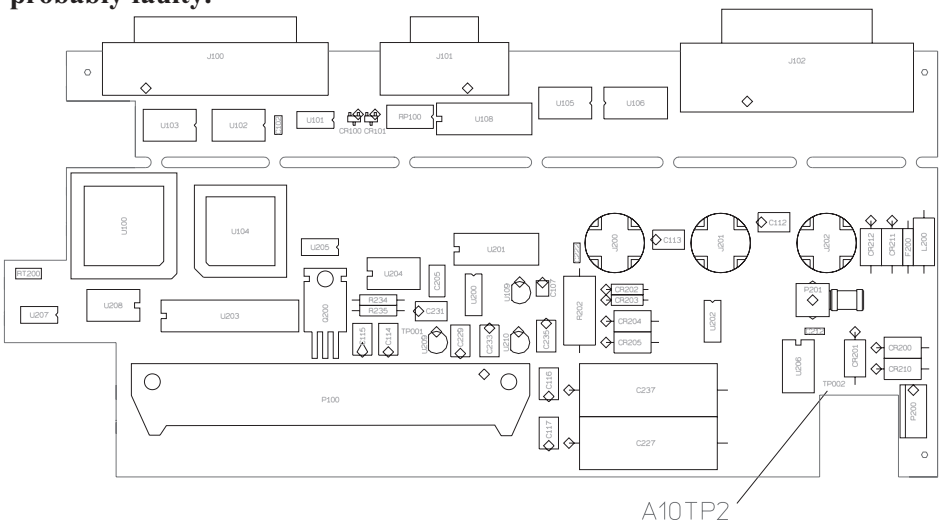
[**Trigger**]
[EXTERNAL TRIGGER]
[TRIGGER SETUP]
[EXT LEVEL USER]
[EXT RANGE +/– 10]

The oscilloscope should display a 370 ⁄ 40 mVp-p square wave.

- **If the signal is incorrect, the A10 Rear Panel assembly is probably faulty.**
- **Set the oscilloscope to 300 mV/div.**
- **Press [** EXT RANGE +/ 2 **].**

The oscilloscope should display a 1.9 ⁄ 0.2 Vp-p square wave.

- **If the signal is incorrect, the A10 Rear Panel assembly is probably faulty.**
- **If the external trigger signals are correct, the A5 Analog assembly is probably faulty.**



To troubleshoot memory battery failures

Use this test when battery-backed-up memory is suspected of failing. This test separates Memory assembly failures from memory battery failures.

- **Press the following keys:**

[**Preset**]
[DO PRESET]
[**System Utility**]
[CLOCK SETUP]
[DATE MMDDYY]
010101
[ENTER]

- **Set the power switch to off (O), then to on (I).**
- **Press the following keys:**

[**System Utility**]
[CLOCK SETUP]
[DATE MMDDYY]

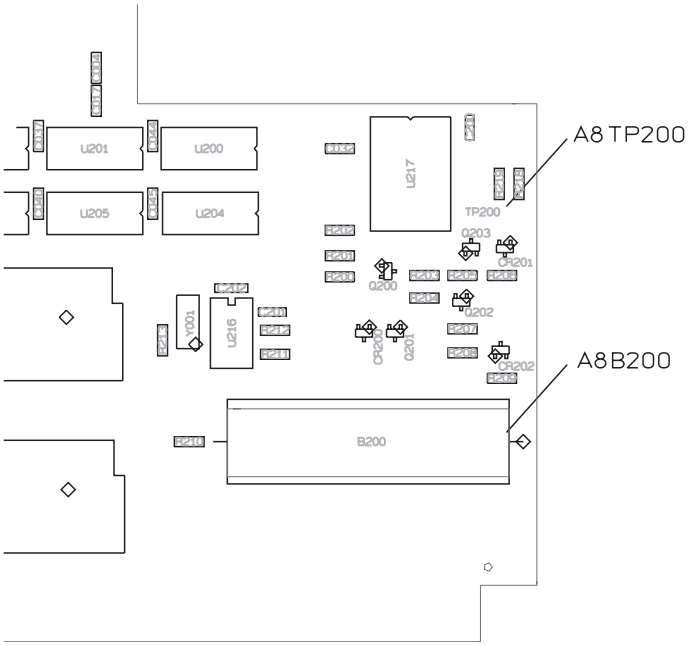
- **If the date is 01-01-01, the battery-backed-up memory is functioning correctly. Enter the current date. Go to page 4-31, ''To perform self tests,'' to continue troubleshooting.**
- **If the date is incorrect, remove the Memory assembly.**

See ''To remove memory'' on page 6-13.

- **Check that the voltage at TP200 is 3.5 1V.**
- **If the voltage is correct, the Memory assembly is probably faulty.**
- **If the voltage is incorrect, replace the battery (B200).**

Caution

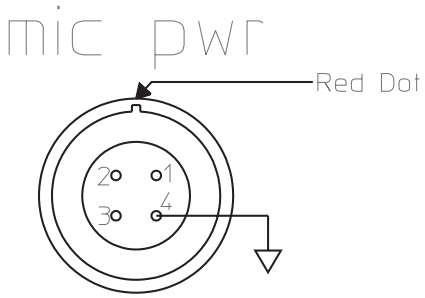
There is danger of explosion if battery is incorrectly replaced. Replace the battery with the same or an equivalent type listed on page 7-12. Discard used batteries according to the battery manufacturer's instructions.


A8 TP200
A8 B200
U201
U200
U205
U204
U217
TP200
Q203
CR201
Q200
Q202
CR202
Y001
U216
B200

To troubleshoot microphone power and adapter failures

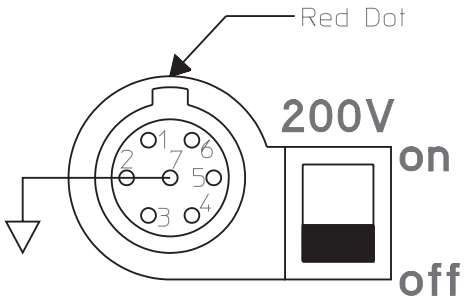
Use this test to isolate Microphone failures to the A5 Analog assembly or option UK4, Microphone Adapter and Power Supply.

❑ Step 1. Check mic pwr on the analyzer's front panel.
- **Set the power switch to on (|).**
- **Check the voltage on pin 2 of the mic pwr connector for +8 ±0.5 Vdc.**



- **If the voltage is incorrect, the A5 Analog assembly is probably faulty.**

❑ Step 2. Check the power from the Microphone Adapter and Power Supply.
- **Connect the mic cable to the analyzer's mic pwr connector.**
- **Check the voltage on pins 5 and 6 of each microphone connector for 28±2.8 Vdc.**



- **If the voltage is incorrect, the A77 Microphone assemby in the Microphone Adapter and Power Supply is probably faulty.**
- **Set the switch for each microphone connector to off.**
- **Check the voltage on pin 3 of each connector for 0 Vdc.**
- **Set the switch for each microphone connector to on.**
- **Check the voltage on pin 3 of each connector for 200 15 Vdc.**
- **If the voltage is incorrect, the A77 Microphone assembly in the Microphone Adapter and Power Supply is probably faulty.**

To troubleshoot tachometer failures

Use this test to isolate tachometer failures to the A10 Rear Panel assembly or A6 Digital assembly.

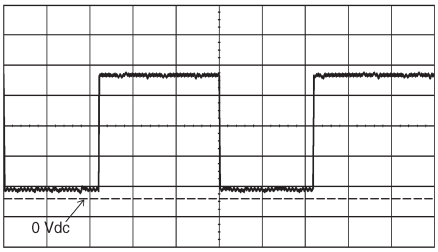
❑ Step 1. Check the rear panel tachometer input.

- **Set the power switch to off (O).**
- **Remove the seven screws holding the rear panel to the analyzer and lean the rear panel back until the A10 Rear panel assembly is visible. Keep the cables connected.**
- **Connect the SOURCE output to the TACH input on the rear panel using a BNC cable.**
- **Set the power switch to on (|).**
- **Press the following keys:**

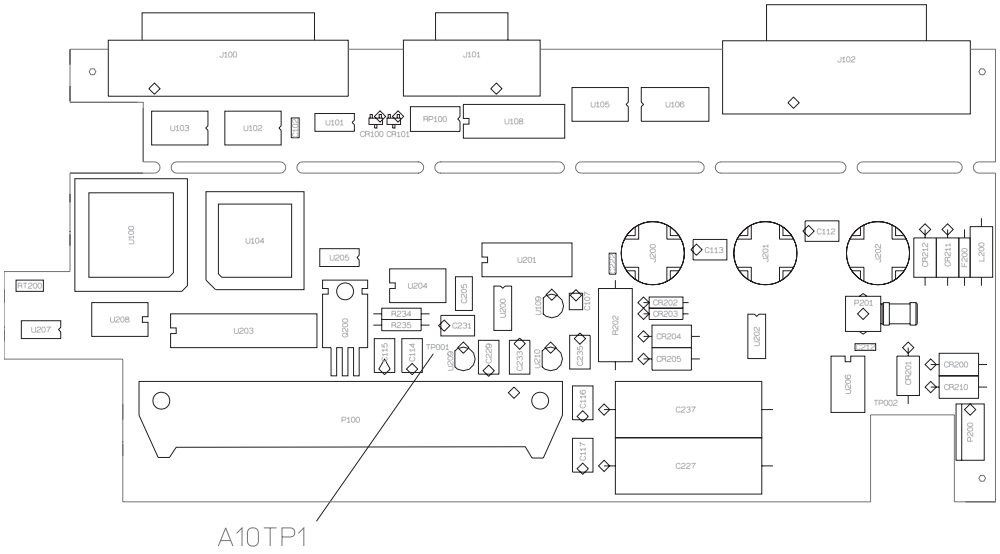
[**System Utility**]
[CALIBRATN]
[AUTO CAL **OFF**]
[**Rtn**]
[MORE]
[SELF TEST]
[LOOP MODE **ON**]
[FUNCTIONL TESTS]
[TACHOMETR]
[CONTINUE]

- **Using an oscilloscope and 1 M 10:1 probe, check the following signal.**

The signal should be displayed while the self test is running. Each time the self test restarts, the source output to the tachometer input will be interrupted.

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A10 TP1		Amplitude Time Duty Cycle Pulse shape	
CH1 V/div	1 V/div		
Input Impedance	1 M Ω		
CH1 Coupling	dc		
Probe Atten	10		
Display Mode	Real Time		
Time/div	2 ms/div		
Trigger	Auto		

- **If the signal is incorrect, the A10 Rear Panel assembly is probably faulty.**



❑ Step 2. Check the tachometer range function.

- **Set the oscilloscope for 20 s/div.**
- **Press the following keys:**

[**Rtn**]
[LOOP MODE **OFF**]
[**Rtn**]
[SERVICE TESTS]
[SPCL TEST MODES]
[SOURCE LEVEL]
[**Source**]
[SOURCE **ON**]
[LEVEL]
500
[mVpk]
[**Trigger**]
[TACHOMETR SETUP]
[TRG RANGE +/– **20**]

- **Check that the oscilloscope displays a dc voltage of approximately 4 Vdc.**
- **Press [** TRG RANGE +/ **4].**
- **Check that the oscilloscope displays a 4 0.4 Vp-p, 10.24 kHz sine wave, with 2 ±0.2 Vdc offset.**
- **If the signal is incorrect, the A10 Rear Panel assembly is probably faulty.**
- **If the signal is correct, the A6 Digital assembly is probably faulty.**

5

Adjusting the Analyzer

Adjusting the Analyzer

This chapter contains the adjustment procedures for the Agilent 35670A Dynamic Signal Analyzer. Use these adjustments if the analyzer does not meet its specifications or if instructed in chapter 4, ‘’Troubleshooting the Analyzer,’’ or chapter 6, ‘’Replacing Assemblies,’’ to perform these adjustments. These adjustments are not required for routine maintenance.

Allow the Agilent 35670A analyzer to warm up for an hour before doing any of the adjustments.

During many of these adjustment procedures, an adjustment message appears on the screen. The instructions on the screen are not as complete as the instructions in this guide. When an adjustment message appears on the screen, continue to follow the instructions in this guide. Failure to follow the instructions in this guide may result in an incorrect adjustment, which would appear as a hardware failure.

The following table shows the assembly and components adjusted during each adjustment procedure.

Adjustment	Assembly	Component
Frequency reference	A7 CPU	A7 C85
Source	A5 Analog	A5 R48 A5 R59
ADC gain, offset and reference	A5 Analog	A5 R407 A5 R405 A5 R431
Input dc offset	A1/A2 Input	A1/A2 R39 A1/A2 R539
Common mode rejection	A1/A2 Input	A1/A2 R43 A1/A2 R543
Filter flatness	A1/A2 Input	A1/A2 R115 A1/A2 R235 A1/A2 R615
Display voltage	A102 DC-DC Converter	A102 R25

Safety Considerations

Although the Agilent 35670A analyzer is designed in accordance with international safety standards, this guide contains information, cautions, and warnings that must be followed to ensure safe operation and to keep the unit in safe condition. Adjustments in this chapter are performed with power applied and protective covers removed. These adjustments must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Warning

Any interruption of the protective (grounding) conductor inside or outside the unit, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the Agilent 35670A analyzer. There are no operator controls inside the analyzer.

Equipment Required

See chapter 1, ''Specifications,'' for tables listing recommended test equipment. Any equipment which meets the critical specifications given in the tables may be substituted for the recommended model.

Remote Operation

Adjustments can be set up using the remote operation capability of the Agilent 35670A analyzer. The following table lists the adjustments and corresponding GPIB codes. See the *Agilent 35670A GPIB Programmer's Guide* for general information on remote operation.

Adjustment	GPIB Code
Source DC Offset	DIAG:SERV:ADJ:SOUR:OFFS
Source Filter DC Offset	DIAG:SERV:ADJ:SOUR:FILT:OFFS
ADC Second Pass Gain	DIAG:SERV:ADJ:ADC:GAIN
ADC Offset	DIAG:SERV:ADJ:ADC:OFFS
Channel 1 Offset	DIAG:SERV:ADJ:OFFS1
Channel 2 Offset	DIAG:SERV:ADJ:OFFS2
Channel 3 Offset (option AY6 only)	DIAG:SERV:ADJ:OFFS3
Channel 4 Offset (option AY6 only)	DIAG:SERV:ADJ:OFFS4
Channel 1 Common Mode Rejection	DIAG:SERV:ADJ:CMRR1
Channel 2 Common Mode Rejection	DIAG:SERV:ADJ:CMRR2
Channel 3 Common Mode Rejection (option AY6 only)	DIAG:SERV:ADJ:CMRR3
Channel 4 Common Mode Rejection (option AY6 only)	DIAG:SERV:ADJ:CMRR4
Channel 1 Flatness at 100 kHz	DIAG:SERV:ADJ:FLAT1:FULL
Channel 1 Flatness at 50 kHz (option AY6 only)	DIAG:SERV:ADJ:FLAT1:FULL
Channel 1 Flatness at 50 kHz	DIAG:SERV:ADJ:FLAT1:CENT
Channel 1 Flatness at 25 kHz (option AY6 only)	DIAG:SERV:ADJ:FLAT1:CENT
Channel 2 Flatness at 50 kHz	DIAG:SERV:ADJ:FLAT2:FULL
Channel 2 Flatness at 25 kHz (option AY6 only)	DIAG:SERV:ADJ:FLAT2:CENT
Channel 3 Flatness at 25 kHz (option AY6 only)	DIAG:SERV:ADJ:FLAT3:FULL
Channel 4 Flatness at 25 kHz (option AY6 only)	DIAG:SERV:ADJ:FLAT4:FULL
Preset	SYST:PRES

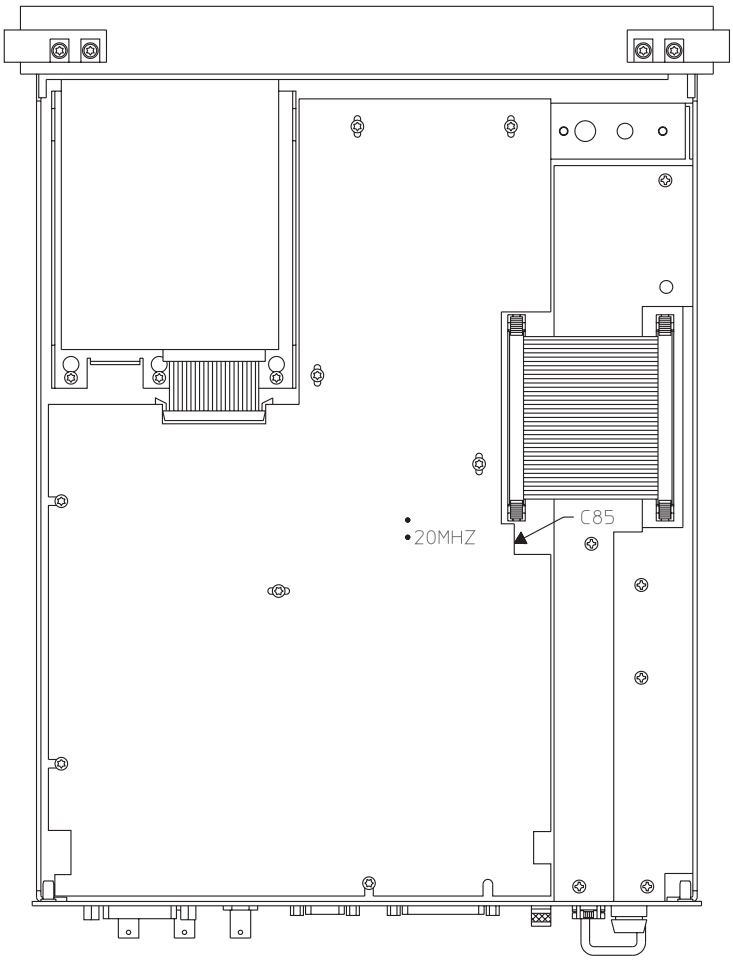
To adjust the frequency reference

This procedure adjusts the 19.923 MHz (or, to be exact, 19.922944 MHz) frequency reference circuit on the A7 CPU assembly. This circuit is the source of the timing reference for the A1/A2 Input and A5 Analog assemblies.

Equipment Required: Frequency Counter
10:1 Oscilloscope Probe

- **Set the power switch to off (O).**
- **Connect the counter to the 20 MHz test point on A7 using a 10:1 oscilloscope probe. Attach the probe ground clip to the instrument chassis (ground).**
- **Set the power switch to on (|).**
- **Adjust A7 C85 for a counter reading of 19.922944 MHz ±200 Hz.**

The analyzer may lock up if C85's plates touch each other during the adjustment. If the analyzer locks up, cycle power.



To adjust the source

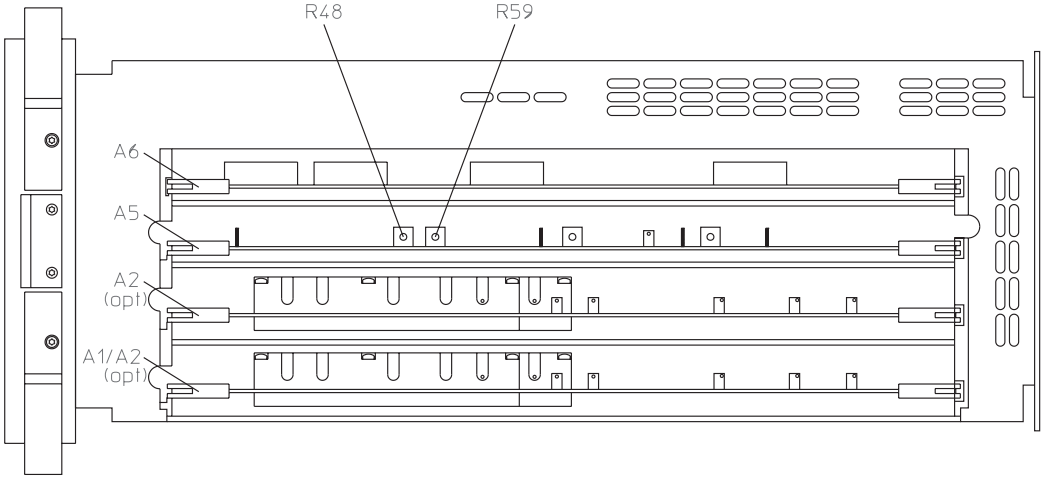
This procedure adjusts the source dc offset on the A5 Analog assembly.

Equipment Required: Multimeter
BNC-to-Dual Banana Cable

- **Connect the multimeter to the analyzer's rear-panel SOURCE connector.**
- **Press the following keys:**

[**System Utility**]
[MORE]
[SERVICE TESTS]
[ADJUSTMTS]
[SOURCE ADJUSTMNT]
[DC OFFSET]

- **Adjust A5 R48 for 0 Vdc±1 mV.**
- **Press the [** FILTER DC OFFSET **] softkey.**
- **Adjust A5 R59 for 0 Vdc ±1 mV.**

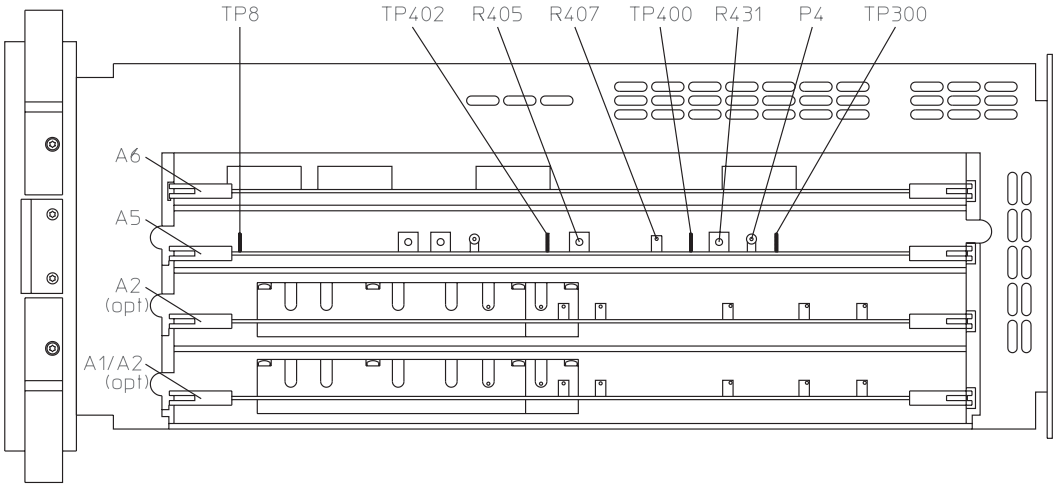


To adjust the ADC gain, offset and reference

This procedure adjusts the second-pass gain, the first-pass offset, and the reference voltage for the ADC on the A5 Analog assembly. This prevents nonlinear Analog-to-Digital Converter (ADC) operation near the Digital-to-Analog Converter (DAC) transition levels.

Equipment Required: Oscilloscope
1:1 Oscilloscope Probe
Capacitive Load
BNC-to-BNC Cable

- **Set the power switch to off (O).**
- **Connect the capacitive load (from the service kit) to the oscilloscope input. Connect the 1:1 oscilloscope probe to the capacitive load. Attach the probe to A5 TP400 and the probe ground clip to the instrument chassis.**



- **Connect the oscilloscope's external trigger connector to the analyzer's SOURCE connector using a BNC cable.**

- **Set the oscilloscope as follows:**

Channel 1	Volts/Div	20 mV/div
	Offset	0V
	Coupling	1 MΩ ac
Channel 2	Volts/Div	500 mV/div
	Offset	0V
	Coupling	1 MΩ ac
Time Base	Time/Div	1.0 ms/div
	Sweep	Triggered
Trigger	Source	Channel 2
	Level	500 mV
	Slope	Positive
	Mode	Edge
Display	Mode	Repetitive
	Averaging	On
	No. of Avg.	8
	Screen	Single

- **Remove the cable from A5 P4. Connect a jumper from A5 TP8 to A5 TP300.**
- **Press [Preset] while setting the power switch to on (|).**
- **Press the following keys:**

[**System Utility**]
[MORE]
[SERVICE TESTS]
[ADJUSTMTS]
[ADC ADJUSTMNT]
[SECOND PASS GAIN]

Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.

- **Adjust A5 R407 for a flat trace on the oscilloscope.**
- **Set the power switch to off (○).**
- **Disconnect the capacitive load and connect the 1:1 oscilloscope probe directly to the oscilloscope input. Attach the probe to A5 TP402 and the probe ground clip to the instrument chassis.**
- **Change the set up for the oscilloscope as follows:**

Channel 1	Volts/Div	115 mV/div
	Coupling	1 MΩ dc
Channel 2	Coupling	1 MΩ dc
Time Base	Time/Div	500 ms/div
Display	Averaging	off
	Display time	2.00 s

- **Set the power switch to on (|).**

- **Press the following keys:**

[**System Utility**]
[MORE]
[SERVICE TESTS]
[ADJUSTMTS]
[ADC ADJUSTMNT]
[OFFSET]

Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.

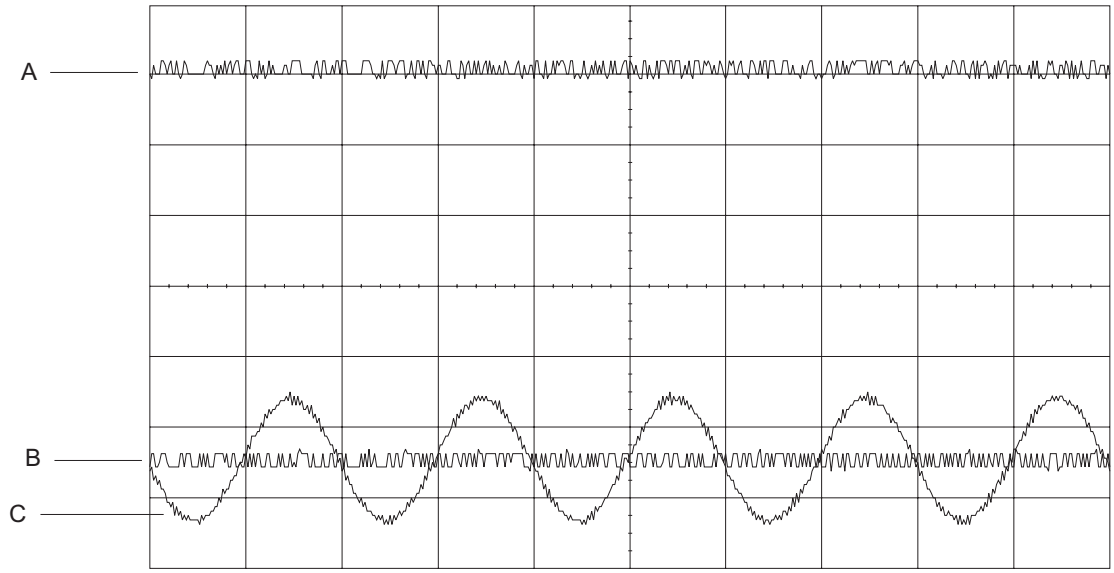
- **If the oscilloscope display looks like the following figure, go to step 17.**

The following describes the signals shown on the oscilloscope display:

''A'' A straight, horizontal trace in the upper half of the display.

''B'' A "noisy" flat trace at the center of the sine wave trace.

''C'' A clean sine wave in the lower half of the display.



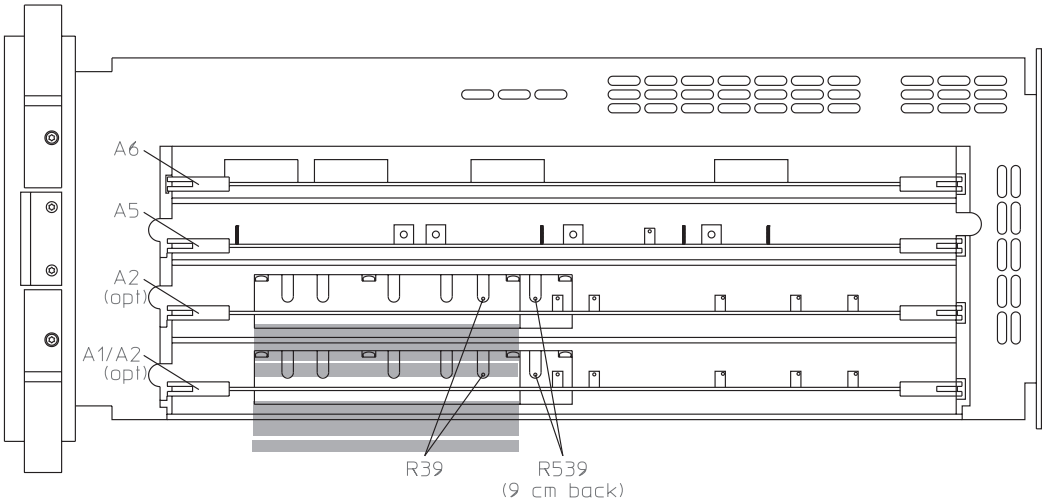
R431 and R405 Correctly Adjusted

- **If trace ''B'' is not flat, adjust A5 R431.**
- **If trace ''C'' is not centered over trace ''B,'' adjust A5 R405.**
- **Set the power switch to off (O).**
- **Disconnect the jumper from A5 TP8 and A5 TP300. Reconnect the cable to A5 P4.**

To adjust the input dc offset

This procedure minimizes the residual dc response of the A1/A2 Input assemblies. The standard two channel analyzer has one A1 Input assembly. The optional four channel analyzer has two A2 Input assemblies: channel 1 and 3 are routed to the A2 Input assembly in the lower slot and channel 2 and 4 are routed to the A2 Input assembly in the upper slot.

Equipment Required: None



- For the standard two channel analyzer, do the following to adjust input dc offset:
  - **Set the power switch to on (|).**
  - **Press the following keys:**

    [System Utility]
    [MORE **]**
    [SERVICE TESTS **]**
    [ADJUSTMTS **]**
    [CHANNEL 1 ADJUSTMNT **]**
    [OFFSET **]**

    Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
  - **Adjust A1 R39 for a Y: reading of 90 dBVrms or less.**
  - **Press the following keys:**

    [Rtn]
    [CHANNEL 2 ADJUSTMNT **]**
    [OFFSET **]**

    Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
  - **Adjust A1 R539 for a Y: reading of 90 dBVrms or less.**

❑ For the optional four channel analyzer, do the following to adjust input dc offset:

- **Set the power switch to on (|).**
- **Press the following keys:**

  [System Utility]
  [MORE **]**
  [SERVICE TESTS **]**
  [ADJUSTMTS **]**
  [CHANNEL 1 ADJUSTMNT **]**
  [OFFSET **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **Adjust A2 R39 in the lower slot for a Y: reading of 90 dBVrms or less.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT **]**
  [OFFSET **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **Adjust A2 R39 in the upper slot for a Y: reading of 90 dBVrms or less.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 3 ADJUSTMNT **]**
  [OFFSET **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **Adjust A2 R539 in the lower slot for a Y: reading of 90 dBVrms or less.**
- **Press the following keys:**

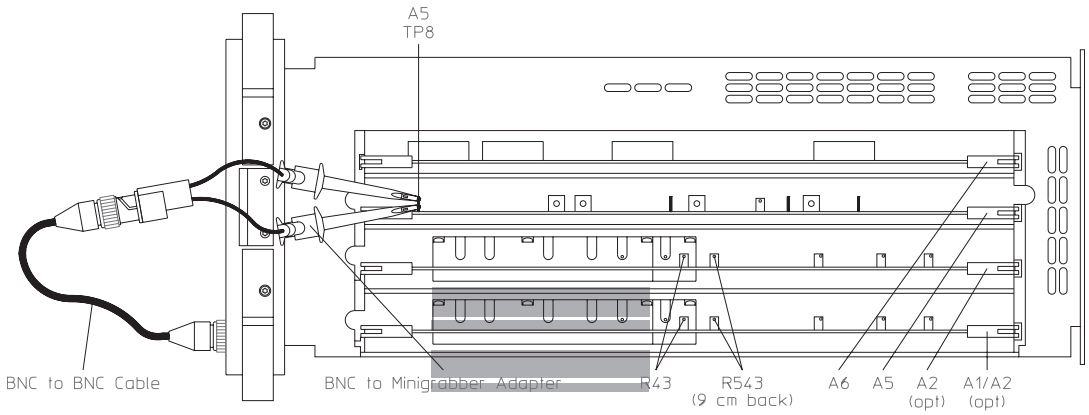
  [Rtn]
  [CHANNEL 4 ADJUSTMNT **]**
  [OFFSET **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **Adjust A2 R539 in the upper slot for a Y: reading of 90 dBVrms or less.**

To adjust common mode rejection

This procedure optimizes the common mode rejection of the A1/A2 Input assemblies. The standard two channel analyzer has one A1 Input assembly. The optional four channel analyzer has two A2 Input assemblies: channel 1 and 3 are routed to the A2 Input assembly in the lower slot and channel 2 and 4 are routed to the A2 Input assembly in the upper slot.

Equipment Required: BNC-to-BNC Cable
BNC(f)-to-Minigrabber Adapter



❑ For the standard two channel analyzer, do the following to adjust common mode rejection:

- **Set the power switch to off (○).**
- **Connect the BNC(f)-to-minigrabber adapter to the BNC cable. Connect both minigrabber clips (signal and ground) to A5 TP8 and the BNC connector to the analyzer's CH 1 connector.**
- **Set the power switch to on (|).**
- **Press the following keys:**

  [System Utility]
  [MORE **]**
  [SERVICE TESTS **]**
  [ADJUSTMTS **]**
  [CHANNEL 1 ADJUSTMNT **]**
  [CMRR **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Y: **value, adjust A1 R43 for a minimum marker value.**
- **Disconnect the BNC cable from the analyzer's CH 1 connector and connect to the CH 2 connector.**
- **Press the the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT **]**
  [CMRR **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Y: **value, adjust A1 R543 for a minimum marker value.**

❑ For the optional four channel analyzer, do the following to adjust common mode rejection:

- **Set the power switch to off (○).**
- **Connect the BNC(f)-to-minigrabber adapter to the BNC cable. Connect both minigrabber clips (signal and ground) to A5 TP8 and the BNC connector to the analyzer's CH 1 connector.**
- **Set the power switch to on (|).**
- **Press the following keys:**

  [System Utility]
  [MORE **]**
  [SERVICE TESTS **]**
  [ADJUSTMTS **]**
  [CHANNEL 1 ADJUSTMNT **]**
  [CMRR **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Y: **value, adjust A2 R43 in the lower slot for a minimum marker value.**
- **Disconnect the BNC cable from the analyzer's CH 1 connector and connect to the CH 2 connector.**
- **Press the the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT **]**
  [CMRR **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Y: **value, adjust A2 R43 in the upper slot for a minimum marker value.**
- **Disconnect the BNC cable from the analyzer's CH 2 connector and connect to the CH 3 connector.**
- **Press the the following keys:**

  [Rtn]
  [CHANNEL 3 ADJUSTMNT **]**
  [CMRR **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.

- **While monitoring the** Y: **value, adjust A2 R543 in the lower slot for a minimum marker value.**
- **Disconnect the BNC cable from the analyzer's CH 3 connector and connect to the CH 4 connector.**
- **Press the the following keys:**

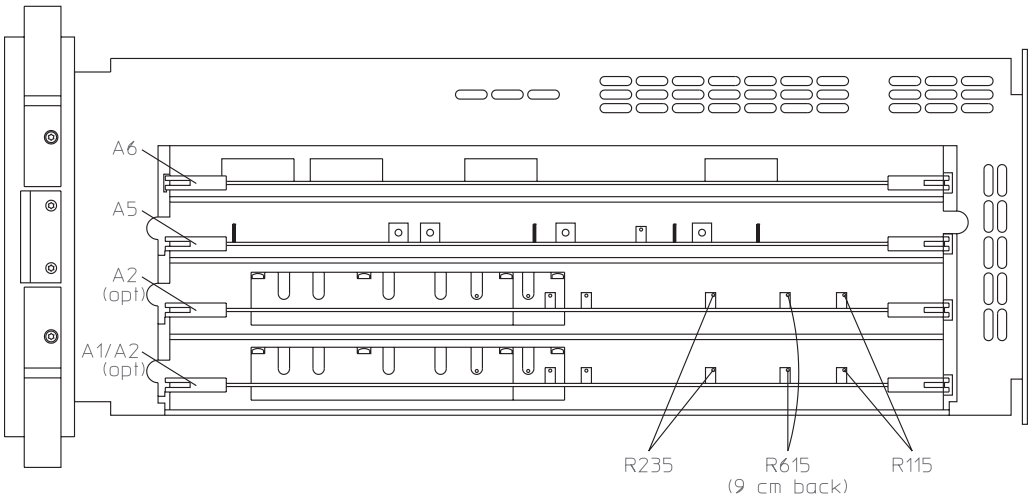
  [Rtn]
  [CHANNEL 4 ADJUSTMNT **]**
  [CMRR **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Y: **value, adjust A2 R543 in the upper slot for a minimum marker value.**
- **Set the power switch to off (O) and disconnect the minigrabber clips from A5 TP8.**

To adjust filter flatness

This procedure adjusts the anti-alias filter on the A1/A2 Input assemblies. The standard two channel analyzer has one A1 Input assembly. The optional four channel analyzer has two A2 Input assemblies: channel 1 and 3 are routed to the A2 Input assembly in the lower slot and channel 2 and 4 are routed to the A2 Input assembly in the upper slot.

Equipment Required: None



❑ For the standard two channel analyzer, do the following to adjust filter flatness:

- **Set the power switch to on (|).**
- **Press the following keys:**

  [System Utility]
  [MORE **]**
  [SERVICE TESTS **]**
  [ADJUSTMTS **]**
  [CHANNEL 1 ADJUSTMNT **]**
  [50 kHz **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A1 R115 for a marker value of 0 0.1 dB.**
- **Press the [** 100 kHz FLATNESS **] softkey.**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A1 R235 for a marker value of 0 0.1 dB.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT **]**
  [50 kHz FLATNESS **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A1 R615 for a marker value of 0 0.1 dB.**

❑ For the optional four channel analyzer, do the following to adjust filter flatness:

- **Set the power switch to on (|).**
- **Press the following keys:**

  [System Utility]
  [MORE **]**
  [SERVICE TESTS **]**
  [ADJUSTMTS **]**
  [CHANNEL 1 ADJUSTMNT **]**
  [25 kHz **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A2 R115 in the lower slot for a marker value of 0 ±0.1 dB.**
- **Press the [** 50 kHz FLATNESS **] softkey.**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A2 R235 in the lower slot for a marker value of 0 ±0.1 dB.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT **]**
  [25 kHz FLATNESS **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A2 R115 in the upper slot for a marker value of 0 ±0.1 dB.**
- **Press the [** 50 kHz FLATNESS **] softkey.**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A2 R235 in the upper slot for a marker value of 0 ±0.1 dB.**

- **Press the following keys:**

  [Rtn]
  [CHANNEL 3 ADJUSTMNT **]**
  [25 kHz FLATNESS **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A2 R615 in the lower slot for a marker value of 0 0.1 dB.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 4 ADJUSTMNT **]**
  [25 kHz FLATNESS **]**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the** Yr: **value, adjust A2 R615 in the upper slot for a marker value of 0 0.1 dB.**

To adjust the display voltage

This procedure adjusts the A102 DC-DC Converter assembly's display voltage to match the voltage required by the A101 Display assembly. This adjustment is only required when the DC-DC Converter assembly or the Display assembly is replaced.

Equipment Required: Multimeter

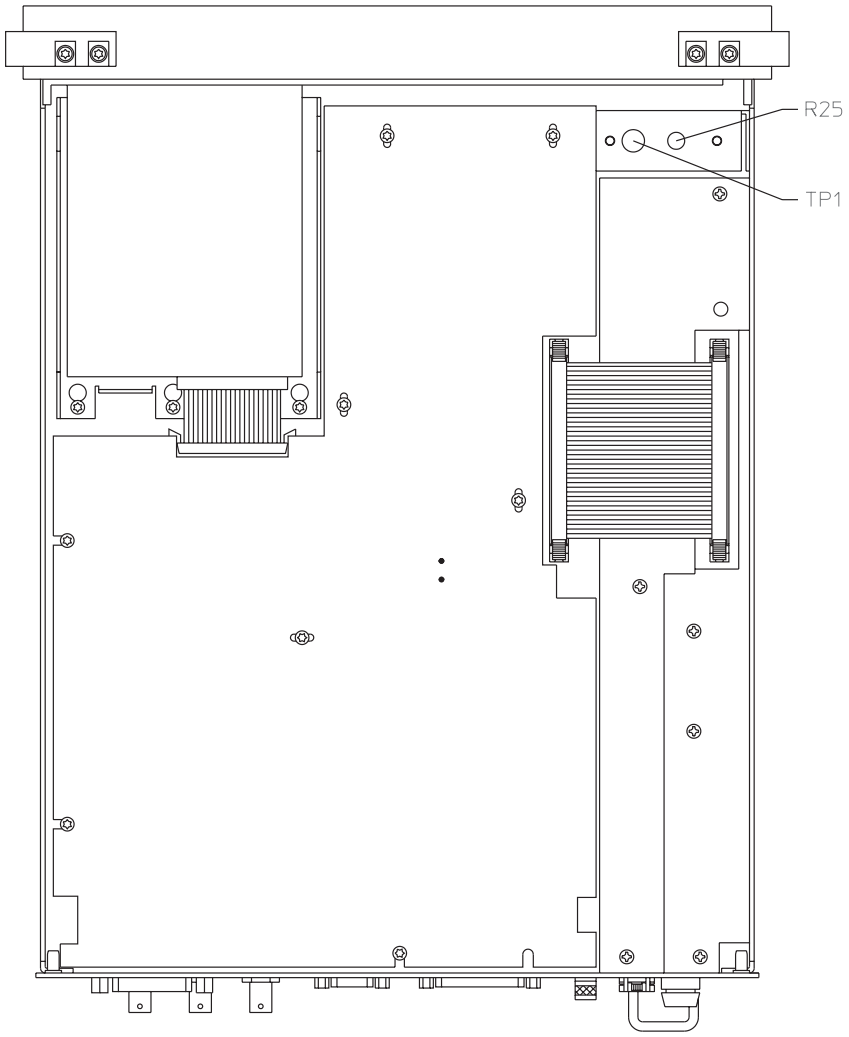
Warning **The display voltage is +210 Vdc 10 Vdc nominal. Use caution when performing this adjustment to avoid personal injury.**

- **Set the power switch to off (O).**
- **Record the V(ALL ON): voltage.**

The V(ALL ON): voltage is printed on a sticker on the component side of the Display assembly. The V(ALL ON): voltage is normally between +200 Vdc and +220 Vdc.

Caution Do not adjust the display voltage above +230 Vdc. The Display assembly can be damaged if the voltage is adjusted above +230 Vdc.

- **Turn A102 R25 clockwise to its stop.**
- **Set the multimeter to a range greater than 220 Vdc and connnect to A102 TP1 using a shielded test clip.**
- **Set the power switch to on (|).**
- **Using a non-metalic flat-edge adjustment tool, adjust A102 R25 for the voltage recorded in step 2.**
- **Set the power switch to off.**


R25
TP1

6

Replacing Assemblies

Replacing Assemblies

This chapter tells you what to do before and after you replace an assembly and shows you how to disassemble the analyzer.

Warning

Disconnect the power cord from the rear panel before disassembly or assembly of the Agilent 35670A.

Even with power removed, there can be sufficient stored energy in some circuits to cause personal injury. These voltages will discharge to a relatively safe level approximately five seconds after the power cord is disconnected.

Caution

Do not connect or disconnect cables from circuit assemblies with the line power turned on (|).

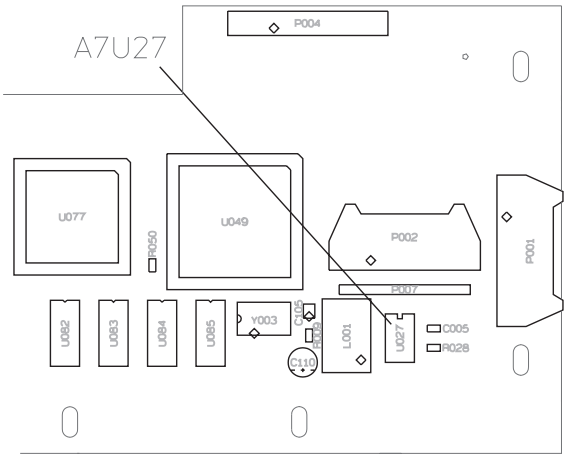
To protect circuits from static discharge, remove or replace assemblies only at static-protected work stations.

What to do before replacing the CPU assembly

The analyzer's serial number and firmware options are stored in EEPROM (U27) on the A7 CPU assembly. Before replacing the CPU assembly, remove A7 U27 from the faulty assembly and insert into the new assembly.

Caution

All firmware options will be lost if A7 U27 is not removed from the faulty assembly and inserted into the new assembly.



What to do after replacing an assembly

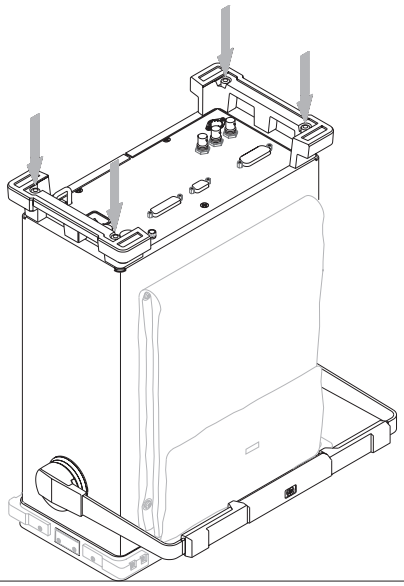
- **Reinstall all assemblies and cables that were removed during troubleshooting.**
- **Do the required adjustments listed in the following table.**
- **Do the self test, page 4-31.**
- **Do the required performance tests listed in the following table.**

Assembly Replaced	Required Adjustment	Required Performance Test
A1 Input	ADC gain, offset and reference, page 5-7 Input dc offset, page 5-10 Common mode rejection, page 5-13 Filter flatness, page 5-17	DC offset Noise Spurious signals Amplitude accuracy Flatness Amplitude linearity A-weight filter Channel match ICP supply
A2 Input	ADC gain, offset and reference, page 5-7 Input dc offset, page 5-10 Common mode rejection, page 5-13 Filter flatness, page 5-17	DC offset Noise Spurious signals Amplitude accuracy Flatness Amplitude linearity A-weight filter Channel match ICP supply
A5 Analog	Source, page 5-6 ADC, page 5-7 Input dc offset, page 5-10	DC offset Noise Spurious signals Amplitude accuracy Flatness Amplitude linearity Channel match Single channel phase accuracy External trigger Source amplitude accuracy Source flatness Source distortion
A6 Digital		Source amplitude accuracy Source dc offset Source flatness

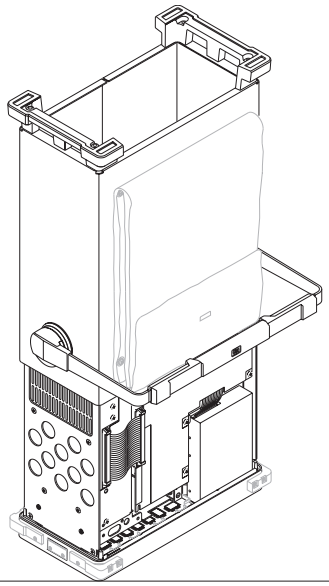
Assembly Replaced	Required Adjustment	Required Performance Test
A7 CPU	Frequency reference, page 5-5	Frequency accuracy
A8 Memory		
A9 NVRAM		
A10 Rear Panel		Tach function (option 1D0 only) External trigger
A11 Keyboard Controller		
A12 BNC		
A13 Primary Keypad		
A14 Secondary Keypad		
A22 BNC		
A90 Fan		
A98 Power Supply		
A99 Motherboard		
A100 Disk Drive		
A101 Display	Display voltage, page 5-21	
A102 DC-DC Converter	Display voltage, page 5-21	

To remove cover

1 Place the analyzer on its front panel. Using a 4 mm hex driver, loosen the four corner screws.



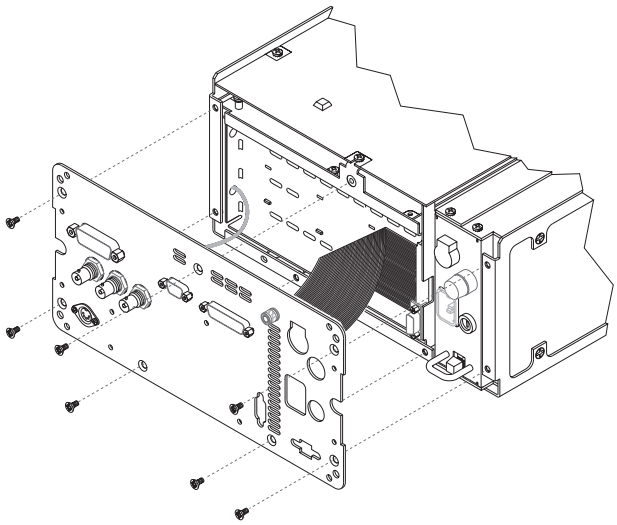
2 Slide the cover straight up.



To remove rear panel

1 Remove cover (see ‘’To remove cover’’).

2 Using a T-15 torx driver, remove the seven screws from the rear panel. Pull the rear panel straight off.

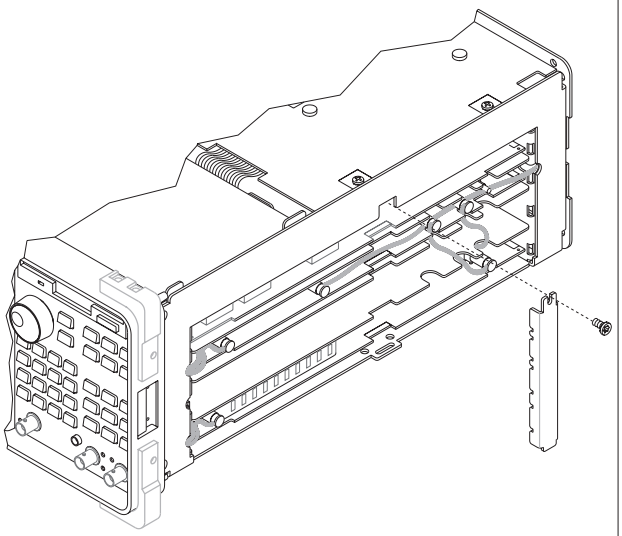


3 Disconnect the ribbon cable and the coaxial cable from the A10 Rear Panel assembly.

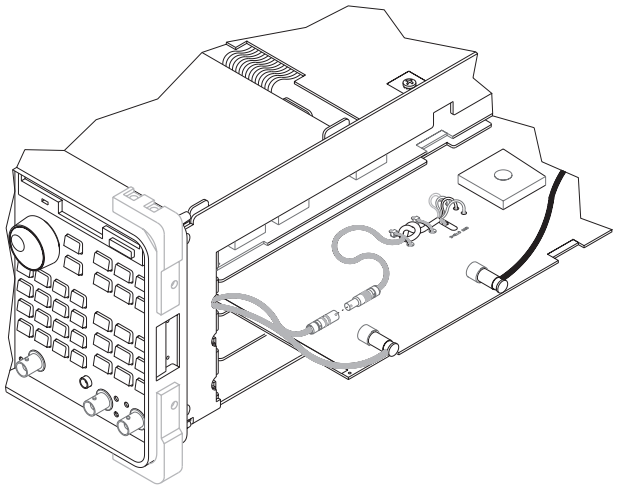
To remove front panel

1 Remove cover (see ''To remove cover'').

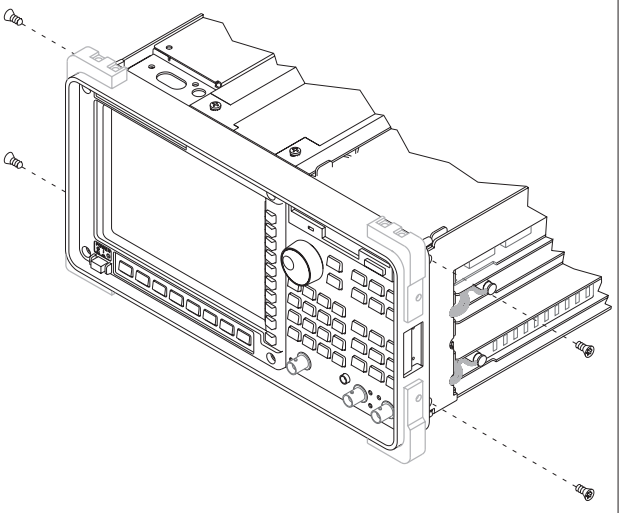
2 Remove assembly retainer bracket.



3 Slide A5 Analog assembly part way out and disconnect gray mic cable.



4 Using a T-15 torx driver, remove the two screws on each side of the front panel.



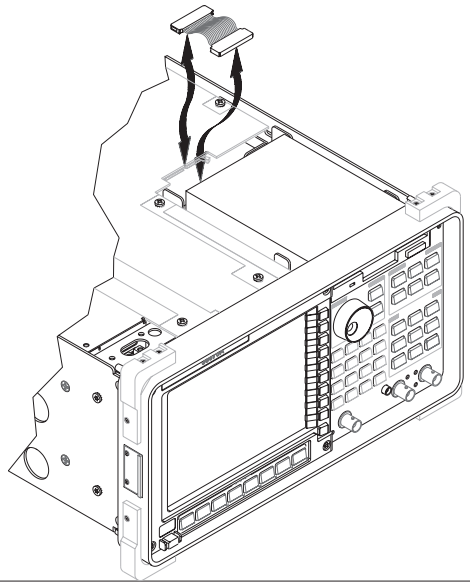
5 Pull the top of the front panel out of the frame.

6 Disconnect the ribbon cables from the front panel. Disconnect the coaxial cables connected to the A12/A22 BNC assembly.

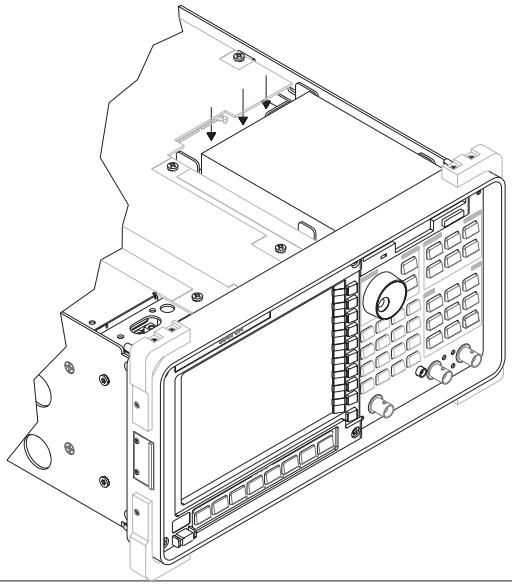
To remove disk drive

1 Remove cover (see ''To remove cover'').

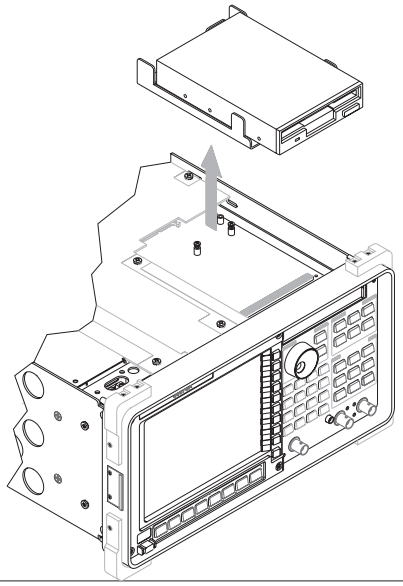
2 Disconnect the disk drive cable.



3 Using a T-10 torx driver, loosen the three screws at the back of the disk drive bracket.



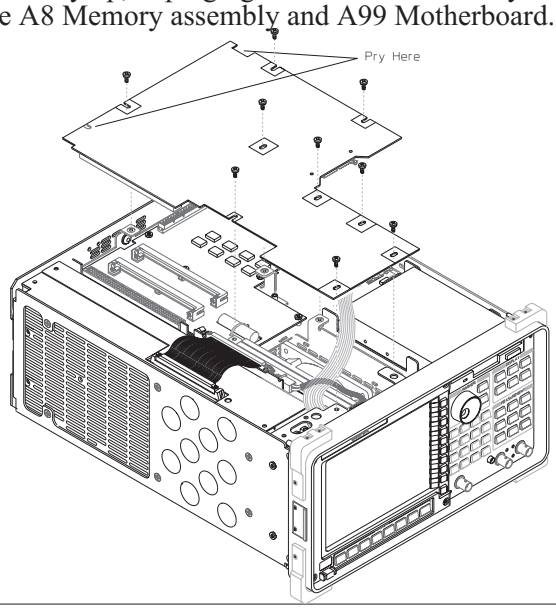
4 Slide the disk drive back and lift up.



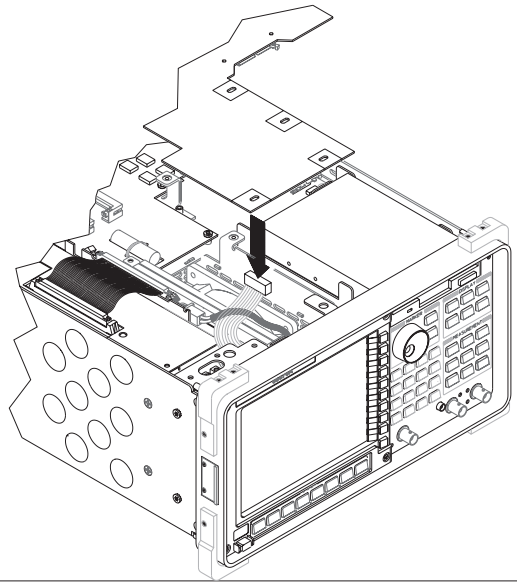
To remove CPU

1 Remove cover (see ''To remove cover'').

2 Using a T-10 torx driver, remove the nine screws from the A7 CPU assembly. Lift the assembly up, unpluging the A7 CPU assembly from the A8 Memory assembly and A99 Motherboard.



3 Disconnect the ribbon cables from the A7 CPU assembly.

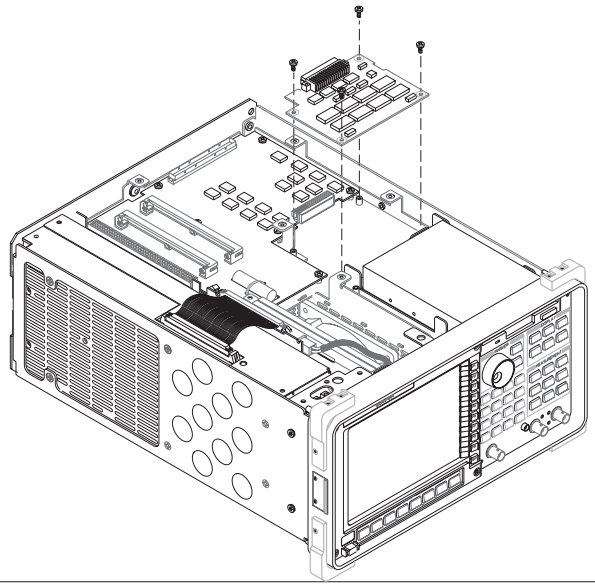


4 The analyzer's serial number and firmware options are stored in EEPROM (U27) on the A7 CPU assembly. Before replacing the CPU assembly, remove A7 U27 from the faulty assembly and insert into the new assembly. See ''What to do before replacing the CPU assembly'' on page 6-3.

To remove NVRAM

1 Remove A7 CPU assembly (see ‘’To remove CPU’’).

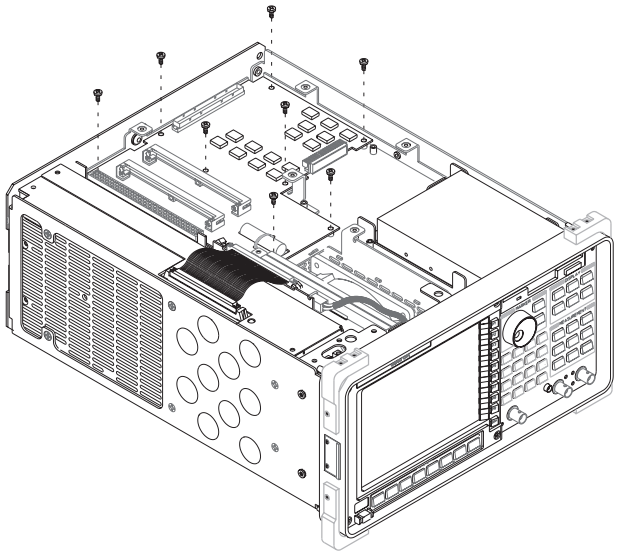
2 Using a T-10 torx driver, remove the four screws from the A9 NVRAM assembly.



To remove memory

1 Remove A7 CPU assembly (see ''To remove CPU''). Remove optional A9 NVRAM assembly (see ''To remove NVRAM'').

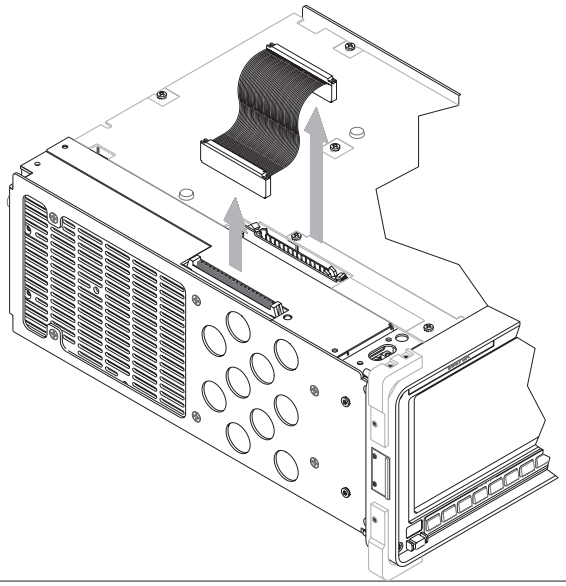
2 Using a T-10 torx driver, remove the eight screws from the A8 Memory assembly.



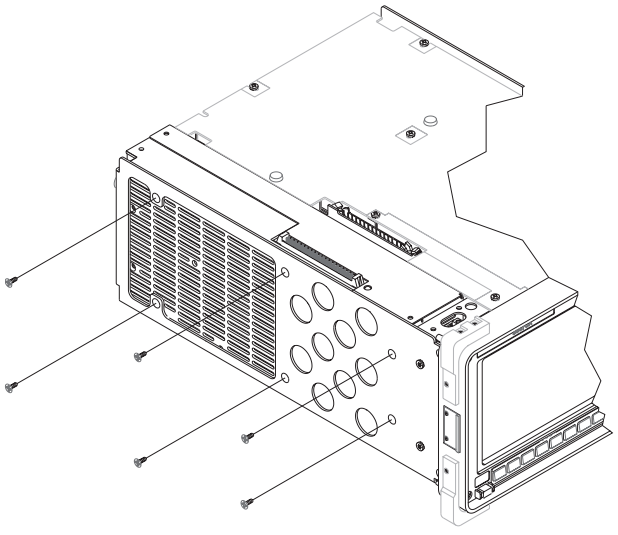
To remove power supply

1 Remove rear panel (see ‘’To remove rear panel’’).

2 Disconnect the ribbon cable from the A98 Power Supply assembly.

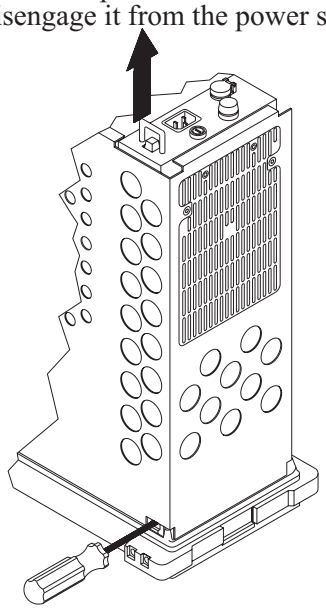


3 Using a T-15 torx driver, remove the six screws from the A98 Power Supply assembly.

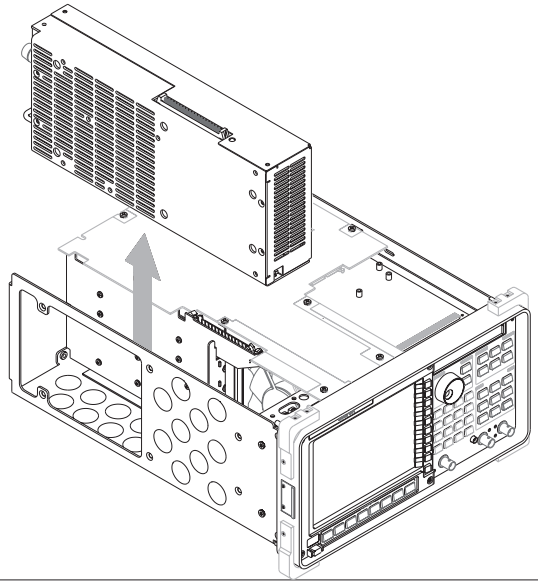


4 Set the front panel power switch in the off (O) position (switch in the out position).

5 Using a straight-edge screw driver, hold the power switch rod in position and lift the A98 Power Supply to disengage it from the power switch rod.



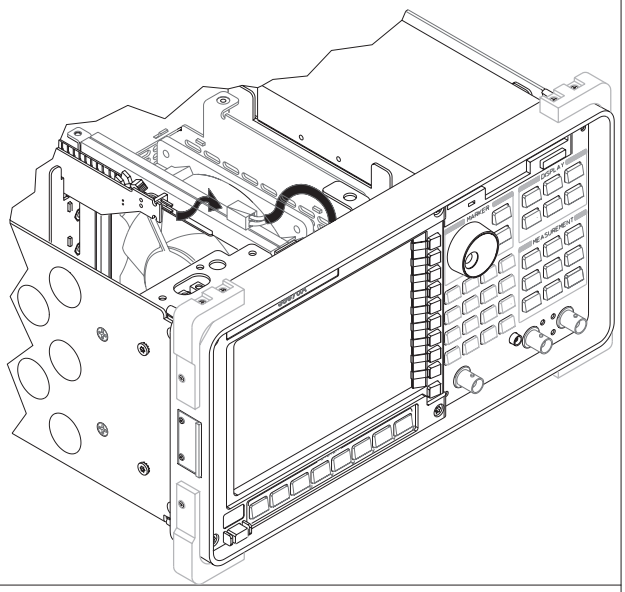
6 Lift the A98 Power Supply assembly straight up.



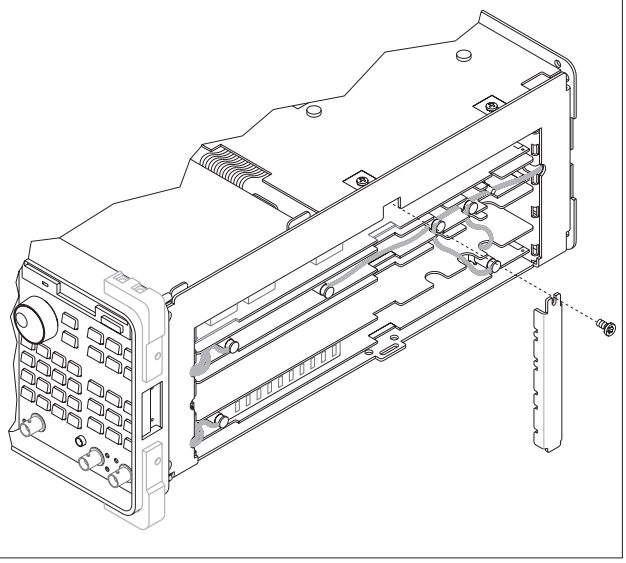
To remove motherboard

1 Remove A98 Power Supply assembly (see ''To remove power supply''). Remove A7 CPU assembly (see ''To remove CPU'').

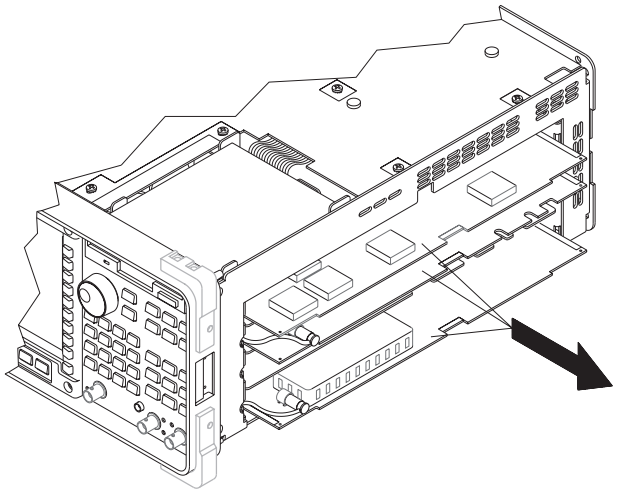
2 Disconnect the fan cable from the A99 Motherboard.



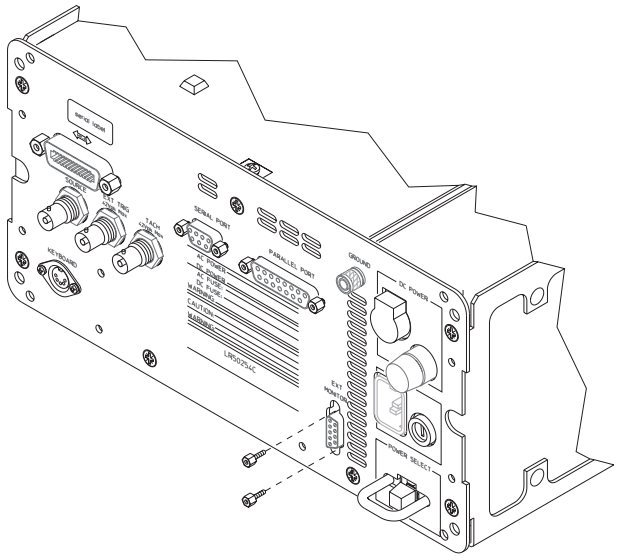
3 Remove assembly retainer bracket.



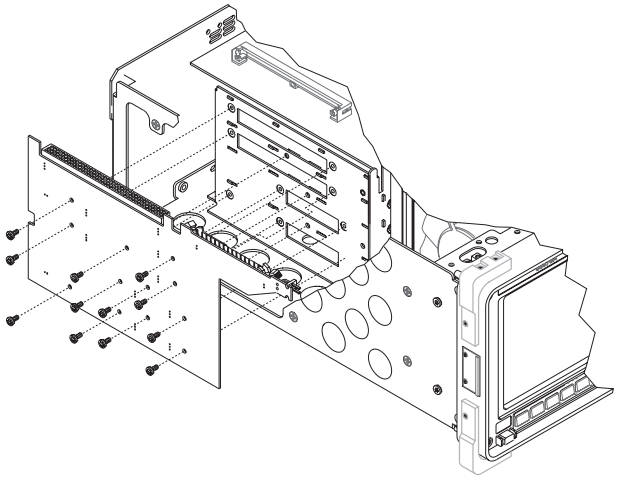
4 Unplug all assemblies from the A99 Motherboard.)



5 Using a 5 mm open-ended wrench, remove the two screws from the EXT MONITOR connector.



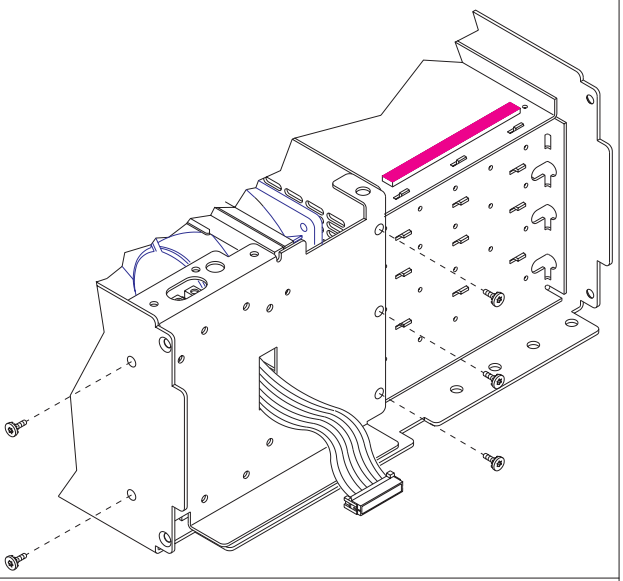
6 Using T-10 torx driver, remove the twelve screws in A99 Motherboard.



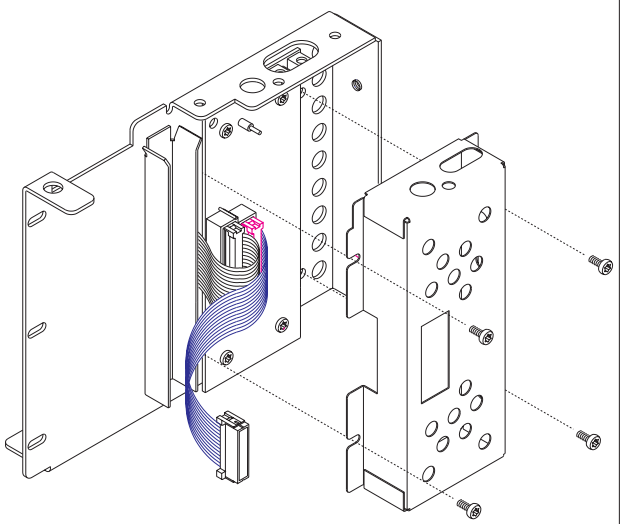
To remove dc-dc converter

1 Remove front panel (see ''To remove front panel''). Remove A7 CPU assembly (see ''To remove CPU'').

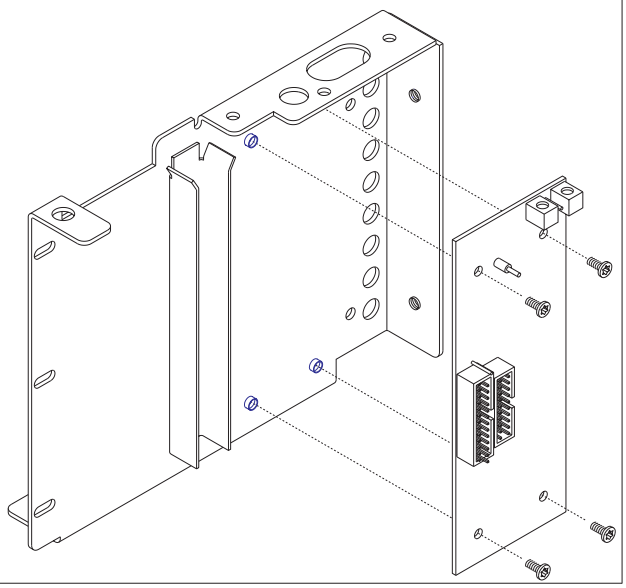
2 Using a T-10 torx driver, remove the five screws from the front wall.



3 Using a T-10 torx driver, remove the four screws from the shield. Unplug ribbon cables.



4 Using a T-10 torx driver, remove the four screws from the A102 DC-DC Converter assembly.



7

Replaceable Parts

Replaceable Parts

This chapter contains information for ordering replacement parts for the Agilent 35670A Dynamic Signal Analyzer.

Ordering Information

Replacement parts are listed in the following ten tables:

- Assemblies
- Cables
- Instrument Covers and Handles
- Assembly Covers and Brackets
- Front Panel Parts
- Rear Panel Parts
- Chassis Parts
- Card Nest Parts
- Screws, Washers, and Nuts
- Miscellaneous Parts

To order a part listed in one of the tables, quote the Agilent Technologies part number (HP Part Number), the check digit (CD), indicate the quantity required, and address the order to the nearest Agilent Technologies sales and service office (see the inside back cover of this guide). The check digit verifies that an order has been transmitted correctly, ensuring accurate and timely processing of the order. The first time a part is listed in the table, the quantity column (Qty) lists the total quantity of the part used in the analyzer. For definitions of the abbreviations and the corresponding name and address of the manufacturers' codes shown in the tables, see ''Code Numbers.''

Caution

Many of the parts listed in this chapter are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unnecessary damage.

Non-Listed Parts

To order a part that is NOT listed in the replaceable parts tables, indicate the instrument model number, instrument serial number, description and function of the part, and the quantity of the part required. Address the order to the nearest Agilent Technologies sales and service office (see the inside back cover of this guide).

Direct Mail Order System

Within the U.S.A., Agilent Technologies can supply parts through a direct mail order system. Advantages of the Direct Mail Order System are:

- Direct ordering and shipment from the Agilent Parts Center.
- No maximum or minimum on any mail order. There is a minimum order for parts ordered through a local Agilent sales and service office when the orders require billing and invoicing.
- Transportation charges are prepaid. A small handling charge is added to each order.
- No invoicing. A check or money order must accompany each order.
- Mail order forms and specific ordering information are available through your local Agilent Technologies sales and service office. See the inside back cover of this guide for a list of Agilent Technologies sales and service office locations and addresses.

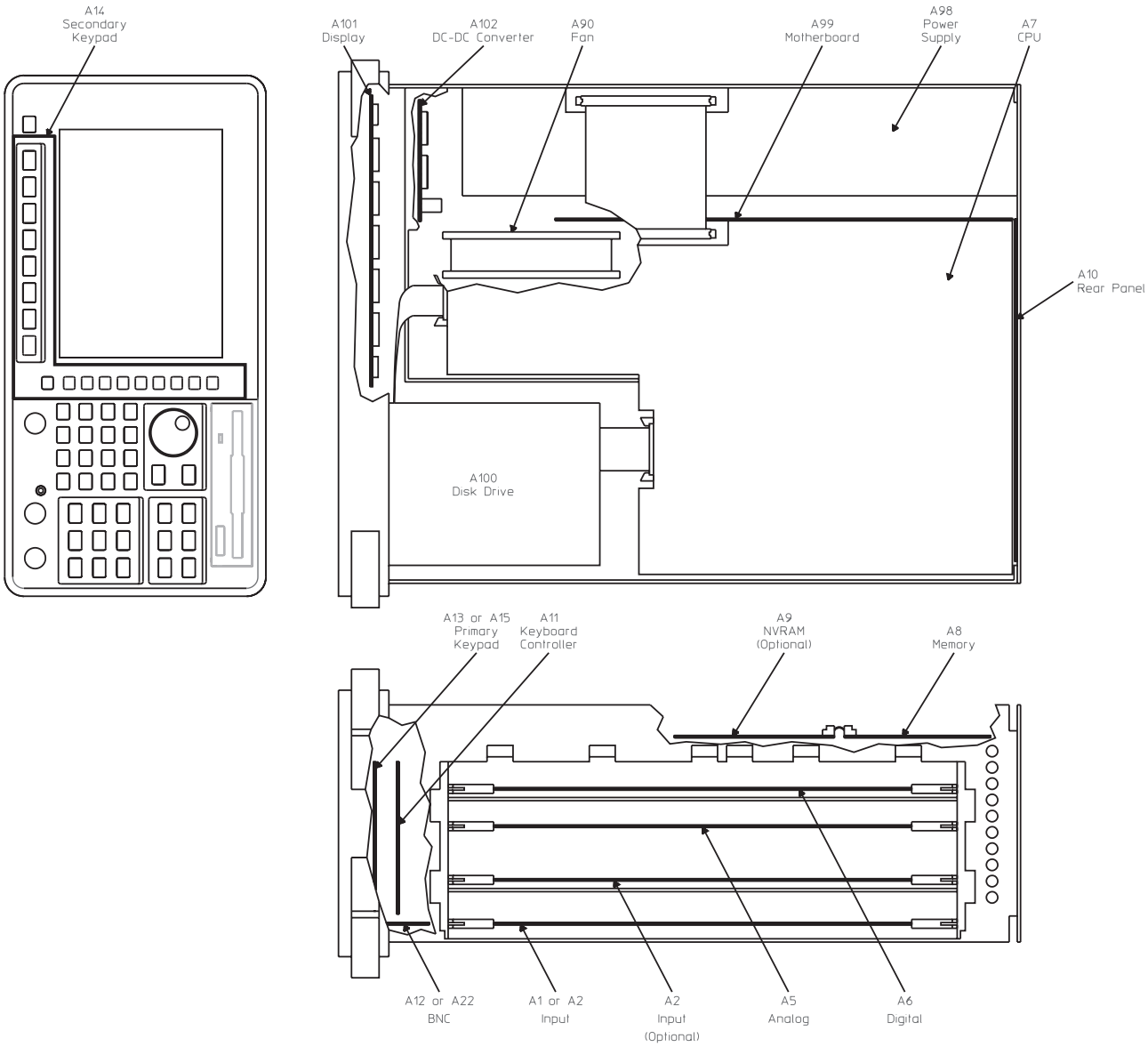
Code Numbers

The following table provides the name and address for the manufacturers' code numbers (Mfr Code) listed in the replaceable parts tables.

Mfr No.	Mfr Name	Address
00268	LEMO USA, Inc.	Santa Rosa, CA 95406 U.S.A.
00779	Amp Inc.	Harrisburg, PA 17105 U.S.A.
00955	Koszegi Industries Inc.	South Bend, IN 46624 U.S.A.
05791	Lyn-Tron Inc	Burbank, CA 91505 U.S.A.
09353	C & K Components Inc	Newton, MA 02158 U.S.A.
10421	Epson America Inc.	Dallas, TX 75284 U.S.A.
11919	Computer Products Inc.	Chicago, IL 60693 U.S.A.
12690	Fuji Polymer Industries Co. Inc.	Nagoya-Shi Japan
24931	Specialty Connector Co	Franklin, IN 46131 U.S.A.
28480	Agilent Technologies Company	Palo Alto, CA 94304 U.S.A.
30817	Instrument Specialties Co. Inc.	Placentia, CA 92670 U.S.A.
34785	Dek Inc.	St Charles, IL 60174 U.S.A.
56501	Thomas & Betts Corp	Bridgewater, NJ 08807 U.S.A
57003	Chomerics Shielding Technology	Carson, CA 90745 U.S.A.
71400	Cooper Industries Inc	St Louis, MO 63178 U.S.A.
73734	Federal Screw Products Co.	Chicago, IL 60618 U.S.A.
75915	Littelfuse Inc.	Des Plaines, IL 60016 U.S.A.
76381	3M Co.	Seattle, WA 98124 U.S.A.

Assemblies

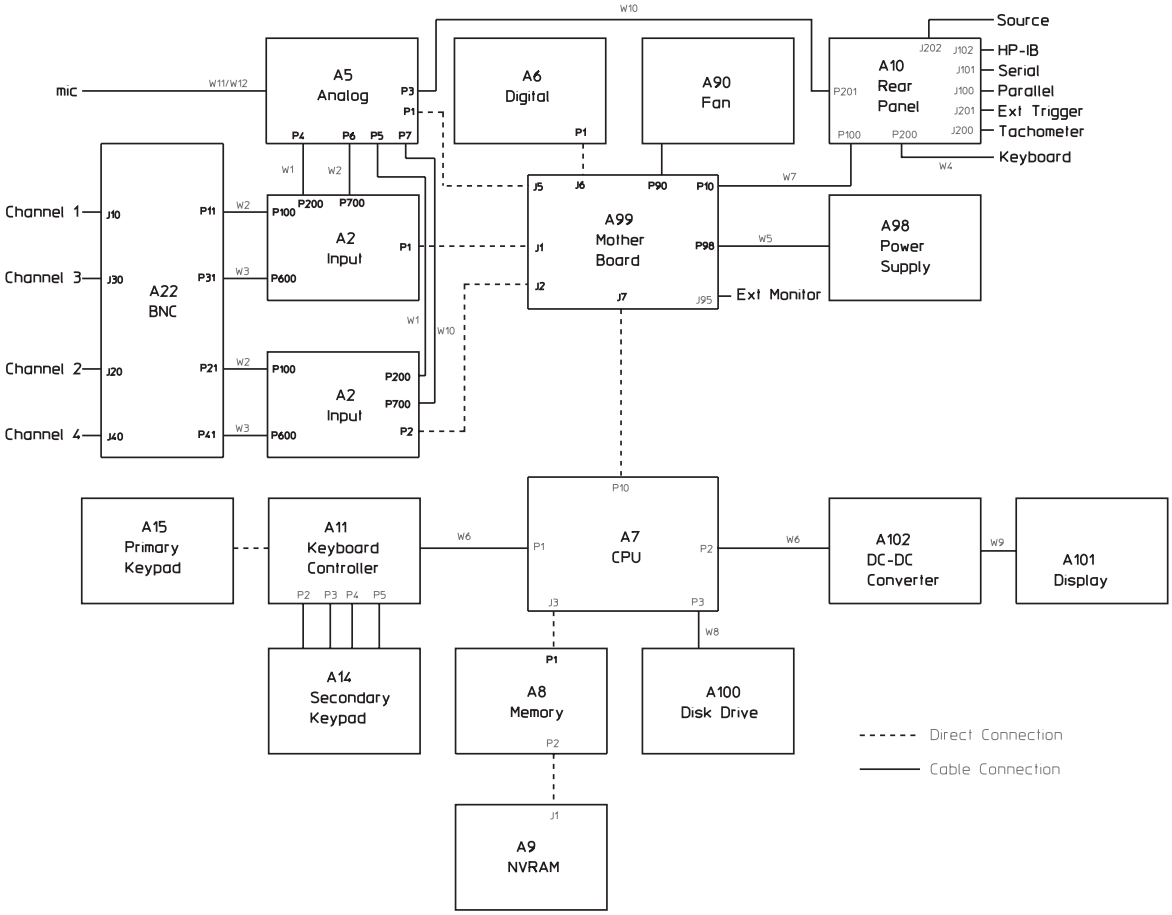
After replacing an assembly, see ‘’What to do after replacing an assembly’’ in chapter 6 for required adjustments and performance tests.
The reference designator for the screws that fasten the A90 Fan assembly is MP600. The reference designator for the screws that fasten the A98 Power Supply assembly is MP603. The reference designator for the screws that fasten all other assemblies is MP601.



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1	35670-69501	9	1	INPUT ASSEMBLY - 2 CHANNEL	28480	35670-69501
A2	35670-69502	0	2	INPUT ASSEMBLY - 4 CHANNEL	28480	35670-69502
A5	35670-69505	3	1	ANALOG ASSEMBLY	28480	35670-69505
A6	35670-69506	4	1	DIGITAL ASSEMBLY	28480	35670-69506
A7	35670-69507	5	1	CPU ASSEMBLY †	28480	35670-69507
A8	35670-66508	6	1	MEMORY ASSEMBLY	28480	35670-66508
A9	35670-66509	7	1	NVRAM ASSEMBLY	28480	35670-66509
A10	35670-66510	4	1	REAR PANEL ASSEMBLY	28480	35670-66510
A11	35670-66511	5	1	KEYBOARD CONTROLLER	28480	35670-66511
A12	35670-66512	6	1	BNC ASSEMBLY- 2 CHANNEL	28480	35670-66512
A13	35670-66513	7	1	PRIMARY KEYPAD ASSEMBLY - 2 CHANNEL	28480	35670-66513
A14	35670-64300	6	1	SECONDARY KEYPAD ASSEMBLY	28480	35670-64300
A15	35670-66515	9	1	PRIMARY KEYPAD ASSEMBLY - 4 CHANNEL	28480	35670-66515
A22	35670-66522	8	1	BNC ASSEMBLY - 4 CHANNEL	28480	35670-66522
A90	03585-68501	6	1	FAN ASSEMBLY	28480	03585-68501
A98	0950-2357	9	1	POWER SUPPLY ASSEMBLY	11919	NFS177-7630
A99	35670-66599	9	1	MOTHERBOARD	28480	35670-66599
A100	0950-2141	9	1	DISK DRIVE ASSEMBLY	10421	SMD-340
A101	2090-0340	9	1	DISPLAY ASSEMBLY	28480	2090-0340
A102	0950-2335	3	1	DC-DC CONVERTER ASSEMBLY	28480	0950-2335

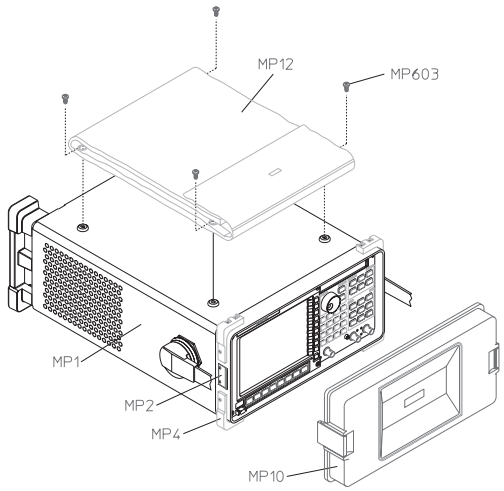
† The analyzer's serial number and firmware options are stored in EEPROM (U27) on the A7 CPU assembly. Before replacing the CPU assembly, remove A7 U27 from the faulty assembly and insert into the new assembly. See ''What to do before replacing the CPU assembly'' on page 6-3.

Cables



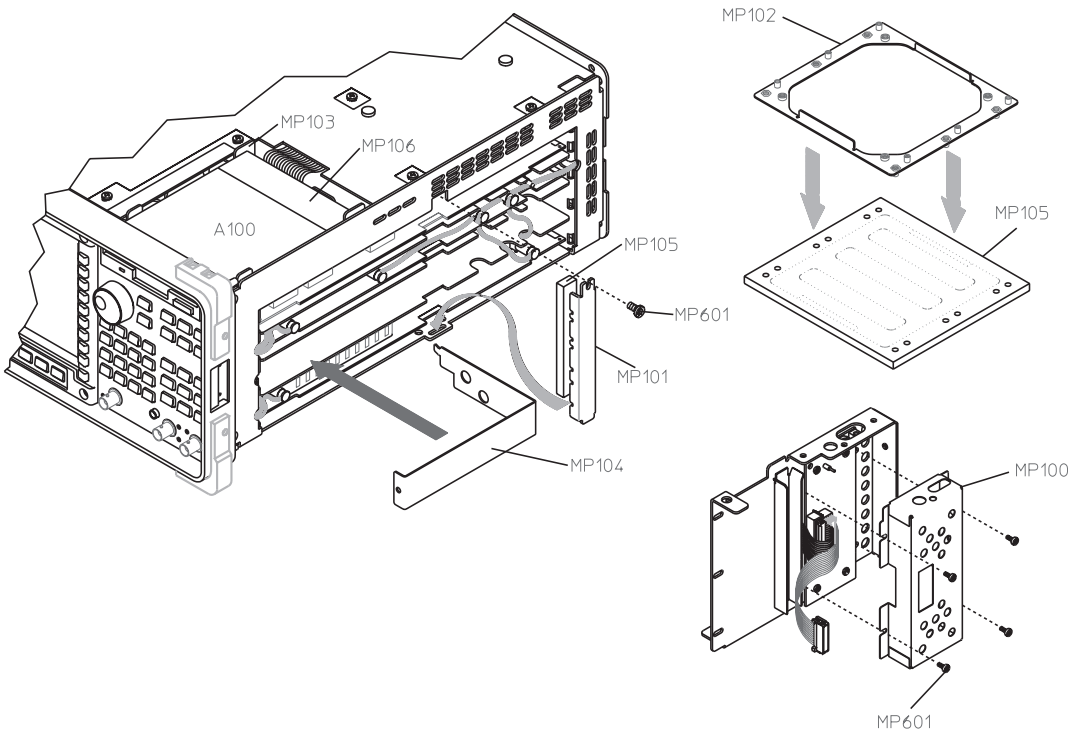
Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
W1	03585-61603	5	2	CBL-ASM CXL FSMB/FSMB 100MM OR	28480	03585-61603
W2	03585-61604	6	3	CBL-ASM CXL FSMB/FSMB 177MM YL	28480	03585-61604
W3	03586-61678	5	2	CBL-ASM CXL FSMB/FSMB 205MM GY	28480	03586-61678
W4	35665-61601	7	1	CBL-ASM CDIN/FHSG 80MM MULT	28480	35665-61601
W5	8120-6243	9	1	CBL-POWER 60POS RIBBON 75MM LG	28480	8120-6243
W6	8120-6236	0	2	CBL-KEYBOARD 16POS RIBBON	28480	8120-6236
W7	8120-6242	8	1	CBL - REAR PANEL 60POS RIBBON	28480	8120-6242
W8	8120-6241	7	1	CBL-DISC DRIVE 34POS RIBBON	28480	8120-6241
W9	8120-6240	6	1	CBL-DISPLAY 20POS RIBBON	28480	8120-6240
W10	03586-61677	4	2	CBL-ASM CXL FSMB/FSMB 265MM BL	28480	03586-61677
W11	35670-61620	7	1	CBL-FRT PNL ADAPTER 4-CON LEMO	28480	35670-61620
W12	35670-61621	8	1	CBL-ADAPTER PLUG 4-COND W/LEMO	28480	35670-61621

Instrument Covers and Handles



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP1	35670-64101	5	1	SHTF ASSY-COVER ALV	28480	35670-64101
MP2	5021-5483	4	2	COVER LATCHES	28480	5021-5483
MP4	5062-4806	9	1	MOLD BUMPER SET 4PC FF CORNRS	28480	5062-4806
MP10	35670-64102	6	1	IMPACT COVER - 35670A	28480	35670-64102
MP12	1540-0292	9	1	PKG-CASE ACCESSORY	00955	1051-B-2
MP13	1530-0272	4	1	VIEWING HOOD	28480	1530-0272
MP15	8160-0689	9	2	STMP RFI GASKET.228LNG BECUZN	30817	0097-954-15

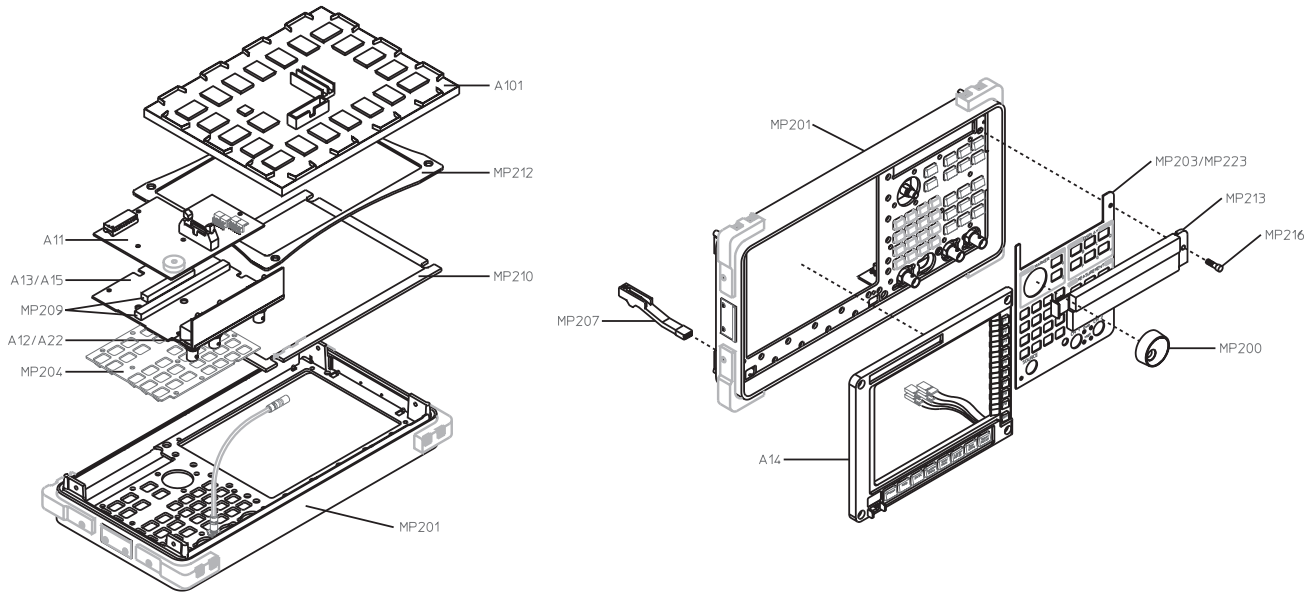
Assembly Covers and Brackets



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP100	35670-00605	0	1	SHTF SHIELD DISP PWR SUPPLY	28480	35670-00605
MP101	35670-01203	6	1	SHTF BRKT,PCB RETAINER	28480	35670-01203
MP102	35670-01204	7	1	SHTF BRACKET-FAN AL	28480	35670-01204
MP103	35670-01205	8	1	SHTF DISC BRKT	28480	35670-01205
MP104	35670-04102	0	1	SHTF SLOT PLUG	28480	35670-04102
MP105	35670-44701	9	2	GSKT FAN MOUNT W/SLUGS	28480	35670-44701
MP106	4040-2321	2	1	DUST COVER DISC DRIVE	28480	4040-2321

Front Panel Parts

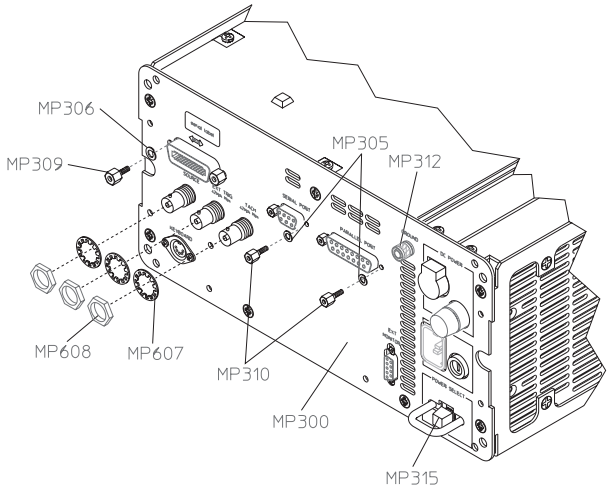
The reference designator for the screws that fasten the bezel (MP208) to the front frame (MP201) is MP604. The reference designator for the nuts that fasten the A101 Display assembly to the front frame is MP611. The reference designator for the screws that fasten the front frame to the chassis is MP603.



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP200	0370-3069	2	1	MOLD KNB-1.12DRD RPG .25ID	28480	0370-3069
MP201	35670-22001	6	1	CSTG-FRT FRAME MACH&PAINTED	28480	35670-22001
MP203	35670-34305	8	1	PNL-OVRLY-DRESS 2CHAN PLCR	28480	35670-34305
MP204	35670-41901	5	1	KYPD HARDKEY HINGED	28480	35670-41901
MP207	35670-43701	7	1	MOLD-PUSHROD PWR WHT	28480	35670-43701
MP209	1252-4960	5	2	CONNECTOR-MULTICONTACT	12690	05-10108
MP210	35670-29301	3	1	LNZ-FLTR RFI/OPTICAL	28480	35670-29301
MP212	35670-44703	1	1	DISPLAY GASKET	28480	35670-44703
MP213	35670-44101	3	1	MOLD-COVER DISC DRIVE PCMT SLS	28480	35670-44101
MP214	8160-0423	9	3	RFI ROUND STRIP MNL/SIL-RBR .125-IN-OD	57003	01-0501-1891
MP215	8160-0467	1	1	RFI STRIP-FINGERS BE-CU BRIGHT DIP	30817	97-555-A-X
MP216	0515-0482	5	1	SCREW-SKT-HD-CAP M3 X 0.5 8MM-LG	28480	0515-0482
MP223	35670-34302	5	1	PNL-OVRLY-DRESS 4CHAN PLCR	28480	35670-34302

Rear Panel Parts

The reference designator for the screws that fasten the KEYBOARD connector and A10 Rear Panel assembly to the rear panel is MP601. The reference designator for the screws that fasten the rear panel to the chassis is MP603.

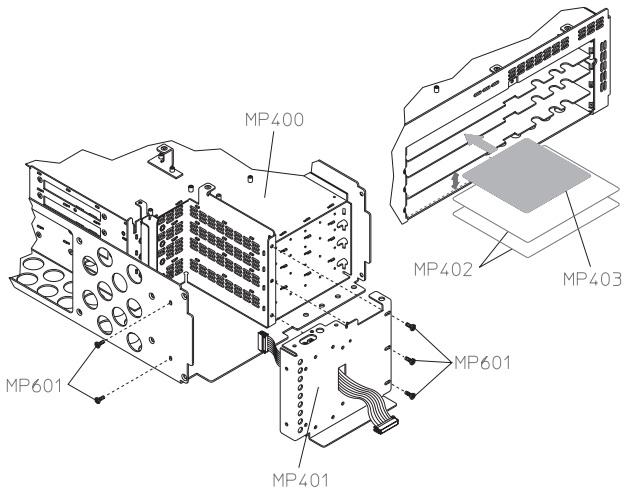


Caution

The POWER SELECT switch must be in the DC position (out position) when the key cap (MP315) is removed. If the switch is not in the DC position when the key cap is removed, the switch may be damaged.

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP300	35670-00201	2	1	SHTF REAR PANEL W/SILKSCREEN	28480	35670-00201
MP305	2190-0913	9	6	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0913
MP306	2190-0586	2	2	WASHER-LK HLCL 4.0 MM 4.1-MM-ID	28480	2190-0586
MP309	0380-0643	3	2	STANDOFF-HEX .255-IN-LG 6-32-THD	28480	0380-0643
MP310	0380-1832	4	4	STDF-HXMF MIXED 4.8MMLG STLZN	00779	747404-3
MP312	1510-0038	8	1	BINDING POST ASSY SGL THD-STUD	28480	1510-0038
MP314	2950-0072	3	1	NUT-HEX-DBL-CHAM 1/4-32-THD .062-IN-THK	28480	2950-0072
MP315	5041-0564	4	1	KEYCAP	28480	5041-0564

Chassis Parts



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP400	35670-00101	1	1	SHTF-CHASSIS ASSY	28480	35670-00101
MP401	35670-00102	2	1	SHTF WALL ASSY FRONT	28480	35670-00102
MP402	35670-04103	1	2	INPUT BD INSULATOR	28480	35670-04103
MP403	35650-00601	2	1	SHTF CVR-SHLD MUFL	28480	35650-00601
MP404	35670-64302	8	1	LBL CABLE 2CH CBL ROUTINE	28480	35670-64302
MP405	35670-64304	0	2	LBL CABLE 4CH CBL ROUTINE	28480	35670-64304

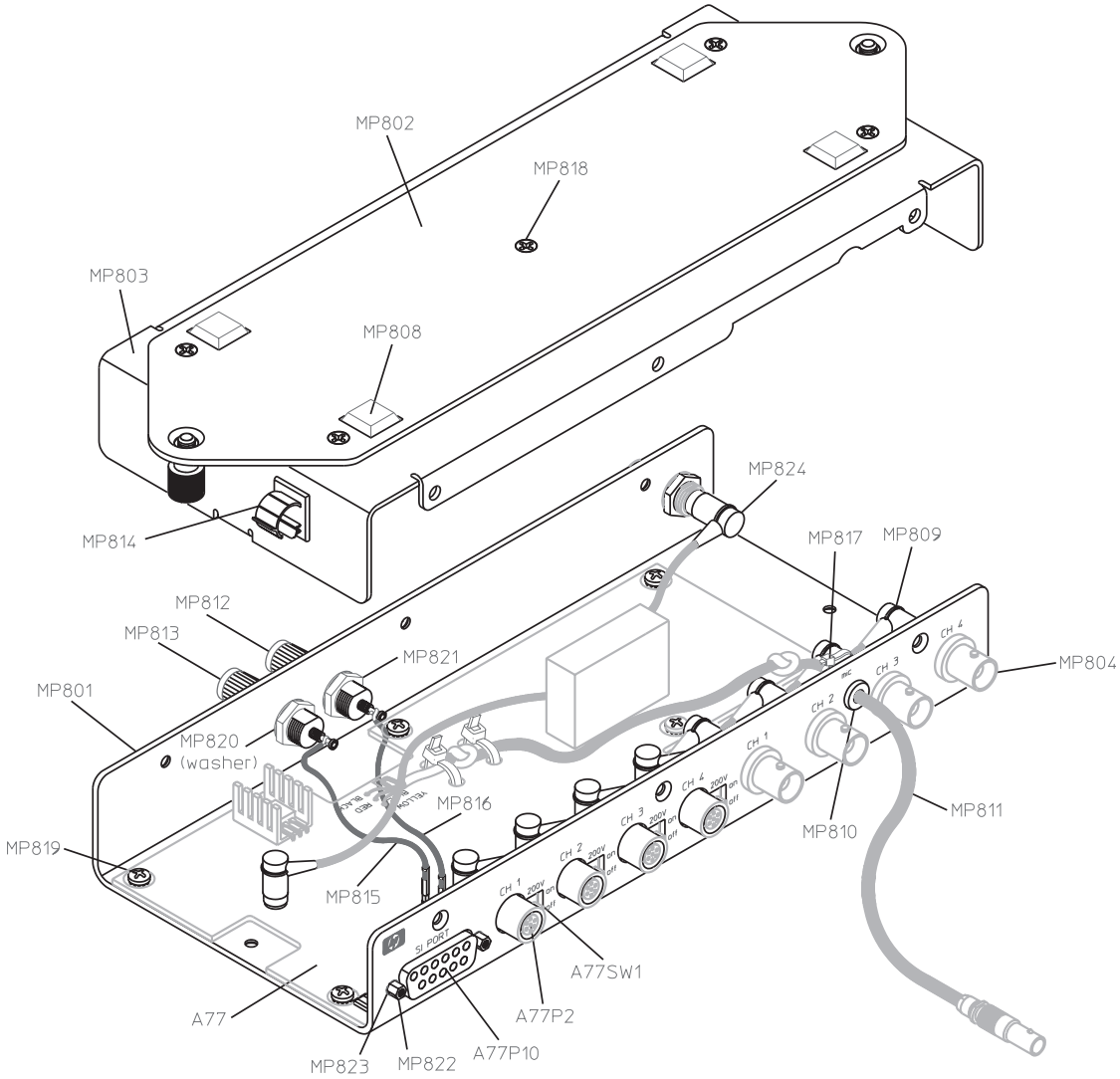
Screws, Washers, and Nuts

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP600	0515-0374	4	16	SCREW-MACHINE ASSEMPLY M3 X 0.5 10MM-LG	28480	0515-0374
MP601	0515-0430	3	66	SCREW-MACHINE ASSEMPLY M3 X 0.5 6MM-LG	28480	0515-0430
MP602	0515-1940	2	4	SCR-MCH M2.5 6MMLG PHTX SST *	28480	0515-1940
MP603	0515-2043	8	21	SCR-MCH M4.0 8MMLG FHTX SST *	28480	0515-2043
MP604	0515-1622	7	4	SCR-CAP M4.0 8MMLG SKHX SSTBL	28480	0515-1622
MP607	2190-0099	2	3	WASHER-LK INTL T 7/16 IN .472-IN-ID	28480	2190-0099
MP608	2950-0035	8	3	NUT-HEX-DBL-CHAM 15/32-32-THD	28480	2950-0035
MP611	0535-0031	2	4	NUT-HEX W/LKWR M3 X 0.5 2.4MM-THK	28480	0535-0031
MP613	2190-0060	7	1	WASHER-LK INTL T 1/4 IN .256-IN-ID	28480	2190-0060
MP619	1252-0699	9	2	SCR-JCK 4-40 .25LG THRD STLZN	05791	ST-9411-36

Miscellaneous Parts

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP702	1400-1122	0	1	CLAMP-CABLE .187-DIA .735-WD NYL	34785	021-0188
MP703	1400-1229	8	1	CLAMP-CABLE .375-DIA 1-WD NYL	34785	021-0375
MP704	0403-0285	9	4	BUMPER FOOT-ADH MTG 12.7-MM-WD	76381	SJ-5018 GRAY
MP705	1400-0249	0	1	CABLE TIE .062-.625-DIA .091-WD NYL	56501	TY-23M-8
MP707	0403-0179	0	18	BUMPER FOOT-ADH MTG	76381	SJ-5012 BLACK
A8B200	1420-0336	8	1	BATTERY	55002	T06/46
A10F200	2110-0665	0	1	FUSE-1A 125V NTD .28X.096	75915	R251001T1
A98 F1	2110-0342	0	1	FUSE 8A 250V NTD 1.25X.25 UL	71400	ABC-8
A98 F2	2110-0920	0	1	FUSE 30A 32VDC NORMAL BLOW 3AG	75915	311-030

Option UK4 Parts



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A77	35670-66577	3	1	MICROPHONE PC ASSEMBLY	28480	35670-66577
A77P2	1252-5280	4	4	CONN-LEMO 7-CNT FEMALE RT - PC	00268	EPG.1B.307.HLN
A77P10	1252-1481	9	1	CON-RECT D-SUB 15CKT 15PN THL	00779	748876-1
A77SW1	3101-3124	4	4	SW -SL .02A 20VA1D	09353	1101-M2S4AV2BE
MP801	35670-00121	5	1	SHTF-BTTM OUTBOX W/SILKSCREEN	28480	35670-00121
MP802	35670-01206	9	1	SHTF BRKT MNTG OUTBOX	28480	35670-01206
MP803	35670-00120	4	1	SHTF LID OUTBOX PAINTED	28480	35670-00120
MP804	1250-1558	7	5	ADAPTER-COAX STR F-BNC F-RCA-PHONO	24931	29JJ126-3
M0808	0403-0285	9	4	BUMPER FOOT-ADH MTG 12.7-MM-WD	76381	SJ-5018 GRAY
MP809	8120-4891	9	4	CBL-RCA 153MM BK	28480	8120-4891
MP810	0400-0009	9	1	GROMMET-RND .125-IN-ID .25-IN-GRV-OD	28480	0400-0009
MP811	35670-61621	8	1	CBL-ADAPTER PLUG 4-COND W/LEMO	28480	35670-61621
MP812	1510-0091	3	1	BINDING POST SGL SGL-TUR JGK RED	28480	1510-0091
MP813	1510-0107	2	1	BINDING POST SGL SGL-TUR JGK CBK	28480	1510-0107
MP814	1400-1122	0	1	CLAMP-CABLE .187-DIA .735-WD NYL	34785	021-0188
MP815	8120-3828	0	1	LJPR 22GA BLK 100MM Dx8	28480	8120-3828
MP816	8120-3860	0	1	LJPR 22GA RED 100MM Dx8	28480	8120-3860
MP817	1400-0249	0	3	CABLE TIE .062-.625-DIA .091-WD NYL	56501	TY-23M-8
MP818	0515-1946	8	13	SCR-MCH M3.0 6MMLG FHTX SST	28480	0515-1946
MP819	0515-0430	3	7	SCR-MCH ASSEMPLY M3 X 0.5 6MM-LG	28480	0515-0430
MP820	2190-0016	3	2	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
MP821	2950-0001	8	2	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	73734	9002-NP
MP822	1252-0699	9	2	SCR-JCK 4-40 .25LG THRD STLZN	05791	ST-9411-36
MP823	2190-0583	9	2	WASHER-LK HLCL 2.5 MM 2.6-MM-ID	28480	2190-0583
MP824	8120-2587	6	1	CABLE ASSY-COAX 50-OHM 1.5KV 8.5-IN-LG	28480	8120-2587
	35670-90014	4	1	MICROPHONE & POWER OP NOTE	28480	35670-90051
	8120-1839	9	1	CABLE ASSY-COAX 50-OHM 24-IN-LG JGK	28480	8120-1839
	8120-6237	1	4	CBL-ASM CXL BNC	28480	8120-6237

8

Circuit Descriptions

Circuit Descriptions

This chapter contains the overall instrument description and individual assembly descriptions for the Agilent 35670A Dynamic Signal Analyzer. The overall instrument description lists the assemblies in the analyzer and describes the analyzer's overall block diagrams. The assembly descriptions give additional information for each assembly. For signal connections and descriptions, see chapter 9, ''Voltages and Signals.''

Overall Instrument Description

The Agilent 35670A Dynamic Signal Analyzer is an FFT spectrum/network analyzer with a frequency range that extends from 0.19531 Hz to 102.4 kHz in single channel mode and from 0.097656 Hz to 51.2 kHz in two channel mode. The optional four channel analyzer has a frequency range that extends from 0.097656 Hz to 51.2 kHz in two channel mode and from 0.048828 Hz to 25.6 kHz in four channel mode. The analyzer has a built-in signal source providing random noise, burst random noise, periodic chirp, burst chirp, pink noise, and fixed sine. Measurements can be saved to an internal 3.5-inch flexible disk drive, an external HP SS-80 disk drive, or to internal non-volatile memory. Plots and prints of the measurements can be made directly to printers and plotters with GPIB, parallel, or serial interfaces. The analyzer also supports the Instrument Basic programming language (IBASIC).

Overall Block Diagram

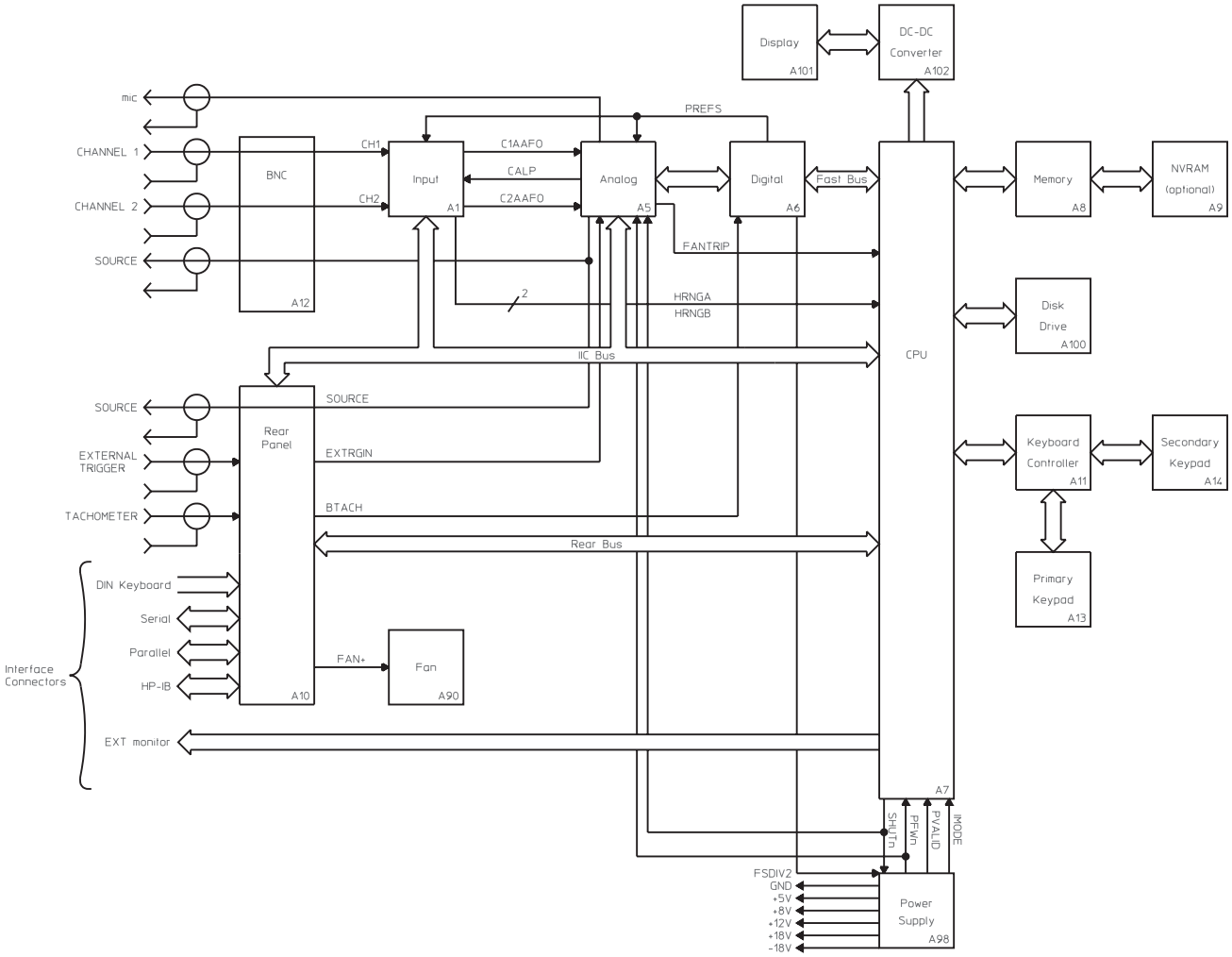
The following figures show the overall block diagrams for both the two channel and the four channel analyzer. Each block in the diagrams represents a functional block in the analyzer. The assembly that performs the function is listed in the block.

BNC	Contains the BNC connectors for both input channels and the source. For the four channel analyzer, the BNC assembly contains the BNC connectors for all four input channels. Both BNC assemblies filter the input channels HIGH (BNC center conductor) and LOW (BNC shell) input signals to reduce noise at the inputs.
Input	Buffers, attenuates, amplifies, and filters the input signals. The input assembly also provides common mode and differential overload detection, and half-range detection. The two channel analyzer contains one A1 Input assembly and the four channel analyzer contains two A2 Input assemblies.
Analog	Converts the input signals from the Input assembly (or assemblies) to digital data. The Analog assembly also converts the digital data from the Digital assembly's digital source to the analog source signal. For the two channel analyzer, the analog source signal is routed to the Rear Panel assembly and to the BNC assembly. For the four channel analyzer, the analog source signal is routed only to the Rear Panel assembly.
Digital	Prepares the digital data from the Analog assembly for the CPU assembly. This assembly also generates the digital source data for the Analog assembly.
CPU	Controls the analyzer. The following is a partial list of the operations it performs: • Configures the assemblies • Controls the Disk Drive assembly • Controls the Display assembly • Initiates the power-up sequence and calibration routine • Processes digital data from the Digital assembly • Computes the Fast Fourier Transform (FFT) • Monitors for a keystroke • Monitors the assemblies for overloads or other error conditions • Runs the self tests
DC-DC Converter	Generates the driver supply voltages for the Display assembly.
Display	Offers a view of the processed data. See the description of the Display Controller for the "A7 CPU" later in this chapter for further details.
Memory	Contains RAM, NVRAM, ROM, and the battery-backed real time clock for the CPU assembly.
NVRAM	Provides the CPU assembly with additional NVRAM. This assembly is optional.
Disk Drive	Stores and retrieves information on 3.5-inch flexible disks.
Keyboard Controller	Tells the CPU assembly which key was pressed.
Primary Keypad	Consists of hardkeys and an RPG.

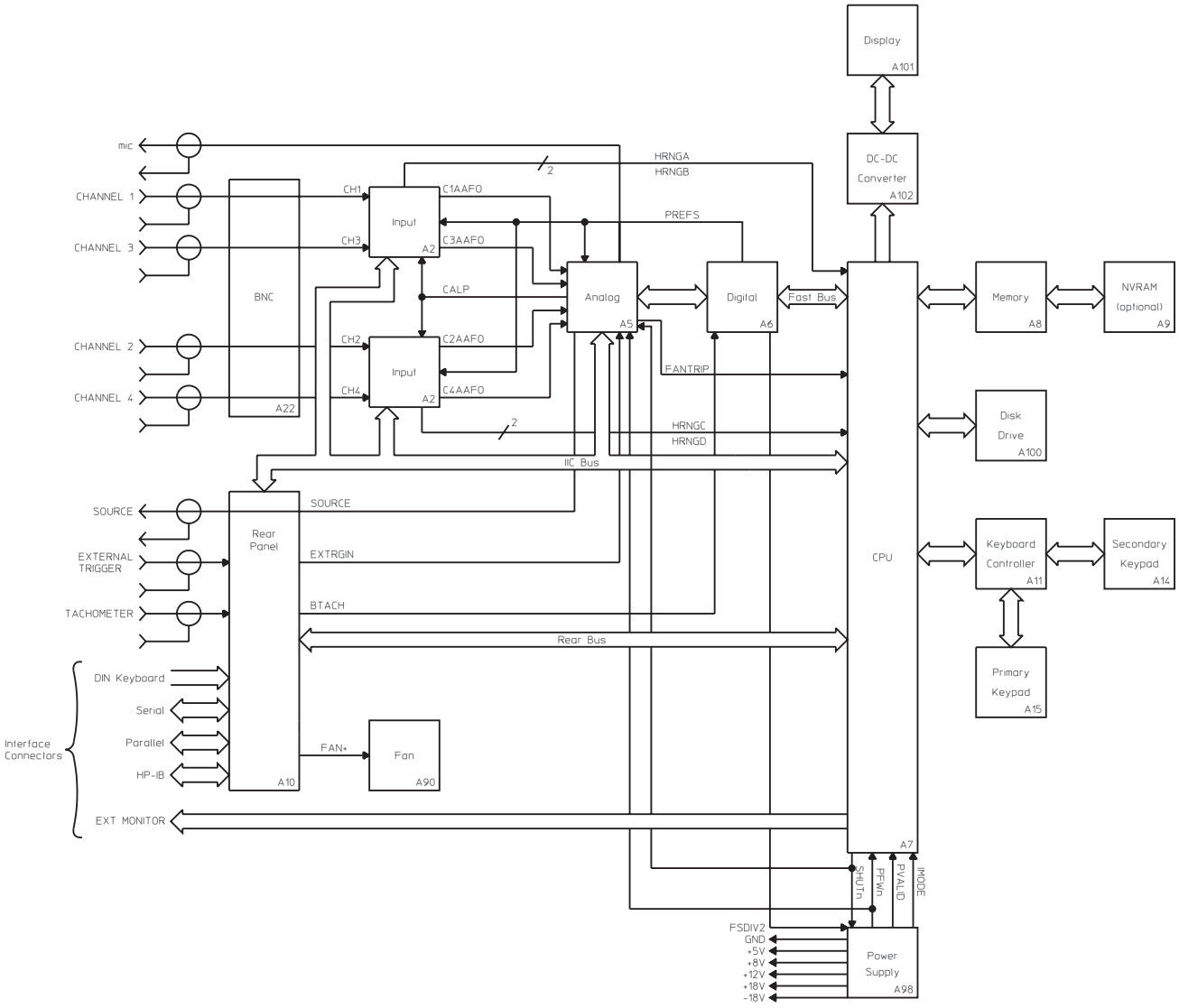
Secondary Keypad — Consists of hardkeys and softkeys.

Power Supply — Supplies the dc voltages shown in the block diagram. See “Power Supply Voltage Distribution” in chapter 9 for additional information.

Rear Panel — Provides the interface for devices connected to its GPIB connector, parallel connector, serial connector, and DIN keyboard connector. The Rear Panel assembly also provides the fan control, external trigger connector, source connector, and tachometer connector and counter.



Two Channel Overall Block Diagram



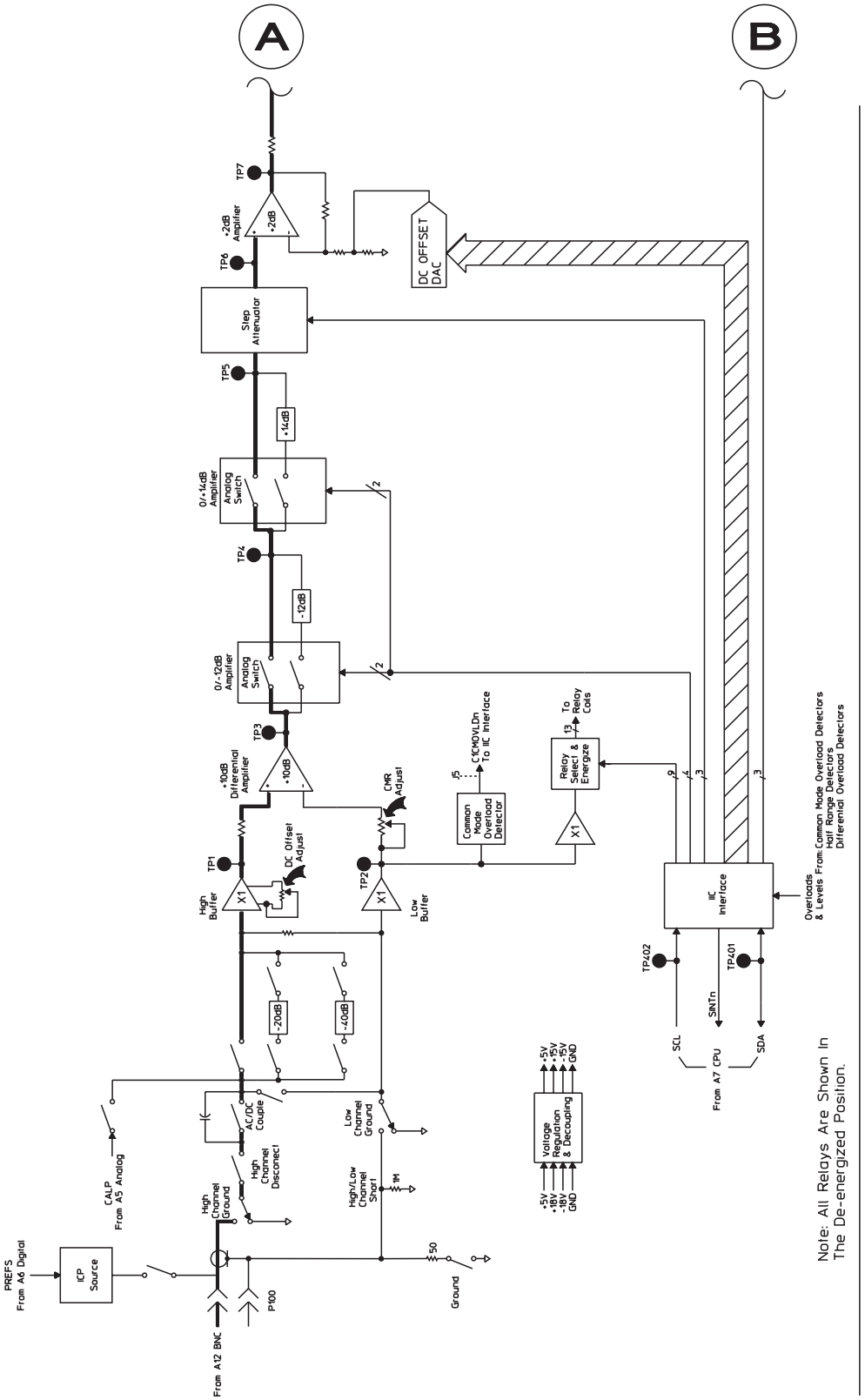
Four Channel Overall Block Diagram

A1 Input

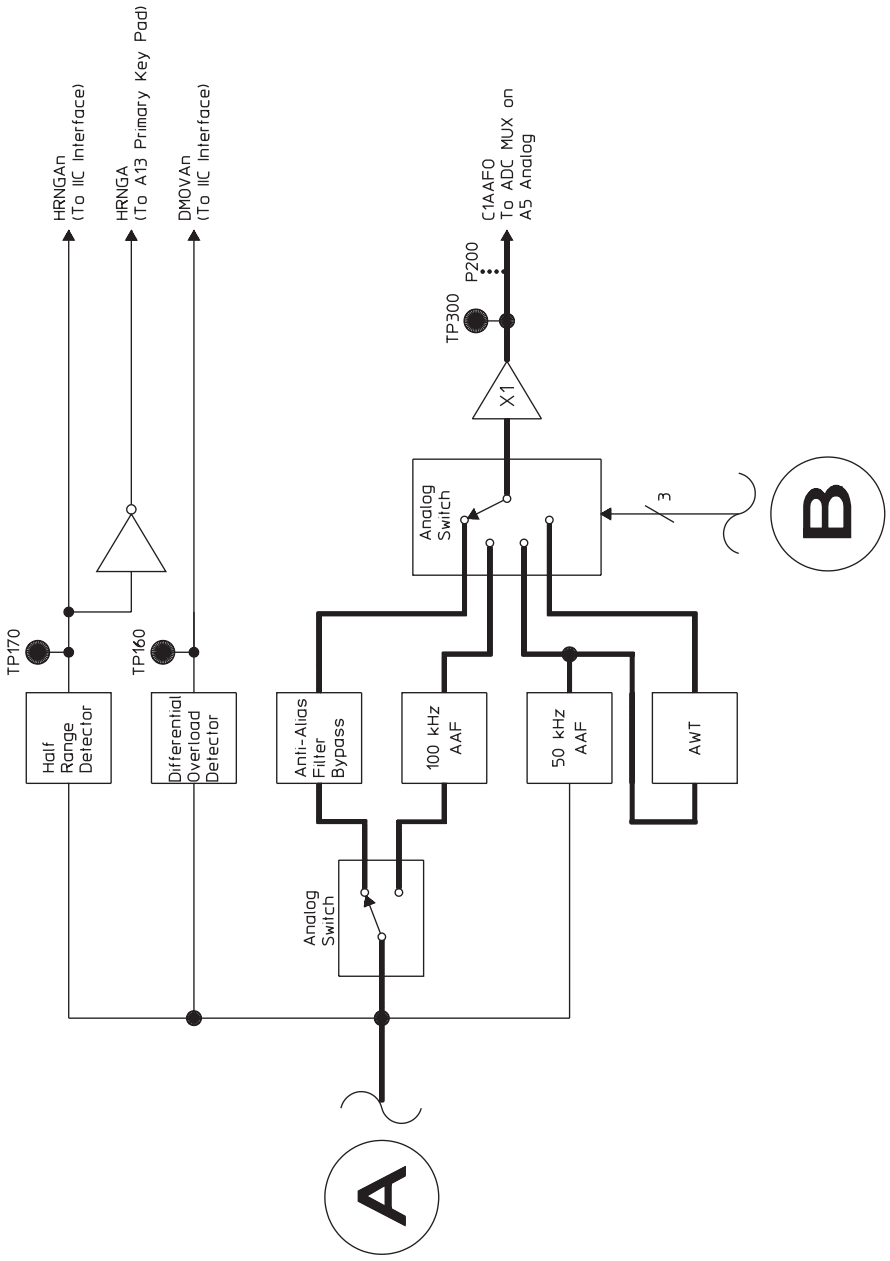
The A1 Input assembly is the input assembly for the two channel analyzer. The A1 Input assembly conditions the channel 1 and channel 2 input signals before they are sent to the analog-to-digital converter on the A5 Analog assembly. The A1 Input assembly sets the voltage ranges, conditions the input signals, and filters out alias components. Signal conditioning is done with relays, high and low buffers, and a series of amplifiers and attenuators. In addition, autozero DACs compensate for any dc offset added to the signals by the circuits on this assembly. This assembly also monitors the input signals for common mode or differential overloads and for half-range conditions. Unless stated otherwise, the following description applies to the block diagrams for both channel 1 and channel 2.

ICP Source	Supplies power to transducers such as accelerometers when enabled. The ICP Source is a 4.25 (1.5 mA floating current source. The power for the current source is obtained by switching the (15 V supplies at the sample frequency (262 kHz), isolating through a 1:1 transformer, rectifying and filtering. When disabled, the source is disconnected by a relay and the switching power supply is disabled.
Input Relays	Select one of the 0 dB, 20 dB, or 40 dB pads and configure the input. The relays are controlled by Relay Select & Energize.
Relay Select & Energize	Selects and energizes the input relays. Relay Select & Energize is controlled by the IIC Interface.
High Buffer	Buffers the HIGH input signal (BNC center conductor). The High Buffer contains a bootstrap circuit that prevents harmonic distortion and large common mode signals from saturating the buffer.
Low Buffer	Buffers the LOW input signal (BNC shell). The operation of the Low Buffer is identical to the High Buffer.
+10 dB Differential Amplifier	Begins the gain and attenuation stages. This amplifier subtracts the HIGH and LOW input signals from the high and low buffers. The common mode rejection adjustment, adjusts the +10 dB Differential Amplifier to reject common mode signals.
0 /–12 dB Amplifier	Can attenuate the signal by 12 dB.
0 /+14 dB Amplifier	Can amplify the signal by 14 dB.
Step Attenuator	Can attenuate the input signal from 0 dB to –14 dB, in 2 dB steps.
+2 dB Amplifier	Adds a gain of 2 dB and allows the DC Offset DAC to vary the dc offset of the input signal. The purpose of the amplifiers and attenuators up to this point is to ensure that the input signal does not overdrive the anti-alias filter or analog-to-digital converter.

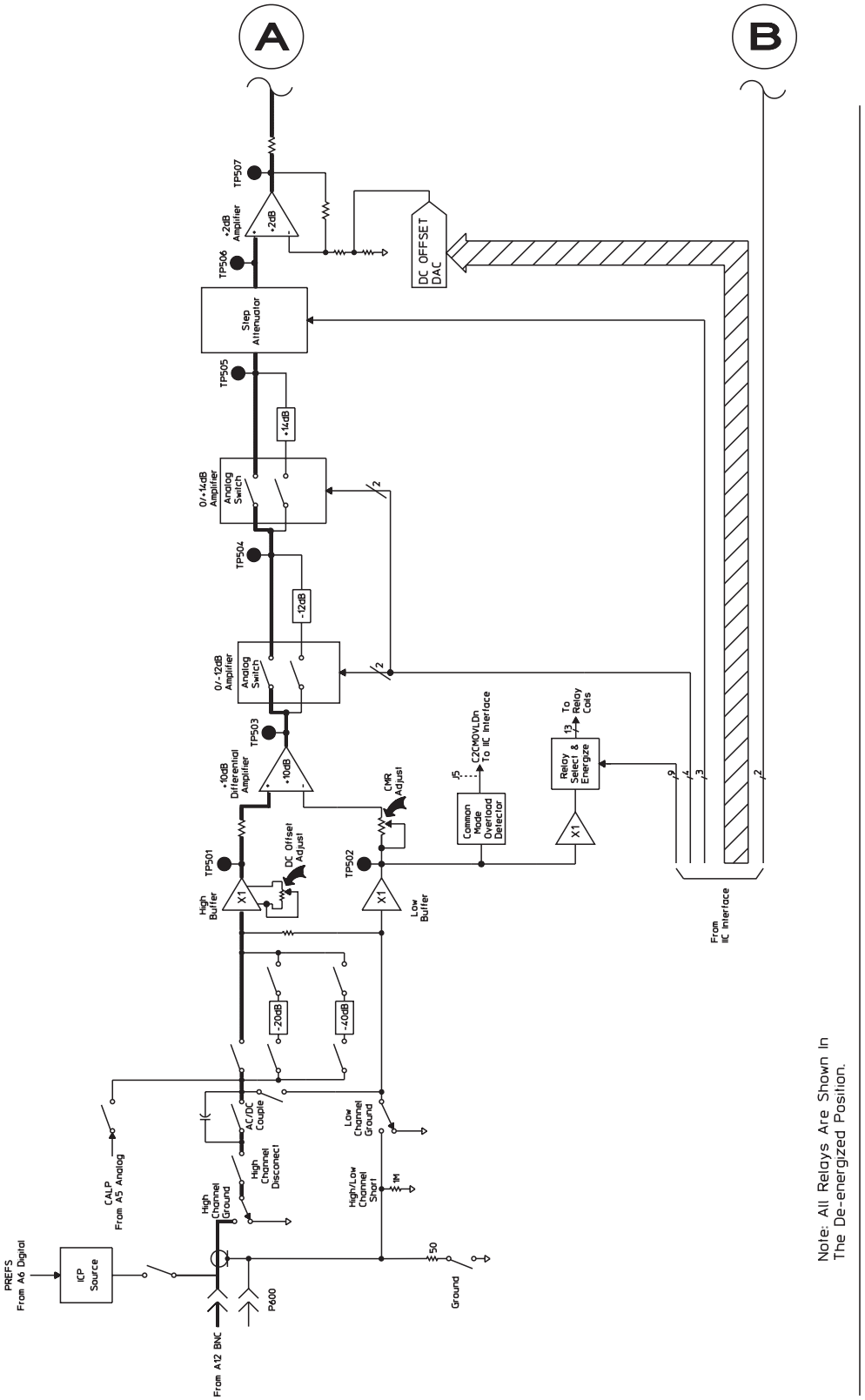
DC Offset DAC	Compensates for any dc offset added to the input signal due to circuitry in the signal path. The required dc offset is calculated during the analyzer's calibration routine and is added to the input signal in 0.345 mV increments by varying the dc offset at the inverting input of the +2 dB Amplifier (see "Calibration Routine Description" in chapter 10).
Anti-Alias Filter Bypass	Bypasses all filters.
100 kHz Anti-Alias Filter	Provides alias protection up to 100 kHz for single channel measurements. Only the channel 1 input path has a 100 kHz Anti-Alias Filter.
50 kHz Anti-Alias Filter	Provides alias protection up to 50 kHz for two channel measurements.
A-Weight Filter	Provides additional filtering in the 50 kHz anti-alias filter path for acoustic measurements.
Analog Switch	Selects one of four possible signals in the channel 1 input path to send to the ADC — the signal from the Anti-Alias Filter Bypass, 100 kHz Anti-Alias Filter, 50 kHz Anti-Alias Filter, or A-Weight Filter. In the channel 2 input path, the Analog Switch selects one of three possible signals to send to the ADC — the signal from the Anti-Alias Filter Bypass, 50 kHz Anti-Alias Filter, or A-Weight Filter.
Half Range and Differential Overload Detectors	Sense the signal at the anti-alias filters. When a detector detects a half-range or overload condition, a digital low is sent to the IIC Interface by the detector. The half-range detector also sends a control signal to the A13 Primary Keypad assembly when a half-range condition occurs.
IIC (Inter-IC) Interface	Contains 32 ports and connects the A1 Input assembly to the serial IIC bus. The A7 CPU assembly uses the IIC bus to configure the input circuits. When a common mode or differential overload occurs, the IIC Interface forces SINTn low to interrupt the CPU assembly. The CPU assembly then reads the IIC Interface to determine the type of interrupt and the channel it occurred on. During up/down autoranging, the A7 CPU queries the A1 Input assembly for half range status. For a description of the IIC bus, see the description of the IIC Controller for the "A7 CPU" later in this chapter.



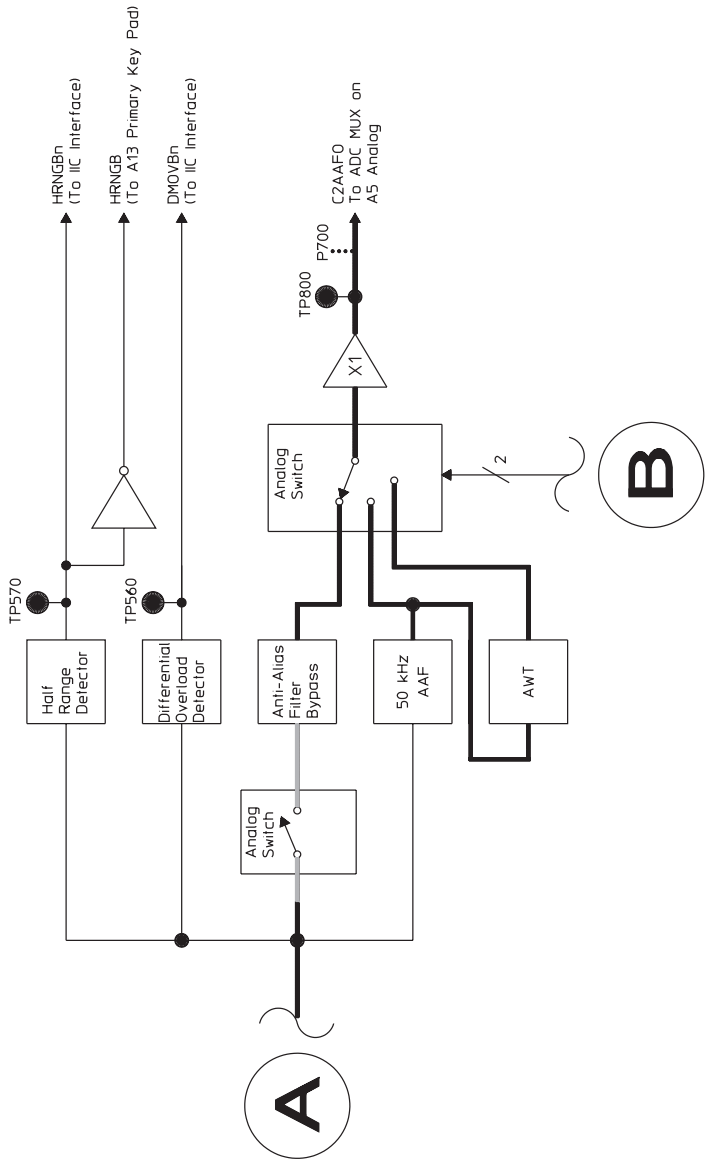
A1 Input Block Diagram: Channel 1



A1 Input Block Diagram: Channel 1 (continued)



A1 Input Block Diagram: Channel 2



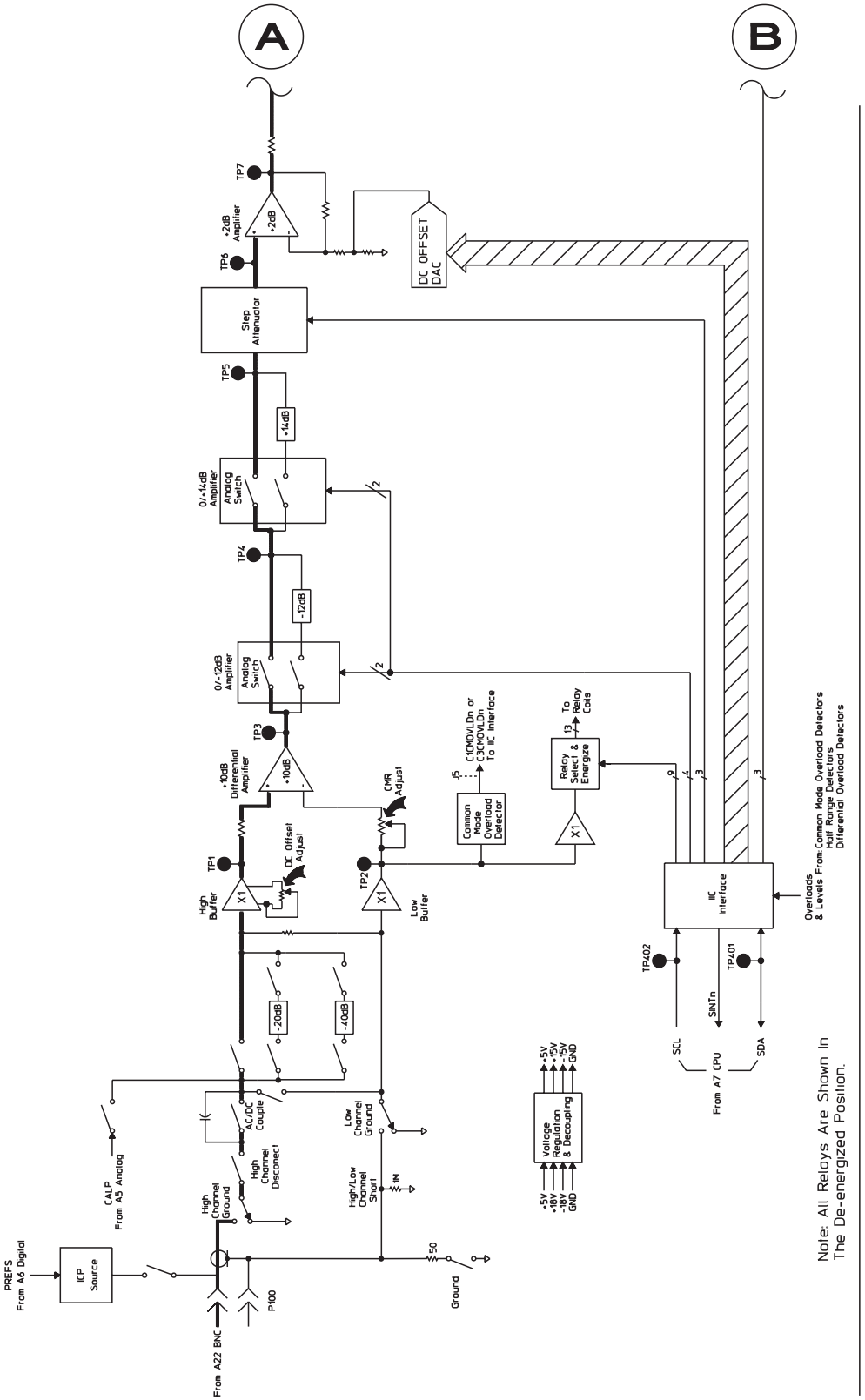
A1 Input Block Diagram: Channel 2 (continued)

A2 Input

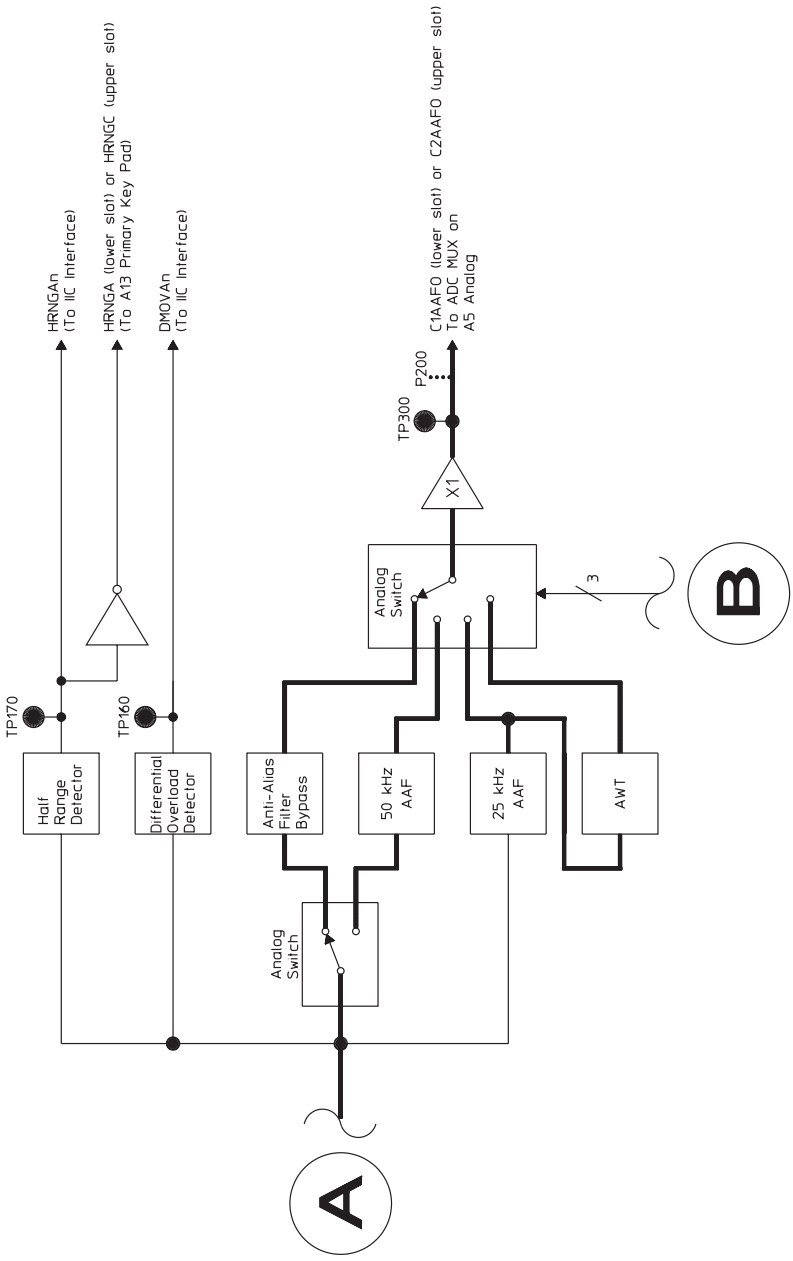
The A2 Input assembly is the input assembly for the four channel analyzer. The four channel analyzer contains two A2 Input assemblies. The A2 Input assembly connected to J1 on the Motherboard conditions the channel 1 and channel 3 input signals before they are sent to the analog-to-digital converter on the A5 Analog assembly. The A2 Input assembly connected to J2 on the Motherboard conditions the channel 2 and channel 4 input signals before they are sent to the analog-to-digital converter on the A5 Analog assembly. The Input assembly sets the voltage ranges, conditions the input signals, and filters out alias components. Signal conditioning is done with relays, high and low buffers, and a series of amplifiers and attenuators. In addition, autozero DACs compensate for any dc offset added to the signals by the circuits on this assembly. The assembly also monitors the input signals for common mode or differential overloads and for half-range conditions. Unless stated otherwise, the following description applies to the block diagrams for all four channels.

ICP Source	Supplies power to transducers such as accelerometers when enabled. The ICP Source is a 4.25 (1.5 mA floating current source. The power for the current source is obtained by switching the (15 V supplies at the sample frequency (262 kHz), isolating through a 1:1 transformer, rectifying and filtering. When disabled, the source is disconnected by a relay and the switching power supply is disabled.
Input Relays	Select one of the 0 dB, 20 dB, or 40 dB pads and configure the input. The relays are controlled by Relay Select & Energize.
Relay Select & Energize	Selects and energizes the input relays. Relay Select & Energize is controlled by the IIC Interface.
High Buffer	Buffers the HIGH input signal (BNC center conductor). The High Buffer contains a bootstrap circuit that prevents harmonic distortion and large common mode signals from saturating the buffer.
Low Buffer	Buffers the LOW input signal (BNC shell). The operation of the Low Buffer is identical to the High Buffer.
+10 dB Differential Amplifier	Begins the gain and attenuation stages. This amplifier subtracts the HIGH and LOW input signals from the high and low buffers. The common mode rejection adjustment, adjusts the +10 dB Differential Amplifier to reject common mode signals.
0 /–12 dB Amplifier	Can attenuate the signal by 12 dB.
0 /+14 dB Amplifier	Can amplify the signal by 14 dB.
Step Attenuator	Can attenuate the input signal from 0 dB to –14 dB, in 2 dB steps.
+2 dB Amplifier	Adds a gain of 2 dB and allows the DC Offset DAC to vary the dc offset of the input signal. The purpose of the amplifiers and attenuators up to this point is to ensure that the input signal does not overdrive the anti-alias filter or analog-to-digital converter.

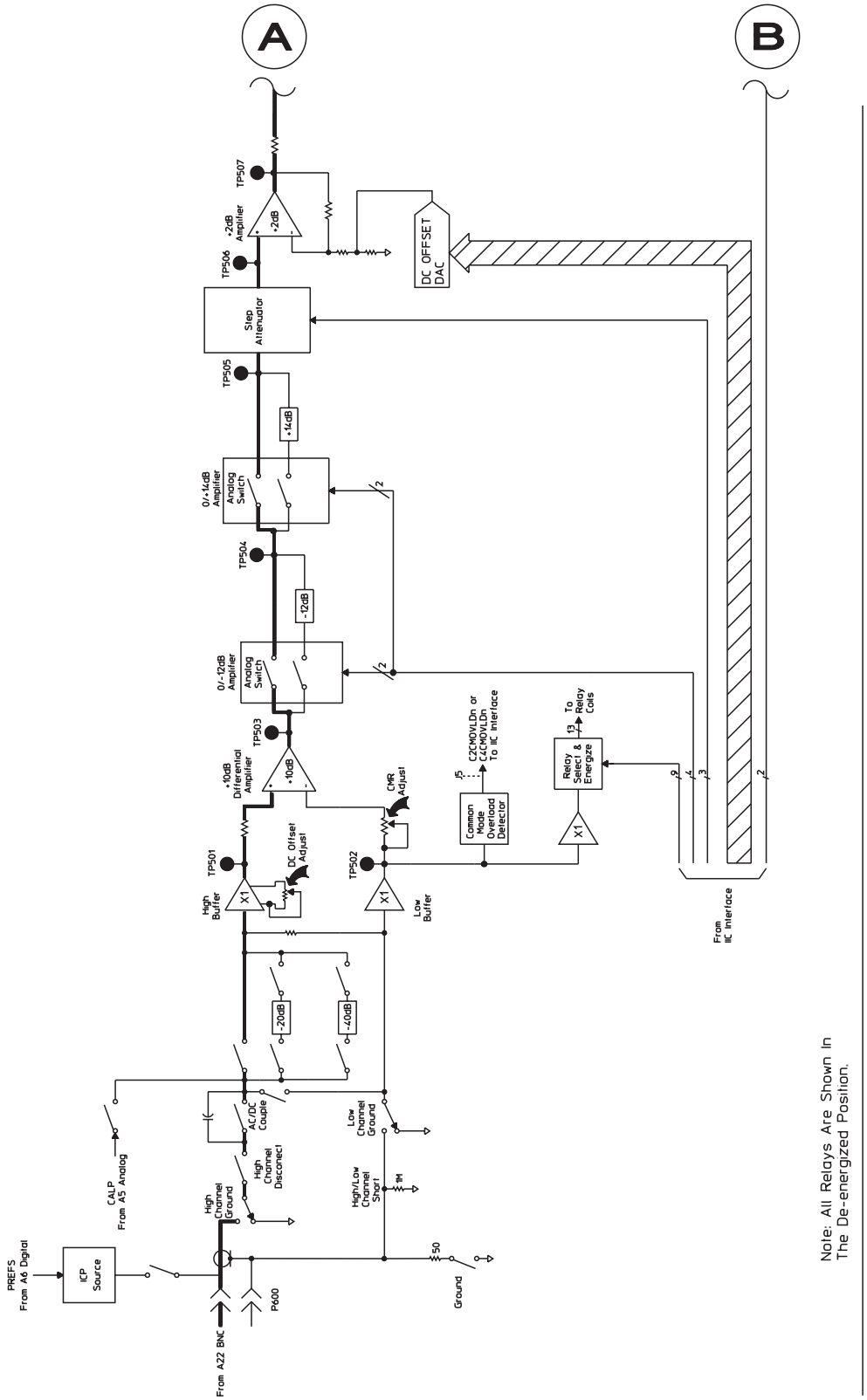
DC Offset DAC	Compensates for any dc offset added to the input signal due to circuitry in the signal path. The required dc offset is calculated during the analyzer's calibration routine and is added to the input signal in 0.3.45 mV increments by varying the dc offset at the inverting input of the +2 dB Amplifier (see "Calibration Routine Description" in chapter 10).
Anti-Alias Filter Bypass	Bypasses all filters.
50 kHz Anti-Alias Filter	Provides alias protection up to 50 kHz for two channel measurements.
25 kHz Anti-Alias Filter	Provides alias protection up to 25 kHz for four channel measurements.
A-Weight Filter	Provides additional filtering in the 25 kHz anti-alias filter path for acoustic measurements.
Analog Switch	Selects one of four possible signals in the channel 1 or channel 2 input path to send to the ADC — the signal through the Anti-Alias Filter Bypass, 50 kHz Anti-Alias Filter, 25 kHz Anti-Alias Filter, or A-Weight Filter. In the channel 3 or 4 input path, the Analog Switch selects one of three possible signals to send to the ADC — the Anti-Alias Filter Bypass, 25 kHz Anti-Alias Filter, or the A-Weight Filter.
Half Range and Differential Overload Detectors	Sense the signal at the anti-alias filters. When a detector detects a half-range or overload condition, a digital low is sent to the IIC Interface by the detector. The half-range detector also sends a control signal to the A13 Primary Keypad assembly that lights an LED when a half-range condition occurs.
IIC (Inter-IC) Interface	Contains 32 ports and connects the A2 Input assembly to the serial IIC bus. The A7 CPU assembly uses the IIC bus to configure the input circuits. When a common mode or differential overload occurs, the IIC Interface forces SINTn low to interrupt the CPU assembly. The CPU assembly then reads the IIC Interface to determine the type of interrupt and the channel it occurred on. During up/down autoranging, the A7 CPU queries the A1 Input assembly for half range status. For a description of the IIC bus, see the description of the IIC Controller for the "A7 CPU" later in this chapter.



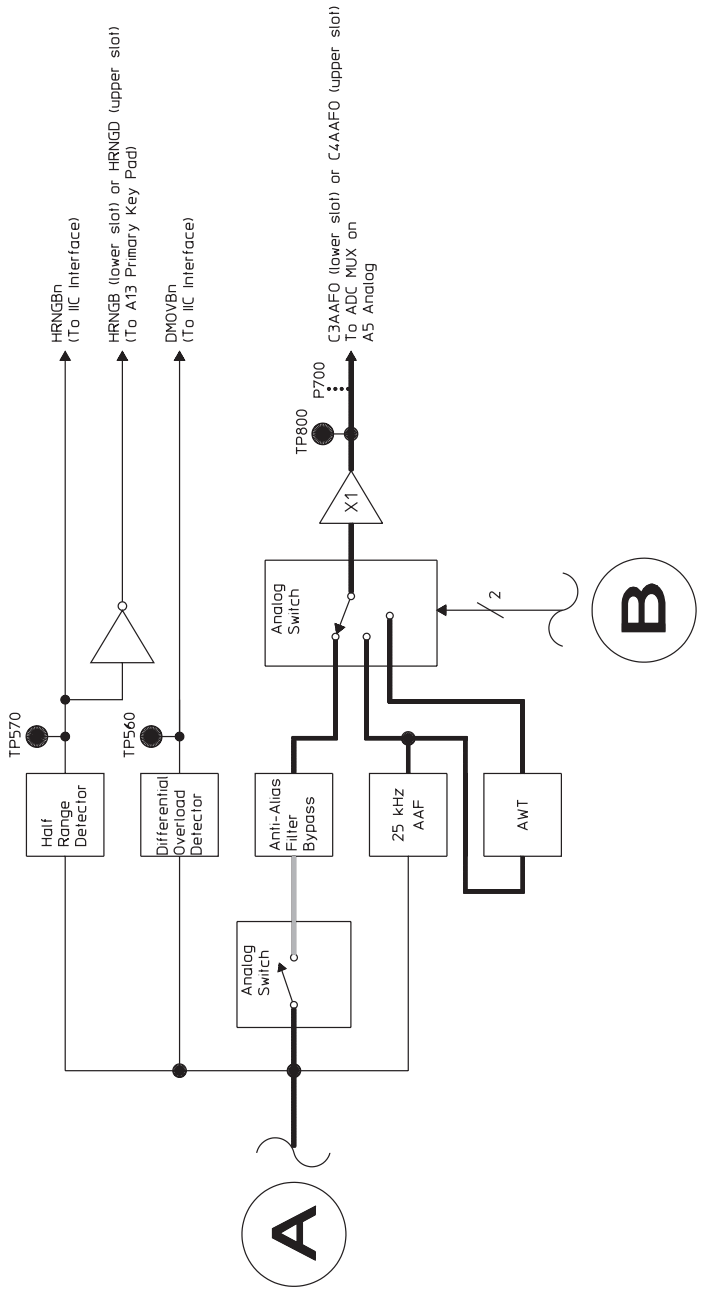
A2 Input Block Diagram: Channel 1 or Channel 2



A2 Input Block Diagram: Channel 1 or Channel 2 (continued)



A2 Input Block Diagram: Channel 3 or Channel 4



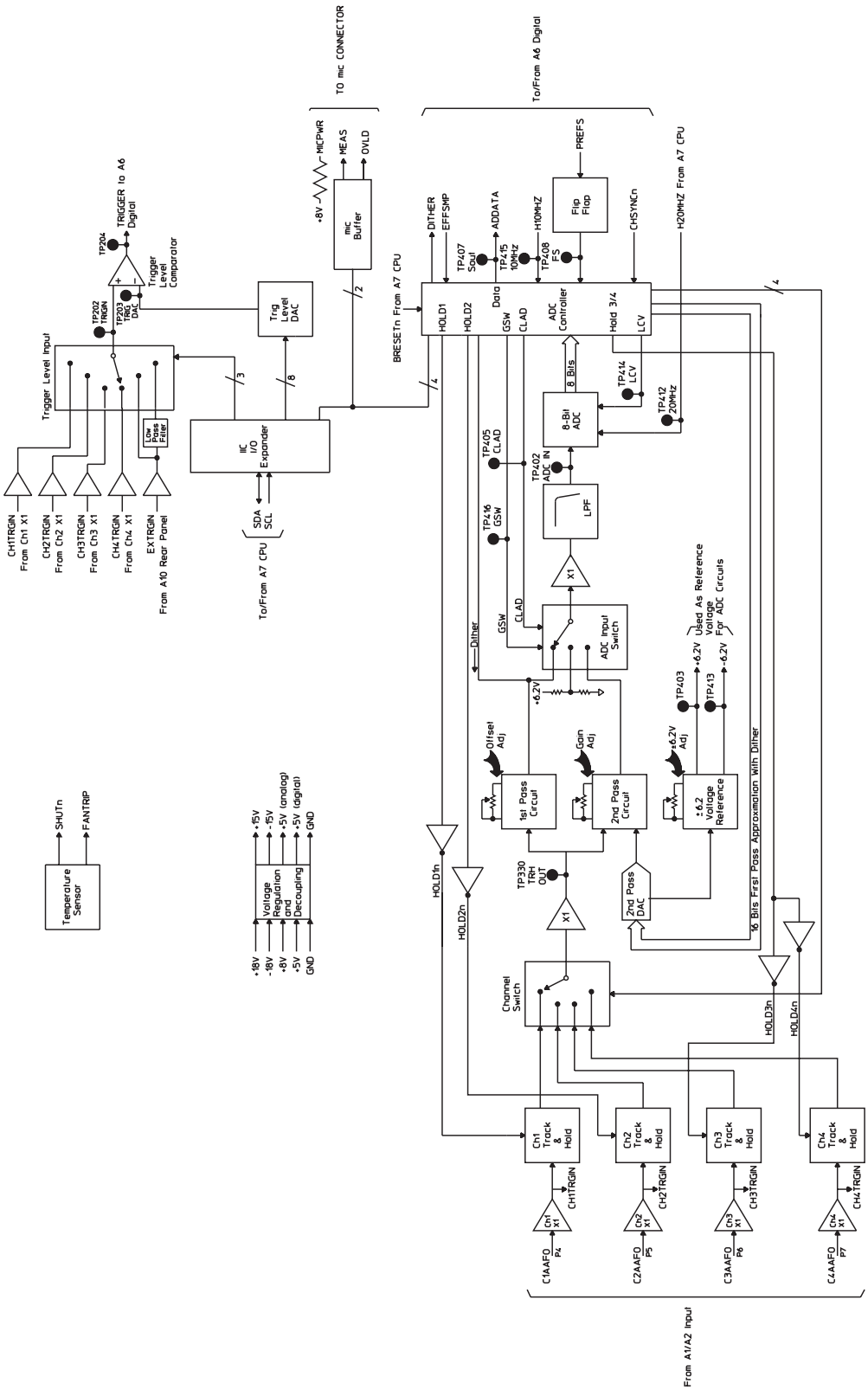
A2 Input Block Diagram: Channel 3 or Channel 4 (continued)

A5 Analog

The A5 Analog assembly converts the analog input from the A1 Input assembly or A2 Input assemblies to 16-bit serial, digital data. The Analog assembly also converts digital data from the A6 Digital assembly to the analog source output.

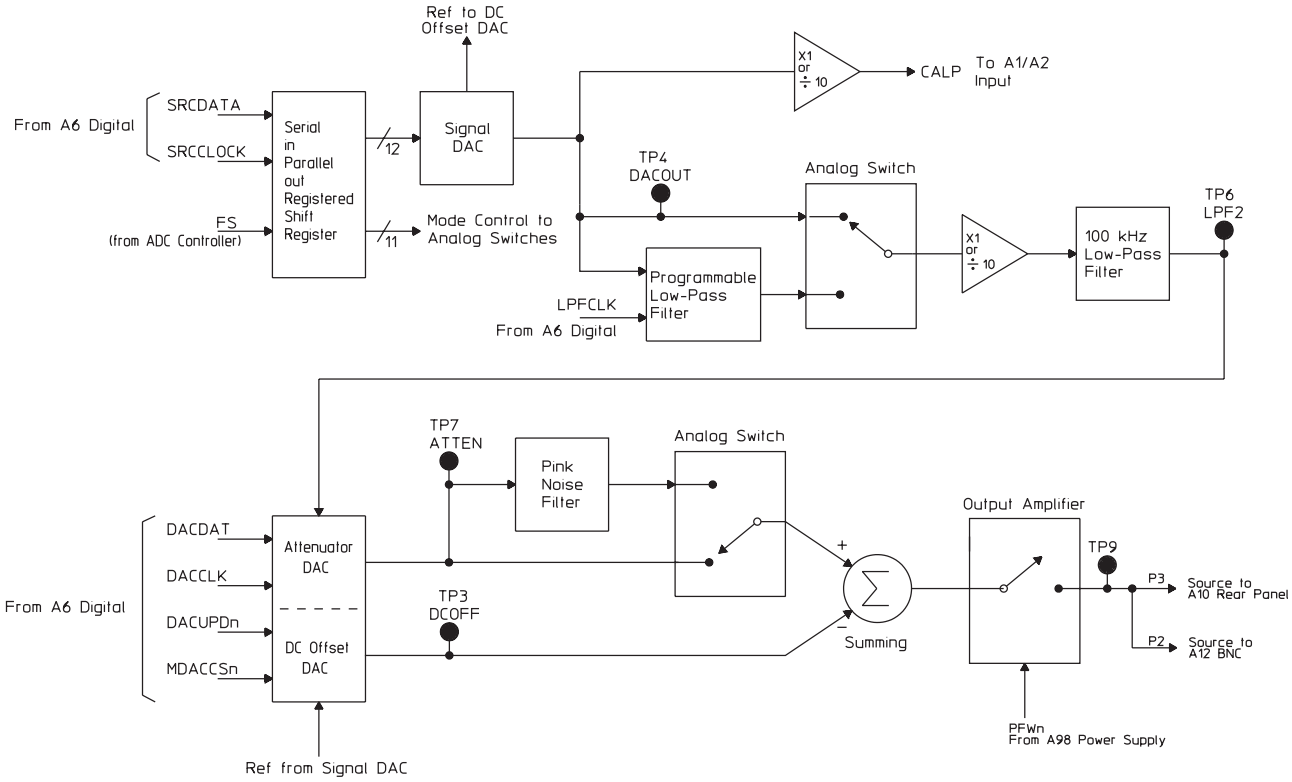
The input conversion process passes the analog inputs from all active channels through an 8-bit ADC (analog-to-digital converter) twice adding dither (noise) to improve linearity and the accuracy of low-level signals. All active inputs are sampled simultaneously and held until all have been converted. For the first-pass conversion, the input is scaled then converted to 8-bit serial, digital data. Dither is added to the first-pass data and the sum is converted to an analog voltage. The analog voltage is subtracted from the input and the difference is scaled then converted to 8-bit, serial data in the second pass. The first-pass and second-pass values are added to get the final 16-bit data word. A third conversion clears the 8-bit ADC.

Channel 1 Track & Hold	Holds a voltage sample of the channel 1 input signal for the period of time required by the ADC circuits to digitize the voltage.
Channel 2 Track & Hold	Holds a voltage sample of the channel 2 input signal for the period of time required by the ADC circuits to digitize the voltage.
Channel 3 Track & Hold	Holds a voltage sample of the channel 3 input signal for the period of time required by the ADC circuits to digitize the voltage.
Channel 4 Track & Hold	Holds a voltage sample of the channel 4 input signal for the period of time required by the ADC circuits to digitize the voltage.
Channel Switch	For the two channel analyzer, the Channel Switch multiplexes the channel 1 and channel 2 input signals during two channel measurements . During single channel measurements, the channel 1 and channel 2 signals are not multiplexed. Instead, the Channel Switch is fixed to the output of the Channel 1 Track & Hold. For the four channel analyzer, the Channel Switch multiplexes the channel 1 and channel 2 input signals during two channel measurements. During four channel measurements, the Channel Switch multiplexes the channel 1, 2, 3, and 4 input signals. The output of the Channel Switch is converted to a 16-bit digital word by passing the signal through an 8-bit ADC twice.
1st Pass Circuit	Divides the Channel Switch output by four and level shifts it to the 8-bit ADC input range of 0 to –0.5 V.
ADC Controller	Adds dither (noise) to the first pass signal to increase the accuracy and reduce the non-linearity of the Analog-to-Digital conversion. After the first pass signal is filtered and converted to an 8-bit word, the ADC Controller adds the dither and outputs a 16-bit word to the 2nd Pass DAC. After the second pass signal is filtered and converted to an 8-bit word, the ADC Controller adds the second pass word to the first pass word to obtain a 16-bit data word. The ADC Controller then sends the converted data as ADDATA to the A6 Digital assembly. The ADC Controller also detects an ADC overload when the signal to the analog-to-digital converter is too high. The overload information is sent as ADCOL and ADCUL to the A6 Digital assembly.



A5 Analog Block Diagram: ADC and Trigger

ADC Input Switch	Connects the first pass signal to the low pass filter on the first pass. On the second pass, the ADC Input Switch connects the second pass signal to the low pass filter. After the second pass, the ADC Input Switch connects a 0.34 Vdc signal to the low pass filter to reset the 8-Bit ADC.
Low Pass Filter	Reduces noise and prevents high frequency signals from overdriving the 8-bit ADC.
8-Bit ADC	Converts the signal to an 8-bit word.
2nd Pass DAC	Converts the first pass word plus dither to a voltage that is sent to the 2nd Pass Circuit.
2nd Pass Circuit	Compares the output of the 2nd Pass DAC (converted first pass signal plus dither) to the original input signal (which is still held by the Track & Hold) and produces a difference voltage. This difference voltage is the second pass signal.
±*6.2 Voltage Reference*	Reduces the error due to temperature variations. This voltage reference is used by the 1st Pass Circuit, 2nd Pass Circuit, ADC Input Switch, 8-bit ADC, and Track & Hold. Since the 8-bit ADC's gain is derived from this voltage reference, the adjustment for this voltage reference is also the gain adjustment for the 8-bit ADC.
Trigger-Level Input	Connects the appropriate signal to the Trigger-Level Comparator.
Temperature Sensor	Senses the analyzer's internal temperature. If the internal temperature exceeds a set point, this circuit sets FANTRIP high which turns the fan back on if the fan was turned off by the user. If the temperature becomes excessive, this circuit sets SHUTn low which forces all A98 Power Supply assembly output voltages to zero.
Trigger-Level Comparator	Compares the signal level with the value from the Trigger Level DAC.
Trigger Level DAC	Provides the trigger level. The A7 CPU assembly sets the trigger level via the IIC bus using the value set with the [TRIGGER SETUP] and [LEVEL] softkeys.
Mic Buffer	Buffers control signals for the optional sound intensity probe. When a measurement is being made, the MEAS line goes high to turn on the probe's green LED. If an overload occurs during the measurement, the OVLD line goes high to turn on the probe's yellow LED.
IIC Interface	Provides the interface between the A7 CPU assembly and the A5 Analog assembly.
Serial In Parallel Out Shift Register	Provides the mode control to the Analog Switches and the digital source data to the DAC.
Signal DAC	Converts the digital source data to an analog signal. During calibration, the analog signal from the DAC is buffered or attenuated by 10. The calibration signal (CALP) is then routed to each input channel.
Programmable Low-Pass Filter	Filters the analog signal from the Signal DAC when selected. Filter bandwidth is set by LPFCLK from the A6 Digital assembly; it can be set from 51.2 kHz to 1.56 Hz in binary steps. Random noise and burst random noise signals below 51.2 kHz are filtered. Arbitrary signals below 51.2 kHz can be filtered using the front panel keys.
100 kHz Low-Pass Filter	Provides image rejection, reduces noise, and prevents high frequency signals from overdriving the Attenuator DAC. It also compensates for sinx/x rolloff at the 262.144 kHz sample rate.
Attenuator DAC/DC Offset DAC	Attenuates the signal and generates a dc offset.
Pink Noise Filter	Shapes the noise for a flat response in octave mode.
Summing	Combines the signal with the dc offset.
Output Amplifier	Amplifies and buffers the signal. A relay disconnects the signal from the SOURCE connector 10 ms before the A98 Power Supply assembly's output voltages fall out of regulation.



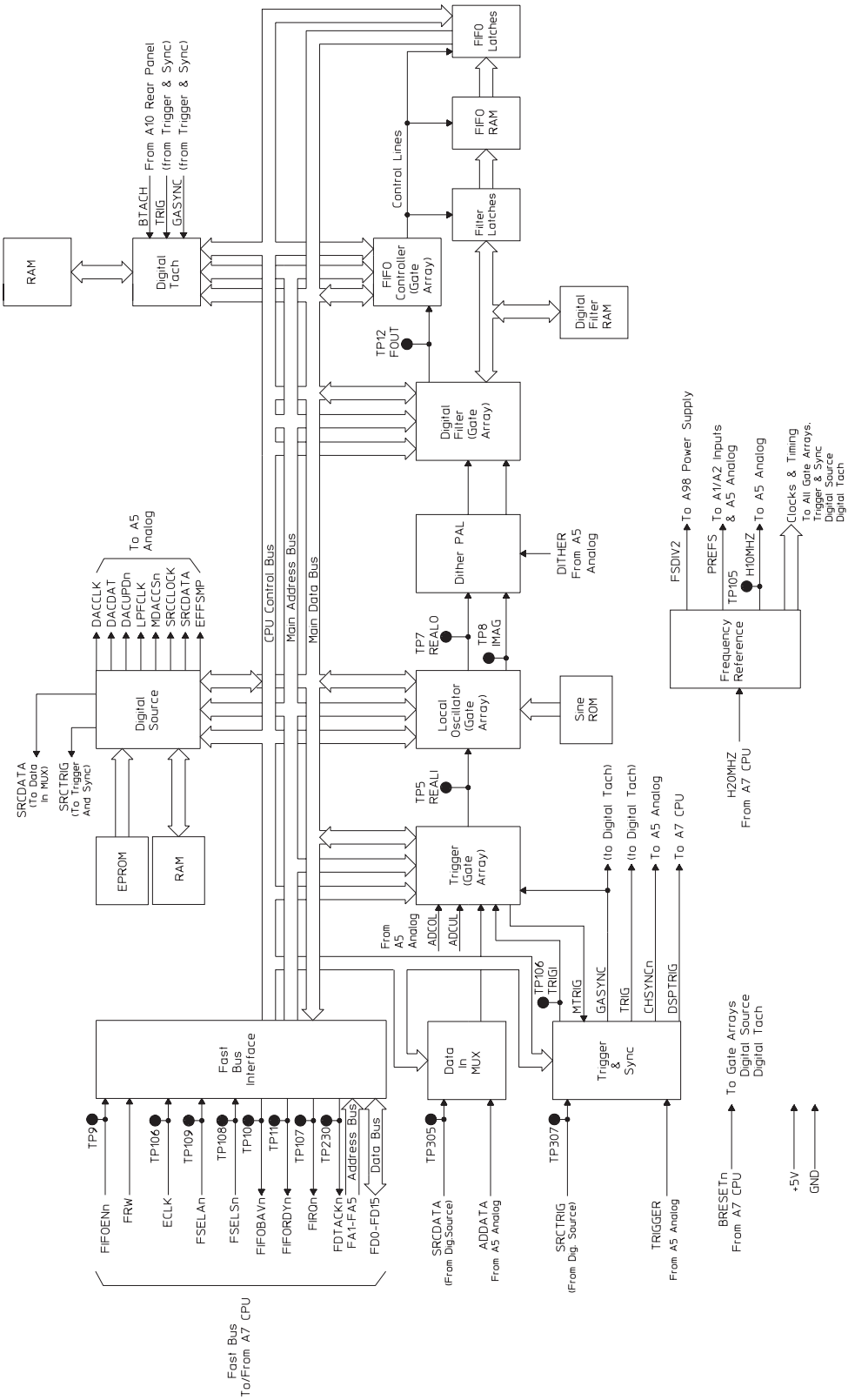
A5 Analog Block Diagram: Analog Source and Calibrator

A6 Digital

The A6 Digital assembly prepares the digital input data for the A7 CPU assembly. The Digital assembly also generates the digital source data for the A5 Analog assembly. The Digital assembly receives the input signals as 16-bit serial, digital data from the Analog assembly. The Digital assembly uses digital signal processing to prepare the data for the CPU assembly. The CPU assembly configures the Digital assembly via the fast bus. This includes setting up the source, calibrator, and all gate arrays. See "A99 Motherboard" in chapter 9 for a description of the fast bus signals. This assembly provides the following:

- Trigger
- Local Oscillator
- Digital Filter and RAM
- FIFO Controller and RAM
- Digital Source
- Digital Tachometer
- ADC timing and synchronization signals

Data in MUX	Selects ADDATA from the A5 Analog assembly for most modes of operation. For time capture and some self-tests, the Data in Mux selects SRCDATA from the Digital Source.
Trigger & Sync	Pulls TRIGI low to inform the Trigger circuit that the selected trigger occurred. Synchronizes the ADC (on the A5 Analog assembly), Digital Source, Digital Tach, and Trigger Gate Array.
Trigger Gate Array	Synchronizes data transfer by telling the FIFO Controller when to collect the time record in FIFO RAM. This circuit also controls pre- and post-trigger.
Local Oscillator	Frequency shifts the data to allow start frequencies other than 0 hertz. To frequency shift the data, the Local Oscillator digitally mixes or heterodynes the data down into the range of the FFT span selected. This makes the data complex and the sample is now represented by two serial, digital signals — REALO and IMAG. During baseband measurements (where the start frequency is 0 hertz), the data is only scaled through the Local Oscillator.
Dither PAL	Adds span-dependent dither (noise) to the digital data.
Digital Filter	Filters the digital data before placing the samples in the Filter Latches for the FIFO. As the Digital Filter operates, it may discard some samples to effectively reduce the sample rate. This allows frequency spans narrower than full span (due to the properties of the FFT, the sample rate must be varied to vary the frequency span). During full span measurements, no samples are discarded and data is just passed through.
Digital Filter RAM	Stores intermediate values for the Digital Filter during the filtering process.
Filter Latches	Temporarily hold a data point as it is passed from the Digital Filter to the FIFO RAM.



A6 Digital Block Diagram

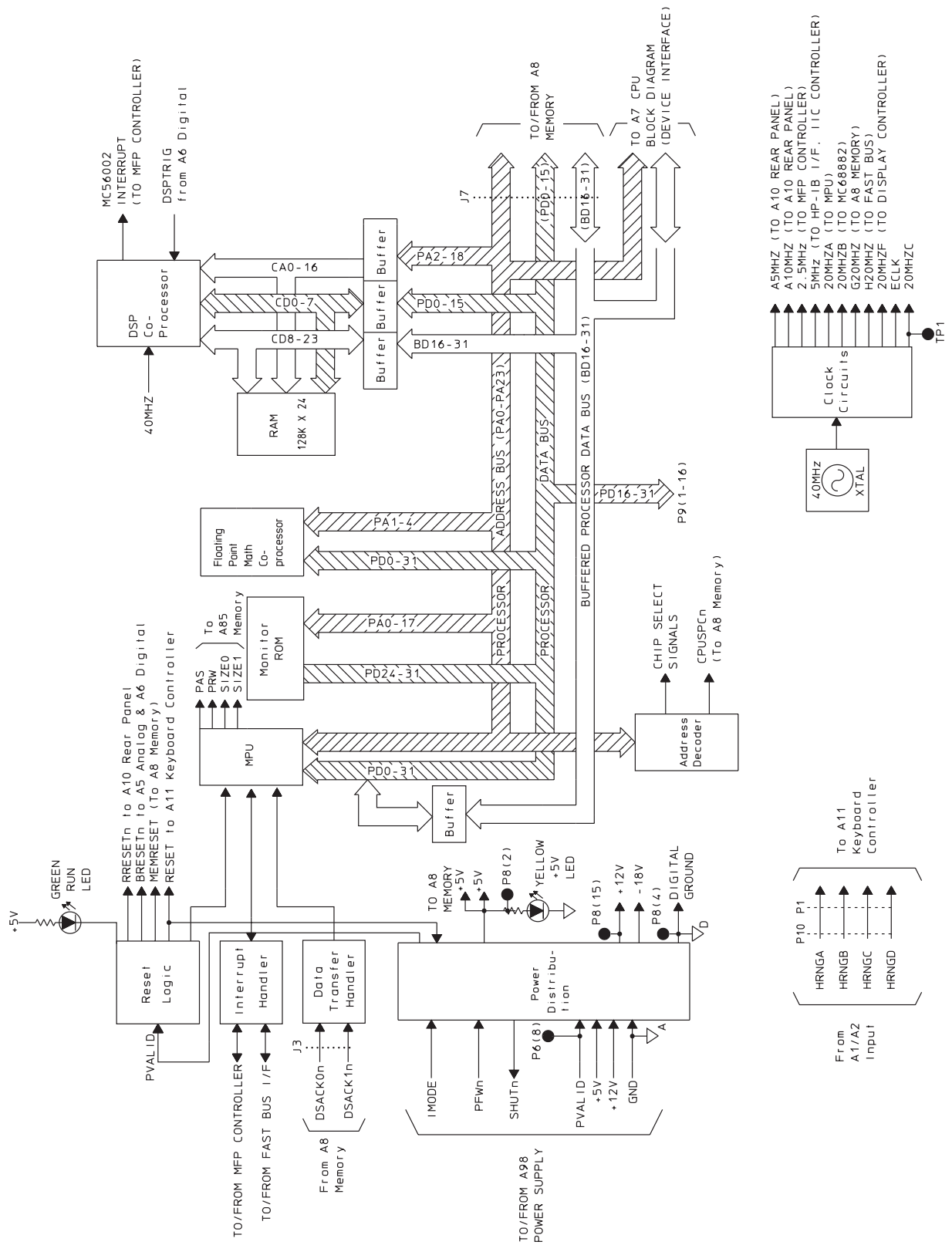
FIFO Controller	Gathers the data from the Filter Latches when the selected trigger occurs and places the data into FIFO RAM. After a time record is collected, this circuit controls data flow from FIFO RAM to the CPU.
FIFO RAM	Stores data from the Digital Filter. When the FIFO RAM has a complete time record, the FIFO Controller pulls FIFOBAVn low to inform the A7 CPU assembly that a block of data is ready for transfer.
FIFO Latches	Hold a data sample until the Fast Bus Interface is ready to transfer the sample.
Digital Source and RAM	The A7 CPU assembly loads the Digital Source RAM by putting the data needed by the Digital Source into main memory (on the A8 Memory assembly). The CPU assembly then performs a memory-to-memory DMA transfer from main memory to Digital Source RAM via the fast bus. This data represents any source type except random, pink, or fixed sine which are generated internally by the Digital Source. Any source type, except fixed sine, will be frequency-translated and bandwidth-limited to correspond to the instrument frequency range.
Digital Tachometer and RAM	Counts and stores the buffered tachometer pulses (BTACH) from the A10 Rear Panel assembly. At the start of a measurement, GASYNC sets the Digital Tachometer's counter to zero. The counter starts counting and the tachometer signal latches the counter outputs. The latched tachometer times are stored in RAM and read over the Fast Bus Interface by the A7 CPU assembly as needed.
Frequency Reference	Provides all clocks and timing for the gate arrays, Trigger & Sync, Digital Source, and Digital Tach. In addition, the Frequency Reference generates PREFS and H10MHZ to synchronize data transfers from the ADC on the A5 Analog assembly, and FSDIV2 for the A98 Power Supply assembly.
Fast Bus Interface	Connects the A6 Digital assembly to the fast bus. The fast bus transfers time records from FIFO RAM to the A7 CPU assembly for processing. The fast bus is also used by the CPU assembly to read tachometer data, to send time capture data or source data to the Digital Source, and to configure the Trigger, Local Oscillator, Digital Filter, FIFO Controller, Digital Source and Digital Tachometer.

A7 CPU

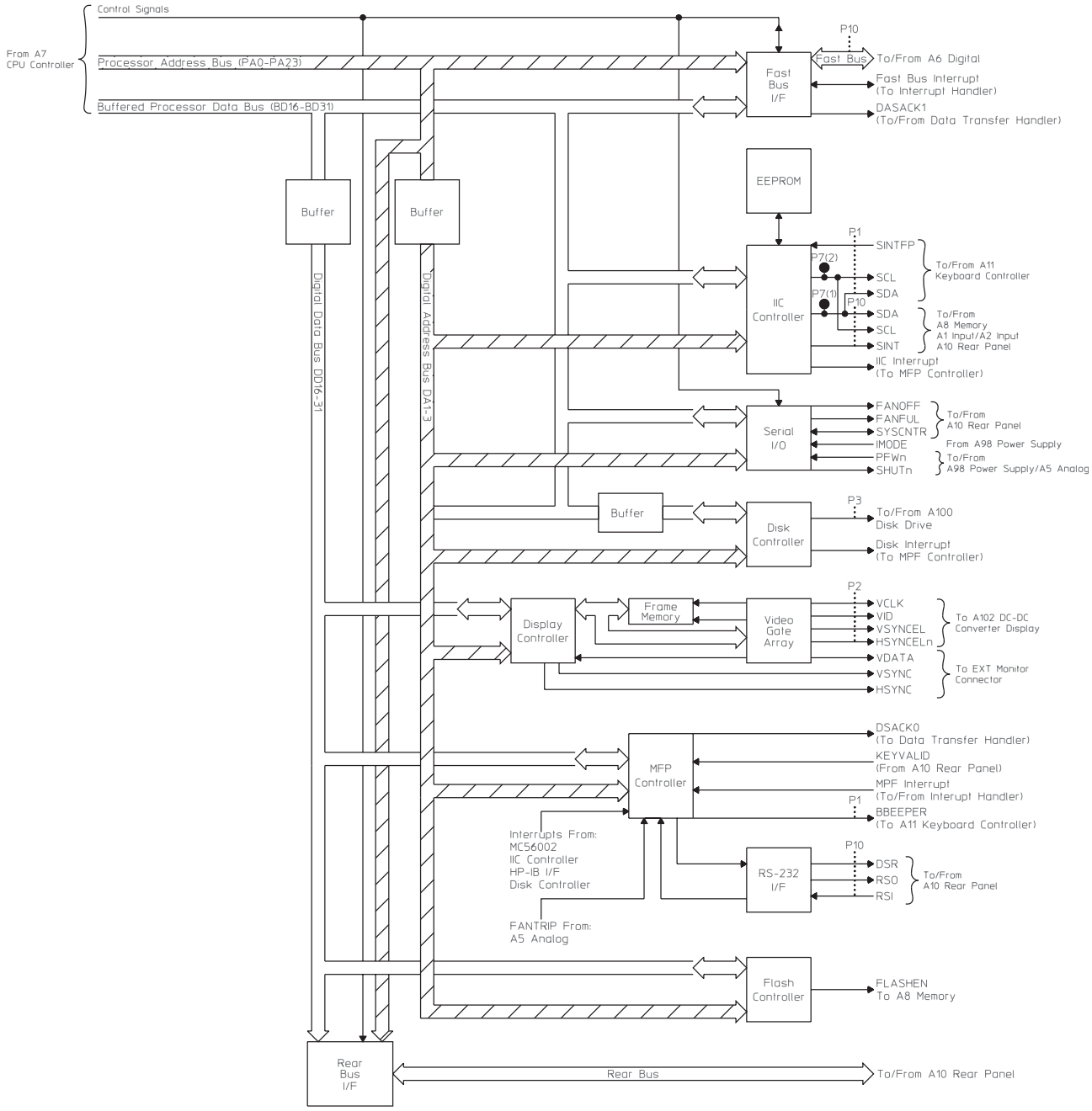
The A7 CPU assembly controls the entire analyzer. It performs multiple tasks, such as:

- Initiating the power-up sequence and calibration routines
- Capturing front panel keystrokes
- Configuring the measurement hardware
- Processing input data from the A6 Digital assembly
- Controlling the A101 Display assembly
- Monitoring the hardware for faults or overloads
- Running the self tests
- Handling all data transfers for the fast bus, rear bus, and A100 Disk Drive assembly

MPU (Microprocessor)	Controls the processor address bus and the buffered processor data bus. At power-up, this circuit initializes the analyzer from the information stored in the Monitor ROM. This circuit also processes interrupts from the Interrupt Handler and synchronizes data transfers on the processor data bus with the Data Transfer Handler. The MPU also has access to battery-backed-up SRAM on the A8 Memory assembly. This allows the CPU assembly to store and update information such as the analyzer's address, default disk, and peripheral addresses.
Monitor ROM	Stores the information used by the MPU to initialize the analyzer.
DSP and Floating Point Math Co-processor	Relieve the MPU of math intensive-tasks by supplying the computational power needed for accurate, high-speed signal processing operations — for example, windowing and Fast Fourier Transform (FFT) for the analyzer's narrow-band zoom mode. The DSP Co-processor is a high speed (40 MHz) math co-processor that performs complex mathematical operations. The Floating Point Math Co-processor performs floating point mathematical operations. The DSP Co-processor and Floating Point Math Co-processor work as slave co-processors to the MPU and the DSP Co-processor has its own RAM. This arrangement leaves the MPU free to perform other functions while the DSP Co-processor and Floating Point Math Co-processor perform math-intensive operations.
Interrupt Handler	Processes interrupts for the MPU. The Interrupt Handler sets the interrupt priority level and returns an interrupt acknowledge to the circuit that generated the interrupt. If the MFP controller causes an interrupt, the MPU reads a status byte from the MFP controller to determine the circuit that caused the interrupt.
Data Transfer Handler	Synchronizes data transfers in the analyzer with the MPU. When a data transfer occurs, the Data Transfer Handler notifies the MPU when the transfer is complete.
Clock Circuits	Provide the clocks for the CPU assembly and the A8 Memory assembly.



A7 CPU Block Diagram

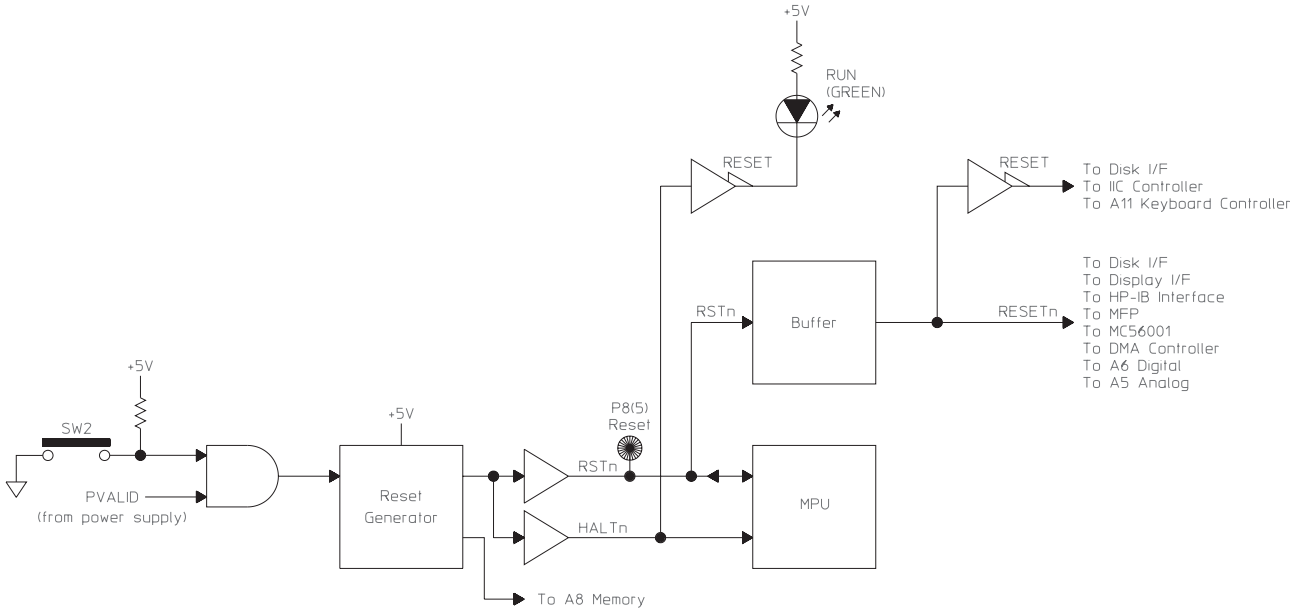


A7 CPU Block Diagram: Interface

Reset Logic

Puts the analyzer into a known state. A reset occurs at power-up and power-down (PVALID from the A98 Power Supply assembly goes high), when the reset switch S2 (located on the CPU assembly) is pressed, or when a RESET instruction is executed.

PVALID from the power supply goes high when +5 volts reaches a valid level. The Reset Generator produces a 128 ms reset pulse when PVALID goes high and S2 is open, or when S2 is closed then opened and PVALID is high. At the end of the reset pulse, RSTn goes high, which terminates the reset and allows all circuits to begin operation.



Reset Logic

Fast Bus Interface

Connects the CPU assembly to the fast bus. All data transfers between the A6 Digital assembly and the CPU assembly occur over the fast bus. The fast-bus address lines (FA0 through FA5) and data lines (FD0 through FD15) are simply extensions of the processor address and data busses. This allows fast transfers between the two assemblies. See ''A99 Motherboard'' in chapter 9 for a description of the fast bus signals.

MFP (Multiple-Function Peripheral) Controller

Handles interrupts and handshaking during data transfers for the IIC Controller, Disk Controller, Display Controller, and RS-232 Interface.

Interrupts from these circuits are sent to the MFP Controller. When the MFP Controller receives an interrupt, it interrupts the prioritized Interrupt Handler, which in turn interrupts the MPU. The MPU then reads a status byte from the MFP Controller to determine the cause of the interrupt. The MFP Controller also tells the Data Transfer Handler if any data transfers occurred for these circuits.

IIC (Inter-IC) Controller

Manages the IIC bus. It allows direct communication between the CPU assembly and the following assemblies via the IIC bus:

- A1 or A2 Input
- A5 Analog
- A8 Memory (calendar/clock chip)
- A10 Rear Panel (tachometer control)
- A11 Keyboard Controller

All of these assemblies appear as slaves to the IIC Controller. The IIC Controller has access to EEPROM, which allows the CPU assembly to store information such as the analyzer's serial number. If the CPU assembly is replaced, the EEPROM integrated circuit (U27) on the faulty assembly must be removed and inserted into the new assembly (see ''What to do before replacing the CPU assembly'' in chapter 6). The IIC Controller also has access to a battery backed real-time clock on the A8 Memory assembly.

The IIC bus consists of the following four signal lines:

- SCL (serial clock)
- SDA (serial data)
- SINTn (serial interrupt)
- SINTFPn (serial interrupt for A11 Keyboard Controller assembly)

Pull-up resistors connect these signals to logic high (all four lines are open collector or open drain). See ''A8 Memory,'' ''A11 Keyboard Controller,'' and ''A99 Motherboard'' in chapter 9 for descriptions of the IIC signals.

Disk Controller Allows the analyzer to store or retrieve data from the internal 3.5-inch flexible A100 Disk Drive assembly. It provides all the control signals necessary to operate the Disk Drive assembly. The Disk Controller performs the following functions:

- Turns on the disk drive motor
- Selects the disk drive head
- Turns on the disk drive LED
- Selects a track on the flexible disk
- Writes or reads serial data to or from the flexible disk

The Disk Controller puts data on the flexible disk in a bit stream that consists of data and clock bits. When data is read from the disk, this circuit separates the data bits from the clock bits, converts the serial data bits to an 8-bit parallel word, and puts the data word on the processor data bus. The operation is reversed when data is written to the disk.

Display Controller Takes parallel data from the processor data bus and places the data in Frame Memory.

Frame Memory Consists of four 256K ⎫4-bit RAM chips. One bit in Frame Memory corresponds to one pixel on the display. The data in Frame Memory is then sent to the Video Gate Array.

Video Gate Array Continuously updates the display with the contents of Frame Memory. The Video Gate Array also supplies the horizontal and vertical sync signals for the display.

RS-232 Interface Allows the analyzer to communicate with other devices such as terminals, plotters, or printers via Instrument Basic. See *Using Instrument Basic with the Agilent 35670A* for additional information.

A8 Memory

The A8 Memory assembly provides the A7 CPU assembly with ROM, dynamic RAM (DRAM), static RAM (SRAM), and a real-time clock.

Memory Controller

Provides the interface between the A7 CPU assembly and the Memory assembly for data transfer.

FLASH ROM, DRAM, and SRAM

Stores data in 32-bit words. To access a memory location, the A7 CPU assembly puts the address of the desired 32-bit word on the processor address bus. The following user-accessible states are stored in SRAM. These states are unchanged by power-up or preset.

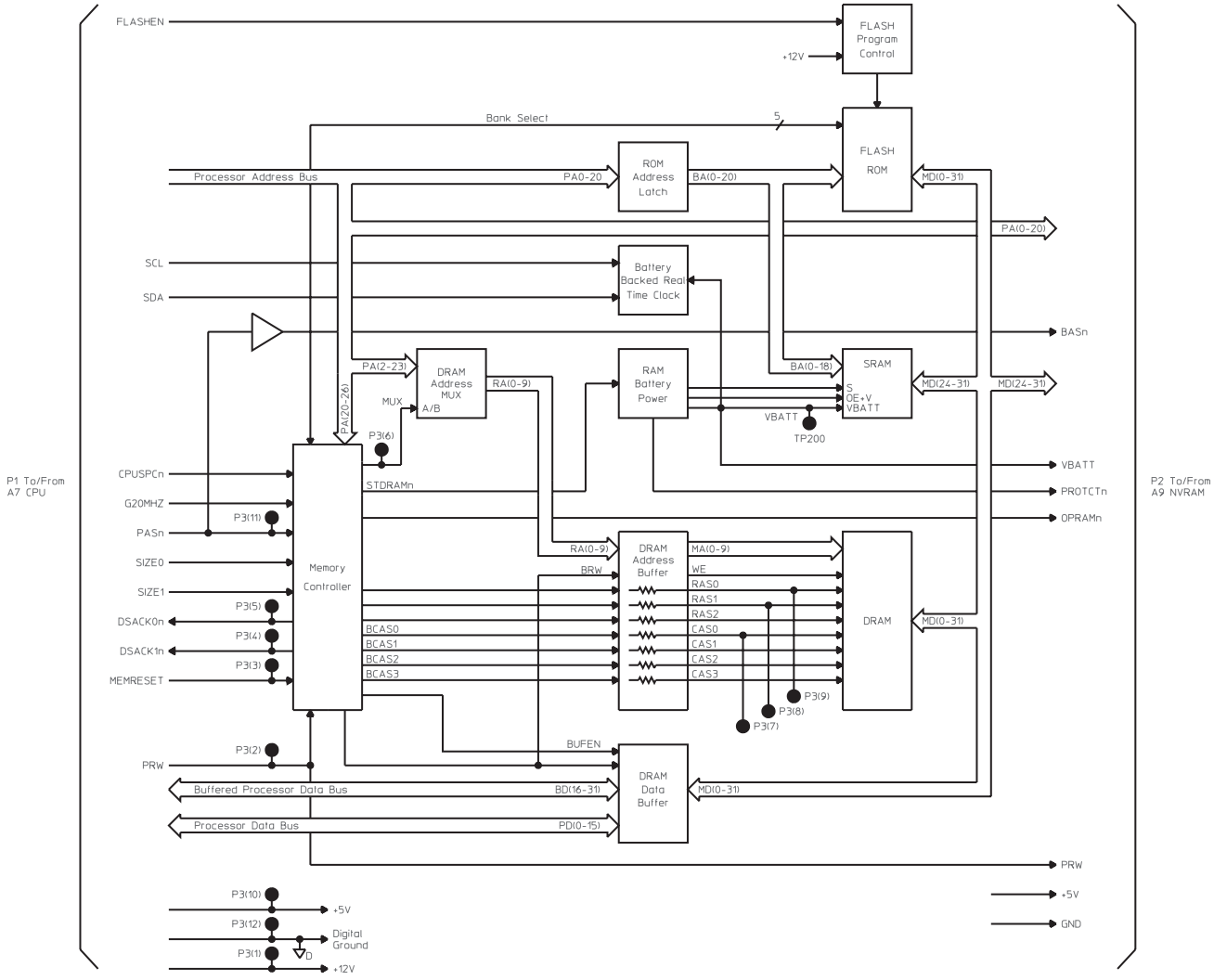
[**Local/Gpib**]
[SYSTEM CONTOLLR]
[ADDRESSBL ONLY]
[ANALYZER ADDRESS]
[PLOTTER ADDRESS]
[PRINTER ADDRESS]
[DISK ADDRESS]
[DISK UNIT]

[**System Utility**]
[CLOCK SETUP]
[TIME HHMM]
[DATE MMDDYY]
[TIMESTAMP SETUP]
[KEYBOARD SETUP]

[**Plot/Print**]
[PLOT/PRNT DEVICE]
[PLOT/PRNT DESTINATN]
[SETUP]
[PLOT LINE SETUP]
[MORE SETUP]
[PLOT PEN SPEED]
[P1 P2 SETUP]
[TIME STMP ON OFF]
[PAGE EJCT ON OFF]
[SERIAL SETUP]

[**Disk Utility**]
[FORMAT DISK]
[DISK TYPE LIF DOS]
[DEFAULT DISK]
[NON-VOL RAM DISK]
[VOLATILE RAM DISK]
[INTERNAL DISK]
[EXTERNAL DISK]

ROM Address Latch,DRAM Address MUX and Buffer	Buffer the processor address bus.
DRAM Data Buffer	Buffers the data on the Processor Data Bus and the Buffered Processor Data Bus.
FLASH Program Control	Allows the FLASH ROM to be reprogrammed.
RAM Battery Power	Provides battery backup for SRAM and the Battery Backed Real Time Clock.
Battery Backed Real Time Clock	Keeps track of the current time and date.



A8 Memory Block Diagram

A9 NVRAM

The optional A9 NVRAM assembly provides the A7 CPU assembly with additional nonvolatile RAM.

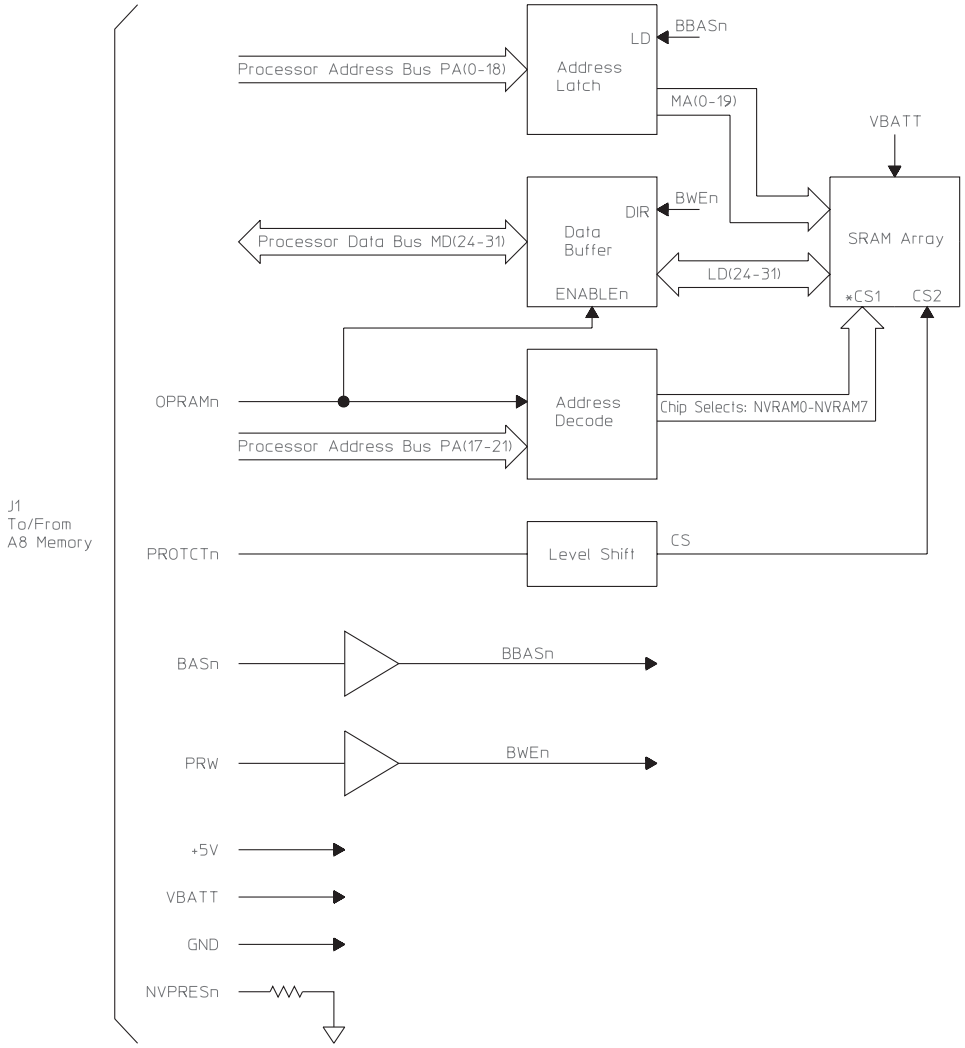
Address Latch — Holds the address from the processor address bus. This circuit latches the address when an address strobe occurs (BBASn goes low).

Data Buffer — Buffers the processor data bus.

Address Decode — Enables one of the eight battery-backed static RAM chips in the SRAM Array.

Level Shift — Disables the SRAM Array during power-up and power down, when the A7 CPU assembly's processor is externally reset, and when +5 volts on the A8 Memory assembly is too low.

SRAM Array — Contains eight battery-backed static RAM chips.

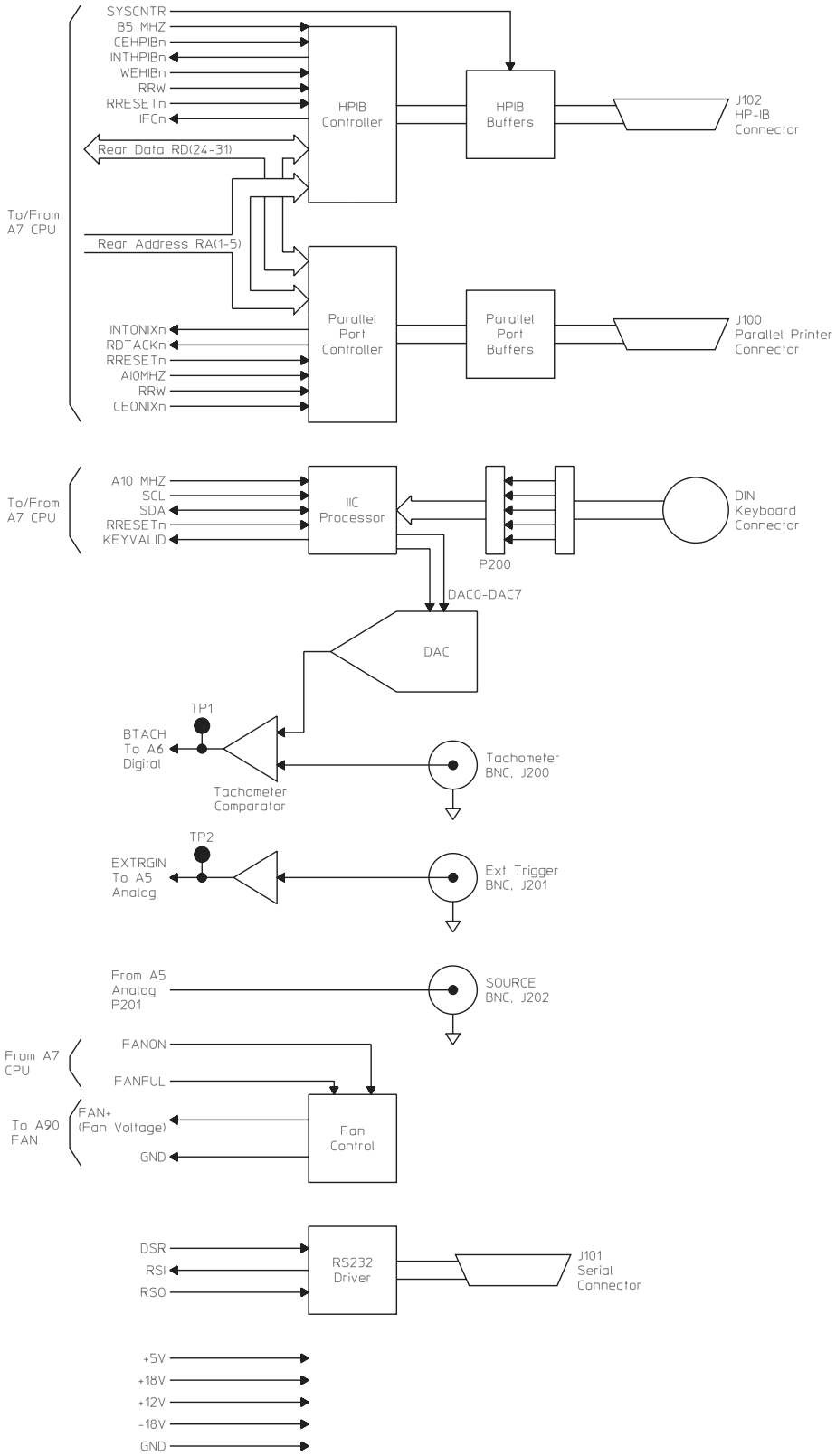


A9 NVRAM Block Diagram

A10 Rear Panel

The A10 Rear Panel assembly contains the BNC connectors for the external trigger input, tachometer input, and source output. The Rear Panel assembly also contains DIN, GPIB, serial, and parallel interface connectors. In addition, the Rear Panel assembly provides the fan control for the A90 Fan assembly.

GPIB Controller and *Buffers*	Allow the analyzer to communicate with devices such as plotters, printers, or a host computer via an GPIB cable. These circuits handle all GPIB functions for the analyzer.
Parallel Port Controller and Buffers	Allow the analyzer to send data to printers with Centronics interfaces.
IIC Processor	Provides the interface from the DIN keyboard connector to the A7 CPU assembly. The IIC Interface also decodes the control lines for the DAC.
DAC	Sets the tachometer trigger level. The A7 CPU assembly sends the control signals to the Rear Panel assembly over the IIC bus. The IIC Processor decodes the control signals.
Tachometer Comparator	Compares the input signal from the Tachometer BNC connector with the trigger level set by the DAC. The output of the comparator changes TTL levels when the input signal crosses the trigger level.
External Trigger Buffer	Buffers the external trigger signal.
Fan Control	Provides the A90 Fan assembly with a voltage that controls the fan speed. A temperature sensor provides a control signal that changes with the analyzer's internal temperature. When the temperature increases, Fan Control increases the fan speed. When the temperature decreases, Fan Control decreases the fan speed. Control lines from the A7 CPU assembly can also set the fan speed to high or turn the fan off.
Serial Driver	Drives the serial data lines to and from devices connected to the Serial Port. The serial port is only available using Instrument Basic.



A10 Rear Panel Block Diagram

A11 Keyboard Controller

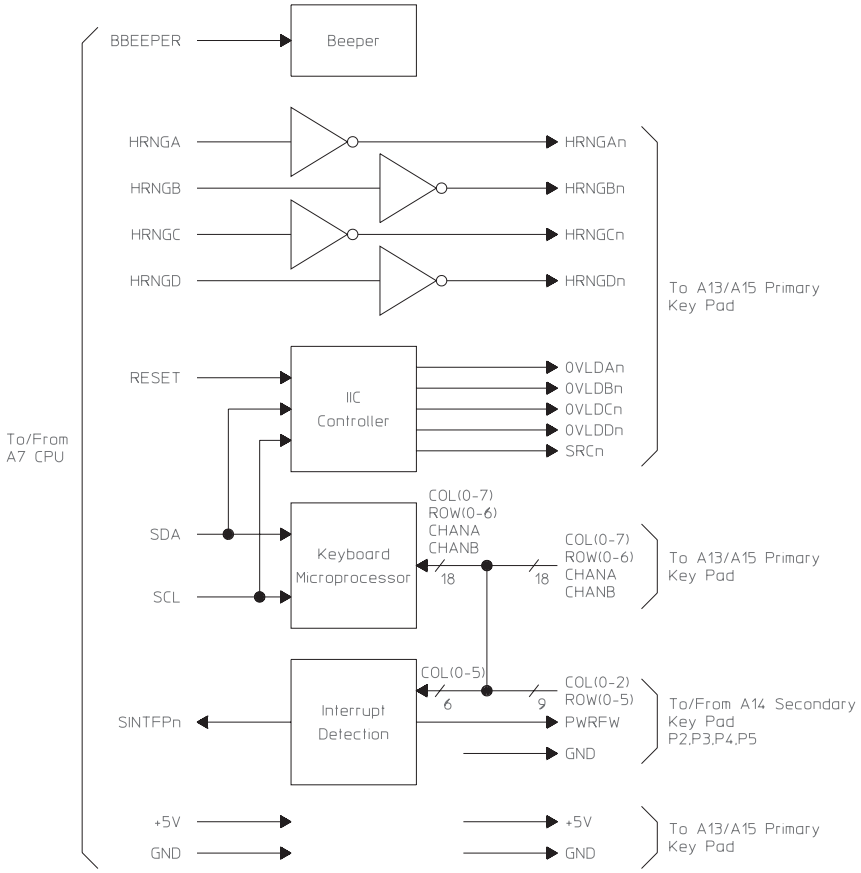
The A11 Keyboard Controller assembly together with the A13 Primary and A14 Secondary Keypad assemblies make up the front panel keyboard. This assembly provides the interface between the A7 CPU assembly and the keypads.

Beeper Generates a tone when instructed by the A7 CPU assembly. The beeper can be turned off by pressing [**System Utility**] [BEEPER ON **OFF**].

IIC Controller Decodes data from the IIC bus providing the A13 Primary Keypad assembly with control lines that turn overload and source LEDs on and off.

Keyboard Microprocessor Interrupts the A7 CPU assembly when a key is pressed or the RPG is turned. The CPU assembly then addresses the Keyboard Microprocessor and reads an 8-bit frame of data from the IIC bus to determine which key was pressed (for information about the IIC bus, see the description of the IIC Controller in the ''A7 CPU'' earlier in this chapter).

Interrupt Detection Informs the A7 CPU assembly every time a key is pressed or the RPG is turned.



A11 Keyboard Controller Block Diagram

A12 BNC

The A12 BNC assembly connects the BNC connectors on the two channel analyzer's front panel to their respective assembly. The Source BNC is connected to the A5 Analog assembly and the Channel 1 and Channel 2 BNCs are connected to the A1 Input assembly. In addition, this assembly provides RFI filtering for the Channel 1 and Channel 2 HIGH and LOW inputs.

A13 Primary Keypad

The A13 Primary Keypad assembly contains the marker, display, numeric, and measurement keys for the two channel analyzer. The Primary Keypad assembly also contains the RPG and the LEDs that indicate a half range or overload condition on a channel. See ‘’A11 Keyboard Controller’’ for additional information.

A14 Secondary Keypad

The A14 Secondary Keypad assembly contains the system keys and the softkeys. See ‘’A11 Keyboard Controller’’ for additional information.

A15 Primary Keypad

The A15 Primary Keypad assembly contains the marker, display, numeric, and measurement keys for the four channel analyzer. The Primary Keypad assembly also contains the RPG and the LEDs that indicate a half range or overload condition on a channel. See ‘’A11 Keyboard Controller’’ for additional information.

A22 BNC

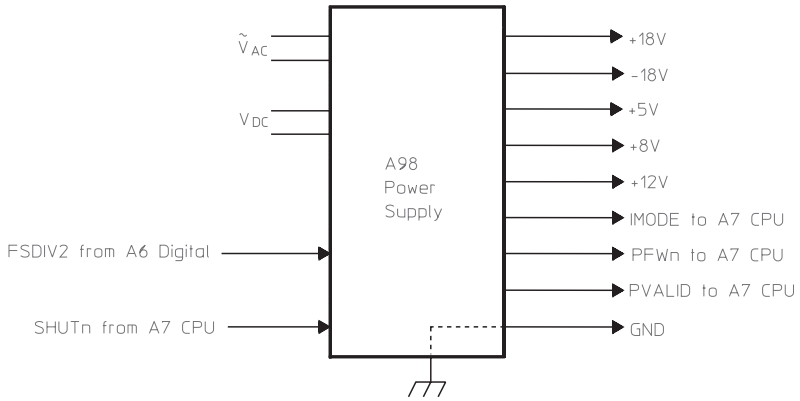
The A22 BNC assembly connects the BNC connectors on the four channel analyzer’s front panel to their respective assembly. The Channel 1 and Channel 3 BNCs are connected to the A2 Input assembly connected to A99 J1. The Channel 2 and Channel 4 BNCs are connected to the A2 Input assembly connected to A99 J2. In addition, this assembly provides RFI filtering for the HIGH and LOW inputs.

A90 Fan

The A90 Fan assembly cools the analyzer. The A10 Rear Panel assembly controls the speed of the Fan assembly. As the temperature increases, the Rear Panel assembly increases the fan speed. As the temperature decreases, the Rear Panel assembly decreases the fan speed. The fan can also be turned off or set to full speed by pressing [**System Utility**] [FAN SETUP] [FAN OFF] or [FULL SPEED].

A98 Power Supply

The A98 Power Supply assembly is a switching power supply that provides the voltages for all the assemblies in the analyzer. The Power Supply can operate on ac line power or on a dc battery pack. See ''Power Supply Voltage Distribution'' in chapter 9 for a list of the voltages and the assemblies that use each voltage.



A98 Power Supply Block Diagram

A99 Motherboard

The A99 Motherboard assembly provides a common point of contact for voltage and signal distribution. The Motherboard also buffers the external monitor signals and routes the buffered signals to the EXT MONITOR connector. See ''A99 Motherboard'' in chapter 9 for a list of all signals that are distributed via the Motherboard assembly.

A100 Disk Drive

The internal A100 Disk Drive assembly stores and retrieves information from 3.5-inch flexible disks. This assembly is controlled by the A7 CPU assembly. See the description of the Disk Controller in ''A7 CPU'' (earlier in this chapter) for additional information.

A101 Display

The A101 Display assembly shows processed data sent by the A7 CPU assembly. See the description of the Display Controller for the ''A7 CPU'' (earlier in this chapter) for further details.

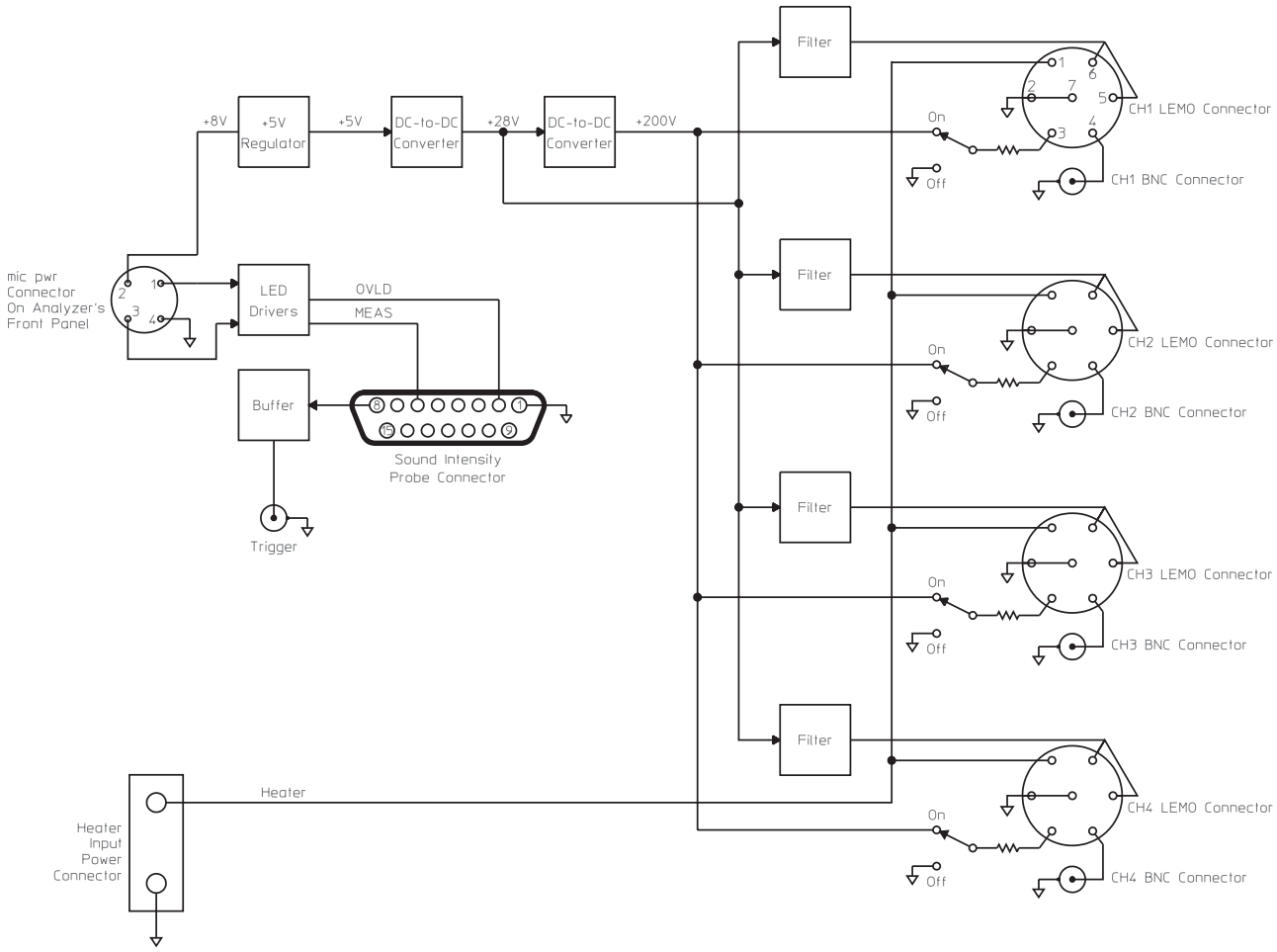
A102 DC-DC Converter

The A102 DC-DC Converter assembly generates the driver supply voltages for the A101 Display assembly and routes the display data from the A7 CPU assembly to the Display assembly.

Option UK4 Microphone Adapter and Power Supply

The optional Microphone Adapter and Power Supply provides four LEMO connectors with power for microphones. The input signal from each LEMO connector is routed to a BNC connector. BNC cables then connect the input signals to the analyzer's input channels.

+5 V Regulator	Regulates +8 V to +5 V.
DC-to-DC Converter	Converts +5 V to +28 V. The second DC-to-DC Converter converts +28 V to +200 V.
Filter	Filters +28 V providing the microphone preamplifier voltage to pins 5 and 6 of each LEMO connector.
On Off	Connects a 200 V polarization voltage or ground to pin 3 of each LEMO connector.
Heater Input Power	Allows an externally supplied heater voltage to be connected to pin 1 of each LEMO connector.
LED Drivers	Provides control lines for the overload and measurement LEDs on the HP 35230A Sound Intensity Probe.
Buffer	Buffers the trigger signal from the HP 35230A Sound Intensity Probe. A BNC cable connects the trigger signal to the analyzer's rear panel.
Sound Intensity Probe Connector	Provides the interface to the HP 35230A Sound Intensity Probe.



Option UK4 Microphone Adapter and Power Supply Block Diagram

9

Voltages and Signals

Voltages and Signals

This chapter shows where the signals and voltages are used in the analyzer and describes each signal. The signals are described in groups as shown in the following table.

Section Title	Describes signals routed ...
A1 Input	through SMB cables from A1 Input to A5 Analog
A2 Input	through SMB cables from A2 Input to A5 Analog
A8 Memory	between A8 Memory and A7 CPU
A9 NVRAM	between A9 NVRAM and A8 Memory
A10 Rear Panel	between A10 Rear Panel and external connectors
A11 Keyboard Controller	between A11 Keyboard Controller and A7 CPU
A12 BNC	through A12 BNC
A13 Primary Keypad	between A13 Primary Keypad and A11 Keyboard Controller
A14 Secondary Keypad	between A14 Secondary Keypad and A11 Keyboard Controller
A22 BNC	through A22 BNC
A99 Motherboard	through A99 Motherboard
A100 Disk Drive	between A100 Disk Drive and A7 CPU
A101 Display	between A101 Display and A7 CPU
A102 DC-DC Converter	between A102 DC-DC Converter and A101 Display

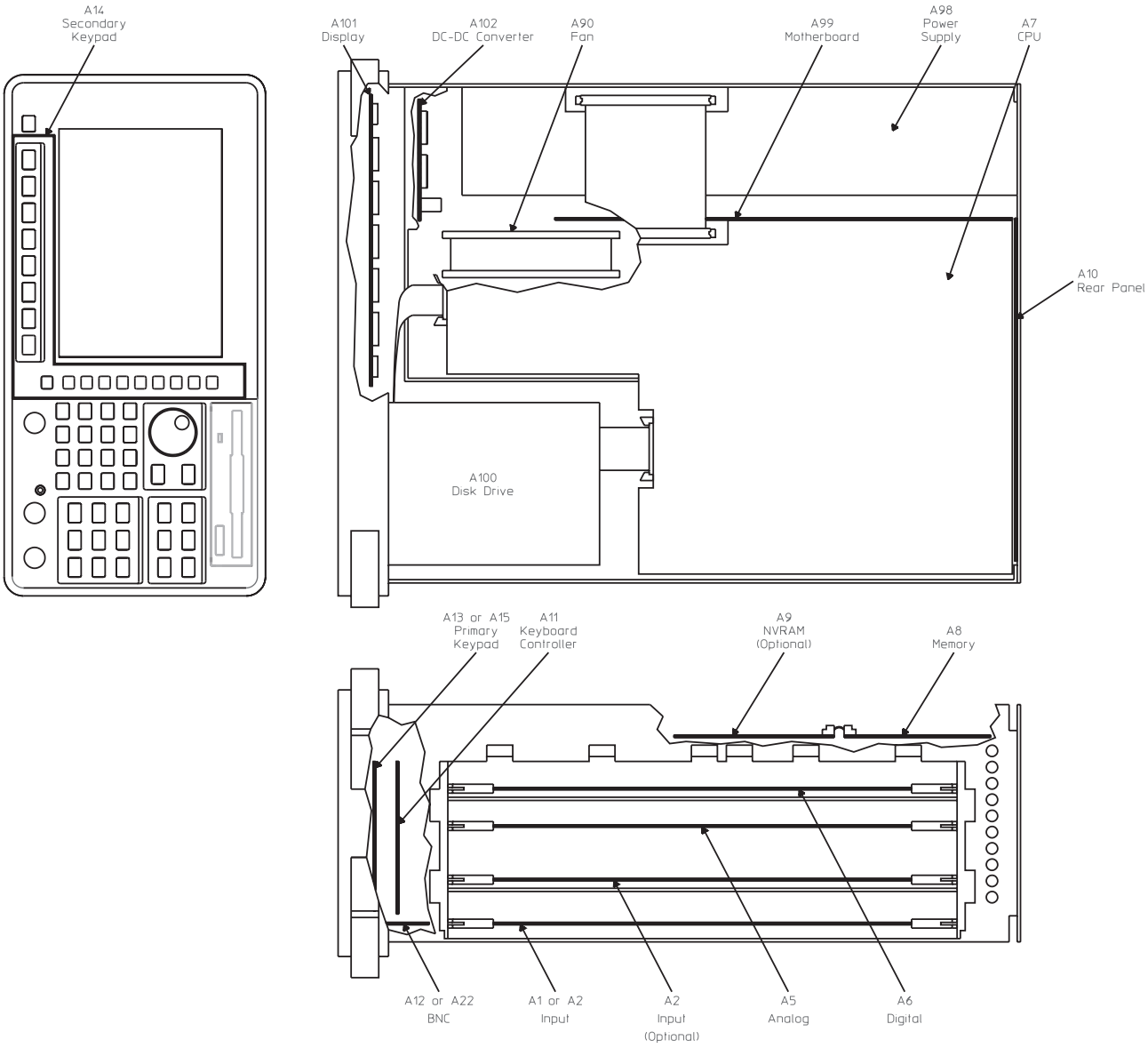
Note

Signals with a mnemonic that end with a lower case ‘’n’’ are active low.

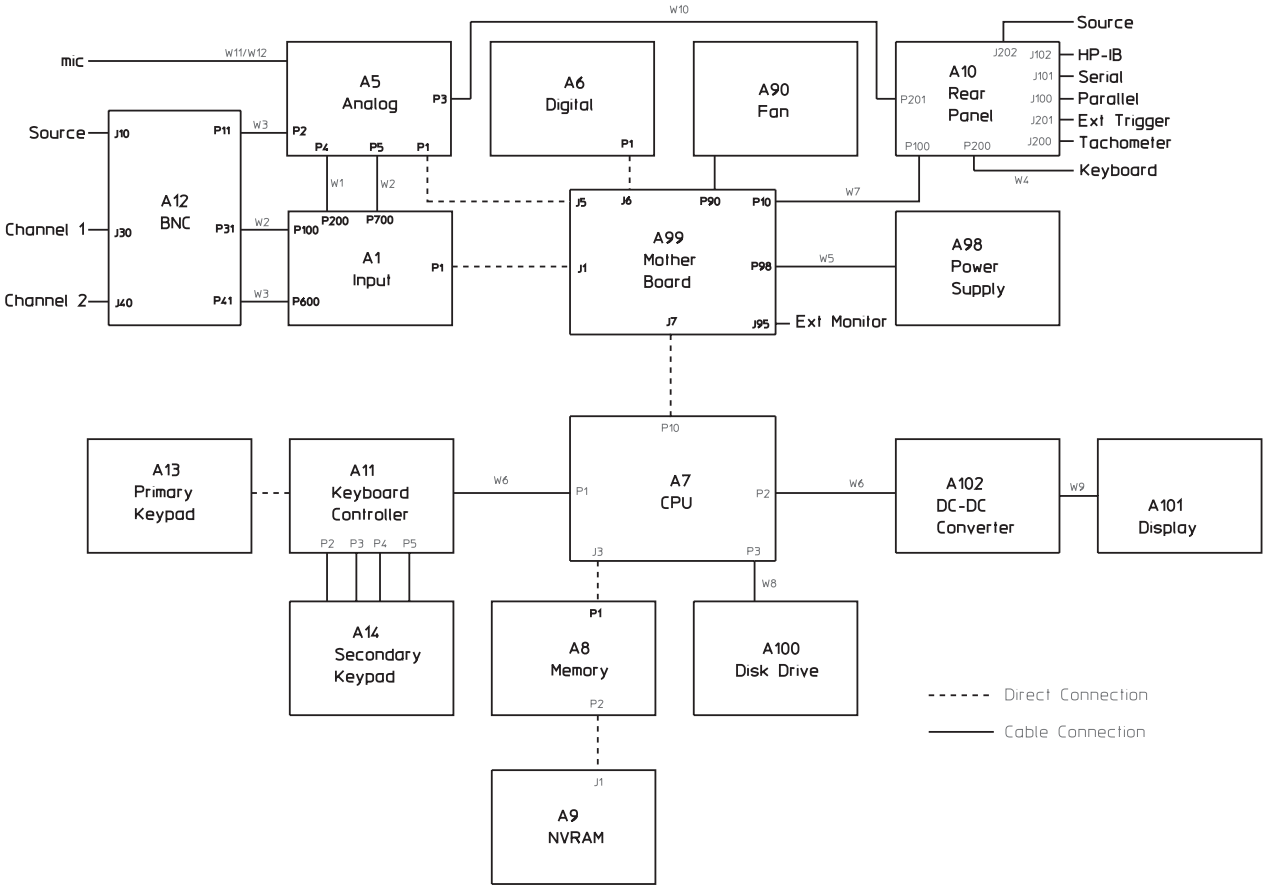
Signal levels listed as low or high are TTL levels unless stated otherwise.

Measurements given in dBm are terminated in 50 ohms unless stated otherwise.

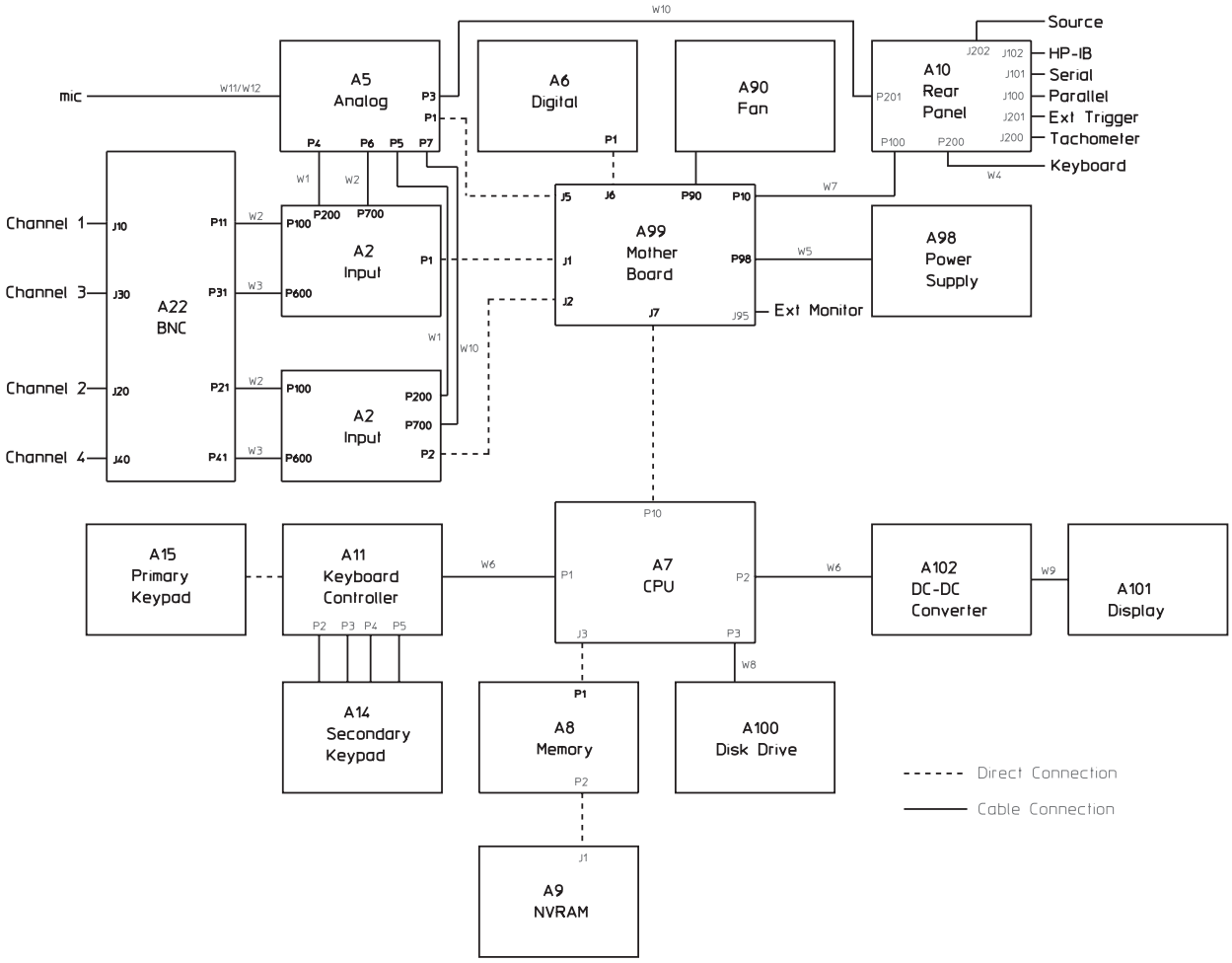
Assembly Locations and Connections



Assembly Locations



Assembly Connections for Two Channel Analyzer



Assembly Connections for Four Channel Analyzer

Power Supply Voltage Distribution

The following table shows the power supply voltages used by each assembly in the analyzer. In addition, the table also shows the path taken by these voltages. Some assemblies use the power supply voltages as supplied by the Power Supply assembly. However, most assemblies contain voltage regulation and voltage decoupling circuits to provide additional regulation and decoupling for their own use.

From	Path	To	Voltages					
			+18 V	–18 V	+12 V	+8 V	+5 V	Gnd
Pwr Supply	W5	A99	•	•	•	•	•	•
	W5/A99	A1/A2	•	•		•		•
	W5/A99	A5	•	•		•	•	•
	W5/A99	A6					•	•
	W5/A99/W7	A10	•	•	•		•	•
	W5/A99	A90					•	•
	W5/A99	A7		•	•		•	•
	W5/A99/A7	A8			•		•	•
	W5/A99/A7/A8	A9					•	•
	W5/A99/A7/W6	A11					•	•
	W5/A99/A7/W6/A11	A13					•	•
	W5/A99/A7/W6/A11	A14						•
	W5/A99/A7/W8	A100					•	•
	W5/A99/A7/W6	A101			•		•	•
	W5/A99/A7/W6	A102			•		•	•

A1 Input

Analyzers with only two channels contain one A1 Input assembly. The A1 Input assembly conditions both input signals. After the signals are conditioned by the Input assembly they are routed through SMB cables to the A5 Analog assembly. The signal from A1 P200 to A5 P4 is C1AAFO (Channel 1 Anti-Alias Filter Out). The signal from A1 P700 to A5 P5 is C2AAFO (Channel 2 Anti-Alias Filter Out). The amplitude of C1AAFO or C2AAFO is 1 Vrms with the analyzer set to the 1 dBVrms range and a 1.122 Vrms signal connected to the channel's input connector.

A2 Input

Analyzers with the four channel option contain two A2 Input assemblies. The A2 Input assemblies condition all four input signals. After the signals are conditioned by the Input assemblies they are routed through SMB cables to the A5 Analog assembly. For the Input assembly connected to A99 J1, the signal from A2 P200 to A5 P4 is C1AAFO (Channel 1 Anti-Alias Filter Out) and the signal from A2 P700 to A5 P6 is C3AAFO (Channel 3 Anti-Alias Filter Out). For the Input assembly connected to A99 J2, the signal from A2 P200 to A5 P5 is C2AAFO (Channel 2 Anti-Alias Filter Out) and the signal from A2 P700 to A5 P7 is C4AAFO (Channel 4 Anti-Alias Filter Out). The amplitude of C1AAFO, C2AAFO, C3AAFO, or C4AAFO is 1 Vrms with the analyzer set to the 1 dBVrms range and a 1.122 Vrms signal connected to the channel's input connector.

A8 Memory

The following table lists signals routed between the A8 Memory assembly and the A7 CPU assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	A7 J3 Pin(s)	A8 P1 Pin(s)	A7 J3	A8 P1
BD16	25C	C8	⇔	⇔
BD17	25B	B8	⇔	⇔
BD18	26C	C7	⇔	⇔
BD19	26B	B7	⇔	⇔
BD20	26A	A7	⇔	⇔
BD21	27C	C6	⇔	⇔
BD22	27B	B6	⇔	⇔
BD23	27A	A6	⇔	⇔
BD24	28C	C5	⇔	⇔
BD25	28B	B5	⇔	⇔
BD26	28A	A5	⇔	⇔
BD27	29C	C4	⇔	⇔
BD28	29B	B4	⇔	⇔
BD29	29A	A4	⇔	⇔
BD30	30C	C3	⇔	⇔
BD31	30B	B3	⇔	⇔
CPUSPCn	17A	A16	S	•
DSACK0n	3A	A30	•	S
DSACK1n	4A	A29	•	S
FLASHEN	19A	A14	S	•
G20MHZ	32C	C1	S	•
MEMRESET	20A	A13	S	•
PA0	1C	C32	S	•
PA1	1B	B32	S	•
PA2	2C	C31	S	•
PA3	2B	B31	S	•
PA4	3C	C30	S	•
PA5	3B	B30	S	•
PA6	4C	C29	S	•

S This assembly is the source of the signal.

• This assembly uses the signal.

⇔ This signal is bidirectional.

Signal Name	A7 J3 Pin(s)	A8 P1 Pin(s)	A7 J3	A8 P1
PA7	4Bjio	B29	S	•
PA8	5C	C28	S	•
PA9	5B	B28	S	•
PA10	6C	C27	S	•
PA11	6B	B27	S	•
PA12	8C	C25	S	•
PA13	8B	B25	S	•
PA14	9C	C24	S	•
PA15	9B	B24	S	•
PA16	10C	C23	S	•
PA17	10B	B23	S	•
PA18	11C	C22	S	•
PA19	11B	B22	S	•
PA20	12C	C21	S	•
PA21	12B	B21	S	•
PA22	13C	C20	S	•
PA23	13B	B20	S	•
PA24	11A	A22	S	•
PA25	18A	A15	S	•
PA26	31B	B2	S	•
PASn	16A	A17	S	•
PD0	16C	C17	⇔	⇔
PD1	16B	B17	⇔	⇔
PD2		C16	⇔	⇔
PD3	17B	B16	⇔	⇔
PD4	18C	C15	⇔	⇔
PD5	18B	B15	⇔	⇔
PD6	19C	C14	⇔	⇔
PD7	19B	B14	⇔	⇔
PD8	20C	C13	⇔	⇔
PD9	20B	B13	⇔	⇔
PD10	21C	C12	⇔	⇔
PD11	21B	B12	⇔	⇔
PD12	22C	C11	⇔	⇔
PD13	22B	B11	⇔	⇔
PD14	23C	C10	⇔	⇔
PD15	23B	B10	⇔	⇔
PRW	9A	A24	S	•
SCL	22A	A11	S	•
SDA	23A	A10	⇔	⇔
SIZE0	12A	A21	S	•
SIZE1	13A	A20	S	•
+5	5A, 6A, 10A, 15A, 15B, 15C	A18, B18, C18, A23, A27, A28	•	•
+12	31A, 32A	A1, A2	•	•

Gnd	1A, 2A, 7A, 7B, 7C, 8A, 14A, 14B, 14C, 21A, 24A, 24B, 24C, 25A, 30A, 31C	C2, A3, A8, A9, B9, C9, A12, A19, B19, C19, A25, A26, B26, C26, A31, A32	•	•
Not Used	32B	B1	—	—

S This assembly is the source of the signal.

• This assembly uses the signal

⇔ This signal is bidirectional.

— This assembly *does not* use this signal.

BD16 —31 Buffered Data Bus — This is the buffered processor data bus from the A7 CPU assembly. This bus is further buffered on the A8 Memory assembly.

CPUSPCn CPU Space — This line goes low when the CPU space transfer occurs. When this line is low the A8 Memory assembly does not respond.

DSACK0n — DSACK1n Data Strobe Acknowledge — During a write cycle, DSACK0n goes low after the A8 Memory assembly places valid data on the data bus. During a read cycle, DSACK0n goes low after the Memory assembly reads the data. When DSACK0n goes low and DSACK1n is low, 32 bits of data are valid on PD0-15 and BD16-31. When DSACK0n goes low and DSACK1n is high, 8 bits of data are valid on BD24-31.

FLASHEN Flash Enable — This line is high only when the FLASH memory on the A8 Memory assembly is being programmed. This line enables +12 V to the FLASH memory programming pin.

G20MHZ 20 MHz Clock — This is a 50% duty cycle, 20 MHz clock. This clock provides the timing for the A8 Memory assembly.

MEMRESET Memory Reset — A high on this line resets the digital logic on the A8 Memory assembly. This line pulses high during power-up and power-down, and when the A7 CPU assembly's microprocessor executes the RESET instruction or is externally reset.

PA0 — PA26 Processor Address Bus — This is the processor address bus from the A7 CPU assembly. This bus is buffered on the A8 Memory assembly. PA0 and PA1 also operate with SIZE0 and SIZE1 to specify the alignment of the operand.

PASn Processor Address Strobe — A low on this line starts a memory access cycle. This line pulses low when a valid address is on the processor address bus (PA1 — PA23).

PD0 — 15 Processor Data Bus — This is the processor data bus from the A7 CPU assembly.

PRW Processor Read/Write — This line is high when the current memory cycle is a read and low when the current memory cycle is a write.

SCL Serial Clock — This is the serial clock for the IIC bus. The IIC controller on the A7 CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.

SDA Serial Data — This is the IIC bus bidirectional data line. This line transmits real-time clock data between the A7 CPU assembly and the A8 Memory assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.

SIZE0 — SIZE1	Data Size — These lines determine the size of the operand. When SIZE0 is high and SIZE1 is low, the operand size is 8 bits. When SIZE0 is low and SIZE1 is high, the operand size is 16 bits. When both SIZE0 and SIZE1 are high, the operand size is 24 bits. When both SIZE0 and SIZE1 are low, the operand size is 32 bits.

A9 NVRAM

The following table lists signals routed between the optional A9 NVRAM assembly and the A8 Memory assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A8 P2	A9 J1
BASn	A6	•	•
MD24	B4	⇔	⇔
MD25	C4	⇔	⇔
MD26	B3	⇔	⇔
MD27	C3	⇔	⇔
MD28	B2	⇔	⇔
MD29	C2	⇔	⇔
MD30	B1	⇔	⇔
MD31	C1	⇔	⇔
NVPRESn	A16	—	S
OPRAMn	A2	S	•
PA0	C6	S	•
PA1	B6	S	•
PA2	C7	S	•
PA3	B7	S	•
PA4	C8	S	•
PA5	B8	S	•
PA6	C9	S	•
PA7	B9	S	•
PA8	C10	S	•
PA9	B10	S	•
PA10	C12	S	•
PA11	B12	S	•
PA12	C13	S	•
PA13	B13	S	•
PA14	C14	S	•
PA15	B14	S	•
PA16	C15	S	•
PA17	B15	S	•

S This assembly is the source of the signal.

• This assembly uses the signal.

⇔ This signal is bidirectional.

— This assembly *does not* use this signal.

Signal Name	Pin(s)	A8 P2	A9 J1
PROTCTn	A9	S	•
PA18	C16	S	•
PA19	A4	S	•
PA20	A12	S	•
PA21	B16	S	•
PRW	A3	•	•
VBATT	A13, A14, A15	S	•
+5	A10, A11, B11, C11	•	•
Gnd	A1, A5, B5, C5, A7, A8	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.
⇔ This signal is bidirectional.
— This assembly *does not* use this signal.

BASn — Buffered Address Strobe — This line pulses low when a valid address is on the processor address bus (PA0 — PA21).

MD24 — MD31 — Memory Data Bus — This is the buffered processor data bus from the A7 CPU assembly. This bus is further buffered on the A8 Memory assembly.

NVPRESn — NRAM Present — A low on this line indicates that the A9 NVRAM assembly is connected to the A8 Memory assembly. This line is checked only during manual troubleshooting procedures.

OPRAMn — Optional RAM — A low on this line enables the battery-backed static RAM on the A9 NVRAM assembly.

PA0 — PA21 — Processor Address Bus — This is the processor address bus from the A7 CPU assembly. This bus is buffered on the A8 Memory assembly.

PROTCTn — Protect — A low on this line disables the battery-backed static RAM on the A9 NVRAM assembly. This line pulses low during power-up and power-down, when the A7 CPU assembly's microprocessor is externally reset, and when +5 volts on the A8 Memory assembly is too low.

PRW — Processor Read/Write — This line is high when the current memory cycle is a read and low when the current memory cycle is a write.

VBATT — Battery Voltage — This line provides the power to the battery-backed static RAM on the A9 NVRAM assembly. When the analyzer is on, the +5 volts on the A8 Memory assembly provides the power for this line. When the analyzer is off, the battery on the Memory assembly provides the power for this line. Since power is applied to the static RAM even when the analyzer is off, the static RAM is non-volatile.

A10 Rear Panel

This section describes the signals at the A10 Rear Panel assembly's interface connectors and input connectors. The signals are described in the following order:
GPIB
Serial Port
Parallel Port
DIN Keyboard
Source Output
Tachometer Input
External Trigger Input

GPIB

The following table lists signals at the GPIB connector (A10 J102). A general description of each signal follows the table. For a detailed description of how the analyzer interprets the GPIB lines, see the *Agilent 35670A GPIB Command Reference*.

Signal Name	Pin
ATN	11
DAVn	6
DIO1	1
DIO2	2
DIO3	3
DIO4	4
DIO5	13
DIO6	14
DIO7	15
DIO8	16
EOIn	5
IFCn	9
NDACn	8
NRFDn	7
RENn	17
SRQn	10
Shield	12
GND	18 – 24

ATN — Attention — This line is controlled by the controller in charge. When this line is low, the DIO lines contain interface commands. When this line is high, the DIO lines contain data.

DAVn — Data Valid — This line goes low when valid data is on the bus and NRFDn is high. This line is controlled by the GPIB controller.

DIO1 — DIO8 — Data Input/Output — These are inverted data lines that conform to IEEE specification IEEE-488. When ATN is low, these lines contain interface commands. When ATN is high, these lines contain data.

EOIn — End or Identify — If ATN is high, a low on this line marks the end of a message block. If ATN is low, a low on this line requests a parallel poll.

IFCn — Interface Clear — This line goes low to halt all current operations on the bus, unaddress all other devices, and disable serial poll. The system controller becomes the controller in charge. This line is only used during the analyzer's developement.

NDACn — Not Data Accepted — This line goes high when the DIO lines have been latched by the acceptor.

NRFDn — Not Ready for Data — This line goes high when the acceptor is ready to accept data.

RENn — Remote Enable — This line is low when the GPIB has control and high during local operation.

SRQn — Service Request — This line is low when a device on the GPIB needs service.

Serial Port

The following table lists signals at the Serial Port connector (A10 J101). The Serial Port is a 9-pin EIA-574 port that is only available using Instrument Basic. A description of each signal follows the table.

Signal Name	Pin
DSR	6
DTR	1
RTS	4
RxD	3
TxD	2
Logic Gnd	7
Not Used	5, 8-9

DSR — Data Set Ready — Some devices check this line for a high to verify that the analyzer is connected and ready. The user can set this line high or set this line to go high only when the analyzer is ready for data transfer.

DTR — Data Terminal Ready — This line is tied high. Some devices check this line for a high to verify that the analyzer is connected and ready.

RTS — Request To Send — This line is tied high. Some devices require this line to be high before transferring data.

RxD — Receive Data — This is the serial EIA-574 receive data line. This line transmits data from peripheral devices one byte at a time.

TxD — Transmit Data — This is the serial EIA-574 transmit data line. This line transmits data to peripheral devices one byte at a time.

Parallel Port

The Parallel Port is a 25-pin, Centronics port. The Parallel Port can interface with printers or plotters. The following table lists signals at the Parallel Port connector (A10 J100). A description of each signal follows the table.

Signal Name	Pin
ACKn	10
BUSY	11
FAULTn	15
IPn	16
PA0	2
PA1	3
PA2	4
PA3	5
PA4	6
PA5	7
PA6	8
PA7	9
PE	12
SELECT	13
STROBEn	1
Logic Gnd	18
Not Used	14, 17, 19 - 25

ACKn — Acknowledge — The printer pulses this line low after it accepts a byte of data and is ready for more data.

BUSY — Busy — The printer sets this line high when it cannot receive data due to data entry, a full buffer, or error status.

FAULTn — Fault — The printer sets this line low if it reaches an error state.

IPn — Input Prime — This line pulses low to reset the printer and clear the print buffer.

PA0 - PA7 — Printer Data Bus —This is the 8-bit parallel data bus. These lines transmit a byte of data to the printer.

PE — Paper Error — The printer sets this line high when it is out of paper.

SELECT — Selected — The printer sets this line high to indicate that it has been selected.

STROBEn — Strobe — This line pulses low when a byte of data is ready. A low pulse on this line clocks the data into the printer.

DIN Keyboard

The following table lists signals at the DIN keyboard connector (A10 P200). A description of each signal follows the table.

Signal Name	Pin
KEYCLK	1
KEYDAT	3
+5 V	4
Logic Gnd	2
Not Used	5

KEYCLK — Key Board Clock — This clock synchronizes the transfer of keyboard data from the external keyboard to the A10 Rear Panel assembly.

KEYDAT — Key Board Data — This is 8-bit serial data from an external keyboard to the A10 Rear Panel assembly .

Source Output

The source output is routed from P3 on the A5 Analog assembly through an SMB cable to P201 on the A10 Rear Panel assembly. The A10 Rear Panel assembly then routes the source signal to the Source BNC connector. In two channel analyzers, the source output is also routed from P2 on the A5 Analog assembly through an SMB cable to P11 on the A12 BNC assembly. The A12 BNC assembly then routes the source signal to the Source BNC connector on the front panel. The source signal can be random noise, burst random noise, periodic chirp, burst chirp, pink noise, or fixed sine. The signal's amplitude range is ±5 Vpk.

Tachometer Input

The A10 Rear Panel assembly converts the signal connected to the Tachometer BNC connector to a TTL representation of the tachometer input (BTACH).

External Trigger Input

The A10 Rear Panel assembly buffers the signal connected to the External Trigger BNC connector. The maximum trigger input level is ±25 Vpk. The minimum trigger pulse width is 600 ns and the maximum trigger pulse rate is 800 kHz.

A11 Keyboard Controller

The following table lists signals routed between the A11 Keyboard Controller assembly and the A7 CPU assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A7 P1	A11
BBEEPER	3	S	•
HRNGA	11	—	•
HRNGB	9	—	•
HRNGC	2	—	•
HRNGD	1	—	•
RESET	5	S	•
SCL	15	S	•
SDA	13	⇔	⇔
SINTFPn	7	•	S
+5 V	10	•	•
Gnd	6, 8, 12, 14, 16	•	•
Not Used	4	—	—

S This assembly is the source of the signal.
• This assembly uses the signal.
⇔ This signal is bidirectional.
— This assembly *does not* use this signal.

BBEEPER — Buffered Beeper — This line controls the frequency of the front panel beeper tone.

HRNGA — Half Range A — In both the two channel and four channel analyzer, a high on this line turns on the channel 1 half range LED. This line goes high when the A1 or A2 Input assembly detects that the amplitude of the channel 1 input signal reached half the set range.

HRNGB — Half Range B — In a two channel analyzer, a high on this line turns on the channel 2 half range LED. In a four channel analyzer, a high on this line turns on the channel 3 half range LED. This line goes high when the A1 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range or when the A2 Input assembly detects that the amplitude of the channel 3 input signal reached half the set range.

HRNGC — Half Range C — In a four channel analyzer, a high on this line turns on the channel 2 half range LED. This line goes high when the A2 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range. This line is only used in four channel analyzers.

HRNGD — Half Range D — In a four channel analyzer, a high on this line turns on the channel 4 half range LED. This line goes high when the A2 Input assembly detects that the amplitude of the channel 4 input signal reached half the set range. This line is only used in four channel analyzers.

RESET — System Reset — A high on this line resets the digital logic on the A11 Keyboard Controller assembly. This line pulses high during power-up and power-down, and when the A7 CPU assembly's microprocessor executes the RESET instruction or is externally reset.

SCL	Serial Clock — This is the serial clock for the keyboard IIC bus. The IIC controller on the A7 CPU assembly generates this clock to synchronize the transfer of data from the A11 Keyboard Controller assembly.
SDA	Serial Data — This is the keyboard IIC bus. When a key is pressed or the RPG is turned, SINTFPn interrupts the A7 CPU assembly and this line transmits data to the A7 CPU assembly in 8-bit frames.
SINTFPn	Serial Interrupt from the Front Panel — A high-to-low transition on this line interrupts the A7 CPU assembly. This line goes low when a key is pressed or when the RPG is turned.

A12 BNC

The A12 BNC assembly is only used in two channel analyzers. The A12 BNC assembly routes the signals connected to the Channel 1 BNC connector and Channel 2 BNC connector to the A1 Input assembly. The A12 BNC assembly also routes the source signal from the A5 Analog assembly to the Source BNC connector. The signal connected to Channel 1 should be between 0.19531 Hz to 102.4 kHz in single channel mode and between 0.097656 Hz to 51.2 kHz in two channel mode. The signal connected to Channel 2 should be between 0.097656 to 51.2 kHz. For both channels, the signal's amplitude range must be between +27 dBVrms and –51 dBVrms for full scale measurements. The source output signal can be random noise, burst random noise, periodic chirp, burst chirp, pink noise, or fixed sine. The amplitude range of the source output is ±5 Vpk.

A13 Primary Keypad

The following table lists signals routed between the A11 Keyboard Controller assembly and the A13 Primary Keypad assembly. This table shows several things — if the assembly generates or uses the signal. A description of each signal follows the table.

Signal Name	A11 Location	A11	A13
CHANA	U1 pin 21	•	S
CHANB	U1 pin 6	•	S
COL0	U1 pin 5	•	S
COL1	U1 pin 4	•	S
COL2	U1 pin 3	•	S
COL3	U1 pin 2	•	S
COL4	U1 pin 1	•	S
COL5	U1 pin 27	•	S
COL6	U1 pin 26	•	S
COL7	U1 pin 25	•	S
HRNGAn	U3 pin 2	S	•
HRNGBn	U3 pin 4	S	•
HRNGCn	U3 pin 6?	S	•
HRNGDn	U3 pin 8?	S	•
OVLDAn	U2 pin 4	S	•
OVLDBn	U2 pin 5	S	•
OVLDCn	U2 pin 6	S	•
OVLDDn	U2 pin 7	S	•
ROW0	U1 pin 13	•	S
ROW1	U1 pin 14	•	S
ROW2	U1 pin 15	•	S
ROW3	U1 pin 16	•	S
ROW4	U1 pin 17	•	S
ROW5	U1 pin 22	•	S
ROW6	U1 pin 23	•	S
SRCn	U2 pin 9	S	•
+5 V	U1 pin 19	•	•
Gnd	U1 pin 12	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.

CHANA — CHANB

These lines indicate the RPG's direction and offset.

COL0 - COL7

Column 0 - Column 7 — A high-to-low transition on one column line indicates that a key in that column was pressed. After the A11 Keyboard Controller assembly's microprocessor determines the keypad row location and the key number, the microprocessor sets columns 0 to 5 low which forces SINTFPn low. A high-to-low transition on SINTFPn informs the A7 CPU assembly that a key was pressed.

HRNGAn

	Half Range A — In both the two channel and four channel analyzer, a low on this line turns on the channel 1 half range LED. This line goes low when the A1 or A2 Input assembly detects that the amplitude of the channel 1 input signal reached half the set range. This line is HRNGA inverted by the A11 Keyboard Controller assembly.
HRNGBn	Half Range B — In a two channel analyzer, a low on this line turns on the channel 2 half range LED. In a four channel analyzer, a low on this line turns on the channel 3 half range LED. This line goes low when the A1 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range or when the A2 Input assembly detects that the amplitude of the channel 3 input signal reached half the set range. This line is HRNGB inverted by the A11 Keyboard Controller assembly.
HRNGCn	Half Range C — In a four channel analyzer, a low on this line turns on the channel 2 half range LED. This line goes low when the A2 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range. This line is HRNGC inverted by the A11 Keyboard Controller assembly. This line is only used in four channel analyzers.
HRNGDn	Half Range D — In a four channel analyzer, a low on this line turns on the channel 4 half range LED. This line goes low when the A2 Input assembly detects that the amplitude of the channel 4 input signal reached half the set range. This line is HRNGD inverted by the A11 Keyboard Controller assembly. This line is only used in four channel analyzers.
OVLDAn	Overload A — In a four channel analyzer, a low on this line turns on the channel 1 overload LED. This line goes low when the A2 Input assembly detects that the amplitude of the channel 1 input signal exceeded the set range. This line is only used in four channel analyzers.
OVLDBn	Overload B — In four channel analyzers, a low on this line turns on the channel 2 overload LED. This line goes low when the A2 input assembly detects that the amplitude of the channel 2 input signal exceeded the set range. This line is only used in four channel analyzers.
OVLDCn	Overload C — In a two channel analyzer, a low on this line turns on the channel 1 overload LED. In a four channel analyzer, a low on this line turns on the channel 3 overload LED. This line goes low when the A1 Input assembly detects that the amplitude of the channel 1 input signal exceeded the set range or when the A2 Input assembly detects that the amplitude of the channel 3 input signal exceeded the set range.
OVLDDn	Overload D — In a two channel analyzer, a low on this line turns on the channel 2 overload LED. In a four channel analyzer, a low on this line turns on the channel 4 overload LED. This line goes low when the A1 Input assembly detects that the amplitude of the channel 2 input signal exceeded the set range or when the A2 Input assembly detects that the amplitude of the channel 4 input signal exceeded the set range.
ROW0 - ROW6	Row 0 - Row 7 — When the row lines are set high, the row line that remains low indicates that a key in that row was pressed.
SRCn	Source On — A low on this line turns on the source LED. This line goes low when the Source is turned on.

A14 Secondary Keypad

The following table lists signals routed between the A11 Keyboard Controller assembly and the A14 Secondary Keypad assembly. This table shows several things — if the assembly generates or uses the signal. A description of each signal follows the table.

Signal Name	A11 Connection	A11	A14
COL0	P2 Pin 3	•	S
COL1	P2 Pin 2	•	S
COL2	P2 Pin 1	•	S
ROW0	P3 Pin 3	•	S
ROW1	P3 Pin 2	•	S
ROW2	P3 Pin 1	•	S
ROW3	P4 Pin 3	•	S
ROW4	P4 Pin 2	•	S
ROW5	P4 Pin 1	•	S
PWRFW	P5 Pin 3	S	•
GND	P5 Pin 1	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.

COL0 - COL2 — Column 0 - Column 2 — A high-to-low transition on one column line indicates that a key in that column was pressed. After the A11 Keyboard Controller assembly's microprocessor determines the keypad row location and the key number, the microprocessor sets the column lines low which forces SINTFPn low. A high-to-low transition on SINTFPn informs the A7 CPU assembly that a key was pressed.

ROW0 - ROW5 — Row 0 - Row 5 — A low on one row line indicates that a key in that row was pressed.

PWRFW — Power Fail Warning — A high on this line turns on the power-on LED.

A22 BNC

The A22 BNC assembly is only used in four-channel analyzers. The A22 BNC assembly routes the signals connected to the Channel 1 BNC connector and Channel 3 BNC connector to the A2 Input assembly connected to J1 on the Motherboard. The A22 BNC assembly also routes the signals connected to the Channel 2 BNC connector and Channel 4 BNC connector to the A2 Input assembly connected to J2 on the Motherboard. The signal connected to Channel 1 and Channel 2 should be between 0.097656 Hz to 51.2 kHz in two-channel mode and between 0.048828 Hz to 25.6 kHz in four-channel mode. The signal connected to Channel 3 and Channel 4 should be between 0.048828 Hz to 25.6 kHz. For all channels, the signal's amplitude range must be between +27 dBVrms and –51 dBVrms for full-scale measurements.

A99 Motherboard

The following table lists all signals routed through the Motherboard. The table uses bold face type to show which assembly can generate the signal. A description of each signal follows the ''Motherboard Voltages'' table.

Signal Name	Assembly Using Signal								
	A1/A2	A2	A5	A6	A7	A10	A90	A98	Ext Mon
	Motherboard Connector								
	J1	J2	J5	J6	J7	P10	P90	P98	P95
	Connector Pin Number								
A10MHZ					**150**	59			
ADCOLn			**17B**	17A					
ADCULn			**17C**	17B					
ADDATA			**20C**	20A					
B5MHZ					**148**	60			
BRESETn			12A	12B	**112**				
BTACH				32A		**10**			
CALP	C1	C1	**1A**						
CEHPIBn					**138**	25			
CEONIXn					**139**	31			
CHSYNCn			18C	**18A**					
DACCLK			9C	**9B**					
DACDAT			10C	**10A**					
DACUPDn			8C	**8B**					
DITHER			**11A**	11A					
DSPTRIG				**25A**	125				
DSR					**46**	11			
ECLK				22C	**72**				
EFFSMP			19C	**18B**					
EXTRGIN			32B			**8**			
FA1				13B	**64**				
FA2				13C	**114**				
FA3				14B	**65**				
FA4				14C	**115**				
FA5				15B	**66**				
FAN+						**43**	2		
FANFUL					**93**	46			
FANOFF					**143**	45			
FANTRIP			9A		61				
FD0				**25B**	**76**				

Signal Name	Assembly Using Signal								
	A1/A2	A2	A5	A6	A7	A10	A90	A98	Ext Mon
	Motherboard Connector								
	J1	J2	J5	J6	J7	P10	P90	P98	P95
	Connector Pin Number								
FD1				**25C**	**126**				
FD2				**26B**	**77**				
FD3				**26C**	**127**				
FD4				**27B**	**78**				
FD5				**27C**	**128**				
FD6				**28B**	**79**				
FD7				**28C**	**129**				
FD8				**29B**	**80**				
FD9				**29C**	**130**				
FD10				**30B**	**81**				
FD11				**30C**	**131**				
FD12				**31B**	**82**				
FD13				**31C**	**132**				
FD14				**32B**	**83**				
FD15				**32C**	**133**				
FDTACKn				**19B**	69				
FIFOBAVn				**18C**	68				
FIFOENn				23B	**123**				
FIFORDYn				**24B**	75				
FIRQn				**20C**	70				
FRW				19C	**119**				
FSDIV2				**6C**				30	
FSELAn				24C	**74**				
FSELSn				23C	**124**				
H10MHZ			22C	**22B**					
H20MHZ			21C	21B	**121**				
HRNGA	**A10**				107				
HRNGB	**B10**				57				
HRNGC		**A10**			108				
HRNGD		**B10**			58				
HSYNC					56				8
IFCn					84	**14**			
IMODE					102			**28**	
INTHPIBn					88	**26**			
INTONIXn					89	**32**			
KEYVALID					135	**17**			
LPFCLK			10B	**10B**					

Signal Name	Assembly Using Signal								
	A1/A2	A2	A5	A6	A7	A10	A90	A98	Ext Mon
	Motherboard Connector								
	J1	J2	J5	J6	J7	P10	P90	P98	P95
	Connector Pin Number								
MDACCSn			8B	**8A**					
PFWn			16A		101			**29**	
PREFS	B16	B16	23C	**23A**					
PVALID					52			**59**	
RA1					**140**	**35**			
RA2					**91**	**38**			
RA3					**141**	**37**			
RA4					**92**	**40**			
RA5					**142**	**39**			
RD24					**94**	**48**			
RD25					**144**	**49**			
RD26					**95**	**50**			
RD27					**145**	**51**			
RD28					**96**	**54**			
RD29					**146**	**53**			
RD30					**97**	**56**			
RD31					**99**	**55**			
RDTACKn					137	**23**			
RRESETn					**134**	12			
RRW					**90**	36			
RSI					86	**20**			
RSO					**136**	19			
SCL	B15	B15	11C		**60**	2			
SDA	**A15**	**A15**	**11B**		**111**	1			
SHUTn			4C		**51**			58	
SINTn	**C15**	**C15**			62				
SPARE1			7C	7B					
SPARE2			9B	9A					
SPARE3				6B	53				
SPARE4	A1	A1	1C						
SRCCLOCK			7B	**7A**					
SRCDATA			6C	**6A**					
SYSCNTR					**85**	18			
TRIGGER			**12C**	12A					
VDATA					**73**				3, 4, 5
VSYNC					**106**				9
WEHPIBn					**87**	24			

The following table lists all voltages routed through the Motherboard (see ‘’Power Supply Voltage Distribution’’ earlier in this chapter for a complete list of assemblies using each voltage).

Voltage	Assembly Using Voltage								
	A1/A2	A2	A5	A6	A7	A10	A90	A98	EXT MON
	Motherboard Connector								
	J1	J2	J5	J6	J7	P10	P90	P98	P95
	Connector Pin Number								
+18 V	A3 – C3	A3 – C3	3A – 3C			5 – 6		18 – 19 48 – 49	
–18 V	A5 – C5	A5 – C5	5A – 5C		103	3 – 4		25 – 26 55 – 56	
+12 V					4 – 5 54 – 55 104–105	21 – 22		15 – 17 45 – 47	
+8 V	A7 – C7	A7 – C7	14A–14C					27 57	
+5 V			16B–16C	1A – 4C	1 – 3 12 – 20 47 – 50 63 98 100 113	27 – 30		1 – 8 31 – 38	
GND	B1 A2 C2 A4 C4 A6 – C6 A8 – C8 A9 C9 A11 C11 A12–C12B 13–C13C14 A16 C16	B1 A2 C2 A4 C4 A6 – C6 A8 – C8 A9 C9 A11 C11 A12 C12 C13 A14 C14 A16 C16	1B 2A – 2C 4A – 4B 6A – 6B 7A 8A 12B 13A–13 15A–15 17A 18A–18B 19A–19B20 A–20B21A –21B22A–2 2B23A–23 B25A < @1 50 > 25C26A–26 B27A–27C 28A–28C29 A–29C30A 31A	5A – 5C 7C 9C 10C 11B–11C12 C 13A 15A 17C 19A 20B 21A 21C 22A 24A 26A 27A 28A 29A 30A	7 – 11 21 – 45 59 71 109 118 120 122 147 149	7 9 13 15 – 16 33 – 34 44 47 52 57 – 58	1	9 – 14 20 – 24 39 – 44 50 – 54 60	1 2 6

A10MHZ	10 MHz Clock — This is a 50% duty cycle, 10 MHz clock. This clock provides the timing for the IIC processor on the A10 Rear Panel assembly.
ADCOLn	ADC Overload — This line goes low when the input to the A5 Analog assembly's ADC exceeds its positive limit.
ADCULn	ADC Underload — This line goes low when the input to the A5 Analog assembly's ADC exceeds its negative limit.
ADDATA	Analog to Digital Data — This line is the digital representation of the input signal from the A5 Analog assembly's ADC controller. The ADC controller sends this digital representation to the A6 Digital assembly once per sample (3.8147 ms).
B5MHZ	5 MHz Clock — This is a 50% duty cycle, 5 MHz clock. This clock provides the timing for the GPIB controller on the A10 Rear Panel assembly.
BRESETn	Buffered Reset — A low on this line resets the digital logic on the A5 Analog and A6 Digital assembly. This line pulses low during power-up and power-down, and when the A7 CPU assembly's microprocessor executes the RESET instruction or is externally reset.
BTACH	Buffered Tachometer — This line is a TTL representation of the A10 Rear Panel assembly's tachometer input.
CALP	Calibration Signal — This line is the calibration signal from the A5 Analog assembly. During calibration routines, this signal calibrates the input circuit on the A1 or A2 Input assembly. See "Calibration Routine Description" in chapter 10, ''Internal Test Descriptions,'' for further details.
CEHPIBn	GPIB Controller Chip Enable — This line is low whenever the GPIB controller is accessed for read or write operations.
CEONIXn	Chip Enable for the Parallel Port Controller — A low on this line enables the parallel port controller on the A10 Rear Panel assembly.
CHSYNCn	Channel Synchronize — A low on this line synchronizes the A5 Analog assembly's ADC controller with the A6 Digital assembly.
DACCLK	Source Attenuation DAC Clock — This clock provides the timing for data transfer to the A5 Analog assembly's source attenuator and dc offset DAC. This clock is generated by the A6 Digital assembly's digital source.
DACDAT	Source Attenuation DAC Data — This line provides the control for the A5 Analog assembly's attenuator DAC and dc offset DAC. This serial data line is generated by the A6 Digital assembly's digital source.
DACUPDn	Source Attenuation DAC Latch — This is a control line from the A6 Digital assembly's digital source. A low on this line latches DACDAT after it is clocked into the A5 Analog assembly's attenuator DAC and dc offset DAC.
DITHER	Dither — This line provides digital noise to the A6 Digital assembly's digital filter. The noise bandwidth is set by EFFSMP.
DSPTRIG	DSP Trigger — This is a trigger line for the DSP processor on the A7 CPU assembly. The DSP processor uses this line during gated measurements.
DSR	Data Set Ready — Some devices connected to the serial port check this line for a high to verify that the analyzer is connected and ready. The user can set this line high or set this line to go high only when the analyzer is ready for data transfer.
ECLK	E Clock — The gate arrays on the A6 Digital assembly use this clock for read and write timing.
EFFSMP	Effective Sample Rate — This line sets the update rate for DITHER. The update rate is frequency and span dependent, and controls the dither bandwidth.

EXTRGIN	External Trigger In — This is a buffered version of the A10 Rear Panel assembly's external trigger input.
FA1 — FA5	Fast Bus Address Lines — These lines are a buffered form of the A7 CPU assembly's microprocessor address bus. The CPU assembly uses these lines to address different circuits on the A6 Digital assembly.
FAN+	Fan Voltage — This voltage can vary from approximately +12 V to 0 V. This variable voltage turns the fan on and off and controls the speed of the A90 Fan assembly.
FANFUL	Fan Full — A high on this line causes FAN+ to go to its positive limit. When FAN+ is at its positive limit, the A90 Fan assembly is on and turning at its highest speed.
FANOFF	Fan Off — A high on this line causes FAN+ go to its negative limit. When FAN+ is at its negative limit, the A90 Fan assembly is off.
FANTRIP	Fan Trip — A high on this line causes FANOFF to go low which allows the fan to turn on and cool the analyzer. This line goes high when the fan is turned off and the internal temperature exceeds a set point.
FD0 — FD15	Fast Bus Data Lines — These bidirectional data lines are a buffered version of the A7 CPU assembly's buffered microprocessor data bus. These lines allow communication between the CPU assembly and A6 Digital assembly.
FDTACKn	Fast Bus Data Transfer Acknowledge — A low on this line terminates asynchronous bus cycles.
FIFOBAVn	First In First Out Block Available — This line goes low after the FIFO gate array on the A6 Digital assembly collects a complete block of data.
FIFOENn	First In First Out Enable — This line pulses low in response to a low on FIFOBAVn. This line enables the transfer of one data word from the A6 Digital assembly's FIFO gate array to the A7 CPU assembly over the fast bus.
FIFORDYn	First In First Out Ready — This line goes low when a data word is ready to be transferred from the A6 Digital assembly over the fast bus.
FIRQn	Fast Bus Interrupt Request — A low on this line interrupts the A7 CPU assembly.
FRW	Fast Bus Read/Write — This line is high during a read cycle and low during a write cycle. This line is a buffered version of the read/write line (PRW).
FSDIV2	Sample Clock Divided By 2 — This is a 50% duty cycle, 131.072 kHz clock generated by the A6 Digital assembly to synchronize the A98 Power Supply assembly. The Power Supply assembly phase locks its switching frequency to this clock.

FSELAn	Fast Bus Asynchronous Select — This line is low when an asynchronous fast bus cycle is in operation.
FSELSn	Fast Bus Synchronous Select — This line is low when a synchronous fast bus cycle is in operation. The A6 Digital assembly uses this signal to enable I/O to its gate arrays and to the A5 Analog assembly's source attenuator DAC and dc offset DAC.
H10MHZ	10 MHz Clock — This is a 50% duty cycle, 9.961472 MHz clock. This clock is H20MHZ divided by 2.
H20MHZ	20 MHz Clock — This is a 50% duty cycle, 19.922944 MHz clock. This clock provides the timing for the analyzer.
HRNGA	Half Range A — In both the two channel and four channel analyzer, a high on this line turns on the channel 1 half range LED. This line goes high when the A1 or A2 Input assembly detects that the amplitude of the channel 1 input signal reached half the set range.
HRNGB	Half Range B — In a two channel analyzer, a high on this line turns on the channel 2 half range LED. In a four channel analyzer, a high on this line turns on the channel 3 half range LED. This line goes high when the A1 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range or when the A2 Input assembly detects that the amplitude of the channel 3 input signal reached half the set range.
HRNGC	Half Range C — In a four channel analyzer, a high on this line turns on the channel 2 half range LED. This line goes high when the A2 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range. This line is only used in four channel analyzers.
HRNGD	Half Range D — In a four channel analyzer, a high on this line turns on the channel 4 half range LED. This line goes high when the A2 Input assembly detects that the amplitude of the channel 4 input signal reached half the set range. This line is only used in four channel analyzers.
HSYNC	Horizontal Synchronization — A high on this line causes the external monitor to do a horizontal retrace. The Motherboard buffers this signal and routes it to the EXT MONITOR connector.
IFCn	Interface Clear — This line is only used during the analyzer's development.
IMODE	Input Mode — This line indicates the A98 Power Supply assembly's input power mode. When this line is high, the Power Supply assembly is operating on ac power. When this line is low, the Power Supply assembly is operation on dc power.
INTHPIBn	GPIB Controller Interrupt — A low on this line interrupts the A7 CPU assembly. This line is controlled by the A10 Rear Panel assembly's GPIB controller.
INTONIXn	Parallel Port Interrupt — A low on this line interrupts the A7 CPU assembly. This line is controlled by the A10 Rear Panel assembly's parallel port controller.
KEYVALID	Key Valid — A high on this line interrupts the A7 CPU assembly. This line goes high when a key is pressed on an external keyboard.

LPFCLK	Low Pass Filter Clock — This is a control line from the A6 Digital assembly's digital source. This line controls the cut-off frequency of the A5 Analog assembly's programmable low pass filter.
MDACCSn	Source Attenuation DAC Chip Select — This is a control line from the A6 Digital assembly's digital source. A low on this line enables the Attenuator DAC and DC offset DAC on the A5 Analog assembly.
PFWn	Power Fail Warning — This line goes low 10 ms before the A98 Power Supply assembly's output voltages fall out of regulation. A low on this line tells the A7 CPU assembly to prepare for power down and opens a relay which disconnects the source output on the A5 Analog assembly. This line goes low in response to SHUTn going low or when the supply voltage is disconnected or is too low.
PREFS	Pre-Sample Clock — This is a 262.144 kHz clock. This clock is at the same frequency as the system sample rate, but it is inverted and advanced in time by 100 ns.
PVALID	Power Valid — This line is high when the +5 V supply from the A98 Power Supply assembly is stabilized.
RA1 - RA5	Rear Bus Address Lines — These lines are a buffered form of the A7 CPU assembly's microprocessor address bus. The CPU assembly uses these lines to address different circuits on the A10 Rear Panel assembly.
RD24 - RD31	Rear Bus Data Lines — These bidirectional data lines are an extension of the A7 CPU assembly's digital data bus. These lines allow communication between the CPU assembly and A10 Rear Panel assembly.
RDTACKn	Rear Bus Data Transfer Acknowledge — A low on this line terminates asynchronous bus cycles.
RRESETn	Rear Reset — A low on this line resets the digital logic on the A10 Rear Panel assembly. This line pulses low during power-up and power-down and when the A7 CPU assembly's microprocessor executes the RESET instruction or is externally reset.
RRW	Rear Bus Read/Write — This line is high during a read cycle and low during a write cycle. This line is an extension of the processor read/write line (PRW).
RSI	RS-232 Input — This is the serial RS-232-C receive data line. This line transmits data to the A7 CPU assembly from peripheral devices one byte at a time.
RSO	RS-232 Output — This is the serial RS-232-C transmit data line. This line transmits data from the A7 CPU assembly to peripheral devices one byte at a time.
SCL	Serial Clock — This is the serial clock for the IIC bus. The IIC controller on the A7 CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.
SDA	Serial Data — This is the IIC bus bidirectional data line. This line transmits data to or from the A7 CPU assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.
SHUTn	Power Supply Shut Down — A connection to ground on this line forces all Power Supply output voltages to zero. This line is normally an open circuit, but becomes a connection to ground if the analyzer's internal temperature becomes excessive or if the power supply is operating on dc power and no measurement has been made within 30 minutes.
SINTn	Serial Interrupt — This is the IIC bus interrupt line. A low on this line interrupts the A7 CPU assembly.

SRCCLOCK	Source Clock — This clock provides the timing for data transfer to the A5 Analog assembly's serial-in parallel-out shift register. This clock is generated by the A6 Digital assembly's digital source.
SRCDATA	Source Data — This is the data line for the A5 Analog assembly's serial-in parallel-out shift register. This serial data line is generated by the A6 Digital assembly's digital source.
SYSCNTR	System Control — A high on this line enables the A10 Rear Panel assembly's GPIB buffers. This line is high when the analyzer is under GPIB control.
TRIGGER	Trigger — This line changes state when the selected trigger (channel 1, channel 2, channel 3, channel 4, or external trigger) equals or exceeds the trigger level. An active edge on this line causes the A6 Digital assembly to trigger the analyzer.
VDATA	Video Data — This is the serial data line for the external monitor. The Motherboard buffers this line and routes three lines to the EXT MONITOR connector. Pin 3 is the data line for the color red, pin 4 is the data line for the color green, and pin 5 is the data line for the color blue.
VSYNC	Vertical Synchronization — A high on this line causes the external monitor to do a vertical retrace. The Motherboard buffers this signal and routes it to the EXT MONITOR connector.
WEHPIBn	GPIB Write Enable — A low on this line enables write operations to the A10 Rear Panel assembly's GPIB controller.

A100 Disk Drive

The following table lists signals routed between the A100 Disk Drive assembly and the A7 CPU assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A7 P3	A100
DIR	17	S	•
DISKINn	22	•	S
DRIVESELn	21, 29	S	•
DSKCHGn	1	•	S
HDSEL	3	S	•
HIDENSn	33	•	S
INDEXn	27	•	S
MTRn	19, 31	S	•
ReDATAn	5	•	S
SEL0	25	S	•
SEL1	23	S	•
STEPn	15	S	•
TOOn	9	•	S
WDATA	13	S	•
WGATE	11	S	•
WRIPROTn	7	•	S
+5 V	24, 26, 28	•	•
Gnd	2-20 (even)	•	•
Not Used	30, 32, 34	—	—

S This assembly is the source of the signal.
• This assembly uses the signal.
— This assembly does not use this signal.

DIR	Direction — This line sets the direction for the disk head. A high on this line sets the direction away from the spindle. A low on this line sets the direction toward the spindle.
DISKINn	Disk In — This line goes low when a flexible disk is inserted in the A100 Disk Drive assembly.
DRIVESELn	Drive Select — A low on this line selects the A100 Disk Drive assembly.
DSKCHGn	Disk Change — This line goes low when a flexible disk is removed from the A100 Disk Drive assembly. This line remains low until a flexible disk is installed and STEPn goes low.
HDSEL	Head Select — A low on this line selects the lower disk drive head. A high on this line selects the upper disk drive head.
HIDENSn	High Density Select — This line goes low when a high density flexible disk is inserted in the A100 Disk Drive assembly.
INDEXn	Index — This line pulses low with each revolution of the flexible disk.
MTRn	Motor On — A low on this line turns on the disk drive motor.
ReDATAn	Read Data — This line pulses low for each bit detected on the flexible disk.
SEL0 - SEL1	Drive Select — When SEL0 and SEL1 are low, the A100 Disk Drive assembly is enabled.
STEPn	Step — A low on this line moves the disk drive head. When STEPn and DIR are low, the head moves toward the disk spindle. When STEPn is low and DIR is high, the head moves away from the disk spindle.
T00n	Track 00 — This line is low when the head is positioned over track 0 on the flexible disk.
WDATA	Write Data — When WGATE is low, a low pulse on this line writes a bit to the disk.
WGATE	Write Gate — When this line is low, information may be written to the A100 Disk Drive assembly under control of the WDATA line.
WRIPROTn	Write Protect — This line is low when a write-protected disk is installed in the A100 Disk Drive assembly.

A101 Display

The following table lists signals routed between the A102 DC-DC Converter assembly and the A101 Display assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A102	A101
HSYNCELn	11	•	•
PSENBLn	18	•	S
VCLK	15	•	•
VID	13	•	•
VSYNCEL	9	•	•
+215 V	4	S	•
-175 V	1	S	•
+40 V	5	S	•
+20 V	17	S	•
+12 V	6	•	•
+5 V	7	•	•
Gnd	2, 3, 12, 14, 16	•	•
Not Used	19, 20	—	—

S This assembly is the source of the signal.
• This assembly uses the signal.
— This assembly does not use this signal.

HSYNCELn — Horizontal Synchronization — A low on this line causes a horizontal retrace on the A101 Display assembly. Between each HSYNCELn pulse, 560 pixels are sent to the Display assembly.

PSENBLn — Power Supply Enable — A low on this line enables the A102 DC-DC Converter assembly's power supply. The power supply generates the driver supply voltages. The driver supply voltages are +20 V, +40 V, +215 V, and −175 V.

VCLK — Video Clock — This 20 MHz clock provides the timing reference for HSYNCELn, VID, and VSYNCEL. The rising edge of this clock determines setup and hold times.

VID — Video Data — This is the serial data line for the A101 Display assembly. This line transmits video data to the Display assembly. The video data is transmitted at the VCLK rate between horizontal and vertical retraces (during the time HSYNCELn is high and VSYNCEL is low). Only the first 400 lines of data are displayed after a VSYNCEL pulse.

VSYNCEL — Vertical Synchronization — A high on this line causes a vertical retrace on the A101 Display assembly.

A102 DC-DC Converter

The following table lists signals routed between the A7 CPU assembly and the A102 DC-DC Converter assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A7 P2	A102
HSYNCELn	11	S	•
VCLK	13	S	•
VID	15	S	•
VSYNCEL	9	S	•
+12 V	1, 2	•	•
+5 V	3, 4	•	•
Gnd	7, 8, 10, 12, 14, 16	•	•
Not Used	5, 6	—	—

S This assembly is the source of the signal.
• This assembly uses the signal.
— This assembly does not use this signal.

HSYNCELn — Horizontal Synchronization — A low on this line causes a horizontal retrace on the A101 Display assembly. Between each HSYNCELn pulse, 560 pixels are sent to the Display assembly.

VCLK — Video Clock — This 20 MHz clock provides the timing reference for HSYNCELn, VID, and VSYNCEL. The rising edge of this clock determines setup and hold times.

VID — Video Data — This is the serial data line for the A101 Display assembly. This line transmits video data to the Display assembly. The video data is transmitted at the VCLK rate between horizontal and vertical retraces (during the time HSYNCELn is high and VSYNCEL is low). Only the first 400 lines of data are displayed after a VSYNCEL pulse.

VSYNCEL — Vertical Synchronization — A high on this line causes a vertical retrace on the A101 Display assembly.

10

Internal Test Descriptions

Internal Test Descriptions

This chapter describes the power-on test, calibration routine, fault log messages, and self tests. This chapter also contains a list of the GPIB commands for each self test.

Power-on Test Description

The power-on test is run when the analyzer is powered up. The calibration routine is run immediately following the power-on test. The power-on test exercises the A7 CPU assembly and A8 Memory assembly. This test is divided into low-level and high-level subtests.

Low-level Subtests

The low-level power-on subtests exercise the core of the A7 CPU assembly and A8 Memory assembly. If an error occurs during the low-level subtests, the test stops and displays an error code on the A7 CPU assembly's power-on test LEDs.

High-level Subtests

The high-level power-on subtests exercise the fast bus and the multi-function peripheral on the A7 CPU assembly. The high-level subtests are also self tests (see ''Self-Test Descriptions''). If an error occurs during the high-level subtests, an error message is entered in the test log.

Power-on Test Messages

The ''Power-on Test Messages'' table provides additional information for interpreting the power-on test LEDs. Using the ''Binary to Hexadecimal'' table, translate the power-on test LEDs to their equivalent hexadecimal code (see ''To troubleshoot power-up failures'' on page 4-15 for details on decoding the power-on test LEDs to their binary code). The ''Power-on Test Messages'' table describes the power-on subtests in the order they are run. The table also shows the relationship between a failing power-on subtest and the assemblies or sub-blocks.

False error codes can be caused by shorts on the buses, reset line, or interrupt line. If an error code is caused by the last bus connected, it is probably the source of the failure.

Binary to Hexadecimal

Binary 1 = LED on 0 = LED off	Hexadecimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power-on Test Messages

Hexadecimal Code	Message	Assembly/Sub-block								
		A98 Power Supply	A7 MPU & Address Decoder	A7 MPU Buses, Coprocessor, DSP, MFP	A7 Monitor ROM	A7 Display Controller	A8 Memory	Fast Bus or IIC Bus	A11 Keyboard Controller	
Undefined	Initial power-on	X	X	X						
FF*	CPU flashes LEDs	0	X	X	X					
04	LED DSACK failure	0	X	X	X					
13	CPU failure	0	X	X	X					
01	Coprocessor DSACK failure	0	0	X	X					
17	Coprocessor failure	0	0	X	X					
18	Boot ROM checksum failure	0	0	0	X					
06	Display DSACK failure	0	0	0	0	X				
10	Display failure	0	0	0	0	X				
1B	Main RAM too small	0	0	0	0	0	X			
02	Main RAM DSACK	0	0	0	0	0	X			
14	Main RAM bit failure	0	0	0	0	0	X			
16	Main RAM refresh failure	0	0	0	0	0	X			
1C	Program ROM checksum error	0	0	0	0	0	X			
00	Clear ~4s	0	X	X	0	0				
A1	Starting DSP test	0	0	X	0	0	0			
A2	Fast bus test	0	0	0	0	0	0	X		
A0	MFP test failure	0	0	X	0	0				
AE	Front panel test	0	0	X	0	0	0	0	X	

0 Assembly or sub-block is used but is probably not the cause of the failure message.
X Assembly or sub-block is probably the cause of the failure message.
(blank) Assembly or sub-block is not used in the test.
FF* If the area of failure is unclear, all LEDs flash continuously.

Calibration Routine Description

The calibration routine consists of a dc-offset calibration and a frequency calibration. The calibration routine occurs immediately following the power-on tests and periodically afterwards to compensate for any drift. The calibration routine sets the input relays to disconnect the internal circuitry from the BNC center conductor and shell, and connect the source (via CALP) to the input channels. Measurements are then taken using several input paths to produce correction curves for all input ranges.

If calibration fails, the calibration routine is repeated up to two more times. Each time calibration fails, a calibration failure message is added to the fault log. If calibration fails all three times, a calibration failure message is displayed on the screen.

If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening, press [**Preset**] [DO PRESET] or cycle power after you abort a self test.

To manually start the calibration routine, press the [**System Utility**] [CALIBRATN] [SINGLE CAL].

To prevent the calibration routine from occurring, set the power switch to on (|), then as soon as Booting System appears on the display, press and hold in the [**Preset**] key until Autorange in progress appears. This not only prevents the calibration routine from occurring but also bypasses the auto start file if one exists.

DC-Offset Tables and Frequency Correction Curves

The dc-offset calibration builds 5 dc-offset tables — one for each anti-alias filter and one for each channel when the anti-alias filters are bypassed. The values in the dc-offset tables are sent to the channel dc-offset DACs to compensate for dc offsets introduced by analog input circuits. Forty values are entered in each table — a value for each range setting from –51 dB to +27 dB, in 2 dB increments. For each range, the table value is derived by changing the offset values of the dc offset DAC until the best possible offset compensation is found. In all instrument modes, the analyzer corrects for dc offsets by setting each channel's dc-offset DAC to the value from the table that matches the current anti-alias filter and range setting.

The frequency calibration generates correction curves in the frequency domain to compensate for unflatness in the analog input circuits. A precise signal is connected from the source to the input channels via the calibration path (CALP). Correction curves are then produced for each range setting by taking the difference between the source output and the measured response. In FFT analysis, correlation analysis, and swept sine instrument modes, the analyzer multiplies the measured result with the value from the frequency correction curve that matches the current range and span setting. In this way, errors introduced by circuits in the analyzer are removed before the measurement is displayed.

Calibration Error Messages

The dc-offset tables and frequency correction curves produced by the calibration routine are compared with a set of maximum allowable error curves. The Quick Confidence self test runs the calibration routine and places error messages in the Test Log if any measurement exceeds the maximum allowable error. To run the Quick Confidence self test press the following keys:

[**System Utility**]
  [SELF TEST]
  [QUICK CONF TEST]

The following lists the possible error messages:

Quick Confidence failure information:
Channel X 0 dB freq
Channel X 20 dB freq
Channel X 40 dB freq
Channel X step attenuator
Channel X –12 dB pad
Channel X +14 dB pad
Quick Confidence FAIL

Where X = 1, 2, 3, or 4 and freq = 100k, 50k, or 25k

Viewing the Calibration Correction Curves

The calibration correction curves can be viewed for any input range or frequency span. However, there is no frequency correction if the anti-alias filter is bypassed or if the A-weight filter is on. When there is no frequency correction, the calibration curve is a flat 0 dB line.

You can save the calibration trace to a data register only when in FFT analysis or correlation analysis instrument mode. However, these data registers can be displayed in any instrument mode.

The following key sequence shows how to view the calibration correction curves for channel 1 and 2 at a 1 Vrms range setting, full span. Other curves can be displayed by changing the input range and frequency span.

[**Inst Mode**]
[2 CHANNEL]
[**Input**]
[CHANNEL 1 RANGE]
1
[dBVrms]
[CHANNEL 2 RANGE]
1
[dBVrms]
[**Disp Format**]
[UPPER/LOWER]
[**System Utility**]
[CALBRATIN]
[SAVE CH1 CAL TRACE]
[INTO D1]
[SAVE CH2 CAL TRACE]
[INTO D2]
[**Meas Data**]
[MORE]
[DATA REGISTER]
[D2]
[**Active Trace**]
[D1]
[**Scale**]
[Y PER DIV (DECADES)]
1
[ENTER]
[CENTER REFERENCE]
0
[ENTER]
[**Active Trace**]
[Y PER DIV (DECADES)]
1
[ENTER]
[CENTER REFERENCE]
0
[ENTER]

Note

Display A shows the message D1 CAL CHAN 1 and display B shows the message D2 CAL CHAN 2.

The calibration correction curves should be contained within ±5 dB. The ±5 dB limit applies to all ranges at full span.

Fault Log Messages

0	Unknown Fault	This error message occurs when the fault could not be determined.
1	I2C: Timeout	This error message occurs if the A7 CPU assembly's IIC controller takes too long to tell the MPU that it is ready for a new command.
2	I2C: No Device Acknowledge	This error message occurs if the A7 CPU assembly's IIC controller does not sense the acknowledge part of the formal handshake used to transmit data over the IIC bus.
3	Calibration failure	This error message occurs if the calibration routine generates correction vectors that exceed the maximum allowable error vectors or if the calibration routine is bypassed because of a hardware failure.
4	ROM Checksum error	This error message occurs if the power-on test detects a ROM checksum error.
5	BOOTROM Checksum Error	This error message occurs if the power-on test detects a BOOTROM checksum error.
6	DSP Failure	This error message occurs if the power-on digital signal processor test fails.
7	Main RAM Error	This error message occurs if the power-on RAM test fails.
8	Math Coprocessor Failure	This error message occurs if the power-on math coprocessor test fails.
9	LED Error	This error message occurs if the power-on LED test fails.
10	Display Failure	This error message occurs if the power-on display test fails.
11	CPU Failure	This error message occurs if the power-on CPU test fails.
12	Floppy Controller Timeout	This error message occurs if the A7 CPU assembly's disk drive controller did not respond within 10 ms of receiving a command.
13	Internal Disk Trk0 Failure	This error message occurs if the A100 Disk Drive assembly did not locate track 0 (as indicated by a low on T00n) when instructed by the A7 CPU assembly to move to track 0.
14	NVRAM or Battery Backup Failure	This error message occurs if the A7 CPU assembly's IIC Controller determined that the A8 Memory assembly's non-volatile RAM or RAM battery power failed.

Self-Test Descriptions

Thirty-seven self tests are available that can be run in groups or individually. The following table lists the group of self tests that are run when you select [FUNCTIONL TESTS], [ALL]. This group does not include any of the self tests that require a formatted flexible disk. The table lists the assemblies used by each self test and shows the assembly that would most likely cause the failure. To run these self tests in the order shown, press the following keys:

[**System Utility**]
  [SELF TEST]
  [FUNCTIONL TESTS]
  [ALL]

To run a single self test, press the softkey shown in the table instead of [ALL]. To determine the key path for the self-test softkeys, see “Self-Test Menu Map and GPIB Commands” starting on page 10-18.

Certain instrument malfunctions cause multiple self-test failures. Therefore, to determine the most likely cause when more than one self test fails, look in the ‘’Functional Tests All Self-Test Group’’ table for assemblies common to all failing self tests.

Functional Tests All Self-Test Group

Softkey	Self Test Name	Assembly									
		CPU	Memory	Digital	BNC	Input	Input	Analog	Rear Panel	Keyboard Contrr	Disk Driv
		A7	A8	A6	A12/ A22	A1	A2	A5	A10	A11	A100
[INTERRUPT]	Interrupt	X	0								
[MULTI FCTN PERIPHERL]†	Multi Fctn Peripheral	X	0								
[FRONT PANEL]†	Front Panel	X	0							X	
[GPIB FUNC TEST]	GPIB	X	0								
[DISK CONTROLLR]	Disk Controller	X	0								
[DISK FIFO]	Disk FIFO	X	0								
[IIC BUS]	IIC Bus	X	0	X		X	X	X	X	X	
[FAST BUS]†	Fast Bus	X	0	X							
[TRIGGER]	Trigger Gate Array	0	0	X							
[LO]	LO Gate Array	0	0	X							
[DIGITAL FILTER]	Digital Filter Gate Array	0	0	X							
[FIFO]	FIFO	0	0	X							
[BASEBAND]	Baseband	0	0	X		X	X	X			
[ZOOM]	Zoom	0	0	X		X	X	X			
[DGTL SRCE THRU DSP]	Source through DSP	0	0	X							
[SOURCE LO]	Source LO	0	0	X							
[SOURCE TO CPU]	Source to CPU	0	0	X							
[WITHOUT LO]	Source without LO	0	0	X		X	X	X			
[WITH LO]	Source with LO	0	0	X		X	X	X			
[ADC GATE ARRAY]	ADC Gate Array	0	0	0				X			
[OFFSET]	Input Offset	0	0	0		X	X	X			
[DISTORTN]	Input Distortion	0	0	0		X	X	X			
[INPUT TRIGGER]	Input Trigger	0	0	0		X	X	X			
[INPUT A-WEIGHT]	Input A-Wt Filter	0	0	0		X	X	X			
[AAF BYPASS]	Input AAF/Bypass	0	0	0		X	X	X			
[INPUT ICP]	Input ICP Source	0	0	0		X	X	X			
[TACHOMETR]$! C5,5,0,255,255,255	Tachometer	0	0	X	0				X		
[QUICK CONF TEST]	Quick Confidence	0	0	0		X	X	X			

X This assembly or sub-block is the most likely cause of the failure message. 0 This assembly or sub-block is used by the self test but is not the most likely cause of the failure message. No symbol means that the assembly is not used by the self test.

† High-level power-on tests
The power supply and display are used in every test.

Self Tests that Perform a Measurement

The following self tests perform measurements:

Self Test	Front Panel Softkey
Baseband	[BASEBAND]
Zoom	[ZOOM]
Source thru DSP	[DGTL SRCE THRU DSP]
ADC gate array	[ADC GATE ARRAY]
Source to CPU	[SOURCE TO CPU]
Source with LO	[WITH LO]
Source Without LO	[WITHOUT LO]
Input Offset	[OFFSET]
Input Distortion	[DISTORTN]
Input Trigger	[INPUT TRIGGER]
Input A-Wt Filter	[INPUT A-WEIGHT]
Input AAF/Bypass	[AAF BYPASS]
Input ICP Source	[INPUT ICP]

The measurements that these self tests perform are averaged measurements, with only one trace per average. Some hardware setup modes used in these self tests are not used by normal measurements and can not be accessed from the front panel.

The measurements bypass any standard corrections and do not perform calibration data corrections. Therefore, all self-test measurements using analog data have limits larger than the standard calibration tolerances.

Once the hardware is set up, data is taken and time records are processed according to the needs of the specific test. Some tests monitor overloads, others require spectrum data, and others require time record data. After the data is collected, it is compared to an internal reference specification to determine if the self test passed or failed. The pass or fail information along with any additional information is placed in the Test Log.

Individual Self-Test Descriptions

[AAF BYPASS] This test verifies that the anti-alias filters and the bypass circuits on the A1 Input assembly or A2 Input assemblies are operating correctly. In this test, the A5 Analog assembly's source outputs a signal that is connected to the input channels via the calibration path (CALP). For the A1 Input assembly's channel 1, power spectrum measurements are made with the signal routed through the 100 kHz anti-alias filter, the 50 kHz anti-alias filter, and the bypass circuit. For the A1 Input assembly's channel 2, power spectrum measurements are made with the signal routed through the 50 kHz anti-alias filter and the bypass circuit. For the A2 Input assembly's channel 1 or 2, power spectrum measurements are made with the signal routed through the 50 kHz anti-alias filter, the 25 kHz anti-alias filter, and the bypass circuit. For the A2 Input assembly's channel 3 or 4, power spectrum measurements are made with the signal routed through the 25 kHz anti-alias filter and the bypass circuit.

[ADC GATE ARRAY] This test verifies that the A5 Analog assembly's ADC gate array is functioning correctly. This test consists of 7 tests — positive overflow, negative overflow, positive limit, negative limit, 1st pass, 2nd pass, and zero. The positive and negative overflow tests set up the ADC test mode to cause positive and negative overflows, then check the A6 Digital assembly's digital filter for interrupt flags. The positive and negative limit tests check the ADC's positive and negative limits. The 1st and 2nd pass tests connect the calibration signal from the A5 Analog assembly to the A1 Input assembly or A2 Input assemblies. The 1st pass test sets the 2nd pass result to zero and checks the signal into the ADC for the proper value and the A6 Digital assembly's gate array for interrupts or overloads. The 2nd pass test sets the 1st pass result to zero and checks the signal into the ADC for the proper value and the A6 Digital assembly's gate array for interrupts or overloads. The zero test checks for minimal output while the gate array outputs zero data.

[BASEBAND] This test verifies that the A6 Digital assembly's gate arrays are operating correctly. The trigger gate array provides dc input data. The signal is then measured at 0 Hz for 63.58 Vpk ±0.635V and from 4 Hz to 1.6 kHz for 0 Vpk ±0.06358V.

[DGTL SRCE THRU DSP] This test verifies that the A6 Digital assembly's gate arrays and digital source are operating correctly. In this test, the digital source outputs a periodic chirp to the gate arrays. The resultant spectrum is then checked from 384 Hz to 51.2 kHz.

[DIGITAL FILTER] This test verifies that the digital filter's gate array on the A6 Digital assembly is operating correctly. The A7 CPU assembly's microprocessor configures the digital filter's gate array over the fast bus. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. This test also writes to and reads from the gate array's RAM, checking for stuck bits. The Trigger Gate Array test [TRIGGER] and the LO Gate Array test [LO] must pass for this test to pass. No data paths on the A6 Digital assembly are checked.

[DISK CONTROLLR] This test verifies that the disk controller on the A7 CPU assembly is operating correctly. In this test, the microprocessor sends a series of writes to and reads from the disk controller.

[DISK FIFO] This test verifies that the disk controller's FIFO on the A7 CPU assembly is operating correctly. In this test, the CPU assembly's microprocessor writes 2048 pseudo-random bytes to the disk FIFO. The microprocessor then reads the disk FIFO.

[DISTORTN] This test checks for noise and distortion in the input circuits of the A1 Input assembly or A2 Input assemblies. In this test, the A5 Analog assembly's source outputs a signal that is connected to the input channels via the calibration path (CALP). For each channel in the A1 Input assembly, the signal is measured at 16.640 kHz for 5 Vpk ±0.5 Vpk and from 24.96 kHz to 51.2 kHz for 0 Vpk ±0.01V. For each channel in the A2 Input assemblies, the signal is measured at 8.320 kHz for 5 Vpk ±0.5 Vpk and from 12.48 kHz to 25.6 kHz for 0 Vpk ±0.01V.

[FAST BUS] This test verifies that the fast bus is operating correctly. In this test, the microprocessor on the A7 CPU assembly writes data to the trigger gate array and digital tach on the A6 Digital assembly over the fast bus. The microprocessor then reads the data.

[FIFO] This test verifies that the FIFO gate array on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the FIFO gate array. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. The Trigger Gate Array [TRIGGER], Digital Filter Gate Array [FILTER], and LO Gate Array [LO] tests must pass for this test to pass. No data paths on the Digital assembly are checked.

[FRONT PANEL] This test verifies that the IIC controller on the A11 Keyboard Controller assembly is operating correctly. In this test, the microprocessor on the A7 CPU assembly reads the IIC controller on the Keyboard Controller assembly and verifies that no front-panel keys are held down.

[GPIB CONNECTOR] This test was not implemented.

[GPIB FUNC TEST] This test verifies that the GPIB interface on the A10 Rear Panel assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor sets the GPIB interface to a listen only state, then tests for a listen only state.

[IIC BUS] This test verifies that the A7 CPU assembly can write to and read from all assemblies with IIC interfaces. This test also checks the A7 CPU assembly's EEROM. The following assemblies have IIC interfaces:

A1 Input
A2 Input
A5 Analog
A6 Digital
A8 Memory
A10 Rear Panel
A11 Keyboard Controller

[INPUT A-WEIGHT] This test verifies that the A-weight filters on the A1 Input assembly or A2 Input assemblies are operating correctly. In this test, the A5 Analog assembly's source outputs a chirp signal that is connected to the input channels via the calibration path (CALP). For each channel, the power spectrum is measured at three frequencies with and without the A-weight filter in the input path.

[INPUT ICP] This test verifies that the ICP sources on the A1 Input assembly or A2 Input assemblies are operating correctly. In this test, the ICP sources are turned on, then measured for 25 ±10 Vdc. During this test, the front panel input BNC connectors must not be connected to anything.

[INPUT TRIGGER] This test checks the trigger-level circuits on the A5 Analog assembly for both positive and negative slope triggering. In this test, the A5 Analog assembly's source outputs a 512 Hz, 5 Vpk signal that is connected to the input channels via the calibration path (CALP).

[INTERRUPT] This test verifies that the interrupt circuits on the A7 CPU assembly are operating correctly. In this test, the microprocessor writes to the multi-function peripheral interrupt registers and reads the registers for verification. This test does not actually set up an interrupt but does test the multi-function peripheral in greater depth than the [MULTI FCTN PERIPHERL] test.

[LO] This test verifies that the local oscillator gate array on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the local oscillator gate array. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. The microprocessor then checks the phase of its internal oscillator. The Trigger Gate Array [TRIGGER] test must pass for this test to pass. No data paths on the A6 Digital assembly are checked.

[LONG CONF TEST] This test performs most of the self tests. The tests are performed in the following order:

[INTERRUPT]
[MULTI FCTN PERIPHERL]
[FRONT PANEL]
[GPIB FUNC TEST]
[DISK CONTROLLR]
[DISK FIFO]
[IIC BUS]
[FAST BUS]
[TRIGGER]
[LO]
[DIGITAL FILTER]
[FIFO]
[BASEBAND]
[ZOOM]
[DGTL SRCE THRU DSP]
[SOURCE LO]
[SOURCE TO CPU]
[WITHOUT LO]
[WITH LO]
[ADC GATE ARRAY]
[OFFSET]
[DISTORTN]
[INPUT TRIGGER]
[INPUT A-WEIGHT]
[AAF BYPASS]
[QUICK CONF TEST]

[MULTI FCTN PERIPHERL] This test verifies that the multi-function peripheral on the A7 CPU assembly is operating correctly. In this test, the microprocessor writes to the multi-function peripheral, then reads the registers checking for errors. Further testing of the multi-function peripheral is done by the [INTERRUPT] test.

[OFFSET] This test verifies that the analyzer can correct for dc offsets generated by the input circuits on the A1 Input assembly or A2 Input assemblies. In this test, the input circuits are connected to ground. For the A1 Input assembly's channel 1, time record measurements are taken with the signal routed through the 100 kHz anti-alias filter and through the 50 kHz anti-alias filter with the dc offset DAC set to 127, then to –127. For the A1 Input assembly's channel 2, time record measurements are taken with the signal routed through the 50 kHz anti-alias filter with the dc offset DAC set to 127, then to –127. For the A2 Input assembly's channel 1 or 2, time record measurements are taken with the signal routed through the 50 kHz anti-alias filter and through the 25 kHz anti-alias filter with the dc offset DAC set to 127, then to –127. For the A2 Input assembly's channel 3 or 4, time record measurements are taken with the signal routed through the 25 kHz anti-alias filter with the dc offset DAC set to 127, then to –127.

[QUICK CONF TEST] This test calibrates the analyzer and checks the calibration limits. Any calibration errors are entered in the Test Log. See "Calibration Routine Description" earlier in this chapter for a description of the calibration routine.

[RANDOM SEEK] This test verifies that the A100 Disk Drive assembly's head can move to a random sector on the flexible disk. In this test, the disk controller on the A7 CPU assembly instructs the disk-drive head to move to a random record. This test requires a formatted flexible disk.

[READ] This test verifies that the A100 Disk Drive assembly can read a flexible disk. In this test, the A7 CPU assembly's disk controller instructs the Disk Drive assembly to read the current record on the flexible disk. While the current record is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The current record is set by the [SEEK RECORD] test. This test requires a formatted flexible disk.

[READ/WRITE] This test verifies that the A100 Disk Drive assembly can read and write to a flexible disk. In this test, the A7 CPU assembly's disk controller instructs the Disk Drive assembly to read the current record on the flexible disk. While the current record is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to the current record. While the current record is being written to, the disk controller monitors the WDATAn signal to verify the write operation. The current record is set by the [SEEK SECTOR] test. This test requires a formatted flexible disk that is not write protected.

[READ/WRITE ALL] This test verifies that the A100 Disk Drive assembly can read and write to all records of a flexible disk. In this test, the A7 CPU assembly's disk controller instructs the Disk Drive assembly to read every available record on the flexible disk (excluding privileged tracks). While the flexible disk is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to every available record on the flexible disk (excluding privileged tracks). While the flexible disk is being written to, the disk controller monitors the WDATAn signal to verify the write operation. This test stops on the first error. The execution time for this test depends upon the size of the disk. For example, if there are no errors, this test takes approximately one hour for a double-sided, low-density disk. This test requires a formatted flexible disk that is not write protected.

[RESTORE] This test verifies that the A100 Disk Drive assembly's head can move away from track 0, then back to track 0. In this test, the A7 CPU assembly's disk controller instructs the disk-drive head to move away from track 0, then back to track 0. The disk controller monitors the T00n signal to verify the move operation. This test requires a formatted flexible disk.

[SERIAL PORT] This test verifies that the RS-232 interface on the A7 CPU assembly is capable of sending and receiving data. In this test, the user connects the transmit data line to the recieve data line. Data is sent out on the transmit data line and read back on the receive data line.

[SEEK RECORD] This test verifies that the A100 Disk Drive assembly's head can move to a user specified record on the flexible disk. In this test, the disk controller on the A7 CPU assembly instructs the disk-drive head to move to a user specified record. The user specified record number must be in the range of valid record numbers. The default record number is 0. This test requires a formatted flexible disk.

[SOURCE LO] This test verifies that the local oscillator (LO) gate array on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the LO gate array and reads its control lines to check circuits internal to the gate array and verify correct configuration. No data paths on the Digital assembly are checked.

[SOURCE TO CPU] This test verifies that the core of the digital source on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the digital source to output a 12.8 kHz chirp. The microprocessor then reads the final chirp value in the digital-source RAM. This test does not use the time record to verify the chirp.

[TACHOMETR] This test verifies that the tachometer circuits on the A10 Rear Panel assembly and A6 Digital assembly are operating correctly. In this test, a BNC cable must be connected from the source connector to the tachometer connector. The tachometer pulses are counted for 200 milliseconds with the source turned off. The count should be zero. Next the source is set to 100 Hz, 3.53 Vrms and the tachometer pulses are counted for another 200 milliseconds. This time the count should be 20 ±1.

[TRIGGER] This test verifies that the trigger gate array on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the trigger gate array. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. This test also verifies functions internal to the gate array such as internal trigger level, trigger interrupts, overload interrupts, and post trigger delay.

[WITH LO] This test verifies the capability of the A5 Analog assembly's analog source to output a flat zoomed periodic chirp signal. In this test, the A6 Digital assembly's local oscillator is used with the analog source to produce a zoomed periodic chirp signal. The signal is connected to the input channels via the calibration path (CALP). The flatness of the signal is measured from 13.6 kHz to 26.4 kHz.

[WITHOUT LO] This test verifies the capability of the A5 Analog assembly's analog source to output a flat baseband chirp signal. In this test, the Analog assembly's analog source outputs a baseband chirp signal (starting at 0 Hz) that is connected to the A1 Input assembly or A2 Input assemblies via the calibration path (CALP). The flatness of the signal is measured from 384 Hz to 51.2 kHz.

[ZOOM] This test checks most of the DSP chain, including the LO gate array. In this test, the Digital assembly's trigger gate array outputs a dc value to the DSP chain.

Self-Test Menu Map and GPIB Commands

The analyzer's self tests can be run from the front panel or by a controller via GPIB. To run a test from the front panel, press [**System Utility**] followed by the appropriate softkey in the table. To run a test via GPIB, send the equivalent GPIB command (to abort a test, send TEST:ABOR).

To view the analyzer's fault log via GPIB, send DISP:CONT FTAB. To clear the fault log send SYST:FLOG:CLE. To return to the top line of the test log and delete the line from the test log, send TEST:LOG:DATA:LINE?

The following table shows the softkeys and GPIB commands for each self test.

Self Test	GPIB Command
[SELF TEST]	–
[QUICK CONF TEST]	*TST?
[LONG CONF TEST]	TEST:LONG
[FUNCTIONL TESTS]	–
[DISPLAY PATTERN]	TEST:DISP:PATT ON | OFF
[I/O]	–
[FRONT PANEL]	TEST:IO:FPAN; *WAI
[GPIB]	–
[GPIB FUNC TEST]	TEST:IO:GPIB; *WAI
[GPIB CONNECTOR]	–
[INTERNAL DISK]	–
[DISK CONTROLLR]	TEST:IO:DISK:CONT; *WAI
[DISK FIFO]	TEST:IO:DISK:FIFO; *WAI
[RESTORE]	TEST:IO:DISK:REST; *WAI
[RANDOM SEEK]	TEST:IO:DISK:RAND; *WAI
[SEEK RECORD]	TEST:IO:DISK:SEEK n; *WAI †
[READ]	TEST:IO:DISK:READ; *WAI
[READ/WRITE]	TEST:IO:DISK:WRIT; *WAI
[READ/WRITE ALL]	TEST:IO:DISK:RWR; *WAI
[ALL]	TEST:IO:DISK:ALL; *WAI
[IIC BUS]	TEST:IO:IIC; *WAI
[FAST BUS]	TEST:IO:FBUS; *WAI
[SERIAL PORT]	TEST:IO:SER; *WAI
[ALL]	TEST:IO:ALL; *WAI

† where n = 0 to [(tracks per side x sides x sectors per track) –1]

Self Test	GPIB Command
[SELF TEST]	–
[FUNCTIONL TESTS]	–
[DIGITAL PROCESSOR]	–
[TRIGGER]	TEST:DSP:TRIG; *WAI
[LO]	TEST:DSP:LO; *WAI
[DIGITAL FILTER]	TEST:DSP:FILT; *WAI
[FIFO]	TEST:DSP:FIFO; *WAI
[BASEBAND]	TEST:DSP:BAS; *WAI
[ZOOM]	TEST:DSP:ZOOM; *WAI
[DGTL SRCE THRU DSP]	TEST:DSP:SOUR; *WAI
[ALL]	TEST:DSP:ALL; *WAI
[SOURCE]	–
[SOURCE LO]	TEST:SOUR:LO; *WAI
[SOURCE TO CPU]	TEST:SOUR:CPU; *WAI
[WITHOUT LO]	TEST:SOUR:BAS; *WAI
[WITH LO]	TEST:SOUR:ZOOM; *WAI
[ALL]	TEST:SOUR:ALL; *WAI
[INPUTS]	–
[OFFSET]	TEST:INP:OFFS; *WAI
[DISTORTN]	TEST:INP:DIST; *WAI
[INPUT TRIGGER]	TEST:INP:TRIG; *WAI
[INPUT A-WEIGHT]	TEST:INP:AWE; *WAI
[AAF BYPASS]	TEST:INP:AAF; *WAI
[INPUT ICP]	TEST:INP:ICP; *WAI
[ALL]	TEST:INP:ALL; *WAI
[TACHOMETR]	TEST:TACH; *WAI
[ADC GATE ARRAY]	TEST:ADC:GARR; *WAI
[OTHER]	–
[INTERRUPT]	TEST:PROC:INT; *WAI
[MULT FCTN PERIPHERL]	TEST:PROC:MFP; *WAI
[ALL]	TEST:PROC:ALL; *WAI
[ALL]	TEST:ALL; *WAI
[LOOP MODE ON/OFF]	TEST:LOOP:MODE ON|OFF
[TEST LOG]	DISP:CONT TTAB
[CLEAR TEST LOG]	TEST:LOG:CLE
[NEXT PAGE]	–
[PREVIOUS PAGE]	–

11

Backdating

Backdating

This chapter provides information necessary to modify this manual for instruments that differ from those currently being produced. The information in this chapter documents earlier instrument configurations and associated servicing procedures.

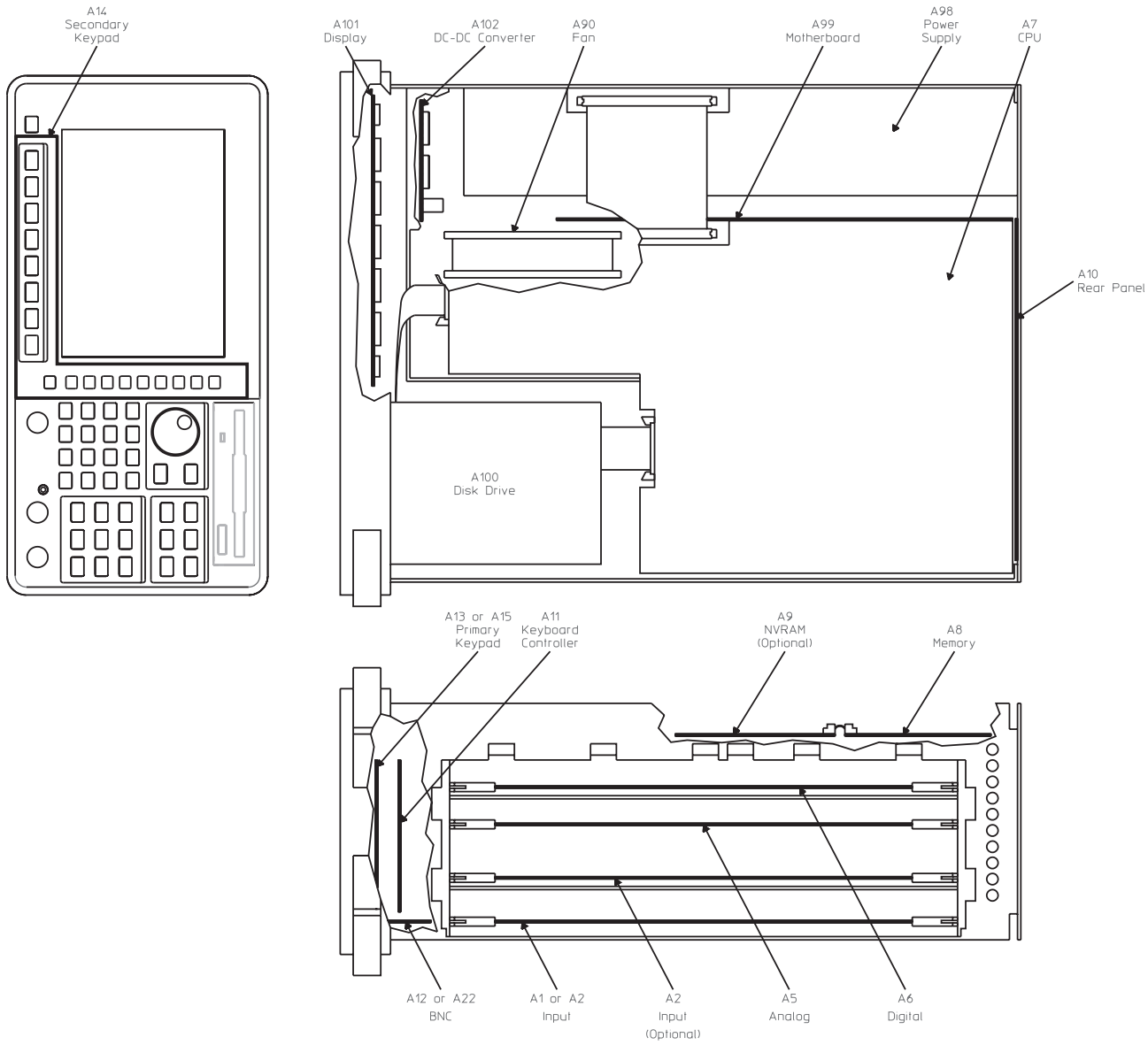
With the information provided in this chapter, this manual can be corrected so that it applies to any earlier version or configuration of the instrument.

12

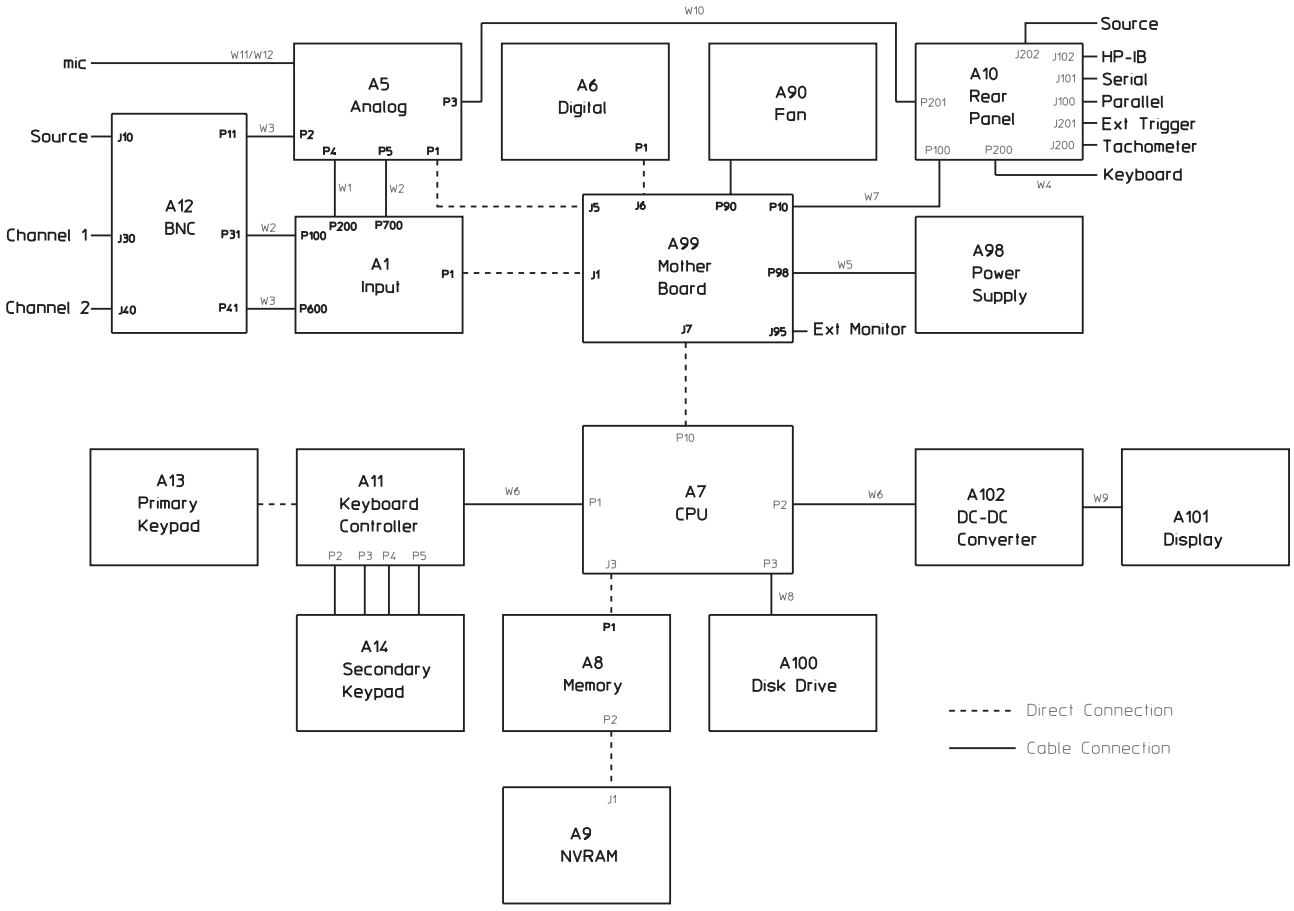
Quick Reference

Quick Reference

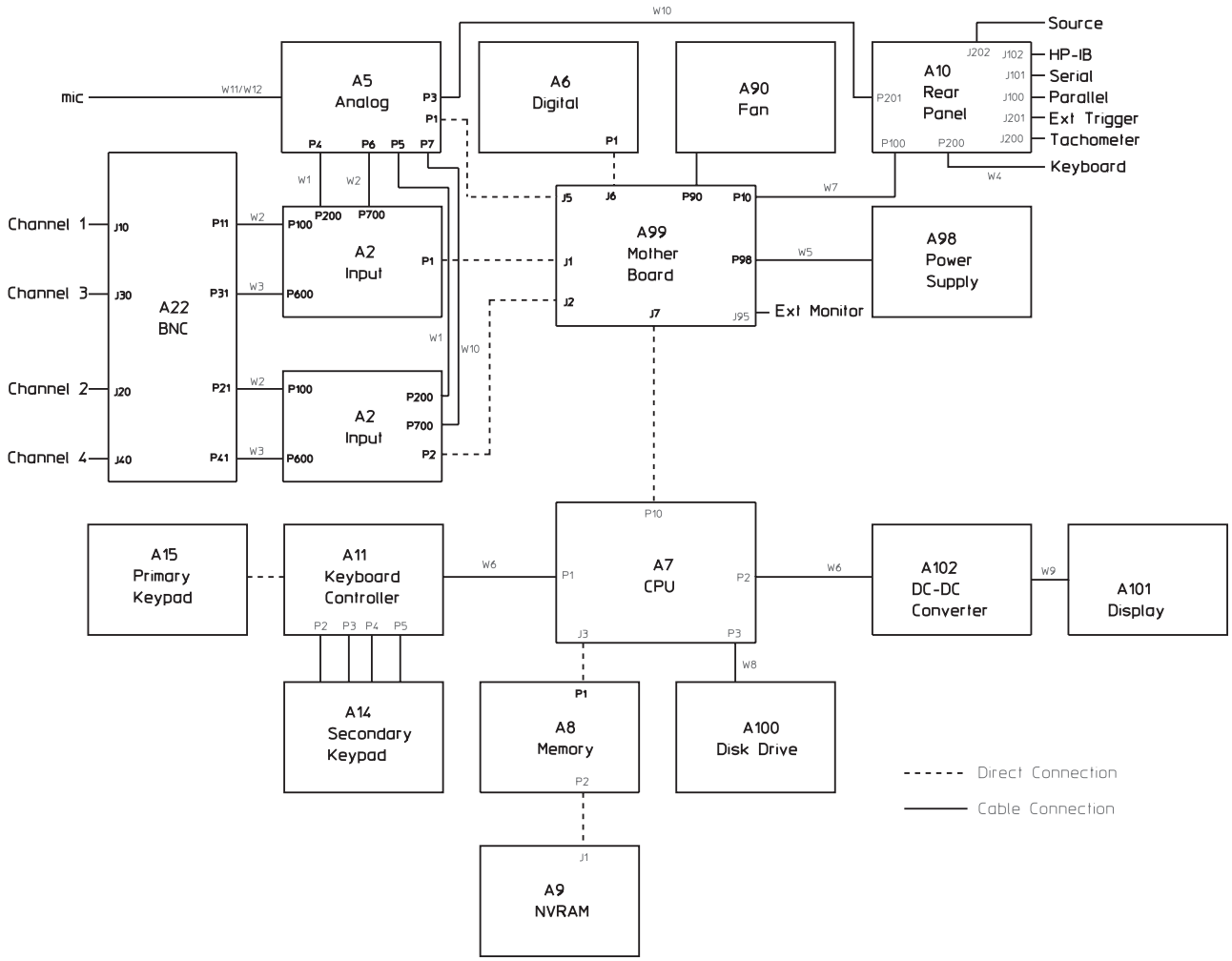
This chapter shows assembly locations, cable connections, and all the block diagrams for the Agilent 35670A Dynamic Signal Analyzer. All block diagrams, except the overall block diagrams, show the connector numbers for signals routed through RF cables. The block diagrams do not show connector numbers for signals routed through the analyzer's Motherboard assembly.



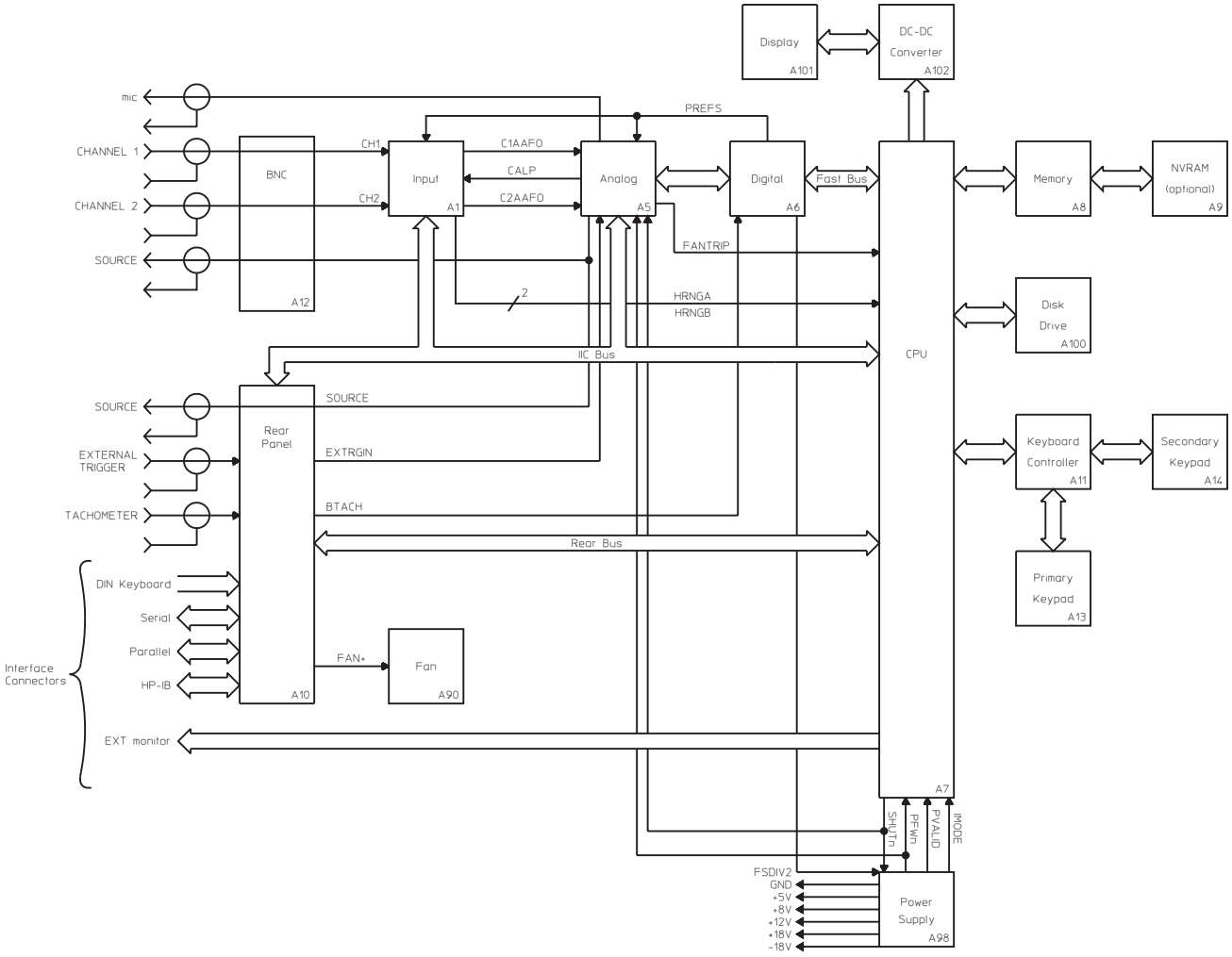
Assembly Locations



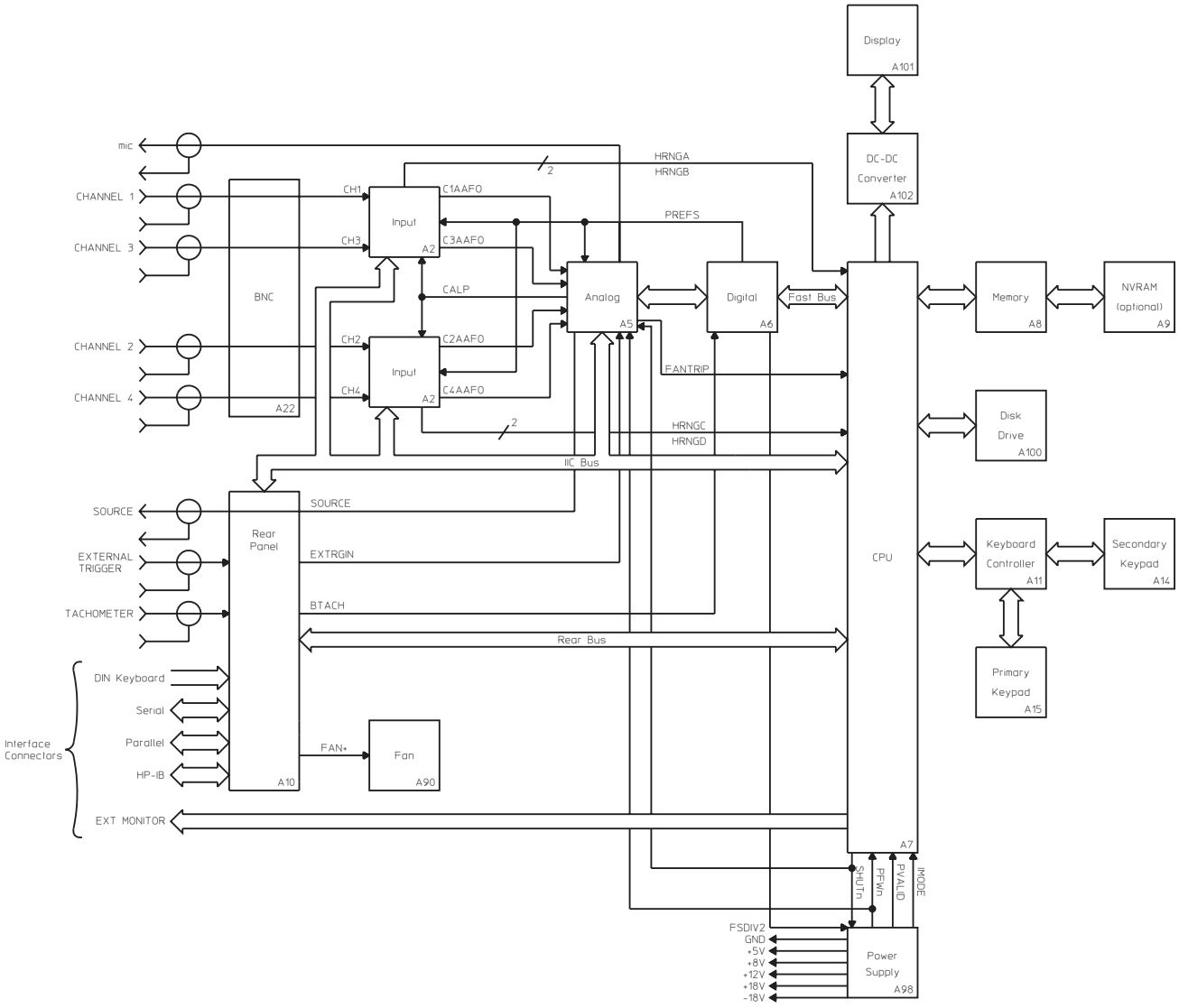
Assembly Connections for Two Channel Analyzer



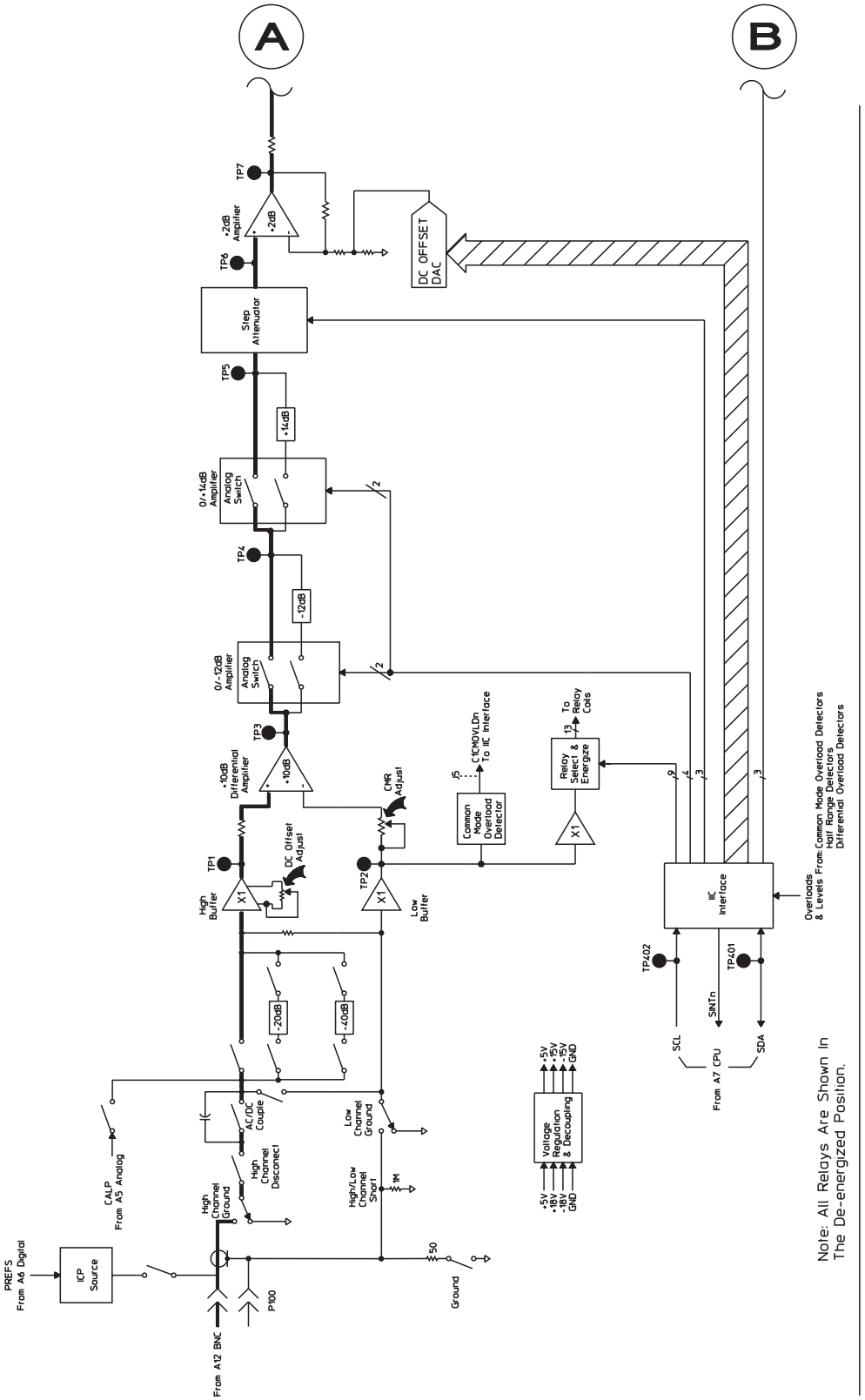
Assembly Connections for Four Channel Analyzer



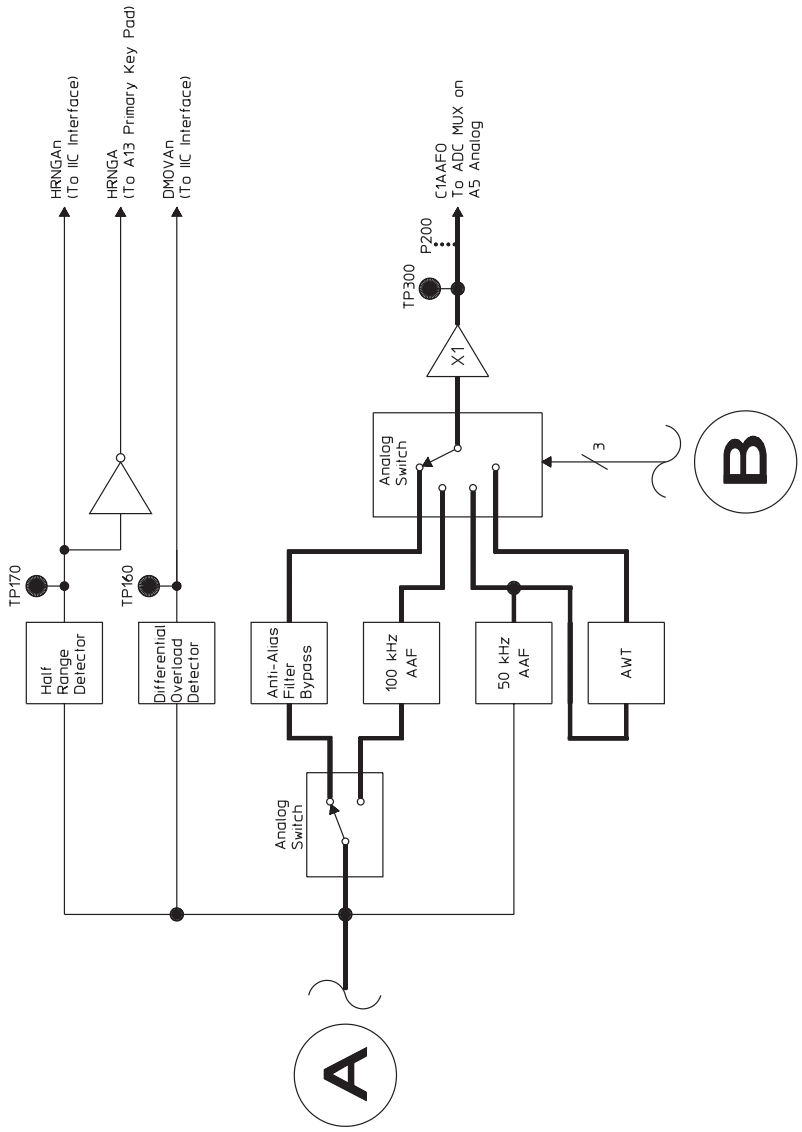
Two Channel Overall Block Diagram



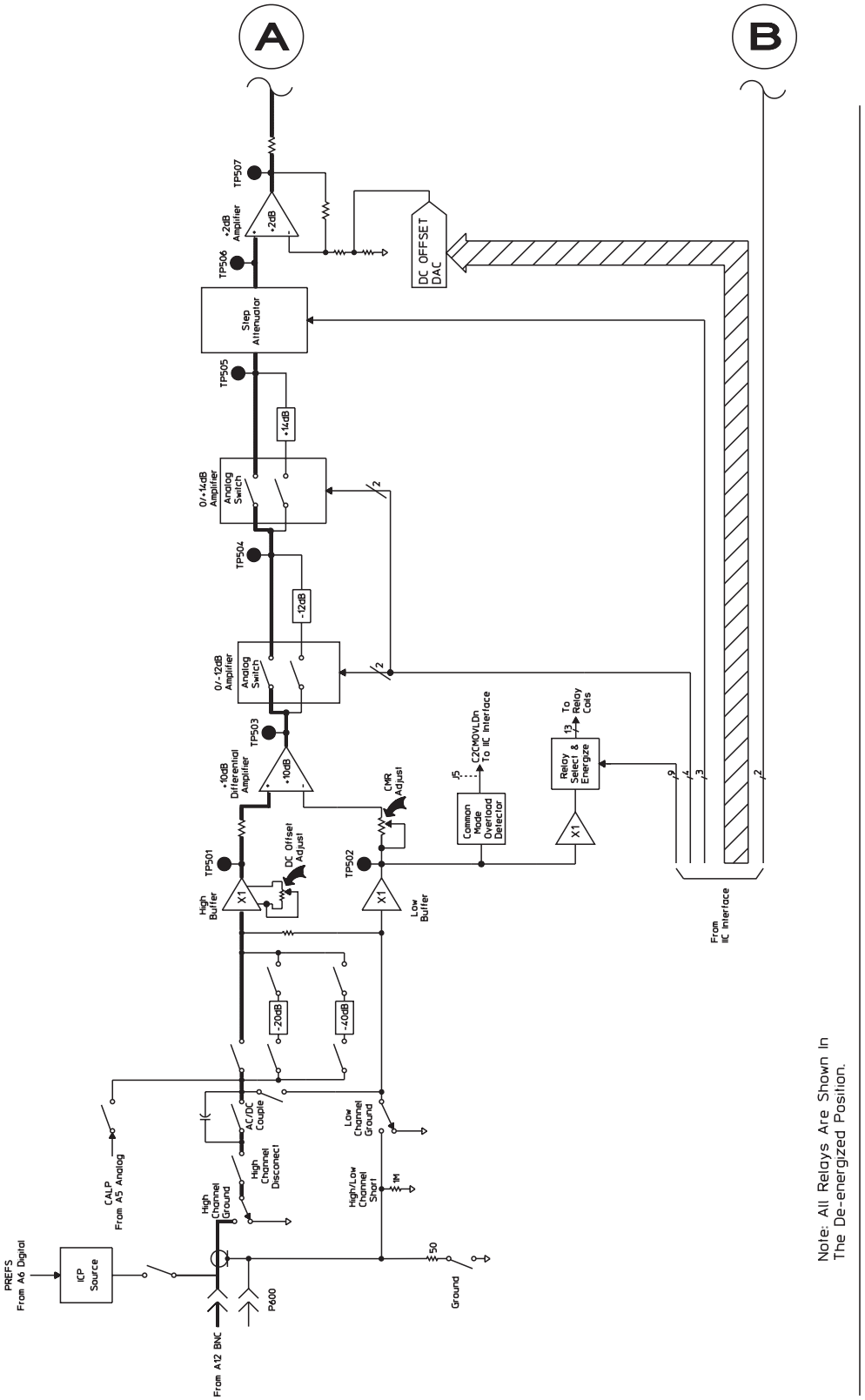
Four Channel Overall Block Diagram



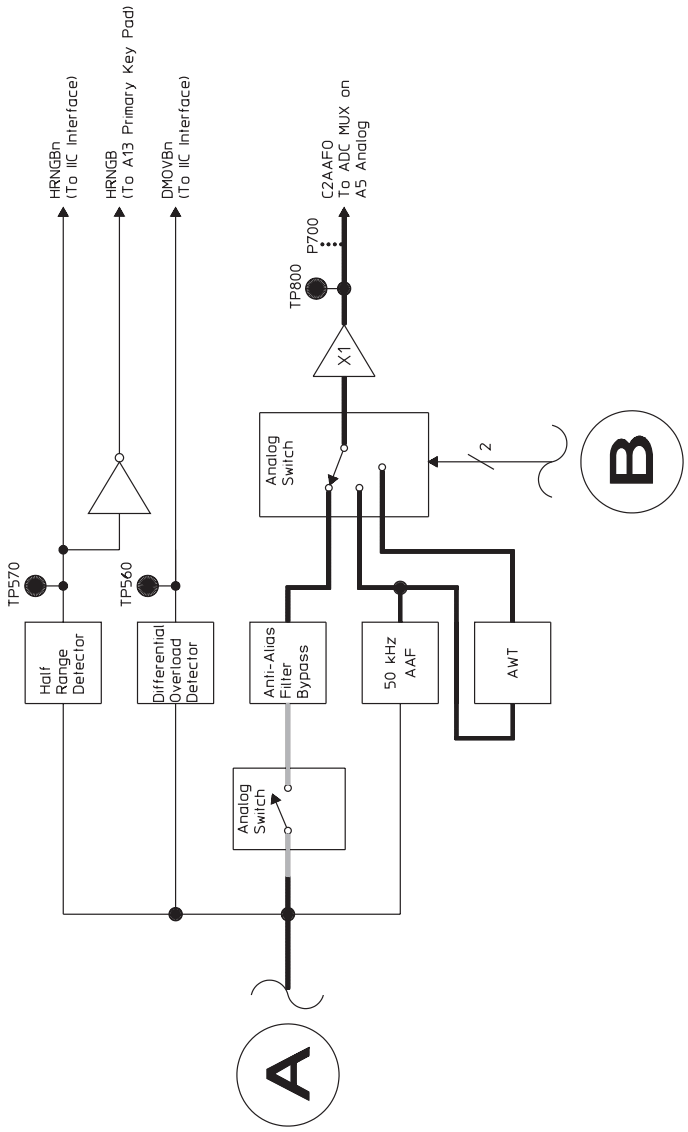
A1 Input Block Diagram: Channel 1



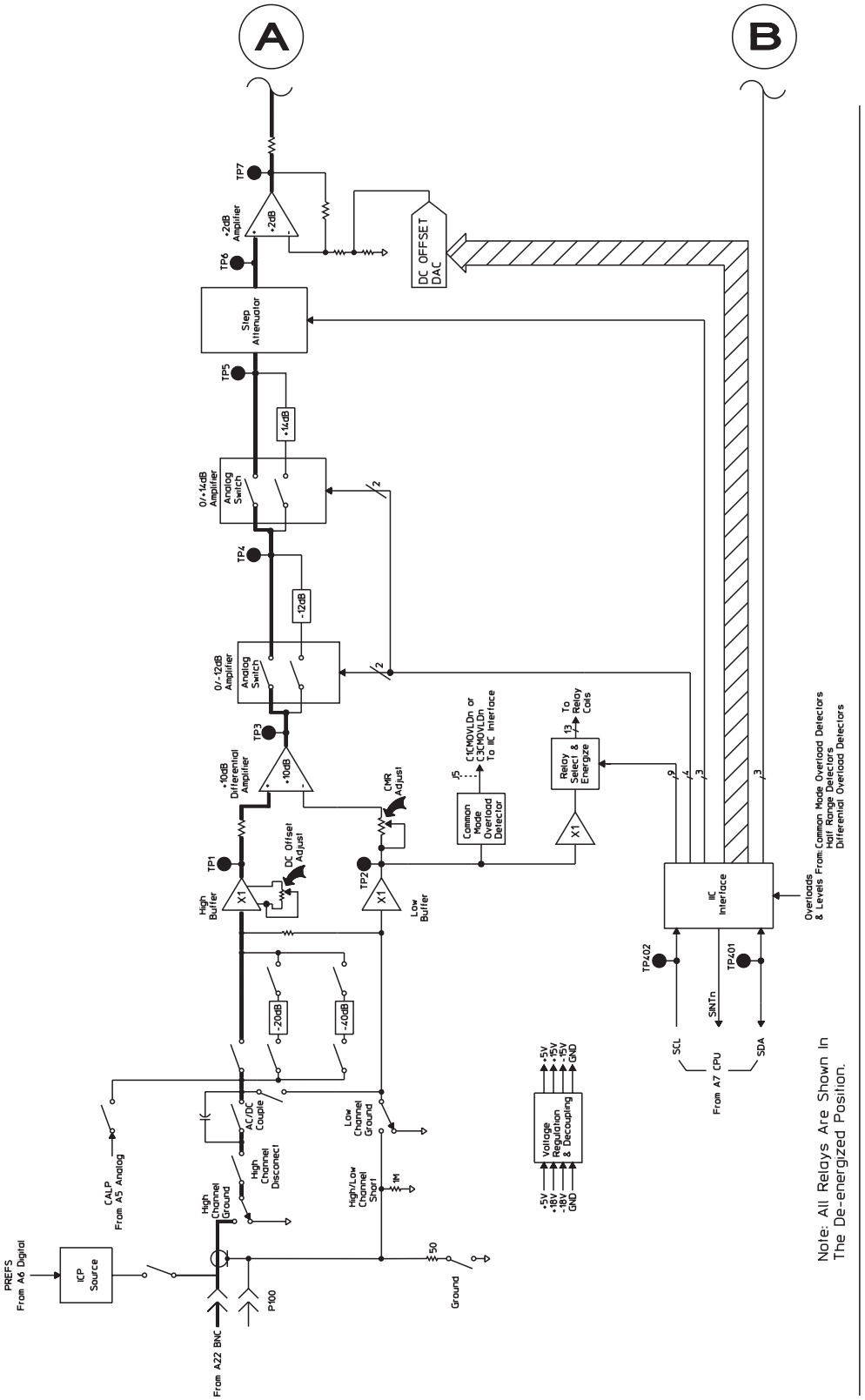
A1 Input Block Diagram: Channel 1 (continued)



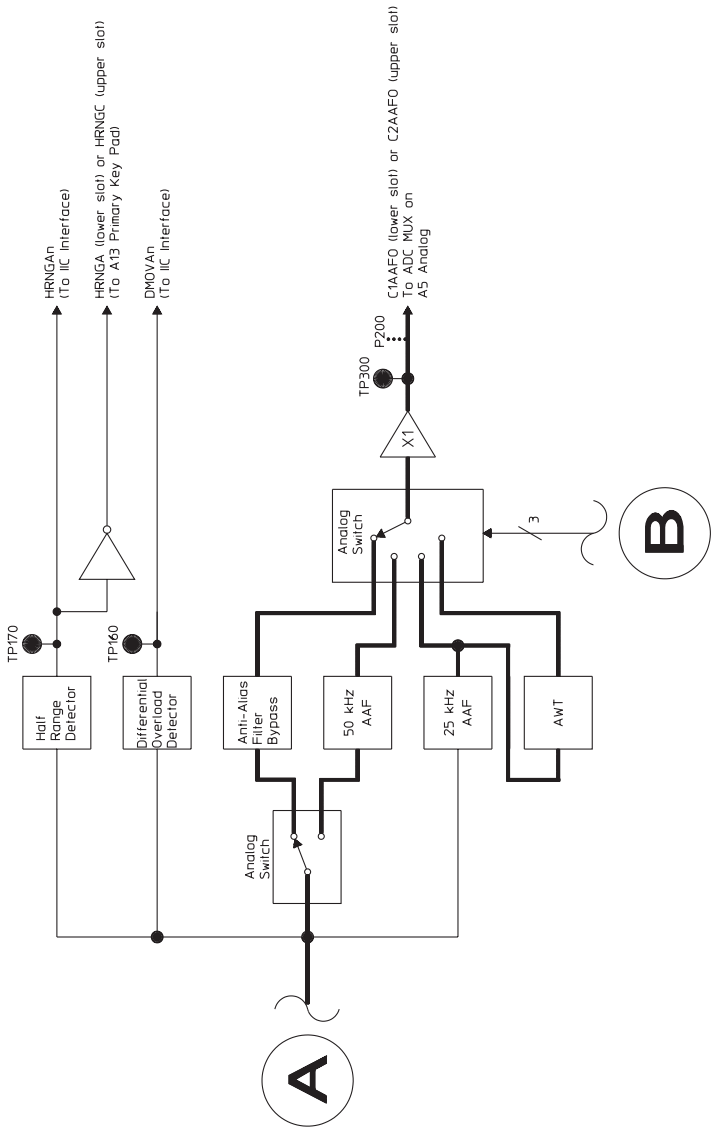
A1 Input Block Diagram: Channel 2



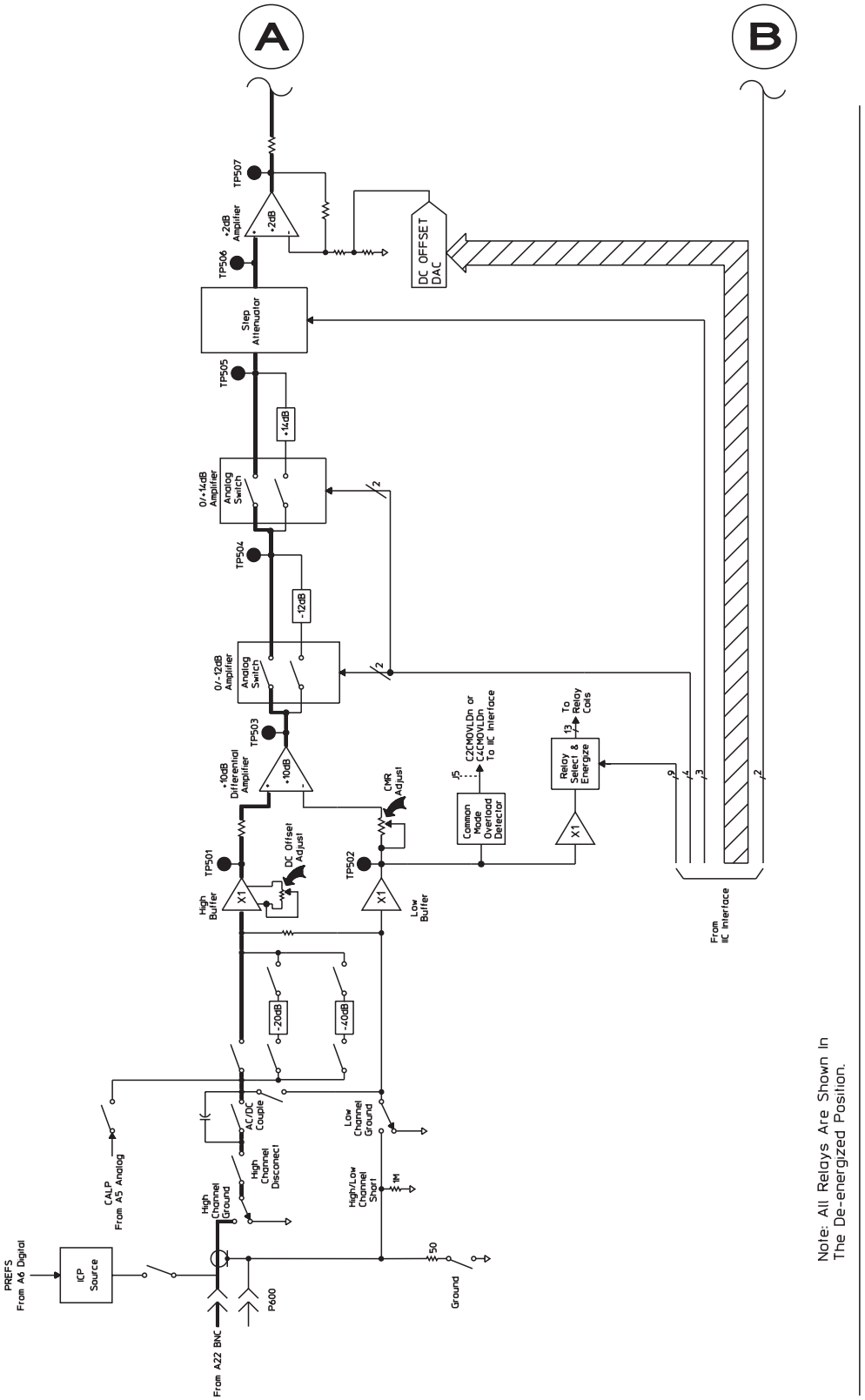
A1 Input Block Diagram: Channel 2 (continued)



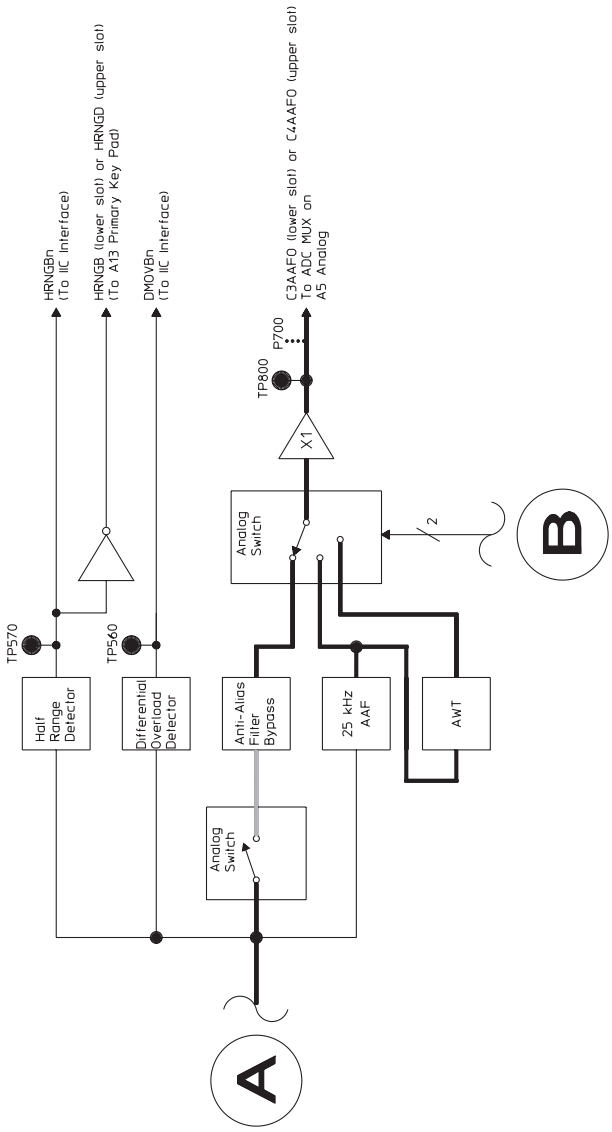
A2 Input Block Diagram: Channel 1 or Channel 3



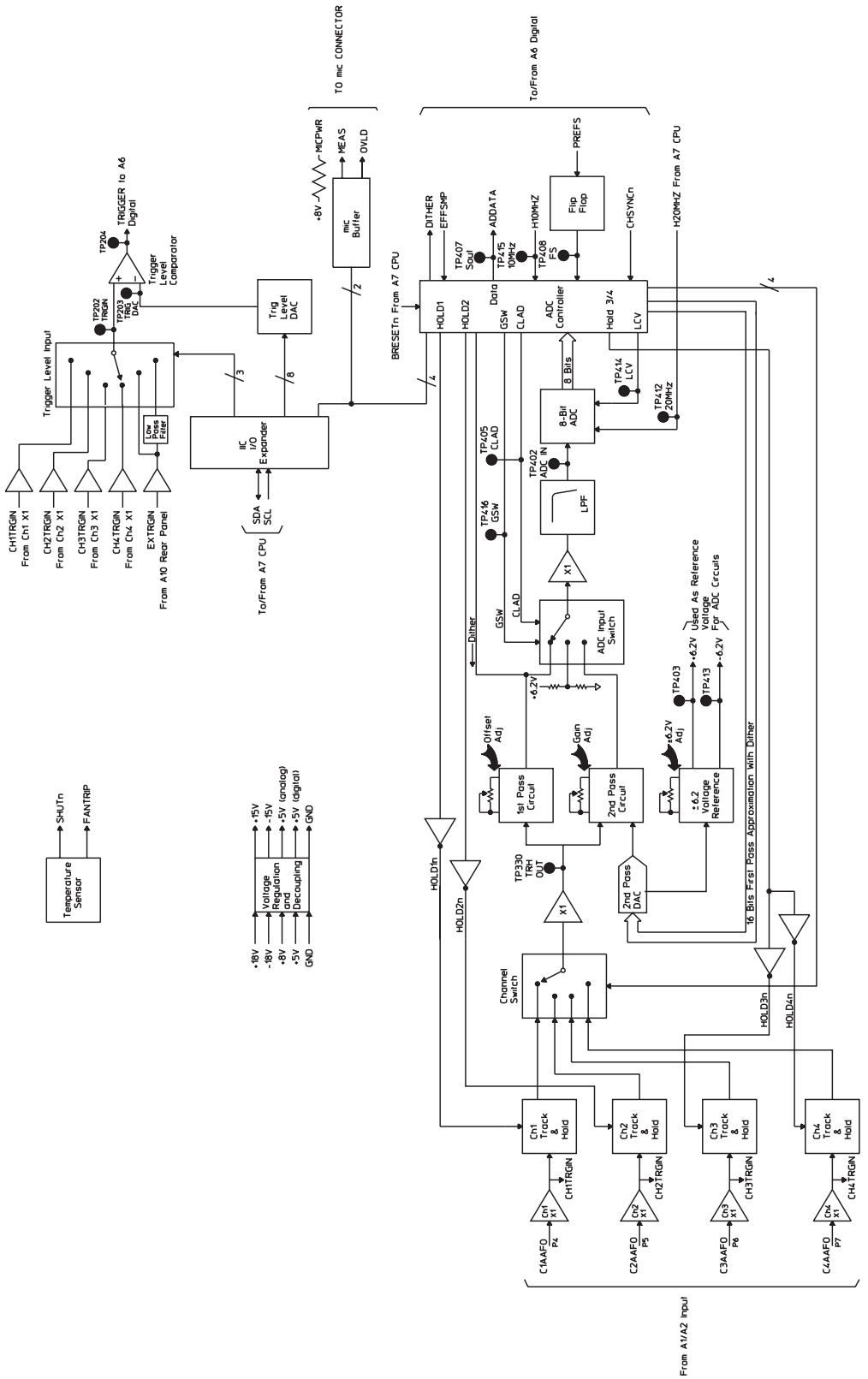
A2 Input Block Diagram: Channel 1 or Channel 3 (continued)



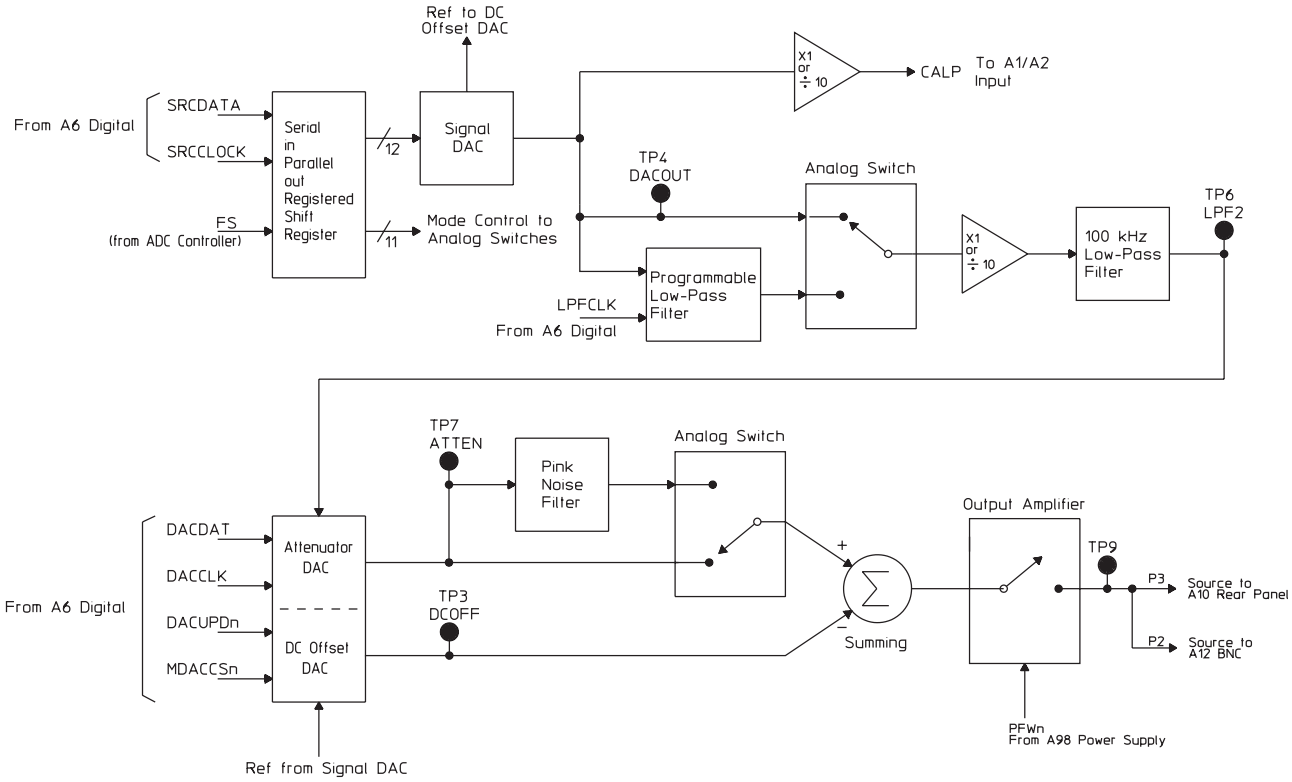
A2 Input Block Diagram: Channel 2 or Channel 4



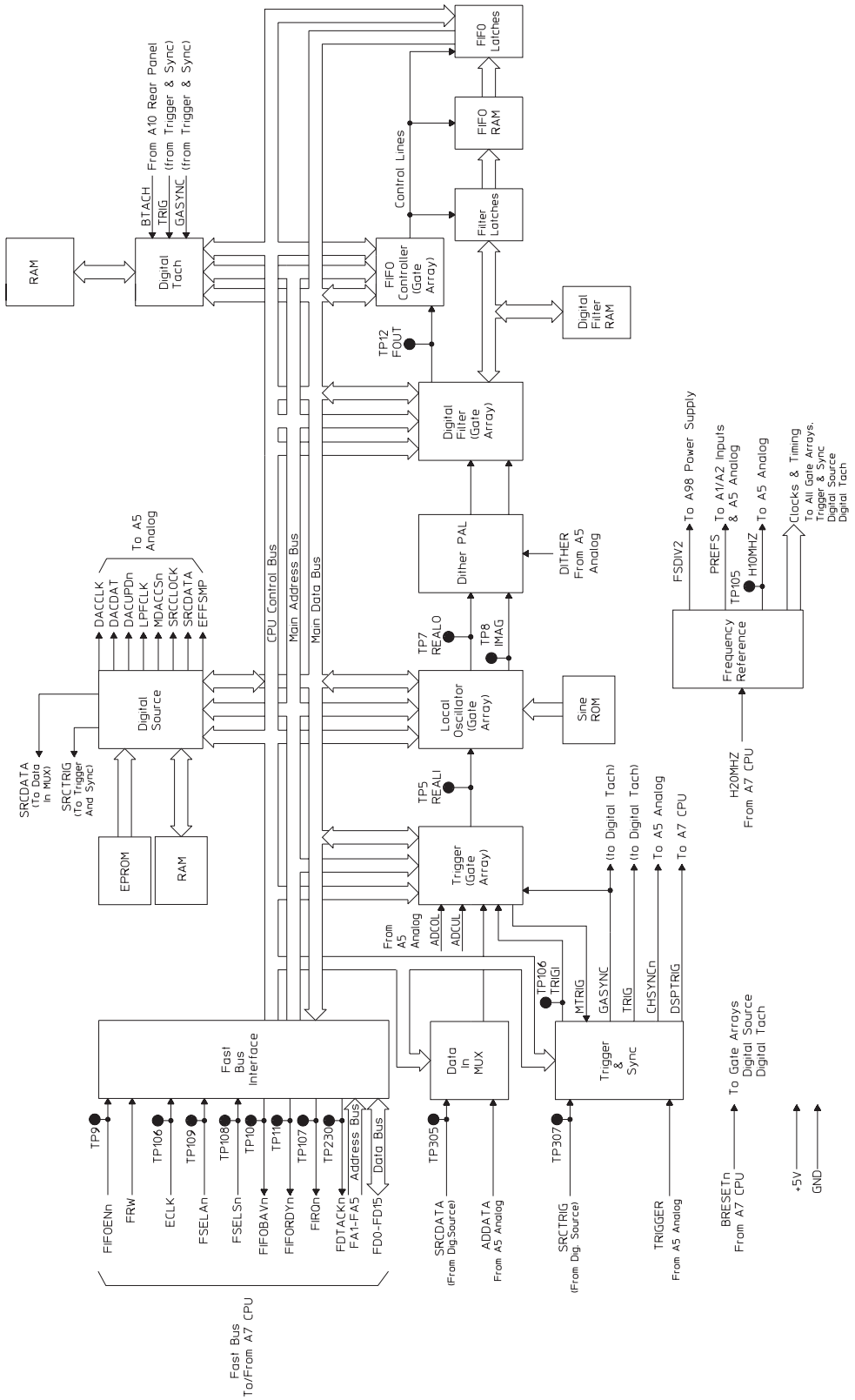
A2 Input Block Diagram: Channel 2 or Channel 4 (continued)



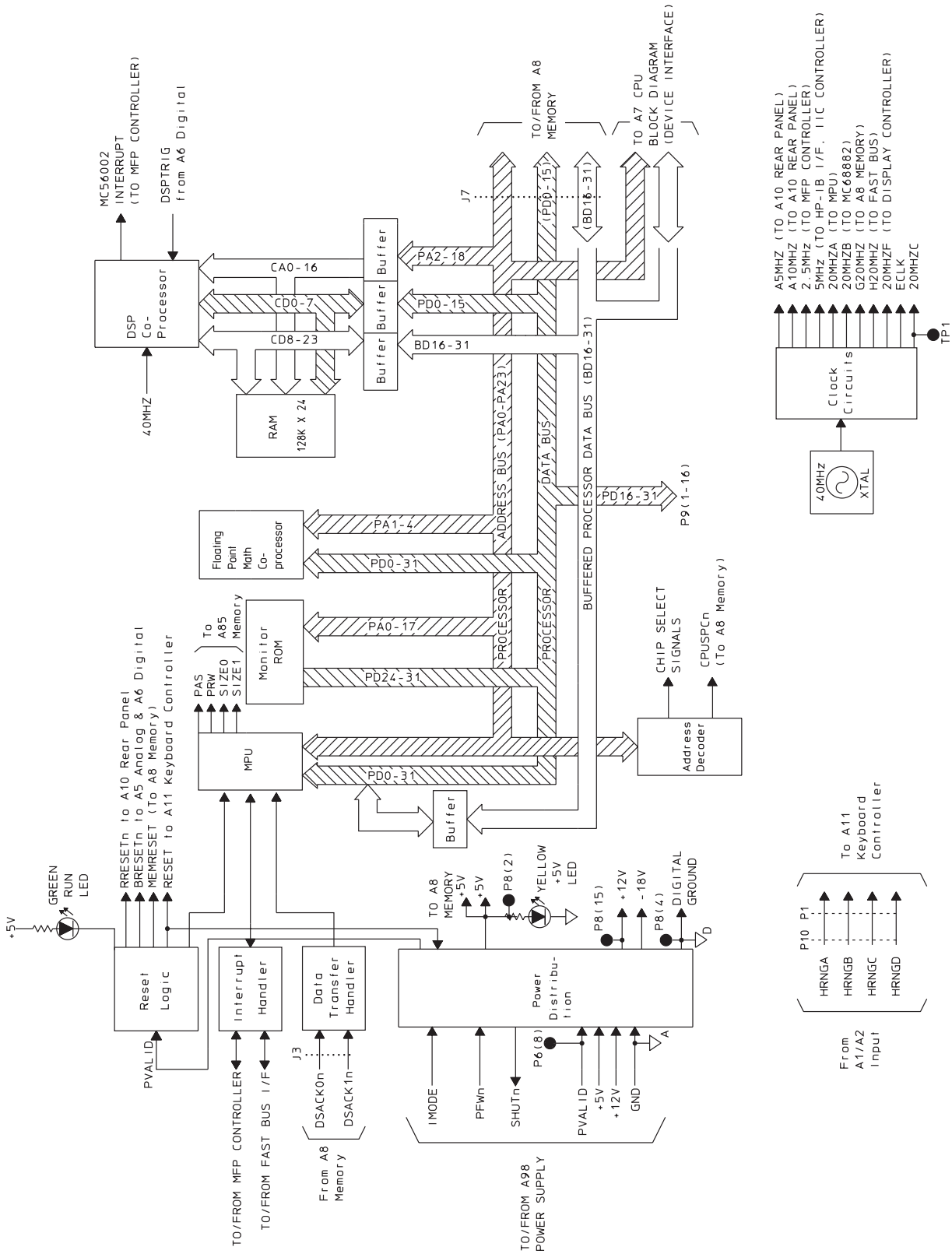
A5 Analog Block Diagram: ADC and Trigger



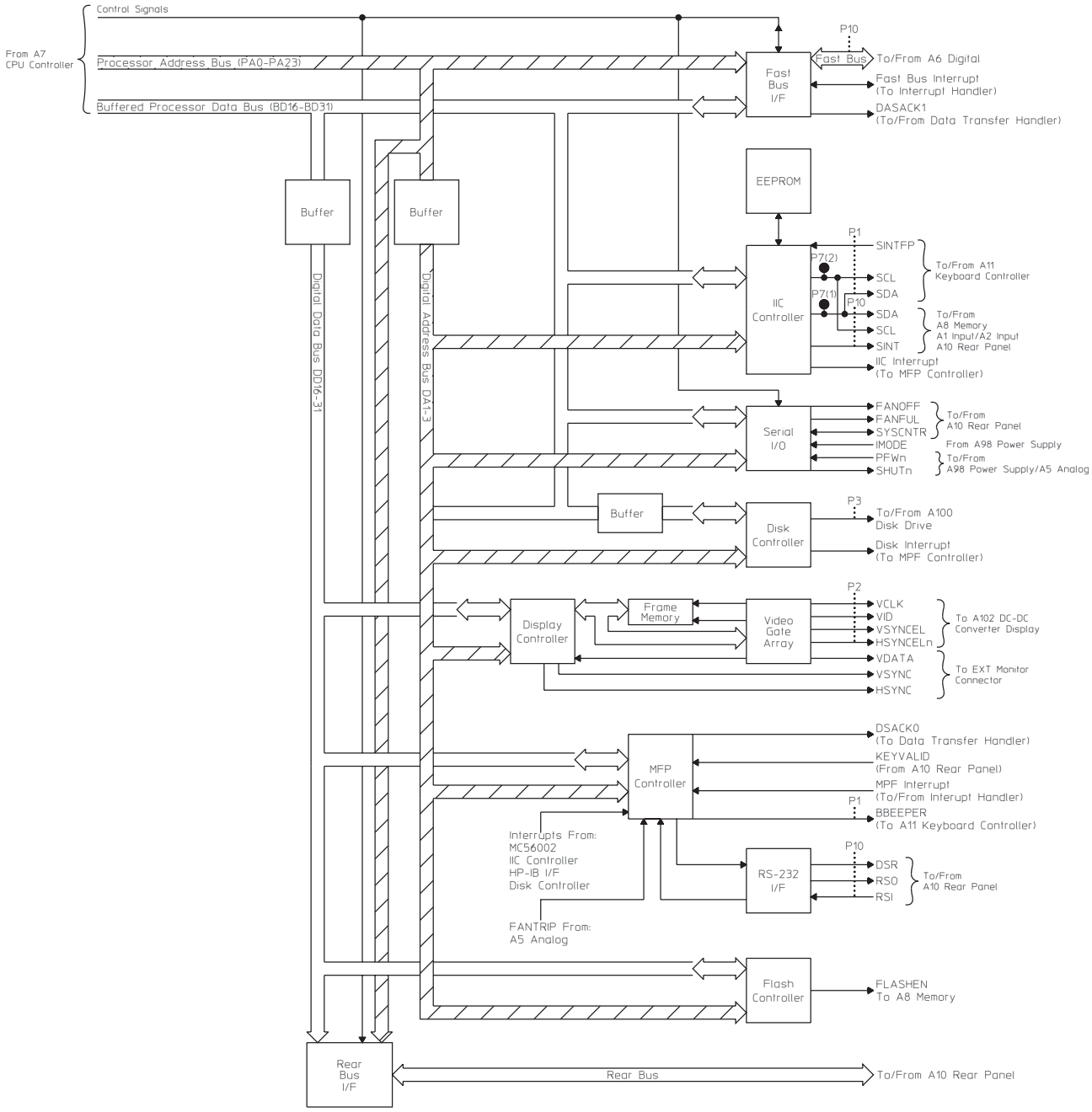
A5 Analog Block Diagram: Analog Source and Calibrator



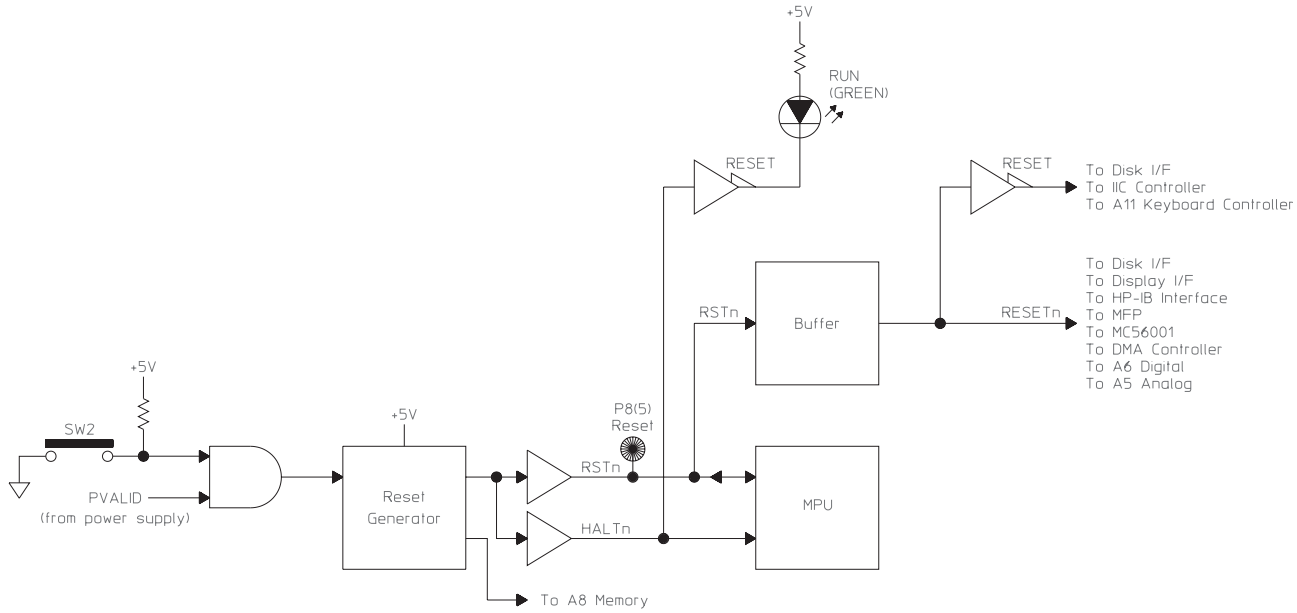
A6 Digital Block Diagram



A7 CPU Block Diagram



A7 CPU Block Diagram: Interface



Reset Logic

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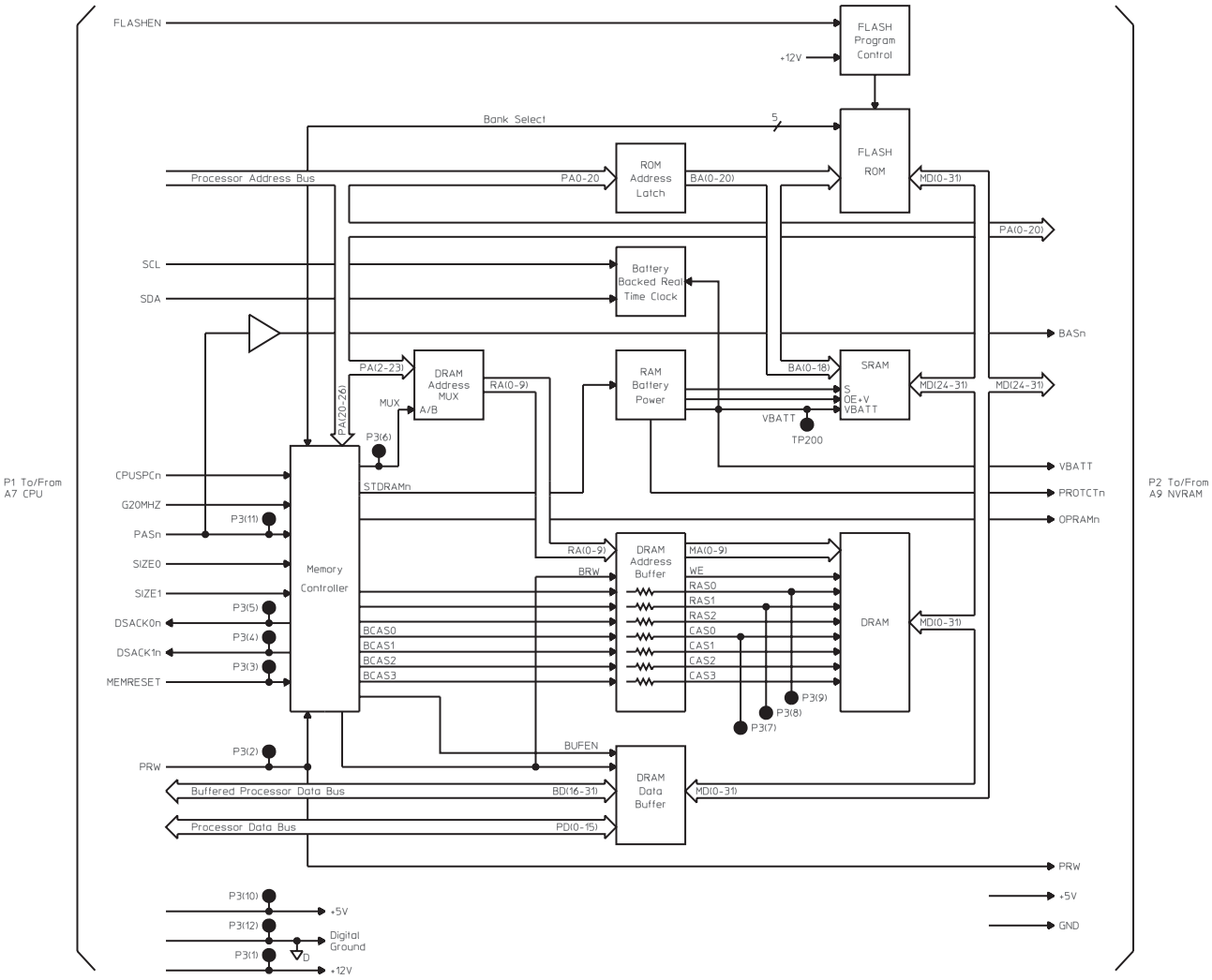
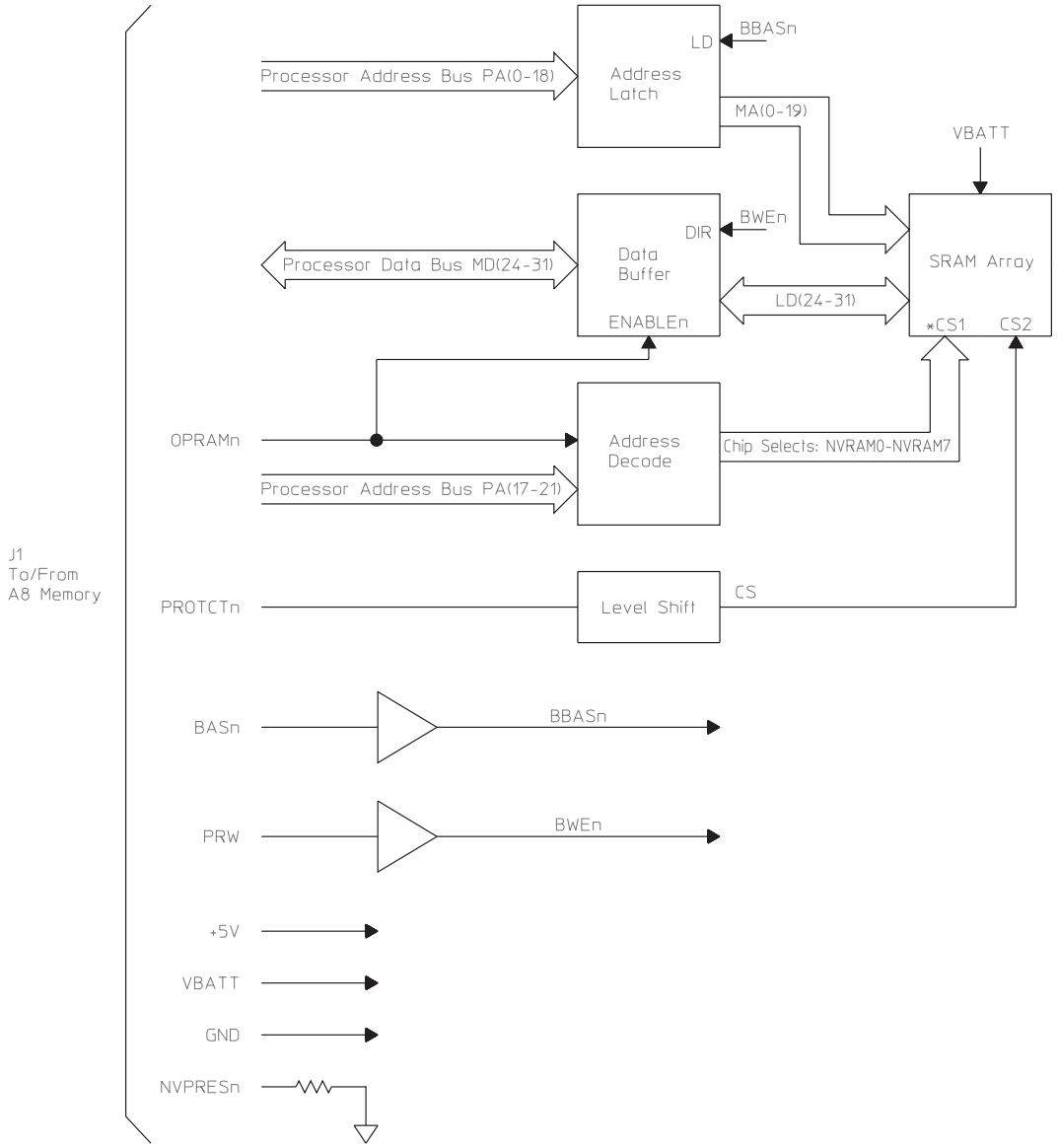
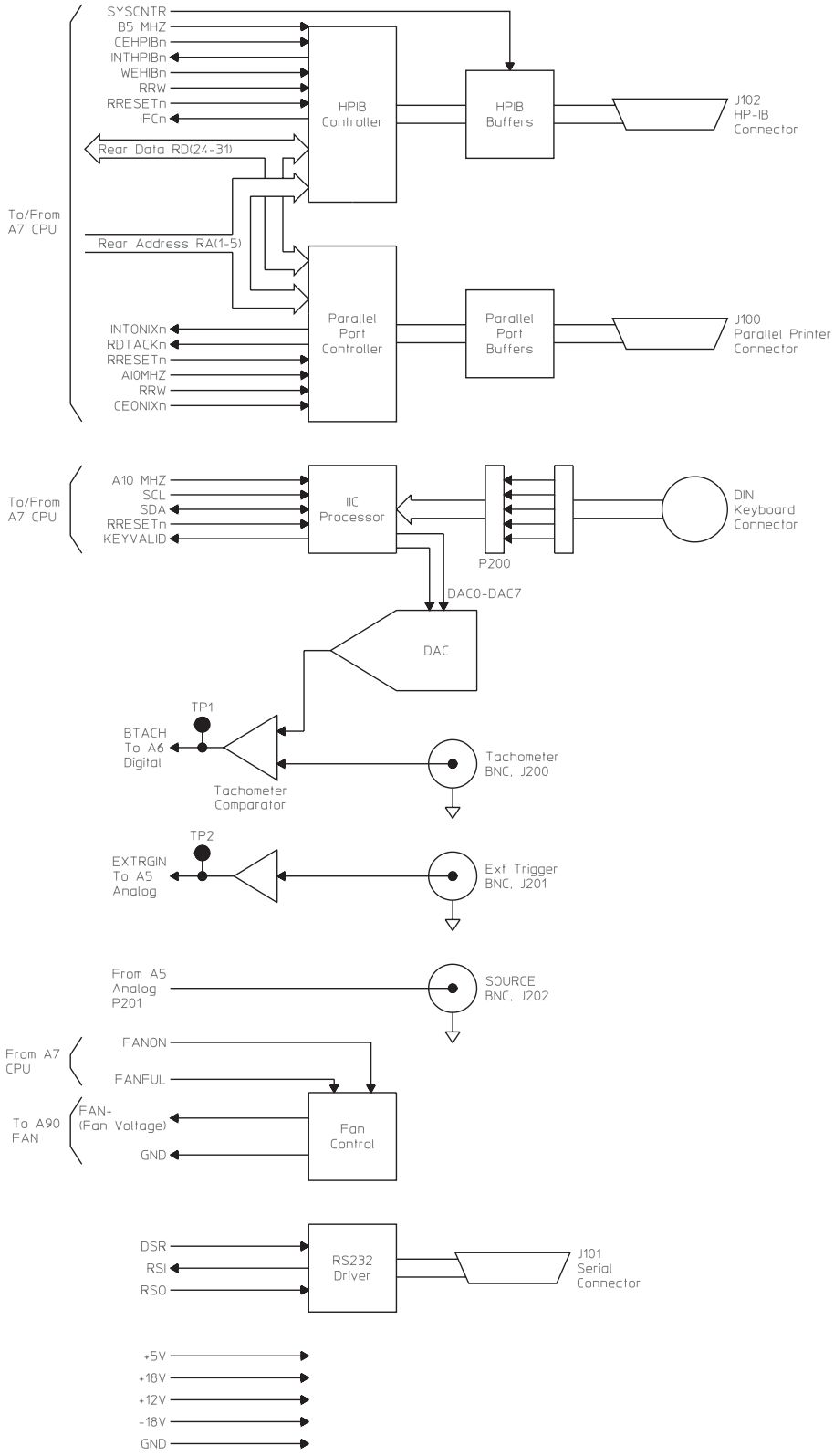


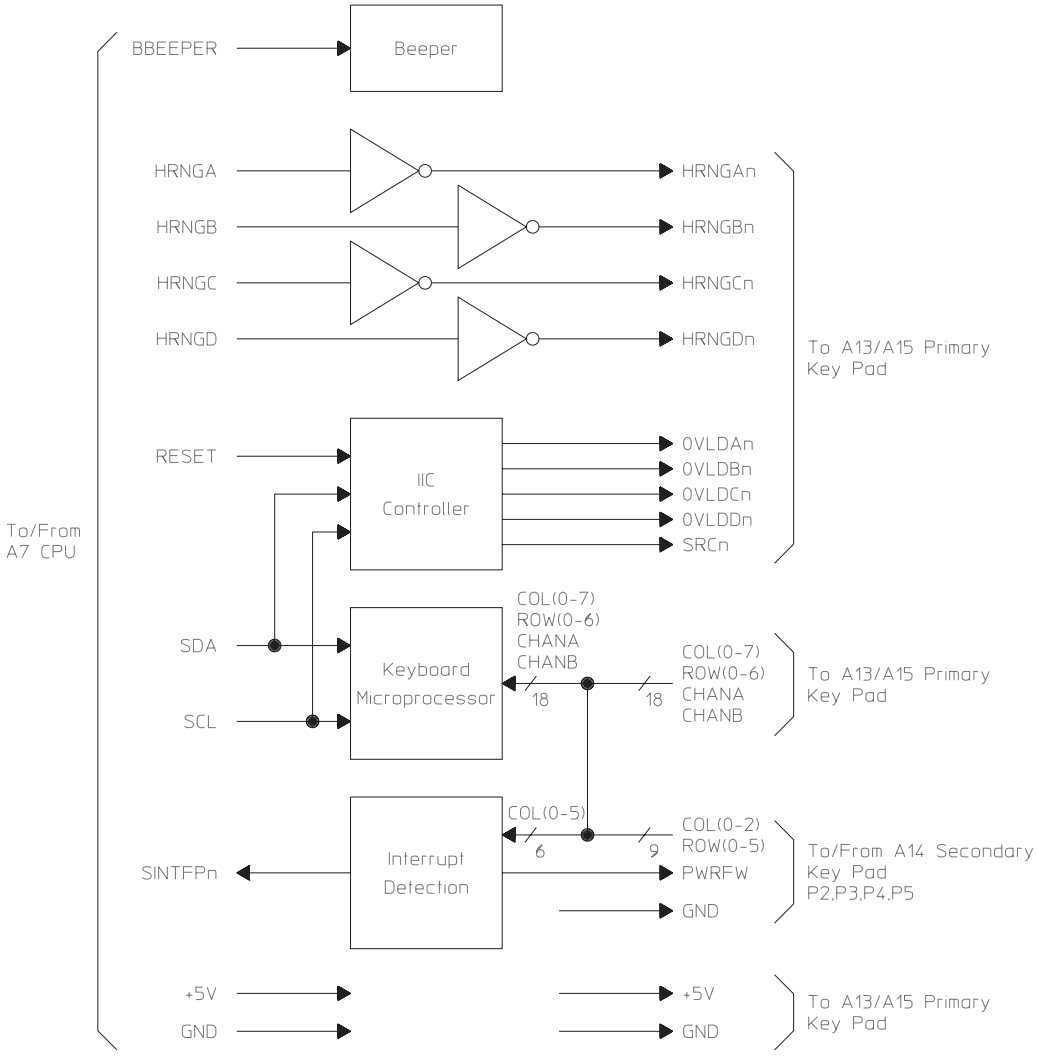
A8 Memory Block Diagram



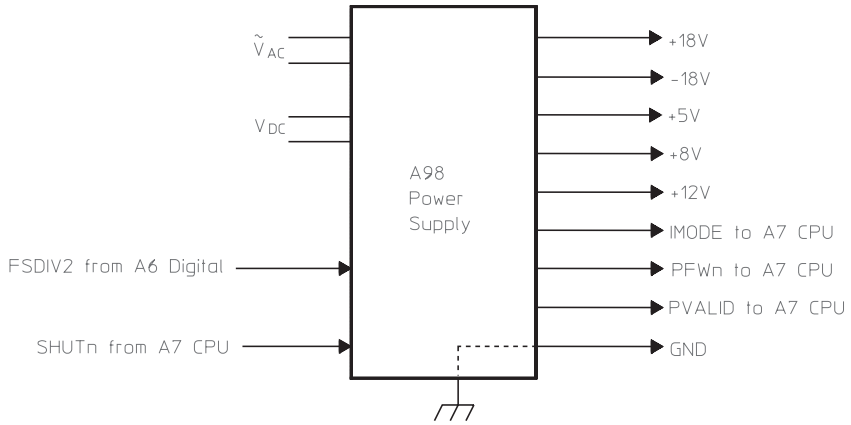
A9 NVRAM Block Diagram



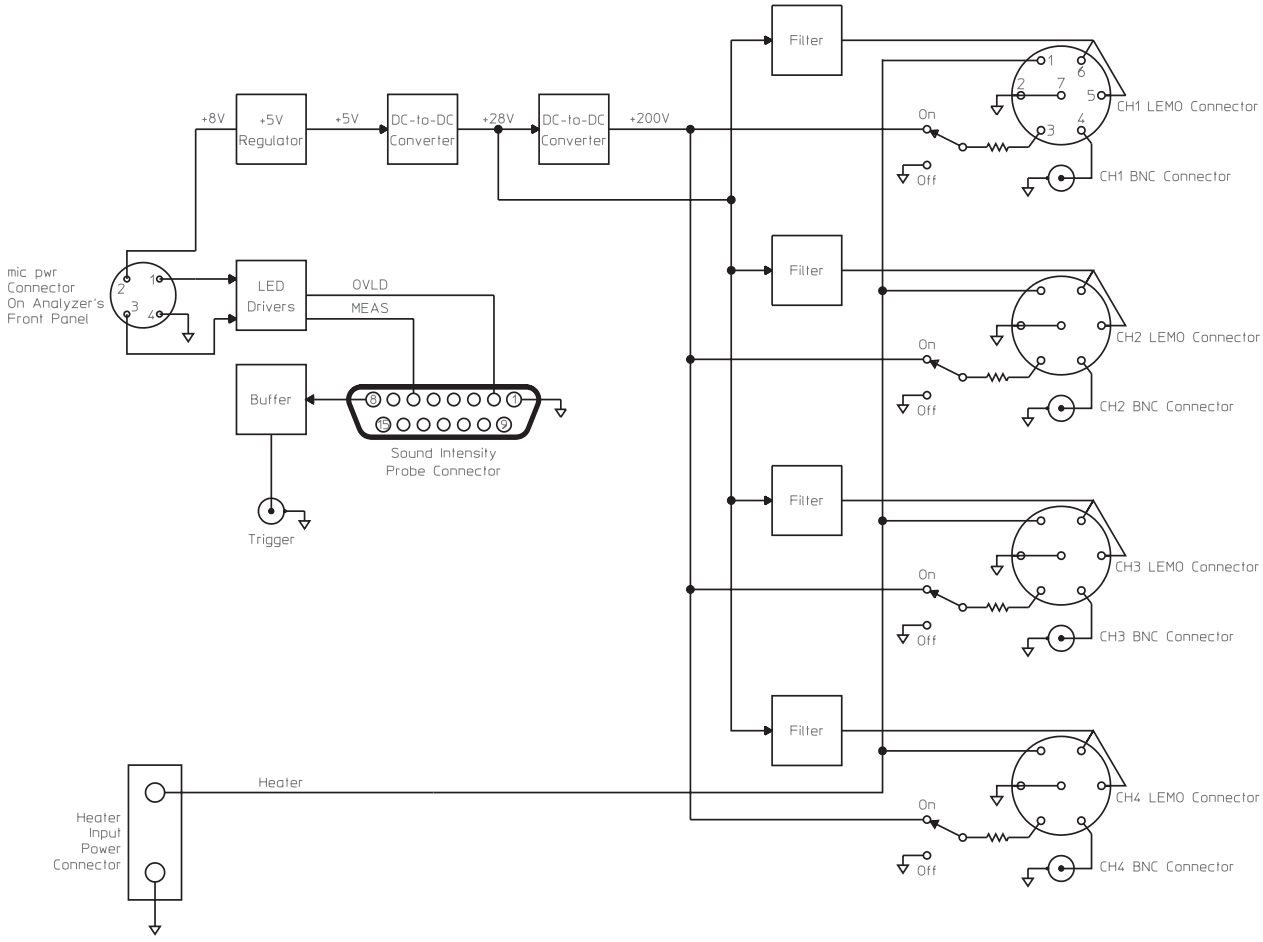
A10 Rear Panel Block Diagram



A11 Keyboard Controller Block Diagram



A98 Power Supply Block Diagram



Option UK4 Microphone Adapter and Power Supply Block Diagram

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Guide to Agilent 35670A Documentation

If you are thinking about...	And you want to...	Then read...
♦ Unpacking and installing the Agilent 35670A	Install the Agilent 35670A Dynamic Signal Analyzer	*Agilent 35670A Installation and Verification Guide*
	Do operation verification or performance verification tests	*Agilent 35670A Installation and Verification Guide*
♦ Getting started	Make your first measurements with your new analyzer	*Agilent 35670A Quick Start Guide*
	Review measurement basics	*Agilent 35670A Operator's Guide*
	Learn what each key does	Use the analyzer's [**Help**] key
♦ Making measurements	Learn how to make typical measurements with the Agilent 35670A	*Agilent 35670A Operator's Guide*
	Understand each of the analyzer's instrument modes	*Agilent 35670A Operator's Guide*
♦ Creating automated measurements	Learn the Instrument Basic interface	*Using Instrument Basic with the Agilent 35670A*
	Record keystrokes for a particular measurement	*Agilent 35670A Quick Start Guide*
(Instrument Basic is Option 1C2)	Program with Instrument Basic	*Instrument Basic User's Handbook*
♦ Remote operation	Learn about the GPIB	*GPIB Programmer's Guide*
	Learn how to program with GPIB	*GPIB Programming with the Agilent 35670A*
	Find specific GPIB commands	*Agilent 35670A GPIB Commands: Quick Reference*
♦ Using analyzer data with a PC application	Display or plot analyzer data on or from a Personal Computer	*Standard Data Format Utilities: User's Guide*
	Transfer analyzer data to a PC sofware application forma	
	Transfer data from a PC software application format tothe analyzer (for example, to load data into a data register)	
♦ Servicing the analyzer	Adjust, troubleshoot, or repair the analyzer	*Agilent 35670A Service Guide*

Need Assistance?

If you need assistance, contact your nearest Agilent Technologies Sales and Service Office listed in the Agilent Catalog. You can also find a list of local service representatives on the Web at:
http://www.agilent.com/find/assist *or contact your nearest regional office listed below.*

If you are contacting Agilent Technologies about a problem with your Agilent 35670 Dynamic Signal Analyzer, please provide the following information:

- ❑ Model number: Agilent 35670A
- ❑ Serial number:
- ❑ Options:
- ❑ Date the problem was first encountered:
- ❑ Circumstances in which the problem was encountered:
- ❑ Can you reproduce the problem?
- ❑ What effect does this problem have on you?

You may find the serial number and options from the front panel of your analyzer by executing the following:

Press [**System Utility**], [more], [serial number].

Press [**System Utility**], [options setup].

If you do not have access to the Internet, one of these centers can direct you to your nearest representative:

United States	Test and Measurement Call Center (800) 452-4844 (Toll free in US)
Canada	(905) 206-4725
Europe	(31 20) 547 9900
Japan	Measurement Assistance Center (81) 426 56 7832 (81) 426 56 7840 (FAX)
Latin America	(305) 267 4245 (305) 267 4288 (FAX)
Australia/New Zealand	1 800 629 485 (Australia) 0800 738 378 (New Zealand)
Asia-Pacific	(852) 2599 7777 (FAX) (852) 2506 9285

About This Edition

March 2010: Updated "General Specifications" section on page 1-13.

October 2000: Rebranded to Agilent Technologies.

February 1995: In "Replaceable Parts" section starting on page 7-5, updated three parts.

July 1994: Previous Edition.