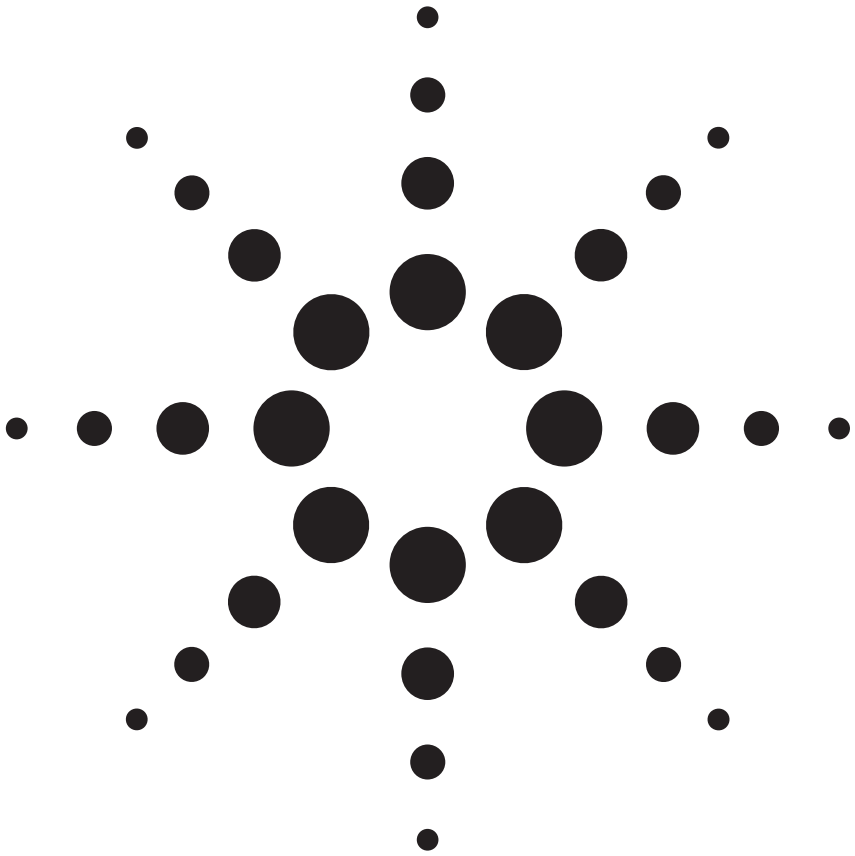
Agilent
Correlation of Simulation versus Measurement in Frequency and Time Domain

White Paper



Agilent Technologies

Contents

Overview

A measurement/simulation correlation effort was launched between Agilent Technologies and Cadence Design Systems to validate the new technology developed in the new Cadence Allegro PCB SI 630 product, which was used to produce all simulated data in this paper. The test vehicle consisted of a production Advanced Telecomm Computing Architecture (ATCA) backplane from Kaparel Corporation (a mutual Agilent/Cadence customer), and adaptor cards developed by Agilent, which plug into the backplane and provide surface mount SMA test access. The backplane has 18 layers with a nominal thickness of 125 mils, and uses the Z-PACK HM-Zd 4-pair connector from Tyco Electronics. A picture of the test configuration is shown in Figure 1. A stripline path of approximately 19" through the backplane was studied to correlate simulation vs. measured results in the frequency and time domain.

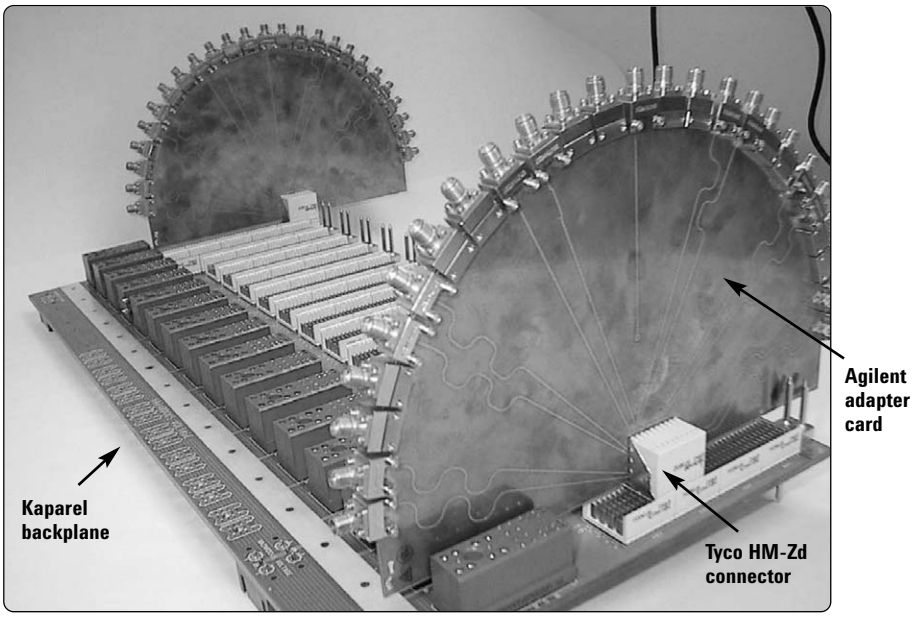


Figure 1. Test configuration

Measurement Equipment

All measurements were taken by Agilent Technologies. The Agilent equipment used was the following:

- **Oscilloscope:**
  Infiniium DCA Agilent 86100A Wide-Bandwidth Oscilloscope using 54754A Differential TDR/TDT Plug-In Module
- **Pulse Generator:**
  Agilent N4872A 13.5 Gbps Plug-In Generator from Parallel Bit Error Ratio Tester
- **Vector Network Analyzer:**
  N1957B Agilent Physical Layer Test System (PLTS), 10 MHz to 50 GHz Description E8364B PNA, N4421B Test Set, N1930A PLTS software, 4-Ports / 4-Receivers
- **Calibration Kit:**
  Agilent 85052D 3.5 mm

TDR Measurements

TDR measurements were taken of the physical boards. These plots showed that the adapter card and backplane impedances ran to the high side of the tolerance, at about 107 ohms. The measured TDR plot is shown below.

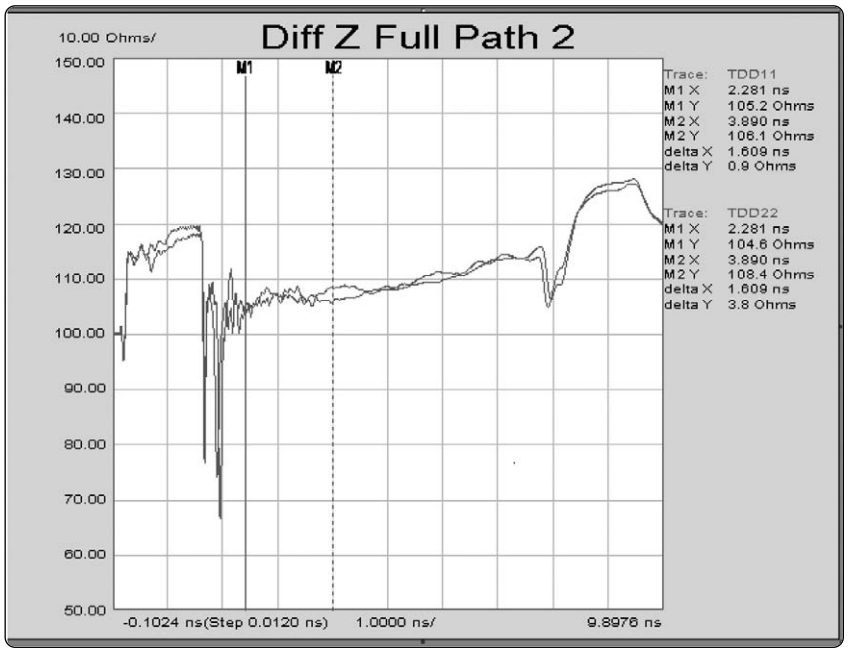


Figure 2. TDR plot of differential impedance

The topology was extracted from the backplane Allegro database. Trace and dielectric geometries were modified (within manufacturing tolerances) to mimic the impedance seen on the measured backplane. The resulting SigXplorer topology is shown below.

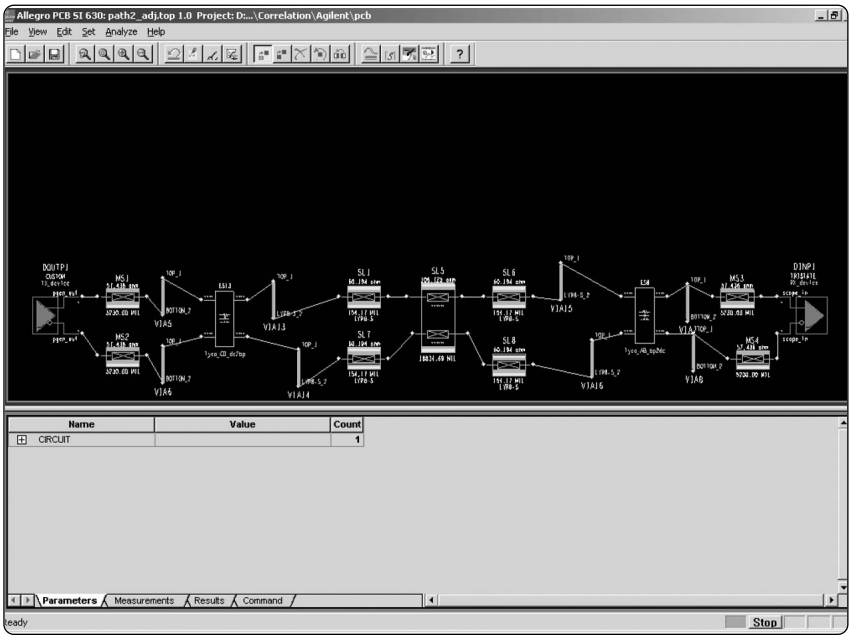


Figure 3. Stripline topology

Vias were modeled using the Via Model Generator in Cadence's Allegro PCB SI 630 product. Connector models were provided by Tyco, in SPICE format.

Frequency Domain Correlation Results

S-parameter measurements were taken by Agilent for the path through the backplane. S-parameter generation was then done in Cadence's SigXplorer environment. All of the frequency domain data in this paper refers to single-ended measurement or simulation results for the 4-port network representing the differential pair.

Below is the comparison of measured (thin line) versus simulated (thick line) insertion loss end-to-end through the system for the entire "P-side" of the differential pair. Insertion loss is often plotted as "S21" in S-parameter format, and refers to the amount of energy transmitted through the network.

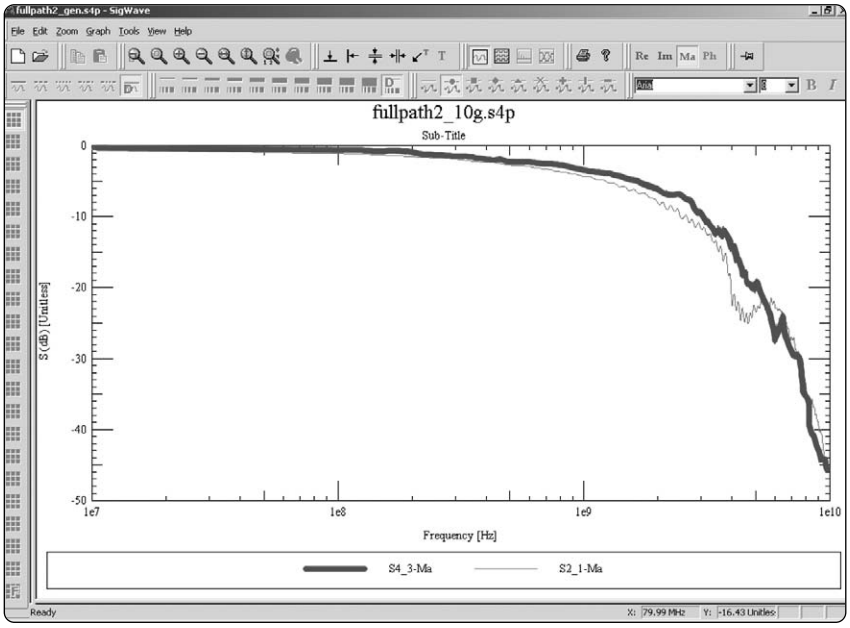


Figure 4. Insertion loss (S21) measured (thin line) vs. simulated (thick line)

The “ts2dml” utility in Allegro PCB SI 630 was used to mathematically convert the single-ended 4-port S-parameter data (both measured and simulated) to equivalent 2-port S-parameter data, in order to show the effective insertion loss seen by the differential signal. Differential insertion loss is often plotted as “SDD21” in S-parameter format, and refers to the amount of energy transmitted through the differential network. Results are shown in Figure 5.

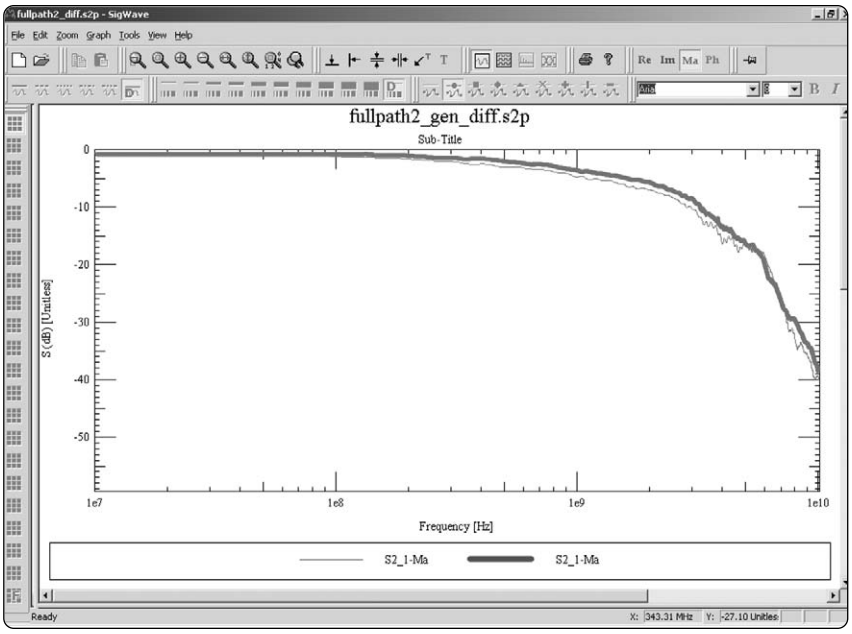


Figure 5. Insertion loss (SDD21) measured (thin line) vs. simulated (thick line) for the equivalent 2-port differential network

The comparison of measured and simulated insertion loss showed very good agreement, generally within 1 dB up to 10 GHz.

Figure 6 is a comparison of the return loss for the entire “P-side” of the differential pair, measured (thin line) versus simulated (thick line). This also correlated closely. Return loss is often plotted as “S11” in S-parameter format, and refers to the amount of energy reflected back by the network.

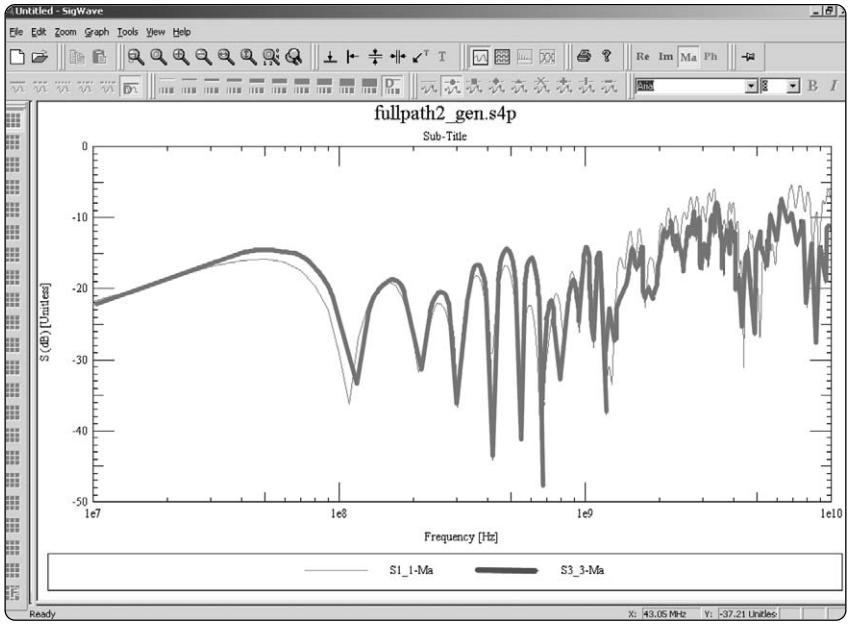


Figure 6. Return loss (S11) measured (thin line) vs. simulated (thick line)

The close correlation of measured versus simulated results permitted the opportunity to study the impact of the via models on the overall behavior of the interconnect in the frequency domain. This can be done by removing the via models, re-generating the S-parameters, and comparing the new simulated result with the initial measured and simulated results. This helps to quantify the impact the vias have on the results, and the relative accuracy with which the via's behavior is being captured by the model. Insertion loss comparisons for the entire "P-side" of the differential pair (S21) are shown in Figure 7.

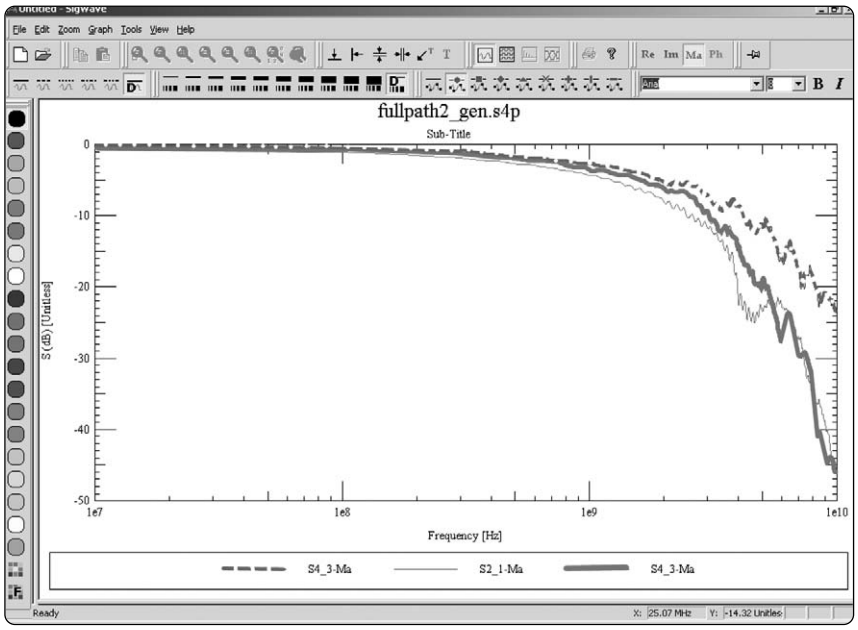


Figure 7. Insertion loss (S21) measured (thin line) vs. simulated (thick line) vs. simulated with no via models (dashed line)

In the comparison in Figure 7, the result without the via models generally stays within 1 or 2 dB of the measured data until about 1 GHz, but then starts to significantly deviate from both the measured and the initial simulated results. The loss contributed by the via models clearly plays a very significant role in the correlation with measurement over 1 GHz.

Figure 8 shows a similar comparison for the return loss (S11).

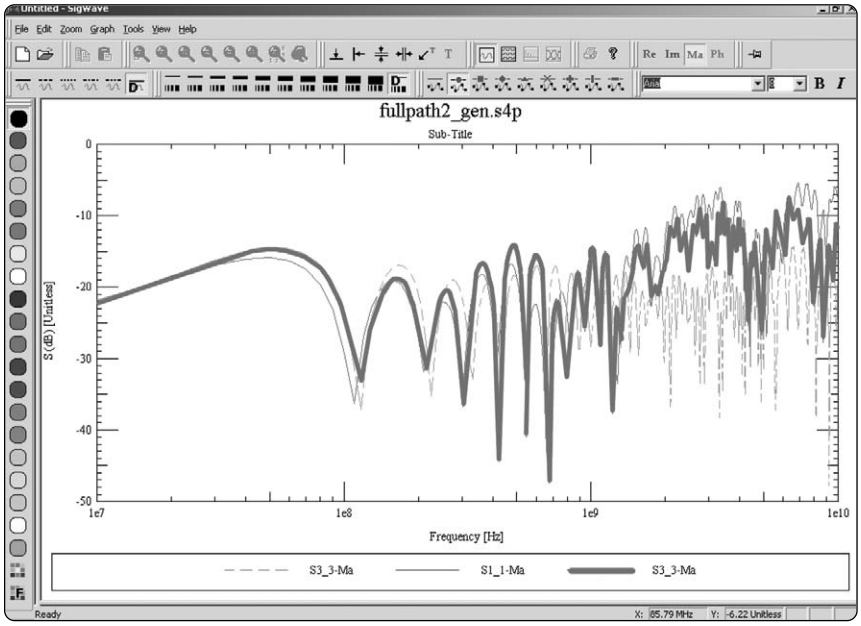


Figure 8. Return loss (S11) measured (thin line) vs. simulated (thick line) vs. simulated with no via models (dashed line)

Here, the via models again clearly play a dominant role in correlation at the higher frequencies. After about 1 GHz, the correlation is completely lost without the via models. This may possibly be due to the reflections caused by the via stubs.

Comparison with Agilent TRL Calibration

Agilent's N1957B PLTS has Thru-Reflect-Line (TRL) capability to calibrate out the effect of the adapter cards, and extract an S-parameter measurement for just the backplane and the mated backplane connectors. In this case the calibration reference plane is essentially between the backplane connector and the surface of the adapter card. These measurements were performed and compared with those generated from SigXplorer.

For cases in which specific elements of the signal path to be designed already exist in hardware, this TRL capability is a powerful addition to the design methodology. It enables very accurate measurement-based models to be extracted from hardware, and included in the design process. These known elements of the channel can be treated as "fixed", while the parameters for elements still to be designed can be explored in greater detail.

To model this case in SigXplorer, the ports were placed at the backplane vias on the adapter cards. The rest of the topology was then removed, as shown below.

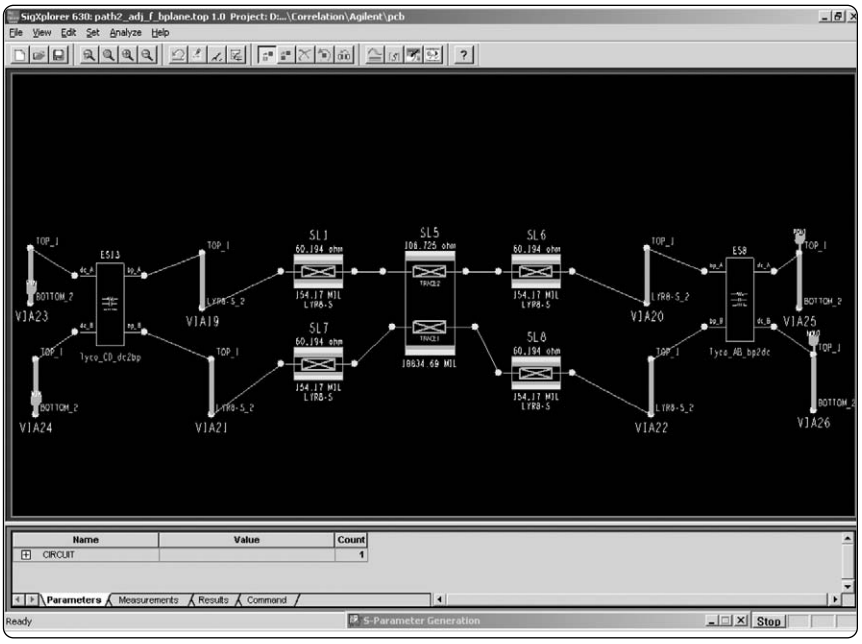


Figure 9. Topology for TRL comparison

The TRL measurements for the “backplane only” showed slightly less loss without the adapter cards than the full path VNA measurements, as expected. This is shown in Figure 10 as differential insertion loss measurements for comparison (using a linear y-axis for clarity).

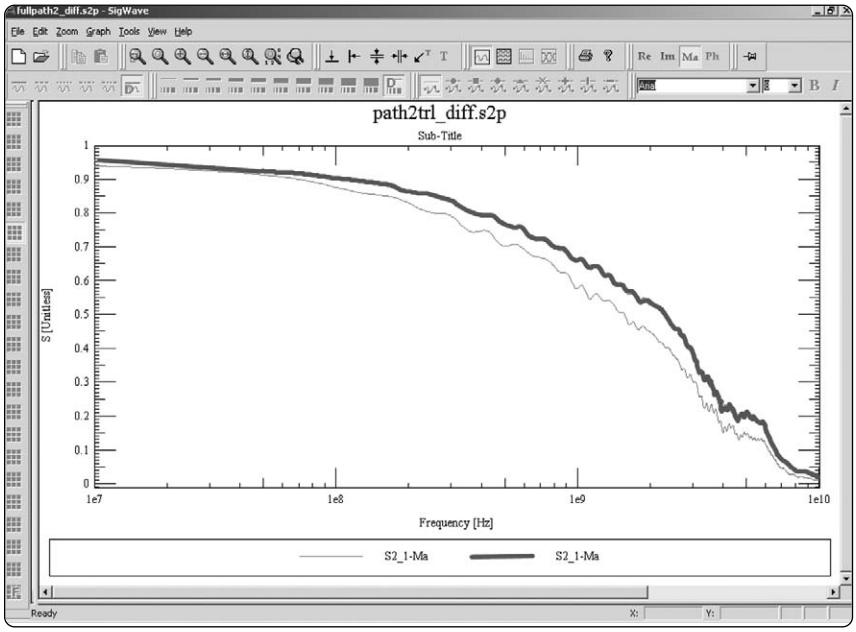


Figure 10. Full path differential insertion loss (SDD21) measurement (thin line) vs. TRL measurement for backplane and connector portion only (thick line)

The backplane-only measurement was compared with the generated S-parameters from the SigXplorer topology. This comparison for the differential insertion loss (SDD21) is shown in Figure 11.

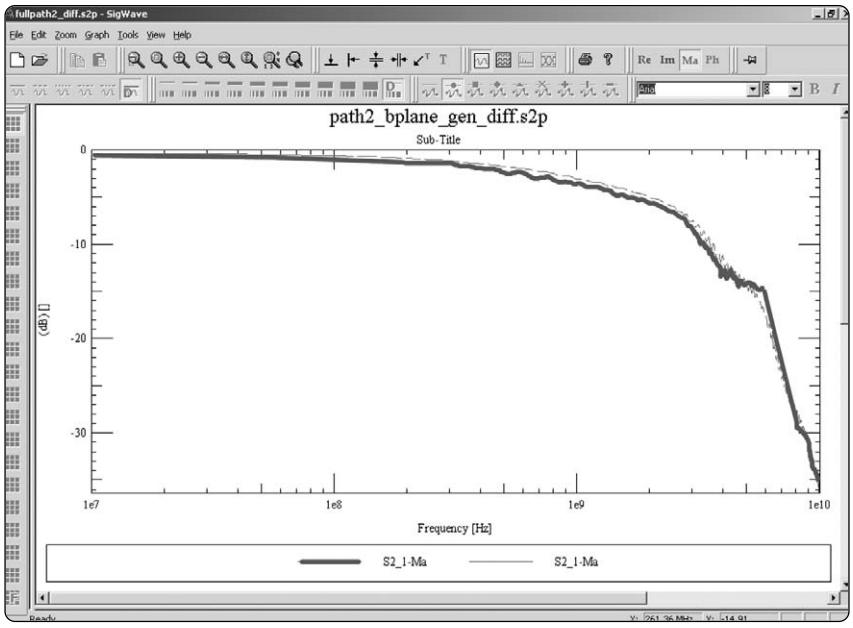


Figure 11. Differential insertion loss (SDD21) from TRL measurement for backplane and connector portion only (thick line) vs. simulated result (thin dashed)

The measured and simulated results matched very closely, within 1 dB.

Measured Time Domain Results at 3.125 Gbps

Next, measured eye patterns were captured on a sampling oscilloscope, using a pattern generator to drive the channel. First, the pattern generator was connected directly to the scope, to baseline how much jitter was contributed from the test setup, using a data rate of 3.125 Gbps. A PRBS, using a pattern of 2^{23} bits, was used to drive the channel. This result is shown in Figure 12.

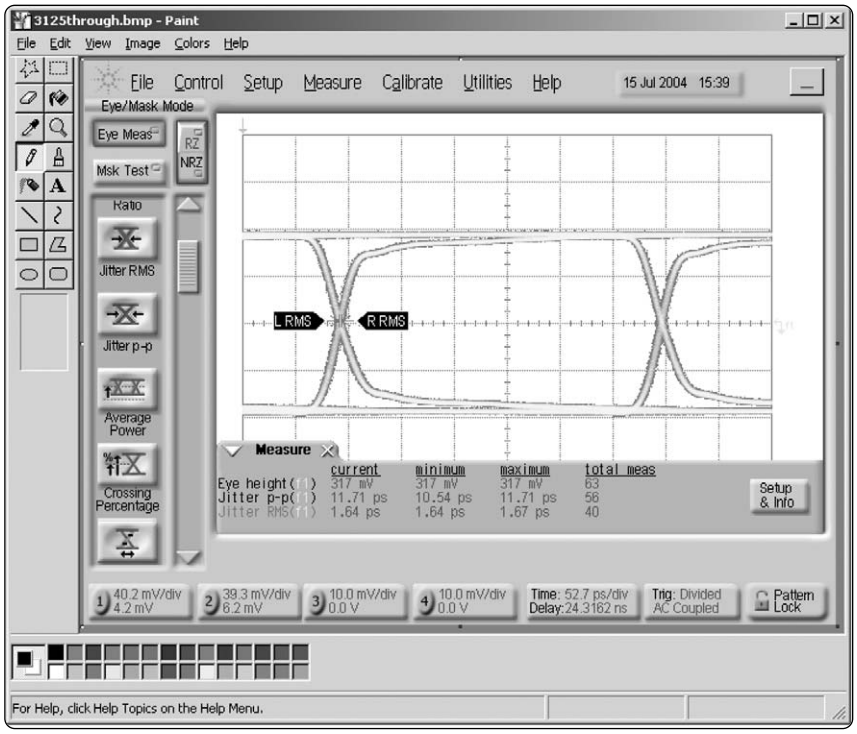


Figure 12. Baseline jitter measurement at 3.125 Gbps

The observed peak to peak jitter from the pattern generator was about 12 ps. This represents about 4% of the 320 ps unit interval (UI).

The measured eye pattern at 3.125 Gbps is shown in Figure 13.

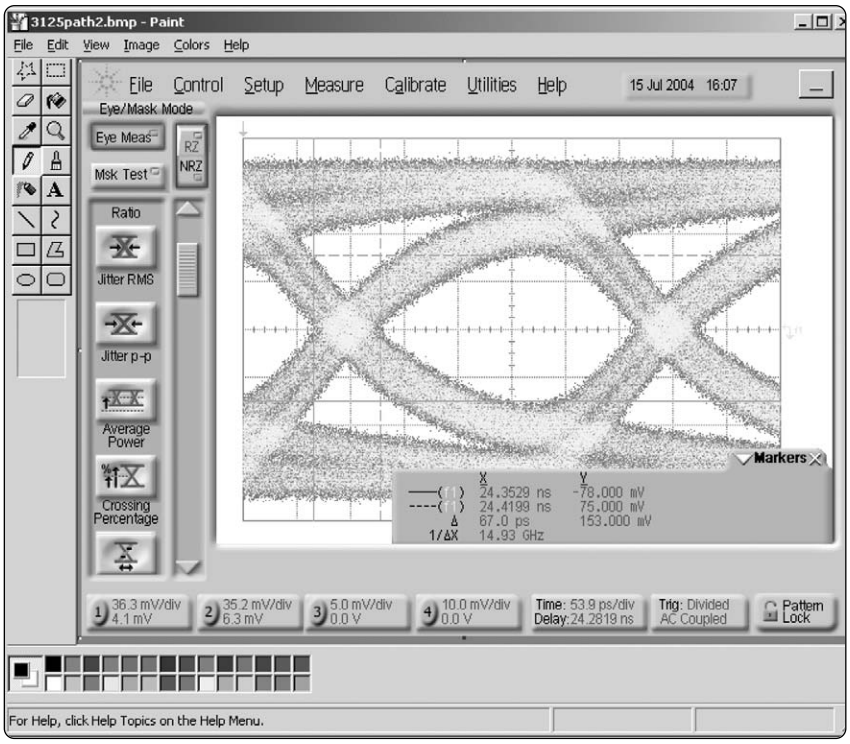


Figure 13. Measured eye pattern for 3.125 Gbps

Observed eye height and peak-to-peak jitter were 153 mV and 67 ps respectively. This jitter represents 0.21 UI at this data rate.

Number of Bits Sampled by the Oscilloscope

An interesting question to ask is “how many bits are used to generate the eye pattern seen on the oscilloscope?” This is an important item, as it will tell us how many bits to run in the time domain simulation of the channel, which is required in order to get close to an “apples-to-apples” comparison scenario for correlation. The following data was used to estimate this number:

- 40 k samples/sec taken by the scope
- 1350 horizontal pixels (samples) taken for a full “record” (once across the entire screen)
- eye patterns were allowed to stabilize for approximately 60 seconds

Using the data above, it is estimated that about 40 k samples/sec x 60 sec = 2.4 million samples were taken to generate the eye patterns. At 1350 pixels per record, this means that approximately 2.4 million samples / (1350 samples/record) = 1778 records (or full screens) were captured and overlaid to generate the measured eye pattern.

From these estimates, it was decided to use an input bit stream of about 1800 bits as stimulus for the time domain simulation, in order to best compare with measurement.

Simulated Time Domain Results at 3.125 Gbps

The pattern generator was modeled as a simple differential driver with an output impedance of 50 ohms, a peak-to-peak differential voltage swing of 400mV, and 16ps rise and fall times (20% to 80% single-ended). The channel was then stimulated with a 3.125 Gbps 2^{23} PRBS of 1800 bits. To mimic the pattern generator, 4% UI of jitter was added to the input stimulus, as seen in the baseline jitter measurement. Simulated results from the Channel Analysis capability within Cadence's Allegro PCB SI product are shown in Figure 14.

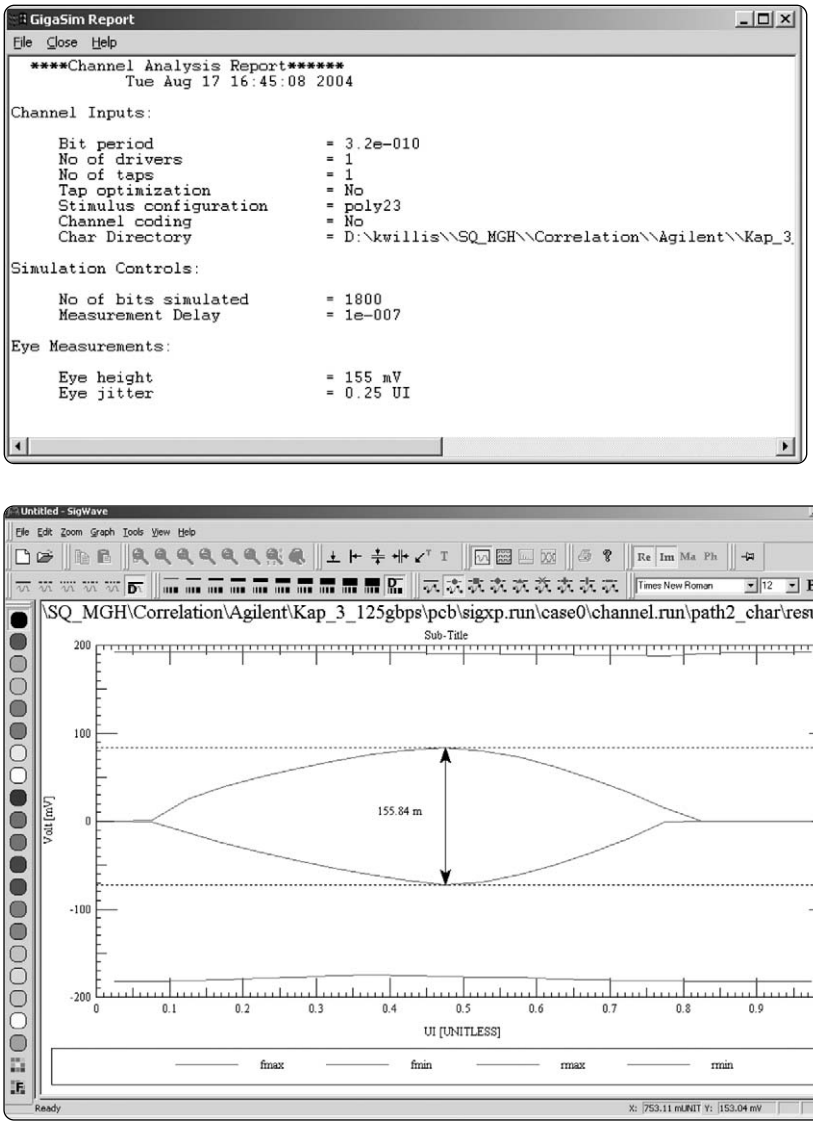


Figure 14. Simulated eye pattern for 3.125 Gbps, sampling 1800 bits and including input jitter

Conclusions

- Good correlation in the frequency domain was achieved after adjusting the channel model to have similar impedance characteristics to the actual hardware, which ran to the high side of the impedance tolerance. This is an important step when attempting to correlate measured and simulated results.

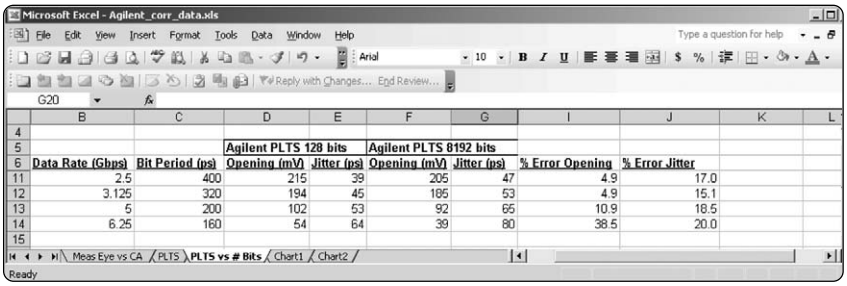
- Correlation to eye pattern measurements in the time domain was also good, with eye height matching very closely and peak-to-peak jitter matching within 0.04UI. Some of this deviation between measured and simulated peak-to-peak jitter can be attributed to differences between the channel model and the actual hardware, which can be seen in the frequency domain results. Tabulated time domain data is shown below. Based on this, it appears that the interconnect modeling of Allegro PCB SI 630 is effective for data rates up to the 3.125 Gbps tested here.

Table 1. Tabulated Time Domain Results

Measured Eye Height (mV)	Simulated Eye Height (mV)	Measured Jitter (%UI)	Simulated Jitter (%UI)
153	155	0.21	0.25

- Eye patterns close as larger and larger bit streams are simulated, approaching some asymptotic value. In order to get accurate eye pattern predictions, it is important to simulate many more bits than is typically done in practice today. This is supported by the data provided by Agilent's PLTS (Physical Layer Test System) as well as Cadence's Allegro PCB SI 630 product. The next table shows the differences shown by Agilent PLTS when running 128 bits through the path vs. running 8192 bits.

Table 2. Eye closure as # of simulated bits increases



	B	C	D	E	F	G	I	J	K	L
4										
5			Agilent PLTS 128 bits		Agilent PLTS 8192 bits					
6	Data Rate (Gbps)	Bit Period (ps)	Opening (mV)	Jitter (ps)	Opening (mV)	Jitter (ps)	% Error Opening	% Error Jitter		
11	2.5	400	215	39	205	47	4.9	17.0		
12	3.125	320	194	45	185	53	4.9	15.1		
13	5	200	102	53	92	65	10.9	18.5		
14	6.25	160	54	64	39	80	38.5	20.0		
15										

This is shown graphically below.

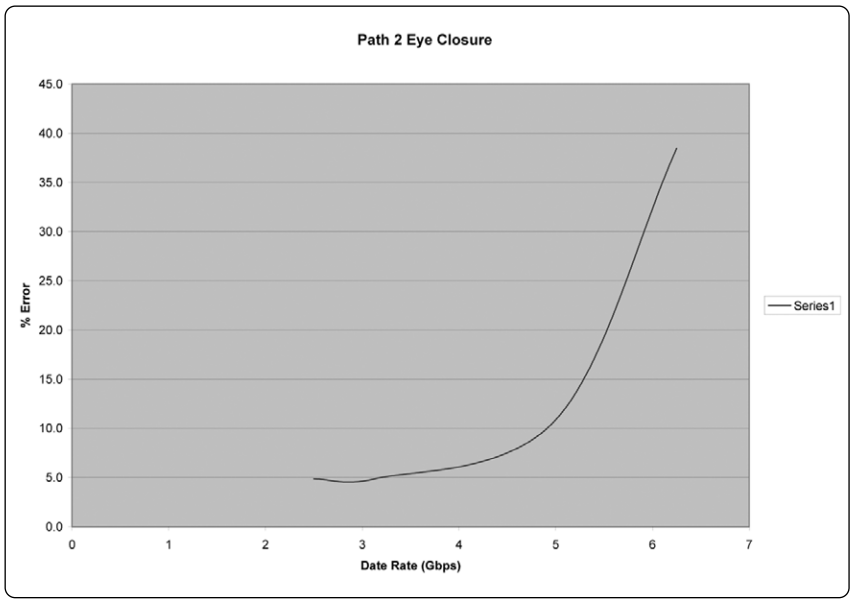


Figure 15. Eye opening measurement error when simulating 128 bits vs. 8192 bits

- Based on this data, it appears that the % error users may experience by simulating small bit streams (which do not give the eye pattern time to stabilize) increases exponentially as data rates increase. New simulation methodologies will be required in order to address this issue.

Agilent Physical Layer Test System Configuration Guide

PNA Network Analyzer Bundles
(PNA+ Test Set+Software)

- N1953B (10 MHz to 20 GHz)
- N1955B (10 MHz to 40 GHz)
- N1957B (10 MHz to 50 GHz)

Test Set Only

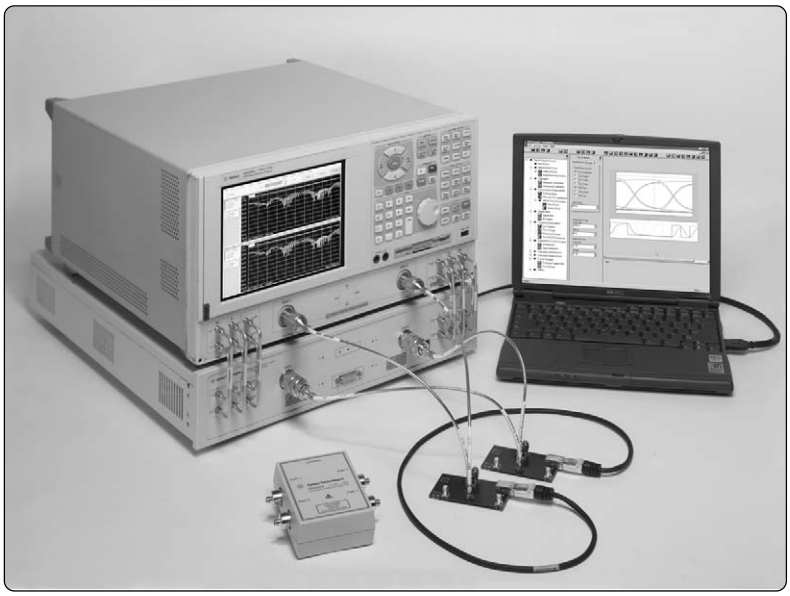
- N4419B (10 MHz to 20 GHz)
- N4420B (10 MHz to 40 GHz)
- N4421B (10 MHz to 50 GHz)

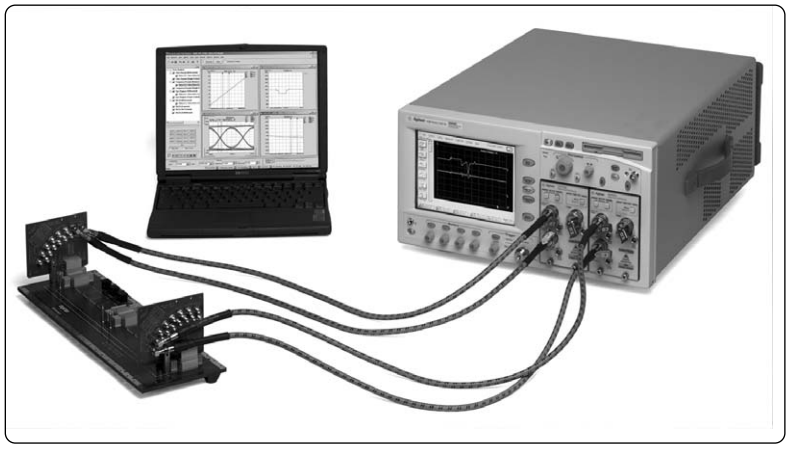
TDR

- 86100C w/54754A TDR module(s)
- CSA8000 w/80E04 TDR module(s)
- TDS8000 w/80E04 TDR module(s)

Software Only

- N1930A-010 node-locked license
- N1930A-020 floating license





Web Resources

Cadence Design Systems home page:
http://www.cadence.com

Allegro PCB SI data sheets:
http://www.cadence.com/products/si_pk_bd/pcb_si/index.aspx

Allegro PCB SI community:
http://www.allegrosi.com

Agilent Technologies home page:
http://www.agilent.com

Agilent Technologies PLTS page:
http://www.agilent.com/find/plts

Agilent Technologies PNA network analyzer page:
http://www.agilent.com/find/pna

Kaparel Corporation home page:
http://www.kaparel.com

Acknowledgment

Special thanks is given to the Kaparel Corporation for the contribution of their ATCA backplane as a basis for measurement and correlation on a real-world multi-gigahertz serial data application.

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent T&M Software and Connectivity
Agilent's Test and Measurement software and connectivity products, solutions and developer network allows you to take time out of connecting your instruments to your computer with tools based on PC standards, so you can focus on your tasks, not on your connections. Visit **www.agilent.com/find/connectivity** for more information.

By internet, phone, or fax, get assistance with all your test & measurement needs

Online Assistance:
www.agilent.com/find/assist

Product specifications and descriptions in this document subject to change without notice.

Printed in USA December 6, 2004
5989-1940EN

Agilent Technologies