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Practical RF Amplifier Design Using the Available Gain Procedure and the Advanced Design System EM/Circuit Co-Simulation Capability
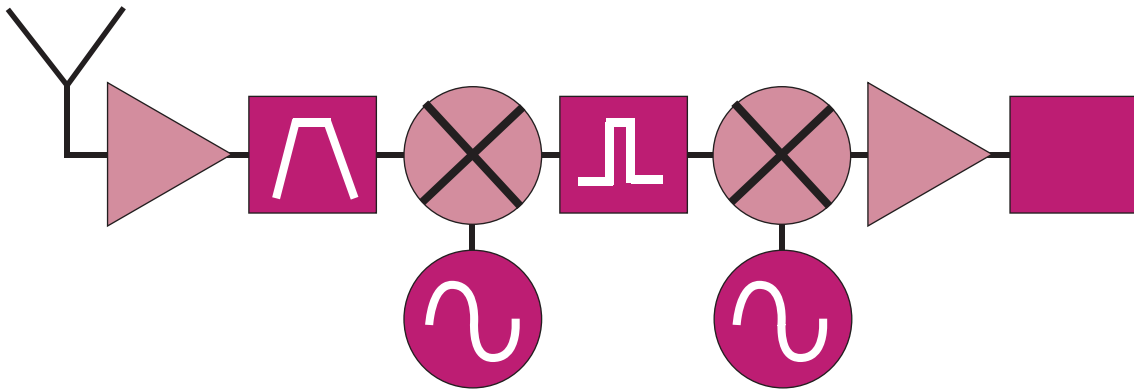
White Paper by Ken Payne

Figure 1

Abstract

This article features a method of designing a low noise RF amplifier for an 802.11b receiver application and contains an Avago ATF54143 PHEMT transistor. ADS design tools are used such that the techniques presented remove much of the guesswork from the design process. Design speed and cost along with RF performance are of utmost importance for most RF designs, thus, one of the main objectives is to yield a design that works with the first PCB pass. If successful, multiple PCB layouts are avoided, which saves design cost and time. This design procedure is considered successful even if some of the lumped component values have to be adjusted slightly to get the desired RF performance – as long as the layout does not have to be modified to have a working circuit. It is also considered successful even if the model prediction doesn't exactly agree with measured results, but the resulting circuit still meets the design criteria and specifications. The featured amplifier covers a frequency range of 2.4 GHz to 2.48 GHz. The design is illustrated from start to finish, with construction of a printed circuit board and measurement results.

Introduction

An amplifier circuit consists mainly of a gain device or devices, and input and output matching or coupling networks. The amplifier should make weak signals larger without adding too much noise or distortion. Ideally, the amplifier would add no noise and would not distort the signal in any way. Electronic devices are not ideal however, and thus degrade the signal to some degree. The amplifier design objective is to minimize the noise added and the distortion created while increasing the amplitude of the signal. Design trade-offs allow one to obtain the best possible performance from a particular active device.

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Background

For low noise amplifier designs, the available gain design approach is typically utilized to facilitate a gain versus noise "trade-off". Most applications do not allow or necessarily require a minimum noise design since gain is reduced to allow for the lower noise performance. Thus, a gain versus noise "trade-off" is appropriate. Knowledge about the system in which the amplifier is to be used is required to make the appropriate gain versus noise trade-off. If subsequent stages following the RF amplifier have a high cumulative noise figure, more gain is required to "take-over" the noise figure of those stages, thus providing the lowest possible system noise. An example system is shown in Figure 1. System noise factor is calculated using the Friis formula as follows:

Equation 1.
$$F_T = F_1 + \frac{F_2 - 1}{g_1} + \frac{F_3 - 1}{g_1 g_2} + \cdots + \frac{F_n - 1}{g_1 g_2 \cdots g_{n-1}}$$

where: F_T is the total system noise factor,
F_1 is the noise factor of stage one,
F_2 is the noise factor of stage two,
F_n is the noise factor of stage number n.
g_1 is the numeric gain factor of stage one,
g_2 is the numeric gain factor of stage two,
g_{n-1} is the numeric gain factor of the second to the last stage.

Based on Equation 1, earlier gain stages diminish the effect of cumulative noise added by stages farther back in the system. Thus, trading away too much gain for lower noise figure in the early stages of the system may degrade the overall system noise due to less noise "take-over" of the following stages.

Equations 2 and 3, respectively, convert noise figure, NF in dB, to numeric noise factor, F and gain, G in dB to gain factor, g:

Equation 2. $F = 10^{NF/10}$ Equation 3. $g = 10^{G/10}$

Equations 4 and 5 respectively, convert noise factor, F to noise figure, NF in dB, and gain factor, g to gain, G in dB:

Equation 4. $NF = 10 \log F$ Equation 5. $G = 10 \log(g)$

Use Equations 1 through 5 to determine amplifier gain and noise figure requirements for a given system.

Transducer Gain

A two-port network is terminated as shown in Figure 2. The generalized transducer numeric gain equation for the two-port s-parameter block terminated by Γ_S and Γ_L of Figure 2 is given by Equation 6:

Equation 6.
$$g_T = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_S |\Gamma_L||}$$

The s-parameters describe a device for a particular set of conditions, such as frequency, bias, and temperature as shown in Equation 6. Transducer gain, g_T, is a function of the s-parameters, Γ_S, and Γ_L. Convert numeric transducer gain g_T, to gain G_T in dB by use of Equation 5. When the device is terminated in the same impedance as when s-parameters were measured, Γ_S and Γ_L are zero and $g_T = |S_{21}|^2$.
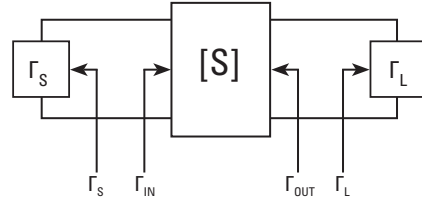

Figure 2.

Stability Analysis

The Figure 2 two-port network may be stable or potentially unstable. It is imperative that the amplifier does not oscillate in the product environment, since such behavior leads to product malfunction. If the two-port is potentially unstable, there are conditions where oscillations can occur. Certain source or load terminations that produce the oscillations provide the conditions necessary for the unstable behavior. This type of design is called a conditionally stable design. If the conditionally stable design method is utilized, extreme care must be observed to guarantee that a source or load termination that produces an oscillation is never presented to the amplifier. This applies to all frequencies in-band and out-of-band. This can be a difficult task at best in most applications. The unconditionally stable design approach allows any source or load terminations, which have reflection coefficient magnitudes between 0 and 1, inclusive, presented to the amplifier without the possibility of an oscillation. It is highly recommended that the two-port is made unconditionally stable at all frequencies. An unconditionally stable design guards against unexpected oscillations, which cause product malfunction.

Two-port stability is analyzed using stability circles or equations. In this design example, stability equations are used to achieve an unconditionally stable design at all frequencies. The stability equations are a function of the Figure 2 two-port s-parameters. Equation 7 gives the value for stability factor K, which is made greater than or equal to unity for stability. Additionally, stability factors Δ, B1, and B2 are shown by Equations 8, 9, and 10 respectively. To achieve unconditional stability, the two-port must satisfy Equation 7 and either Equation 8, 9, or 10. If Equation 8, 9, or 10 is satisfied, all three equations are, by definition, satisfied. Thus, if K ≥ 1, the two-port network may not be unconditionally stable. Having K ≥ 1 is a necessary, but not sufficient, condition for unconditional stability. Additionally, Equation 8, 9, or 10 is analyzed to determine if the two-port network stability is unconditional. Thus, |Δ| < 1, or B1 > 0, or B2 > 0 must also be met along with K ≥ 1 to guarantee unconditional stability.

Equation 7.
$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \geq 1$$

Equation 8.
$$|\Delta| = |S_{11}S_{22}-S_{21}S_{12}| < 1$$

Equation 9.
$$B_1 = 1+|S_{11}|^2-|S_{22}|^2-|\Delta|^2 > 0$$

Equation 10.
$$B_2 = 1+|S_{22}|^2-|S_{11}|^2-|\Delta|^2 > 0$$

Alternately, the single test stability factor μ_{Source} or μ_{Load} is calculated using Equation 11 or Equation 12. If $\mu_{Source} \geq 1$ then $\mu_{Load} \geq 1$ by definition and vice versa. If Equation 7 is satisfied and either of Equations 8, 9, or 10 are satisfied, then both Equations 11 and 12 are satisfied. And, of course, if Equations 11 or 12 are satisfied, then Equations 7 through 10 are satisfied.

Equation 11.
$$\mu_{Source} = \frac{1-|S_{11}|^2}{|S_{22} - \Delta\,(S_{11}^*)| + |S_{21}\,S_{12}|} \geq 1$$

Equation 12.
$$\mu_{Load} = \frac{1-|S_{22}|^2}{|S_{11} - \Delta\,(S_{22}^*)| + |S_{21}\,S_{12}|} \geq 1$$

If the two-port network is not unconditionally stable, and unconditional stability is required, stabilizing networks are added. Methods of stabilizing the two-port include feedback. These methods typically degrade some parameter such as maximum gain or noise figure. If care is taken, minimal degradation is possible while achieving unconditional stability. Once the stability networks are added, they become part of the two-port network and new s-parameters that describe the new two-port network are calculated. These new s-parameters are used in the stability equations to verify stability. Once the two-port network is unconditionally stable, input and/or output matching networks are added to get the desired performance.

Available Gain Design Procedure

For low noise amplifier design, the available gain design approach is typically performed. When performing the available gain design procedure, the source termination is constrained to some arbitrary impedance (usually for better noise performance), and the resulting output reflection coefficient of the device is conjugately matched. Thus, a mismatch may exist at the input whereas the output is perfectly matched. If a mismatch exists at the device input, the amount of gain is less than the maximum possible gain as is the case when both input and output are conjugately matched. To determine the amount of available gain with the input mismatched, Equation 6 is modified. Since the output is conjugately matched for a given source termination, Γ_{OUT} is expressed in terms of Γ_S and the two-port s-parameters. By substitution and rearrangement, this also allows Equation 6 to be expressed in terms of ΓS and the two-port s-parameters. The available gain design procedure is applicable to both the conditionally stable and unconditionally stable cases. This amplifier design procedure examines the unconditionally stable case only.

The transducer gain equation g_T of Equation 6, is rearranged as shown in Equations 13 and 14:

Equation 13.
$$g_T = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}\,|S_{21}|^2\,\frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT}\Gamma_L|^2}$$

where:

Equation 14.
$$\Gamma_{OUT} = S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1-S_{11}\Gamma_S}$$

When the device output is conjugately matched for a given source termination Γ_S, then transducer gain, g_T, is simplified in terms of the s-parameters and Γ_S. Conjugately matching the output mathematically yields $\Gamma_L = \Gamma_{OUT}^*$ and Equation 15 yields available gain, g_A:

Equation 15.
$$g_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \; |S_{21}|^2 \; \frac{1}{1-|\Gamma_{OUT}|^2}$$

Substituting Equation 14 into Equation 15 yields the available gain equation, g_A, as shown in Equation 16, which is a function of Γ_S and the two-port s-parameters.

Equation 16.
$$g_A = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{\left(1-\left|\dfrac{S_{22}-\Delta\Gamma_S}{1-S_{11}\Gamma_S}\right|^2\right)|1-S_{11}\Gamma_S|^2}$$

A family of circles known as available gain circles are constructed that provide a specific amount of mismatch at the device input. An infinite number of source terminations forming the circle allow selection of mismatch at the device input. To construct an available gain circle, locate the center of the circle on a Smith chart and draw the circumference from a calculated radius. Locate the center for a particular gain circle using Equation 20, which yields a magnitude and angle. The desired available gain in dB is converted to numeric gain factor g_A for Equation 17. Equation 17 is then used in Equations 19 and 20.

Equation 17.
$$g_a = \frac{g_A}{|S_{21}|^2}$$

Equation 18.
$$C_1 = S_{11} - \Delta S_{22}^*$$

The radius of an available gain circle is calculated by equation 19:

Equation 19.
$$R_a = \frac{[1 - 2K|S_{12}S_{21}|g_a + |S_{12}S_{21}|^2 g_a^2]^{\frac{1}{2}}}{1 + g_a(|S_{11}|^2 - |\Delta|^2)}$$

Equation 20.
$$C_a = \frac{g_a C_1^*}{1 + g_a(|S_{11}|^2 - |\Delta|^2)}$$

Plotting available gain circles in conjunction with noise contours allows an easy selection of gain versus noise figure for the amplifier.

Noise Figure Design Procedure

Equation 21 describes transistor noise factor performance. As shown in this equation, transistor noise performance is independent of load termination and is determined solely by its source termination and noise parameters. The noise parameters fully describe the noise performance of a device for a specific set of conditions such as frequency, bias, and temperature.

Equation 21.
$$F = F_{Min} + \frac{4r_n|\Gamma_S - \Gamma_{opt}|^2}{(1-|\Gamma_S|^2)|1 + \Gamma_{opt}|^2}$$

Transistor noise factor F is a function of Γ_S, F_{Min}, r_n, and Γ_{opt}, where F_{Min}, r_n, and Γ_{opt} are known as the transistor noise parameters. Γ_S terminates the two-port input of Figure 2. As Γ_S approaches Γ_{opt}, the transistor noise factor approaches its minimum. As Γ_S departs from Γ_{opt}, the noise factor increases from its minimum value. The rate at which the noise factor increases depends on the noise resistance r_n. Conversion of transistor noise factor to noise figure in dB is obtained from Equation 4. Equation 22 obtains the noise resistance rn if F_{Min}, Γ_{opt}, and the noise factor with the input terminated in 50 Ω is known. ($\Gamma_S = 0$)

Equation 22. $$r_n = (F_{\Gamma_s=0} - F_{min}) \frac{|1+\Gamma_{opt}|^2}{4|\Gamma_{opt}|^2}$$

Since noise factor degrades as the source termination departs from Γ_{opt}, contours may be constructed which yield a given noise performance for a particular source termination called noise circles. An infinite number of source terminations forming a circle provide a given noise figure. The noise circles are plotted by first locating the center of a particular circle using Equation 24.

Equation 23. $$N_i = \frac{F_i - F_{min}}{4r_n} |1+\Gamma_{opt}|^2$$

Equation 24. $$C_{F_i} = \frac{\Gamma_{opt}}{1+N_i}$$

Equation 25 calculates the radius of each noise circle.

Equation 25. $$R_{F_i} = \frac{1}{1+N_i} \sqrt{N_i^2 + N_i(1-|\Gamma_{opt}|^2)}$$

For low noise amplifier design, a gain versus noise trade-off is typically made. Available gain circles are plotted with constant noise figure circles for a trade-off between gain and noise figure. The optimum noise performance seldom coincides with the maximum gain of the device. Since each gain or noise circle describes the device performance under a given set of conditions, a prediction of gain and noise figure is determined by a known source termination. Enhanced noise performance is obtained with a source termination closer to the optimum noise termination Γ_{opt}, at the expense of gain. More gain results when the source termination is conjugately matched to the device input, Γ_{MS}, at the expense of noise figure. A trade-off is made between noise and gain by selecting an intermediate source termination. Thus, neither optimum noise nor maximum gain is obtained.

802.11b Amplifier Design Requirements

A low noise amplifier (LNA) is required for a WCS (wireless communication system) receiver application. Using Equations 1 through 5 and system specifications, it is determined that the LNA requires the following performance:

Frequency range:..................................... 2.4 GHz to 2.48 GHz
Gain: .... > 12 dB
Noise figure: .... < 2.5 dB
Input return loss...................................... > 10 dB
Output return loss .... > 10 dB
Third order input intercept point:.......... > 0 dBm
Supply voltage: .... 3.3 Volts
Supply current: .... < 100 mA

Several manufacturers produce high performance transistors that are suitable for this particular design. Frequency range, maximum gain, minimum noise figure, and linearity are all considered during the active device selection process. One aspect that is often overlooked during the selection process is whether or not measured s-parameters, noise parameters, and a nonlinear model exist for the chosen transistor. Design cycle times are significantly reduced if nonlinear models and measured s-parameter and noise parameter data is available from the manufacturer. Having the data in electronic form speeds import into the chosen RF/μ_{Wave} circuit simulator. It is highly recommended that supplied data is verified in a measurement lab if available to ensure its validity before too many design resources are committed to a particular device.

Transistor S-Parameters and Nonlinear Model

Several transistors were selected as candidates for the WCS LNA by inspection of corresponding data sheets. Many devices were quickly eliminated since a nonlinear model and measured s-parameters were not available from the particular manufacturer in electronic form. The Avago ATF54143 has measured s-parameter and noise parameter data at various bias conditions and a nonlinear model available in electronic form and specifications that should yield a design with the desired performance. The ATF54143 nonlinear model available from Avago is shown in Figure 3.

Latest ATF-54143curtice ADS MODEL

Figure 3. ATF54143model.dsn

Since both the nonlinear model and measured s-parameters are available, a quick validation is possible and recommended. Avago measured s-parameter data with a 3.0 Volt bias voltage at the drain and a drain-to-source current of 60 mA. Figure 4 shows an s-parameter simulation that plots the Avago measured s-parameter. An Amplifier Design Guide (from a schematic, select: DesignGuides > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay) is used to quickly set up the simulation as shown in Figure 4. The ATF541433_3V60mA.s2p file has both s-parameters and noise data included. The simulation is performed from 100 MHz to 6 GHz, stepped every 10 MHz and stored in a dataset. These results are later compared to the nonlinear model s-parameter simulation.
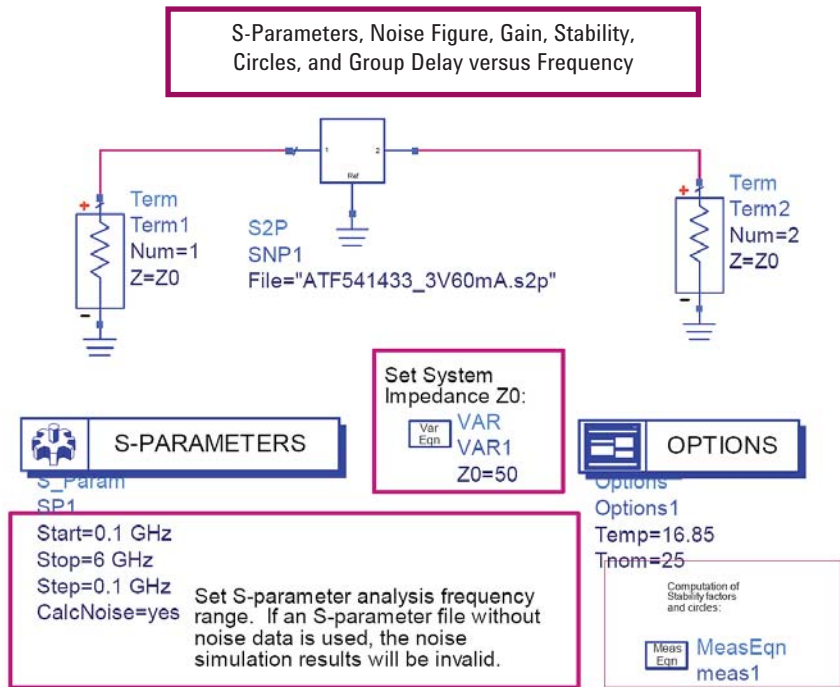
Figure 4. ATF54143_Avago_S-parameters.dsn

Now, the nonlinear model is biased at the same DC operating point as was the device for the measured s-parameter data provided by Avago as shown in Figure 5. The target product has a 3.3 V regulated supply voltage available for biasing the amplifier. The ATF54143 nonlinear model sub-circuit is shown as a symbol (sub-circuit) and labeled "Latest_ATF54143". The ATF54143 nonlinear model has the 3.3 V supply voltage connected to the drain through a 5 Ω resistor Rd. This resistor drops the supply voltage from 3.3 V to 3.0 V when 60 mA of bias current flows through the drain terminal. The transistor s-parameters are affected very little when the drain voltage is 3.3 V instead of 3.0 V. However, adding the resistor will make the application conditions more closely resemble conditions for the Avago measured device s-parameters. It could also slightly limit a short circuit condition at the transistor drain when the bias choke coil is at its self-resonant frequency. Figure 5 shows a DC choke coil, "DC_Feed" that is later replaced with an inductor in the built-up circuit. Note that the ATF54143 is an enhancement mode FET that requires a positive gate voltage with respect to its source to obtain the desired drain-to-source bias current of 60 mA. A voltage divider network is provided by Ra and Rb and is adjusted in the simulator to quickly obtain the required 60 mA drain-to-source current. Standard resistor values are used. Ra is arbitrarily set to 33 kΩ. Next, Rb is manually adjusted by entering standard resistor values to yield the desired bias current as shown in Figure 5. Note that Rg, the 10 kΩ resistor is not necessary for transistor DC bias, but acts as an "all-frequency" choke to effectively isolate the gate from the bias network "RF-wise". This will be important when the RF aspects of the design are accomplished. Nearly any resistor value is acceptable from a DC bias standpoint since no DC current flows through this resistor. Larger resistor values provide better RF isolation than smaller ones. A smaller resistor can be used in this position if it is determined that the transistor is unstable and requires parallel loading at the input to achieve stability. Adding a bypass capacitor to ground at the Ra, Rb, and Rg junction effectively AC grounds Rg. For now, the 10 kΩ resistor is used for the DC simulations and preliminary RF simulations.
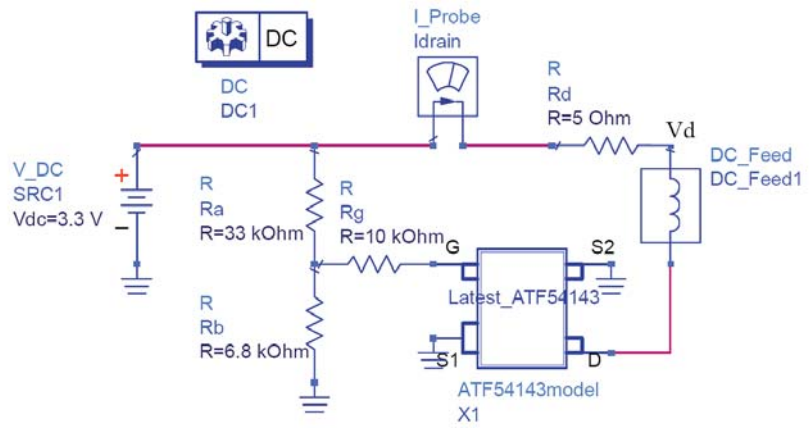
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Figure 5. DCbias.dsn

Figure 6 shows the DC simulation results with Ra set to 33 kΩ and Rb set to 6.8 kΩ. Note that the drain bias current is nearly 60 mA (61.38mA) and the drain voltage is nearly 3 Volt (2.993V). This is close enough to the target bias values.

freq	Idrain.i	Vd
0.0000 Hz	61.38 mA	2.993 V

Figure 6. DCbias.dds

An s-parameter simulation is now possible on the biased nonlinear model. DC blocking capacitors and 50 Ω terminations are added to the circuit input and output of Figure 5 to obtain the circuit shown in Figure 7. S-parameter simulations are now obtained from 100 MHz to 6 GHz with a frequency step of 10MHz. (The Avago ATF54143 datasheet indicates that device s-parameters were measured on a 20 mil thick PCB and recommends connecting two vias in parallel with each other on each source to ground. This was added to the Figure 7 circuit and found to have a minimal effect. The nonlinear model simulated s-parameter data without the ground vias closely matches measured s-parameter data. Thus, the PCB ground vias are not added as indicated in the datasheet.) Figure 8 plots nonlinear model simulated s-parameters and the Avago measured s-parameter data. Note the close similarity between the two s-parameter data sets.
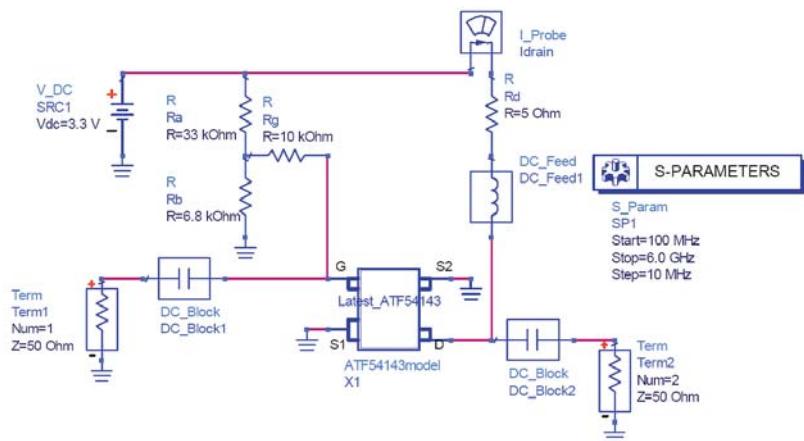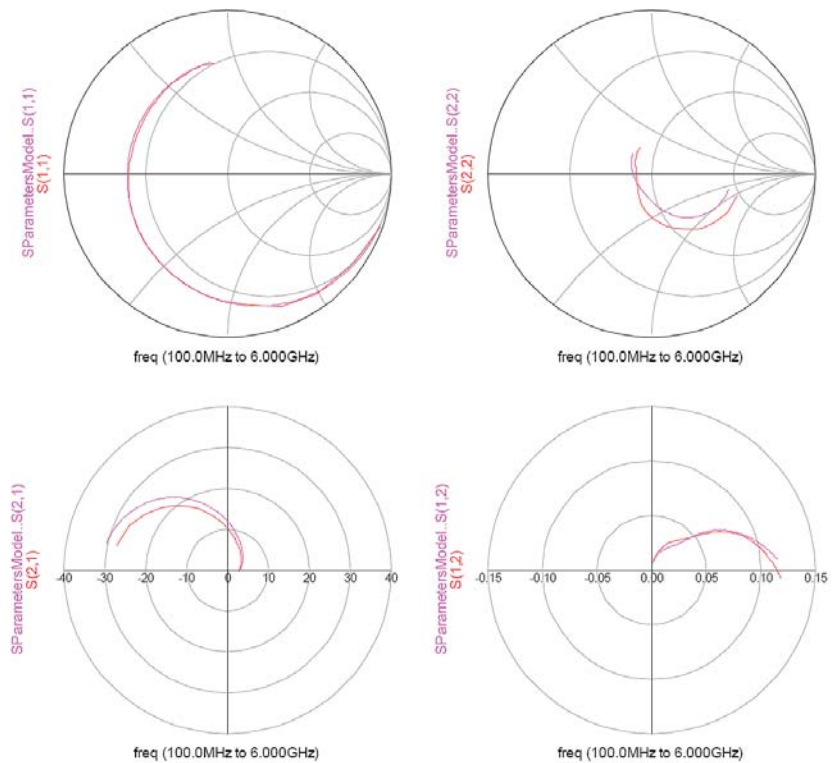

Figure 7. S-parametersModel.dsn

freq (100.0MHz to 6.000GHz)   freq (100.0MHz to 6.000GHz)

freq (100.0MHz to 6.000GHz)   freq (100.0MHz to 6.000GHz)

Figure 8. ATF54143_MeasVsModel_S-parameters.dds

S-Parameter Data Validation

It is beneficial to validate data obtained from any vendor if a measurement lab is available. In this case, s-parameter data is measured with an Intercontinental Microwave (ICM) transistor test fixture. The ICM transistor test fixture is used with the appropriate midsection and ICM TOSL-3001 calibration kit. Before calibration is performed, all TOSL-3001 calibration coefficients are loaded into the network analyzer. Each calibration standard has a unique set of coefficients that describe it's RF response. The ICM calibration coefficients used to describe the TOSL-3001 calibration kit are shown in Tables 1 and 2. The upper frequency limit for the ICM calibration kit is 6 GHz. Once the ICM calibration coefficients are loaded into the network analyzer, the TOSL calibration for the transistor test fixture is possible.

Figure 9 shows the measurement setup used to measure ATF54143 s-parameter data. The HP4142B DC Source/Monitor is connected to the E8364B network analyzer bias tees located on the back of that instrument. The HP4142B will supply 3.0 Volts to the Port 2 bias tee and will supply a voltage between 0 V and 1 V at the Port 1 bias tee. The current sourced from the HP4142B is limited to 100 mA to ensure that the 500 mA bias tee fuses are not accidentally blown. The HP4142B DC Source/Monitor should be disconnected or turned off during calibration to avoid blowing the port bias fuses in the network analyzer as an added safety precaution. The E8364B network analyzer source power is set to –25 dBm to ensure the measured device is not driven into compression during measurement. The network analyzer IF bandwidth is set to 300 Hz to limit noise and increase the dynamic range of the measurement system. The TOSL calibration is now performed using the ICM TOSL-3001 calibration kit.
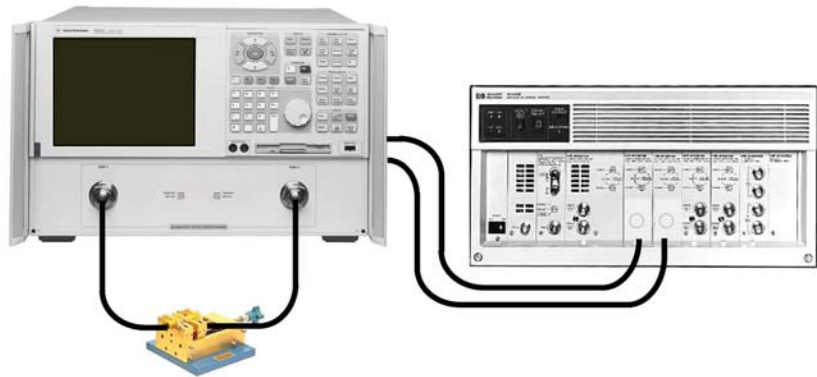
Figure 9. Transistor s-parameter measurement setup

Standard Class Assignments   Calibration Kit: ICM TOSL-3001

CLASS	A	B	C	D	E	F	G	Standard Class Label
$S_{11}A$	2							
$S_{11}B$	1							
$S_{11}C$	3							
$S_{11}A$	2							
$S_{11}B$	1							
$S_{11}C$	3							
Forward Transmission	4							
Reverse Transmission	4							
Forward Match	4							
Reverse Match	4							
Response	1	2	4					
Response & Isolation	1	2	4					
TRL Thru								
TRL Reflect								
TRL Line								
Adapter								

TRL Option

Cal Z0: _____ System Z0 _____ Line Z0

Set Ref: _____ Thru _____ Reflect

Table 1.

Calibration kit: 1CM TOSL-3001

STANDARD		C0 10^{-15}F	C1 10^{-27}F/Hz	C2 10^{-36}F/Hz2	C3 10^{-45}F/Hz3	Fixed or Sliding	Terminal Impedance Ω	Offset			Frequency (GHz)		Coax or Waveguide	Standard Label
#	TYPE	L0 10^{-12}H	L1 10^{-24}H/Hz	L2 10^{-33}H/Hz2	L3 10^{-42}H/Hz3			Delay pSec	Z0 Ω	Loss GΩ /s	MIN	MAX		
1	SHORT	0						0.49	154.8	0	0	6.1	COAX	SHORT
2	OPEN	37.7	4860	-5000	560			0	50	0	0	6.1	COAX	OPEN
3	LOAD					FIXED		1.485	120.9	0	0	6.1	COAX	LOAD
4	THRU							0	50	0	0		COAX	THRU
5														

Table 2.

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S-Parameters, Noise Figure, Gain, Stability, Circles, and Group Delay versus Frequency

Term
Term1
Num=1
Z=Z0

S2P
SNP1
File="ATF54143_ICM.s2p"

Term
Term2
Num=2
Z=Z0

Set System Impedance Z0:
VAR
VAR1
Z0=50

S-PARAMETERS
S_Param
SP1
Start=0.1 GHz
Stop=6 GHz
Step=0.1 GHz
CalcNoise=yes

Set S-parameter analysis frequency range. If an S-parameter file without noise data is used, the noise simulation results will be invalid.

OPTIONS
Options1
Temp=16.85
Tnom=25

Computation of Stability factors and circles:
MeasEqn
meas1

Figure 10. ATF54143_ICM_S-parameters.dsn

Once calibration is completed and verified, the HP4142B DC Source/Monitor is reconnected or turned back on as shown in Figure 9. Using the HP4142B is a very accurate way of setting/monitoring voltages and currents. First, the 3 Volt DC bias is supplied to Port 2 on the network analyzer through the Port 2 bias tee to bias the transistor drain terminal. The HP4142B DC Source/Monitor compliance is set to 100 mA so as to limit current into the bias tees. The desired bias current into Port 2 is 60 mA, thus the compliance (current limit) is set to 100 mA. Essentially, no current is needed to bias the gate of the FET connected to Port 1, so the compliance is set to 10 mA. The bias voltage on Port 1, which is connected to the transistor gate through the bias tee, is set to 0.5 Volt. Drain current is now measured with the HP4142B DC Source/Monitor and found to be slightly below 60 mA. The Port 1 (gate) voltage is slowly increased until 60 mA is measured with the HP4142B DC Source/Monitor going into Port 2 – the drain terminal. Once the drain-to-source current is set to 60 mA with the drain voltage at 3.0 V, the s-parameters are now measured and saved to a Touchstone file. Figure 10 uses an Amplifier Design Guide to plot the lab-measured s-parameters with the simulator.
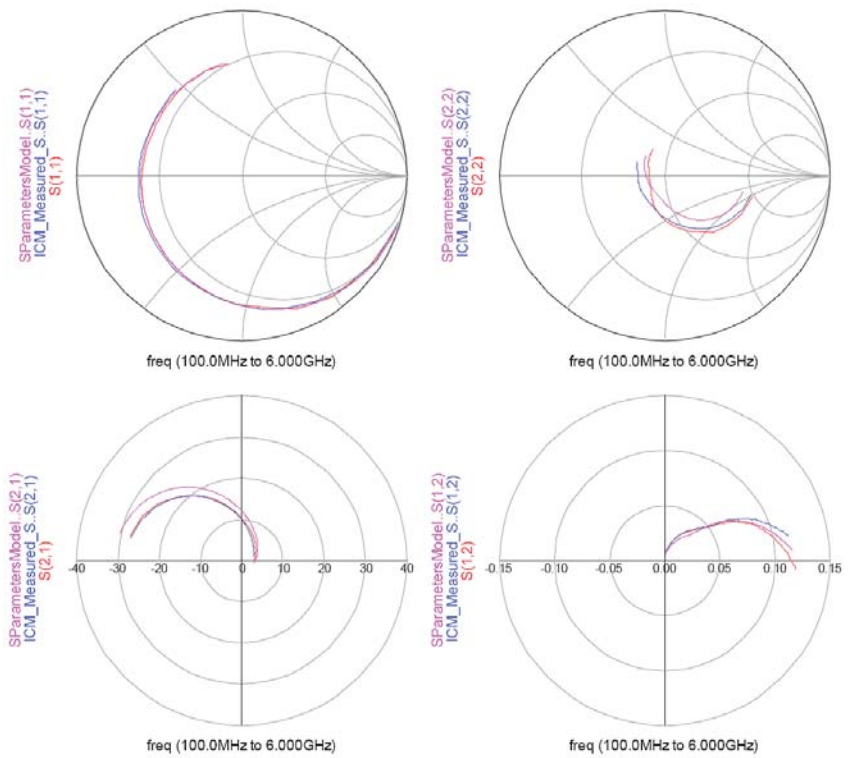
Figure 11. ATF54143_ALL3_S-parameters.dds

A comparison is now made between the Avago measured s-parameters, the nonlinear model generated s-parameters, and the lab measured s-parameters. Figure 11 plots all s-parameter results and shows that all are in close agreement with each other. Since measured data and modeled data are consistent with each other, any of these can be used to proceed with the linear design. Of course, third order intermodulation distortion and gain compression require the nonlinear model for simulation purposes. Noise figure simulation requires linear noise parameters. Noise parameters are included in the s-parameter Touchstone file ATF541433_3V60mA.s2p provided by Avago. This s-parameter data file also has data up to 18GHz where as the ICM data is only measured to 6 GHz due to the calibration kit frequency limitation. Stability should be considered for all frequencies or at least with data covering as much frequency range as possible. Thus, the Avago measured data is used to simulate stability, available gain, and noise figure.

ATF54143 Stability

A preliminary stability analysis is performed using an Amplifier Design Guide and the Avago measured s-parameter data as shown in Figure 12. Note that the stability analysis is performed from 100 MHz to 18 GHz – the entire range of the data file.

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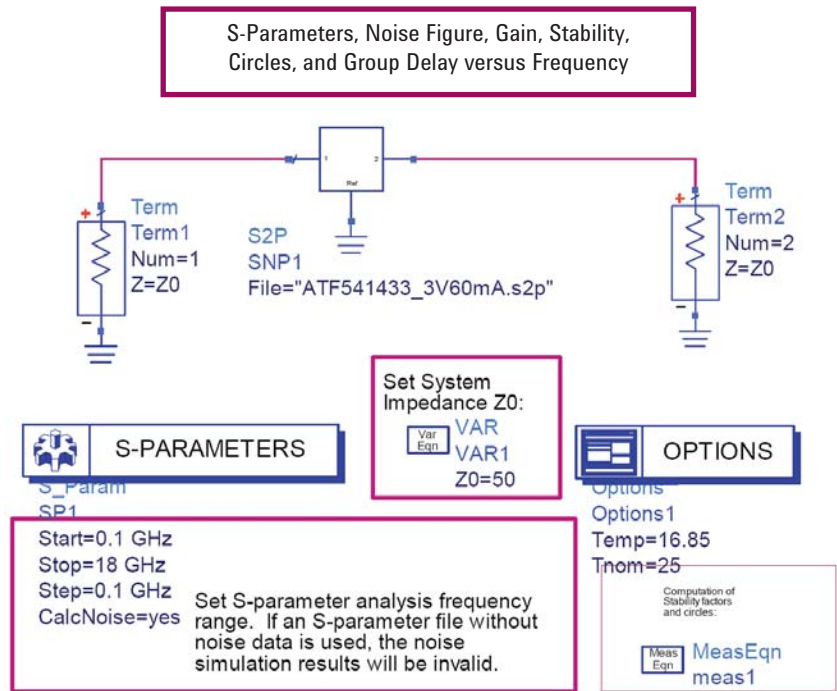
Figure 12. ATF54143_StabilityAnalysis.dsn

It is highly recommended that the amplifier circuit is made unconditionally stable at all frequencies to ensure that it does not produce unwanted oscillations. If the amplifier should happen to oscillate while being used in it's product environment, it may cause product malfunction. It can be very difficult to determine the root cause of product malfunction due to oscillating amplifiers. To achieve unconditional stability, Equations 7 through 10, show that $K \geq 1$ and $\{|\Delta| < 1$ or $B1 > 0$ or $B2 > 0\}$; or separately Equation 11 or Equation 12 geometric stability factors $\mu_{source} \geq 1$ or $\mu_{load} \geq 1$. The ADS Amplifier Design Guide calculates and displays Equations 7, 11, and 12. Note that satisfying K ≥ 1 does not indicate or guarantee unconditional stability. If either $\mu_{source} \geq 1$ or $\mu_{load} \geq 1$ then the amplifier circuit is guaranteed to be unconditionally stable. If the equations indicate unconditional stability, it means that the amplifier will not oscillate when its input and output are terminated with impedances having zero or positive resistances. In other words, as long as the input and output are terminated with reflection coefficient magnitudes between 0 and 1, inclusive, the circuit will not oscillate. If feedback through inductive coupling is introduced or modified, by putting the amplifier in a metal housing, the amplifier may still oscillate. Environmental conditions, such as temperature, can also produce unwanted oscillations. A change in temperature changes the active device s-parameters. To ensure unconditional stability, s-parameters should be taken under all extreme conditions and a stability analysis performed. One other way to ensure stability as far as environmental conditions are concerned is to provide significant margin to the stability conditions. In other words, make K >> 1 at all frequencies if possible.
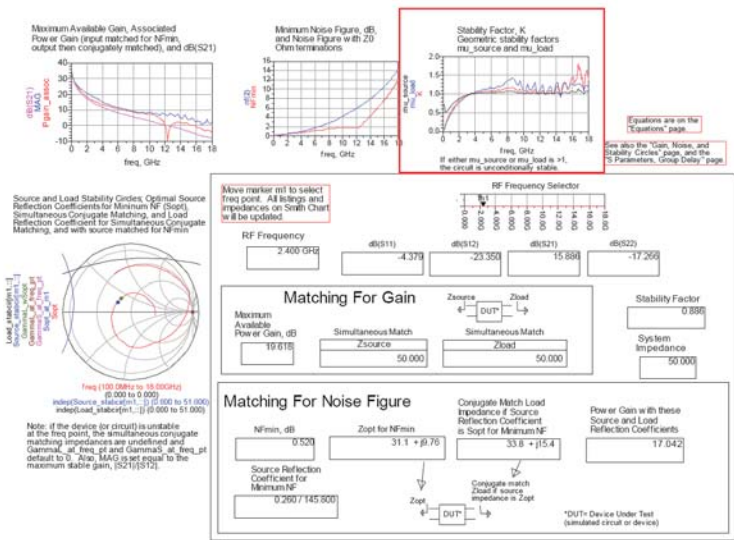
15

Figure 13. ATF54143_StabilityAnalysis data display. Insert from schematic menu pick DesignGuide > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay.

Figure 13 shows the Figure 12 analysis results. This plot was set up using one of the data display Amplifier Design Guides that correspond to the Stability Analysis Amplifier Design Guide used to set up the simulation. The Amplifier Design Guide plots K, μ_{source}, and μ_{load} (Equations 7, 11, and 12) as shown in the red box. Note that the Amplifier Design Guide plots stability factor K, which, on its own, is necessary, but not sufficient to guarantee unconditional stability. Either $|\Delta|$, B1, or B2 also have to be plotted to use K as the stability indicator. Satisfying either $\mu_{source} \geq 1$ or $\mu_{load} \geq 1$ guarantees unconditional stability. Observation of the Stability Factor K, geometric stability factors μ_{source} and μ_{load} all indicate potential instability below 4 GHz and marginal unconditional stability above 4 GHz. (Marginal unconditional stability above 4 GHz can only be assessed with μ_{source} and μ_{load} since K alone does not indicate unconditional stability.) Above 8 GHz, the data looks questionable since the K, μ_{source}, and μ_{load} plots have an up-and-down variation associated with them. Since the amplifier is used well below 8 GHz, this variation will be ignored to some degree. It is highly recommended that the amplifier is unconditionally stable at all frequencies to ensure that the circuit does not produce unwanted oscillations in or out of the operating frequency band. Thus, it is important to stabilize this device and ensure that unconditional stability exists at all frequencies. At frequencies above 8 GHz where variation in K, μ_{source}, and μ_{load} are noticed, a stabilizing network that provides significant stability margin is employed so that data inaccuracies can be ignored. Also note, that this is a preliminary stability analysis. If it is not possible to stabilize the ideal circuit without layout and component parasitics and still meet design objectives, it may not be possible to stabilize the device once it is placed in a physical layout. Therefore, an attempt is made to stabilize the device without parasitics. If the device is stabilized and still meets all the performance criteria, then parasitics are added. A new stability analysis is then performed. If the circuit is again unstable, attempts are made to stabilize the device with parasitics. Once the circuit is stable, it is checked to ensure that it still meets its design objectives.

Transistors are stabilized through the use of series and parallel feedback and series and parallel loading at the input and output. A combination of these networks may be necessary to get the desired stability results. Stabilizing network selection and approach depends on the type of device(s) used, the amplifier configuration, and design performance objectives. A common source FET amplifier has a relatively high input reflection coefficient and typically requires input loading to achieve stability. In a low noise amplifier application, however, resistive loss added to the amplifier input degrades noise figure and should be avoided if possible.

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An ADS Amplifier Design Guide that stabilizes an unstable circuit is used to stabilize the transistor circuit as shown in Figure 14 (From a schematic, select DesignGuide > Amplifier > S-Parameter Simulations > Feedback Network Optimization to Attain Stability). The ADS default Amplifier Design Guide has parallel feedback and parallel loading at the input and output. Unconditional stability is desired at all frequencies, thus, the Amplifier Design Guide default stabilizing networks are modified. Series loading (R1) is added at the output, the inductor in the feedback path is removed, and the capacitors CFB and COUT are changed to DC blocking capacitors by setting them to 1uF. Since this amplifier is used in a low noise application, it is desirable to limit loss at the device input, which degrades amplifier noise figure. Thus, capacitor CIN is changed to 0.5 pF to limit input loading at the operating frequency since loss added at the input degrades noise figure. The 0.5 pF capacitor has a relatively high reactance at 2.5 GHz and this reactance decreases with an increase in frequency. This allows input parallel loading at higher frequencies and very little loading at 2.5 GHz. This type of loading can be thought of as frequency selective loading. The CIN capacitor is also renamed to C1 such that it is not altered during the optimization process. Input series loading also degrades noise figure. Series loading could be frequency selective as well by putting an inductor in parallel with the load resistor, but inductors typically have higher parasitics than do capacitors, thus input series loading will not be considered in this design. Resistive feedback can also degrade noise figure. In this particular case, the resistive feedback helps stabilize the circuit at low frequencies and has little impact at the operating frequency.
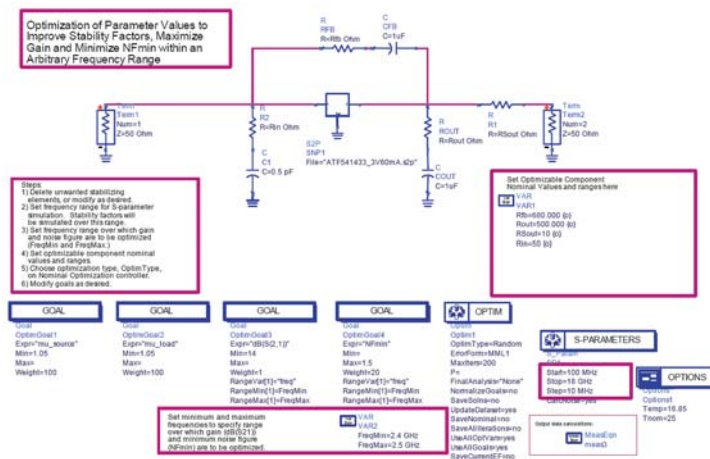

Figure 14. ATF54143_StabilityOpt.dsn

The optimization goals are set to optimize for stability, maximum gain, and minimum noise figure. The stability goals OptimGoal1 and OptimGoal2 are set to a Min = 1.05 as a default over the entire simulation frequency range. These goals ensure that $\mu_{source} \geq 1$ and $\mu_{load} \geq 1$, which indicates unconditional stability. Note that if either $\mu_{source} \geq 1$ or $\mu_{load} \geq 1$ then the other is, by definition, greater than unity. OptimGoal3 is set to a Min = 14 dB for dB(S21) over the 2.4 GHz to 2.5 GHz operating frequency range. Noise figure is set to a Max = 1.5 dB over the same operating frequency range. The starting values for each of the stabilizing components in the optimization are arbitrarily chosen as R_{fb} = 680 Ω, R_{in} = 50 Ω, RS_{out} = 10 Ω, and R_{out} = 500 Ω. The optimization simulation is now executed and the results are shown in Figure 15. The optimized resistance values shown in the figure indicate that R_{fb} = 547.4 Ω, R_{in} = 278.7 Ω, RS_{out} = 6.1 Ω, and R_{out} = 216 Ω and unconditional stability is achieved from 100 MHz to 18 GHz. Also note that at 2.5 GHz gain is 14.17 dB, which exceeds the design target of 12 dB. The minimum noise figure in the plot at 2.5 GHz is 1.03 dB as indicated. The minimum noise figure is not necessarily the noise figure of the circuit as indicated by Equation 21, but depends on how the device input is terminated. Note that the desired 2.5 dB noise figure is possible with this circuit.
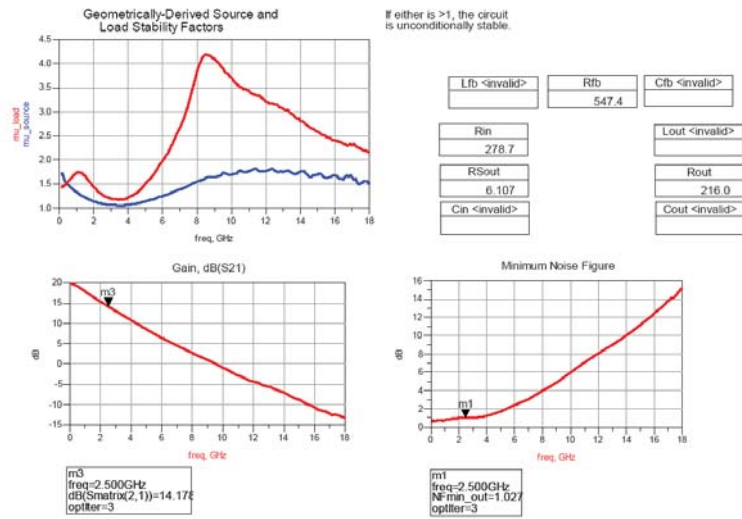
Figure 15. ATF54143_StabilityOpt.dds

Component and layout parasitics are not included in the design yet. Typically, if the preliminary analysis does not meet the design criteria, the final actual circuit with parasitics will not meet the objectives. In other words, parasitics typically degrade RF performance. In this case, the preliminary analysis indicates the transistor and amplifier topology chosen may indeed yield a design that meets all design objectives. Next, some of the component parasitics and preliminary layout parasitics are considered to determine what affects they may have on circuit performance.

Component parasitics include loss and unexpected reactance. Inductors have losses and parasitic capacitance whereas capacitors have loss and parasitic inductance. For this design, an inductor is needed to feed DC bias into the FET drain terminal. Figures 5 and 7 show an ideal DC feed (choke) to inject bias current into the FET drain. A Coilcraft Midi series air-wound inductor replaces the ideal DC feed. The inductor is needed merely to feed DC bias current to the FET drain. Ideally, a very large inductance is needed for the DC feed coil. Inductor parasitic capacitance limits the allowable inductance value due to self-resonance. A 27 nH Coil Craft Midi series inductor has a minimum self-resonance frequency of 2.7 GHz. This gives the highest possible inductive reactance at the 2.5 GHz operating frequency while the inductor self-resonant frequency is still above the amplifier operating frequency.
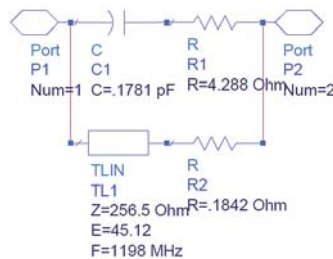

Figure 16. CC1812SMS.dsn

Figure 16 shows an equivalent circuit model of the Midi series air-wound inductor supplied by CoilCraft with part number 1812SMS-27N. Notice the transmission line TL1 in the model. Using a transmission line in this model causes the model to diverge from actual inductor performance at frequencies above self-resonance due to the nature of transmission lines. A subcircuit (CC1812SMS) is now created with the 27 nH inductor lumped equivalent circuit for use in the amplifier circuit.
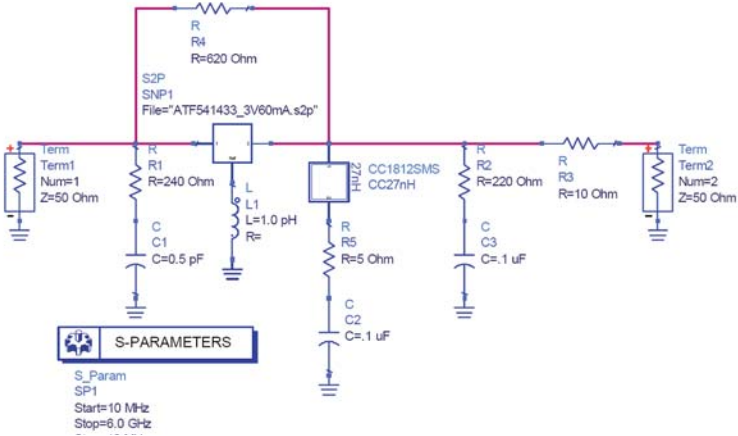

Figure 17. ATF54143amp1_1pH.dsn

The stabilized circuit is now updated with standard resistor values and the 27 nH bias choke coil subcircuit from Figure 16 as shown in Figure 17. The parallel input load resistor R1 is optimized to 278.7 Ω. A 240 Ω standard value resistor is used for the parallel input load. The output parallel load resistor R2 optimized to 216 Ω. A 220 Ω standard value resistor is used for the output parallel load. The series output load R3 optimized to 6.1 Ω. A 10 Ω standard value resistor is used for the series output load. The feedback resistor R4 optimized to 547.4 Ω. A 620 Ω standard value resistor is used for the feedback resistor as shown. Figure 5 shows that the 3.3V bias is first fed through a 5 Ω resistor R5 before being fed into the choke coil to drop the drain bias from the 3.3 V battery voltage to 3.0 V. Note in Figure 17 that the "cold" end of the 27 nH inductor is connected in series with this 5 Ω resistor. The 3.3 V battery is not needed for the s-parameter analysis, but the effects of the bias choke (27 nH inductor) is included in the RF simulation. The bias choke and 5 Ω resistor series combination is bypassed with the 0.1 µF capacitor, C2, as shown in Figure 17. The battery is connected to the 5 Ω resistor and 0.1 µF capacitor junction in the final circuit. Thus, this node is grounded "RF-wise" due to C2.

Layout parasitics that can wreak havoc on RF circuit performance include ground or lead inductance and parasitic capacitance on the signal path. Minute amounts of ground or lead inductance can cause a calculated unconditionally stable circuit to be unstable. Ground inductance can also cause actual measured circuit gain to be significantly dissimilar to gain predicted with ideal s-parameter simulations. Resistive loading or feedback is used to stabilize a transistor as discussed earlier. Parasitic inductance in the ground or layout traces can effectively isolate such stabilizing circuits from the active device. Parasitic ground inductance in a transistor source or emitter circuit is a form of reactive series feedback that can cause unwanted oscillations. The circuit in Figure 17 includes parasitic ground inductance at the FET source terminal represented by the lumped inductor L1. At this point in the design process, it is helpful to find out how sensitive the circuit may be to this unavoidable parasitic ground inductance. The circuit in Figure 17 has virtually no parasitic ground inductance since the L1 inductance value is set to 1 pH, but the inductor is inserted for the analysis. Later, this inductance will be increased to determine what effects it has on final circuit performance.

Figure 18 shows an s-parameter plot from the Figure 17 analysis. Both |S11| and |S22| are inside the unit radius Smith chart, which is a necessary, but not sufficient condition for unconditional stability. The dB(S21) plot shows the 50 Ω gain of 13.82 dB at 2.5 GHz which is slightly lower than the 14.17 dB of gain predicted by Figures 14 and 15. The lower gain is partly due to the resistor values being changed to standard value resistors and the additional loss added by the 27 nH bias tee choke inductor.

A stability analysis could be performed on this circuit since the |S11| and |S22| are inside the unit radius Smith chart, but a study of ground inductance effects on circuit performance is now desirable. As mentioned earlier, the lumped inductor L1 in Figure 17 is added to represent parasitic ground inductance. An arbitrary value of 1nH is now used to get an indication on how sensitive the circuit is to parasitic ground inductance. The 1 nH inductance value is very small. Higher values of ground inductance are not uncommon in PCB layouts. Figure 19 shows the L1 parasitic ground inductor from Figure 17 is changed to 1nH. Everything else in the circuit remains unchanged. The simulation is now executed from 10 MHz to 10 GHz.
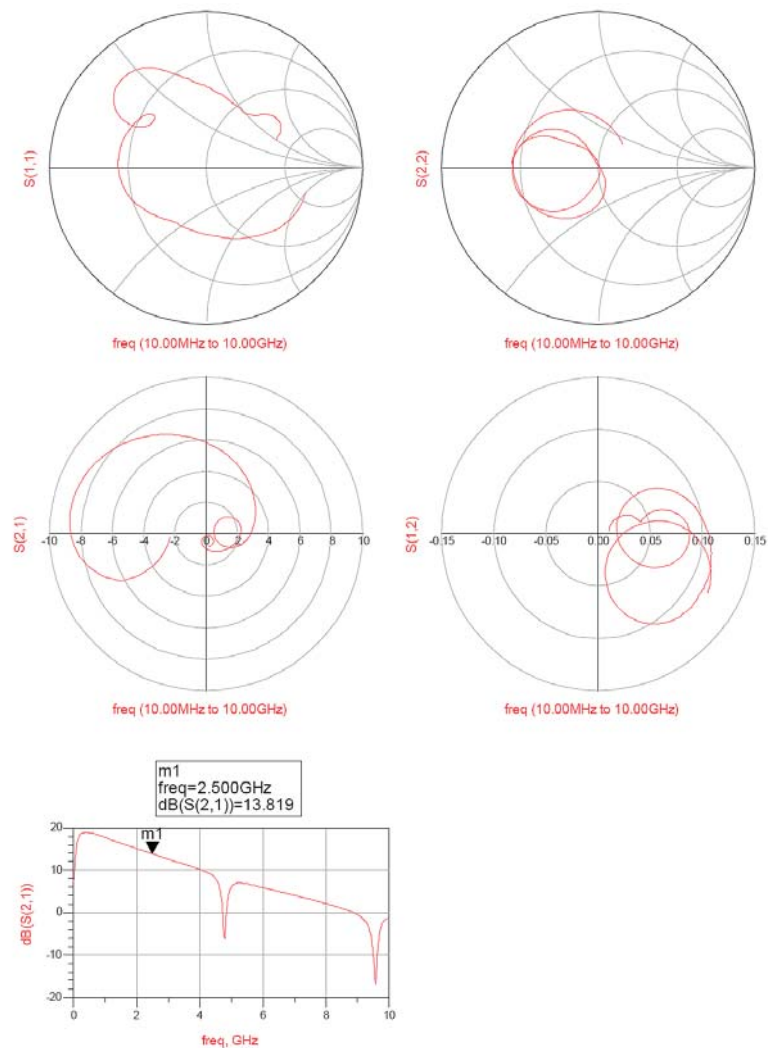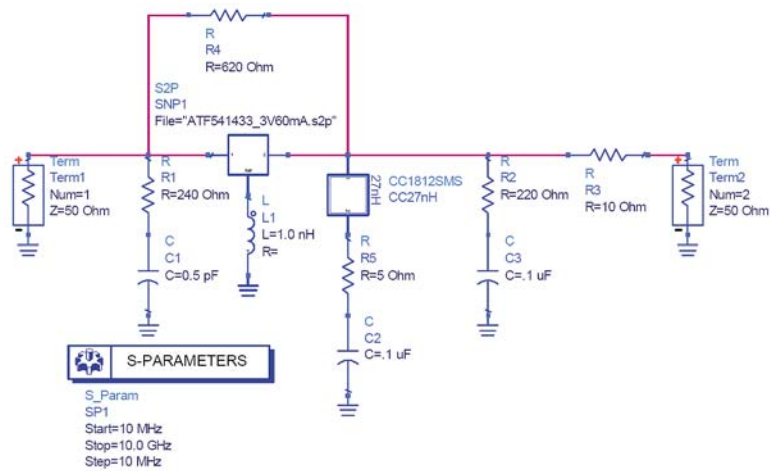
Figure 18. ATF54143amp1_1pH.dds

Figure 19. ATF54143amp1_1nH.dsn

Figure 20 displays the Figure 19 circuit s-parameters. The |S11| is outside the unit radius Smith chart indicating an input reflection coefficient magnitude greater than unity. This indicates that small amounts of parasitic ground inductance make this circuit potentially unstable at some frequencies. Since the input reflection coefficient magnitude is greater than unity, a stability analysis is not necessary to determine whether or not the amplifier has a propensity to oscillate. Having the output terminated in 50 Ω already causes the input reflection coefficient magnitude to become greater than unity, in other words producing negative resistance – a condition needed for oscillation. The dB(S21) plot shows that the 50 Ω gain at 2.5 GHz is reduced from 13.82 dB to 7.48 dB. That's a 6.3 dB gain loss from the circuit without parasitic ground inductance. This simple analysis indicates how crucial the layout is with respect to the parasitic ground inductance at the source lead. Every effort is made to minimize layout ground inductance so the amplifier meets the gain requirement and does not oscillate in the application. The analysis also indicates that the stability networks need to load the circuit more out-of-band in case the layout parasitic ground inductance is not low enough. There is no way to totally eliminate the ground inductance, thus, more loading is employed. Since the transistor high input reflection coefficient is causing the problem, loading the output has little affect on stability for this circuit. Currently, the input is loaded with a parallel 240 Ω resistor at high frequencies. Loading only occurs at high frequencies because of the 0.5 pF capacitor C1. Figure 21 shows the input reflection coefficient plotted on an admittance plane Smith chart. The marker is moved to a location on the trace that has the highest value of negative conductance. Now the reciprocal of the conductance gives the additional parallel load necessary to move the input reflection coefficient magnitude to the edge of the Smith chart. As indicated by the marker, an additional parallel input load of 200 Ω is required to move the input reflection coefficient magnitude to unity. The total parallel load is therefore 109 Ω. More margin is needed, thus the 240 Ω resistor is adjusted to a smaller value and set to 50 Ω to stabilize the device input with greater margin. Since the bypass input loading capacitor is small, the input parallel 50 Ω resistor has little contribution to the circuit at 2.5 GHz.
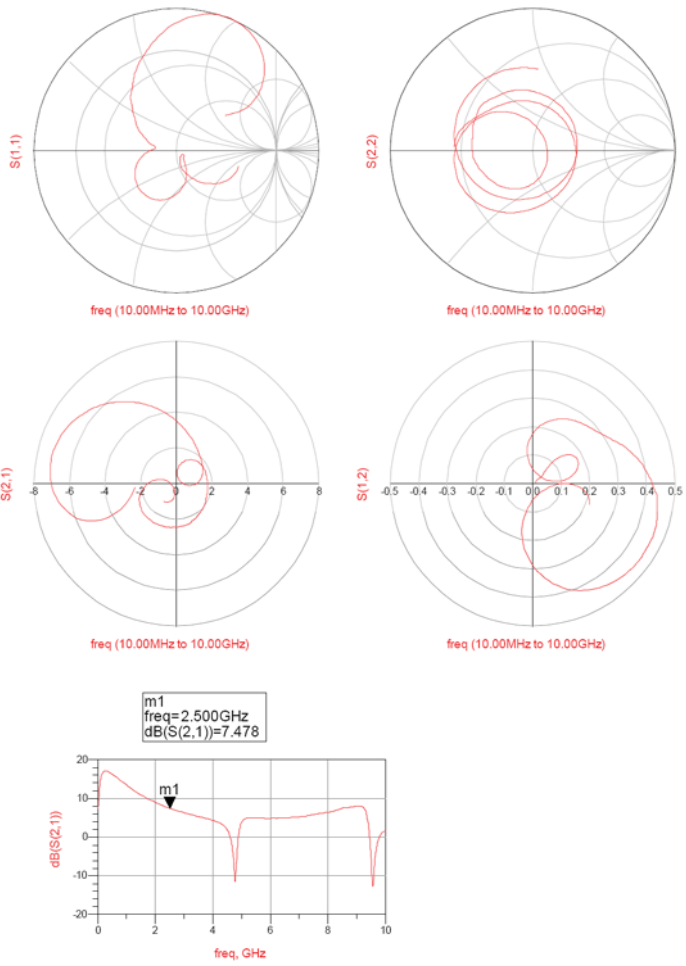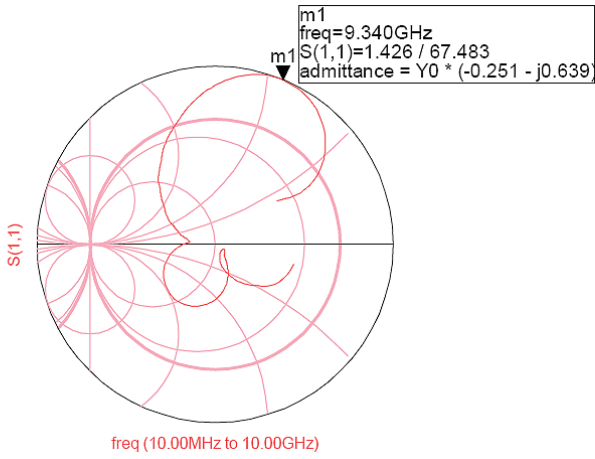
S(1,1)

freq (10.00MHz to 10.00GHz)

S(2,2)

freq (10.00MHz to 10.00GHz)

S(2,1)

-8 -6 -4 -2 0 2 4 6 8

freq (10.00MHz to 10.00GHz)

S(1,2)

-0.5 -0.4 -0.3 -0.2 -0.1 0.0 0.1 0.2 0.3 0.4 0.5

freq (10.00MHz to 10.00GHz)

m1
freq=2.500GHz
dB(S(2,1))=7.478

m1

dB(S(2,1))

freq, GHz

Figure 20. ATF54143amp1_1nH.dds

m1
freq=9.340GHz
S(1,1)=1.426 / 67.483
admittance = Y0 * (-0.251 - j0.639)

m1

S(1,1)

freq (10.00MHz to 10.00GHz)

Figure 21. ATF54143amp1_1nH_Admittance
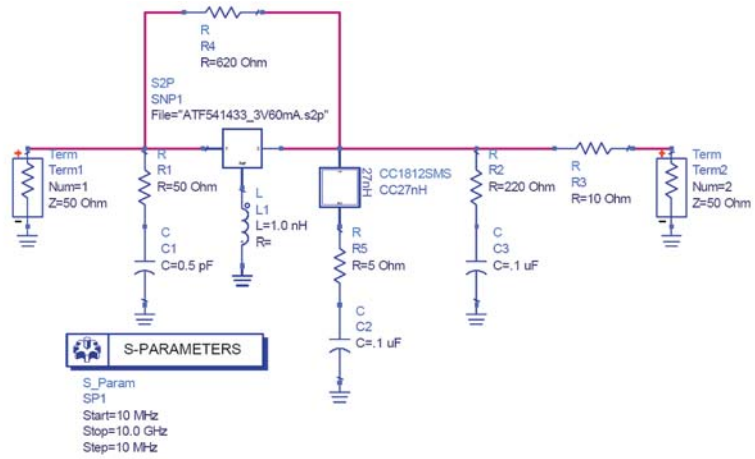
Figure 22. ATF54143amp1_1nH_Stabilize.dsn

Figure 22 shows the input parallel load resistor set to 50 Ω. The parasitic ground inductance is still set to 1 nH. Figure 23 shows the analysis results. With the parallel input 50 Ω resistor R1, the input reflection coefficient magnitude remains less than unity at all frequencies from 10 MHz to 10 GHz. The 50 Ω gain is 7.47 dB which is only 0.01 dB less than the case with the 240 Ω input parallel resistive load. This shows that the input loading has little affect on the circuit at 2.5 GHz due to the 0.5 pF capacitor being used as the bypass, but has a huge affect at higher frequencies. Since both input and output reflection coefficient magnitudes remain less than unity when the circuit input and output is terminated with 50 Ω, a stability analysis is now performed. Note that because the input and output reflection coefficient magnitudes are less than unity, doesn't mean the circuit is unconditionally stable. There may still be source or load terminations other than 50 Ω that can cause unwanted oscillations.
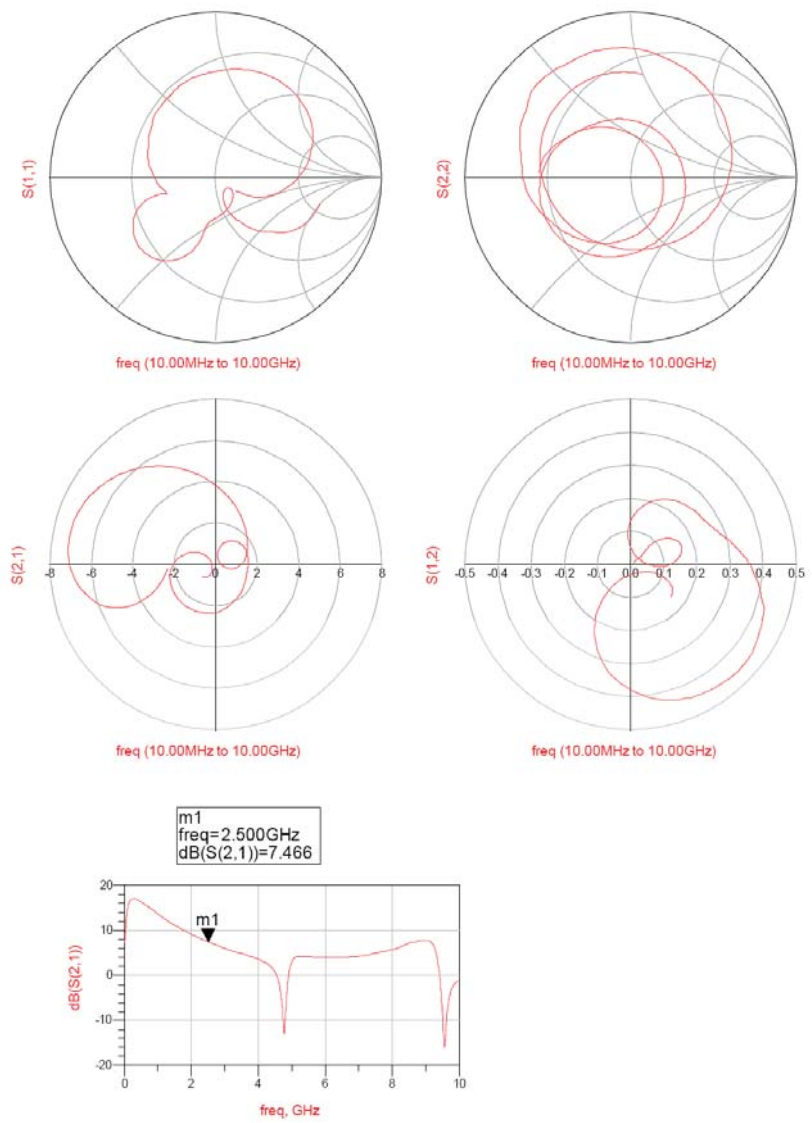
S(1,1)

freq (10.00MHz to 10.00GHz)

S(2,2)

freq (10.00MHz to 10.00GHz)

S(2,1)

-8 -6 -4 -2 0 2 4 6 8

freq (10.00MHz to 10.00GHz)

S(1,2)

-0.5 -0.4 -0.3 -0.2 -0.1 0.0 0.1 0.2 0.3 0.4 0.5

freq (10.00MHz to 10.00GHz)

m1
freq=2.500GHz
dB(S(2,1))=7.466

m1

dB(S(2,1))

20
10
0
-10
-20

0   2   4   6   8   10

freq, GHz

Figure 23. ATF54143amp1_1nH_Stabilize.dds

24
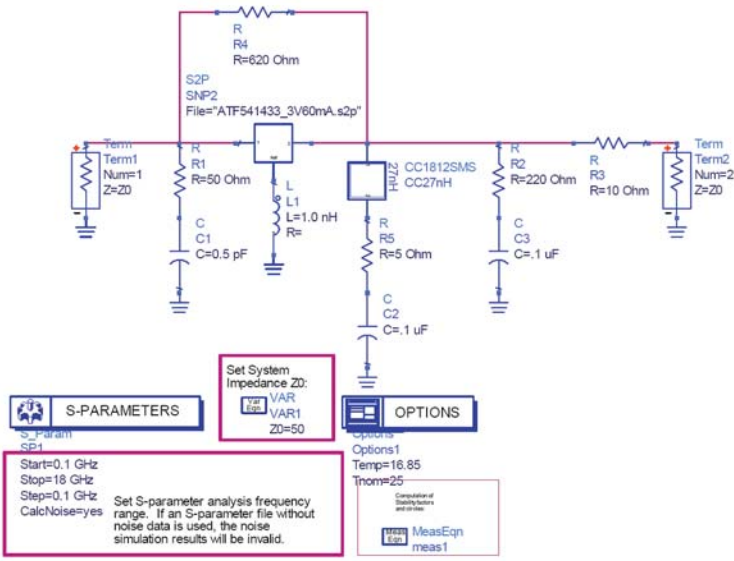
Figure 24. ATF54143_StabilityAnalysis2.dsn

Figure 24 is a stability analysis from 100 MHz to 18 GHz with the parasitic ground inductance set to 1 nH and the input parallel load resistor set to 50 Ω from Figure 22. The 50 Ω gain of 7.47 dB plotted in Figure 23 is not adequate gain for the 12 dB design goal. Stability is checked for the case of 1 nH ground inductance before investigating the next case of parasitic ground inductance.

Figure 25 is the same ADS Amplifier Design Guide data display from before that plots Equations 7, 11, and 12 – stability factors K, μ_{source}, and μ_{load} respectively. The circuit from Figure 24 data indicates potential instability between 6 GHz and 9.5 GHz as shown in the red box since μ_{source} < 1 and μ_{load} < 1.

Before making any further adjustments to stabilizing networks, the parasitic ground inductance L1 is adjusted down to 0.5 nH. The 1nH value was arbitrarily chosen to begin with, so it is helpful to see how sensitive the circuit is when the parasitic ground inductance is cut in half. Figure 26 shows the new circuit set up with the 0.5 nH parasitic ground inductance L1 for the stability analysis.
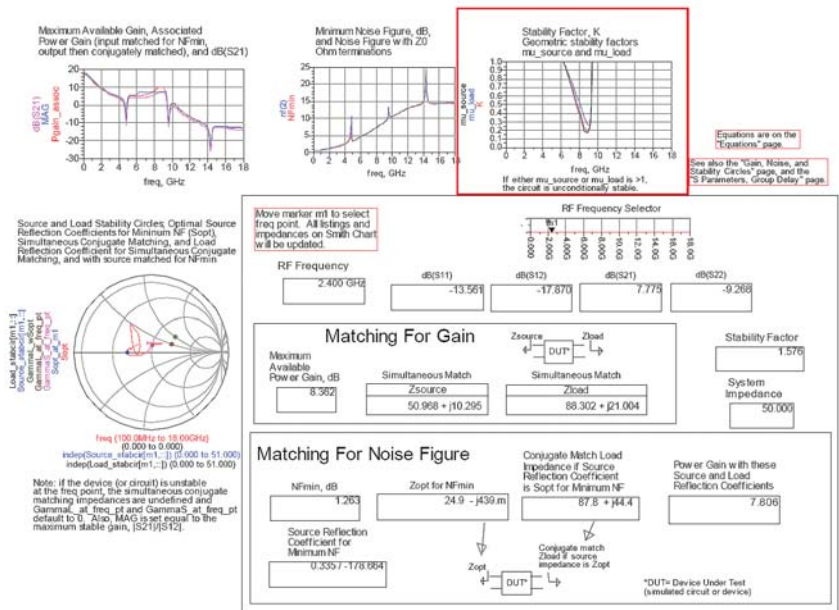
Maximum Available Gain, Associated
Power Gain (input matched for NFmin,
output then conjugately matched), and dB(S21)

Minimum Noise Figure, dB,
and Noise Figure with Z0
Ohm terminations

Stability Factor, K
Geometric stability factors
mu_source and mu_load

Equations are on the
"Equations" page.

If either mu_source or mu_load is >1,
the circuit is unconditionally stable.

See also the "Gain, Noise, and
Stability Circles" page, and the
"S Parameters, Group Delay" page.

Source and Load Stability Circles; Optimal Source
Reflection Coefficients for Minimum NF (Sopt),
Simultaneous Conjugate Matching, and Load
Reflection Coefficient for Simultaneous Conjugate
Matching, and with source matched for NFmin

freq (100.0MHz to 18.00GHz)
(0.000 to 0.000)
indep(Source_stabcir[m1,::]) (0.000 to 51.000)
indep(Load_stabcir[m1,::]) (0.000 to 51.000)

Note: if the device (or circuit) is unstable
at the freq point, the simultaneous conjugate
matching impedances are undefined and
Gammal_at_freq_pt and GammaS_at_freq_pt
default to 0. Also, MAG is set equal to the
maximum stable gain, |S21|/|S12|.

Move marker m1 to select
freq point. All listings and
impedances on Smith Chart
will be updated.

RF Frequency Selector

RF Frequency

dB(S11)	dB(S12)	dB(S21)	dB(S22)
2.400 GHz	-13.561	-17.870	7.775	-9.268

Matching For Gain

Maximum Available Power Gain, dB	Simultaneous Match Zsource	Simultaneous Match Zload	Stability Factor
8.382	50.968 + j10.295	88.302 + j21.004	1.576

System Impedance 50.000

Matching For Noise Figure

NFmin, dB	Zopt for NFmin	Conjugate Match Load Impedance if Source Reflection Coefficient is Sopt for Minimum NF	Power Gain with these Source and Load Reflection Coefficients
1.263	24.9 - j439.m	87.8 + j44.4	7.806

Source Reflection Coefficient for Minimum NF
0.335 / -178.664

Conjugate match Zload if source impedance is Zopt

*DUT= Device Under Test
(simulated circuit or device)

Figure 25. ATF54143_StabilityAnalysis2.dds

Figure 27 displays the Figure 26 simulation results with ground parasitic inductance set to 0.5 nH. K, μ_{source}, and μ_{load} are plotted and highlighted in the red box. The plot indicates unconditional stability from 100 MHz to 18 GHz with more stability margin at higher frequencies as desired. At this stage of the design, it is not yet known how much parasitic ground inductance at the transistor source is contained in the PCB layout because the layout is not yet started. Special attention is given to the layout procedure to ensure that parasitic ground inductance at the transistor source is kept as low as possible. Once the layout is complete, EM simulations give an estimate on the amount of parasitic ground inductance. If estimated parasitic ground inductance is too high on the initial layout, the layout is revised in an attempt to lower the PCB ground inductance parasitic. Once electromagnetic (EM) simulations are performed on grounding and other layout features, a stability and gain analysis with PCB layout parasitics included are performed to ensure the amplifier meets all design objectives.

S-Parameters, Noise Figure, Gain, Stability,
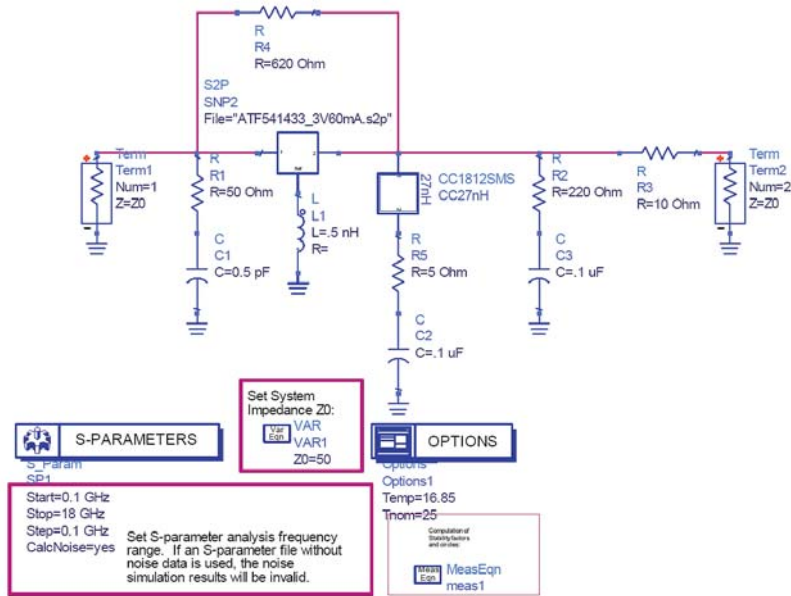Circles, and Group Delay versus Frequency

R
R4
R=620 Ohm

S2P
SNP2
File="ATF541433_3V60mA.s2p"

Term
Term1
Num=1
Z=Z0

R
R1
R=50 Ohm

C
C1
C=0.5 pF

L
L1
L=.5 nH
R=

CC1812SMS
CC27nH
27nH

R
R5
R=5 Ohm

C
C2
C=.1 uF

R
R2
R=220 Ohm

R
R3
R=10 Ohm

C
C3
C=.1 uF

Term
Term2
Num=2
Z=Z0

Set System
Impedance Z0:

VAR
VAR1
Z0=50

S-PARAMETERS

S_Param
SP1
Start=0.1 GHz
Stop=18 GHz
Step=0.1 GHz
CalcNoise=yes

Set S-parameter analysis frequency
range. If an S-parameter file without
noise data is used, the noise
simulation results will be invalid.

OPTIONS

Options
Options1
Temp=16.85
Tnom=25

Computation of
Stability factors
and circles

MeasEqn
meas1

Figure 26. ATF54143_StabilityAnalysis3.dsn

The gain, noise figure, and stability plots of Figure 25 show three spikes over the
100 MHz to 18 GHz frequency range. The transmission line used in the Coilcraft 27 nH
inductor model causes these spikes in the frequency response plots. The actual Coilcraft
inductor does not behave as suggested by the model above its self-resonance frequency.
A one-port measurement of the inductor is made using an E8364B network analyzer up to
6GHz and saved to a touchstone file named Lp1812SMS_27NG. This one-port measured
data file is now used in the amplifier circuit simulation to more accurately predict the
behavior of the amplifier circuit above the self-resonant frequency of the inductor up to
6 GHz. It was noticed during the inductor measurement that the results above the self
resonant frequency are sensitive to the position of the inductor in the fixture. These
variations cause more variability in the model prediction results above the 2.7 GHz
inductor self-resonant frequency. In other words, it is more difficult to get the circuit
model data to agree with final circuit measured data especially above the inductor self-
resonant frequency because of the measurement sensitivity.
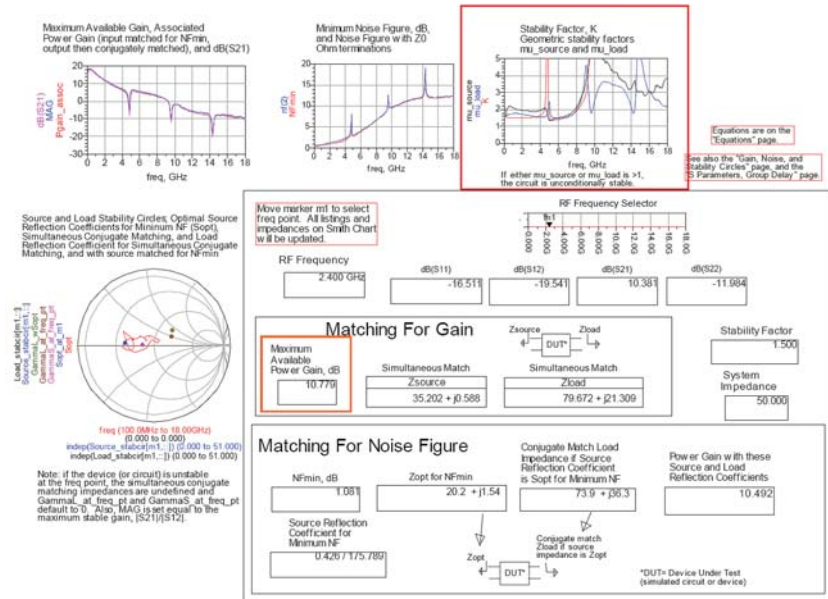
Figure 27. ATF54143_StabilityAnalysis3.dds

Figure 28 shows the amplifier circuit with the 27 nH inductor one-port s-parameter measurements included in place of the Coilcraft lumped equivalent model. Figure 29 presents the Figure 28 simulation results. The inductor primary self-resonant frequency response is still noticeable in the amplifier frequency response plots as expected, although it is not as pronounced.
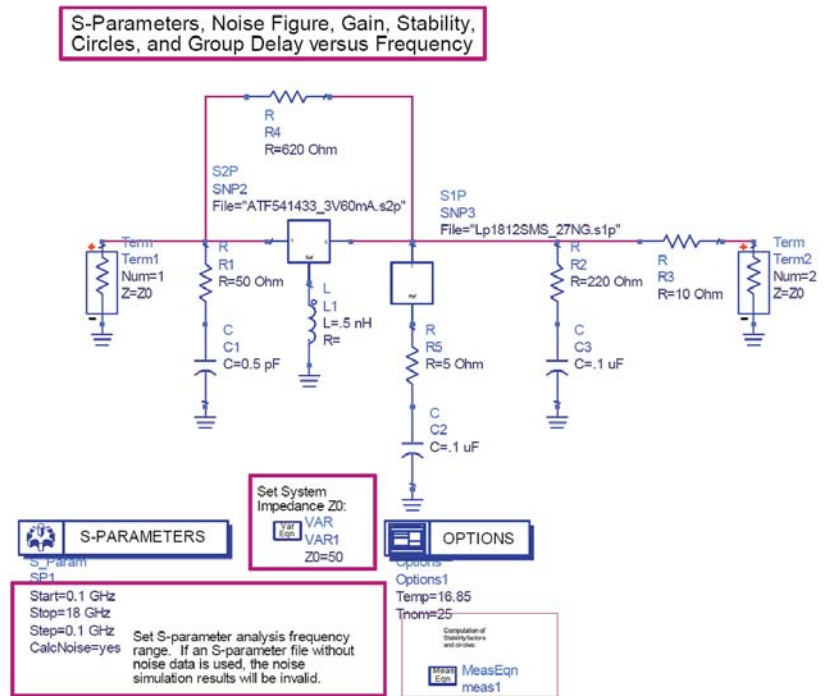
Figure 28. ATF54143_StabilityAnalysis4.dsn

Maximum Available Gain is displayed and highlighted with orange boxes in Figures 27 and 29. The predicted maximum possible gain is around 10.8 dB in both figures. This is 1.2 dB below the 12 dB design goal. Note that this predicted gain value is obtained with an arbitrary estimated amount of transistor source terminal parasitic ground inductance – 0.5 nH for Figures 27 and 29. Although the gain is below the target value in these simulations, the gain without parasitic inductance is well above the target value. A matching network is added at the amplifier input. In this case, a parallel inductor followed by a series capacitor is added. These values have not yet been calculated, but a preliminary match analysis indicates that the parallel inductor coming from the 50 Ω source followed by a series capacitor going into the transistor input provides a valid matching topology for the amplifier input. The matching design procedure is further explained later for the final input matching analysis. The approximate matching inductor value allows selection from a family of inductors that may be used. This allows a layout of the inductor footprint. In this case, a CoilCraft air core inductor from the Mini-Spring family of inductors provides a range of inductors suitable for the input matching network. Next, the amplifier circuit is laid out with special attention to grounding the FET source terminals. Once the layout is completed, an EM simulation predicts parasitic ground inductance at the transistor source terminal. With an estimate of parasitic inductance, new predictions of gain and stability are possible.
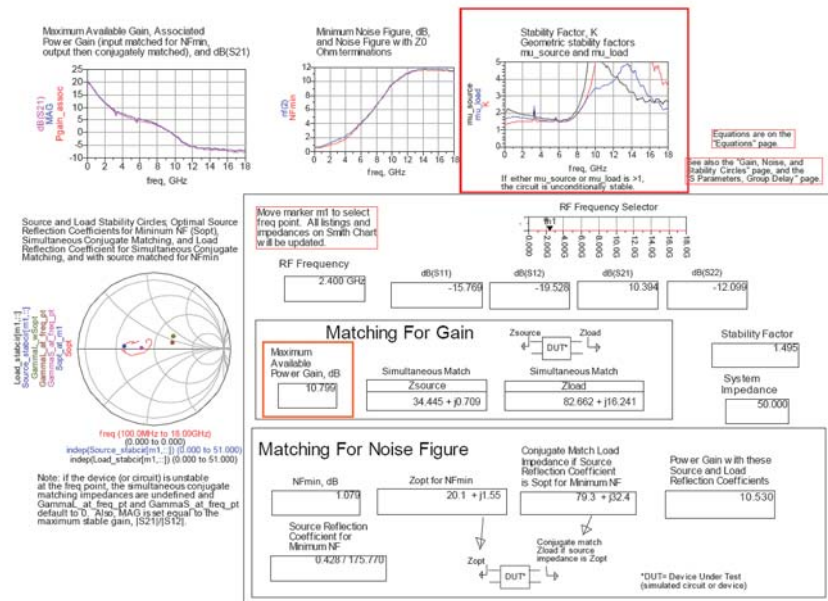
Figure 29. ATF54143_StabilityAnalysis4.dds

Amplifier EM/Circuit Co-Simulation and PCB Fabrication

The amplifier is built on Arlon 25N, which is available in many standard laminate thicknesses. Arlon 25N has a dielectric constant of 3.38 and a loss tangent of about 0.0023 at 2.5 GHz. Double-sided laminate having 1 ounce copper on each side, with a 30 ±3 mil thickness is selected for the design. Arlon 25N has a very consistent dielectric constant over frequency and temperature and is easily processed by manufacturers that process standard FR4 PCBs. Since performance specifications are very consistent and repeatable, using the Arlon 25N material greatly enhances the possibility of completing a one-pass design. In other words, the 25N material properties are used in the EM and circuit simulations to get an accurate simulation of PCB and circuit performance before resources are committed to actually building a board. Circuit repeatability from lot-to-lot is also greatly increased due to the repeatability of the Arlon 25N material.

Figure 30 shows the amplifier layout top layer and Figure 31 shows the layout bottom layer. All components are located on the top layer as shown by the figures. EM simulations are now performed so that PCB effects can be included in the circuit analysis. Each critical layout node is simulated individually and results combined with a circuit analysis to include PCB effects. The EM/Circuit Co-Simulation feature in ADS is then employed to combine the EM results with the circuit simulation. Linecalc is used to design the input and output 50 Ω transmission lines. Each line is 250 mil long so that a TRL calibration kit can be used for measurement. Arlon 25N material properties are used in Linecalc to ensure correct line dimensions.
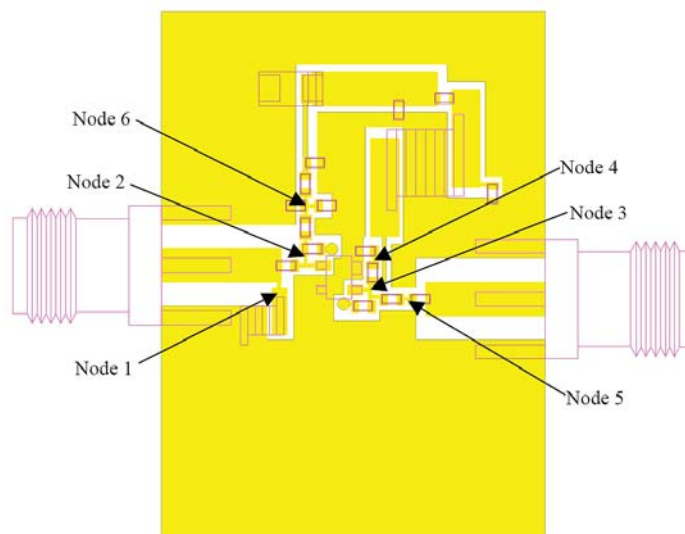
Figure 30. AvagoEnhGND.dsn – TopMetal
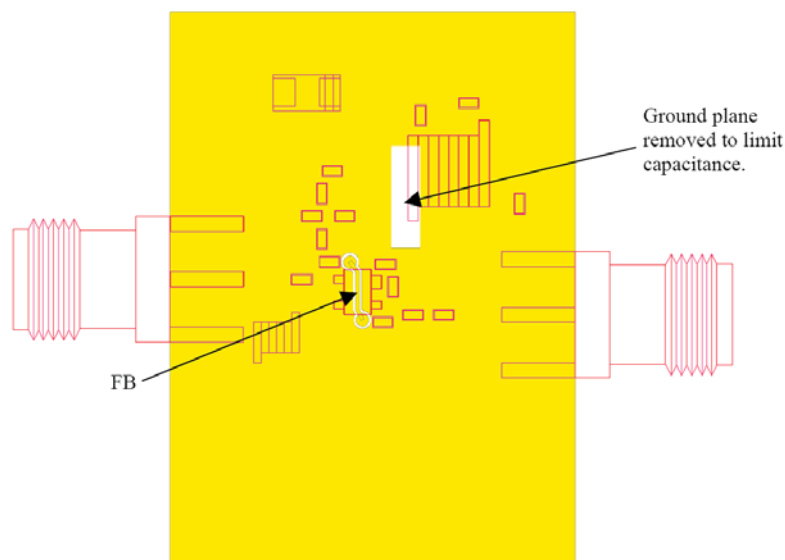
Figure 31. AvagoEnhGND.dsn – BottomMetal

For the EM analysis, the substrate is first defined using the Arlon 25N material properties and simulated from 10 MHz to 10 GHz. The "Substrate Layers" are defined as:

FreeSpace	Boundary: Open		Substrate Layer Name: FreeSpace	
	Permittivity: Loss Tangent	Real: 1	Loss Tangent: 0	
	Permeability: Loss Tangent	Real: 1	Loss Tangent: 0	
Arlon25N	Boundary: Interface		Substrate Layer Name: Arlon25N	
	Thickness: 30mil			
	Permittivity: Loss Tangent	Real: 3.38	Loss Tangent: 0.0023	
	Permeability: Loss Tangent	Real: 1	Loss Tangent: 0	
///GND///	Boundary: Closed		Plane: Bulk conductivity in Siemens/meter	
	Conductivity: 5.8E7			

The "Metalization Layers" are defined as follows:

FreeSpace
----Strip cond Layout Layer: Mapped to TopMetal, Sheet Conductor, Sigma 5.8E7S/m
Arlon25N Via Layer: Mapped to Plated Hole
///GND///

Once the substrate is computed, it is used for all PCB parasitic simulations. First, each node is analyzed with the EM simulator to ensure convergence. Once each component footprint parasitic is analyzed, a component is created from the Momentum Component menu, which allows the ADS EM/Circuit Co-Simulation capability. Each node is labeled in Figure 30 for reference.

Node 1 is labeled in Figure 30 and shown in Figure 32. This node connects the input matching inductor to the amplifier input. The amplifier is first simulated without the input matching network and then with the input matching network. For the first case, the inductor is not connected at the amplifier input. Thus, the inductor footprint pad is connected to the input microstrip line as shown in Figure 30. A "Single" port is used for this EM simulation as shown in Figure 32. The EM simulation creates a one-port s-parameter dataset named AvagoEnhNode1.
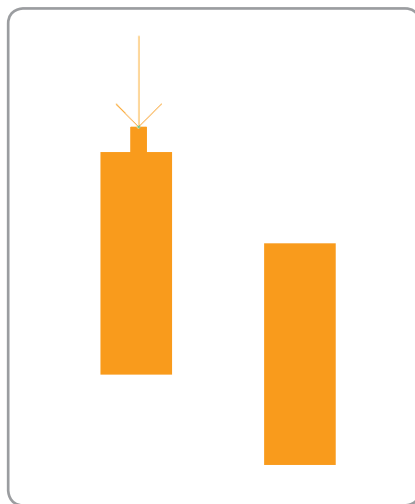
Figure 32. AvagoEnhNode1.dsn

Node 2 is labeled in Figure 30 and shown in Figure 33. This trace connects the
input matching capacitor to the transistor gate, the feedback resistor R4 to the transistor
gate, and the input parallel load resistor R1 to the transistor gate. Four "Internal"
ports are used for the EM simulation setup since each component is soldered to the
footprint pad. The ports are connected to each pad center as shown in Figure 33. An EM
simulation creates a four-port s-parameter dataset named AvagoEnhNode2 for this PCB
trace.
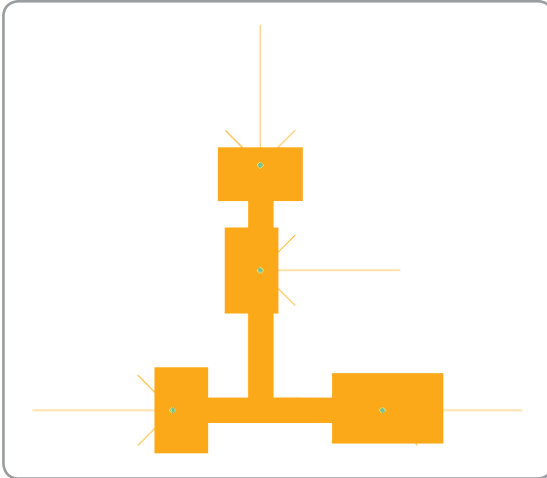
Figure 33. AvagoEnhNode2.dsn

Node 3 is labeled in Figure 30 and shown in Figure 34. This PCB trace connects
the transistor drain to the series and parallel output loads R3 and R2, the transistor
drain to the 27 nH bias choke coil, and the transistor drain to a feedback DC blocking
capacitor. (The DC feedback blocking capacitor is put in series with feedback resistor
R4 to block the DC bias. This DC blocking capacitor was not included in the schematics
up to this point.) The footprint pad of the 27 nH choke inductor is quite large and would
add parasitic capacitance in parallel with the inductor, which in turn, would lower the
self-resonant frequency of the bias tee. Figure 34b is the actual trace on the PCB layout.
Since there would be a substantial amount of parasitic capacitance on this pad, it was
decided that the ground plane would be removed from beneath this pad on the bottom
layer (BottomMetal) to limit parasitic capacitance. Figure 31 shows the absence of
ground plane under the inductor footprint pad. The EM simulator assumes infinite ground
plane in all directions when it is set up in the simple case. Note, that the BottomMetal
layer could be defined as a layer in the EM simulator, and then an open boundary layer
could be defined below that layer. A ground reference port could be used to reference
the BottomMetal layer to ground. This approach would likely be more accurate, but
would require much more simulation time. This approach also requires a new substrate
definition and simulation for the added layers. Thus, the Arlon25N substrate definition is
not usable for the approach where BottomMetal is used as the ground reference. Instead
of the more complicated, time consuming approach, the inductor pad was removed and
not included on the trace for the EM simulation as shown in Figure 34a. This approach
is less accurate, but will simulate much faster and should capture most of the parasitic
effects of the trace. When the pad is removed, the fringe capacitance around the edge
of that pad would not be included as well as the inductance associated with the pad.
Although the pad is not included, an EM simulation should yield a good estimate of the
parasitics added by this particular trace. Five "Internal" ports are connected to each pad
center with the exception of the inductor pad removed. In this case, an internal port is
added to the trace end as shown in Figure 34a. An EM simulation creates a five-port
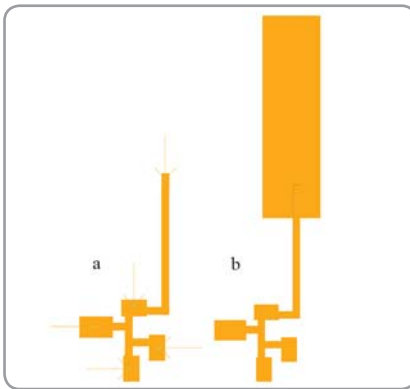s-parameter dataset named AvagoEnhNode3a for this PCB trace.

Figure 34. AvagoEnhNode3a.dsn EnhNode3b.dsn

Node 4 is labeled in Figure 30 and shown in Figure 35. This node connects the output parallel load resistor R2 to the parallel load DC blocking capacitor C3. Two "Internal" ports are connected to the pad centers as shown in the figure. An EM simulation of this trace creates a two-port s-parameter dataset called AvagoEnhNode4.
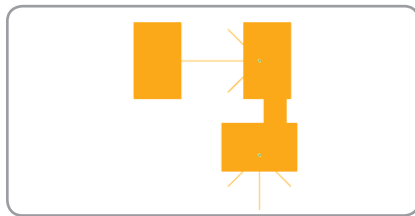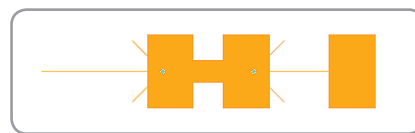

Figure 35. AvagoEnhNode4.dsn

Node 5 is labeled in Figure 30 and is shown in Figure 36. This trace connects the output series load resistor R3 to a series output DC blocking capacitor. The DC blocking capacitor is added to block the DC from the amplifier output. It has not been included in any simulations up to this point. Two "Internal" ports are connected to the pads as shown. An EM simulation of this trace creates a two-port s-parameter dataset called AvagoEnhNode5.

Figure 36. AvagoEnhNode5.dsn

Node 6 is denoted in Figure 30 and shown in Figure 37. This trace connects the input parallel load resistor R1 to the 0.5 pF bypass capacitor C1, and connects gate bias resistors to each other and to the input parallel load resistor R1 and 0.5 pF bypass capacitor C1. A four-port s-parameter dataset called AvagoEnhNode6 is created upon execution of an EM simulation of this PCB trace.
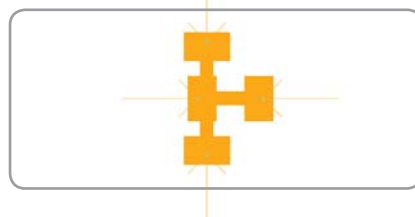
Figure 37. AvagoEnhNode6.dsn

The feedback trace is shown in Figure 31 on the PCB. This trace is on the BottomMetal layer underneath the TopMetal ground plane and connects the feedback resistor R4 to the feedback capacitor. Thus, for the EM simulation, an assumption is made that the trace is on the top of the PCB so that the existing Arlon25N substrate may be used for the EM simulation. In other words, the BottomMetal layer is mapped to the top of the substrate and the TopMetal layer is mapped to the GND plane. In reality, the runner is actually copied to the TopMetal layer and no mapping of the BottomMetal layer occurs. Thus, the runner in Figure 38 is on the substrate top layer and the bottom layer is a ground plane for the EM simulation. The vias cutting through the PCB on the actual layout are not included in the EM simulation since they would be shorted to ground. The footprint pads for the feedback resistor R4 and feedback DC blocking capacitor are also not included. This is an estimate that includes most of the parasitic effects of the feedback runner. A "Single" port is used on each end of the runner as shown in Figure 38. A twoport s-parameter dataset is created upon completion of the EM simulation.
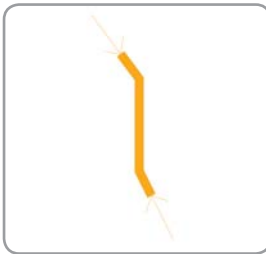
Figure 38. AvagoEnhFB.dsn

Finally, an estimate of parasitic ground inductance on the transistor source leads is simulated. The transistor has two source leads that are connected internally to each other. For the source terminal parasitic ground inductance estimate, an EM simulation is performed at the connection point of each transistor source lead on the PCB. Since the transistor s-parameter data uses a two-port representation that has only one ground reference, the inductance value estimates for the two lead connections are combined as parallel inductances to obtain one parasitic ground inductance value for the circuit simulations. According to the Avago 54143 data sheet, the s-parameters are measured in a fixture that has vias tying the source terminals to ground. This adds some uncertainty to the end result of actual amplifier performance versus model performance. An estimate of ground inductance on the PCB layout is accomplished with an EM simulation. The Arlon 25N substrate is set up with an infinite ground plane on the bottom layer. Using this approach is likely to under-estimate the parasitic inductance. An alternate approach changes the bottom layer of the substrate to a strip layer like the top layer and maps the BottomMetal layer to this new bottom strip layer. An open boundary layer is added below the bottom metal layer. A ground reference port is now added to the BottomMetal layer. Placement of this ground reference port on the BottomMetal layer is problematic. Where is the actual ground reference? No two points on the bottom ground layer are at the exact same RF voltage potential since there is inductance and loss in the ground plane. Thus, placement of the ground reference port will affect analysis results.Parasitic inductance is likely to be higher and more realistic with this approach, but the simulation time is longer. Since an estimate of parasitic ground inductance is the objective, the first method is used for simulation.

Figure 39 shows a portion of the layout where vias connect the top layer metal to the bottom layer metal. An "Internal" port is added to the TopMetal layer where the thin transistor source leg connects to the PCB. The Arlon25N substrate is used for the EM simulation. Edge meshing is not used and the analysis is performed only at 2.5 GHz. Upon completion of the EM simulation a one-port s-parameter dataset is created.
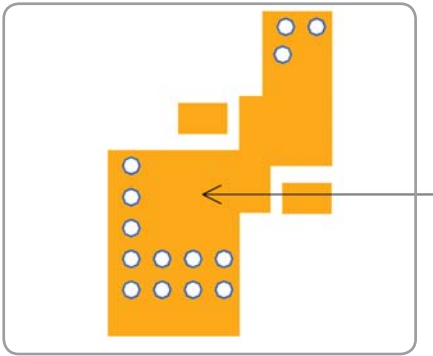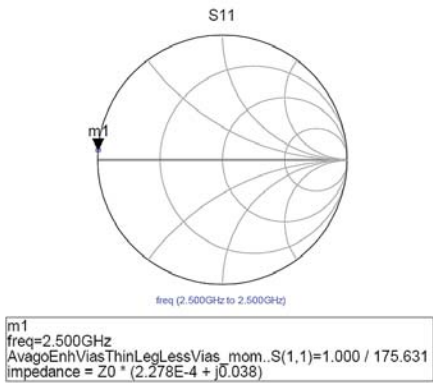
Figure 39. AvagoEnhViasThinLegLessVias.dsn

Figure 40. AvagoEnhViasThinLegLessVias.dds

Figure 40 shows the results of the first parasitic ground inductance simulation. The inductive reactance is j(50 × 0.038) = j1.9 as shown on the Smith chart marker readout. Solving for the inductance value:

Equation 26.
$$\frac{X_L}{2\,\pi\,f} = \frac{1.9}{2\,\pi\,(2.5\mathrm{x}10^9)} = 0.1214\ nH$$
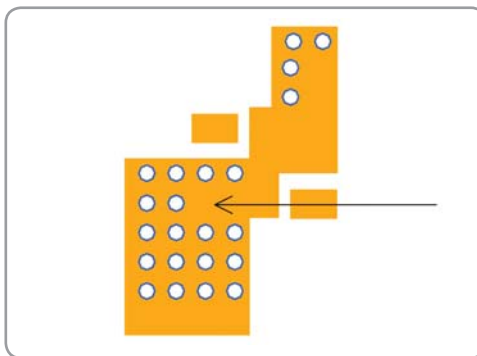
Figure 41. AvagoEnhViasThinLeg.dsn

Figure 41 has 4 additional vias added close to the transistor thin leg in an attempt to lower the parasitic ground inductance. The internal port is in the same location as in Figure 39. The 2.5 GHz EM simulation creates a one-port s-parameter dataset. Figure 42 plots the data on a Smith chart as shown. The marker readout yields the inductive reactance j(50 × 0.017) = j0.85, which is less than half of the parasitic inductive reactance from the first case. Solving for the inductance value:

$$\text{Equation 27.} \qquad \frac{X_L}{2\,\pi\,f} = \frac{0.85}{2\,\pi\,(2.5\text{x}10^9)} = 0.0541nH$$

The four extra vias are included in the layout since they lower the parasitic inductance value to less than half.

Figure 43 shows the setup for estimating parasitic ground inductance where the wide transistor source leg connects to the TopMetal layer. The internal port connects where the center of the transistor lead attaches. The EM simulation creates a one-port s-parameter dataset that is plotted in Figure 44. The marker readout lists inductive reactance j(50 × 0.0505) = j2.526 as shown in the figure. Solving for the inductance value:

$$\text{Equation 28.} \qquad \frac{X_L}{2\,\pi\,f} = \frac{2.526}{2\,\pi\,(2.5\text{x}10^9)} = 0.1608nH$$

S11

freq (2.500GHz to 2.500GHz)

```
m1
freq=2.500GHz
AvagoEnhViasThinLeg_mom..S(1,1)=1.000 / 178.039
impedance = Z0 * (1.504E-4 + j0.017)
```
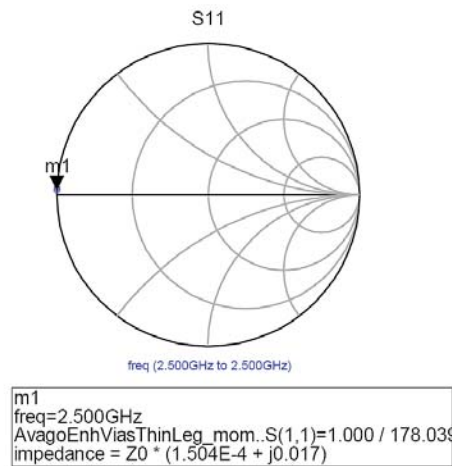
Figure 42. AvagoEnhViasThinLeg.dds

Figure 43. AvagoEnhViasWideLeg.dsn

S11

freq (2.500GHz to 2.500GHz)

m1
freq=2.500GHz
AvagoEnhViasWideLeg_mom..S(1,1)=0.999 / 174.213
impedance = Z0 * (3.199E-4 + j0.051)

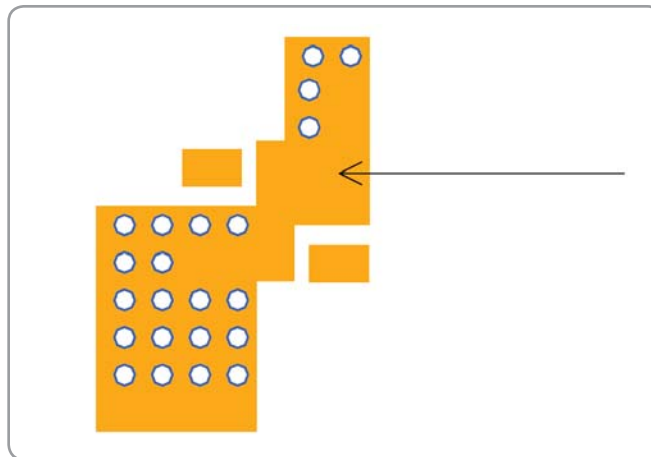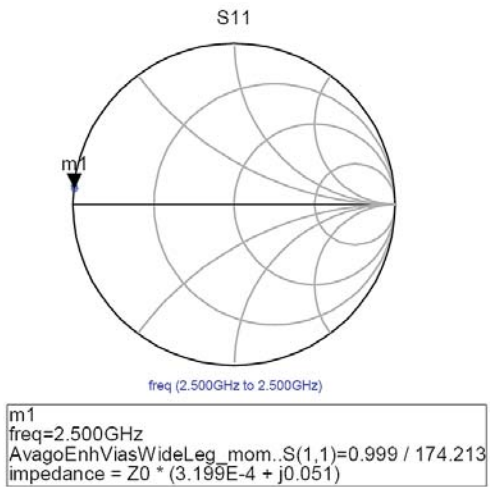*Figure 44. AvagoEnhViasWideLeg.dds*

The two calculated inductance values of 0.05447 nH and 0.1608 nH are now put in parallel to obtain an estimate of parasitic inductance. Note that putting the inductance values in parallel with each other is a very crude approach, but will likely give a decent ballpark estimate of parasitic ground inductance. Putting the inductances in parallel yields an estimated parasitic ground inductance of 0.045 nH. An alternate approach to putting the inductance values in parallel would be to use the nonlinear model for the simulation since it includes both source leads. Then, the narrow transistor leg calculated parasitic ground inductance is connected to the narrow source leg and the wide leg calculated parasitic ground inductance is connected to the wide source leg and used for simulation. Note also that the Avago measured s-parameter data was measured in a fixture with vias that add parasitic ground inductance.

Figure 45 combines the PCB layout node of each PCB layout trace with the circuit component models to EM/Circuit Co-Simulate the entire circuit with layout parasitics. Each PCB trace was first simulated with the EM simulator to produce a multiport s-parameter dataset.
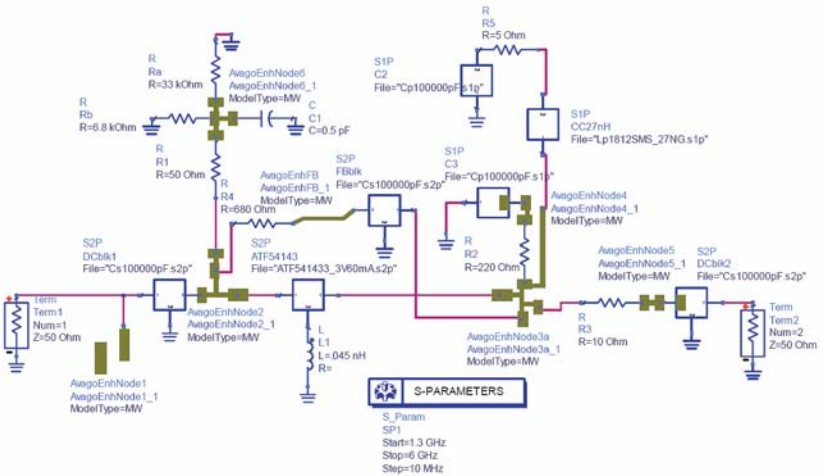

Figure 45. ATF54143ampEM.dsn

Figure 45 contains the estimated parasitic ground inductance represented by the
L1 inductor. Measured data for the 0.1 uF capacitor is included for the DC blocking
capacitors and DC bypassing capacitors as well.

Figure 46 plots the Figure 45 s-parameter simulation data. Note that the input
matching network is not yet included in the Figure 45 schematic. It is useful to analyze
amplifier stability results without matching networks since matching networks can
decouple the gain block from the measurement system at some frequencies. The
50 Ω gain is 14.2 dB according to Figure 46. Notice the resonance at 3.3 GHz caused by
the output choke coil. This resonance is seen in the S11, S22, S21, and S12 plots. The
output reflection coefficient is low at low frequencies below the primary resonance. It
is therefore, unlikely that the amplifier requires an output matching network. The input
reflection coefficient below the primary resonance indicates that a matching network will
improve amplifier input return loss. Input matching also impacts amplifier noise figure as
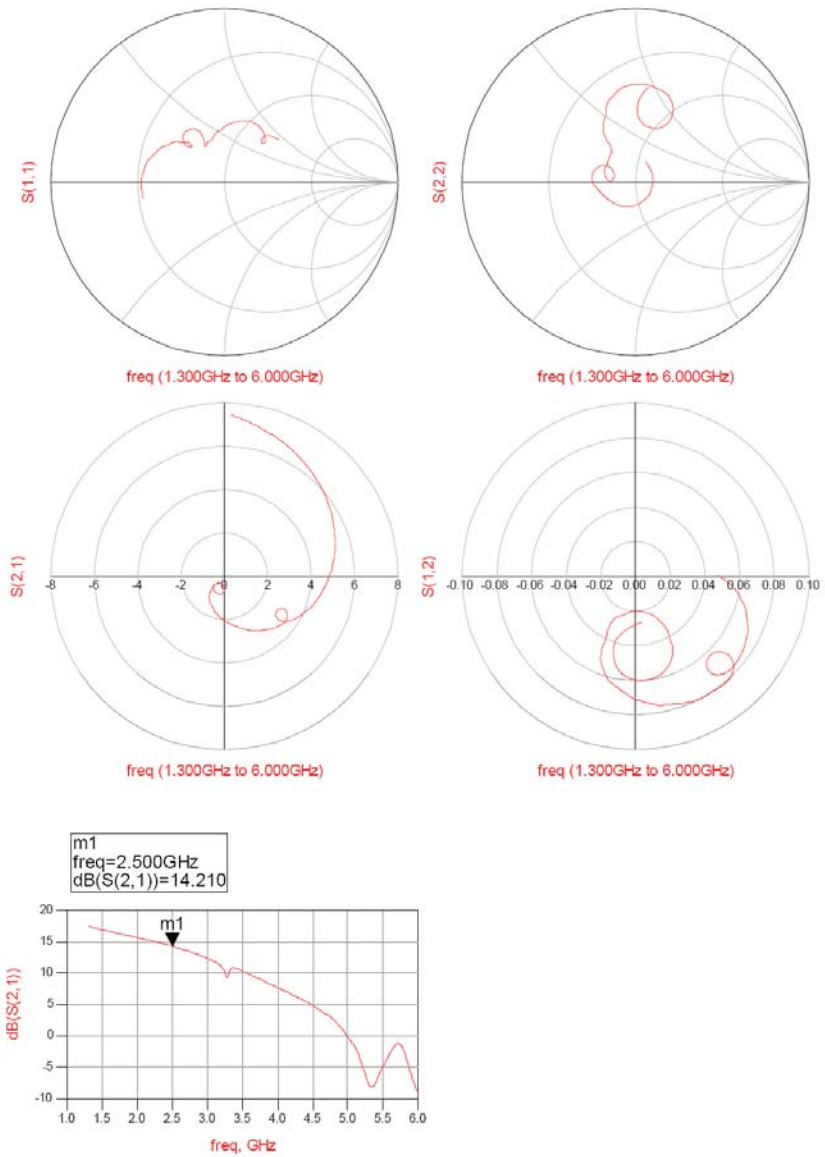indicated by Equation 27.

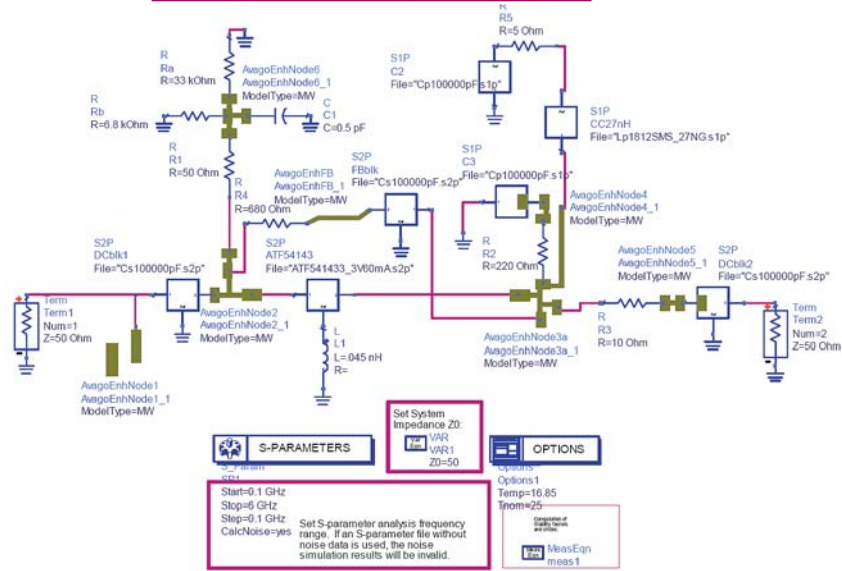*Figure 46. ATF54143ampEM.dds*

Figure 47. ATF54143_StabilityAnalysis5.dsn

A stability analysis of the amplifier circuit, which includes PCB layout and component parasitics is shown in Figure 47. This ADS Amplifier Design Guide not only calculates stability factors K, μ_{Source}, and μ_{Load}, but also allows an available gain design with available gain circles and noise circles. The stability analysis is limited from 100 MHz to 6 GHz since the choke inductor measured data is limited to 6 GHz. Figure 48 shows K, μ_{Source}, and μ_{Load} plotted in the red box. Note that $\mu_{Source} \geq 1$ and $\mu_{Load} \geq 1$ for all frequencies from 100 MHz to 6 GHz, either of which, guarantee unconditional stability over that frequency range.

Available gain circles are plotted with noise circles in Figure 49. Figure 50 gives specific readouts for Figure 49. The minimum noise figure, NF_{min}, is 1.23 dB according to Figure 48. The first noise circle is 0.2 dB higher than NF_{min}, or 1.4 dB. The 1.4 dB noise circle passes right through Γ_{MS}, the simultaneous conjugate input match. Thus, the marker is moved to the 1.4 dB noise figure circle at Γ_{MS}.
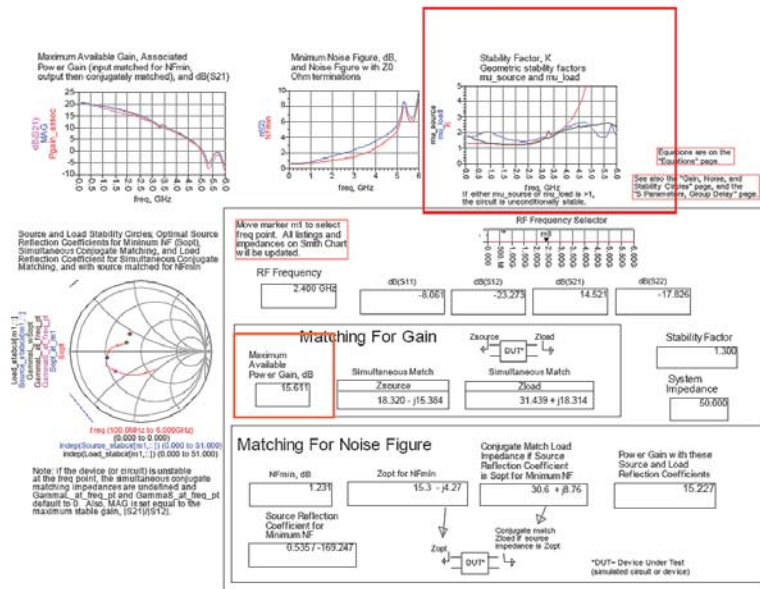
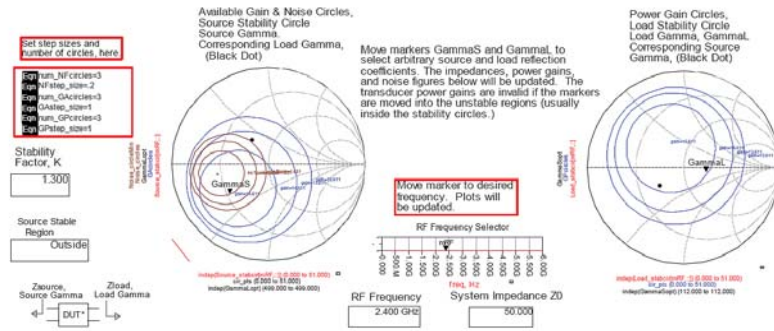*Figure 48. ATF54143_StabilityAnalysis5 (Page 1)*

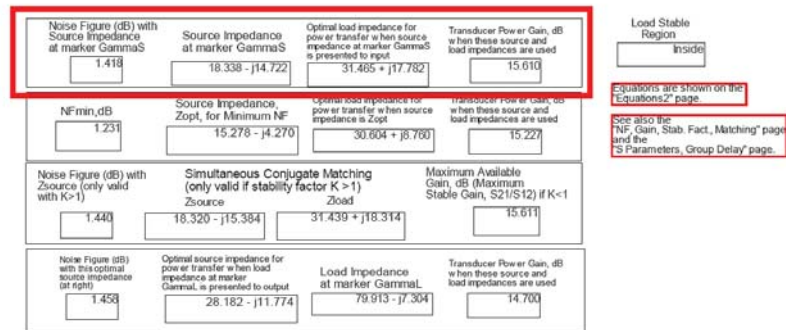*Figure 49. ATF54143_StabilityAnalysis5 (Page 3)*

Figure 50. ATF54143_StabilityAnalysis5 (Page 3)

The marker readout in the red box of Figure 50 shows the impedance that must be presented to the amplifier input to achieve 1.42 dB noise figure and 15.6 dB of gain. The impedance of 18.338-j14.722 is what the amplifier input "wants to see" to obtain these results. It is also assumed that the output will be conjugately matched when the amplifier input is terminated with this impedance. In reality, the amplifier output doesn't require much output matching since it's output reflection coefficient is already pretty low. Thus, the last step of the available gain design procedure, which is to conjugately match the output for the given source termination, will not be executed. The expected gain of 15.6 dB will not be reached, but will be reduced by a very small amount.

The input match must transform 50 Ω to 18.338-j14.722 at 2.5 GHz. An ADS Matching Design Guide is used to develop the matching network. The Design Guide assumes that one impedance is being matched to another impedance, whereas, the Figure 50 marker readout is what the amplifier input "wants to see". Figure 51 demonstrates how the reference is changed from what the amplifier "wants to see" at its input to how the ADS Matching Network Design Guide is configured.
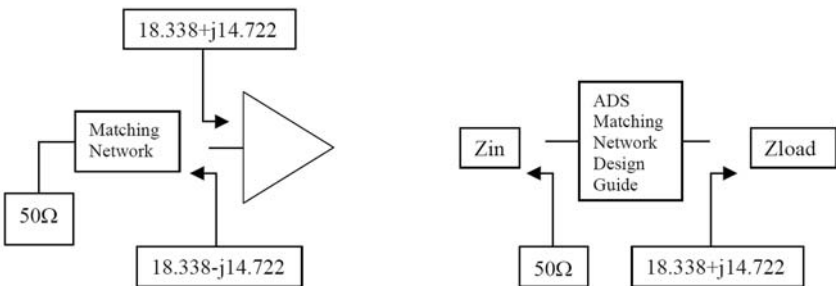

Figure 51. Matching References

DA_LEMatch1_untitled1
DA_LEMatch1
F=2.5 GHz
Zin=50 Ohm
Zload=18.338+j*14.722 Ohm
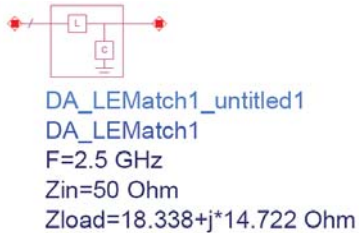
Lumped Element Match Design Assistant
Need Help? Please see the appropriate DesignGuide User Manual

VAR
VAR1
Parameters="#2.5 GHz#50 Ohm#18.338+j*14.722 Ohm#0"

Port
P1
Num=1

L
L1
L=2.42 nH
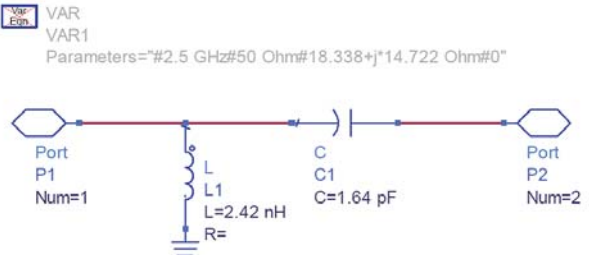R=

C
C1
C=1.64 pF

Port
P2
Num=2

Figure 52. InMatch_Synthesis.dsn

The input matching network is designed using the ADS Matching Network Design Guide as shown in Figure 52 and demonstrated in Figure 51. An L-match is designed consisting of a parallel 2.42 nH inductor next to the 50 Ω source and a series 1.64 pF capacitor connected to the amplifier input as displayed in Figure 52.

Figure 53 adds the ideal input matching network to the Figure 47 amplifier, which contains PCB and lumped component parasitics. Note that the 2.4 nH parallel inductor is connected in parallel with the 50 Ω source and the 1.6 pF series capacitor then connects to the amplifier input. The inductor is not connected to the inductor pad from the Node1 EM simulation since the first Node1 EM simulation is a one-port s-parameter dataset.
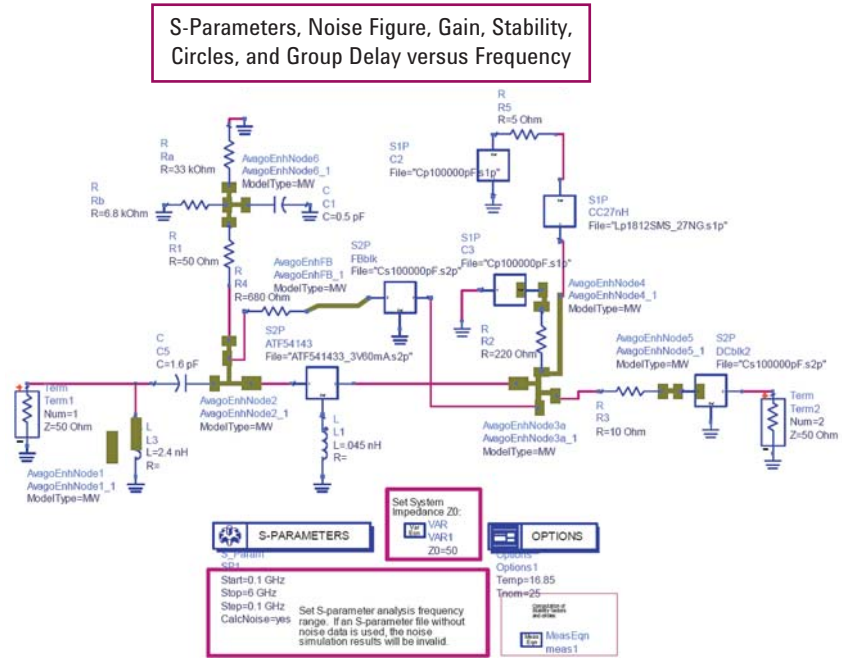

Figure 53. ATF54143_InMatch.dsn

The Figure 53 s-parameters are plotted in Figure 54. The Smith charts indicate both the input and output are well matched at 2.5 GHz. The numeric gain on the S21 polar chart at 2.5 GHz is 5.53, which converts to 14.85 dB.
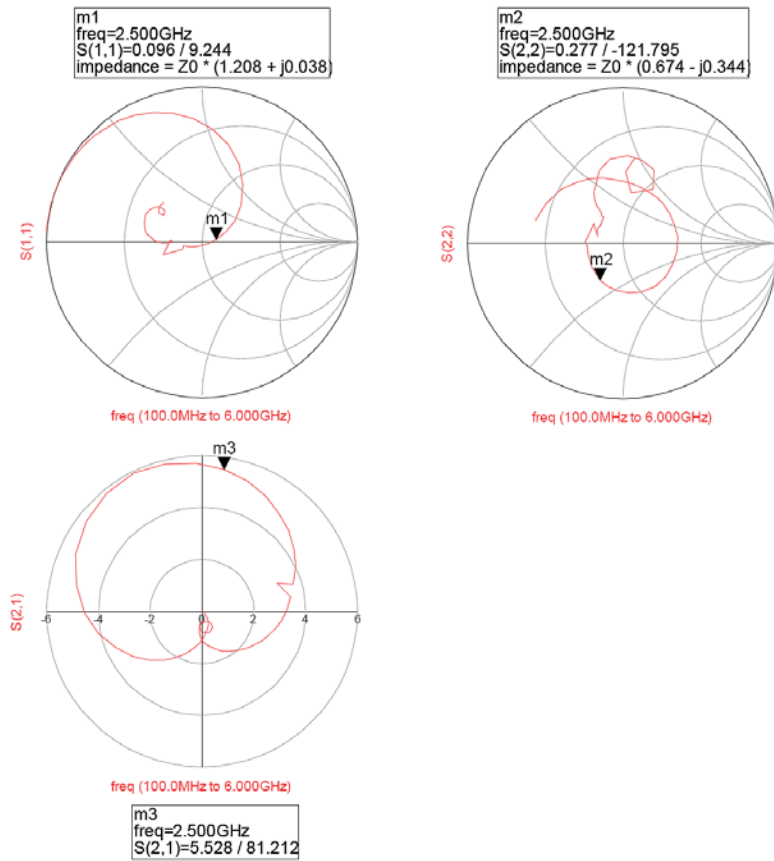
m1
freq=2.500GHz
S(1,1)=0.096 / 9.244
impedance = Z0 * (1.208 + j0.038)

m2
freq=2.500GHz
S(2,2)=0.277 / -121.795
impedance = Z0 * (0.674 - j0.344)

freq (100.0MHz to 6.000GHz)

freq (100.0MHz to 6.000GHz)

freq (100.0MHz to 6.000GHz)

m3
freq=2.500GHz
S(2,1)=5.528 / 81.212

Figure 54. ATF54143_InMatch.dds

A gain of 15.15 dB at 2.4 GHz is plotted on the rectangular plot of Figure 55. A 20 dB input return loss and 10 dB output return loss are also plotted. The predicted noise figure with the input match is 1.56 dB at 2.5 GHz.

A 2.4 nH Coilcraft airwound inductor is available for the input matching network. A lumped equivalent model supplied by Coilcraft is shown in Figure 56. The subcircuit model is created for use in the amplifier circuit.

43

m4
freq=2.500GHz
dB(S(1,1))=-20.375

m5
freq=2.400GHz
dB(S(2,1))=15.145
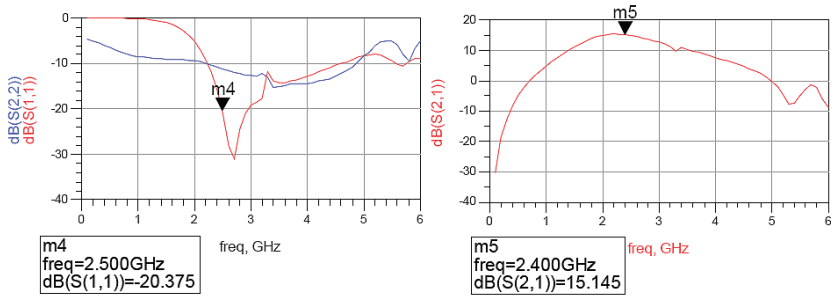
freq	nf(2)
100.0 MHz	46.633
200.0 MHz	34.725
300.0 MHz	27.837
400.0 MHz	23.017
500.0 MHz	19.338
600.0 MHz	16.396
700.0 MHz	13.968
800.0 MHz	11.931
900.0 MHz	10.002
1.000 GHz	8.925
1.100 GHz	7.709
1.200 GHz	6.655
1.300 GHz	5.739
1.400 GHz	4.944
1.500 GHz	4.257
1.600 GHz	3.669
1.700 GHz	3.169
1.800 GHz	2.752
1.900 GHz	2.410
2.000 GHz	2.151
2.100 GHz	1.937
2.200 GHz	1.776
2.300 GHz	1.666
2.400 GHz	1.599
2.500 GHz	1.562
2.600 GHz	1.562
2.700 GHz	1.593
2.800 GHz	1.650
2.900 GHz	1.730
3.000 GHz	1.829

Figure 55. ATF54143_InMatch.dds
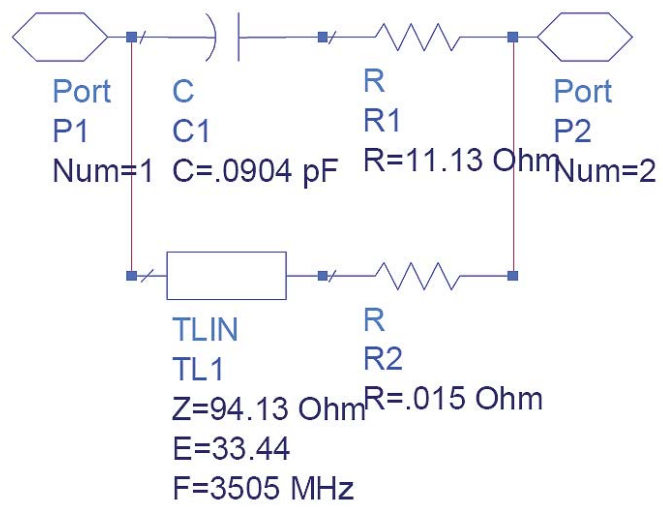
Port
P1
Num=1

C
C1
C=.0904 pF

R
R1
R=11.13 Ohm

Port
P2
Num=2

TLIN
TL1
Z=94.13 Ohm
E=33.44
F=3505 MHz

R
R2
R=.015 Ohm

Figure 56. CCA01T.dsn

44
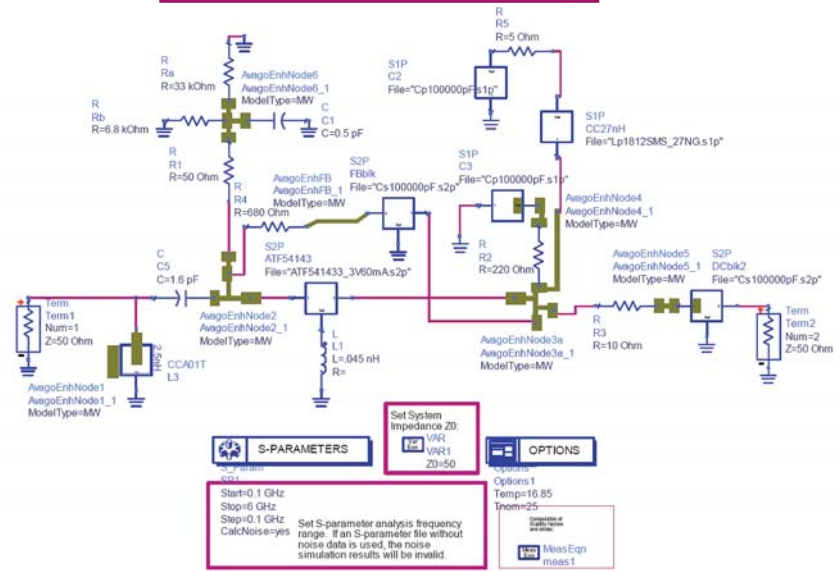
Figure 57. ATF54143_InMatch2.dsn

The lumped equivalent 2.4 nH Coilcraft inductor L3 replaces the ideal inductor in Figure 53 to give the Figure 57 circuit. Figure 58 plots the simulation results of Figure 57. S11 and S22 Smith chart plots indicate that both input and output are very well matched. The input return loss with the inductor model plotted in Figure 59 shows a slight degradation from 20 dB to 17.6 dB. The 15.14 dB gain is unaffected by the slight input loss degradation. The 2.4 nH coil loss slightly degrades noise figure to 1.62 dB.

Figure 58. ATF54143_InMatch2.dds

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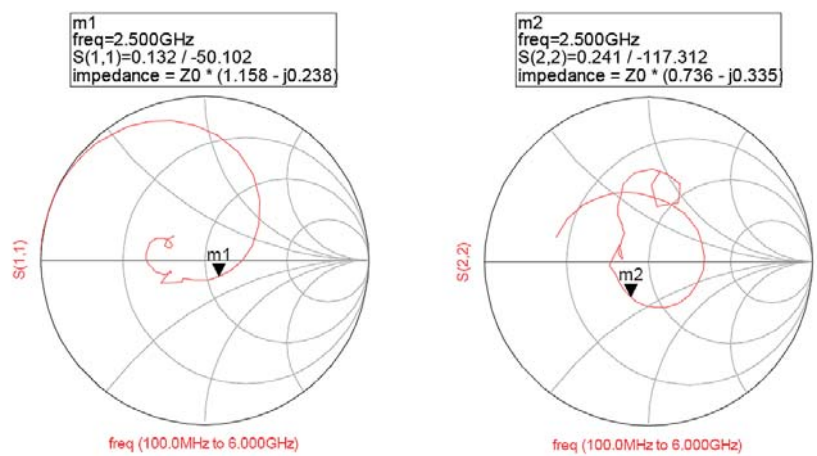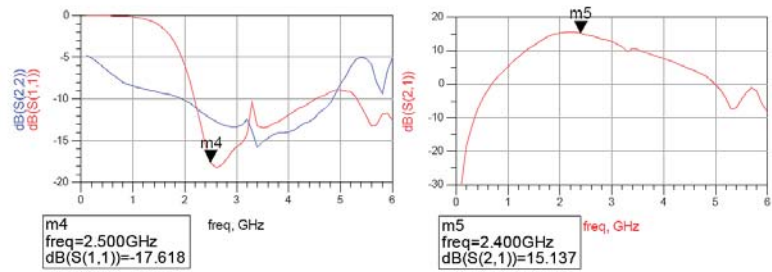| freq	nf(2)
100.0 MHz	46.297
200.0 MHz	34.385
300.0 MHz	27.488
400.0 MHz	22.656
500.0 MHz	18.964
600.0 MHz	16.007
700.0 MHz	13.565
800.0 MHz	11.513
900.0 MHz	9.574
1.000 GHz	8.483
1.100 GHz	7.261
1.200 GHz	6.206
1.300 GHz	5.296
1.400 GHz	4.514
1.500 GHz	3.848
1.600 GHz	3.288
1.700 GHz	2.825
1.800 GHz	2.451
1.900 GHz	2.157
2.000 GHz	1.950
2.100 GHz	1.788
2.200 GHz	1.681
2.300 GHz	1.622
2.400 GHz	1.605
2.500 GHz	1.616
2.600 GHz	1.658
2.700 GHz	1.726
2.800 GHz	1.816
2.900 GHz	1.924
3.000 GHz	2.046

Figure 59. ATF54143_InMatch2.dds
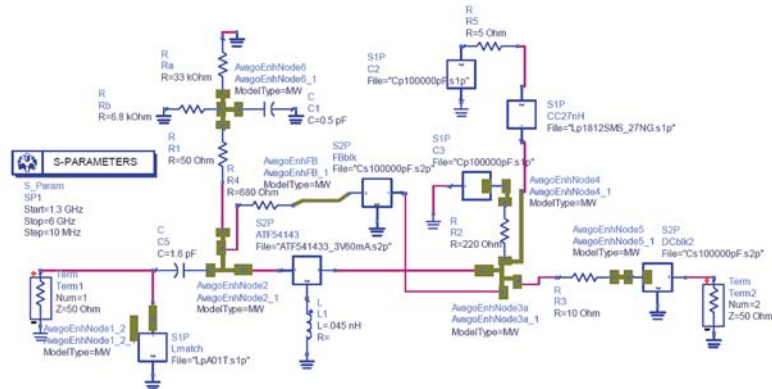
Figure 60. ATF54143ampEM2.dsn

The Node1 one-port s-parameter EM simulated dataset is replaced by the two-port s-parameter data so that the lumped equivalent circuit model is connected correctly to the PCB trace pad. Previously, the AvagoEnhNode1 was treated as a one-port network and the 2.4 nH matching inductor was placed in parallel with that trace representation. Further, and more importantly, the 2.4 nH Coil Craft lumped equivalent model is replaced by one-port measured data in Figure 60. The 2.4 nH matching inductor attaches to the pad center, thus the updated Node1 trace is used in Figure 60. Figure 61 plots the updated simulation results. The measured data for the 2.4 nH input matching inductor indicates that the lumped equivalent model under-estimates loss of the actual inductor. Gain degrades from 15.137 dB to 14.65 dB and noise figure degrades from 1.6 dB to 1.78 dB at 2.5 GHz as shown by Figures 59 and 61.

m2
freq=2.450GHz
S(1,1)=0.238 / -70.633
impedance = Z0 * (1.050 - j0.500)

m3
freq=2.450GHz
S(2,2)=0.214 / -103.262
impedance = Z0 * (0.834 - j0.364)

S(1,1)

freq (1.300GHz to 6.000GHz)

S(2,2)

freq (1.300GHz to 6.000GHz)

S(2,1)

-8 -6 -4 -2 0 2 4 6 8

freq (1.300GHz to 6.000GHz)

S(1,2)

-0.10 -0.08 -0.06 -0.04 -0.02 0.00 0.02 0.04 0.06 0.08 0.10

freq (1.300GHz to 6.000GHz)

m1
freq=2.500GHz
dB(S(2,1))=14.646

dB(S(2,1))

freq, GHz

dB(S(2,2))
dB(S(1,1))

freq, GHz

m4
freq=2.500GHz
dB(S(1,1))=-12.725

m5
freq=2.500GHz
dB(S(2,2))=-13.560

freq	nf(2)
2.370 GHz	1.725
2.380 GHz	1.729
2.390 GHz	1.730
2.400 GHz	1.731
2.410 GHz	1.736
2.420 GHz	1.738
2.430 GHz	1.743
2.440 GHz	1.748
2.450 GHz	1.753
2.460 GHz	1.758
2.470 GHz	1.763
2.480 GHz	1.768
2.490 GHz	1.774
2.500 GHz	1.779
2.510 GHz	1.785
2.520 GHz	1.792
2.530 GHz	1.799
2.540 GHz	1.806
2.550 GHz	1.815
2.560 GHz	1.821
2.570 GHz	1.831
2.580 GHz	1.840
2.590 GHz	1.846
2.600 GHz	1.853
2.610 GHz	1.864
2.620 GHz	1.867
2.630 GHz	1.875

Figure 61. ATF54143ampEM2.dsn

Amplifier Nonlinear Analysis
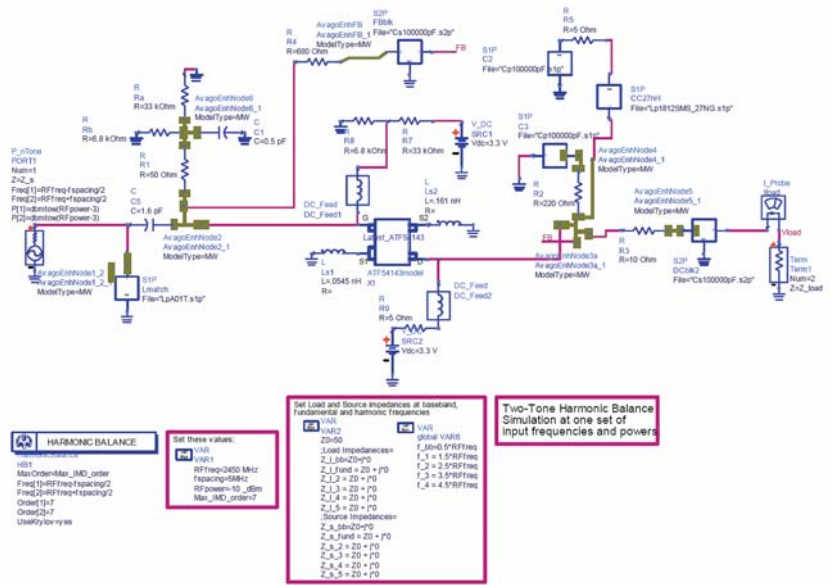
Figure 62. ATF54143_Amp_HBT2Tone.dsn
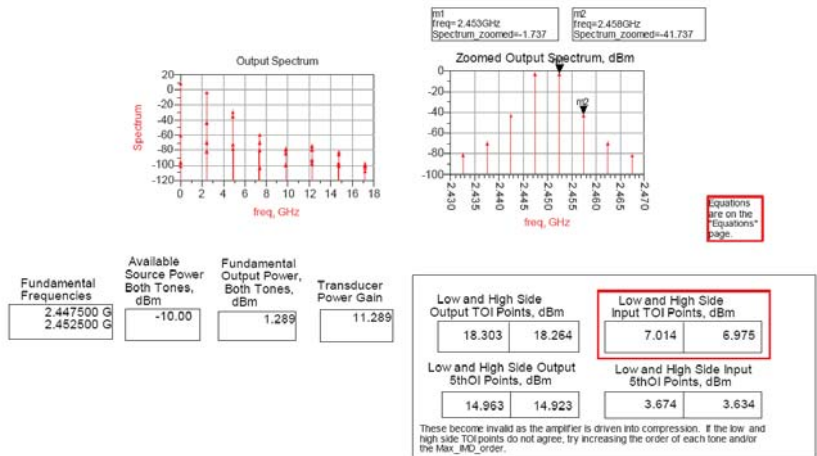
Figure 63. ATF541413_Amp_HBT2Tone.dds

A third order intermodulation distortion simulation is configured using the ADS Amplifier Design Guide (from a schematic, select DesignGuide > Amplifier > 2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5th OI Points) in Figure 62. The Figure 60 ATF54143 two-port s-parameter data is replaced in the parasitic model by the biased non-linear model from Figure 5. The red box in Figure 63 displays a third order input intercept point of 7 dBm.

Simulation Results Versus Specification Requirements

The simulated amplifier that includes PCB layout and component parasitics meets all amplifier design requirements as follows:

	Specification requirement	Simulated value
Frequency range	2.4 GHz to 2.48 GHz	2.4 GHz to 2.48 GHz
Gain	> 12 dB	14.65 dB
Noise figure	< 2.5 dB	1.78 dB
IP3i	> 0 dBm	7 dBm
Input return loss	> 10 dB	12.7 dB
Output return loss	> 10 dB	13.6 dB
Current drain	< 100 mA	61.38 mA
Supply voltage	3.3 V	3.3 V
Stability	Unconditional	Unconditional

Table 3.

TRL Calibration Kit

Since the simulated amplifier with all PCB layout and component parasitics meet or exceed the specification requirements, the PCB layout of Figures 30 and 31 is fabricated. Additionally, it is convenient to design and construct a TRL calibration kit so that precise measurements are possible without the need of de-embedding procedures. Linecalc is again used to design the TRL calibration standards. Required standards include an Open, Load, Thru, and at least one Line. Since the amplifier input and output 50 Ω transmission lines are 250 mils long in Figure 30, the Open standard is also 250 mils long. The Thru is made twice as long so that a zero length Thru is constructed. Thus, the zero length Thru is 500 mils long. The Load standard is used for the isolation calibration and also has a length of 250 mils. Next a Line standard is constructed. The Intercontinental Microwave transistor calibration data is valid to 6 GHz, thus the TRL calibration Line 1 standard is designed to cover up to 6 GHz. The electrical length of the line standard is valid from 30° to 150°. Thus, the Line 1 standard should be no longer electrically than 150° at 6 GHz. Using Linecalc, the physical line length is 500 mils. Thus, the Line 1 standard is the 500 mil electrical length of the zero length Thru standard plus the additional Line 1 length of 500 mils, yielding a total Line 1 length of 1000mils. The lowest frequency for the Line 1 standard that yields an electrical length of 30° is just above 1.2 GHz, therefore 1.3 GHz is used as the Line 1 standard lower frequency limit. Therefore, the Line 1 standard, which is physically 500 mils long, covers a frequency range of 1.3 GHz to 6 GHz. The electrical delay of the Line 1 standard is given by:

Equation 29.

$$\tau = \frac{1\sqrt{\epsilon_r}}{c} = \frac{.0127m\sqrt{2.66}}{2.997925E8 \, m/sec} = 69.1pSec$$

The TRL zero length Thru standard measures 500 mils long and is shown in Figure 64. The TRL Open standard is 250 mils long and is shown in Figure 65. The TRL Load standard used for the isolation calibration is 250 mils long and shown in Figure 66. The TRL Line 1 standard measures 1000 mils long and is shown in Figure 67.
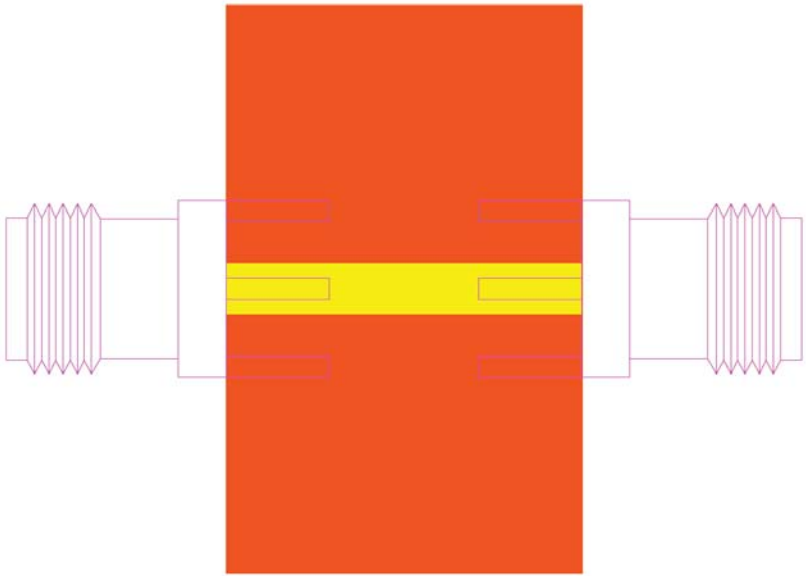
Figure 64. Thru25N.dsn
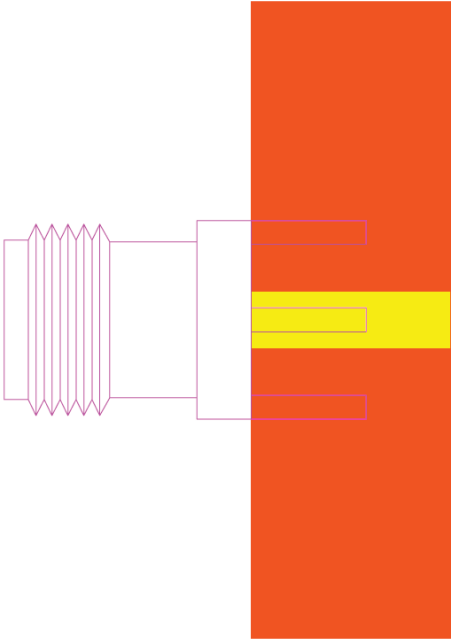
Figure 65. Open25N.dsn
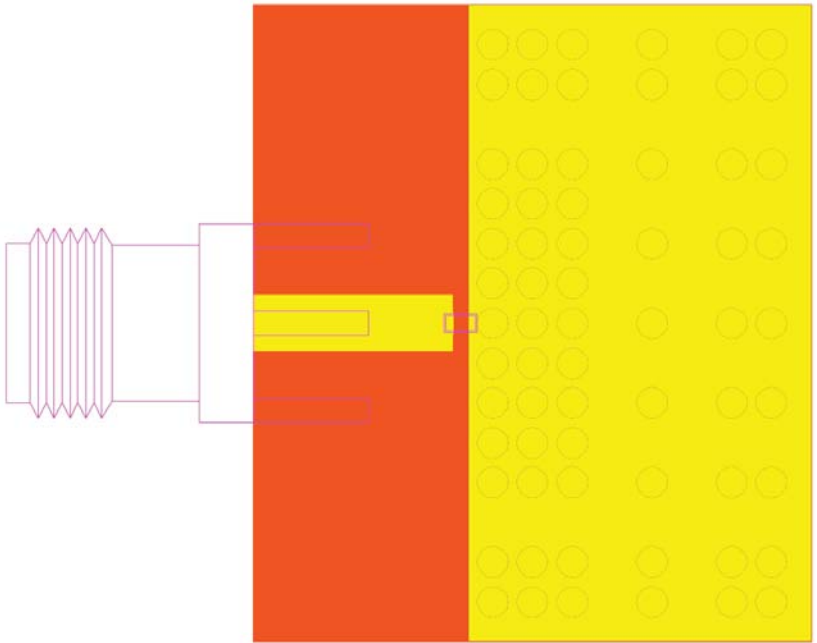
Figure 66. Load25N.dsn
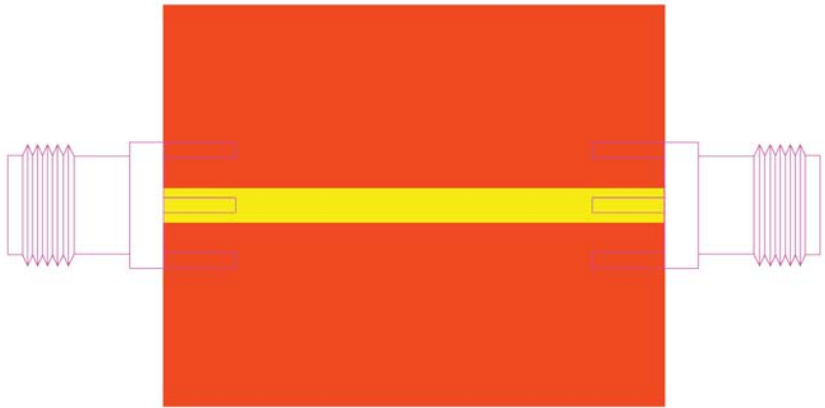
Figure 67. Line1_25N.dsn

The Standard Class Assignments for the Arlon 25N TRL calibration kit are shown in Table 4. The Arlon 25N Standard Definitions are shown in Table 5. Other Line standards listed in Tables 4 and 5 are available in the Arlon 25N TRL calibration kit, which are developed in a similar fashion to the Line 1 Calibration Standard.

Standard Class Assignments   Calibration Kit _____Arlon25N

| CLASS	A	B	C	D	E	F	G	Standard Class Label
$S_{11}A$	1							Open
$S_{11}B$								
$S_{11}C$	3							Load
$S_{22}A$	1							Open
$S_{22}B$								
$S_{22}C$	3							Load
Forward Transmission	2							Thru
Reverse Transmission	2							Thru
Forward Match	2							Thru
Reverse Match	2							Thru
Response								
Response & Isolation	3							Isoln Std
TRL Thru	2							Thru
TRL Reflect	1							Open
TRL Line	4	5	6	7	8	9		Lines
Adapter								
TRL Option								
Cal Z_0: _____ System Z_0 _____ Line Z_0								
Set Ref: __x__ Thru _____ Reflect								

Table 4.

Calibration Kit: Arlon25N

STANDARD		$C0$ $10^{-15}F$	$C1$ $10^{-27}F/Hz$	$C2$ $10^{-36}F/Hz2$	$C3$ $10^{-45}F/Hz3$	Fixed or Sliding	Terminal Impedance Ω	Offset			Frequency (GHz)		Coax or Waveguide	Standard Label
#	TYPE	$L0$ $10^{-12}H$	$L1$ $10^{-24}H/Hz$	$L2$ $10^{-33}H/Hz2$	$L3$ $10^{-42}H/Hz3$			Delay pSec	$Z0$ Ω	Loss GΩ/s	MIN	MAX		
1	Open	0	0	0	0		50	0	154.8		0.2	20		Open
2	Thru						50	0	50		0.2	20		Thru
3	Load					Fixed	50	0	120.9		0.2	20		Load
4	Line 1						50	69.1	50		1.3	6		1.3-6 Line
5	Line 2						50	207.31	50		0.4	2		0.4-2 Line
6	Line 3						50	19.348	50		4.5	20		4.5-20 Line
7	Line 4						50	20.177	50		4.2	20		4.2-20 Line
8	Line 5						50	96.74	50		0.87	4.3		0.87-4.3 Line
9	Line 6						50	428.42	50		0.2	0.97		0.2-0.97 Line
10														

Table 5.

Fabricated Amplifier and TRL Calibration Standards

Figure 68 shows the amplifier and TRL calibration standards fabricated on Arlon 25N 30 mil thick PCB laminate.
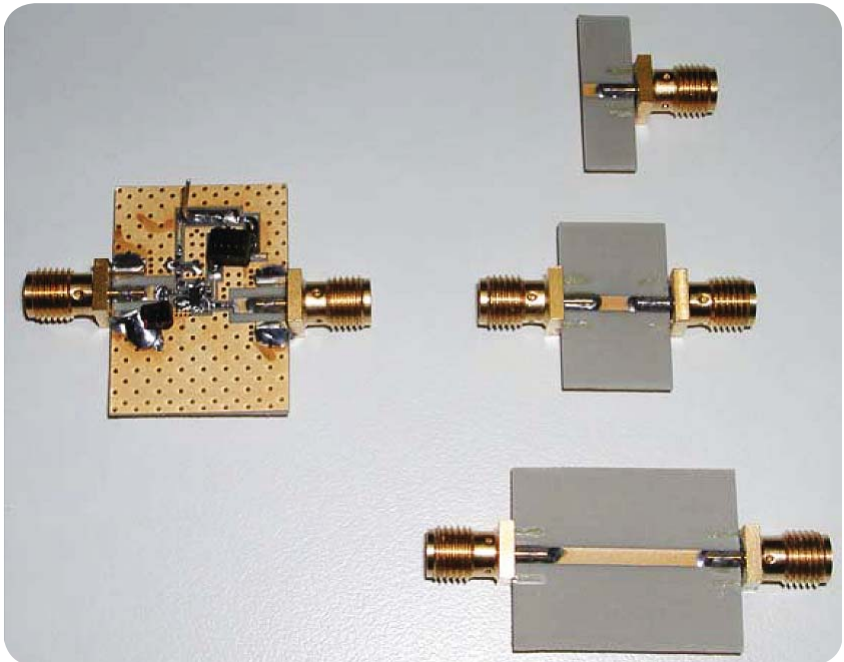

Figure 68. Fabricated amplifier and TRL calibration kit

Amplifier Linear S-Parameter Measurements Using TRL

The Table 4 and Table 5 calibration coefficients are entered into the network analyzer. The network analyzer is now calibrated using the Arlon 25N TRL calibration kit using the Line 1 standard. This allows a calibration over the frequency range from 1.3 GHz to 6 GHz. The amplifier input matching network is not yet placed on the PCB. (The input matching network is shown in Figure 68.) A DC blocking capacitor C5 is used at the input instead of the 1.6 pF matching capacitor in order to measure the amplifier s-parameters without the input matching network. The measured s-parameter data is saved to a data file and pulled into the simulator using Figure 69. Measured amplifier s-parameter data is plotted in Figure 70. Unmatched gain at 2.5 GHz is shown at 13.26 dB.
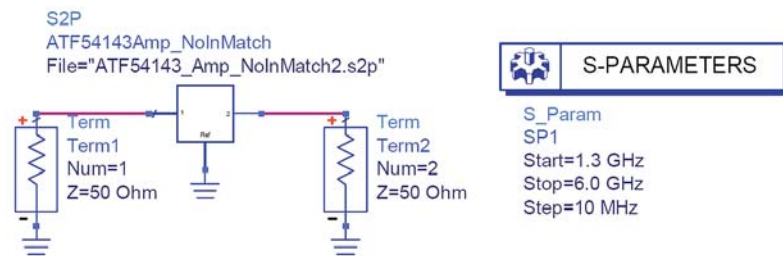
Figure 69. ATF54143Amp_NoInputMatch.dsn

S(1,1)

freq (1.300GHz to 6.000GHz)

S(2,2)

freq (1.300GHz to 6.000GHz)

S(2,1)

freq (1.300GHz to 6.000GHz)

S(1,2)

freq (1.300GHz to 6.000GHz)

m1
freq=2.500GHz
dB(S(2,1))=13.263

m1

dB(S(2,1))

freq, GHz
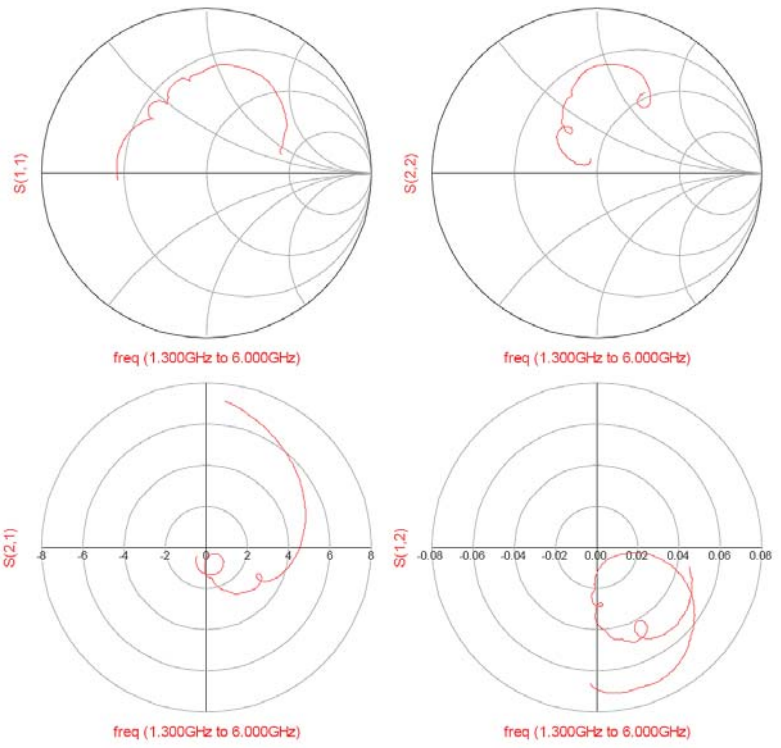
Figure 70. ATF54143Amp_NoInputMatch.dds

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Figure 71 allows a stability analysis on the measured s-parameter data from 1.3 GHz to 6 GHz. Stability analysis results are plotted in Figure 72. The red box highlights μ_{Source} and μ_{Load} plots. Note that $\mu_{Source} \geq 1$ and $\mu_{Load} \geq 1$ for all frequencies from 1.3 GHz to 6 GHz, either of which, guarantee unconditional stability over that frequency range. Thus, the measured s-parameters indicate unconditional stability.

Figure 71. ATF54143_StabilityAnalysis6.dsn

Figure 72. ATF54143_StabilityAnalysis6.dds

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Measured Versus Modeled

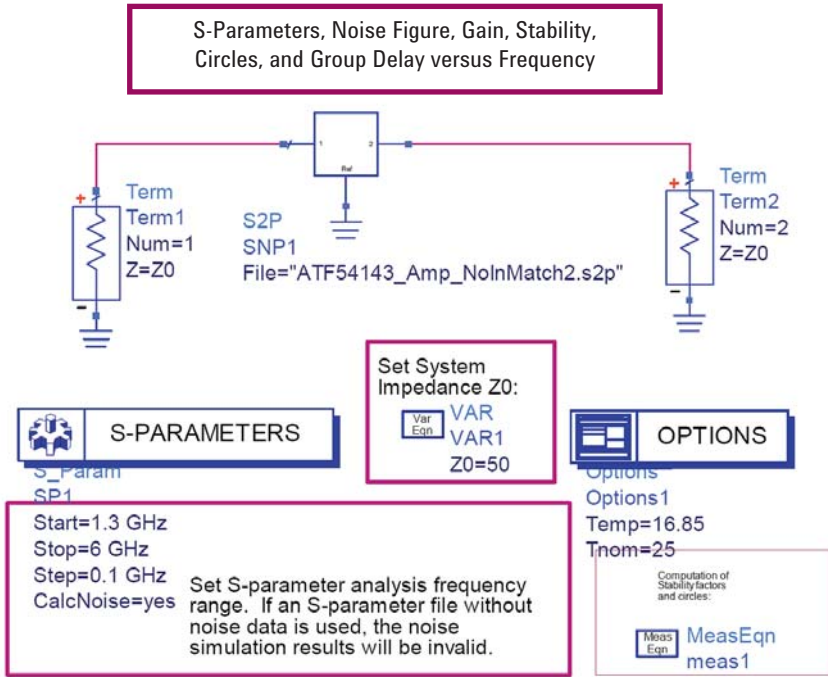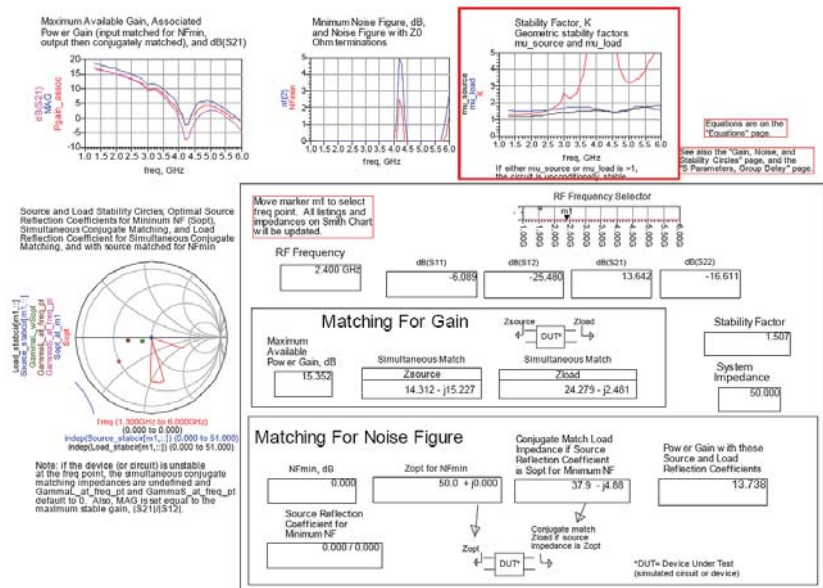Figure 73 compares the simulated amplifier using red traces with the measured amplifier using blue traces. Good agreement is shown between the two results. Measured gain at 2.5 GHz is 13.26 dB whereas the model predicts 14.2 dB. Gain is very sensitive to source terminal ground inductance shown by previous analysis. Source terminal inductance is analyzed with EM simulation for both transistor source terminals. Then, these two inductances are combined in parallel to use in the circuit simulation. Some method of combining the two inductances is necessary since an s-parameter linear component in ADS has only one ground reference terminal. The input reflection coefficient at 2.5 GHz is slightly higher for the measured amplifier versus the simulated amplifier. This accounts for a portion of the measured amplifier lower gain versus the simulated amplifier in the unmatched case. The method of combining parasitic transistor source terminal inductance and the higher input reflection coefficient of the measured amplifier easily leads to the gain discrepancy between modeled and measured results. Note that the measured amplifier exceeds the 12 dB gain requirement.
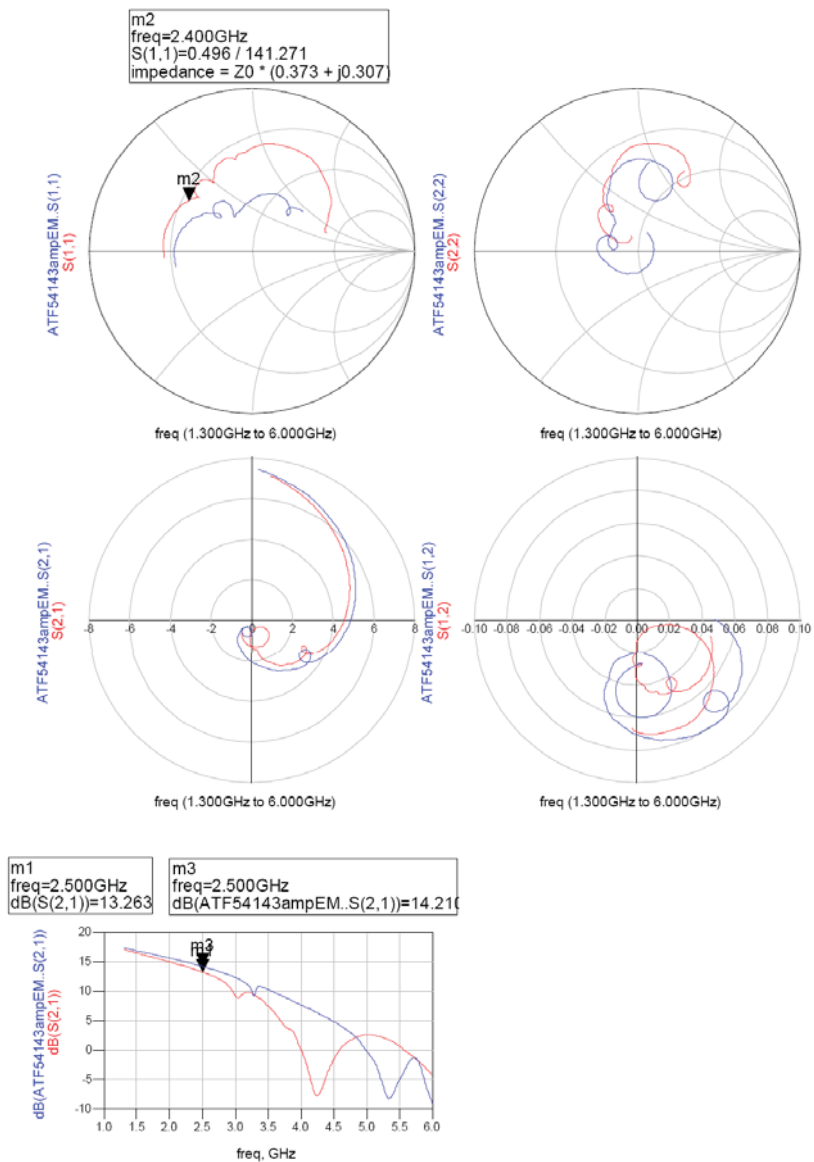
Figure 73. ATF54143Amp_NoInMatchCompare.dds

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The input matching network is now added by removing the DC blocking capacitor C5 at the amplifier input and replacing it with the 1.6 pF matching capacitor and adding the 2.4 nH Coil Craft air wound inductor at location L3 (Lmatch). S-parameter measurements using the TRL calibration procedure are repeated on the amplifier with the matching network in place. Figure 74 brings the measured data into ADS as shown.
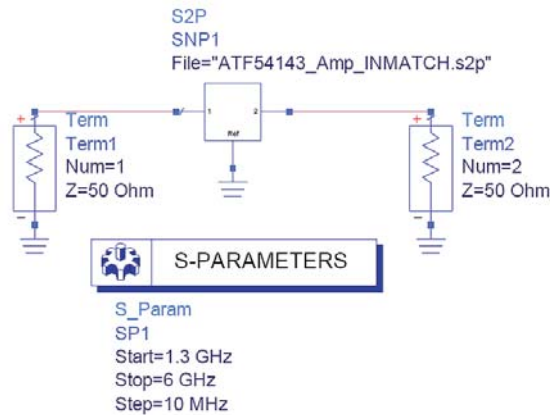

Figure 74. ATF54143_InMatchMeasured.dsn

Figure 75 plots the amplifier measured s-parameter data with the input matching network in place. The measured gain of 13.62 dB is shown along with an input return loss of 9.7 dB and an output return loss of 13.6 dB. The measured gain is slightly below the simulated value (14.2 dB) as was the case for the unmatched gain case because of the method used to estimate source ground parasitic inductance. The actual gain exceeds the 12 dB specification requirement with margin, and is therefore acceptable. Note that the input return loss of 9.7 dB marginally fails the 10 dB specification requirement, but will also be accepted in this particular design since the input return loss is considered to be a "soft" or negotiable specification. The output return loss of 13.64 dB exceeds the 10 dB goal with some margin. Figure 76 plots the simulated amplifier on the same graphs as the measured amplifier for an easier comparison. Note that the plots show a close agreement between simulated and measured data.

The noise figure and third order intercept point are now measured on the amplifier and compared to the simulated values. Noise figure is measured at 1.91 dB and input third order intercept point at 2.45 GHz is 13.6 dBm. The simulated noise figure of 1.78 dB closely predicts the measured value. The measured third order input intercept point of 13.7 dBm is substantially better than the 7 dBm simulated value. An Avago representative confirms that nonlinear performance of the actual device is somewhat better than modeled performance. Note that the measured nonlinear performance is significantly better than the 0 dBm specification requirement.

m1
freq=2.500GHz
S(1,1)=0.327 / -102.412
impedance = Z0 * (0.716 - j0.512)

m2
freq=2.500GHz
S(2,2)=0.208 / 160.653
impedance = Z0 * (0.666 + j0.096)

S(1,1)

freq (1.300GHz to 6.000GHz)

S(2,2)

freq (1.300GHz to 6.000GHz)

m3

S(2,1)

freq (1.300GHz to 6.000GHz)

m3
freq=2.500GHz
S(2,1)=4.795 / 58.923

m4
m6

dB(S(2,2))
dB(S(1,1))

freq, GHz

m5

dB(S(2,1))

freq, GHz

m4
freq=2.500GHz
dB(S(1,1))=-9.711

m6
freq=2.500GHz
dB(S(2,2))=-13.641

m5
freq=2.500GHz
dB(S(2,1))=13.616

Figure 75. ATF54143_InMatchMeasured.dds

m2
freq=2.450GHz
S(1,1)=0.238 / -70.633
impedance = Z0 * (1.050 - j0.500)

m3
freq=2.450GHz
S(2,2)=0.214 / -103.262
impedance = Z0 * (0.834 - j0.364)

m5
freq=2.450GHz
ATF54143_InMatchMeasured..S(1,1)=0.330 / -96.032
impedance = Z0 * (0.756 - j0.558)

m6
freq=2.450GHz
ATF54143_InMatchMeasured..S(2,2)=0.197 / 163.539
impedance = Z0 * (0.679 + j0.079)

freq (1.300GHz to 6.000GHz)

freq (1.300GHz to 6.000GHz)

m7
freq=2.450GHz
S(2,1)=5.513 / 72.982

m8
freq=2.450GHz
ATF54143_InMatchMeasured..S(2,1)=4.921 / 64.364

freq (1.300GHz to 6.000GHz)

freq (1.300GHz to 6.000GHz)

m1
freq=2.500GHz
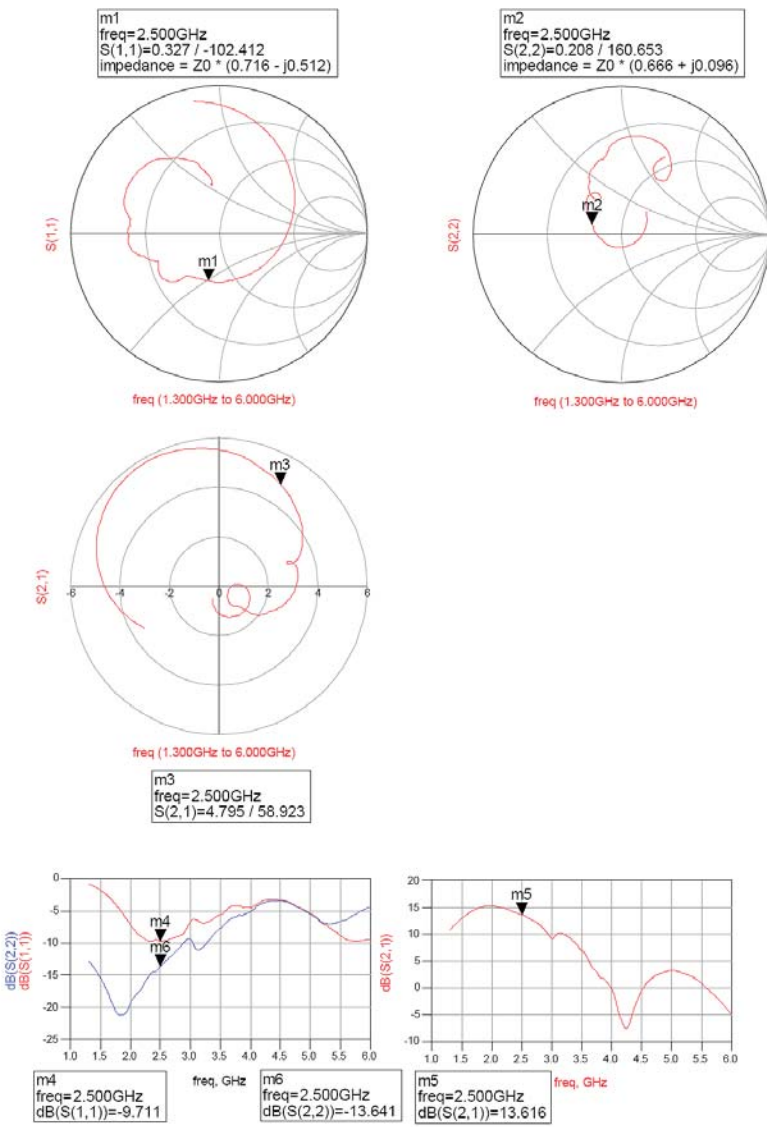dB(S(2,1))=14.646

m4
freq=2.500GHz
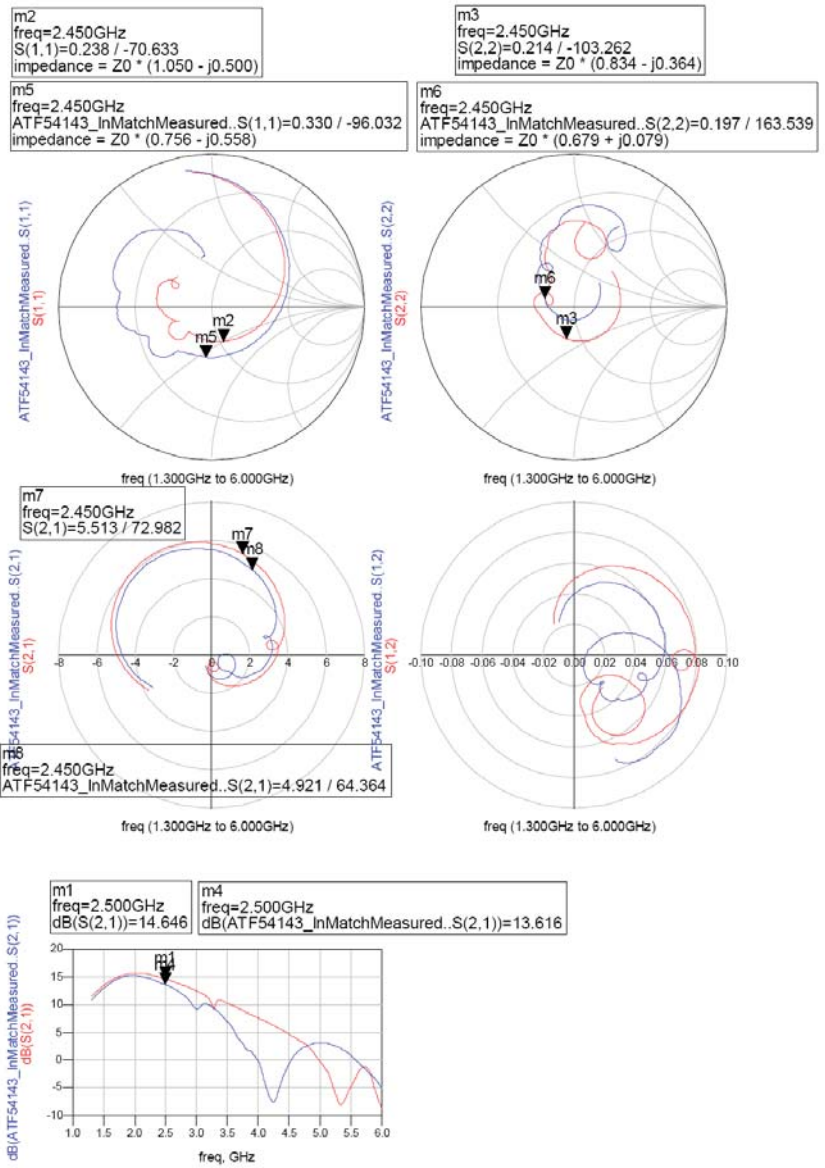dB(ATF54143_InMatchMeasured..S(2,1))=13.616

Figure 76. ATF54143_AmpCompare.dds

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Conclusion

The simulated and measured amplifier that includes PCB layout and component parasitics meets all amplifier design requirements as illustrated in Table 6:

	Specification requirement	Simulated value	Measured value
Frequency range	2.4 GHz to 2.48 GHz	2.4 GHz to 2.48 GHz	2.4 GHz to 2.48 GHz
Gain	> 12 dB	14.65 dB	13.62 dB
Noise figure	< 2.5 dB	1.78 dB	1.91 dB
IP3i	> 0 dBm	6.9 dBm	13.7 dBm
Input return loss	> 10 dB	12.7 dB	9.7 dB
Output return loss	> 10 dB	13.6 dB	13.6 dB
Current drain	< 100 mA	61.38 mA	63 mA
Supply voltage	3.3 V	3.3 V	3.3 V
Stability	Unconditional	Unconditional	Unconditional

Table 6.

Table 6 indicates that the first-pass amplifier exceeds most of the requirements. The input return loss is marginal but acceptable. The input match could be adjusted slightly to improve input return loss at the possible expense of noise figure. One of the main objectives was to obtain a working design with the first pass layout. The procedure is considered successful as long as the layout does not have to be altered to obtain a working circuit. The procedure is also considered a success if the components had to be slightly adjusted to achieve performance without a layout modification. In this case, the circuit components did not require adjustment to meet the objectives.

Using the EM/Circuit Co-Simulation capability in ADS allows a first-pass design. Careful attention to layout and simulation results speeds the design process and provides a design cost savings by avoiding multiple pass PCB designs. Note also that the entire PCB does not have to be simulated with the EM simulator to obtain good results. Putting the entire PCB in the simulator may improve the results at the expense of significantly longer simulation time.

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KEN PAYNE began his engineering career at RCA, developing circularly polarized TV and FM broadcast antennas and feed systems. He was also involved with wide bandwidth receivers and transmitters, covering from DC to 1GHz, for fiber-optic test equipment. Later, at Motorola's Communications Division, he designed RF amplifiers, mixers, filters, oscillators, antennas and other transceiver circuits and systems for two-way portable and paging products. He developed and directed circuit and system design projects and created a wide range of active and passive RF device models for the HP-EEsof Microwave Design System (MDS) and Advanced Design System (ADS). In addition, Ken also developed RF and microwave design automation, measurement techniques, and interfaces between design workstations and test equipment. As a sideline, he conducted seminars and wrote articles on design methodologies for high performance, low-cost, and high-yield wireless communication circuits and systems. Ken was an instructor for Besser Associates and CEI of Europe for many years where he gave training seminars on RF design and measurement methodologies. Ken was one of the authors of the Oscillator Design Guide available in ADS. Ken now provides consulting services in RF/microwave design.

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France	0825 010 700*
	*0.125 €/minute
Germany	07031 464 6333
Ireland	1890 924 204
Israel	972-3-9288-504/544
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland	0800 80 53 53
United Kingdom	44 (0) 118 9276201

Other European Countries:
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