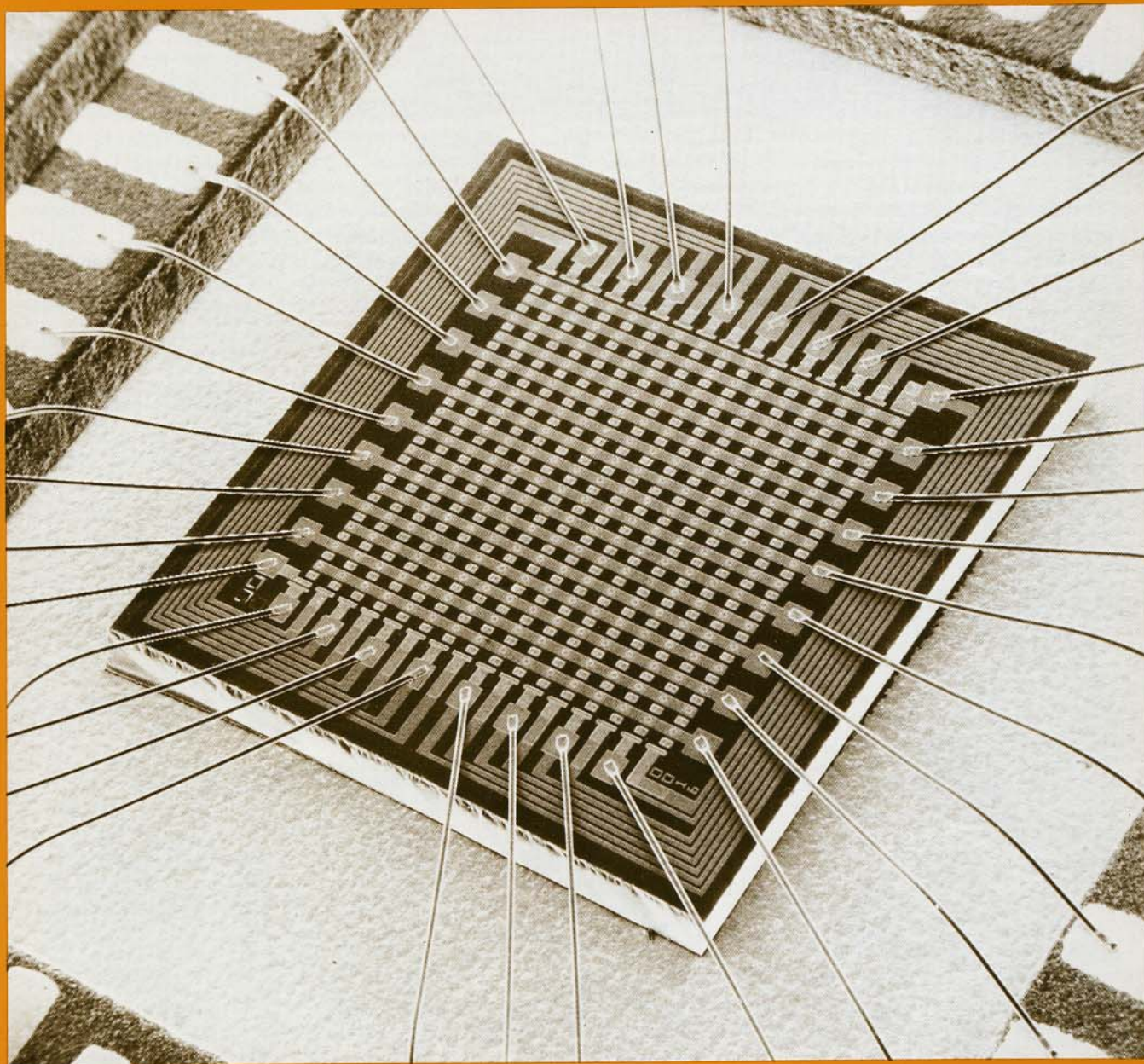


Testing Ovonic Read-Mostly Memories

A Solution to a Measurement Problem for: ENERGY CONVERSION DEVICES
Troy, Michigan



The RM-256 Memory array. Typically configured as a 16 x 16 matrix, the circuit includes a diode-isolated Ovonic memory switch at each crosspoint. The chip size is 116 x 126 mils.

Testing Ovonic Read-Mostly Memories

At Energy Conversion Devices in Troy, Michigan, a Hewlett-Packard computer system controls research, development, and production testing of a relatively new type of memory element – the read-mostly memory (RMM). Based on Ovonic technology – first used by ECD – the RMM combines amorphous and silicon semiconductors to provide a non-volatile device with repetitive electrical alterability.

In terms of some of the more common memory devices, the RMM provides: (a) the data retention capabilities of the read-only memory (ROM), (b) the field programmability of “write-once” devices such as a programmable ROM, a fusible ROM, or a scribable ROM, and (c) the re-programmability of a random-access memory (RAM). Thus, the RMM might well be thought of as an electrically alterable ROM, or a fast-read/slow-write RAM, or a re-programmable diode memory. Energy Conversion Devices is presently producing a variety of Ovonic memories for both read/write and read-

only systems. A highly successful product of ECD’s capability is exemplified by the Ovonic RM-256 Read-Mostly Memory; a chip is shown on the front cover (see box for more details). It is particularly suited for a diversity of applications such as microprogramming, machine tool control, table look-up, character generation, and emulation.

CONFIGURING THE TEST SYSTEM

During its initial R&D stages, the Ovonic memory switch was physically large enough for easy handling, thus allowing performance characteristics to be measured in the traditional manner with probe and instrument. Ongoing technological improvements in the switch have brought about a considerable reduction in its size. In fact, using thin-film, large-scale integration techniques, an entire 256-bit chip now measures only 116 x 126 mils (3.04 x 3.20 mm), with further size reduction imminent.

THE OVONIC RM-256 READ-MOSTLY MEMORY

The RM-256 Read-Mostly Memory, as shown in the partial schematic diagram of Figure 1, is a 16 x 16 matrix with a diode-isolated Ovonic memory switch (OMS) at each crosspoint. Organization can be 256 x 1, 128 x 2, 64 x 4, 32 x 8, or 16 x 16 as desired. It can also be expanded vertically and horizontally to add bits and words. Figure 2 is a close-up showing some OMSs and diodes in an RM-256. The individual OMS is an amorphous glass semiconductor device sandwiched between two molybdenum electrodes and connected to the silicon diodes by an aluminum metallization. The OMS derives its unique memory characteristics from the fact that it is, in essence, an electrically resettable bistable resistor. It can exist in either an amorphous phase (non-conducting) or a polycrystalline phase (conducting). The OMS can be reversibly and repetitively switched between these two phases by application of controlled energy/time pulses. It exhibits a very high resistance (300K ohms) in the amorphous phase and a very low resistance (500 ohms) in the polycrystalline phase. In addition, the OMS will retain either state indefinitely – even if all power is removed from the circuit.

When the electrical pulse is applied to the amorphous material so that a predetermined transition point is reached, the material undergoes a reversible structural change to the polycrystalline phase, at which time its resistivity also changes from 5×10^4 ohm-cm to 0.3 ohm-cm; this is the SET function. The material may be changed back (RESET) to its high resistance amorphous state by applying a pulse with the proper energy/time profile. READ functions can be accomplished by sensing the resistance of the OMS, or in a selective manner by applying a low current to the OMS and sensing the voltage drop across each cell.

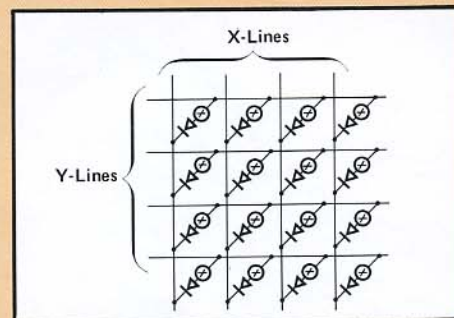


Figure 1. Partial schematic diagram of the RM-256 matrix (16 x 16). Symbol \otimes represents an Ovonic memory switch.

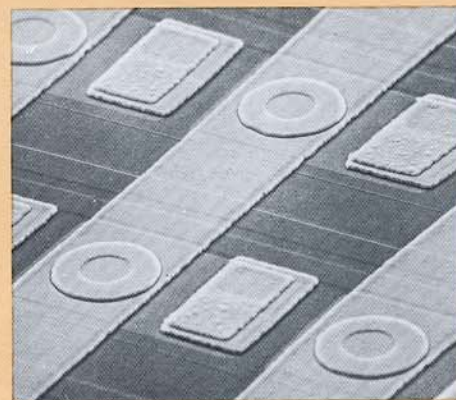


Figure 2. Scanning electron micrograph of the RM-256 Memory array. Circles are Ovonic memory switches; the rectangles are pn diodes.

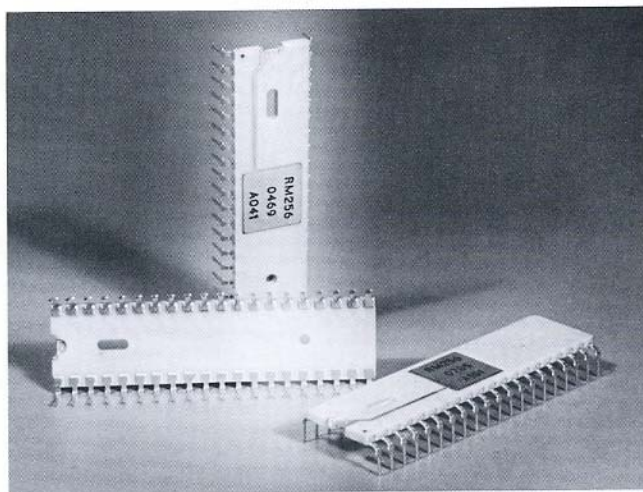


Figure 3. RM-256 Read-Mostly Memories, fully tested and packaged – ready for use.

The need for testing was an established fact – it had to be done because the very nature of the electronic device demands extensive proof of performance. Moreover, testing individual chips and weeding out the bad and weak from the good before packaging, and packaging only the good chips, can result in a substantial cost savings. Packaged RM-256s are shown in Figure 3. The only question was: what techniques and equipment would best suit ECD's testing needs?

Once in the production stage, it became quite evident that the very large amount of testing that would be required and the number of data values needed were much too great for manual testing. Also, the passed/failed criteria of the Ovonic memory are far more complicated than some types of go/no-go testing where a decision is based on whether a voltage level is above or below a certain value. Further, ECD required a multi-testing capability to handle packaged RMMs as well as arrays of RMM chips on silicon wafers. And lastly, since ECD anticipated new and varied memory configurations, a system was required that could be expanded to handle future needs at minimum cost and minimum system downtime.

The newness of Ovonic memory technology and the very real need for high-volume testing, led ECD to study the various data acquisition techniques and component testers available. Since no in-house precedent was established, ECD applied the above criteria in selecting its test system. Results of the study ruled out the use of specialized testers because: (1) a separate and complete tester would be required for each test stand and be dedicated to that stand only, and (2) existing testers were primarily designed to retrieve and log data and, as such, had little data analysis capability. ECD needed to analyze the raw data in order to print out final measurement results in a readily understood digital format. These factors very clearly indicated that only a highly-flexible computerized data acquisition system could supply the measurement needs.

ECD chose the computerized system shown in Figure 4 as the best solution to its Ovonic memory testing requirements. At the heart of the system is an HP 2116B Computer with 16K 16-bit words of memory. The computer is equipped to interface with a wide variety of data logging and display peripherals and data input devices, in addition to those specifically used in the memory test system. Three teleprinters are used for general purposes of communication with the system and also for hard-copy printout. The high-speed tape punch is used to obtain a paper tape copy of an edited source or object program, and for a permanent copy of some test results that can be reprinted on an off-line teleprinter or reentered into the computer for further analysis. The high-speed punched tape input (reader) is used to read source and binary programs, long edit files, etc. into the system. The two magnetic tape units provide read and write capabilities in IBM-compatible 9-track format and are for long-term storage of test data. The disc memory is used for storage of test system programs and library subroutines, temporary storage of data, and program swapping. Programs stored on the disc are swapped into core for execution and then returned to the disc.

The automatic test system controller, assembled in-house by ECD, consists of two dual HP power supplies which provide specified voltages to devices under test, a multiplexer capable of handling analog data from as many as eight test stations, an analog-to-digital converter to convert the analog data into a computer-compatible input, and a test and measurement

controller. Figure 5 shows the physical arrangement of the controller and two test stations inside the test lab; the computer system, Figure 6, is directly across the room, approximately 10 feet from the controller. Equipment inside a test station is shown in Figure 7; this is a wafer tester. Both the microscope and X- and Y-driver boards are shown in the non-test position in 7(a), revealing the wafer which holds 180 chips, each containing a 16 x 16 array of 256 bits. The waveform generator is on the right. Present configuration of the system allows on-line simultaneous operation of as many as eight test stations (three are presently in use) by merely adding the necessary cabling for digital control and data.

ON-LINE FLEXIBILITY

ECD is very successfully utilizing the power of the Hewlett-Packard real-time executive (RTE) software operating system to achieve highly reliable test results throughout its multiple test facility. Under RTE control, tests are conducted in a real-time, priority-oriented, multiprogramming environment. *With the RTE, the computer controls tests from the several test stations simultaneously in the real-time mode and, at the same time, allows low-priority activities such as program compilation, debugging, and general scientific jobs to take place.* Real-time collection of test data and control signal generation are handled in a section of computer memory designated as foreground, while low-priority activities are handled in the background area of core.

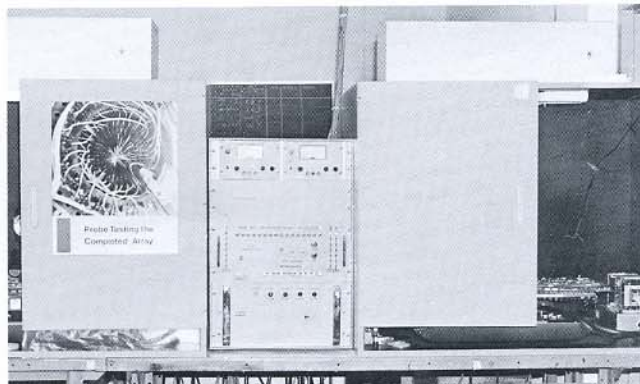


Figure 5. The automatic test system controller (center) handles control, A-D conversion, and signal switching for eight test stations, including the two wafer testers shown. Mounted on the test station door at left is a closeup photo of the probe.



Figure 6. The computerized test system, in the background, has just completed a test sequence, and a hard-copy printout is checked over by Mr. R.L. Herrmann, data processing manager.

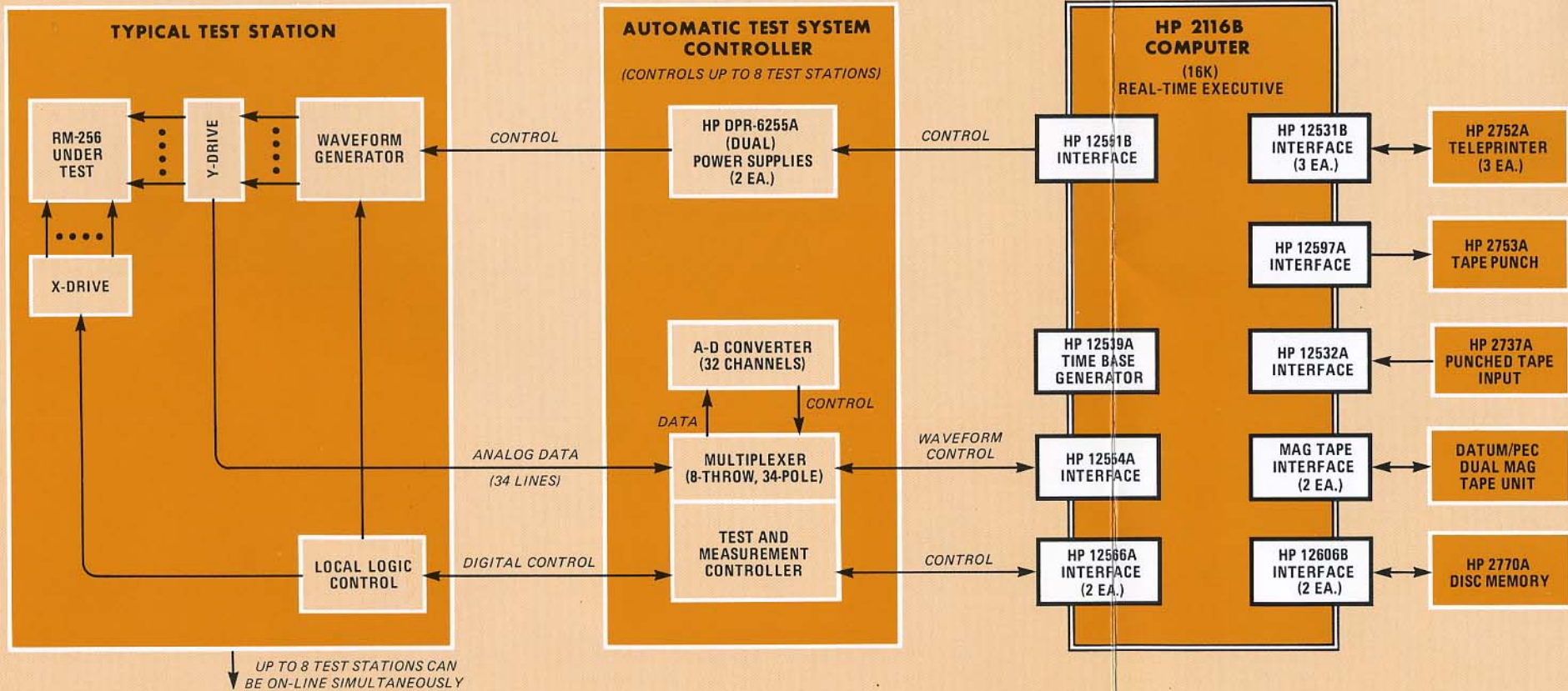
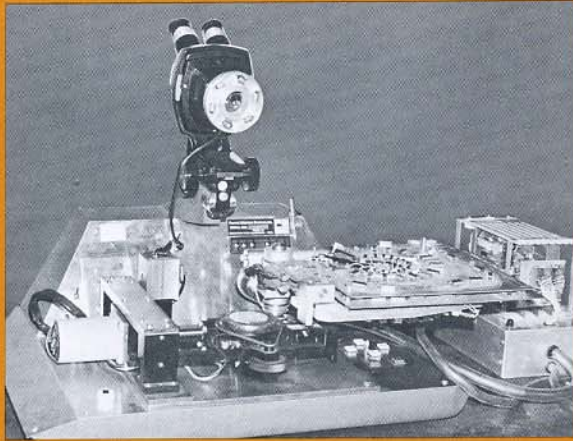
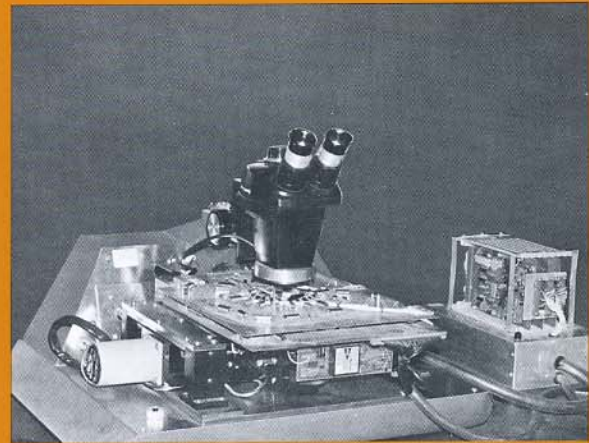


Figure 4. Computerized system for testing Ovonic memories at Energy Conversion Devices.



(a) A wafer (center foreground), containing 180 chips. The microscope and X- and Y-driver boards are shown in the non-test position.



(b) Wafer test in process. The microscope and X- and Y-driver boards are shown in the test position. The waveform generator is on the right.

Figure 7. Inside a wafer test station.

SYSTEM OPERATION

Production testing the RM-256 is done in two phases: (1) wafer testing where individual chips are thoroughly tested before packaging, and (2) packaged array testing where chips which have passed the wafer tests are now packaged and given a final functional test.

The microscope is used to align the wafer (typically containing 180 chips) such that the prober tip contacts will meet exactly on a chip when in the test position. Contacts on the prober tip correspond to the 16 X-lines, 16 Y-lines, and substrate line on the chip. Once aligned, the computer commands the prober to step to a chip and make a test, then step to the next chip to make a test, until all chips on the wafer are tested.

A comprehensive library of FORTRAN callable test subroutines, combined with the RTE software system, enable many thousands of data values to be accumulated and analyzed during the course of a test. The raw data are extensively reduced and then printed out in a passed/failed code. The code consists of a 16-bit pattern of 0s and 1s; a 0 means the chip passed that test and a 1 means the chip failed that test. Thus, the computer condenses many thousands of measurement values from each chip into a single 16-bit pattern. A fully tested wafer, then, is represented by 180 16-bit patterns.

As an example of the extensive testing procedures, consider some of the tests involved in a single bit, say bit 11, in the 16-bit pattern. Calculation of this bit begins by cycling each bit on the chip a number of times in rapid succession and gathering information on threshold and conduction voltages. This information is reduced to maximum and minimum values, average, standard deviation, etc. Based on these values, plus data from several other calculations and comparisons such as the relation between present standard deviation and standard deviation from prior readings, and comparisons of absolute magnitude to another value stored in memory, the computer makes a decision to drive the 11th bit as a 0 or a 1. In the event a chip fails a particular test, the software has built into it a sequence which stops further testing on that chip and steps the prober to begin testing the next chip.

Reduced data are stored on disc until a test is completed. This information is then called from storage for recording on magnetic tape, punched tape, or teleprinter for hard copy printout (0 and 1 pattern). The prober then steps to the next chip and begins a new test sequence. After testing all chips on the wafer, the information from the disc is further analyzed to provide a certain amount of statistical information on the entire wafer, in addition to the passed/failed printout. The wafer data summary typically lists: (1) total number of chips tested, (2) number and percentage of total that passed, and (3) various other percentages along with present yield. Along this same line, different tone patterns generated within the computer during testing are picked up by a small transistor radio mounted on the front of the computer, forming a rather unusual "peripheral" to give a running account of how the test programs are operating. Mr. Robert L. Herrmann, manager and architect of ECD's system, has learned to decipher the tone patterns to follow the sequence of tests.

Chips which have passed the exhaustive wafer tests are packaged and given final tests on a packaged array tester; these testers are electronically identical to the wafer testers. Typically, the silicon diodes and metallization are tested for shorts along with a functional test to determine set and reset capability.

BENEFITS OF COMPUTERIZED TESTING

The computerized test system continues to provide a most significant benefit, applicable to both ECD and its customers: a high degree of confidence that the RM-256 will perform reliably and accurately in accordance with specified requirements. A great deal of data, gathered by 100% testing, are stored on magnetic tape, thus forming a sound statistical data base. Utilizing the computer's data analysis capability, this invaluable reference source is subsequently used by physicists and design engineers to derive useful information for ongoing memory development. From a manufacturing standpoint, the system has reduced testing costs by better than a factor of 10 and has increased production capacity several orders of magnitude over manual testing.



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