

SELECTING THE RIGHT DVM



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INTRODUCTION

The purpose of this application note is to act as a guide in selecting the right DVM from among the many units on the market. This application note will help the user match his application with the various DVM characteristics. The fundamental building blocks of a DVM act as a good starting point. The next topics covered are the A-to-D conversion techniques. These techniques govern a DVM's speed and, to some extent, its noise rejection characteristics. Noise rejection is covered in more detail in the following section. Converters and signal conditioners govern which functions a DVM is able to measure. The characteristics of these "front ends" are very important. Since a prime advantage of a DVM is its ability to be used in a system, a section is devoted to a simplified view of systems operation. Selecting the right DVM starts with its intended application but must be combined with the knowledge required to read and compare DVM data sheets. The last section covers some of the more difficult to understand specifications.

Digital voltmeters (DVM's) have gained widespread acceptance as general purpose measurement tools. In some cases, DVM's have replaced other types of voltmeters. Why this popularity? One obvious advantage is the readout. The result of a measurement is displayed automatically in an easy-to-read manner. The reading is in digits rather than meter deflection. The reading includes decimal point, polarity and units. Many DVM's have automatic ranging to select the optimum range with the greatest resolution. These features make DVM's easy to operate, thus reducing human error.

DVM's have other advantages which involve some of the basic differences in measuring instruments. For example, DVM's have greater resolution than analog meters. The best resolution which can be expected from an analog meter is one part in 120. The lowest resolution 3-digit DVM has a resolution of one part in 1,000. A 6-digit DVM resolves one part in one million.

Although DVM's are generally less accurate than differential voltmeters, they are many times better than analog voltmeters. The best analog meter would have an accuracy specification of $\pm(1/2\%$ of reading + $1/2\%$ of range). A 3-digit DVM (costing not much more) would have 5 times better accuracy. On the opposite end, the best DVM would have an accuracy of $\pm 0.006\%$. A differential voltmeter might have 3 times better accuracy than the best DVM.

DVM's are faster than either analog voltmeters or differential voltmeters. A typical analog voltmeter will take a second or more to respond. Differential voltmeters must be manually nulled to build up the reading, a process requiring many seconds. In contrast, even a relatively slow bench DVM takes at least 5 readings per second. Systems oriented DVM's take up to 1000 readings per second.

A big advantage of a DVM is that the reading can be transmitted digitally without loss of accuracy. DVM readings can be fed directly into a computing device. DVM's are programmable; ranges, functions and filtering can be changed by remote control. Unlike analog voltmeters or differential voltmeters, DVM's are suitable for use in a system.



Analog voltmeters, differential voltmeters and digital voltmeters are contrasted as to their readout, accuracy, sensitivity, resolution and speed. Digital voltmeters have many advantages including the ability to make measurements automatically and to transmit data digitally.

BUILDING BLOCKS

The job of a DVM is to convert an analog signal into its digital equivalent. The analog signal might be a dc voltage, an ac voltage, a resistor, or an ac or dc current. Some DVM's also measure capacitance and frequency. The process of meeting this goal can be divided into four functional blocks as shown in Figure 2-1.

The input signal must first pass through some type of signal conditioner. If the input signal to be measured is a dc voltage, the signal conditioner may be composed of an attenuator for the higher voltage ranges and a dc amplifier for the lower ranges. If the input signal is an ac voltage, a converter is used to change the ac signal to its equivalent dc value. By supplying a dc current, an ohms converter changes resistance to a dc voltage. In nearly all cases, the input signal conditioner converts the unknown quantity to a dc voltage which is within the range of the A-to-D converter.

The job of the A-to-D converter is to take a prescaled dc voltage and convert it to digits; A-to-D converters are single range dc devices. Some take a 1V full scale input while others take a 10V full scale input. For this reason, the signal conditioner must attenuate higher voltages and amplify lower voltages to give the DVM a selection of ranges.

Let's take an example. Suppose a 250V ac signal is applied to a DVM with an A-to-D converter which requires a 1V dc input. The ac signal is attenuated on the 1000V ac range and converted to a dc voltage equal to 0.25V. Conversion and attenuation is carried out in the signal conditioner which, in this case, is an ac converter. The 0.25V dc is digitized by the A-to-D converter to "2500." The decimal point and units are announced from information gathered from the converter's ranges so that the final reading appears as "250.0V ac."

These first two building blocks govern the DVM's basic characteristics such as its number of digits, its ranges, its sensitivity, etc. The logic block manages the flow of information and insures that the various internal functions are carried out in the correct order. The logic also acts as a communicator with the outside world. The logic manages the outward flow of digital information and accepts programming instructions from other devices. The display communicates visually the result of a measurement. In selecting a DVM to fill a specific application, these building blocks combine to give the instrument its characteristics.

A-to-D CONVERTERS

The A-to-D converter is one of the most important components of a DVM. It converts the analog input signal into a digital signal that can be processed by the logic and displayed.

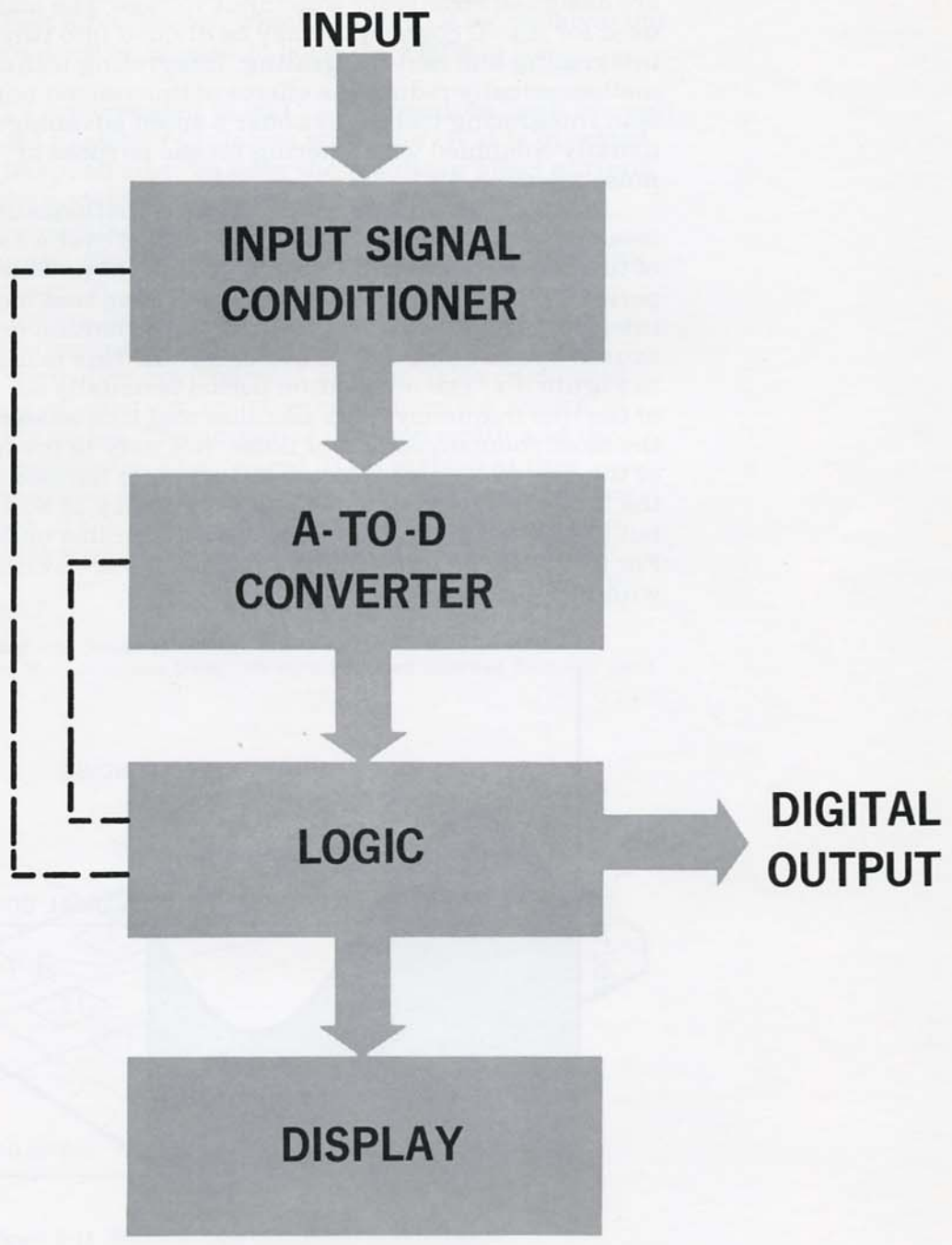


Figure 2-1. The basic building blocks of a DVM.

A-to-D CONVERTERS

The A-to-D converter used in a DVM governs some of the instrument's basic characteristics. This includes its speed and, in some cases, its ability to reject noise. A-to-D converters are designed strictly for a dc input voltage. The many methods used for A-to-D conversion may be divided into two groups: integrating and non-integrating. Integrating techniques mathematically reduce the effects of line related noise. Non-integrating techniques offer a speed advantage and are usually combined with filtering for the purpose of noise rejection.

Integration achieves noise rejection mathematically by measuring the average of the input signal over a fixed period of time. This time is called the "gate length" or "integration period." If the integration period is set such that it contains an integral number of noise cycles, the contribution or error caused by the noise will be averaged out. This is illustrated in Figure 3-1. The integration period is usually set to the period of the line frequency. This assumes that line related noise is the most common source of noise. Not only is the fundamental of the line frequency rejected but all of its harmonics. In the U.S. and Canada a power line frequency of 60 Hz is used but almost all of the rest of the World operates on 50 Hz. For this reason, many integrating DVM's are available with two gate lengths.

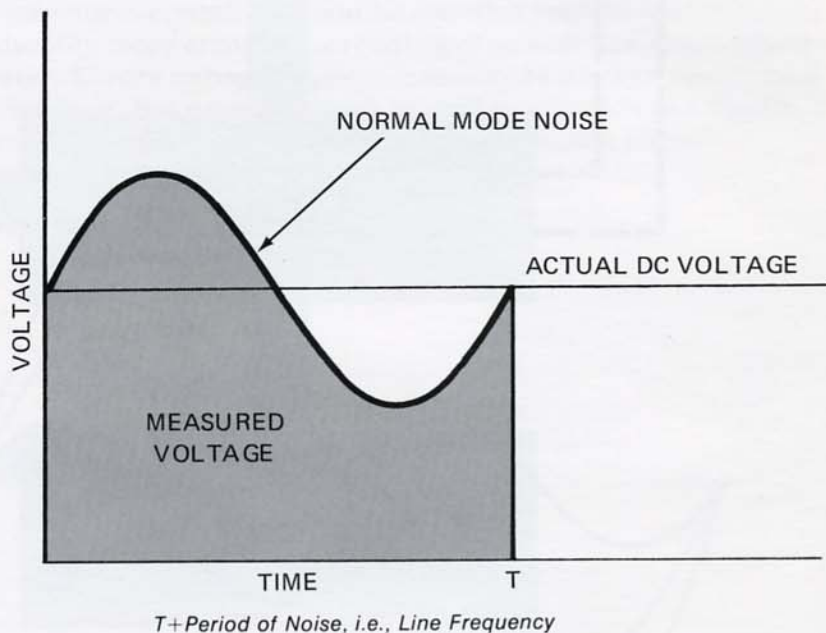


Figure 3-1. Integration eliminates the error caused by noise superimposed on the input signal provided T equals the period of the noise.

Figure 3-2 illustrates noise rejection in dB vs. noise frequency for both 1/10 s and 1/60 s integration periods. Note that both periods will reject 60 Hz noise but that the longer gate length, 1/10 s, has better rejection. The 1/10 s gate length, in addition, rejects 50 Hz noise. In fact, the 1/10 s gate length rejects all frequencies which are multiples of 10 Hz. A modern DVM, equipped with both 1/10 s and 1/60 s gate lengths, will have reading periods of 300 ms and 65 ms respectively. A basic principle is illustrated here: noise rejection can be improved by increasing the gate length but at the sacrifice of measurement speed.

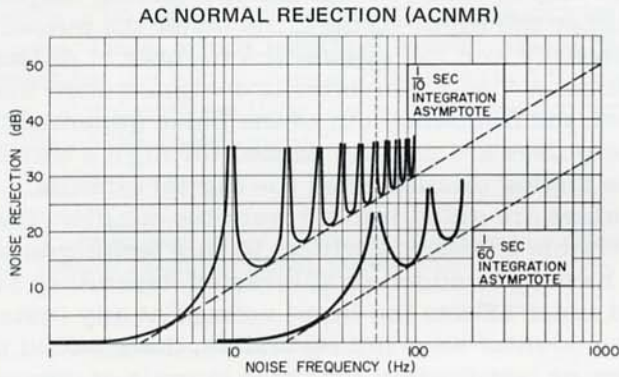
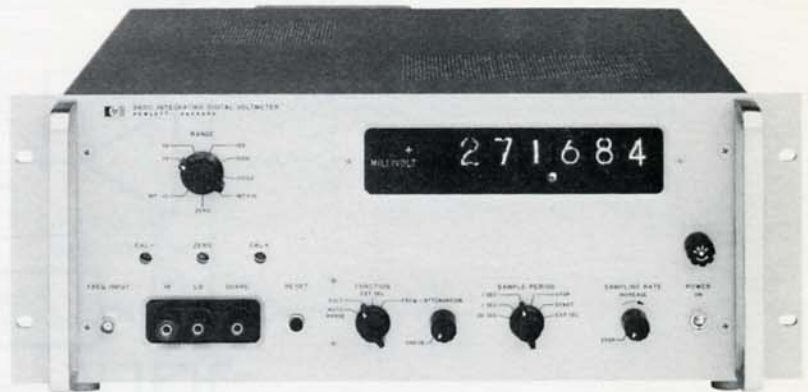


Figure 3-2. Noise rejection for an integrating DVM with 1/10 s or 1/60 s integration periods.

INTEGRATING TECHNIQUES

The voltage-to-frequency technique, which is still in use, was one of the first methods used to integrate the input signal. This technique is valuable in understanding many fundamental concepts in A-to-D conversion.



The -hp- 2401C uses the voltage-to-frequency technique to integrate the input voltage. Any of three integration periods may be selected: 1 s, 1/10 s or 1/100 s. Resolution, however, varies with integration period.

The voltage to the A-to-D converter is applied to a voltage controlled sawtooth generator as shown in Figure 3-3. The input voltage causes a current to flow through R_1 into the summing junction of an operational amplifier. This current causes C_1 to charge. The output from the operational amplifier departs from 0 V in a negative direction for a positive input voltage.

When the output voltage from the operational amplifier reaches $-V$, the comparator triggers the pulse generator. The pulse generator injects a fixed amount of charge in the summing junction via R_2 . The polarity of this pulse is switched to always tend to remove the charge on C_1 thus restoring the output voltage from the operational amplifier to zero. The higher the input voltage, the faster the output voltage reaches $-V$ and the greater the number of pulses per unit of time. A V-to-F converter is designed such that if V_{in} is doubled, the frequency out of the pulse generator is doubled. The pulses are usually passed through a transformer to isolate the analog circuits from the digital circuits.

These pulses are gated into a reversible counter. The use of a reversible counter is critical to this technique since pulses may have to be added or subtracted depending on how injected noise affects the input voltage at any instant in time. If the counter were not reversible, there would be a folding over or rectification for noise signals of opposite polarity as the input signal. This would produce a final reading greater than the average of the input signal. At the end of the integration period, the contents of the reversible counter are transferred to the display. At this time, the display usually contains the prior reading and will appear to change only if there is change in input voltage.

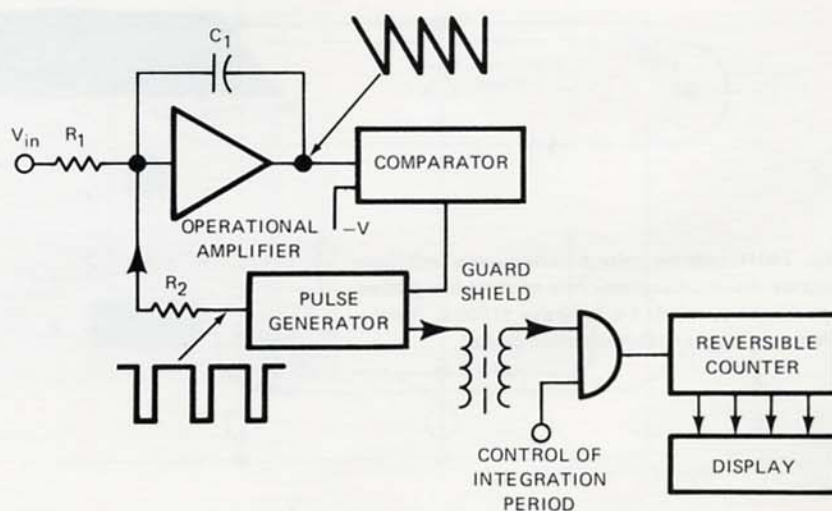


Figure 3-3. Simplified diagram of a voltage-to-frequency integrating DVM.

The voltage-to-frequency technique is limited in accuracy to the precision of the charge removal from C_1 and frequency linearity relative to the input voltage. Typically, V-to-F converters are limited to maximum frequencies of 300 kHz or less.

An important concept is that this frequency limit also limits resolution for a given measurement speed. For example, if the V-to-F converter is limited to 100 kHz, then only one 5-digit reading may be taken per second.

$$\begin{aligned} 5\text{-Digits} &= 100,000 \text{ (at full scale)} \\ 100,000 \text{ Counts/s} &= 100 \text{ kHz} = 1 \text{ Reading/s} \end{aligned}$$

For DVM's using the V-to-F technique, gate length may be selectable and, as a result, resolution will vary with measurement speed. An example of this taken from the -hp- 2401C data sheet is shown below:

| INTEGRATION PERIOD | READING RATE | READING ON 10 V RANGE |
|--------------------|--------------|-----------------------|
| 1 s | 1/s | 10.0000 V |
| 0.1 s | 9/s | 10.000 V |
| 0.01 s | 50/s | 10.00 V |

A modification of the "pure" V-to-F technique partly overcomes the speed vs. resolution limitation. This is the integrating-interpolation technique. The three most significant digits are established via normal V-to-F conversion. The two least significant digits are derived from the residual charge remaining on C_1 at the end of the integration period. By application of a known reference voltage, the time required to discharge C_1 to 0 V equals the two least significant digits. The scale reading for an -hp- 2402A using this technique is composed of the following elements:

$$\begin{array}{ccccc} & & 10.0000 & & \\ & & \text{BY} & \text{BY} & \\ \text{V-to-F CONVERSION} & & & & \text{INTERPOLATION} \end{array}$$

The advantage of the integrating-interpolation technique is speed. Over 40 5-digit readings per second are possible without changing the saturation frequency of the V-to-F converter.



The -hp- 2402A uses the integrating-interpolation technique to achieve 43 readings per second with 5-digit resolution. Effective common-mode rejection exceeds 168 dB at 60 Hz \pm 0.15%. The high effective CMR is a result of integration and guarding.

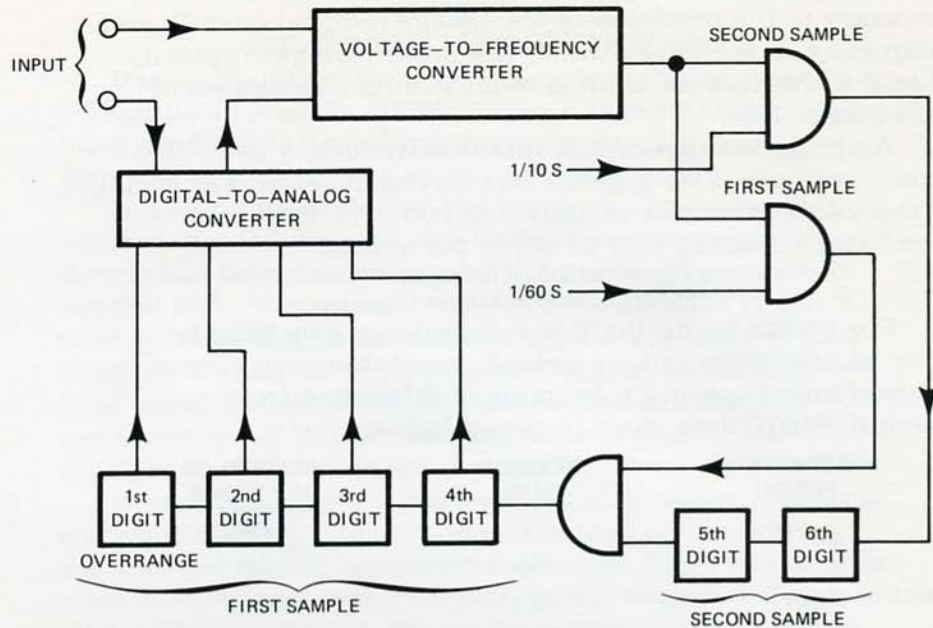


Figure 3-4. Simplified block diagram of the potentiometric-integrating DVM.

The next method of A-to-D conversion acts as an introduction to nonintegrating techniques since it combines the potentiometric technique with integration. The potentiometric technique generates an accurate internal voltage and nulls it against the input voltage. This is the same technique used by a differential voltmeter and, by combining it with integration, DVM accuracy is improved. A simplified block diagram is shown in Figure 3-4.

Each measurement is composed of two sample periods. The first sample makes a simple V-to-F conversion with 3-digit resolution plus an overrange digit. At the end of the integration period, this approximation to the reading is collected in the reversible counting units.

The digital results of this first sample are transferred to the digital-to-analog converter. A voltage equal to the first sample is generated and applied against the input voltage such that part of the input voltage is nulled out. The input to the V-to-F converter is now the difference between the first sample and the input voltage. A second sample is taken by the V-to-F converter and sent to the least significant digits. Once the entire reading is in the counting units, it is transferred to the display.

The demands on the V-to-F converter are less with the potentiometric-integrating technique since no more than 3-digit resolution (plus an overrange digit) is required at any one time. DVM accuracy is improved with excellent noise rejection at line related frequencies. Speeds of 15 readings/s are possible. This technique is not as fast as the integrating-interpolation technique but offers improved accuracy.



The -hp- 3460B uses the potentiometric-integrating technique to achieve $\pm 0.0006\%$ full scale accuracy for 90 days. The 3460B is able to take up to 15 readings per second with 5-digit resolution.

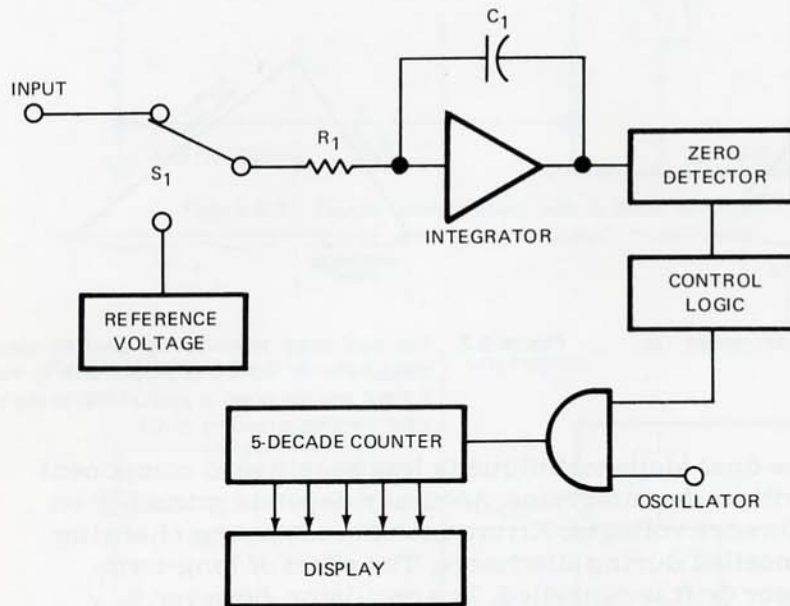


Figure 3-5. Simplified block diagram of a dual-slope integrating DVM.

One of the most important and popular techniques is the dual-slope method of A-to-D conversion. Due to its simplicity, it is used even where noise rejection is relatively unimportant. A simplified block diagram is shown in Figure 3-5. Instead of converting voltage to frequency, voltage is converted to time. A better picture can be gained of this technique by looking at the timing sequence shown in Figure 3-6.

The input voltage is connected to the integrator using switch S_1 for the duration of the integration period. During this time, C_1 is charged at a rate governed by R_1 . At the end of the integration period, C_1 is left with a charge proportional to the input voltage. The action of an operational amplifier, with a capacitor in its feedback loop, causes the voltage across C_1 to build linearly. The charging rate is, therefore, governed by the current through R_1 .

In the second phase of dual-slope operation, S_1 connects a reference voltage to the input of the integrator. The reference is always of the opposite polarity as the input voltage. Quite often two references are used; one negative and the other positive. C_1 is discharged linearly by the reference voltage. At the beginning of discharge, the output from the oscillator is gated into the counter. Gating is stopped when C_1 is discharged through zero.

If the input voltage is doubled, C_1 charges up twice as fast. Since a constant reference voltage is applied, the discharge rate will be constant. This means that the time to discharge C_1 is doubled for double the input voltage as shown in Figure 3-6.

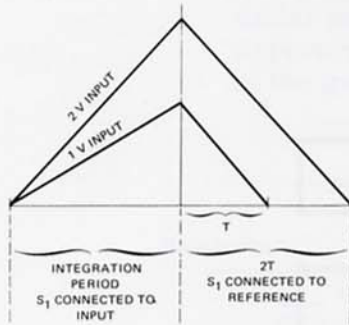


Figure 3-6. Dual-slope integration measurement sequence.

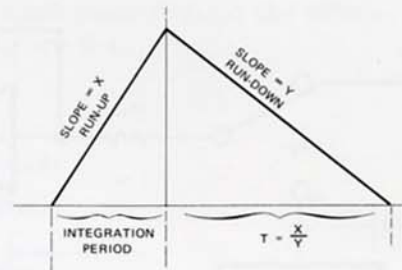


Figure 3-7. The dual-slope technique is ideal for ratio measurements. Run-up is proportional to the X input and run-down is proportional to the Y input yielding a reading of X/Y .

The dual-slope technique is less sensitive to component drift within the integrator. Accuracy depends primarily on the reference voltages. Errors introduced during charging are cancelled during discharge. The effect of long-term oscillator drift is cancelled. The oscillator, however, is usually crystal controlled since it is also used to establish the integration period.

The dual-slope technique is ideal for ratio measurements. The reference voltage may be substituted by an external reference voltage, Y. If the input is defined as X, then the time required for discharge equals X/Y as shown in Figure 3-7.

Dual-slope 5-digit DVM's are able to make up to 15 readings per second; about equal in speed and resolution to the integrating-potentiometric technique.



The hp-3450B is one of many Hewlett-Packard DVM's using the dual-slope integrating technique. The 3450B measures not only ac, dc, and ohms, but also has a four-terminal ratio input which may be used to measure the ratio of two independent, floating voltages.

NONINTEGRATING TECHNIQUES

The linear ramp technique acts as a good starting point leading into other nonintegrating techniques. As shown in Figure 3-8, the input voltage is converted directly to time. A linear ramp which swings from positive full scale to negative full scale is compared against the input voltage. As shown in Figure 3-9, two comparators are used: one to detect coincidence with the ramp and the input voltage, and the other to detect coincidence with the ramp and ground. The order in which coincidence occurs determines polarity. A positive input voltage reaches the input comparator first then the ground comparator.

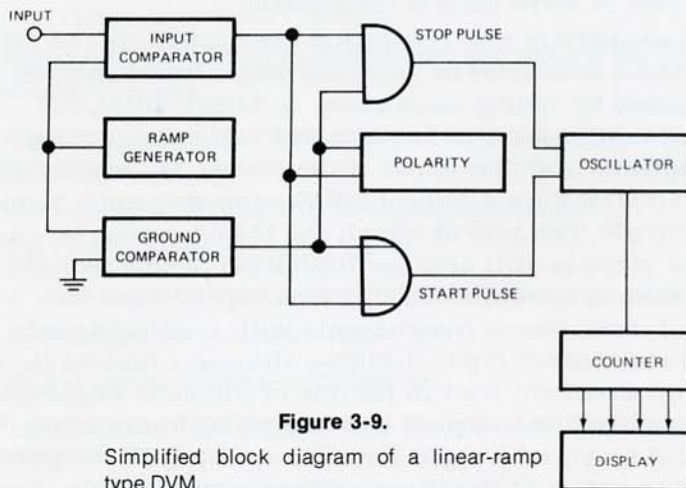


Figure 3-9.

Simplified block diagram of a linear-ramp type DVM.

The pulses from both comparators gate the output from an oscillator into a counter. The slope of the linear ramp and the frequency of the oscillator are chosen to make an accurate voltage-to-counts conversion. Accuracy is highly dependent on ramp linearity and oscillator stability. Readings beyond full scale (overrange) are difficult to make due to design limitations in keeping the ramp linear over a wide dynamic range. Noise creates serious errors by causing coincidence at the wrong points as shown in Figure 3-10. A great deal

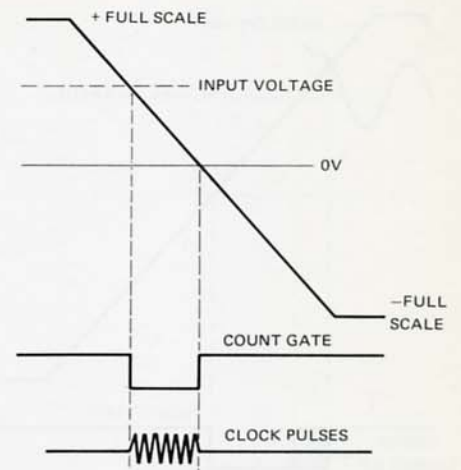
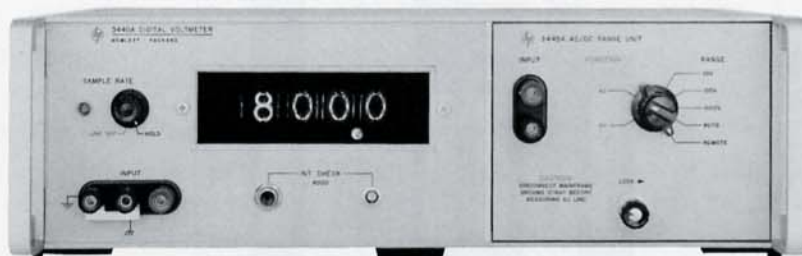


Figure 3-8.

Time sequence for the linear-ramp technique of A-to-D conversion.



The -hp- 3440A uses the linear ramp technique to make 4-digit readings at 5 per second. Accuracy is $\pm 0.06\%$ for 30 days using an internal zener reference calibrator. A front panel pushbutton allows the user to check calibration at any time.

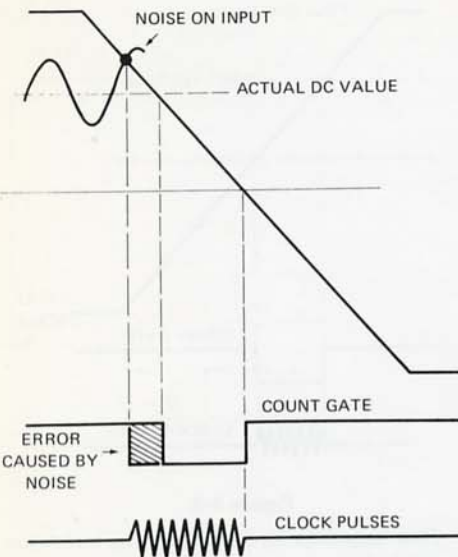


Figure 3-10.

Noise causes serious errors in the linear-ramp technique of A-to-D conversion.

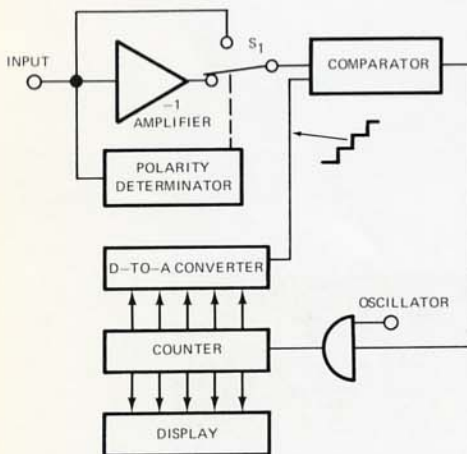


Figure 3-11.

Simplified block diagram of a staircase-ramp DVM.

of filtering is usually incorporated to prevent noise from reaching this type of converter.

The effect of oscillator drift, as it effects accuracy, can be eliminated from the linear ramp technique by using a staircase ramp. This technique is used in a relatively small number of DVM's but it illustrates some basic concepts. The staircase-ramp technique is illustrated in Figure 3-11. The oscillator not only provides clock pulses to the counter but also generates the staircase. The staircase goes from 0 V to positive full scale. Negative input voltages are passed through a -1 amplifier. Each step is of equal weight and when coincidence is reached with the input voltage, the number of steps equals the reading.

The sensitivity and resolution are limited by the ability of the D-to-A converter to generate steps. Resolution can only be increased by using more steps. A 3-digit DVM, for example, requires 1,000 steps at full scale and a 5-digit DVM requires 100,000 steps. If the lowest full scale range equals 100.0 mV on a 3-digit DVM, each step must then equal 100 μ V. The rate at which the D-to-A converter can generate steps is still another limitation of this technique. These reasons have limited this technique to use in low-resolution, bench instruments with reading speeds of 2/s.

The staircase-ramp technique, although limited in use, acts as an excellent lead-in for one of the most important nonintegrating techniques: successive approximation. Instead of an equal weight for each step, a BCD weighting is given to arrive at the input voltage more quickly. For each digit, only 4 "trys" or approximations are needed instead of 10 "trys" or steps. The advantage of this technique is its speed and accuracy. This technique is, however, vulnerable to incoming noise and is invariably associated with filtering.

The successive approximation technique generates a set of voltages sequentially. This same set of voltages is generated for every measurement. Voltages are generated in an 8, 4, 2, 1 BCD weighted sequence as shown in Figure 3-12. Each voltage is compared to the input voltage

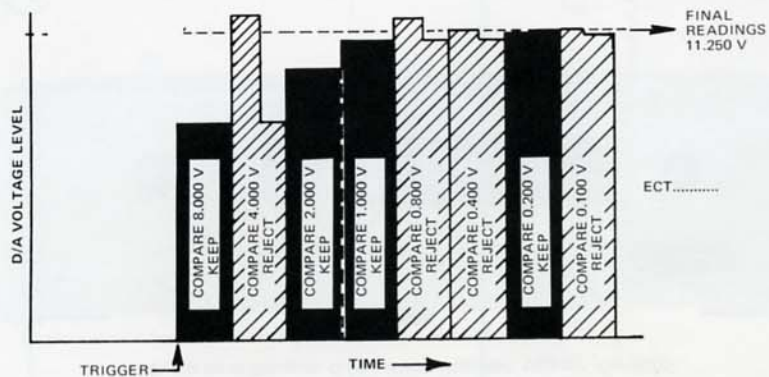


Figure 3-12. The use of successive approximation to convert 11.250 V into its digital equivalent using an 8, 4, 2, 1 BCD sequence.

and, if higher, is rejected. If lower than the input voltage, its value is kept on the D-to-A switches and added to any other voltage held over from preceding tries. As shown in the block diagram in Figure 3-13, the comparator acts as a null detector.

Assume that full scale of the A-to-D converter is 10 V. The first digit is established by generation of 8 V, 4V, 2 V, and 1V. After completion of this sequence, the magnitude of the voltages is decreased by a decade. The next digit is established by a 0.8 V, 0.4 V, 0.2 V and 0.1 V sequence, then the magnitude of the voltages is dropped by another decade. For a 4-digit reading, there will be 4 sequences of 4 tries. Overranging of 50% is automatic since the maximum reading equals "15000". The reading is built-up serially digit-by-digit. Using this technique, the -hp- 3480 is able to take up to 1000 readings/s with 4-digit resolution and $\pm 0.02\%$ full scale accuracy.

This technique is highly dependent on logic since it is the logic that must make the keep-or-reject decisions and keep track of what voltages were retained. It is the logic that transfers the final reading to the display. Accuracy depends mainly on the reference voltage and the resistive dividers used in the D-to-A converter. The clock rate (rate at which keep-or-reject decisions are made) does not effect the accuracy. Therefore, reading speed may be made as high as the switching speed within the D-to-A converter.

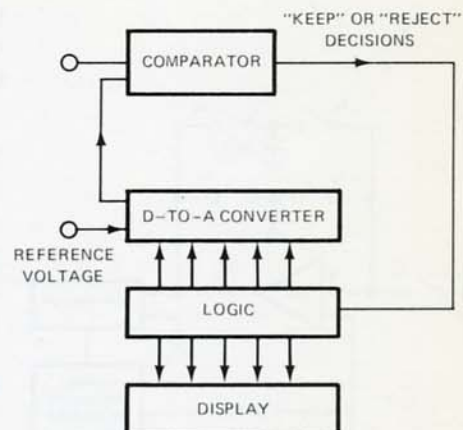


Figure 3-13.

A simplified block diagram of the successive approximation technique.

The -hp- 3480A or B is able to take up to 1000 readings per second with 4-digit resolution and $\pm 0.02\%$ 90 day accuracy. The 3480A/B uses the successive approximation technique for A-to-D conversion.



It is obvious that the input voltage must remain constant while these bits are tried, otherwise wrong voltages will be selected or rejected. Successive approximation has no inherent noise rejection and is therefore usually combined with filtering. Accuracy, however, is excellent relative to other A-to-D techniques.

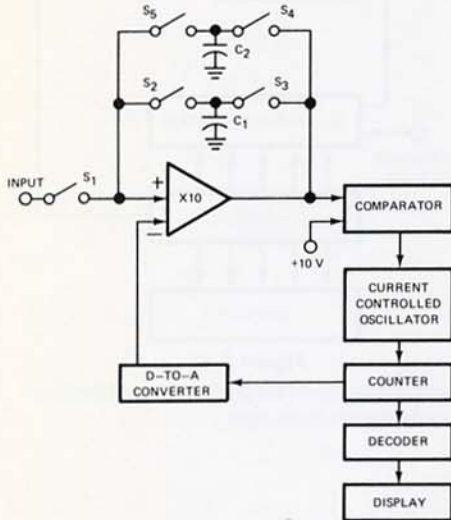


Figure 3-14.

A simplified block diagram of the recirculating remainder technique.

Another method of A-to-D conversion called the recirculating remainder technique (developed by the John Fluke Manufacturing Company) which is a simplification of successive approximation. The A-to-D converter has two basic operating modes. During the first mode, the most significant digit is determined. The last mode, the 4 least significant digits are measured.

Assume a voltage of 6.3524 volts is to be measured, Switch S_1 is closed and 6.3524 is applied to the X10 amplifier. This amplifier's output is clamped to 10 volts and turns-on the comparator/D-to-A circuit. The output of the D-to-A is summed with the input until the difference voltage is less than 1 volt. The output of the D-to-A is quantized in 1 volt steps. Therefore, with the D-to-A's output at 6 volts, and the unknown at 6.3524 volts, the input to the X10 amplifier is .3524 volts. The output of the X10 amplifier is 3.524 volts. This voltage level will turn the comparator off. Since the D-to-A converter's output is quantized to 1 volt, the counter has outputted 6 counts to both the D-to-A and the decoder/display. This ends the first mode and the most significant digit has been determined.

The second mode now starts, the name "recirculating-remainder" evolves because of the operation during this mode.

After the most significant digit has been determined, the output of the X10 amplifier is 3.524 volts. Switch S_1 is opened, and switch S_3 is closed. This allows C_1 to charge to 3.524 volts. Now Switch S_3 is open. Switches S_2 and S_4 are closed. This applies 3.524 volts to the input of the X10 amplifier. The most significant digit of this voltage (3) is now measured in the same manner as in the first mode when the "6" digit was determined. Note the D-to-A's output was reset to zero prior to making this measurement.

After the second most significant digit has been determined to be 3, the output of the X10 amplifier is 5.24 volts. The charge on C_2 is also 5.24 volts. Now the cycle can be repeated to determine the third most significant digit. The recirculation continues until all digits have been measured.

SUMMARY

There are many modifications of the A-to-D techniques covered in this section. They all fall into integrating or nonintegrating categories. The selection between these two main categories involve the differences shown below. Note that accuracy and resolution depend more on the specific technique used within these two categories.

| | INTEGRATING | NON-INTEGRATING |
|------------------------|------------------------------------|--|
| Speed | 15 to 50/s | up to 1000/s |
| Noise Rejection | Excellent at line frequencies | With filtering, good broad band rejection. |
| Accuracy | Depends on the specific technique. | |
| Resolution | Depends on the specific technique. | |

NOISE REJECTION

Noise is a serious problem for any measurement. Noise is an especially severe problem in DVM's due to their high accuracy, resolution and sensitivity. DVM's used in a system encounter noise problems more frequently than those used on the bench. Long signal leads and coupling between adjacent signal leads compound the problem in a system. Understanding the techniques used to protect a DVM from errors caused by noise is therefore, quite important.

Noise may be defined by its origin relative to the signal input lines on the DVM. Normal-mode noise enters **with** the signal and is superimposed on it. Common-mode noise is **common** to both the high and low signal inputs. Common-mode noise becomes normal-mode noise when it flows into the signal inputs.

NORMAL-MODE NOISE

Normal-mode noise originates from power line pickup, electromagnetic fields or even noise which originates within the device being measured. Noise can be sinusoidal, spikes, white noise, etc. If there is such a thing as typical noise, it might look like Figure 4-1. Here, a periodic ripple combined with noise spikes is superimposed on the dc signal. For a typical DVM, errors exceeding 100% could be caused by such noise unless the instrument is in some way, protected.

There are two techniques used to reduce normal-mode noise: integration and filtering. Integration makes a measurement over a fixed time interval during which amplitude variations are averaged out. If the integration period includes an integral number of periodic noise cycles, the noise will be completely averaged out.

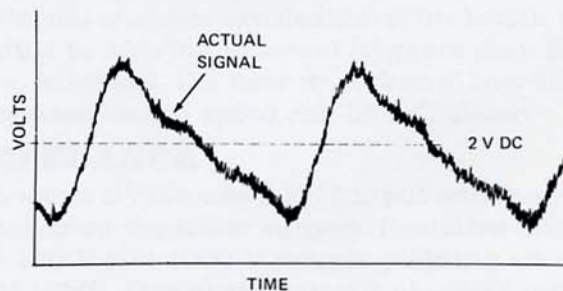


Figure 4-1. "Typical" periodic noise superimposed on a dc signal.

A DVM with a 1/60s integration period would average out one complete 60 Hz noise cycle, two complete 120 Hz cycles, four 240 Hz cycles, etc. In North America, the actual line frequency is subject to short-term frequency fluctuations, typically less than $\pm 0.15\%$. As shown in Figure 4-2, an integrating DVM with a 1/60s integration period achieves 56 dB of rejection for a 0.15% deviation from 60 Hz. This magnitude of rejection is more than adequate for most measurements.

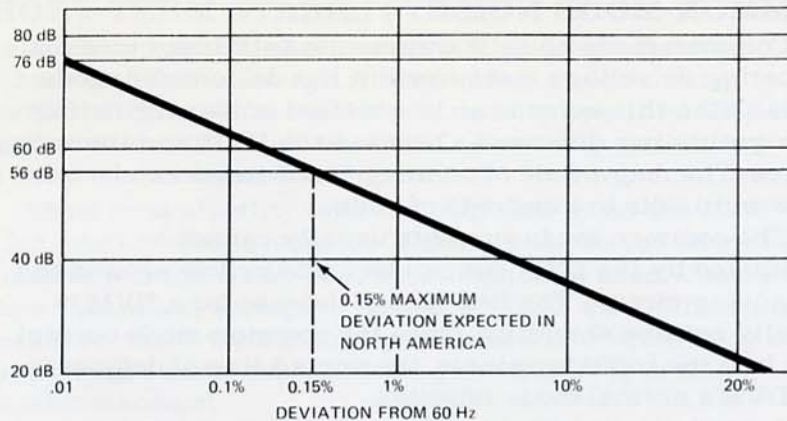


Figure 4-2. Noise rejection of an integrating DVM around 60 Hz.

DVM's using filtering to reject noise become progressively slower with increasing amounts of filtering. Quite often, different degrees of filtering are selectable, thus giving the user the flexibility of trading noise rejection for measurement speed. Below is an actual example of a successive approximation DVM (-hp- 3480A/B) with a three-position active filter:

| FILTER POSITION | 60 Hz REJECTION | READINGS/SECOND |
|-----------------|-----------------|-----------------|
| OUT | NONE | 1000/S |
| A | > 30 dB | 5/S |
| B | > 80 dB | 1/S |

The obvious question is which technique is better? It all depends on the type of noise expected by the user. Integration is better for rejecting line-related noise and filtering is better for broadband noise. The differences are shown in Figure 4-3 for two DVM's with almost identical characteristics except for the noise rejection technique. Both instruments had a reading speed of around 2 to 3 readings/s. Note that the integrating DVM has a 1/10s integration period with cusps at 10 Hz, 20 Hz, 30 Hz, etc. At 60 Hz, integration produces higher rejection but to either side of 60 Hz, filtering wins out. For the "typical" noise shown in Figure 4-1, part of the noise is periodic and part is random or non-line related. A combination of both techniques might work best in this situation.

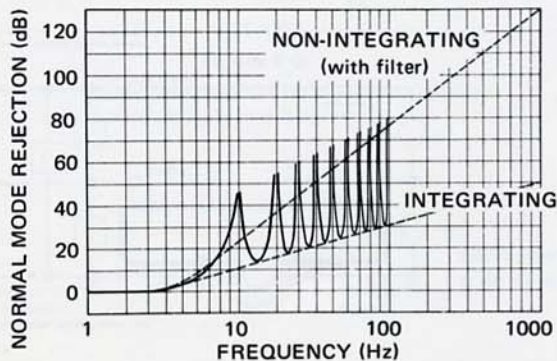


Figure 4-3. Normal mode noise rejection for two DVM's, one using filtering and the other using integration.

COMMON-MODE NOISE

Common-mode noise is common to both input terminals. A floating dc voltage measurement has dc common-mode noise. Often this noise is ac line-related noise originating from grounding differences between the DVM and the voltage source. The magnitude of common-mode noise can be from a few millivolts to hundreds of volts.

The common-mode currents usually cannot be eliminated by the DVM but can be made to flow around the measuring circuit. The first line of defense for a DVM is usually passive shielding. Once the common-mode current gets into the input terminals, the second line of defense is the DVM's normal-mode rejection.

A good place to start is with a simple grounded instrument as shown in Figure 4-4. Assume E_{in} is to be measured. R_a and R_b represent lead resistances. As long as the source ground at E_{in} equals the DVM's ground, no current will flow other than that caused by E_{in} .

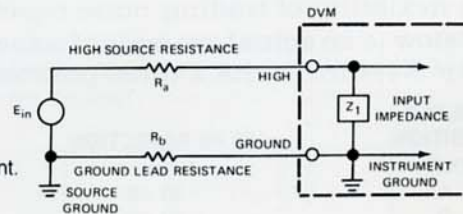


Figure 4-4. Simple grounded instrument.

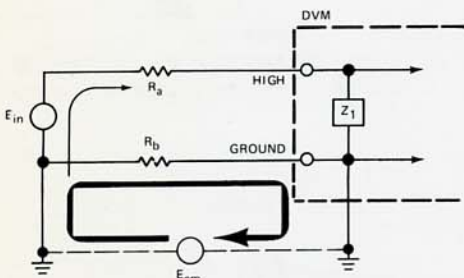


Figure 4-5.

A grounded measurement with a voltage difference between grounds.

Often, the grounds are unequal and a line-related noise signal appears. This case is illustrated in Figure 4-5 with E_{cm} representing a lumped source of a common-mode signal. Due to the DVM's high input resistance, Z_{in} , most of this common-mode current will flow through R_b and automatically appear as a part of the input signal. The only way the DVM can defend itself is by its normal-mode rejection. This type of DVM input is rare due to the fact that floating measurements cannot be made.

A floating input is shown in Figure 4-6. Floating measurements are possible since the low input terminal is isolated from ground. Now there are two potential sources of common-mode currents: one from grounding differences (E_{cm1}) and the other from a floating measurement (E_{cm2}).

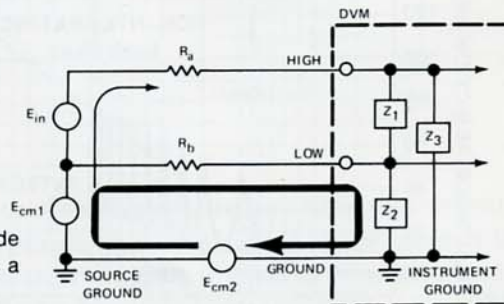


Figure 4-6. A floating measurement with common-mode voltage originating between grounds or as a floating measurement.

The floating DVM greatly reduces the errors due to common-mode currents because Z_2 is usually high. In other words, the instrument's low input is well isolated from the ground. Good instrument design will keep Z_1 and Z_3 higher than Z_2 . The majority of common-mode current will still flow through the low input lead resistance, R_b . This type of input is satisfactory for most bench type DVM's where measurements are made at the input terminals.

For DVM's used in a system, especially where resolution and sensitivity are important, the floating input may not yield enough common-mode noise rejection. This is especially true for transducer bridge measurements. Here the output level may be in the millivolts and source resistance may be high due to the legs of the transducer bridge. This brings up the topic of guarding which is a passive technique using an additional shield around the measuring circuit.

As shown in Figure 4-7, the guard effectively increases the impedance between the low input and ground. In addition, the guard is brought out to the front panel as an additional terminal. The resulting increase in the low-to-ground impedance (Z_2 and Z_3 in Figure 4-7) reduces the effect of common-mode currents. The real strength in guarding, however, comes from what the guard can do if properly connected to the circuit being measured.

Contrasting Figure 4-7 and Figure 4-8 show how the guard works. The situation shown in Figure 4-7 is similar to that of a floating input except the low-to-ground impedance is higher. The situation shown in Figure 4-8 shows the guard used to shunt away common-mode currents at the source. Here the current caused by E_{cm} is given a path through Z_3 which is the path of least resistance. The low input and guard are kept at about the same potential so little current flows through Z_2 .

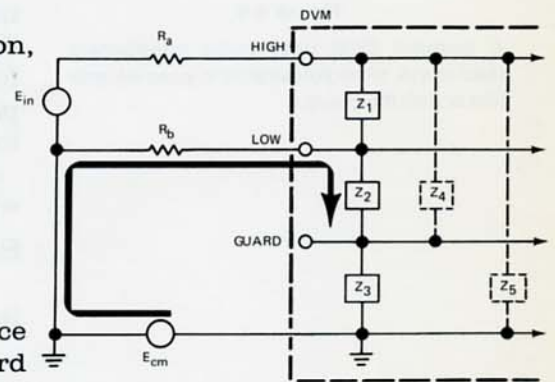


Figure 4-7.

A guarded instrument splits the low-to-ground impedance through the addition of a guard shield.

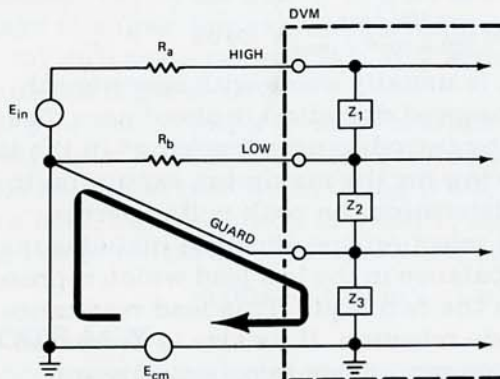
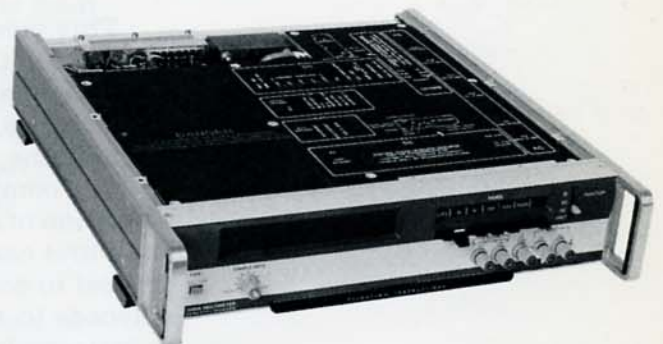


Figure 4-8.

A guarded instrument with the guard connected such that it shunts common-mode currents away from the inputs.



The -hp- 3490A DVM with the top cover removed to show the guard shield. The guard shield is brought out to the front panel (center terminal). The guard is isolated from the chassis as well as the measuring circuits.

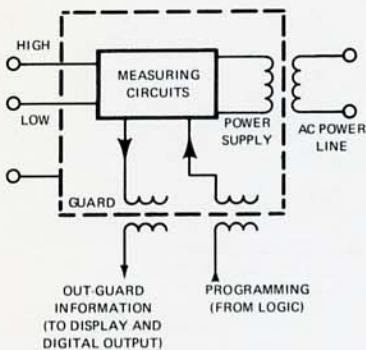


Figure 4-9.

A guarded DVM uses pulse transformers, reed relays, or photo-isolators to pass information across the guard.

For best results, the guard terminal should **always be used**. Here are two rules for connecting the guard:

1. Connect the guard so that it and the low terminal are at the same voltage or as close to the same voltage as possible.
2. Connect the guard so that no common-mode current or guard current flows through any resistance that is across the input terminals (especially the low source resistance).

Physically, the guard is nothing more than a sheet metal box surrounding the measuring circuits. The guard is, in turn, surrounded by the outer chassis of the DVM. The guard shield often passes through the windings of the power transformer. Information generated "in-guard" must be passed to "out-guard" in a manner which maintains isolation. The flow of information is usually carried on via pulse transformers, reed relays, or photo-isolators as shown in Figure 4-9. Sometimes, the pulse transformer is time shared for a two-way flow of information. Sometimes the reading is passed serially and reconstructed on the out-guard side to reduce the number of pulse transformers.

NOTE: Refer to Appendix II for a discussion of guarding which includes power transformer shielding.

SPECIFICATIONS

Rejection of either normal-mode or common-mode noise is specified in terms of a dB voltage ratio as shown below:

$$dB = 20 \log \frac{\text{noise voltage}}{\text{voltage error}}$$

Both the numerator and the denominator must be measured the same way. For example, if a 10V **peak** noise signal is applied to a DVM and its readout deviates 100 μV **peak**, then the noise rejection equals 100 dB. The calculation is as follows:

$$20 \log \frac{10\text{V peak}}{100 \times 10^{-6} \text{V peak}} = 100 \text{ dB}$$

This measurement is usually made with zero signal input such that any observed deviation is about zero. The noise affects the DVM by introducing a "racking" in the last digit or digits. By looking for the maximum excursion in the display, the user can determine the peak voltage error.

The common-mode rejection specification includes the condition of a 1 K Ω unbalance in the **low** lead which represents the worst case between the two leads. This lead resistance is critical to common-mode rejection. If its size is decreased by a decade to 100 Ω , the common-mode rejection appears to improve by 20 dB.

There are really two types of common-mode rejection (CMR). The ratio in dB of the common-mode signal to the normal-mode signal it produces is "pure" CMR and results strictly from shielding or guarding. The "effective" CMR is a combination of "pure" CMR and NMR. The "effective" CMR is the effect on the reading and is a more popular way of specifying CMR. It is often possible to numerically add "pure" CMR to NMR and derive "effective" CMR as shown in Figure 4-10.

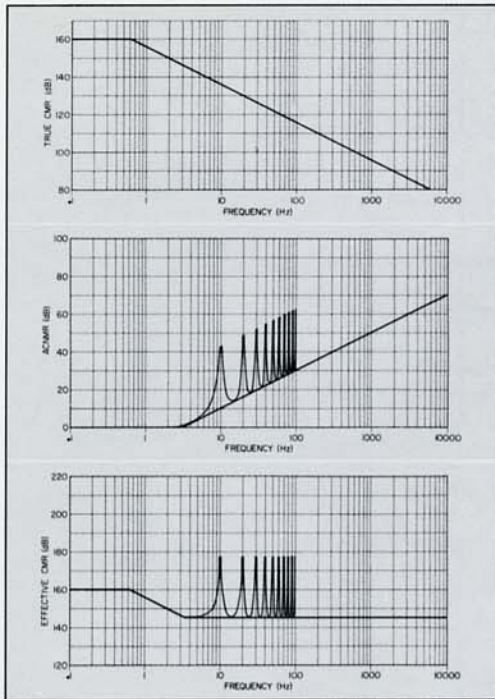


Figure 4-10. The relationship between "pure" CMR, NMR and "effective" CMR.

EXAMPLE OF USING THE GUARD

It is not enough to know the basic rules of connecting the guard. An example is valuable in illustrating some actual situations involved in using the guard. The presence of a guard terminal almost obligates the user to connect it somewhere.

Shown in Figure 4-11 are three ways to connect the guard. The device being measured is assumed to be a floating dc power supply. This power supply has low source resistance. Lead resistances R_a and R_b compose essentially all of the source resistance.

The top connection is the best connection. The guard is at practically the same potential as the low input terminal. No common-mode current passes through R_a or R_b . There are other ways to connect the guard, however.

In the middle example (Figure 4-11), the shorting bar provided with most DVM's is used to short guard to low. This is the easiest connection and might very well be the most commonly used one. Low and guard are definitely at the same potential. The problem is that all of the common-mode current flows through R_b . What is dropped across R_b becomes part of the input signal and must be rejected by the DVM as a normal-mode signal. Also, Z_2 is shorted out and the low-to-ground impedance is lower allowing more common-mode current to flow. In a system where leads are long, the value of R_b becomes more significant. This, then, is not a good way to connect the guard.

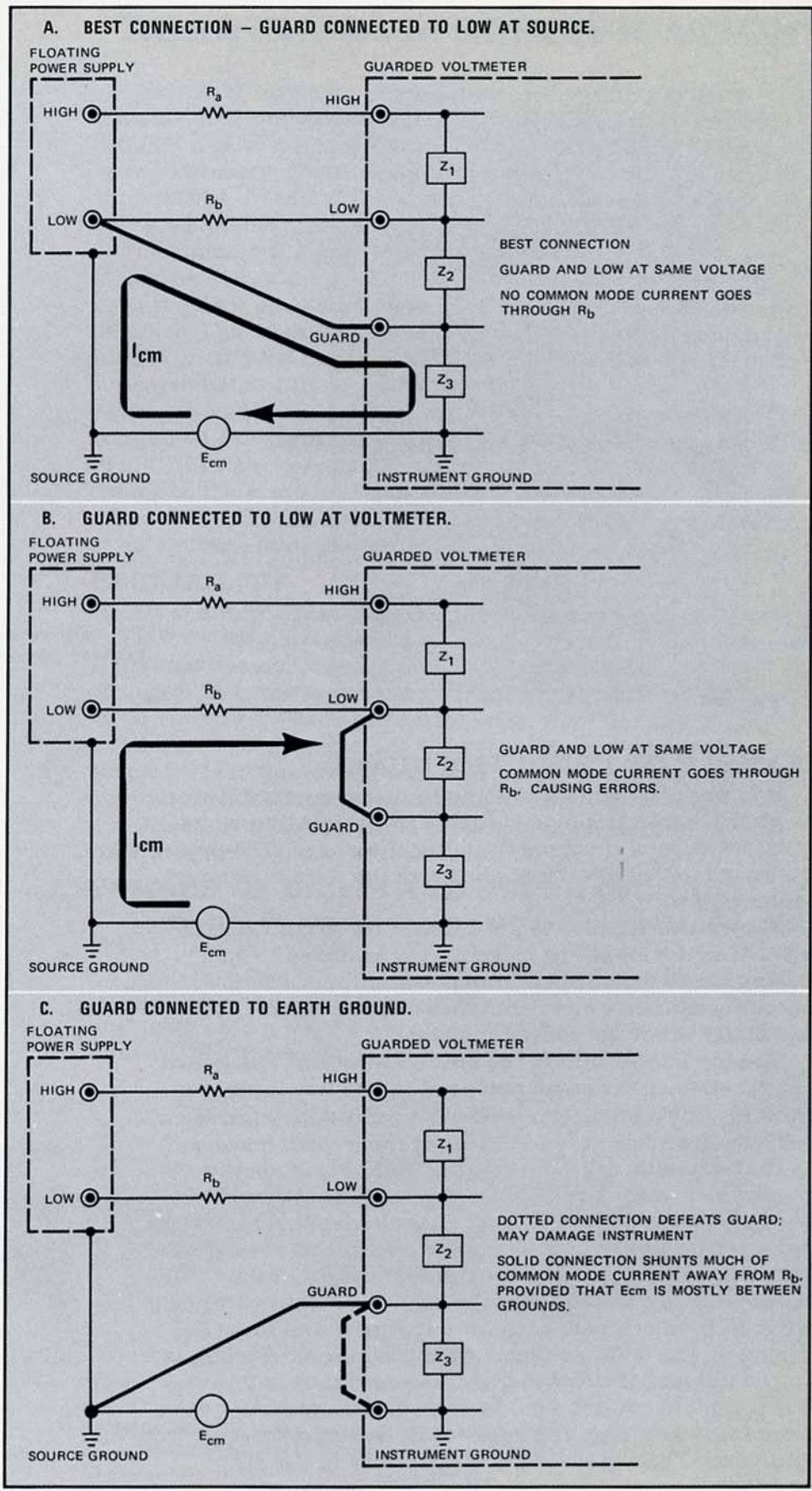


Figure 4-11. Various ways to connect the guard to a floating power supply.

FIGURE 7. Connecting the Guard

The lower example actually illustrates two connections. The solid line shows the guard connected at the source's ground. This can be a good connection. It does shunt away common-mode currents originating between the grounds. Guard and low may not end up at the same potential, however. Common-mode currents originating within the source would not be shunted away from R_b . The breakdown voltage on most DVM's between guard and low is usually a lot less than between guard and chassis. This may impose a limitation on the measurement.

The dotted line in the lower figure shows the guard shorted to chassis. Again, the impedance between low and ground is reduced by shorting Z_3 .

There is another alternative—leave the guard open. Just about **any** connection is better than this one. Any connection which diverts any amount of common-mode current away from R_a or R_b is better. The instrument can also be damaged. The values of Z_2 and Z_3 are usually unequal and if a floating measurement is made, the guard will seek its own division ratio. A 500 V floating measurement could easily cause the guard to float to over 200 V between it and low. This would result in damage to many DVM's. A typical maximum input voltage specification would appear as follows:

Guard-to-Chassis: ± 500 V peak

Guard-to-Low: ± 200 V peak

High-to-Low: ± 1200 V peak

There are many more considerations when using a guarded instrument. The ideal point to connect the guard is not always physically available. Refer to Floating Measurements and Guarding (Application Note 123) for more details.

SIGNAL CONDITIONERS AND CONVERTERS

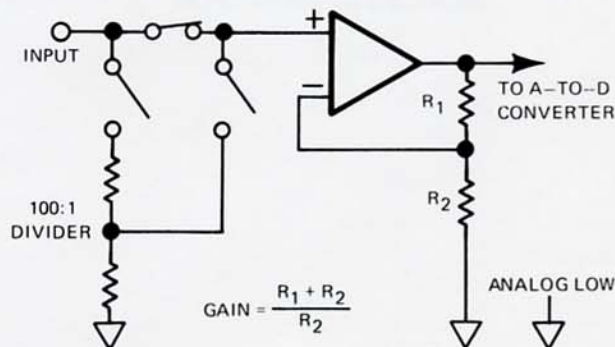
Of all the parts of a DVM, the signal conditioning and conversion has the greatest influence on the instrument's characteristics. As covered in a prior section, the A-to-D converter measures over only one range of dc voltage and usually has relatively low input resistance. To make a DVM useful, a "front end" is required to precede the A-to-D converter. A dc signal conditioner increases input resistance, amplifies small signals and attenuates large ones to give the DVM a selection of ranges. Converters are designed to change ac voltage or resistance to dc voltage.

DC INPUT AMPLIFIER/ATTENUATOR

The signal conditioning for dc must include both amplification and attenuation. These functions are carried out in what could be called an amplifier/attenuator. If the full scale input to the A-to-D converter is 10V, the dc input amplifier/attenuator would amplify the 100 mV and 1 V ranges and attenuate the 100 V and 1000 V ranges. The 10 V range is virtually straight through but buffered with a unity gain amplifier for an increase in input resistance.

Figure 5-1 shows the typical configuration for the dc input amplifier/attenuator. Gains are selected by precision resistors in the feedback loop. On the higher ranges, a resistive divider is used. For example, on the 1000 V range, the divider divides by 100 and the gain is set to X1. For the 100 V range, the voltage is divided by 100 then amplified by X10. By changing R_1 and R_2 , the gain may be set to X1, X10 or X100.

On the upper ranges, the divider controls the input resistance. Most DVMs have a 10 M Ω input resistance on the 100 V and 1000 V ranges. On the lower ranges, the use of a FET input stage on the amplifier yields input resistances up to > 10¹⁰ Ω . (For more details on the construction of a FET input stage, see Appendix IV.)



$$\text{GAIN} = \frac{R_1 + R_2}{R_2}$$

| GAIN | VALUE OR R_1 AND R_2 |
|------|---|
| X1 | $R_1 = 0$ $R_2 = 100 \text{ k}\Omega$ |
| X10 | $R_1 = 90 \text{ k}\Omega$ $R_2 = 10 \text{ k}\Omega$ |
| X100 | $R_1 = 99 \text{ k}\Omega$ $R_2 = 1 \text{ k}\Omega$ |

Figure 5-1. A typical dc input amplifier for a DVM combined with an attenuator for the higher voltage ranges. The input switches are used to switch in the 100:1 divider. Other switches (not shown) change the value of R_1 and R_2 .

One weakness of a dc input amplifier is its offset. This affects its accuracy and its ability to read around zero volts. An auto-zero circuit is commonly employed to overcome this problem. By using a scheme like the one shown in Figure 5-2, offsets are measured, stored and then cancelled. This technique uses the fact that the input amplifier is used only part of the time. While not in use, auto zeroing takes place. The input is shorted to ground by switch S_2 . Switch S_1 opens the DVM's input so that the user's circuit isn't shorted. Any offset is stored on the capacitor relative to ground.

When the amplifier is in use as shown in the lower diagram, switch S_5 and S_3 are opened. The capacitor holding the offset voltage is introduced in series with the feedback loop but in opposite polarity. The capacitor acts like a battery which nulls out the offset voltage. This technique often eliminates the classical zero pot used for calibration. Auto zero circuits are also used in a DVM's integrator to zero the integrating amplifier.

As has been pointed out, FET's are often used as the input stage in the dc amplifier to provide high input resistance. FET's create a problem of their own, however, in the form of injected dc leakage current. Typically, this current is <10 pA but usually increases at higher temperatures. All the user needs to know is that the current is there and that it may affect a measurement where the source resistance is very high. For example, if the source resistance were 10 M Ω , which would be quite unusual, a 10 pA leakage current would produce an offset of 100 μ V. If the 1 V range on a 4-digit DVM were being used, its last digit sensitivity equals 100 μ V. The 10 pA leakage current would produce a 1-digit error in the reading.

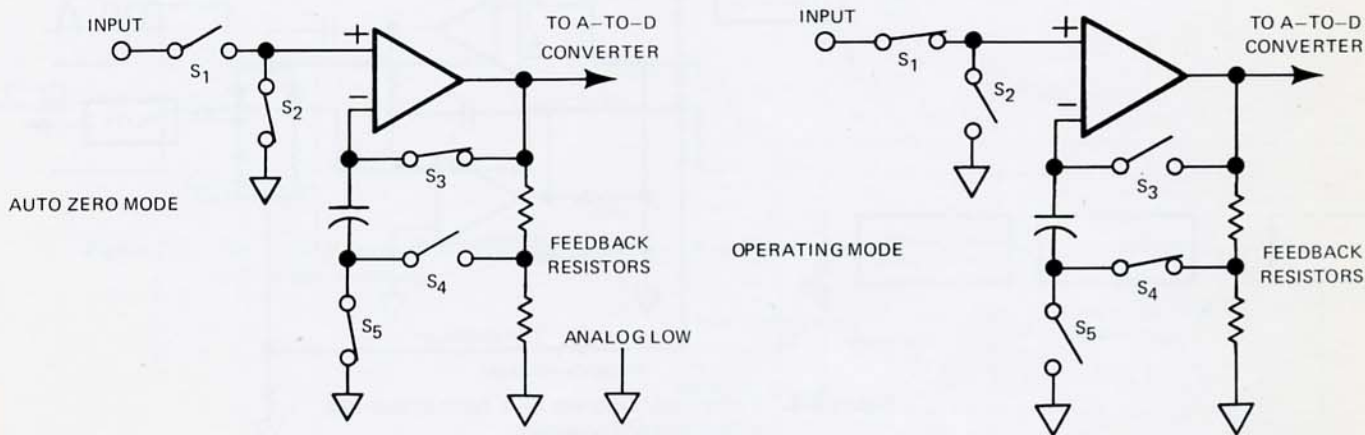


Figure 5-2. Auto zero circuit in the dc input amplifier.

AC CONVERTERS

The dc input amplifier/attenuator rarely enters into a purchase decision since most DVM's use about the same scheme. This is not true, however, for ac converters. There are vast differences between average responding converters and true rms converters.

The main purpose of an ac converter is to change an incoming ac voltage into a dc voltage. An ideal ac converter measures the rms value of the incoming signal and converts it to its equivalent dc voltage. In the process, it takes the square root of the sum of the squares of all of the components of the ac signal.

One approach is to take the average value of the input signal using a simple diode bridge as shown in Figure 5-3. These converters are simple to design, are relatively inexpensive and are used in the majority of DVM's being manufactured. The output from the diode bridge is a half-wave rectified signal which is sent to a filter. The output from the filter is a dc voltage proportional to the average value of the input signal. Gain control is provided by ac feedback. The dc feedback includes an amplifier/integrator to stabilize the converter.

Average responding converters are usually limited in bandwidth to 100 kHz with some going as high as 250 kHz. On the low end, few converters go below 45 Hz. The problem is that the diodes approximate rms response only over a certain range. At high frequencies, the diodes start to become capacitive. On the low end, it is difficult to filter out the low frequency ripple.

Average responding converters measure the average value of a sine wave multiplied by a scale factor. The scale factor yields a readout equal to the rms value:

$$\text{Scale Factor} = \frac{V_{\text{rms}}}{V_{\text{AVR}}} = \frac{0.707 V_{\text{max}}}{0.637 V_{\text{max}}} = 1.11$$

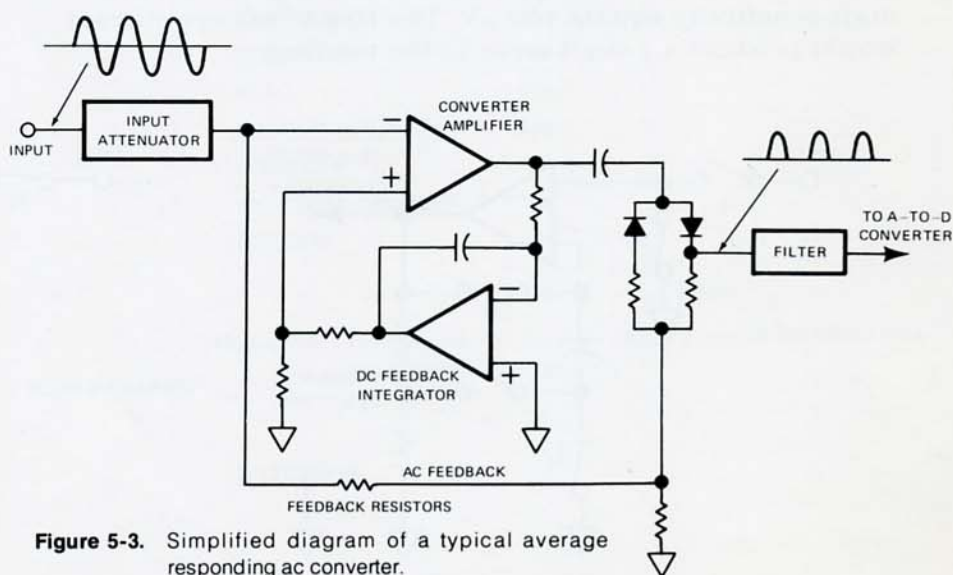


Figure 5-3. Simplified diagram of a typical average responding ac converter.

The catch is that this scale factor is different for each wave shape. In other words, a sine wave with a little distortion might require a different scale factor. The scale factor varies with the phase angle of the distortion. This means that average responding converters are designed strictly for measuring **pure sine waves**.

To give an idea of just how bad errors can be for sine waves with distortion, Figure 5-4 shows a plot of error resulting from 1% odd harmonic distortion. Note that as the phase angle of the distortion changes, the error changes. The same information is shown in Figure 5-5 for distortion as a function of amplitude. By looking at either of these two figures, it is obvious that even small amounts of odd harmonic distortion can cause large errors in the reading of an average responding ac converter.

Even harmonics are usually not a problem. Errors produced by even harmonics remain below $\pm 0.5\%$ even if the harmonic content is 10%. Even harmonics add as much to a rectified waveform as they subtract over the period of the fundamental. Odd harmonics add an extra half cycle to each rectified waveform. (Refer to Appendix V.)

Function generators are popular as signal sources. Typically, distortion is listed as 40 dB below the fundamental. If all of the distortion were concentrated in the 3rd harmonic, the error would be $\pm 0.33\%$. On a 4-digit DVM, this error would equal 33 counts **additive** to the instrument's basic accuracy. Although not listed on the data sheet for a function generator, the harmonics are both odd and even. The even harmonics cause little error. Typically, a user could expect 20 to 25 counts of error on a 4-digit DVM used to measure the output of a function generator.

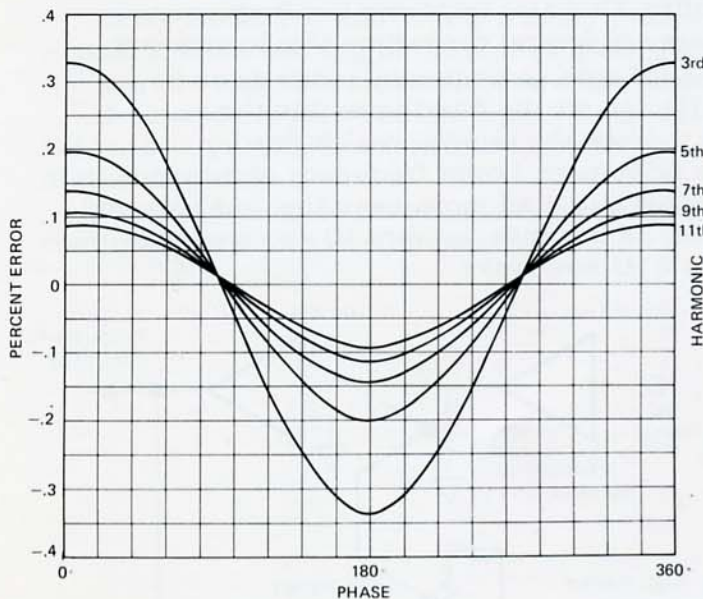


Figure 5-4. Percent Error versus Phase. Each harmonic is 1% of the fundamental magnitude.

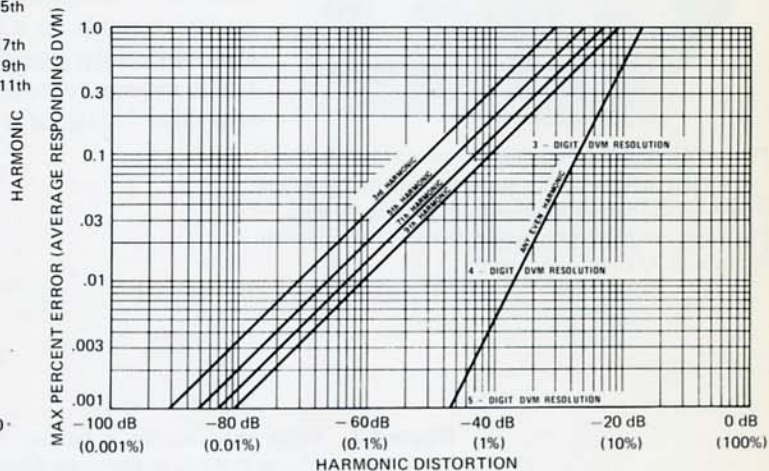


Figure 5-5. Maximum % Error Versus Harmonic Magnitude. Harmonic phase is constant.

As this example illustrates, pure sine waves are rare even from signal sources. Think what happens when the output from a signal source is passed through some circuit being tested. In addition, there are many nonsinusoids such as triangle waves, square waves, pulses, etc. whose amplitudes are of interest.

The second type of ac converter overcomes these limitations but at extra cost. The true rms converter responds to the dc heating value of the input signal. The signal is applied to a heater element as shown in Figure 5-6. The temperature of the heater element is measured by a bimetallic junction or thermocouple. The thermocouple is in close thermal proximity to the heater. By thermocouple action, the dc voltage produced at the junction is proportional to the heat generated by the input signal.

Thermocouples are nonlinear with input signal amplitude. Thermocouples also respond to changes in ambient temperature as well as the input signal. By operating a second matched thermocouple in opposition as shown in Figure 5-7, the output from the converter can be made linear and self-correcting for ambient temperature changes.

The sensitivity of a single thermocouple can be improved by adding more junctions in series but all in proximity to the same heater element. This is called a thermopile. Thermopiles are manufactured by using thin film technology which reduces thermal inertia and improves response time. Matched pairs may be deposited on one substrate at the same time. Thermopiles with as many as 30 junctions have been manufactured with about 30 times the sensitivity of a thermocouple.

The ability to measure not only the ac component of a signal but the dc component as well may be added using a dc coupled amplifier. This also improves low frequency performance. There are several converters able to measure $\sqrt{(\text{true rms ac})^2 + (\text{dc})^2}$ with ac frequency range down to 2 Hz. Between 2 Hz and dc, the filtering within the ac converter begins to track the input signal instead of converting it to a dc voltage. Lower frequency response is theoretically possible but at an increase in the time required for a measurement. As it stands, it takes 10 s to measure the rms value of a 2 Hz sine wave.

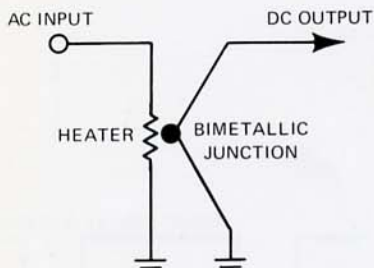


Figure 5-6.

A simplified diagram of a thermocouple/heater combination used for true rms ac conversion.



The 3484A Multifunction unit for the 3480A/B DVM uses a thermopile true rms ac converter. This gives this plug-in an ac frequency range from 1 Hz to 10 MHz. The input can be direct coupled to allow the converter to measure $\sqrt{(\text{dc})^2 + (\text{ac rms})^2}$.

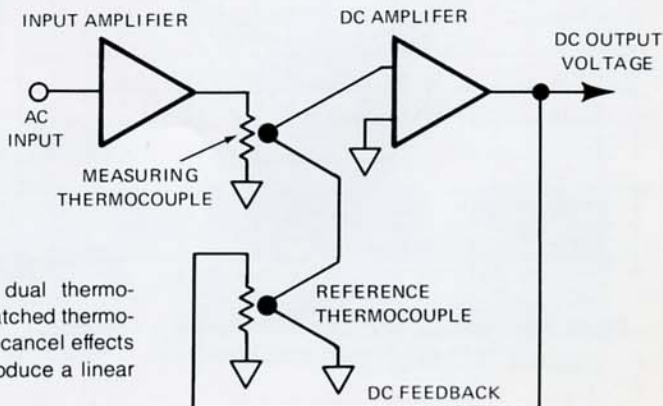
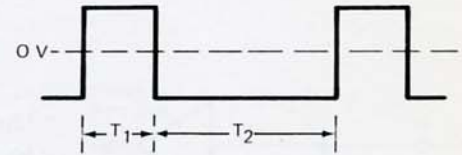


Figure 5-7. Block diagram for a typical dual thermocouple true rms ac converter. Matched thermocouples operated in opposition cancel effects of ambient temperature and produce a linear output.

Thermocouple and thermopiles are square law devices. Their output decreases much more rapidly than the input voltage. For this reason, true rms converters are not specified for operation below 1/10 full scale. When the input is shorted, a true rms converter may appear to have an offset. This is really internal noise which is being amplified.

A figure of merit called crest factor is generally used to tell the user how much of a pulse can be measured. Crest factor is defined as the peak value divided by the rms value or in terms of duty cycle:



$$\text{CREST FACTOR} = \frac{V_{\text{peak}}}{V_{\text{rms}}} = \sqrt{\frac{1-D}{D}}$$

$$D = \text{DUTY CYCLE} = \frac{T_1}{T_1 + T_2}$$



The -hp- 3403C uses a thermopile to make true rms measurements from 2 Hz to 100 MHz. This 3-digit DVM has ac ranges from 10 mV full scale to 1000 V full scale. AC accuracy equals $\pm 0.4\%$ mid-band for 90 days. Crest factor equals 10:1 at frequencies > 25 Hz.

Crest factors as high as 10:1 are available in true rms converters. Incidentally, the crest factor of a sine wave is 1.414 and applies to all average responding converters.

In summary, true rms converters are superior in every aspect to average responding converters but they cost more. True rms converters have wider bandwidth, ac plus dc, ability to measure nonsinusoids, better accuracy and are insensitive to distortion. As far as speed is concerned, true rms converters can be designed to be as fast or faster than average responding converters.

At this point, it should be mentioned that there is a third type of ac converter known as a quasi-rms converter. This type of converter holds a lot of promise but is not as widely used as the average responding or the true rms responding converters. The quasi-rms technique simulates true rms response using operational amplifiers to square the input, take the average of the square, then take the square root. In other words, the mathematical functions performed by a true rms converter are simulated. A diode shaping network is used to gain the square law response. A filter is used to compute the average value of the input signal.

This synthesized rms response is not mathematically perfect and, for that reason, is limited to symmetrical wave shapes. Square waves, triangle waves and sine waves with up to 3% distortion can be measured in a true rms fashion. The quasi-rms converter falls into midground between true rms and average conversion techniques.

OHMS CONVERTERS

The easiest way to measure the value of a resistor with a DVM is to supply a constant current to the resistor. By using the existing dc circuits, the voltage measured is proportional to the value of the unknown resistor. By selecting the right current, the reading is scaled to read directly in ohms.

$$RI = E$$

if I is constant,
then $E \propto R$

The same input terminals are often used to measure the voltage dropped across the unknown resistor as are used to supply the current as shown in Figure 5-8. This 2-wire technique is widely used for bench DVM's where the measurement is made right at the front panel.

In a system, lead resistance becomes a factor especially on the lower ohms ranges. A 6ft lead alone can add 60 mΩ of resistance. On a 100 Ω full scale 5-digit measurement, 60 mΩ equals a 60 count error. The 4-wire ohms converter has become quite common for solving this problem. This type of converter senses the voltage dropped just across the unknown resistor. The drop through the lead resistance is excluded from the measurement. A diagram is shown in Figure 5-9.

The way a 4-wire ohms converter works is by using a dc constant current source totally isolated from the rest of the measuring circuits. The high and low input leads carry virtually no current due to the high input resistance of the dc amplifier. This scheme eliminates errors due to lead resistance in either the current supply leads or the measurement leads.

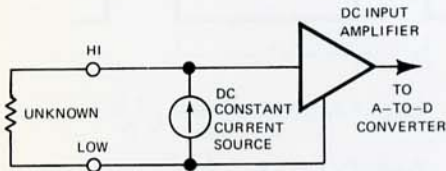


Figure 5-8. Simple 2-wire ohms converter.

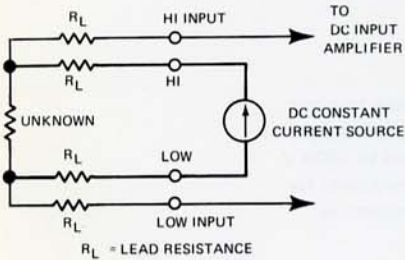


Figure 5-9.

Simplified 4-wire ohms converter used to eliminate lead resistance errors. Current is supplied by a separate current source.



The -hp- 3470 Measurement System is designed for bench use and has a 2-wire ohms converter using separate input terminals (on the right hand side). The 3470 also includes an average responding ac converter with a frequency range from 45 Hz to 100 kHz.

The 4-wire converter costs more than the 2-wire converter due mainly to the independent dc current source needed. In summary, the 4-wire converter is better for systems use and the 2-wire converter is more economical for bench use where lead lengths are short. (Refer to Appendix VI for operating theory.)

RATIO

Some measurements are easier when made as a ratio. A good example is checking a resistive divider as the ratio of one resistor against another. By making an AC/AC ratio measurement, the effective turns ratio of a transformer can be measured.

There are two types of ratio inputs for a DVM: three-terminal and four-terminal. Due to cost, the three-terminal input with a common leg is more popular. The four-terminal input is more versatile, however, and can measure two floating voltages with no common point. The choice depends on the application.

There are other important considerations involved in selecting a ratio measuring DVM. The numerator or X input usually is the normal dc input. The denominator or Y input is substituted for the DVM's internal reference voltage. The X input has the same ranges as the DVM but the Y input is often slighted. It may be limited to something like $10V \pm 10\%$. Some DVMs have a Y input with ranges like 100 mV full scale to 100 V full scale. If the Y input does have ranges, it should also be autoranging, otherwise, the user must seek the correct range on both X and Y inputs. The Y input may also not have as high an input resistance as the X input. In summary, the user should check the characteristics of both inputs before purchasing a ratio measuring DVM. (Refer to Appendix III for more details on three-terminal vs. four-terminal ratio measurements.)



The -hp- 3490 DVM is designed for bench or systems use and has a 4-wire ohms converter. Errors due to lead resistance may be eliminated if the terminals are properly connected.

SCANNING

Multiple inputs are quite valuable in many DVM applications. Scanners used as signal conditioners are still fairly uncommon among commercially available DVM's.

Scanners or multiplexers fall into mechanical types and solid state types. Mechanical scanners use reed relays or stepping switches and can handle a wide range of input voltage. Speed is limited to around 40 channels per second. Mechanical scanners are prone to wear.

Solid state scanners or multiplexers use FET switches which don't wear out. Speeds up to thousands of channels per second are possible. FET switches are limited to input levels below 50 Vdc and have a similar limit on the ability to float. This, in turn, limits common-mode voltages. Cross-talk may also be a problem due to difficulties in isolating the FET drive lines.

There are many advantages of building a scanner into the DVM. As shown in Figure 5-10, the scanner and the DVM are under one logic control. Scanning speeds may be regulated within the instrument to allow for autoranging, settling and digitizing time. The scanner can trigger the A-to-D converter internally. Interfacing is simplified. The cost is lower due to sharing of the power supply, cabinet and logic.

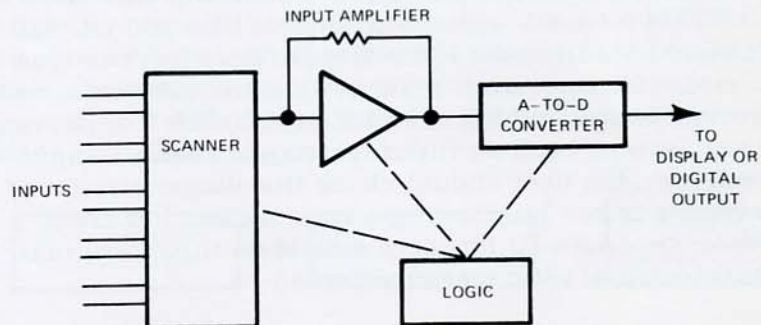
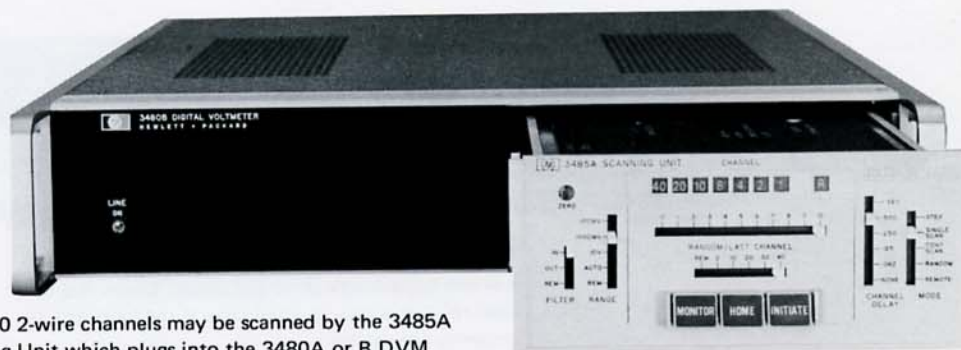


Figure 5-10. Scanning is a valuable form of signal conditioning for a DVM. Combining a scanner and DVM simplifies interfacing.



Up to 50 2-wire channels may be scanned by the 3485A Scanning Unit which plugs into the 3480A or B DVM. This scanner uses FET switches and is able to scan and read at up to 1000 channels per second. In addition, this scanner includes 100 mV, 1 V and 10 V dc ranges complete with autoranging.

SAMPLE ANSWERS

1. The first part of the question asks for the definition of a function. A function is a set of ordered pairs where each first element is associated with exactly one second element. The second part of the question asks for an example of a function. A simple example is the function $f(x) = x^2$, which maps every real number to its square.

2. The first part of the question asks for the domain and range of the function $f(x) = \sqrt{x}$. The domain is the set of non-negative real numbers, $[0, \infty)$, and the range is the set of non-negative real numbers, $[0, \infty)$. The second part of the question asks for the graph of the function. The graph is a curve in the first quadrant that starts at the origin $(0, 0)$ and increases as x increases.

3. The first part of the question asks for the domain and range of the function $f(x) = \frac{1}{x}$. The domain is the set of non-zero real numbers, $(-\infty, 0) \cup (0, \infty)$, and the range is the set of non-zero real numbers, $(-\infty, 0) \cup (0, \infty)$. The second part of the question asks for the graph of the function. The graph consists of two hyperbolic branches, one in the first quadrant and one in the third quadrant, with the x-axis and y-axis as asymptotes.



Figure 1: A flow diagram showing three rectangular boxes connected by arrows. The first box is on the left, the second in the middle, and the third on the right. An arrow points from the first box to the second, and another arrow points from the second box to the third.

SAMPLE-AND-HOLD

DVM's offer advantages over other instruments in resolution and accuracy. DVM's are designed to measure dc voltage, ac voltage, resistance, etc., but not the instantaneous value of a changing voltage. Sample-and-hold expands a DVM's usefulness by freezing a changing input voltage then measuring it with little degradation in resolution or accuracy. With appropriate triggering, applications include peak measurements, digitizing a wave shape or possibly checking the linearity of a ramp.

As has been discussed previously, in the dc mode of operation any change in the input during digitization is considered noise. This prevents a DVM from being used to digitize a changing voltage. For example, a typical 4-digit DVM using successive approximation is able to digitize a change of only 10% of range per second. On the 10 V range, this means that the input cannot change faster than 1 V/s. By adding sample-and-hold to this same DVM, this figure can be improved to 10% of range per **micro-second**. Now this DVM can be used to digitize low frequency wave shapes retaining its resolution and accuracy.

Figure 6-1 shows where sample-and-hold is located within a DVM. It follows the input amplifier/attenuator and is immediately ahead of the A-to-D converter. Due to its location, the sample-and-hold unit assumes the ranges, input resistance, and other characteristics of the input amplifier/attenuator. Sample-and-hold does not change the DVM's accuracy, resolution or speed.



Figure 6-1. Sample-and-hold is located before the A-to-D converter but following the input amplifier/attenuator.

To better illustrate the operation of sample-and-hold, it helps to look at the waveform fed to the A-to-D converter. Figure 6-2 shows what this waveform looks like for one sample taken on the positive half of a sine wave. The sample-and-hold unit freezes the waveform when triggered. After digitization is complete, the output of the sample-and-hold unit is released automatically and tracking resumes. Note that the A-to-D converter always looks at a dc voltage when it is digitizing. The reading equals the instantaneous value of the sine wave at the moment the sample-and-hold unit responds to a trigger.

In some situations, a delay must be used to slow the trigger to the sample-and-hold unit. The response time of the input amplifier/attenuator is many times longer than for the sample-and-hold unit. There is a danger in sampling too early before the input amplifier/attenuator has had time to settle. This is especially true for step inputs.

Most DVM's equipped with sample-and-hold have a switchable delay illustrated in Figure 6-3. This delay holds off sampling until the input has settled. The delay is not needed if the wave shape is continuous or if the user delays the trigger. The delay is used for pulses, square waves and step inputs where triggering takes place along the leading edge.

There are three basic ways to use sample-and-hold: (1) If the DVM has a high enough reading speed, entire low frequency waveforms may be digitized. (2) If the wave shape is repetitive, a series of samples evenly offset in time may be taken on successive cycles. (3) Synchronized sampling may be used to take readings at a specific point on a repetitive wave shape.

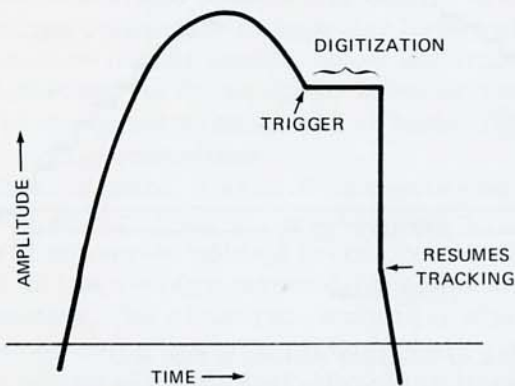


Figure 6-2. The output from a sample-and-hold unit used in a DVM freezes the input voltage during digitization then releases it to resume tracking.

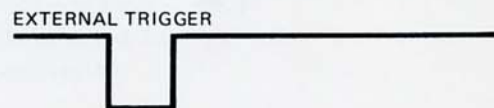
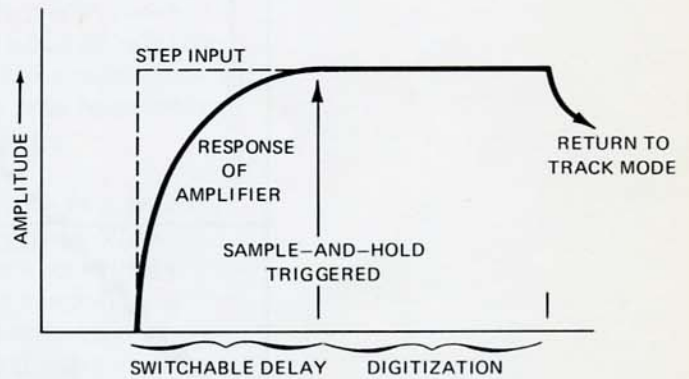


Figure 6-3. Sample-and-hold units usually include a switchable delay to allow the input amplifier/attenuator to settle to final value. The delay is used for step inputs.

Figure 6-4 shows the digitization of an entire wave shape using a DVM able to take 1000 readings/s. Each plateau represents a complete reading. The wave shape need not be repetitive. Applications include transient analysis, mechanical vibration, low frequency waveform analysis, and many more.

If the wave shape is repetitive, then the DVM does not have to have such a high reading rate and samples may be taken on successive cycles. Each sample is offset in time thus an entire wave shape may be digitized as shown in Figure 6-5.

One of the most useful ways to employ sample-and-hold involves synchronous sampling. Specific parts of a repetitive wave shape may be investigated. For example, accurate peak readings may be taken or the flatness of the top of a square wave may be measured. Ramp linearity may be determined.

The simplest way to synchronize the DVM's trigger to the wave shape is to use an oscilloscope equipped with a delayed sweep. The oscilloscope usually has an output pulse marking the beginning of the delayed sweep. The delay is variable using a front panel control. The setup is shown in Figure 6-6.

The delay may be walked along the wave shape to the point where the measurement is to be made. The DVM's reading is continuously updated by the trigger pulse issued by the oscilloscope. The delay sweep control is usually a multiturn pot with a great deal of time resolution. This setup allows precise readings to be taken either offset in time or at any given point on the wave shape.

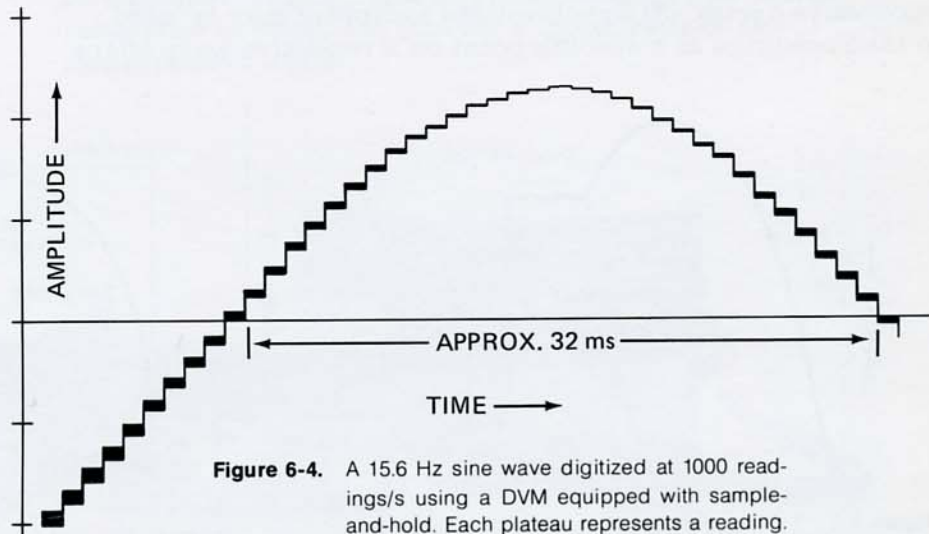
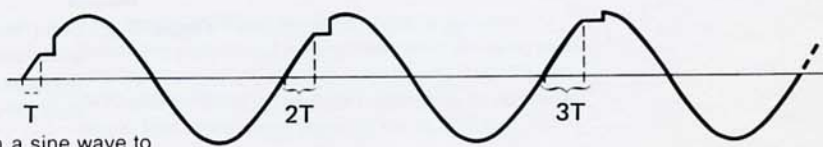


Figure 6-5. Successive samples taken on a sine wave to digitize it. Each sample is offset in time by T . This technique may be used to digitize any repetitive signal.



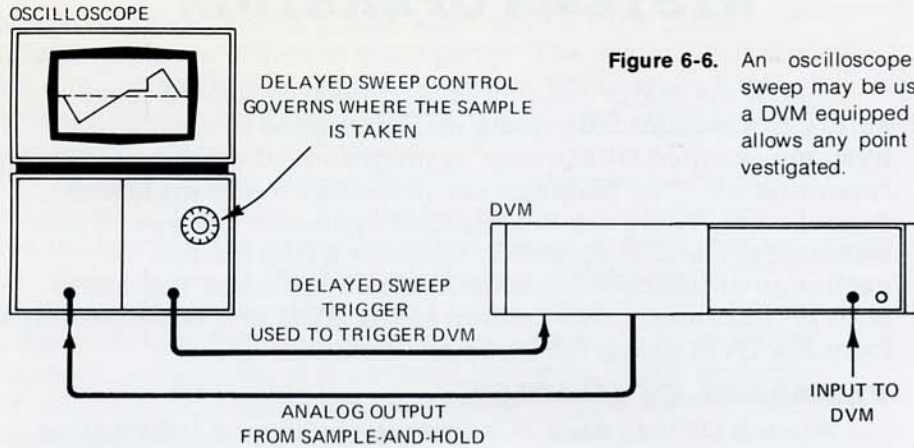


Figure 6-6. An oscilloscope equipped with delayed sweep may be used to synchronously trigger a DVM equipped with sample-and-hold. This allows any point on the waveform to be investigated.

At this point, it is helpful to go into some of the terminology associated with sample-and-hold. When sample-and-hold is used within a DVM, the meaning of some of the terminology differs from that used by manufacturers of sample-and-hold units. For this reason, these definitions are fairly detailed.

Acquisition time: The time for the input amplifier to respond to a full scale step input. This time varies with the type of DVM and varies between ranges. As applied to the sample-and-hold unit alone, acquisition time equals the interval between the sample command and when the output begins to track the input. The first definition applies to DVM's.

Aperture time: The time from application of a command to freeze or hold the input to when it is actually held. This equals the time between the track mode (or sample mode) and the hold mode. Aperture uncertainty is the uncertainty in this time.

Delay mode: The addition of a delay prior to the command to hold to allow settling of the input signal. Used for step inputs.

Acquire-and-hold mode: Same as delay mode.

Hold mode: Mode when the input voltage is frozen or held to be digitized. The hold mode lasts for the digitizing period.

Track mode: Mode where the sample-and-hold unit continuously tracks the input signal.

SYSTEMS OPERATION

One of the major reasons for purchasing a DVM is its ability to automatically make measurements in a system. Systems oriented DVM's may be programmed to change ranges, functions, etc. The readings are presented to the system in digital form. There are two types of operation covered in this section: (1) Parallel operation involves a line-for-line exchange of information, and (2) serial operation transmits both programming information to the DVM and takes readings from the DVM using the same set of lines.

PARALLEL OPERATION

When a DVM is used in a system, the flow of information is managed by control lines. This avoids conflicts in timing. It insures, for example, that the system is not trying to program the DVM while it is making a reading. Instruments must respond to each other.

The most fundamental signal sent to a DVM is an external trigger which commands it to take a reading. The external trigger is acknowledged by a flag or print command. The flag also tells other equipment that the reading is ready. The way it works is—the flag makes a low to high transition to acknowledge the trigger, then falls low when the data is ready. The time that the flag is in a high state equals the digitizing time or reading period. An example is shown in Figure 7-1. The system will not normally issue another trigger until it has absorbed the data.

There is a second way of telling a DVM to take a reading which involves an indirect form of triggering using a hold-off line. This line stops the DVM from using its own built-in trigger. Printers commonly use a hold-off line. When this line is released (goes high), the next internal trigger starts digitization. Precise control over digitization is lost because it is not possible to determine exactly when the internal sample rate generator will trigger again. This form of triggering is shown in Figure 7-2.

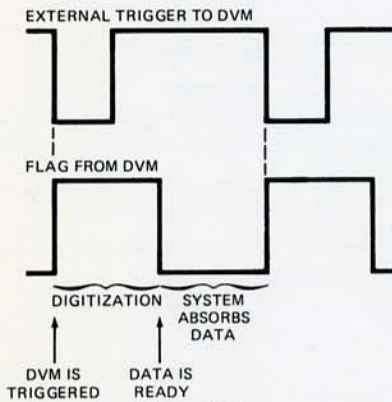


Figure 7-1.

Typical "handshake" between a DVM and the rest of a system.

The 9810A Calculator is shown connected to a 3480B DVM equipped with a 3485A Scanning Unit. This calculator controlled data acquisition system is able to scan and read up to 50 2-wire inputs. Parallel operation is used for programming and BCD information.



Programming also requires management. Once the program lines are set, i.e., range is selected and function is selected, a program exercise line strobes this information into the DVM. A program flag or acknowledgement line indicates that the information was received and that programming is complete. Once programming is complete, a trigger may be issued to take a reading. The sequence is shown in Figure 7-3.

If the DVM is able to carry out some automatic sequence of events, such as scanning a given number of channels, a third line is needed. This is the program initiate line. Actuation of this line follows acknowledgement.

Parallel operation involves a line-for-line approach to data transmission. The output data from a DVM is usually BCD coded in a 8-4-2-1 sequence which means that each digit requires 4-lines. A 4-digit DVM uses 4 x 4 or 16 lines plus an overrange line for data. Function and range are often also BCD coded. Programming is also on a line-for-line basis. A typical AC/DC/ Ω 5-digit DVM would require about 45 data lines to transmit and receive information.

The incoming and outgoing data lines are often isolated which add cost to the DVM. Isolation is quite important, however, since it keeps analog low (low input terminal) isolated from the system ground which is used to transmit data. Most systems are grounded, so without isolation no floating measurements could be made and common-mode rejection specifications would be degraded. Isolation is achieved by passing the digital information across the guard shield using phase transformers, reed relays or photo-isolators. This is illustrated in Figure 7-4. Some DVM's require one isolator for each data line. Other DVM's pass the digital information serially across the guard to reduce the number of isolators.

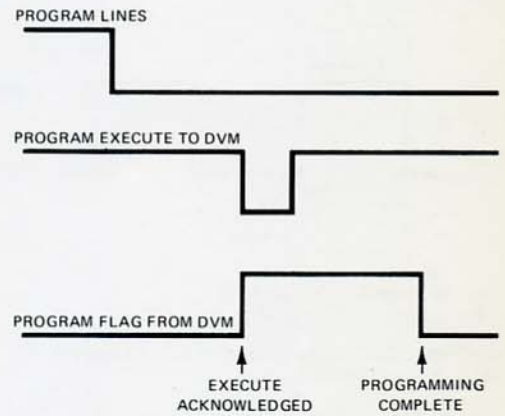


Figure 7-3. Typical programming sequence.

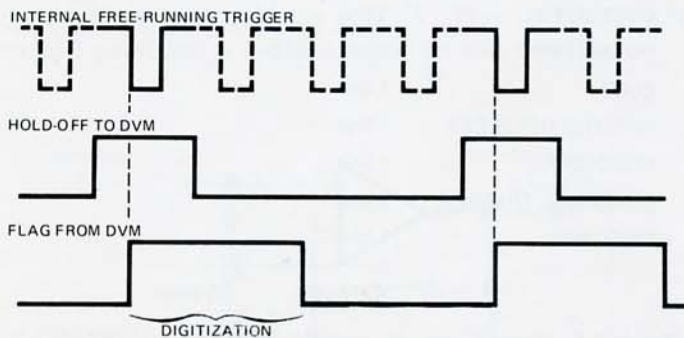


Figure 7-2. The hold-off method of indirectly telling a DVM to take a reading.

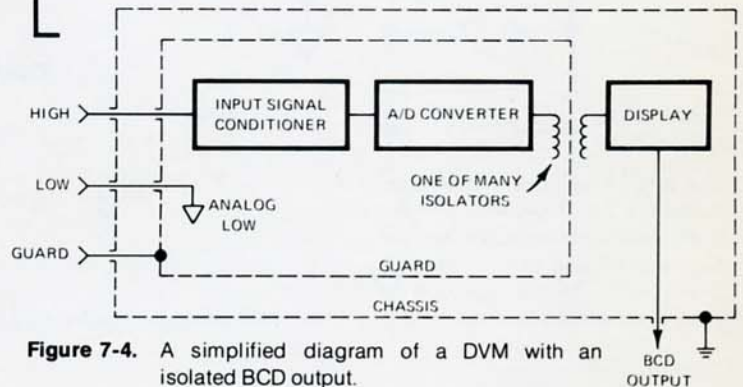


Figure 7-4. A simplified diagram of a DVM with an isolated BCD output.

SERIAL OPERATION

Serial operation has many advantages over parallel operation. Figures 7-5, 7-6 and 7-7 illustrate the lines required for 2-way transmission of data in a parallel manner and in a serial manner. A typical 5-digit DVM would require at least 35 lines to transmit data and 10 more lines for programming. Using the serial approach (also called the ASCII bus), only 15 lines are required.

When data is transmitted serially, a common bus is used. Each instrument on the bus is addressed by a coded number. Once called upon to listen or to talk, the instrument transmits its data using 8 data lines plus 7 additional lines to manage data flow. Each digit in a reading is transmitted one at a time starting with polarity then the most significant digit.

The most common form of serial operation uses ASCII coded characters so that the readings may be printed by a teletype or read directly into a computer or calculator. In contrast, the coding used for parallel operation is not standardized and is different for every instrument.

The I/O slots in a central processor, whether it is a computer or calculator, is one of its most valuable assets.

| | |
|------------------|-----------------------------|
| DATA COLUMN 1 | 4 lines weighted 8, 4, 2, 1 |
| DATA COLUMN 2 | 4 lines weighted 8, 4, 2, 1 |
| DATA COLUMN 3 | 4 lines weighted 8, 4, 2, 1 |
| DATA COLUMN 4 | 4 lines weighted 8, 4, 2, 1 |
| DATA COLUMN 5 | 4 lines weighted 8, 4, 2, 1 |
| OVERRANGE | 1 line |
| RANGE | 3 lines weighted 4, 2, 1 |
| FUNCTION | 4 lines weighted 8, 4, 2, 1 |
| OVERLOAD | 1 line |
| POLARITY | 1 line |
| FLAG | 1 line |
| PRINTED HOLD-OFF | 1 line |
| HOLD-OFF | 1 line |
| EXTERNAL TRIGGER | 1 line |
| GROUND | 1 line |
| TOTAL: | 35 lines |

Figure 7-5. Typical list of parallel BCD information transmitted by a 5-digit DVM.

| | |
|-----------------|--------------------------|
| RANGE | 3 lines weighted 4, 2, 1 |
| AUTORANGE | 1 line |
| FUNCTION | 4 lines, not weighted. |
| PROGRAM EXECUTE | 1 line |
| PROGRAM FLAG | 1 line |
| | <hr/> |
| | 10 lines |

Figure 7-6. Typical list of parallel BCD information required to program a DVM.

| | |
|--------------------------|----------|
| DATA INPUT/OUTPUT | 8 lines |
| TRANSFER CONTROL SIGNALS | 3 lines |
| ADDRESS COMMAND | 1 line |
| SERVICE REQUEST | 1 line |
| REMOTE ENABLE | 1 line |
| END OF OUTPUT | 1 line |
| | <hr/> |
| | 15 lines |

Figure 7-7. Lines required for 2-way transmission using serial operation.



The 9820A Calculator is shown controlling a 3490A DVM using serial operation (the ASCII bus). The 3490A can be one of fifteen devices connected to the same bus. Each instrument on the bus is individually addressable.

The number of I/O slots is often limited. Figure 7-8 shows how I/O slots are used in parallel operation contrasted to serial operation. Since instruments used serially are individually addressable, many different devices can be hung on one 15-wire bus. Two cards, one for programming and one to receive data, are usually required for one single instrument operated in a parallel manner.

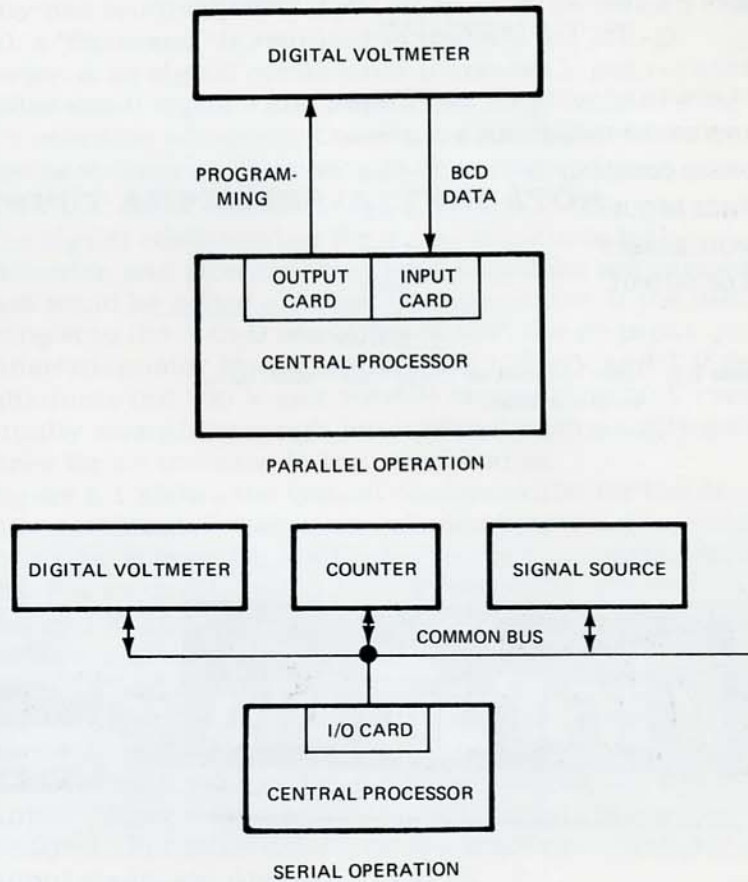


Figure 7-8. Serial operation allows many instruments to be tied together via one I/O card.

SYSTEM STRUCTURE

A system can be anything from a DVM used with a printer to a giant computer-controlled system involving many instruments. In any system, only one device at a time can control it. In the case of a simple DVM/printer combination, the DVM usually tells the printer when it wants its data printed. In larger systems, the central processor is usually the controller.

The central processor can be a programmable calculator or a computer. In either case, the central processor must instruct members of the system what to do. Software driver is usually a machine level set of binary or actual instructions to the instruments in the system. These instructions may have very little literal meaning to the user. For example, the user wishing DVM #3 to take one reading on its 10 V range may be confronted with a set of 100 binary bits, each of which must be sent out. A software driver is used to carry out these instructions. The driver is called as a subroutine. Now the user may program "READ DVM #3" and the driver dumps the 100 or so binary bits to do just that. This is illustrated in Figure 7-9.

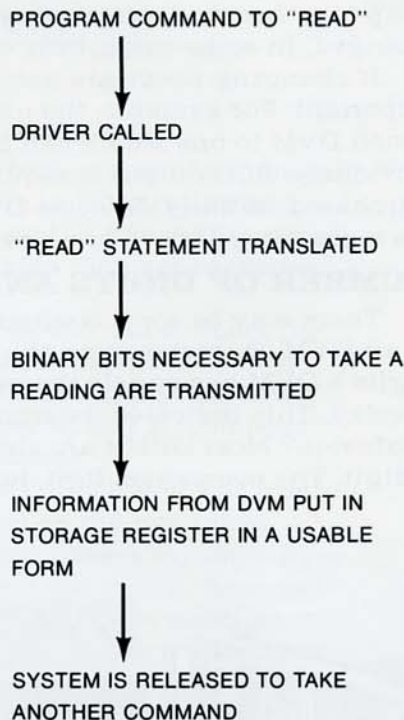


Figure 7-9. Typical sequence in using an English language command to "READ" to when the reading is taken and stored.

READING DVM SPECIFICATIONS

The final selection process involves looking at DVM data sheets from various manufacturers. Selection can be difficult due to the lack of standardization of specifications in the industry. Fortunately, most specifications are easy to understand. In this section, an attempt has been made to cover those which require clarification.

Obviously, the user must first define what is to be measured. Once the immediate measurement problem has been defined, possible future uses for the instrument should be noted. Out of this definition should come some general idea of what levels of resolution and sensitivity are needed. It is also helpful to note what functions are needed. The reason is that there are too many DVM's on the market to compare all of them. DVM's are generally classified according to multifunction capability and the number of digits. For example, if a multifunction 4-digit DVM is needed, this may narrow the choice considerably thus reducing the number of data sheets to be examined.

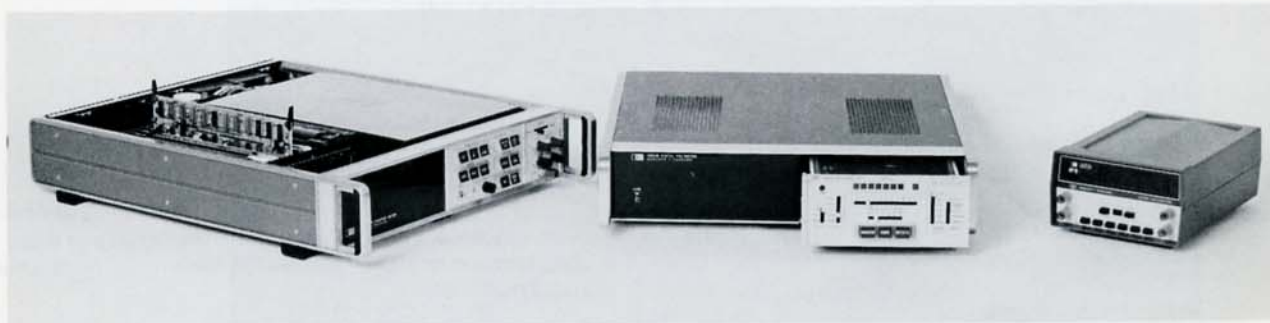
FLEXIBILITY

DVM's vary greatly as to their flexibility. Some DVM's can be changed or added to via plug-in pc boards. Others use snap-together modules or plug-ins. Others cannot be changed. In some cases, only certain things can be changed.

If changing needs are anticipated, then flexibility is important. For example, the user may wish to change his bench DVM to one which can later be used in a system. Obviously, BCD output is required. It could have been purchased initially. In some DVM's, it can be added via a plug-in pc board or a snap-on module.

NUMBER OF DIGITS AND OVERRANGING

There may be some confusion about the most fundamental of all DVM characteristics: the number of digits. The number of digits a DVM has equals the number of "9's" it is able to display. This indicates the number of full digits. Why the confusion? Most DVM's are able to overrange and this adds a digit. The overrange digit, however, is **not** a full digit.



The instruments shown above each use a different type of flexibility. The 3450B uses plug-in PC boards, the 3480B uses plug-in units, and the 3470 uses snap-on modules. Built-in flexibility allows the user to later reconfigure his DVM to meet changing measurement needs.

Let's take an example. A display of "1999" really has only three full digits plus a "1" used for overranging. This overrange digit allows the user to read beyond the normal full scale without loss of accuracy or sensitivity. Overranging is an important specification since it extends a DVM's usefulness. For example, suppose a signal changes from 9.99 V to 10.01V. A 3-digit DVM without overranging can measure up to "9.99V" and would have to up-range to measure the "10.0V." Note that the 0.01V is lost in the process. With overranging, the same 3-digit DVM could measure "10.01V" without loss of sensitivity nor need to up-range.

Overrange is expressed in percentage. A reading of "1999" would equal a 3-digit DVM with 100% overranging. A reading of "1199" equals 20% overranging. A 5-digit DVM with 20% overranging has the same resolution as a 4-digit DVM with 100% overranging under certain conditions. For example, if both instruments are used to measure 1.5 V, both will read "1.5000." The 1V range of the 5-digit DVM cannot be used because it cannot read beyond "1.19999." Of course, the 5-digit DVM has a decade more resolution below its 20% overrange point. The point is that not only does the number of digits determine resolution but also overrange percentage.

SENSITIVITY AND RESOLUTION

These are two voltmeter parameters that are often confused. They are related but define different capabilities. Resolution is a pure number. (i.e., it is a ratio and has no units) Resolution of a DVM, is the ratio of the maximum number of counts that can be displayed to the least number of counts. For example, a 5-digit DVM with 20% overranging can display 120,000 counts. Its resolution is then 120,000 to 1, generally, overranging is ignored and the full scale resolution of a 5-digit DVM is 100,000 to 1, or 0.001%.

Sensitivity is the ability of a DVM to respond to small voltage changes. For example, a 5-digit DVM with a 100 mV full scale range has a 1 μ V sensitivity. The least significant digit is 1 μ V.

If you like to think in more mathematical terms, the sensitivity of a DVM is the lowest full scale range multiplied by the full scale resolution of the DVM. In the examples given here, the resolution is 0.001%, and the lowest full scale range is 100 mV. Therefore, the sensitivity is

$$0.001\% \times 100 \text{ mV} = 1 \mu\text{V}$$

ACCURACY

Accuracy is the exactness to which a voltage can be determined relative to the Legal Volt maintained by the U.S. National Bureau of Standards. Note the word "relative." In order to specify accuracy, the DVM manufacturer must maintain calibration standards traceable back to the Legal Volt. Any errors involved in traceability are added to the accuracy specification.

An equal burden is put on the user. Purchasing a DVM without the equipment or knowledge to calibrate it may not be wise unless the user plans to employ an outside

calibration lab. For DVM's with high accuracy, the calibration equipment can be quite expensive and may enter into the purchase decision.

Rarely is it possible to list where all the errors within a DVM originate. Each DVM design is different and thus the contributing errors are different. Following is a list of individual errors for one specific DVM: the -hp- 2402A.

| | ERRORS |
|---|----------------|
| Linearity of integrator: | ±0.002% |
| Digital ambiguity: | ±0.0005% |
| Full scale drift (24 hour): | ±0.003% |
| Zero drift: | ±0.001% |
| Count-to-count variation: | ±0.0015% |
| Attenuator drift: | ±0.003% |
| 6 month drift: | ±0.003% |
| Initial accuracy traceable to the Legal Volt: | ±0.001% |
| PUBLISHED ACCURACY: | ±0.015% |

Note that the magnitude of each individual error is small. Note also that the error due to traceability to the Legal Volt is included.

To be meaningful, accuracy must be stated along with the conditions under which it will hold. These conditions should include time, temperature, line variations and relative humidity. These conditions should be realistic relative to the DVM's intended application. For example, most manufacturers specify a temperature range of $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ which covers the majority of environments. Other DVM's are specified for $\pm 1^{\circ}\text{C}$ which is fine in a lab but hardly suitable for on-site testing or production use.

Time indicates calibration cycle. DVM's are specified to hold their accuracy for 30 days, 90 days, 6 months and even 1 year. Many times, several accuracy specifications are included for various times.

Accuracy is expressed as a percent of reading plus a percent of range (or full scale). The percent of range may alternately be expressed as $\pm X$ digits. Two identical accuracy specifications are shown below:

$$\begin{aligned} & \text{4-DIGIT DVM} \\ & \pm(0.01\% \text{ of reading} + 0.01\% \text{ of range}) \\ & \text{or} \\ & \pm 0.01\% \text{ of reading} \pm 1 \text{ digit} \end{aligned}$$

The accuracy of a DVM may be considerably less than the resolution. For example, a 4-digit DVM has a resolution of 0.01% or 1 count in 10,000. However, in many applications an accuracy of $\pm 0.05\%$ to 0.08% is sufficient. If the DVM has good linearity, short term stability, and low noise, it is well suited to most applications. In short, if the DVM can make repeatable measurements, its absolute accuracy need not match its resolution. This type of DVM is becoming very common because it is much less expensive to design and manufacture.

SHORT TERM STABILITY

Unlike accuracy, short term stability is **not** relative to the Legal Volt although it is specified under similar conditions. Short term stability is usually specified for 24 hours and for $\pm 1^\circ\text{C}$ instead of $\pm 5^\circ\text{C}$. Accuracy and short term stability are contrasted in Figure 8-2.

Short term stability tells the user how good the DVM is for relative measurements. It also indicates the effective sensitivity of the DVM. This specification is used when a known standard voltage is measured, then an unknown is measured. Short term stability indicates how accurately this comparison can be made or how good the DVM is as a transfer standard.

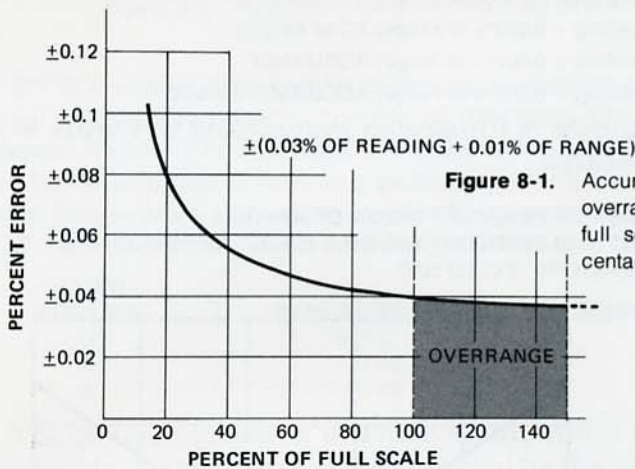


Figure 8-1. Accuracy of a typical 4-digit DVM with 50% overrange plotted as a function of percent of full scale. Accuracy improves at high percentages of full scale.

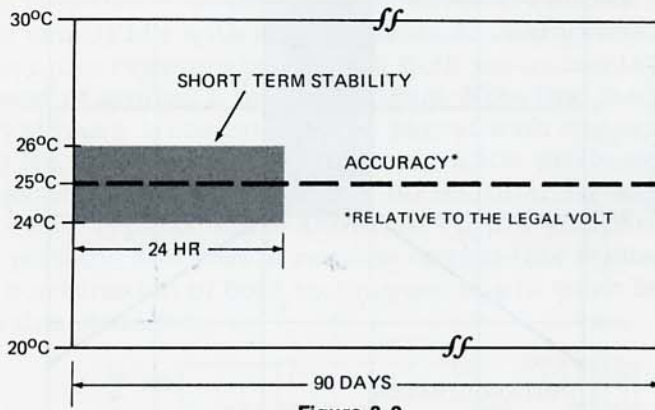


Figure 8-2.

A diagram illustrating the difference between short term stability and accuracy.

TEMPERATURE COEFFICIENT

Temperature coefficient (TC) is the amount of change in accuracy per degree change in temperature outside the temperature band given in the accuracy specification. Errors calculated using the temperature coefficient are additive to the basic accuracy specification. In order to make this calculation, the user must know over what temperature range the instrument was designed to operate.

If, for example, the DVM's accuracy is specified for $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and the user wishes to know what the accuracy is at 40°C , then the TC is multiplied by 10°C and added to the accuracy as shown below:

$$\begin{aligned} & \pm(0.0004\% \text{ of reading} + 0.0003\% \text{ of range}) / ^{\circ}\text{C} \times 10^{\circ}\text{C} = \\ & \pm(0.004\% \text{ of reading} + 0.003\% \text{ of range}) \text{ TC at } 40^{\circ}\text{C} \\ & \pm(0.008\% \text{ of reading} + 0.002\% \text{ of range}) \text{ ACCURACY} \\ & \pm(0.012\% \text{ of reading} + 0.005\% \text{ of range}) \text{ ACCURACY AT } 40^{\circ}\text{C} \end{aligned}$$

This same example is illustrated graphically in Figure 8-3 for all temperatures.

ACCURACY: $\pm (0.008\% \text{ OF READING} + 0.002\% \text{ OF RANGE})$
TEMP. COEFFICIENT: $\pm (0.0004\% \text{ OF READING} + 0.0003\% \text{ OF RANGE}) / ^{\circ}\text{C}$
OPERATING TEMPERATURE: 0°C TO 50°C

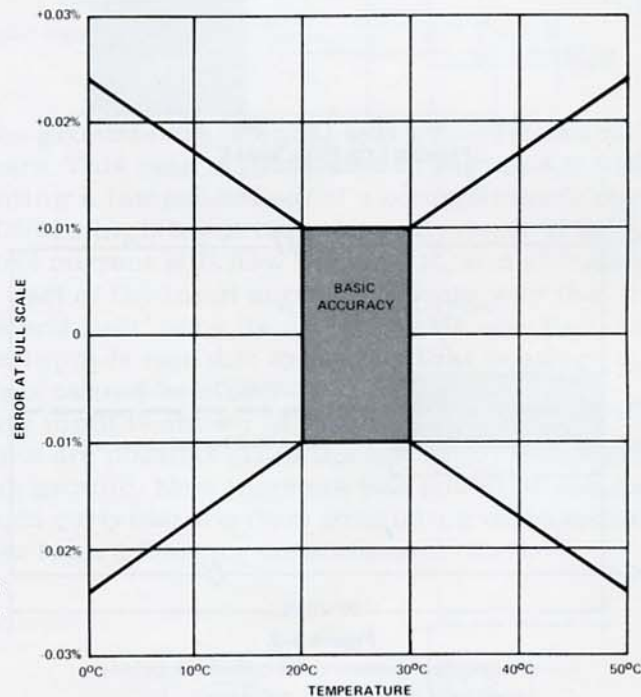


Figure 8-3. A diagram of the temperature coefficient specification as applied to the basic accuracy specification for a 5-digit DVM.

SPEED

The user needs to know two things about the speed of the DVM he contemplates purchasing: (1) how long it takes to respond to a change in the input signal and, (2) how many readings per second can be made both internally and externally.

The time for a DVM to respond is usually specified for the worst case which is a full scale step input. Included in response time is the time required to digitize the signal. As

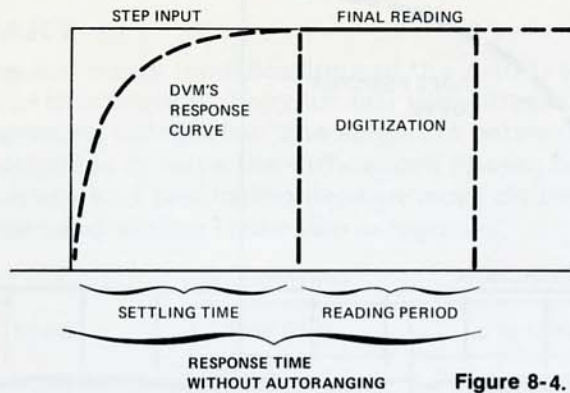
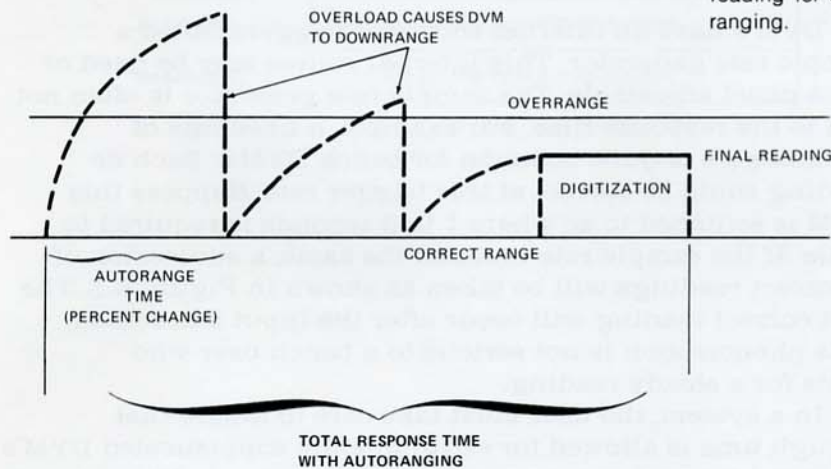


Figure 8-4. An example of DVM response time from the application of an input voltage to a correct reading for operation with and without autoranging.



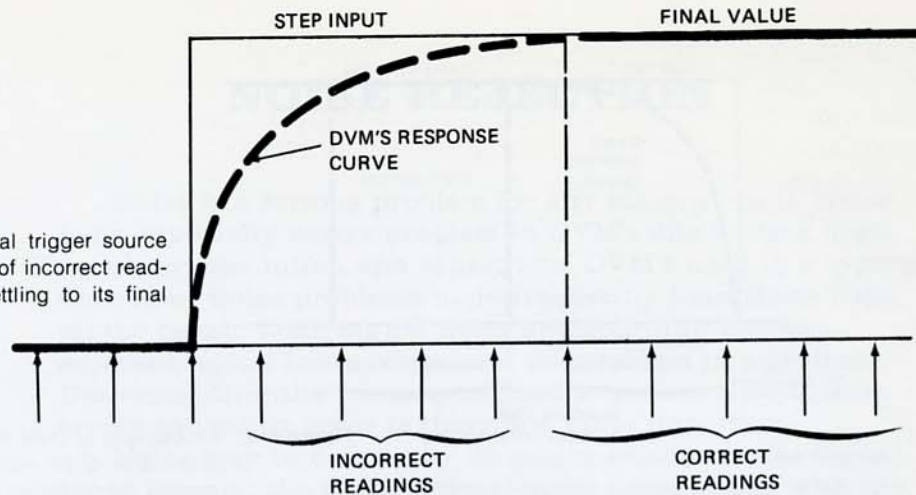
shown in the upper part of Figure 8-4, response time is composed of the settling time of the input amplifier or converter plus the digitizing time or reading period.

Settling time may not be given on a data sheet since the user really wants to know how long it takes to get the final reading. Some DVM's are able to respond in less than 1 ms to a dc input but require 3 s to respond to an ac input. Converters typically add to the response time.

The reading period is a measure of how long it takes the DVM to digitize the signal. The reading period is defined as the time elapsed from when the DVM is given a trigger to the time a valid reading comes back. Some DVM's include the settling time in the reading period. Other DVM's include a switchable delay to allow settling prior to the start of A-to-D conversion.

Elements that increase the response time of a DVM include filtering, a longer gate length for an integrating DVM and autoranging. An increase in the gate length increases the reading period since it is part of the digitization of the input signal. Increases in filtering adds to the settling time but does not effect digitization. Autorange is specified as time per range change and, as shown in the lower part of Figure 8-4, can greatly increase overall response time.

Figure 8-5. A DVM with a fixed internal trigger source can produce a succession of incorrect readings while the input is settling to its final value.



DVM's have an internal source of triggers called a sample rate generator. This internal source may be fixed or front panel adjustable. The sample rate generator is often not tied to the response time. For example, a fixed rate of 5 readings/s is quite common for bench DVM's. Each dc reading could be correct at this trigger rate. Suppose this DVM is switched to ac where 1 to 3 seconds is required to settle. If the sample rate remains the same, a succession of incorrect readings will be taken as shown in Figure 8-5. The first correct reading will occur after the input has settled. This phenomenon is not serious to a bench user who waits for a steady reading.

In a system, the user must take care to insure that enough time is allowed for settling. More sophisticated DVM's designed for systems automatically add enough delay to cover any measurement situation. The delay is variable depending on filter position and function. This situation is illustrated in Figure 8-6.

One more point on speed: The internal sample rate does not necessarily reflect at what rate external triggers may be given. Internal triggers are designed for bench use and are usually limited to 20/s but external triggers may be issued up to 1000/s. All-in-all, the user must know how the DVM is to be used before speed can be calculated.

INPUT IMPEDANCE

Many modern DVM's use a FET input which yields $> 10^{10}\Omega$ input resistance on the lower ranges. Resistive dividers are used on the 100 V and 1000 V ranges yielding an input resistance of $10M\Omega$. One characteristic of a FET input is leakage current. The magnitude is usually less than 10 pA at 25°C but may become greater at higher temperatures. This dc kickback current will only effect readings from a high source resistance.

The input impedance specification for an ac converter will include not only the resistive element but also shunt capacity. In come cases where bandwidth is up in the MHz, inductive elements may be added to the input specification. When measuring sources that are not purely resistive, the shunt capacitance may combine with the source reactance to affect the linearity or bandwidth of the converter.

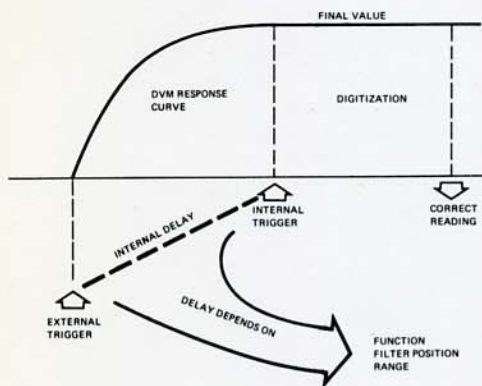


Figure 8-6.

To solve external trigger problems and prevent incorrect readings, some DVM's have a built-in delay to allow the input signal to settle before digitization takes place.

DVM's with high dc reading speeds may list High-to-Low, Low-to-Guard and Guard-to-Chassis capacity. Although these capacities are small, they become important if switching speeds are high. Stored charges may not be able to discharge between readings thus causing errors. This problem occurs most often when scanning, and is illustrated in Figure 8-7 for two bridge measurements. The first bridge may put a small charge on the Low to Guard capacity. If the second bridge is switched too rapidly, the capacitance cannot be discharged fast enough through the source resistance of the second bridge and a reading error will result. There are several solutions: one is to slow the reading speed, and another is to drive the guard with a voltage approximately equal to the potential of the Low input terminal (on the first bridge). This will prevent a charge build-up. Still another solution is to short some of the channels to discharge the internal capacities.

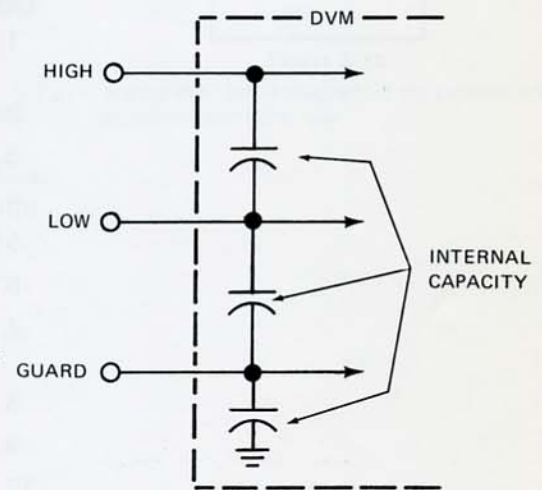
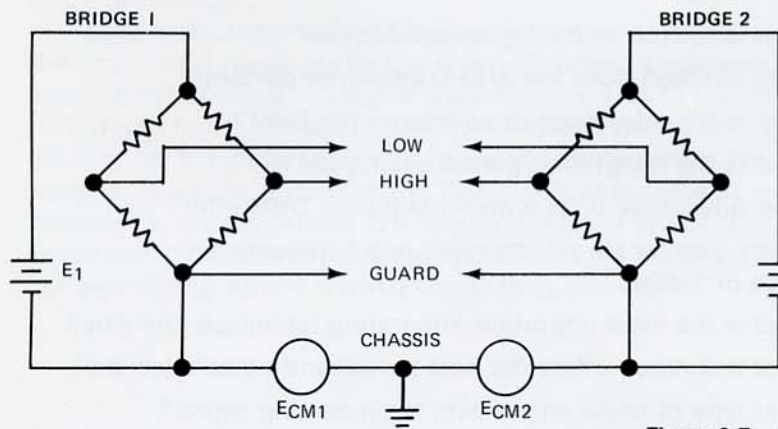


Figure 8-7. When scanning two channels in rapid sequence, such as the two bridges shown above, the internal capacitance of the DVM may develop a charge which causes reading errors. Any charge created by Bridge 1 will discharge through Bridge 2 and produce an offset in the reading.

COMMON MODE REJECTION

As has been pointed out in a prior section, the common mode rejection of a DVM is highly dependent on low input lead resistance. The DVM manufacturers have more or less standardized on using a 1 K Ω unbalance in the low lead. There are some manufacturers which use a 100 Ω unbalance to make the common mode rejection specification look better by 20 dB. In general, for every decade reduction in the value of the unbalance resistor, the CMR specification appears to improve by 20 dB.

APPENDIX

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APPENDIX I SELF TEST QUESTIONS AND ANSWERS

QUESTIONS

1. What are the advantages of a DVM over analog and differential voltmeters?
2. What is the job of the signal conditioner?
3. What function does the A-to-D converter perform?
4. What is the advantage of an integrating DVM?
5. What is the integration period usually set to?
6. What advantage does a non-integrating DVM offer?
7. Which gate length rejects more noise frequencies: 1/10s or 1/60s?
8. What is the most important integrating technique and why?
9. What technique offers the best broadband noise rejection?
10. What type of noise enters with the incoming signal?
11. What techniques are available within a DVM to reduce errors due to normal-mode noise?
12. What technique is used to reduce errors due to common-mode noise?
13. How does guarding work?
14. What are average responding ac converters designed to measure?
15. What type of distortion produces the most serious errors in an average responding converter?
16. What type of ac converter is required to measure a pulse?
17. What benefit does a 4-wire ohms converter offer?
18. What problem does a FET input stage to a dc amplifier create?
19. What technique can be used to allow a DVM to read a changing input voltage accurately?
20. How many digits does a DVM have if its maximum reading equals "1999?" What is the overrange percentage?
21. What is the difference between resolution and sensitivity?
22. What conditions should be included in an accuracy specification?
23. Where is accuracy best relative to full scale?

24. A CMR specification of 100dB with a 100 Ω unbalance equals how many dB with a 1K Ω unbalance?

ANSWERS

1. Over analog meters: readability, resolution, speed, accuracy, and the ability to be used in a system.
Over differential voltmeters: readability, speed, and the ability to be used in a system.
2. Signal conditioner: converts the unknown input quantity to a dc voltage within the range of the A-to-D converter.
3. A-to-D converter: converts the prescaled dc voltage from the signal conditioner to its digital equivalent.
4. Integrating DVM: ability to mathematically reduce the effects of line-related noise.
5. Integration period is usually set to the period of the line frequency.
6. Non-integrating DVM's offer a speed advantage.
7. 1/10s rejects all multiples of 10 Hz.
8. The dual-slope integrating technique offers design simplicity.
9. Broadband noise rejection: filtering.
10. With the signal: normal-mode noise.
11. Integration and filtering are used to reduce errors caused by normal-mode noise.
12. Guarding reduces common-mode noise.
13. Guarding shunts common-mode currents away from the measuring circuit by using a passive shield.
14. Average responding converters are designed to measure pure sine waves.
15. Odd harmonics produce the most serious errors.
16. A true rms converter with a crest factor high enough to accommodate the pulse.
17. A 4-wire ohms converter eliminates errors caused by lead resistance.
18. FET inputs inject a small amount of dc leakage current which only affects measurements from high source resistances.
19. Sample-and-hold freezes a changing input voltage to allow the DVM to make an accurate measurement.
20. The DVM has 3 full digits plus 100% overranging.
21. Sensitivity is the ability to measure a small voltage or voltage change. Resolution is the smallest change which can be observed on the front panel.
22. Accuracy should include time, temperature, power line variations and relative humidity.
23. Accuracy is best at or above full scale.
24. 100 dB rejection with 100 Ω unbalance equals 80 dB rejection with 1 K Ω unbalance.

APPENDIX II MORE ON GUARDING AND CMR

The subject of guarding and common-mode signals can be treated in a slightly different manner by looking at internal impedances and injected noise within the DVM. This approach can best be discussed by a series of examples.

Figure 9-1 shows a circuit to be measured with one model for a real-life three terminal source. E_{A1} and E_{A2} are normal-mode signals. E_{C1} and E_{C2} are common-mode signals. Z_A is the source resistance for the normal-mode sources plus the wiring impedances from the High terminal to the normal-mode sources. Z_B is the lead impedance in the wiring for the Low terminal connections. Z_C is the impedance earth ground at the common-mode source.

Adding to Figure 9-1 the imperfections Z_1 , Z_2 , and Z_3 shown in Figure 9-2, it is easy to see how these imperfections can cause currents to flow through Z_A and Z_B which cause error voltages to occur between the High and Low terminals. Z_3 illustrates the possibility of stray impedances connecting to an internal part of the voltmeter. Although the effect of Z_3 is difficult to determine, it is well to consider the possibility of its existence. In well-designed voltmeters, Z_3 contributes little in the way of inaccuracies and its effect can be included with Z_1 and Z_2 . It appears obvious from Figure 9-2 that, if Z_1 , Z_2 , and Z_3 are sufficiently large, the error they introduce can be exceedingly small.

Figure 9-3 adds a power transformer to provide power for operation of the instrument. This transformer may significantly decrease the value of Z_2 for a voltmeter. Besides lowering the value of Z_2 , the transformer may introduce additional sources of error.

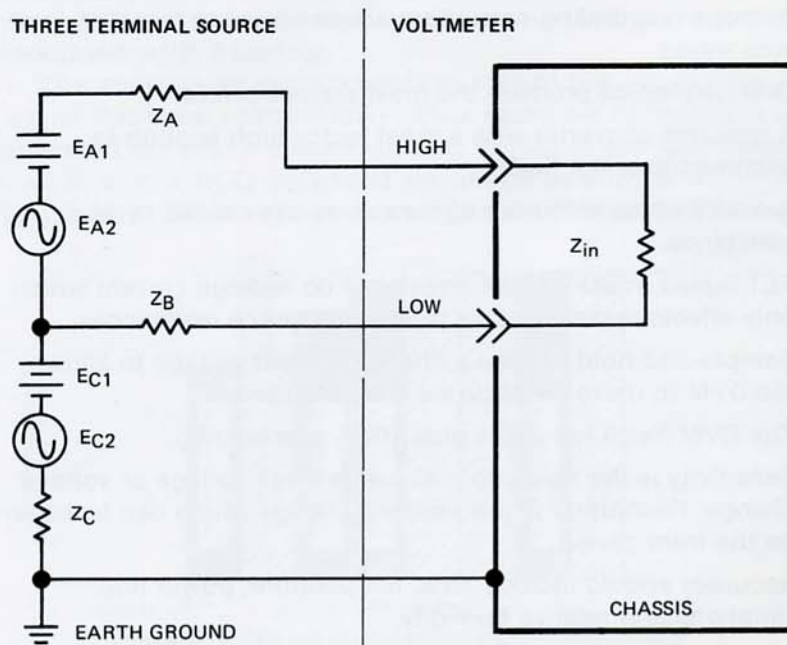


Figure 9-1. Typical measurement with a three terminal source.

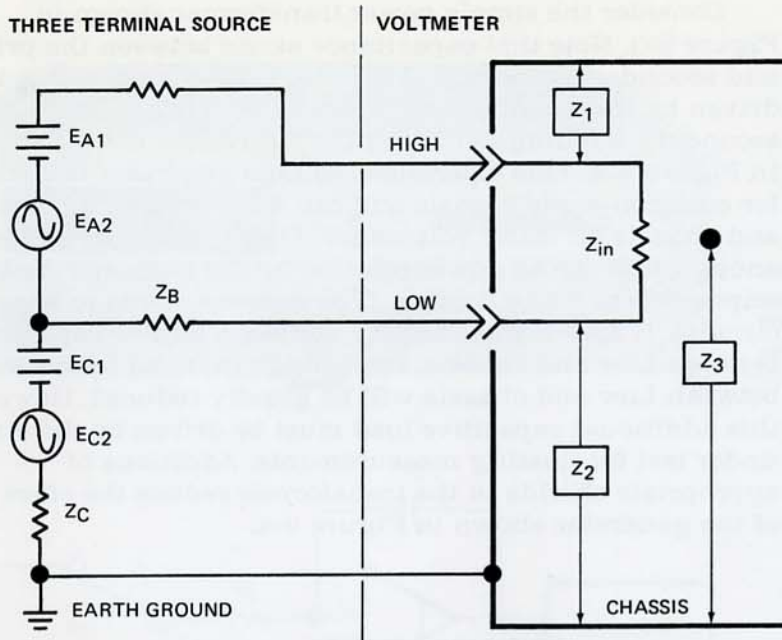


Figure 9-2. Typical measurement with a three terminal source and some voltmeter imperfections added.

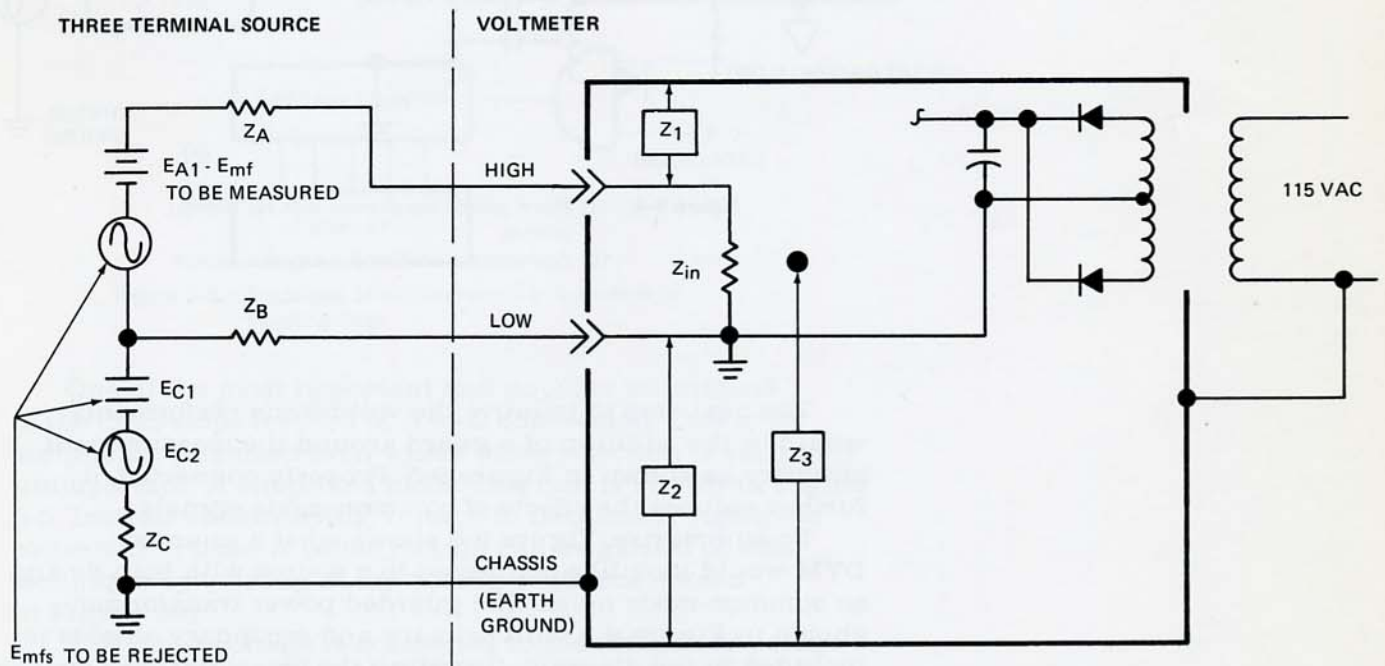


Figure 9-3. Power transformer added to Figure 9.2.

Consider the simple power transformer shown in Figure 9-3. Note that capacitance exists between the primary and secondary windings. This distributed capacitance is driven by the ac voltages present in both the primary and secondary windings yielding the equivalent circuit shown in Figure 9-4. This equivalent voltage generator is a source for common-mode signals and can be measured between Low and chassis on many voltmeters. This signal may be large enough that the ac power injected by the voltmeter makes it impossible to make floating-type measurements in sensitive circuits. If Z_2 is made small by adding a sizable capacitor between Low and chassis, the voltage that can be measured between Low and chassis will be greatly reduced. However, this additional capacitive load must be driven by the circuit under test for floating measurements. Additions of appropriate shields in the transformer reduce the effect of the generator shown in Figure 9-4.

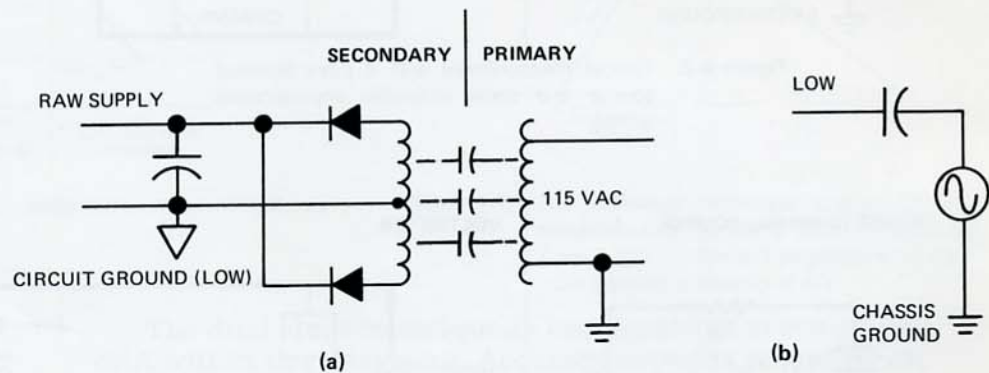


Figure 9-4. (a) Basic power transformer with no internal shields.
(b) Equivalent unwanted signal source.

The next step to improve the voltmeter's performance would be the addition of a guard around the measurement circuitry as shown in Figure 9-5. Properly connected, it further reduces the effects of common-mode signals.

To summarize, Figure 9-6 shows what a guarded DVM would look like connected to a source with both dc and ac common-mode noise. The guarded power transformer shown in Figure 9-5 with primary and secondary shields is included in the diagram. Guarding the transformer as well as the DVM is the key to reducing common-mode signals in the measurement circuit, yet maintains the ability of the DVM to make floating measurements.

Based on:
Carlson, Larry and Larson, Dee, "Voltmeter Seminar,"
Hewlett-Packard Company, Loveland Instrument Division, 1971,
(in-plant publication).

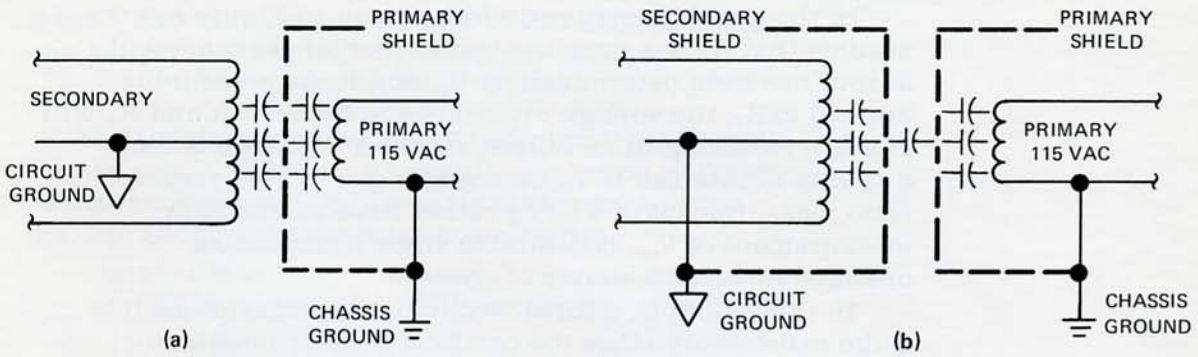


Figure 9-5. (1) Basic power transformer with a primary shield added.
 (b) Basic power transformer with both a primary and secondary shield added.

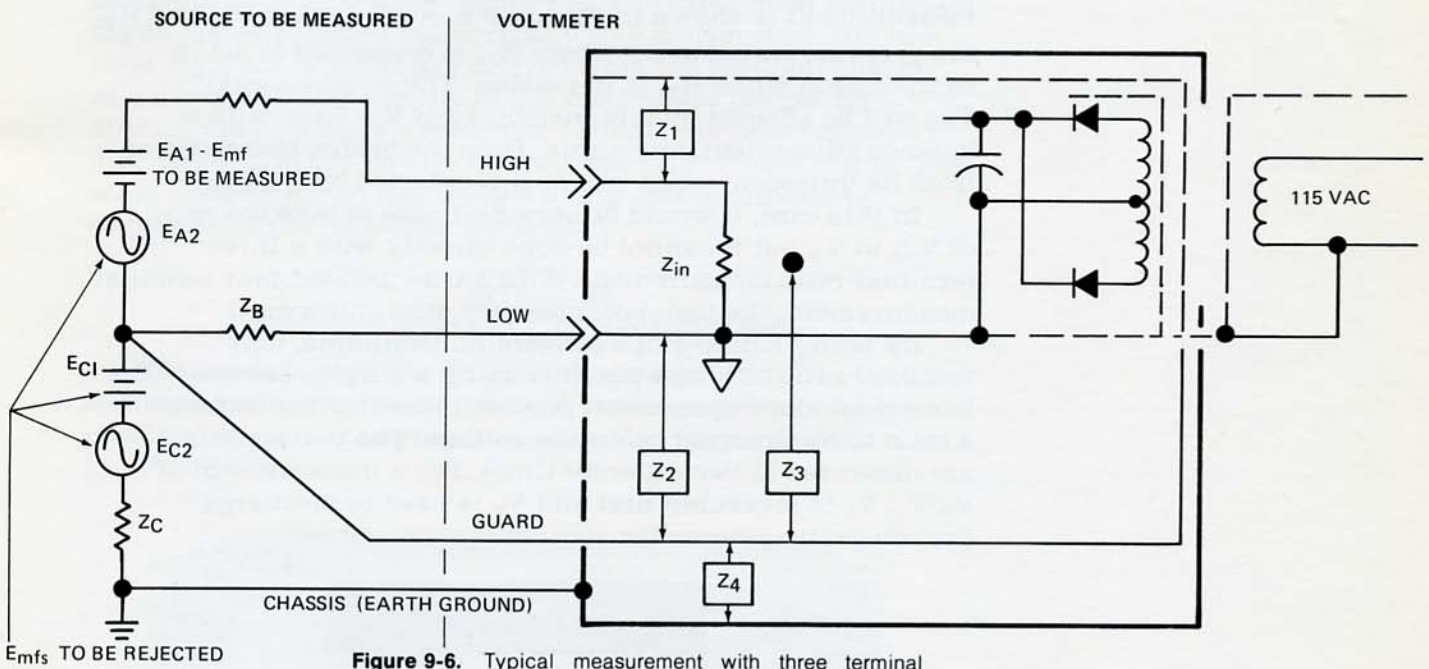


Figure 9-6. Typical measurement with three terminal source using a guarded voltmeter.

APPENDIX III DC RATIO MEASUREMENTS

Ratio capability is a good example of the increase in versatility in modern DVM's. Often it is more convenient and more accurate to determine the ratio of two signals rather than attempt to measure both absolutely.

In the simple resistive divider shown in Figure 9-7, assume that R_T is a pressure transducer whose quiescent output has been determined by V_{in} and R . As pressure is applied to R_T , the voltage division ratio between R and R_T will change, resulting in an output signal ΔV_{out} . This is the quantity of interest. If V_{in} changes, V_{out} will also vary. A ratio measurement of V_{out}/V_{in} rather than an absolute measurement of V_{out} is desirable since it eliminates changes in V_{in} as a source of error.

In this example, a three terminal ratio measurement is quite satisfactory since the common lead for measuring the voltages can be connected to ground. There are a large class of measurements, however, which require a four terminal ratio measurement, i.e., where there cannot be a common connection between the two signals.

An example of a circuit that requires a four terminal measurement is shown in Figure 9-8. Assume that R_{T1} and R_{T2} are pressure transducers where R_{T1} is connected to act in compression when R_{T2} is in tension. The output signal V_{out} will be affected by any instability of V_{in} . Even with a balance adjustment, any signal from the bridge that deviates from its quiescent point will still be affected by a ΔV_{in} .

In this case, it would be very desirable to take the ratio of V_{out} to V_{in} but it cannot be done directly with a three terminal ratio measurement. With a true isolated four terminal measurement, the task becomes very straightforward.

By using a dual-slope conversion technique, four terminal ratio becomes possible using a single converter. The basic dual-slope conversion process measures the input as a ratio to the internal reference voltage. The two signals are measured at two different times. For a measurement of V_X/V_Y , V_X is measured first and V_Y is used to discharge the integrating capacitor.

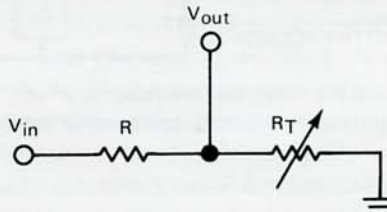


Figure 9-7. To accurately determine R_T , the ratio of V_{out} to V_{in} is more important than the absolute value of V_{out} . As a ratio, accuracy is not dependent on fluctuations in V_{in} .

Since the measurement of V_x/V_y is made successively, it is possible to utilize the same input attenuator, the same input amplifier and the same converters (AC or OHMS) to make a totally isolated measurement of the ratio of two signals. This may be done quite simply by multiplexing the actual voltmeter input between two separate sets of terminals as shown in Figure 9-9.

This multiplexing technique has several advantages. For one, the input impedance for both the V_x and V_y inputs can be identical. Each signal may be attenuated or amplified as required to normalize it to the basic internal range of the instrument. The same autoranging circuits can be used for both inputs. Thus, a four terminal measurement may be made by connecting the two inputs without regard to magnitude, isolation, or polarity (within the voltage breakdown limitations of the instrument).

Based on:

Kay, Bill and Harmon, Jerry L., "Twelve Functions in a New Digital Meter," Hewlett-Packard Journal, March 1969.

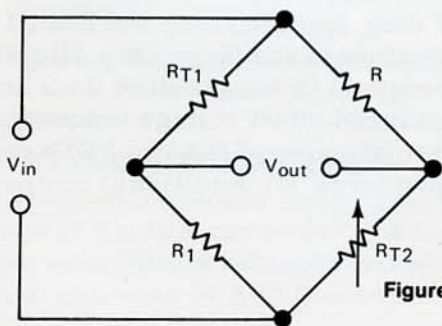


Figure 9-8. A four terminal ratio measurement is required on this balanced bridge to make V_{out} independent of any ΔV_{in} .

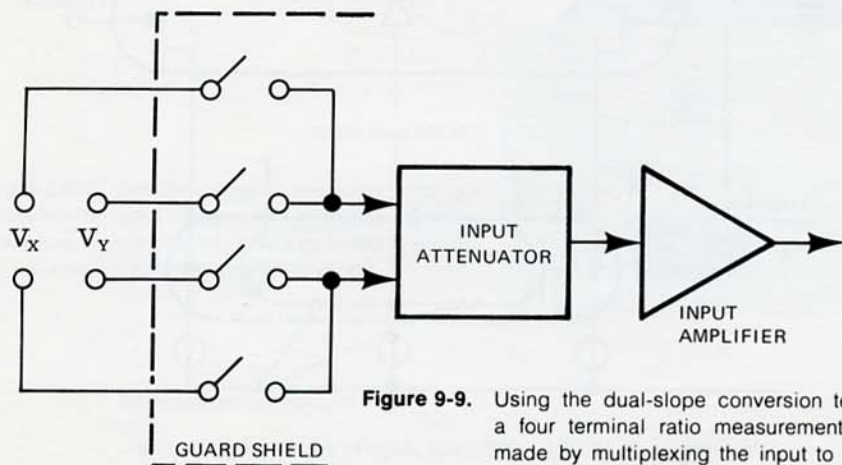


Figure 9-9. Using the dual-slope conversion technique, a four terminal ratio measurement may be made by multiplexing the input to the DVM.

APPENDIX IV FET INPUT TO A DC AMPLIFIER

This section covers the FET input stage to the 3480A/B Digital Voltmeter and illustrates some of the fundamentals of this design approach.

A matched pair of field-effect transistors (FET's) may be used for the differential input stage in a dc input amplifier. The major parts of this input stage are shown in Figure 9-10. The FET offers both high input resistance ($> 10^{10}\Omega$) and relatively small leakage current. Bipolar devices have considerably more leakage current. The FET's are operated in a balance common drain configuration to achieve minimum sensitivity to offset voltages and to gain variations.

To reduce parameter variations caused by temperature fluctuations, the FET environment is temperature controlled at a temperature higher than the maximum expected ambient. An integrated circuit is used as an "oven" to maintain the FET at the desired temperature. The IC used has within it all the circuitry normally associated with an oven. This includes control circuitry, heaters, temperature sensors and amplification. The FET dice, mounted atop the heated IC chip, assume the temperature of the large chip. High thermal gain and the resulting control in temperature does not, however, guarantee a reduced offset voltage temperature coefficient (TC). The thermal gains of the two FET's must be matched due to their own large TC. Additional compensation is therefore necessary.

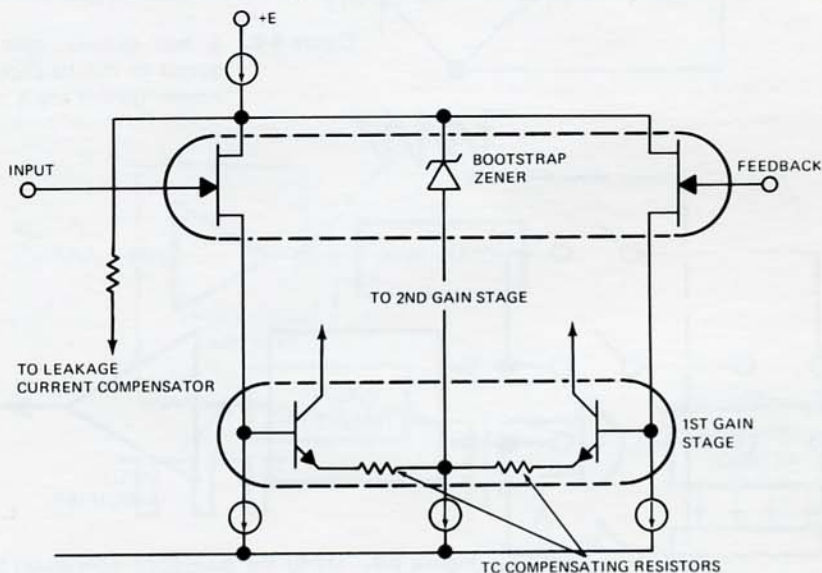


Figure 9-10. Dual FET input stage to the dc amplifier in a DVM. The FET dice are mounted on a heated chip. TC compensation is achieved by resistors in the 1st gain stage.

As shown in Figure 9-11, the device is constructed symmetrically about the two FET dice. Thermal gradients across the face of the IC may be reduced by an anodized aluminum heat sink. Epoxy, which is electrically resistive but thermally conductive, is used to bond the FET's to the heated chip.

The FET's are operated at 80°C, a temperature high enough above ambient to allow regulation when the DVM is operated at elevated temperatures. To keep the resulting offset current (<10pA) independent of input voltage, the compensation circuitry is bookstrapped.

Even though the temperature of the FET's are controlled, the offset voltage TC of the FET may still be greater than desired. To reduce this to < 1 μ V/°C, the entire amplifier is temperature compensated. The amplifier's temperature is varied in a controlled environment and the TC is calculated. Based on this calculation, resistive compensation shown in Figure 9-10 is added. The amplifier is tested again and the reduced TC calculated. The desired TC is arrived at this way. Compensation is achieved by varying the base-emitter voltage match of the first bipolar gain stage. Resistors are added in series with the emitters to get the required match.

Based on:

Walter, Craig and Juneau, H. Mac., and Thompson, Lee, "A New High-Speed Multifunction DVM," Hewlett-Packard Journal, January 1971.

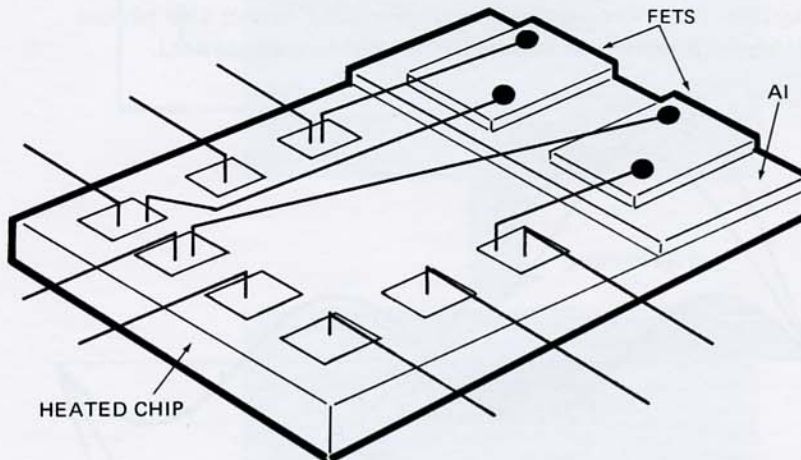


Figure 9-11. Rough diagram of the construction of a heated chip with the FET input stage mounted on the chip. The chip includes heaters.

APPENDIX V
EFFECTS OF DISTORTION
ON AVERAGE AND PEAK RESPONDING METERS

The accuracy with which an average-detecting voltmeter will read the true rms value of a waveform depends both upon the amount of distortion present and upon the phase relationships between the fundamental and its harmonics. The rms reading, E_{rms} , for $E_h < E_f$, is given by:

$$\frac{E_{rms}}{E_{avg}} \cong 1 + 1/2 \left(\frac{E_h}{E_f} \right)^2 \quad (1)$$

where E_h is the magnitude of the harmonic and E_f is the magnitude of the fundamental.

The reading of an average-responding meter is unaffected by the presence of small amounts of even, in-phase harmonics, since no area is added to the waveform as shown in Figure 9-12. An rms reading differs from the average value by:

$$1/2 \left(\frac{E_h}{E_f} \right)^2$$

For a 0.1% second harmonic, the maximum error introduced is only 0.00005%. Second harmonics are usually not an important source of error in **average-reading voltmeters**.

For a quadrature phase relationship, the average value can be approximated by Eq. 1 and essentially no error is introduced.

A waveform containing odd harmonics results in considerably more error in the reading of an **average-responding voltmeter**. Errors caused by even harmonics always result in a lower reading, but errors caused by odd harmonics can result in higher or lower readings, depending upon the phase relationship between harmonics and fundamental.

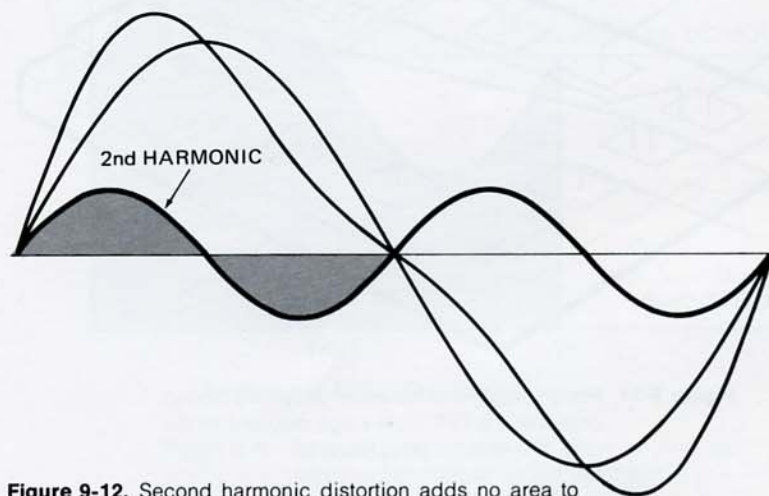


Figure 9-12. Second harmonic distortion adds no area to the composite waveform. For this reason, small amounts of in-phase second harmonic distortion have little effect on an average responding converter.

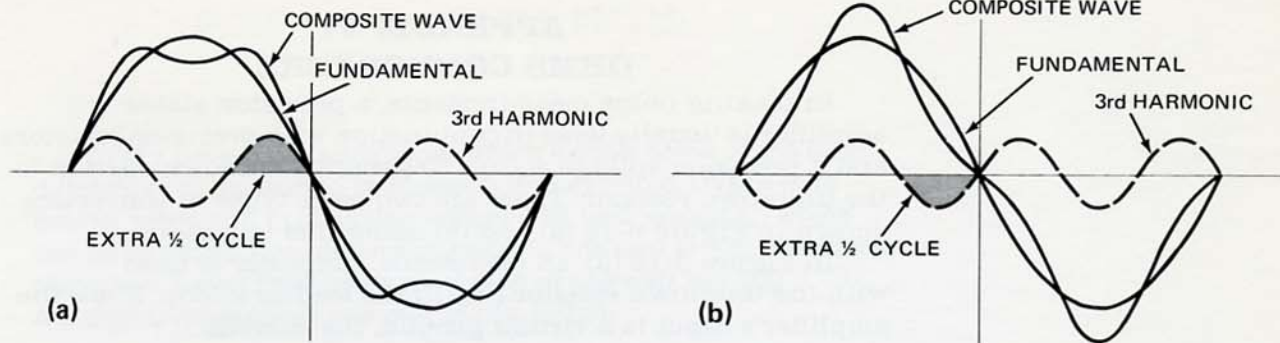


Figure 9-13. In-phase third harmonics (a) add the area of an extra half-cycle to the envelope and cause a higher than rms reading of an average-responding meter, while an out-of-phase harmonic (b) results in a lower than rms reading.

The maximum area under the envelope (and the higher reading) occurs when the harmonic contributes the area of an extra one-half cycle to the fundamental, as shown in Figure 9-13 (a) and (b). Subtracting a one-half cycle results in a low reading. For small amounts of third harmonic generally encountered in precision measurements, the maximum plus or minus errors that can occur are

$$\text{Error} \cong \frac{E_h}{3E_r} \quad (2)$$

The above equation gives total error, since small amounts of third harmonic have little effect upon the rms value. A third harmonic of 0.1% of fundamental could cause a change of 0.033% of the average reading, but only 0.00005% of the rms value.

For odd harmonics higher than the third, the half-cycle contribution becomes less, and the error decreases as the order of harmonic increases. Equation 2 can be rewritten as,

$$\text{Error} \cong \frac{E_h}{nE_r}$$

where n is the order of the odd harmonic.

Effects of Harmonics on Peak-Responding Meters

For peak-responding voltmeters, the maximum error will occur when the phases of the wave components are such that a peak of the harmonic coincides with a peak of the fundamental. The maximum magnitude of the plus error (higher than rms value) will be the same regardless of the order of the harmonic. For small amounts of distortion, the maximum amount of error is plus or minus the amount of distortion directly.

A lower than rms reading occurs when the peak of the harmonic is in phase opposition to the peak of the fundamental. As the order of the harmonic, and/or the amount of distortion increases, peaks are formed adjacent to the peak of the fundamental. The meter will respond to these neighboring peaks. As their amplitude increases, the meter error approaches that of the maximum (higher-than-rms) reading.

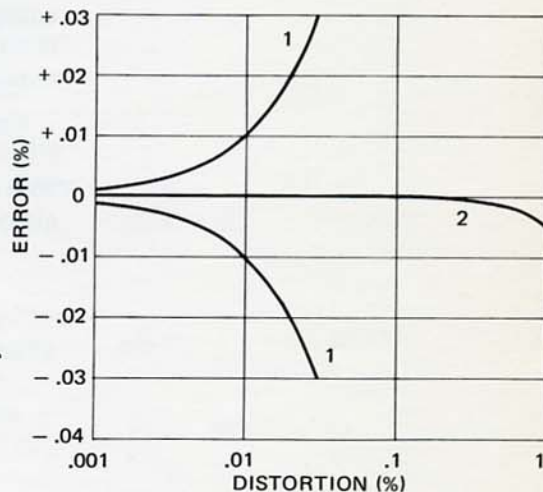


Figure 9-14.

Effect of even harmonics on average-reading voltmeters (Curve 2), and on peak-reading voltmeters (Curve 1).

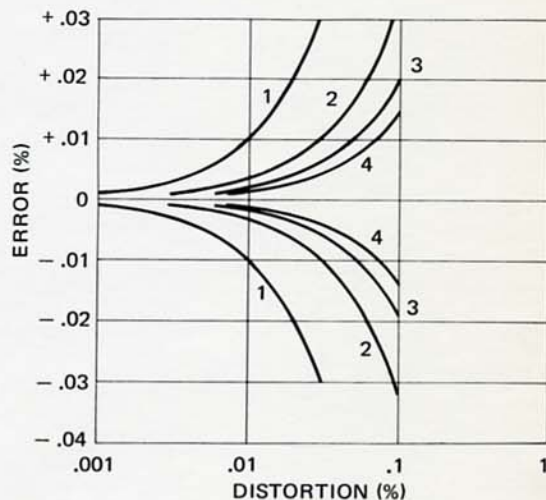


Figure 9-15.

Effect of odd harmonics on average-reading voltmeters (Curves 2, 3, 4), and peak-reading voltmeters (Curve 1).

Based on:

Hanson, Fred L., "High-Accuracy AC Voltage Calibration,"
Hewlett-Packard Journal, June 1968.

APPENDIX VI OHMS CONVERTERS

In making ohms measurements, a precision stable amplifier is usually used in conjunction with precision resistors and a precision voltage source to generate a known current to the unknown resistor. There are two basic types of converters shown in Figure 9-16 (a) and (b) using this technique.

In Figure 9-16 (a), an operational amplifier is used with the unknown resistor (R_x) in the feedback loop. Since the amplifier's input is a virtual ground, the current through R_x is:

$$I = \frac{R}{V_{\text{Ref-e}}}$$

The value of e equals the offset voltage of the operational amplifier. V_{out} is then proportional to IR_x .

In Figure 9-16 (b), a floating amplifier is used as a unity gain amplifier with high internal feedback. As such, it establishes $V_{\text{Ref-e}}$ across R and also generates a current through R_x . This current equals:

$$I = \frac{V_{\text{Ref-e}}}{R}$$

The current which flows in the loop (I_1) can be ignored since the input impedance of the amplifier is extremely high.

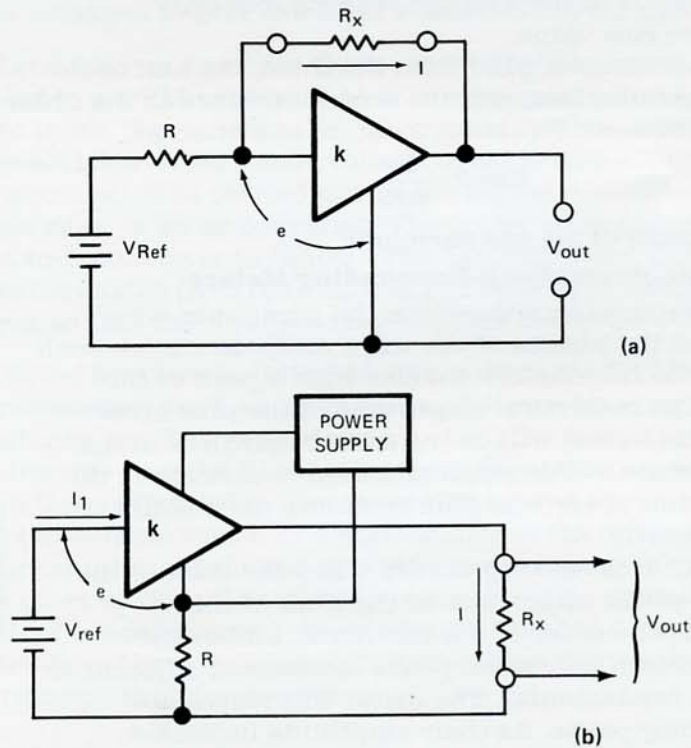


Figure 9-16. Two common techniques used for ohms-to-dc conversion. Each of these techniques depends on the precision of I and the value of R .

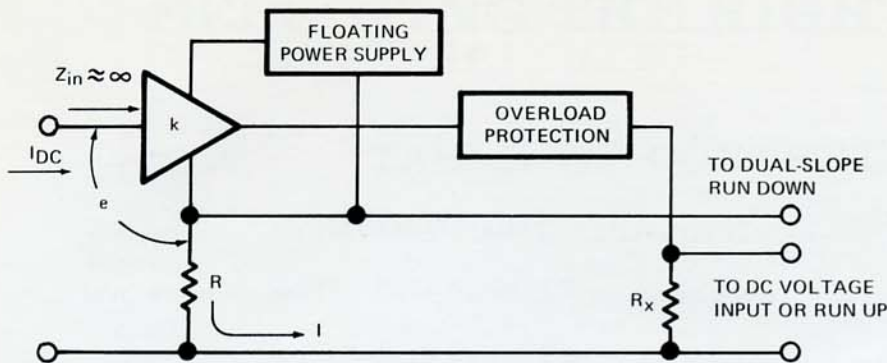
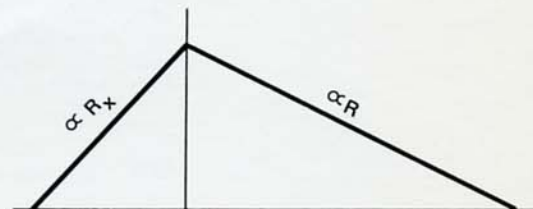


Figure 9-17. Diagram of an ohms-to-dc converter used in a dual-slope DVM. Accuracy is primarily dependent on the value of R due to the use of a ratio technique to determine R_x .



$$\text{DVM Reading} = \frac{R_x}{R}$$

If R is scaled to equal 1, the reading will equal R_x .

Figure 9-18.

The ohms converter in a dual-slope DVM makes its ohms-to-dc conversion using a ratio technique. This eliminates sources of error found in other types of converters.

For both cases shown in Figure 9-16, if V_{out} is measured by the normal dc circuits within the DVM to determine R_x , the current through R_x must be precisely known. This means that the measurement depends on the accuracy of V_{Ref} and R and that the error voltage, e, of the amplifier must approach zero.

If the DVM uses the dual-slope conversion technique, another approach may be used. This approach is illustrated in Figure 9-17 and is not dependent on a precision voltage source nor a precision amplifier. The current out of amplifier K through R is given by:

$$I = \frac{R_{Ref} \cdot e}{R}$$

The gain of K is large. The voltage generated across the unknown resistor is given by:

$$V_{RX} = IR_x = \frac{V_{Ref} \cdot e}{R} R_x$$

The voltage across R is used as the reference during dual-slope rundown as shown in Figure 9-18. The reading equals a ratio:

$$\frac{V_{RX}}{V_{Ref-e}} = \frac{R_x}{R} = \text{DVM Reading}$$

This ratio does not depend on the accuracy of the voltage source or amplifier gain. The value of R can be scaled to make the reading equal R_x . Accuracy depends primarily on R and the short term stability of the voltages and dual-slope A-to-D converter.

Based on:

Kay, Bill and Harmon, Jerry L., "Twelve Functions in a New Digital Meter," Hewlett-Packard Journal, March 1969.



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