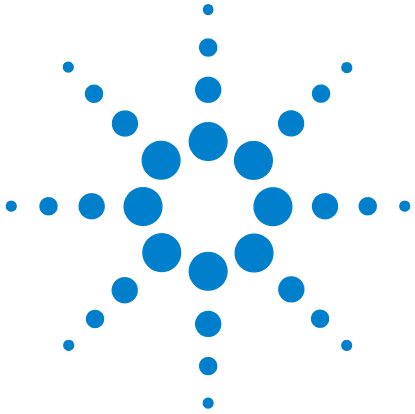

Agilent 16850 Series Portable Logic Analyzers

Service Guide

Agilent Technologies

Notices

Manual Part Number

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Agilent Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

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The Agilent 16850 Series Logic Analyzers—At a Glance

The Agilent Technologies 16850 Series logic analyzers are standalone benchtop logic analyzers that range from 34 to 136 logic acquisition channels depending on the model.

Model Comparison

Table 1 Model comparisons

Agilent model number	16851A	16852A	16853A	16854A
Logic acquisition channels	34	68	102	136

Features, Logic Acquisition

- 2 M to 128 M memory depth per channel (depending on memory option), software upgradeable.
- 350 MHz or 700 MHz maximum state clock rate (depending on state speed option), software upgradeable.
- Full Channel Timing Mode at 2.5 GHz sampling with 12.5 GHz Timing Zoom.
- Half Channel Timing Mode at 5.0 GHz sampling with 12.5 GHz Timing Zoom
- *Eye scan* (automatic threshold and sample position setup) feature.
- 12.5 GHz (80 ps sample resolution) timing zoom with 256 K samples memory depth.

Features, Mainframe

- Built-in 15 inch TFT color LCD display, 1,024 x 768 (XGA) resolution.
- Removable hard drive.
- 10/100/1000 Base-T LAN port.
- USB 2.0 ports (six total, two on front, four on back).

- One PCI Express x4 expansion slot.
- Windows 7 operating system.
- *Agilent Logic and Protocol Analyzer* application which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window.

Supplied Accessories

- USB mouse
- USB keyboard
- Accessory pouch and power cord

Optional Accessories

- Probes

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and returning it to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

Contacting Agilent Technologies

To locate a sales or service office near you, go to www.agilent.com/find/contactus.

In this Service Guide

This book is the service guide for the 16850 Series logic analyzers and is divided into seven chapters.

Chapter 1, “General Information” contains information about the instrument including accessories, specifications and characteristics, and a list of the equipment required for servicing the instrument.

Chapter 2, “Preparing for Troubleshooting or Performance Testing” tells how to prepare the instrument for use.

Chapter 3, “Testing 16850 Series Performance” gives instructions on how to test the performance of the instrument.

Chapter 4, “Calibrating and Adjusting” contains calibration instructions for the instrument.

Chapter 5, “Troubleshooting” contains self-tests and flowcharts for troubleshooting the instrument.

Chapter 6, “Repairing or Replacing a 16850 Series Logic Analyzer” describes how to replace the instrument and assemblies of the instrument, and how to return these to Agilent Technologies.

Chapter 7, “Replaceable Parts” lists replaceable parts, shows exploded views, and gives ordering information.

Document Revision History

Table 2 Revision History

Revision	Reason
16850-97014, October, 2013	First edition.

Contents

1 General Information

This chapter contains information on accessories, specifications, characteristics, and recommended test equipment.

See the 16850 Series logic analyzer's online help for a full listing of all specifications and characteristics.

Accessories

One or more of the following accessories, sold separately, are required to operate the 16850 Series logic analyzers.

Table 3 Logic Analyzer Accessories Available

Accessories	Agilent Part Number
34-channel single-ended data, differential clock, direct connect	U4303A
34-channel single-ended data and clock, direct connect (Mictor)	U4305A
34-channel single-ended data, differential clock, direct connect Soft Touch pro series	U4304A
17-channel single-ended probe for 90 pin LA pod	E5382A
17-channel differential probe for 90 pin LA pod	E5381A
34-channel single-ended probe (Mictor)	E5380A
34-channel single-ended probe for 90 pin LA pod (Samtec)	E5378A
17-channel differential probe for 90 pin LA pod (Samtec)	E5379A
34-channel single-ended for 90 pin LA pod (Soft Touch pro series)	E5406A
Soft Touch pro series: 17-channel differential for 90 pin LA pod	E5405A
17-channel single-ended for 90 pin LA pod (Half-Size Soft Touch)	E5398A
17-channel differential for 90 pin LA pod (Soft Touch classic series)	E5387A
34-channel single-ended for 90 pin LA pod (Soft Touch classic series)	E5390A
34-channel 90 pin logic analyzer cable for use with E5xxxA Adapters	U4201A

Specifications

The specifications are the performance standards against which the product is tested.

Specifications		
Parameter	**Base option**	**Option 700**
Maximum state data rates (using both edges of clock)	700 Mb/s	1.4 Gb/s

Characteristics

The following characteristics are not specifications, but are typical characteristics for the 16850 Series logic analyzers.

Electrical

Power Requirements

100- 240V ± 10%, 50/60Hz, 400 W max

NOTE The mains supply voltage fluctuations are not to exceed ± 10 % of the nominal supply voltage.

CAT II (Line voltage in appliance and to wall outlet).

Pollution degree 2.

Trigger In

The Trigger In Input Signal Level is ± 5 V max.

Clock In

The Clock In connector is 5.5V Max pk and DC, CAT I (line isolated).

Probes

Maximum Input Voltage: ± 40 V, CAT I, CAT I = Category I, secondary power line isolated circuits.

Operating Environment (for indoor use only)

Table 4 Operating Environment Characteristics

Temperature	All 16850 models - 5°C to 40°C (41°F to 104°F) Probes/cables: 0° to + 65° C (+32° to +149° F).
Humidity	80% to temperatures up to 31°C decreasing linearly to 50% rH at 40°C; /// max 80% rh, non-condensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board.
Altitude	2000 m (6,561 ft)
Vibration	Operating: random vibration 0-500 Hz, 10 minutes per axis, 0.3 g (rms).

Non-Operating Environment

Store or ship the instrument in environments within the following limits:

Table 5 Non-Operating Environment Characteristics

Temperature	Temperature -40°C to +75°C (-40°F to 167°F). Protect the system from temperature extremes which cause condensation on the instrument.
Humidity	Humidity up to 90% at 65° C (149°F)
Altitude	Altitude up to 3,000 meters (10,000 feet)
Vibration	Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.5 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.
	Indoor use only. Pollution Degree 2. Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation may occur.

Dimensions

The following table provides dimensions for the 16850 Series logic analyzer unit in inches.

Table 6 16850 Series Logic Analyzer Dimensions

Height	12 inches
Wdith	17.5 inches (19.4 inches with the cables attached)
Depth	18 inches

Weight

Table 7 16850 Series Logic Analyzer Weight

Max Net	Max Shipping
15.0 kg (33.0 lbs)	21.7 kg (48 lbs)

2
Preparing for Troubleshooting or Performance Testing

To inspect the logic analyzer

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

WARNING **Hazardous voltages exist in this instrument. To avoid electrical shock, do not apply power to a damaged instrument.**

2 Check the supplied accessories.

Accessories supplied with the logic analyzer are listed on page 4.

3 Inspect the product for physical damage.

Check the logic analyzer and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement. Contact information is located on page 4.

To apply power

1 Connect the supplied power cord to the instrument and to the power source.

This instrument autodetects the line voltage from 100 VAC to 240 VAC. It is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the model ordered and the country of destination. Refer to "System Replaceable Parts List" on page 89 for more information on power cables.

2 Turn on the power switch located on the front panel.

For first-time power up considerations and setup steps, refer to the *Installation Guide* that came with your instrument. To get the most up-to-date installation guide:

- Go to www.agilent.com.

- Search for 16850 Series Logic Analyzers.
- Look under Technical Support and then Document Library.

To clean the instrument

If the instrument requires cleaning:

1. Remove power from the instrument.
2. Clean the external surfaces of the instrument with a soft cloth dampened with water.
3. Make sure that the instrument is completely dry before reconnecting it to a power source.

To start the user interface

Start the *Agilent Logic and Protocol Analyzer* application from the Start menu or using a shortcut. On the desktop, the Agilent Logic Analyzer icon looks like:

Refer to the *Agilent Logic and Protocol Analyzer* application's on-line help for information on how to operate the user interface.

To test the logic analyzer

- If you require a test to verify the logic analyzer's performance with specifications, refer to "Testing 16850 Series Performance" on page 19."
- If you require a test to verify correct module operation, refer to "Perform the Self-Tests" on page 22.
- If the logic analyzer does not operate correctly, refer to "Troubleshooting" on page 55.

3
Testing 16850 Series Performance

This chapter describes how to test the performance of the 16850 series logic analyzers against the specifications listed on page 11.

To ensure the 16850 series logic analyzers is operating as specified, software tests (self- tests) and a manual performance test are done. The logic analyzer is considered performance- verified if all of the software tests and the manual performance test have passed.

The specifications for the 16850 series logic analyzer define a maximum state data rate at which data can be acquired in state mode. The manual performance test (maximum state data rate test) verifies that the logic analyzer meets these specifications.

Test Strategy

Only specified parameters are tested. Specifications are listed on page 11. The test conditions defined in this procedure ensure that the specified parameter is as good as or better than specifications. Not all channels of the logic analyzer will be tested; a sample of channels is tested. The calibration laboratory may choose to elaborate on these tests and test all channels at their discretion.

Eye Scan is used to adjust the sampling position on each channel tested. Eye scan must be used to achieve maximum state data rate performance.

The 700 Mb/s (1.4 Gb/s for Option 700) state logic analyzer will be tested. All pods will be tested, one pod at a time.

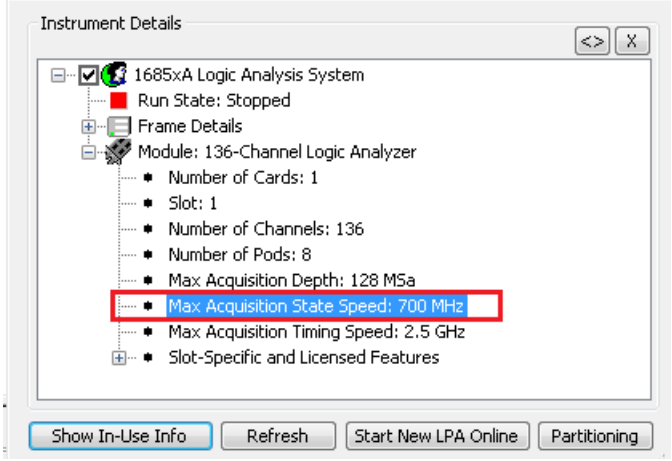
NOTE

You can easily determine whether or not Option 700 is active using the Agilent Notification Center icon. This icon is displayed as a green dot on the taskbar (lower, right-hand corner of your desktop) if the Agilent Logic and Protocol Analyzer GUI is installed. If the GUI is open and running, the Notification Center icon changes to .

1. Right-click the Notification Center icon and select **Show Instrument Details** from the displayed menu.

2. In the Instrument Details dialog box, expand the **Module: <n>-Channel Logic Analyzer** node.

3. Note the entry that specifies the State Speed (for example): **Max Acquisition State Speed: 700 MHz**.



This helps you determine the maximum speed at which you need to perform the State Acquisition tests.

The logic analyzer acquires data on both edges of the clock, so the test frequency is set to half of the acquisition speed.

Test Interval

Test the performance of the 16850 module against its specifications at two-year intervals.

Test Record Description

A Performance Test Record for recording the results of each procedure is provided in this chapter. You may want to make copies of this, and fill-in a copy each time you test the module.

Test Equipment

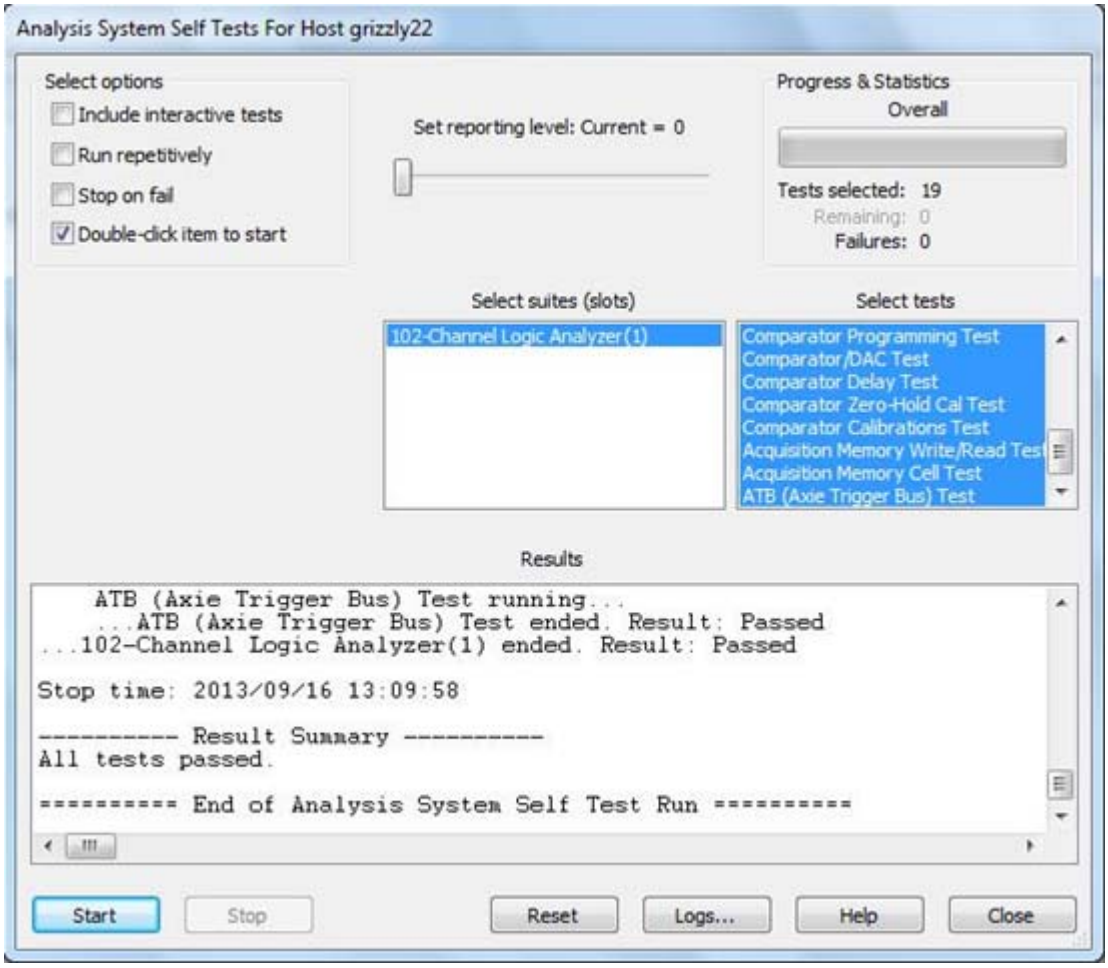
A list of the recommended test equipment is provided. You can use any equipment that satisfies the specifications given. However, the instructions are written with the presumption that you are using the recommended test equipment.

Perform the Self-Tests

Once you have connected all the hardware components for the 16850 logic analyzer, you are ready to run the self tests on the 16850 logic analyzer.

1 Before performing the self-tests, disconnect all probes from the logic analyzer.

2 Select **Help->Self-Test...** from the main menu. The **Analysis System Self Tests** window will appear.



3 In the **Select suites** list, select the logic analyzer. Then, select **All** in the **Select tests** list.

4 Select **Start**. This will perform a complete system self-test.

The progress of the self tests is displayed in the **Results** area of the window.

5 When the self-tests are complete, check the Results window to ensure that the Result Summary indicates that

all tests have passed. If all tests did not pass, refer to "To use the system troubleshooting flowcharts" on page 56.

6 Select the **Close** button to close the Analysis System Self Tests window.

7 If all self-tests pass, then record "PASS" in the "Logic Analysis System Self-Tests" section of the Performance Test Record (page 51).

Equipment Required for the Performance Test

The following equipment is required for the performance test procedure.

Table 8 Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	≥ 800 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Agilent 81134A or equivalent
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset=1V, ΔV=250 mV.) Required for 81134A or 8133A opt. 003.	Agilent 15435A
Flying Lead Probe Set (Qty 2)	A combination of U4201A and E5382A can be used.	Agilent U4203A
SMA/Flying Lead test connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 4)	no substitute	See "Assemble the SMA/Flying Lead Test Connectors" on page 24

Assemble the SMA/Flying Lead Test Connectors

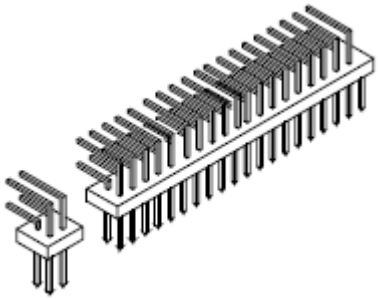
The SMA/Flying Lead test connectors provide a high-bandwidth connection between the logic analyzer and the test equipment. The following procedure explains how to fabricate the four required test connectors.

Table 9 Materials Required for SMA/Flying Lead Test Connectors

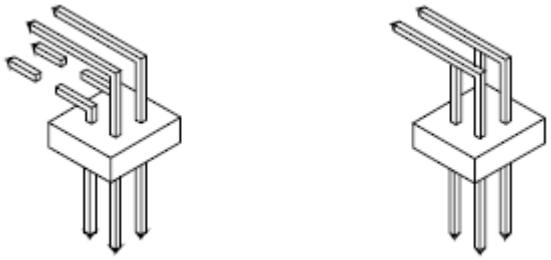
Material	Critical Specification	Recommended Model/Part
SMA Board Mount Connector (Qty 8)		Emerson 142-0701-801 (see www.emersonconnectivity.com)
Pin Strip Header (Qty 1, which will be separated)	0.100" X 0.100" Pin Strip Header, right angle, pin length 0.230", two rows, 0.120" solder tails, 2 X 40 contacts	3M 2380-5121TN or similar 2- row with 0.1″ pin spacing
SMA 50 ohm terminators (Qty 4)	Minimum bandwidth 2 GHz	Emerson 142-0801-866 50 ohm Dummy Load Plug
SMA m-m adapter (Qty 4)		Emerson 142-0901-811 SMA Plug to Plug or similar

1 Prepare the pin strip header:

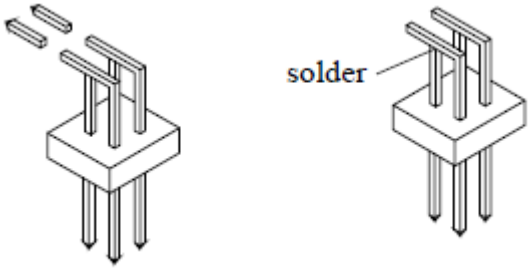
a Cut or cleanly break a 2 x 2 section from the pin strip.



b Trim about 1.5 mm from the pin strip inner leads and straighten them so that they touch the outer leads.



c Trim about 2.5 mm from the outer leads.

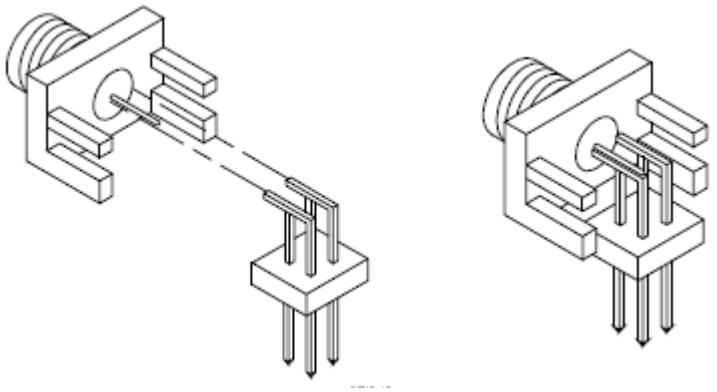


d Using a very small amount of solder, tack each inner lead to each outer lead at the point where they are touching.

2 Solder the pin strip to the SMA board mount connector:

a Solder the leads on the left side of the pin strip to the center conductor of the SMA connector as shown in the diagram below.

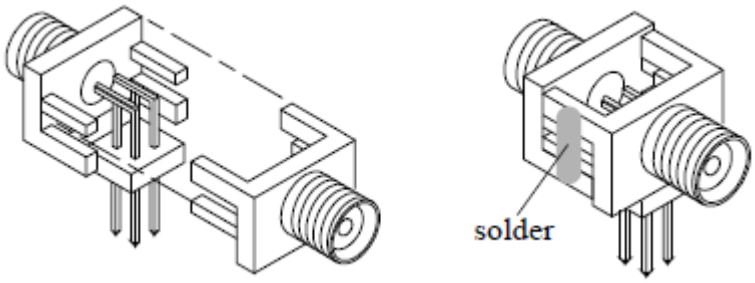
b Solder the leads on the right side of the pin strip to the inside of the SMA connector's frame as shown in the diagram below. Use a small amount of solder.



3 Attach the second SMA board mount connector:

a Re-heat the solder connection made in the previous step, and attach the second SMA connector, as shown in the diagram below. Note that the second SMA connector is upside-down, compared to the first. Add a little solder to make a good connection.

b Solder the center conductor of the second SMA connector to the center conductor of the first SMA connector and the leads on the left side of the pin strip.



c Rotate the assembly 180 degrees and solder the two SMA board mount connector frames together.

4 Check your work:

a Ensure that the following four points have continuity between them: The two pins on the left side of the pin

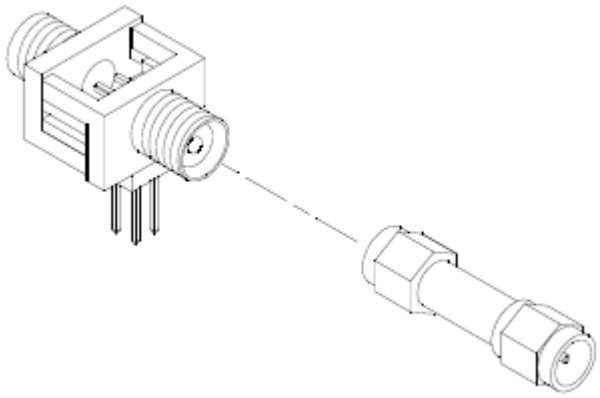
strip, and the center conductors of each SMA connector.

b Ensure that there is continuity between each of the two pins on the right side of the pin strip, and the SMA connector frames.

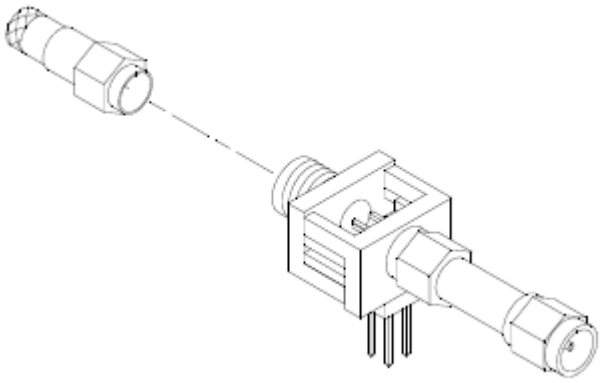
c Ensure that there is NO continuity between the SMA connector center conductor and the SMA connector frame (ground).

5 Finish creating the test connectors:

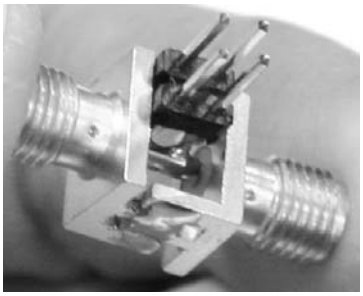
a Attach an SMA m-m adapter to one end of each of the four SMA/Flying Lead test connectors.



b Attach a 50 ohm terminator to the other end of the four SMA/Flying Lead test connectors.



The finished test connector is shown in the pictures below.

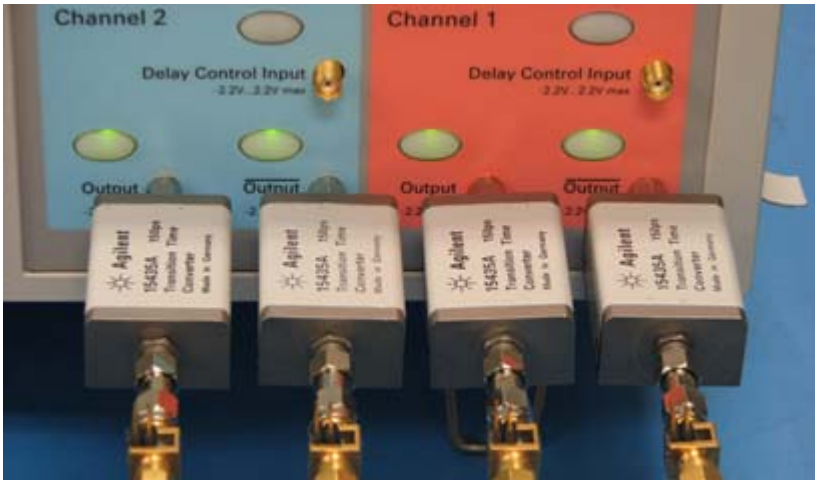


Set Up the Test Equipment

This section explains how to set up the test equipment for the maximum state data rate test.

1 Connect Transition Time Converters (if required - see page 23) to each of the four outputs of the pulse generator: Channel 1 OUTPUT, Channel 1 Output, Channel 2 OUTPUT, Channel 2 Output.

2 Connect the four SMA/Flying Lead test connectors (see "Assemble the SMA/Flying Lead Test Connectors" on page 24) with 50 ohm terminators to the Transition Time Converters on the 4 pulse generator outputs. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)



3 Turn on the Pulse Generator. Let the entire set of test equipment and logic analyzer warm up for 30 minutes before beginning any test.

4 Load the default configuration into the 81134A Pulse Generator.

- Select Main
- Click Recall
- Press 0

5 Set up the pulse generator according to the following.

a Set the frequency of the pulse generator:

In this test procedure, the logic analyzer uses both edges of the clock to acquire data. The test frequency is half the test clock rate because data is acquired on both the rising edge and falling edge of the clock. Set the frequency to:

- 350 MHz plus 2% (357 MHz) for the Base option.
- 700 MHz plus 2% (714 MHz) for Option 700.

This includes the frequency uncertainty of the pulse generator, plus a test margin.

If you are using an 81134A pulse generator, the frequency accuracy is ±0.005% of setting.

b Set the rest of the pulse generator parameters to the values shown in the following table.

Table 10 81134A Pulse Generator Setup

Main	Channel 1	Channel 2	Trigger
Mode: Pulse/Pattern	Mode: Square ÷ 1	Mode: Square ÷ 1	Disable
Freq: set in previous step.	**Timing**	**Timing**	
Clock Internal	Delay Ctrl Input Off	Delay Ctrl Input Off	
	Delay 0 ps	Delay 0 ps	
	Pulse Perf: Normal	Pulse Perf: Normal	
	Deskew: 0 ps	Deskew: 0 ps	
	Levels: Normal, Custom	**Levels: Normal, Custom**	
	Ampl: 450 mV	Ampl: 450 mV	
	Offset: 0 mV	Offset: 0 mV	
	Term Voltage: 0 mV	Term Voltage: 0 mV	
	Limit to current Levels: unselected	Limit to current Levels: unselected	
	Output: Enable (LED on)	Output: Enable (LED on)	
	$\overline{\text{Output}}$: Enable (LED on)	$\overline{\text{Output}}$: Enable (LED on)	

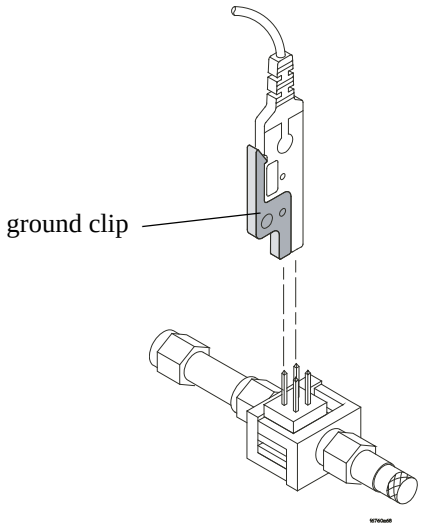

Mode
Pulse/Pattern
Freq
714.000000 MHz
Period
1.40056022 ns
Clock
Internal
Clock In
Start In
Trig Out
Ch 2
Square
Ch 1
Square
Channel 1
Square
Freq. Divider
1
Out
Out_
Ch 2
Timing
Delay Ctrl Input Off
Delay
0 ps
DCycle
50 %
Pulse Perf.
Normal
Deskew
0 ps
Levels
Normal
Custom
Ampl
450 mV
Offset
0 mV
Term. Voltage
0 mV
Limit to current Levels
Main
Channel
Data
Aux
Config

Connect the Test Equipment

Connect the Logic Analyzer Pod to the Pulse Generator

1 Connect one U4203A Flying Lead Probe Set to Pods 1/2 of the 16850 series logic analyzer.

2 Connect the Pod 1 U4203A Flying Lead Probe Set's CLK lead to the pin strip of the SMA/Flying Lead connector at the pulse generator's Channel 1 OUTPUT.



NOTE Be sure to use the black ground clip (supplied with the U4203A Flying Lead Probe Set) and orient the leads so that the black clip is connected to one of the SMA/Flying Lead connector's ground pins!

3 Connect the Pod 1 U4203A Flying Lead Probe Set's $\overline{\text{CLK}}$ lead to the SMA/Flying Lead connector at the pulse generator's Channel 1 $\overline{\text{Output}}$. Again, be sure to use the black ground clip and orient the leads so that the black clip is connected to ground.

4 Connect the Pod 1 U4203A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the pulse generator's Channel 2 OUTPUT.

5 Connect the Pod 1 U4203A Flying Lead Probe Set's bits 6 and 14 to the SMA/Flying Lead test connector's pin strip connector at the pulse generator's Channel 2 $\overline{\text{Output}}$.


81134A
Clock Input
Start Input
Trigger Out
Channel 2
Channel 1

Test the 16850 Series Logic Analyzer

The following sections explain how to test the maximum state data rate.

1 Record the logic analyzer's model and serial number in the Performance Test Record (see page 51). Record your work order number (if applicable) and today's date.

2 Record the test equipment information in the "Test Equipment Used" section of the Performance Test Record.

3 Turn on the logic analyzer frame.

NOTE Before testing the performance of the logic analyzer, warm-up the logic analyzer and test equipment for 30 minutes.

---

a Plug in the power cord to the power connector on the rear panel of the logic analyzer frame.

b Connect a key board and a mouse to the frame.

c Press the ON/Standby button on the front panel of the logic analyzer to power on the logic analyzer.

While the logic analyzer is booting, observe for the following:

- Ensure all of the installed memory is recognized.
- Any error messages.
- Interrupt of the boot process with or without error message.

4 During initialization, check for any failures.

If an error or an interrupt occurs, refer to the troubleshooting section.

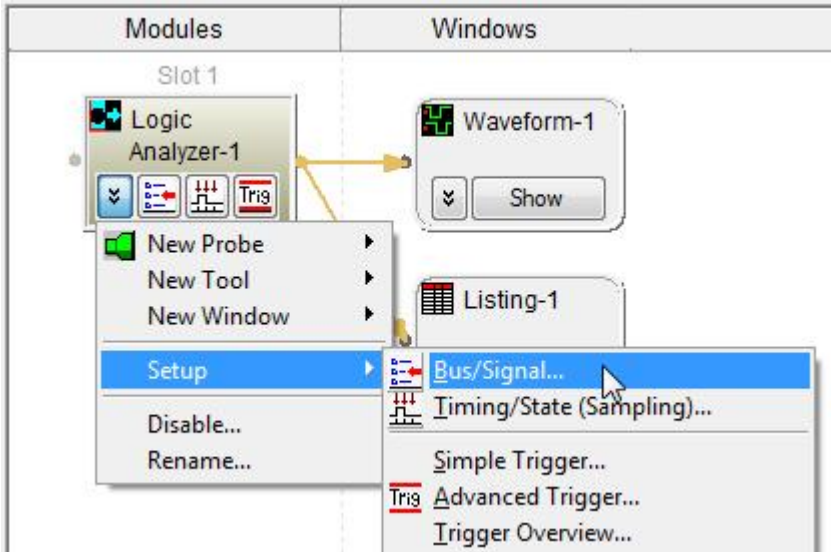
5 Start the Logic and Protocol Analyzer application if it is not already started.

Configure the Logic Analysis System

1 In the *Agilent Logic and Protocol Analyzer* application, choose **File→New**. This puts the logic analyzer into its initial state.

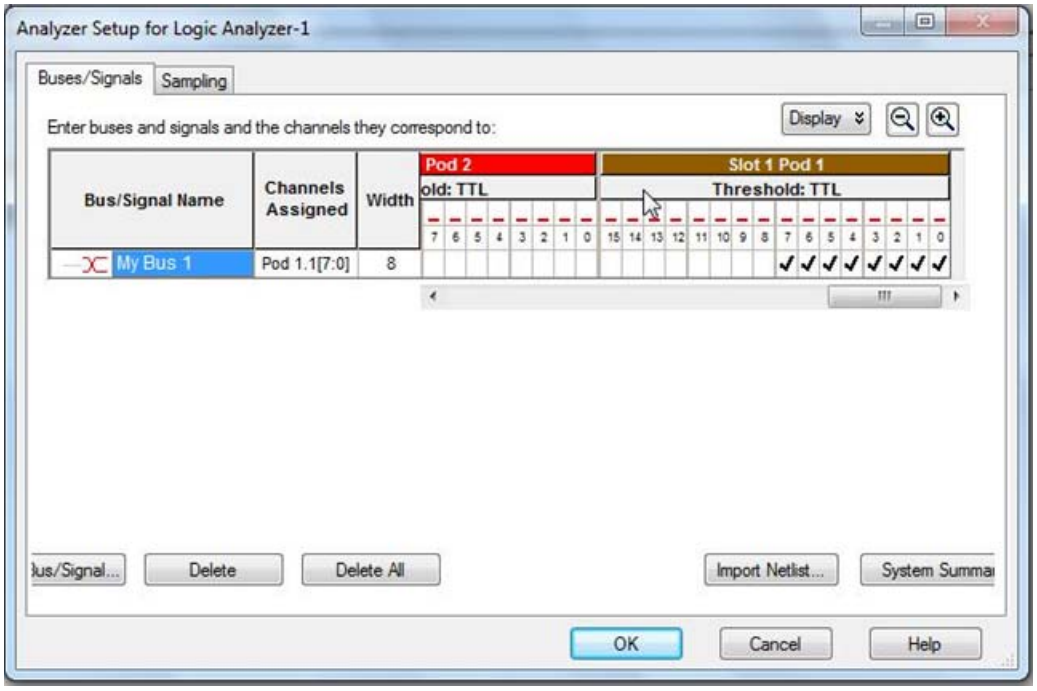
2 Set up the bus and signals:

a In the Overview window, select **Setup→Bus/Signal...** from the logic analyzer's drop-down menu.



NOTE The U4203A probe must be connected to the logic analyzer pod as described on page 32.

b In the **Analyzer Setup** window, choose the **Threshold** button for Pod 1.

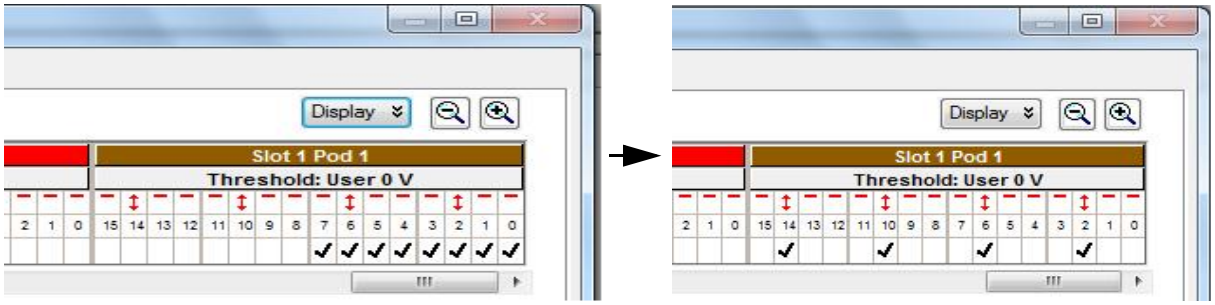


The **Threshold Settings** window appears.

c Set the threshold value for Pod 1 of the logic analyzer to **0 V**. Click **Apply to All Other Pods and Clocks**. Then, click **Done** to close the dialog.

d The activity indicators now show activity on the channels that are connected to the pulse generator. Un-assign all channels. You can do this quickly by

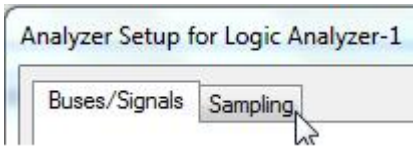
clicking on the left-most check mark and dragging to the right across all of the other check marks.



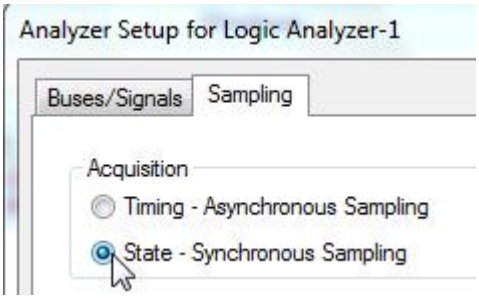
e Click to select channels 2, 6, 10, and 14 as shown in the above picture.

3 Select the State sampling mode and set the State Clock options:

a Select the **Sampling** tab of the Analyzer Setup window.



b Select **State - Synchronous Sampling**.

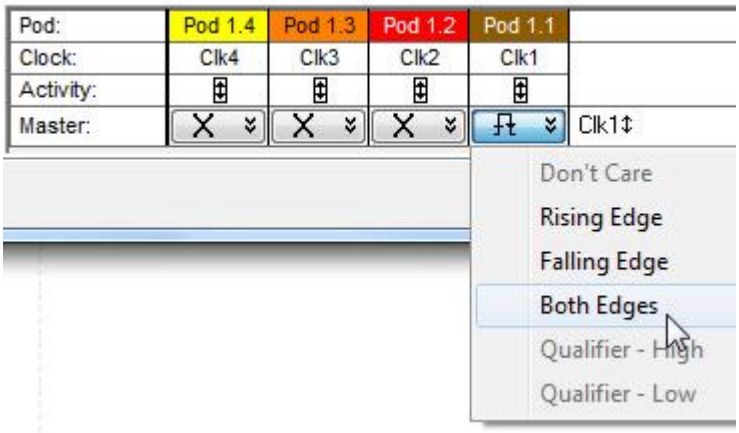


4 Set the trigger position and acquisition memory depth:

a Set the **Trigger Position** to **100% Poststore**.

b Set the **Acquisition Depth** to **128K**.

c Set **Clk1** to **Both edges** clocking. The following screen displays this state clock setting.



d Click **OK** to close the **Analyzer Setup** window.

Determine maximum clock rate

1 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main window.

2 Click the **Run Repetitive** toolbar button to start a repetitive run on the logic analyzer for acquiring data repeatedly.

Acquired data will start appearing in the Listing window.

3 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

4 When the logic analyzer displays an error that the data could not be displayed, decrease the pulse generator frequency by 1 MHz.

5 Close the displayed error dialog by clicking **OK**.

6 Click the **Run Repetitive**  toolbar button.

7 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

8 Click the **Stop**  toolbar button to stop the data acquisition.

Determine PASS/FAIL for the Pulse Generator Frequency test

If you get 100 acquisitions without any error display at a pulse generator frequency (including uncertainty) greater than 350 *MHz* for the base model and 700MHz for the option 700 model, then the logic analyzer passes this portion of the test. For example, a frequency of 720 MHz - 2% uncertainty = 705.6 MHz indicates a PASS result for the test. Record PASS/FAIL result of this test in the "Pulse Generator Frequency Test" section of the Performance Test Record (page 51).

NOTE If any of tests described later in this chapter fail, decrease the pulse generator frequency by 1 MHz and wait for logic analyzer to complete 100 acquisitions at this new pulse generator frequency without displaying any error. Repeat this step until you get 100 acquisitions without any error display.

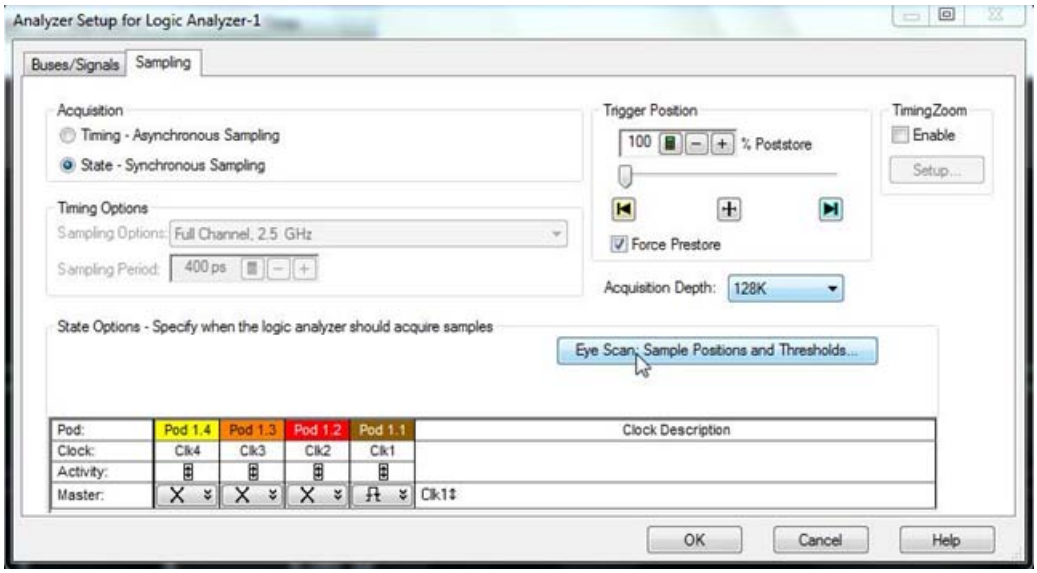
Final pulse generator frequency

If the remaining tests described in this chapter PASS, record the final pulse generator frequency in the "Final Pulse Generator Frequency" section of the Performance Test Record (page 51). Recording this final frequency provides a traceable measurement that is expected to be unique for each 16850 series Logic Analyzer.

Adjust sampling positions using Eye Scan

1 Open the **Sampling** tab in the **Analyzer Setup** window.

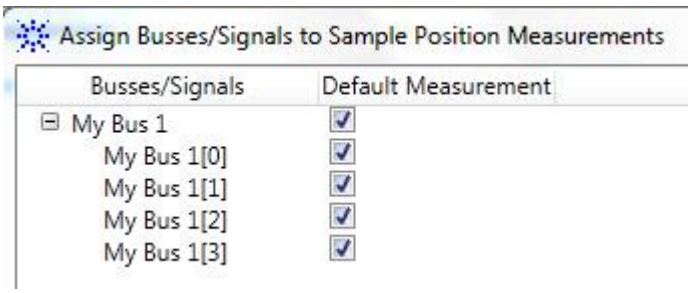
2 Select the **Eye Scan: Sample Positions and Thresholds...** button.



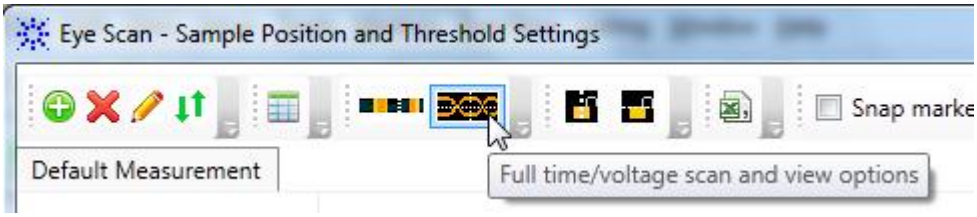
The **Eye Scan - Sample Positions and Threshold Settings** dialog will appear.

3 Click the **Assign Busses/Signals to Measurements** icon.

4 In the **Busses/Signals** section of the dialog, ensure that the checkboxes next to “My Bus 1” and the 4 data bits 0-3 is checked. Then click **OK**.



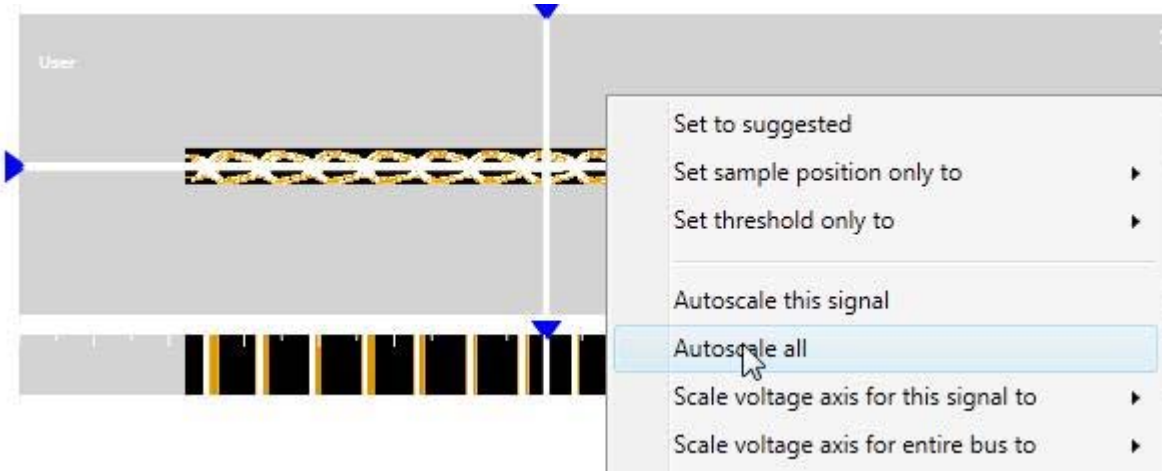
5 Click the **Full time/voltage scan and view options** icon.



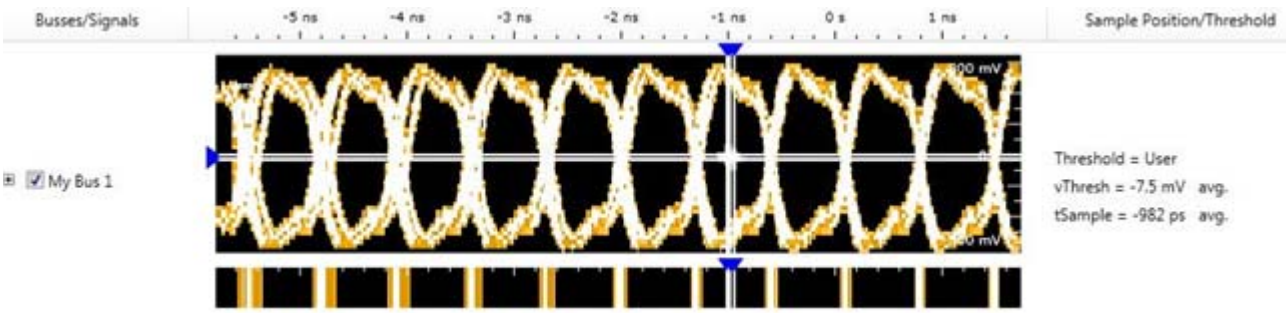
6 From the displayed drop-down list of options, select both the checkboxes - **Do full time/voltage scan** and **Show time/voltage scan**.

7 Run Eye Scan by clicking the **Run This Measurement** button.

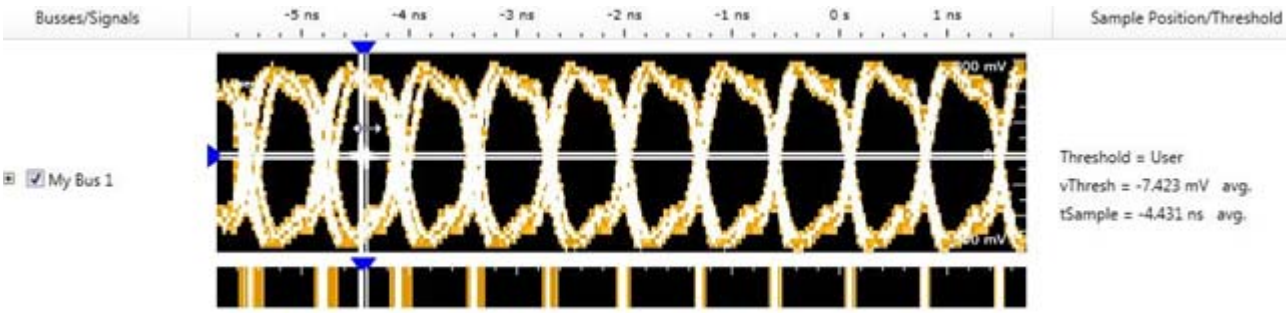
8 If the scan does not fill the scan area, right click in the scan area and select **Autoscale all**.



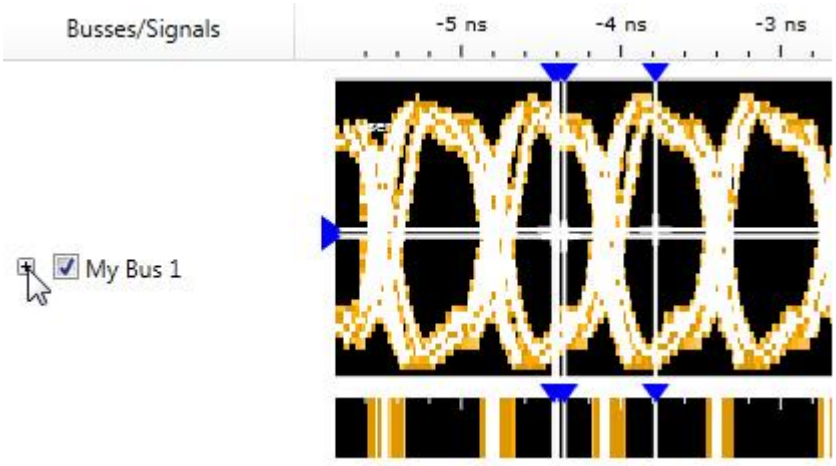
The waveform should now fill the Eye Scan area as displayed below.



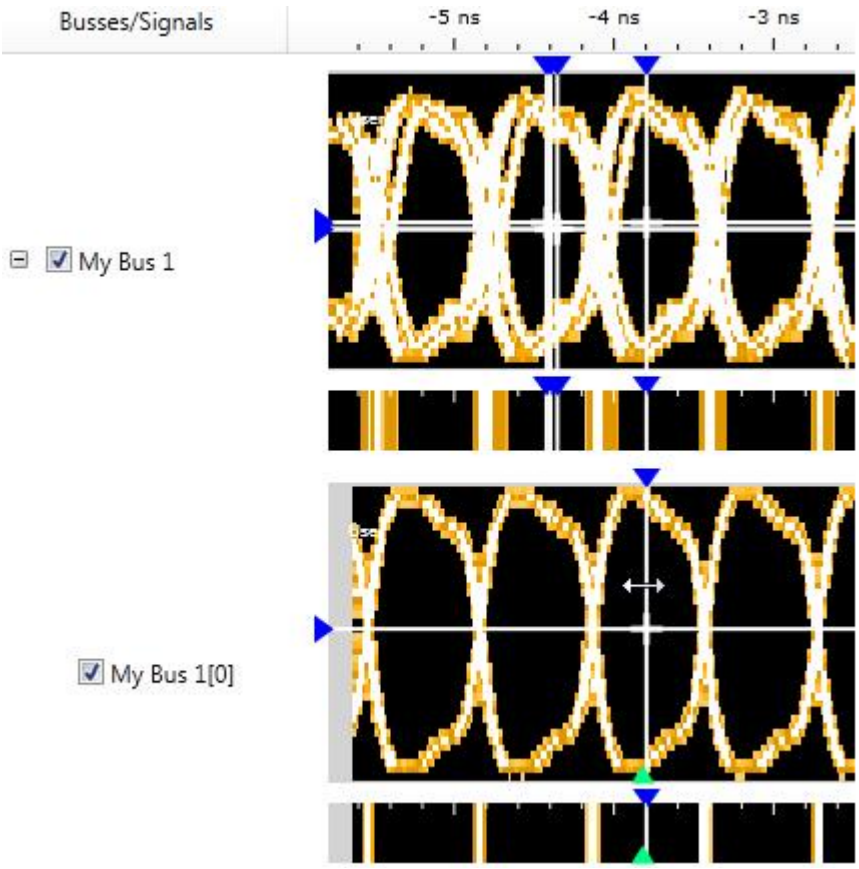
9 Move the sample position of all 4 data bits into the Eye nearest -4.5ns. Using the mouse, grab the vertical lines and move these lines into the correct eye.



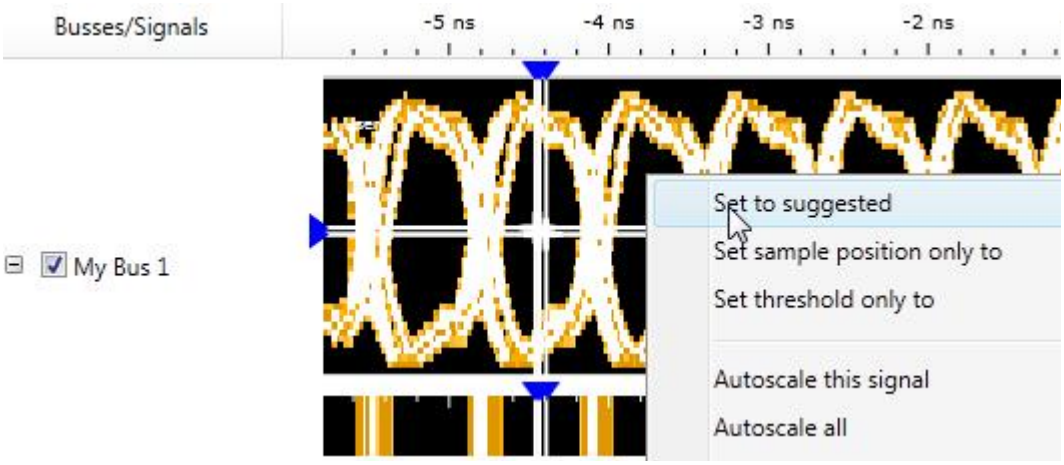
10 If all sample positions are not in the same eye, then click the Plus sign to expand My Bus 1.



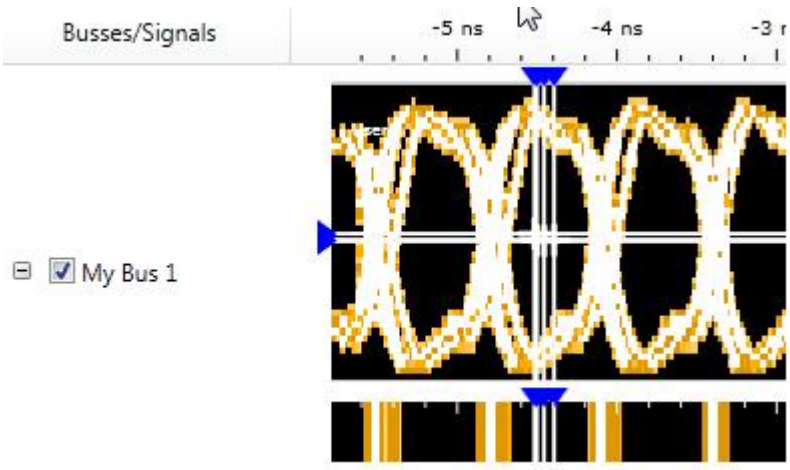
11 Use the mouse to grab the bits that are not in the eye near -4.5 ns. and then drag these into the correct eye.



12 Once all bit sample positions are in the correct eye, right click in the My Bus 1 Scan area and select **Set to Suggested.**



On clicking Set to suggested, all bits should be centered in their own eye near -4.5 ns.



Test Pod 1

The steps that follow include pass/fail criteria.

Determine PASS/FAIL (1 of 2 tests) Eye Scan Location

1 PASS/FAIL: If an eye exists near -4.5 ns for every bit, and Eye Scan places a blue bar in the eye for each bit, then the logic analyzer passes this portion of the test. Record the result in the "Eye Scan locates an eye for each bit" section of the Performance Test Record (page 51).

2 If an eye does not exist near -3.6 ns for every bit or Eye Scan cannot place the blue bar in the eye, then the logic analyzer fails the test. Record the result in the "Eye Scan locates an eye for each bit" section of the Performance Test Record (page 51).

Close the Eye Scan and Analyzer Setup Windows

1 Click **OK** to close the Eye Scan - Sample Positions and Threshold Settings dialog.

2 Click **OK** to close the Analyzer Setup window.

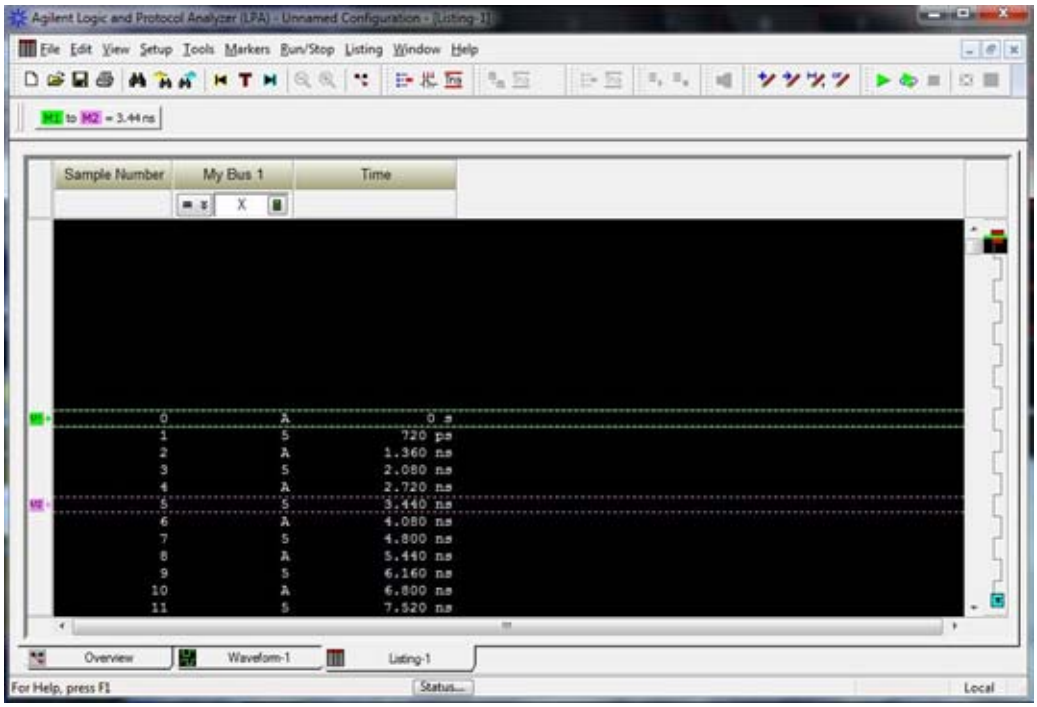
Configure the markers

Data must be acquired before the markers can be configured. Therefore, you need to run the analyzer to acquire data.

1 Switch to the Listing window by selecting the Listing tab at the bottom of the main window.

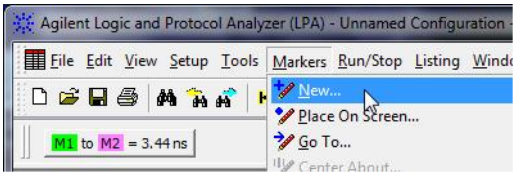
2 Select the Run icon .

3 Data will appear in the Listing Window upon completion of the run.

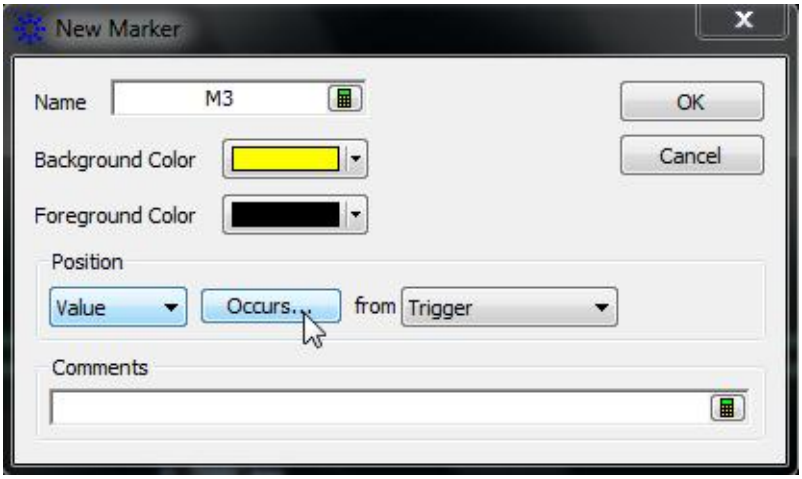


If the data values are not “A”s and “5”s, you may need to set the sampling positions in different eyes.

4 From the Main Menu, choose **Markers→New**.

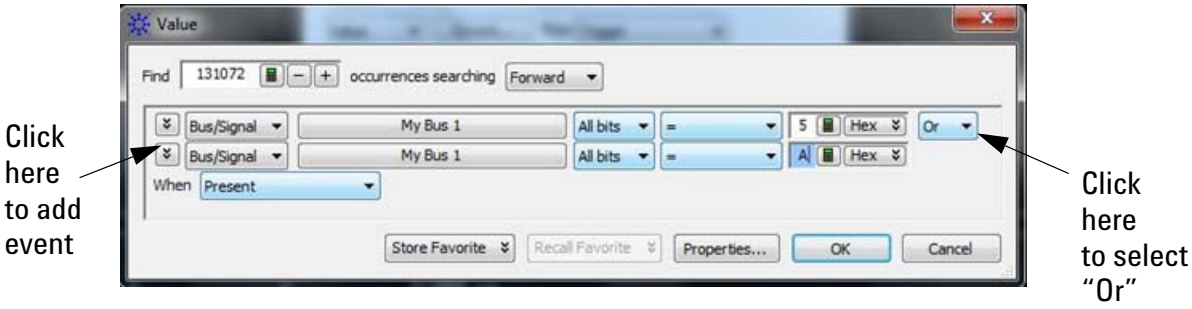


5 You can accept the default name for the new marker.



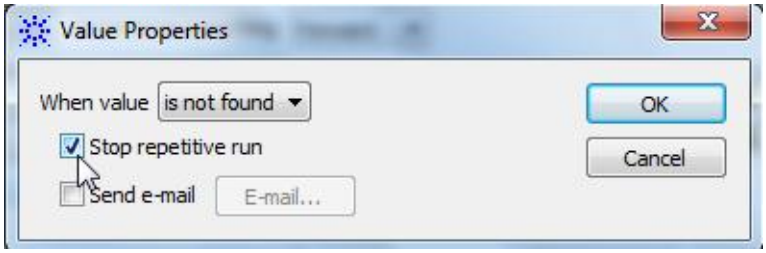
6 Change the **Position** field to **Value**.

7 Select the **Occurs...** button and create the marker setup shown below.



8 In the **Value** window, select the **Properties...** button.

9 In the **Value Properties** window, select **Stop repetitive run** when value is not found.



10 Click **OK** to close the marker's Value Properties window.

11 Click **OK** to close the marker's Value window. The system will search the display for the occurrences specified.

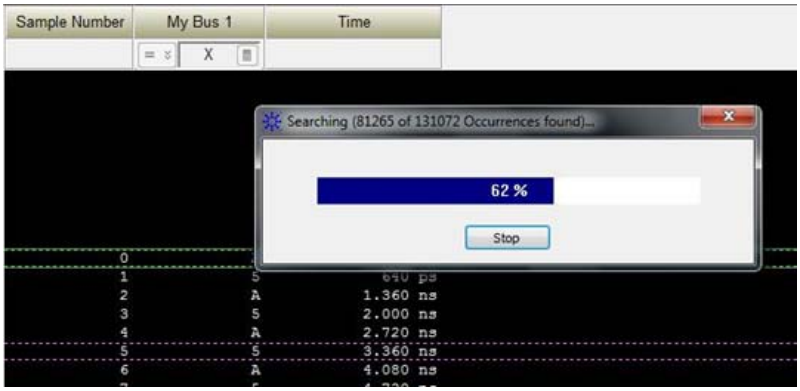
12 Click **OK** to close the New Marker window.

Determine PASS/FAIL (2 of 2 tests) occurrences

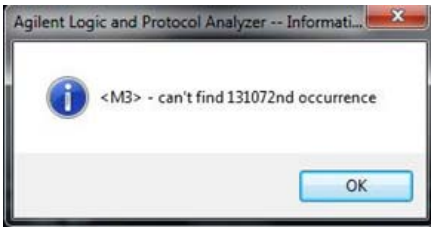
Pass/Fail Point: The Listing window is set up to search for the appropriate number of A's and 5's in the acquisition. If the logic analyzer does not detect the correct number of A's and 5's, an error window will appear.

Record the results in the "correct number of occurrences detected" section of the Performance Test Record.

1 Click the **Run Repetitive** icon  . Let the logic analyzer run for about one minute. The analyzer will acquire data and the Listing Window will continuously update.



If the “can’t find occurrence” window appears, then the logic analyzer fails the test.



Check your test setup. If the failure is not the result of a problem with the test setup, record the failure in the “Correct number of occurrences detected” section of the Performance Test Record.

NOTE Be sure that the black ground clip is making good contact with the ground pin on the test connector.

2 After about one minute, select the **Stop** button  to stop the acquisition.

If the “can’t find occurrence” window does not appear, then the analyzer passes the test. Record “Pass” in the “Correct number of occurrences detected” section of the Performance Test Record.

Test Pod 2

1 Disconnect the U4203A Flying Lead Probe Set Pod1 from channel 2 of the 81134A pulse generator output (Bits 2, 6, 10, 14). Leave the Pod 1 clock connected to channel 1.

2 Connect the probe set from Pod 2 of logic analyzer to the pulse generator channel 2 outputs. (The clock input on Pod 1 remains the clock input when testing Pod 2.)

- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 $\overline{\text{Output}}$

3 In the **Overview** window, select **Setup→Bus/Signal...** from the analyzer's drop-down menu.

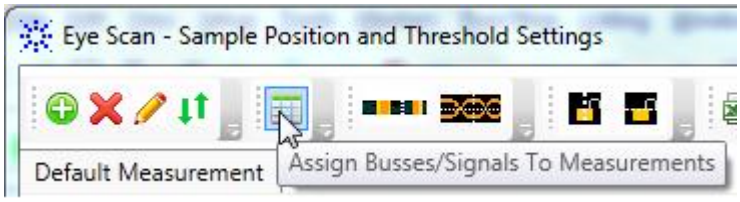
4 Scroll to the right and unassign all Pod 1 bits.

5 Set the Pod 2 threshold to **0 V** (just as you did for Pod 1 on page 36).

6 Assign bits 2, 6, 10, and 14 of Pod 2.

7 Adjust the sampling positions using Eye Scan. Set sample position near -4.5 ns. Realign any stray channels if necessary. See page 40.

8 In **Eye Scan - Sample Positions and Threshold Settings** dialog box, click the **Assign Busses/Signals to Measurements** icon.



9 Determine pass or fail (1 of 2 tests) Eye Scan Location. See page 44.

10 Click **OK** to close the Analyzer Setup window.

11 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main logic analyzer window.

12 Click the **Run Repetitive** icon  .

13 Determine pass or fail (2 of 2 tests)) occurrences. See page 46.

Test Pods 3 (if equipped)

1 Disconnect the U4203A Flying Lead Probe Set Pod2 from channel 2 of the 81134A pulse generator output. Leave the Pod 1 clock connected to channel 1.

2 Connect a second U4203A to the Pod 3/4 connector on the Logic Analyzer frame.

3 Connect the probe set from Pod 3 of logic analyzer to the pulse generator channel 2 outputs. (The clock input on Pod 1 remains the clock input when testing other Pods.)

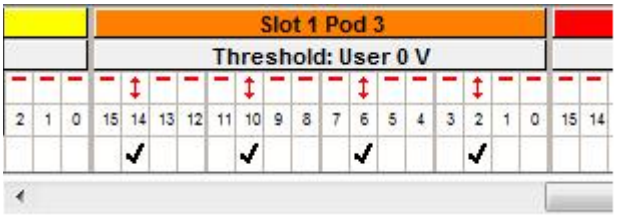
- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 $\overline{\text{Output}}$

4 In the **Overview** window, select **Setup→Bus/Signal...** from the analyzer's drop-down menu.

5 Scroll to the right and unassign all Pod 2 bits.

6 Set the Pod 3 threshold to **0 V**. Apply to All Other Pods and Clocks. (just as you did for Pod 1 on page 36)

14 Assign bits 2, 6, 10, and 14 of Pod 3..



15 Adjust the sampling positions using Eye Scan. Set sample position near -4.5 ns. Realign any stray channels, if necessary. See page 40.

16 In **Eye Scan - Sample Positions and Threshold Settings** dialog box, click the **Assign Busses/Signals to Measurements** icon.

17 Determine pass or fail (1 of 2 tests) Eye Scan Location. See page 44.

18 Click **OK** to close the Analyzer Setup window.

19 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main logic analyzer window.

20 Click the **Run Repetitive** icon  .

21 Determine pass or fail (2 of 2 tests)) occurrences. See page 46.

Other Pods (as needed)

Repeat the above steps for testing pods 4 to 8. Upon completion, the logic analyzer is completely tested.

Conclude the State Mode Tests

Do the following steps to properly shut down the logic analyzer session after completing the state mode tests.

1 End the test.

a From the Main Menu, choose **File→Exit**. At the dialog "Do you want to save the current configuration?" select **No**.

Ending and restarting the logic analysis session will re-initialize the system.

b Disconnect all cables and adapters from the pulse generator.

Performance Test Record

LOGIC ANALYZER MODEL NO. (circle one): 16851A, 16852A, 16853A, 16854A

Logic Analyzer Serial No.	Work Order No.
Date:	Recommended Test Interval - 2 Year/4000 hours
	Recommended next testing:

TEST EQUIPMENT USED

Pulse Generator Model No.	
Pulse Generator Serial No.	
Pulse Generator Calibration Due Date:	

MEASUREMENT UNCERTAINTY

Clock Rate	
Pulse Generator Frequency Accuracy: 81134A: ±0.005% of setting. 2% = uncertainty + at least 1% test margin.	
Base option: 350 MHz + 2% = 357 MHz Option 700: 700 MHz + 2% = 714 MHz	

TEST RESULTS

Logic Analysis System Self-Tests (Pass/Fail):		
Performance Test: Maximum State Data Rate		
Pulse Generator Settings	Freq: Base option: 350 MHz + 2% = 357 MHz Option 700: 700 MHz + 2% = 714 MHz	
	Square wave.	
Pulse Generator Frequency Test (Pass/Fail)		
Final Pulse Generator Frequency		
Test Criteria	Test 1 of 2 Eye Scan locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected
Pod 1 Results (pass/fail)**:**		
Pod 2 Results (pass/fail)**:**		

TEST RESULTS

Pod 3 Results (pass/fail):		
Pod 4 Results (pass/fail):		
Pod 5 Results (pass/fail):		
Pod 6 Results (pass/fail):		
Pod 7 Results (pass/fail):		
Pod 8 Results (pass/fail):		

4
Calibrating and Adjusting

Calibration Strategy

The 16850 series logic analyzer does not require any periodic adjustments or calibration by the user to ensure operational accuracy.

However, Agilent recommends that performance of the 16850 logic analyzer be tested against its specifications at two-years intervals. This testing is required to obtain calibration certification.

You can refer to “Testing 16850 Series Performance" on page 19 to find detailed information on how to test the performance of the 16850 series logic analyzer.

5 Troubleshooting

This chapter provides instructions for troubleshooting a 16850 logic analyzer that is not operating correctly.

The troubleshooting consists of flowcharts, self-test instructions, a cable test, and how to restore system software.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for the 16850 logic analyzer is the replacement of defective assemblies. You can send this logic analyzer to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

Agilent requires that the 16850 logic analyzer unit be repaired only at qualified repair facilities such as the Agilent Repair Centers.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when you perform any troubleshooting procedures to this instrument.

To use the system troubleshooting flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled references on the charts indicate connections with the other flowcharts or other parts within the same flowchart. Start your troubleshooting at the top of the first flowchart (Figure 1 on page 57).

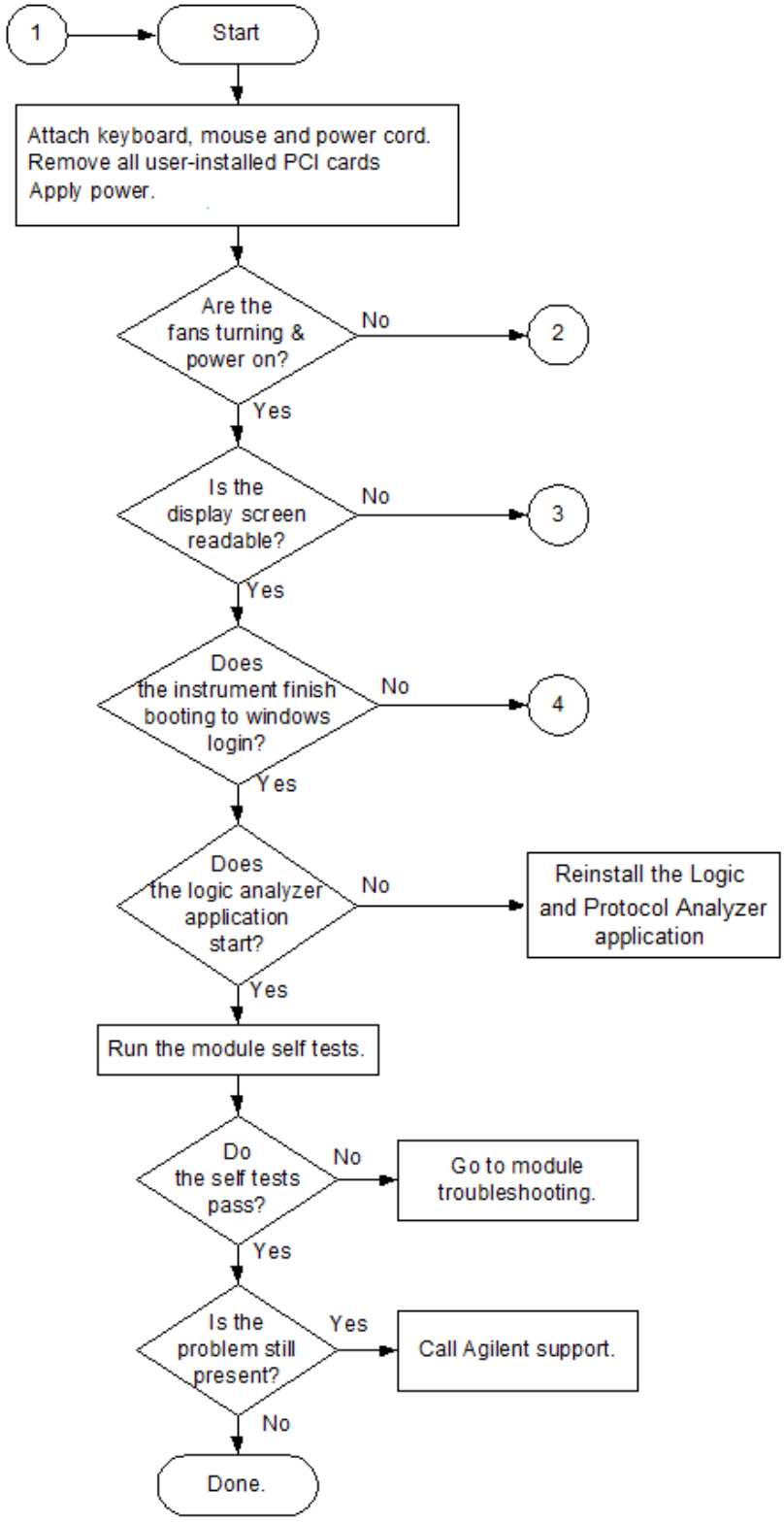


Figure 1 System Troubleshooting Flowchart

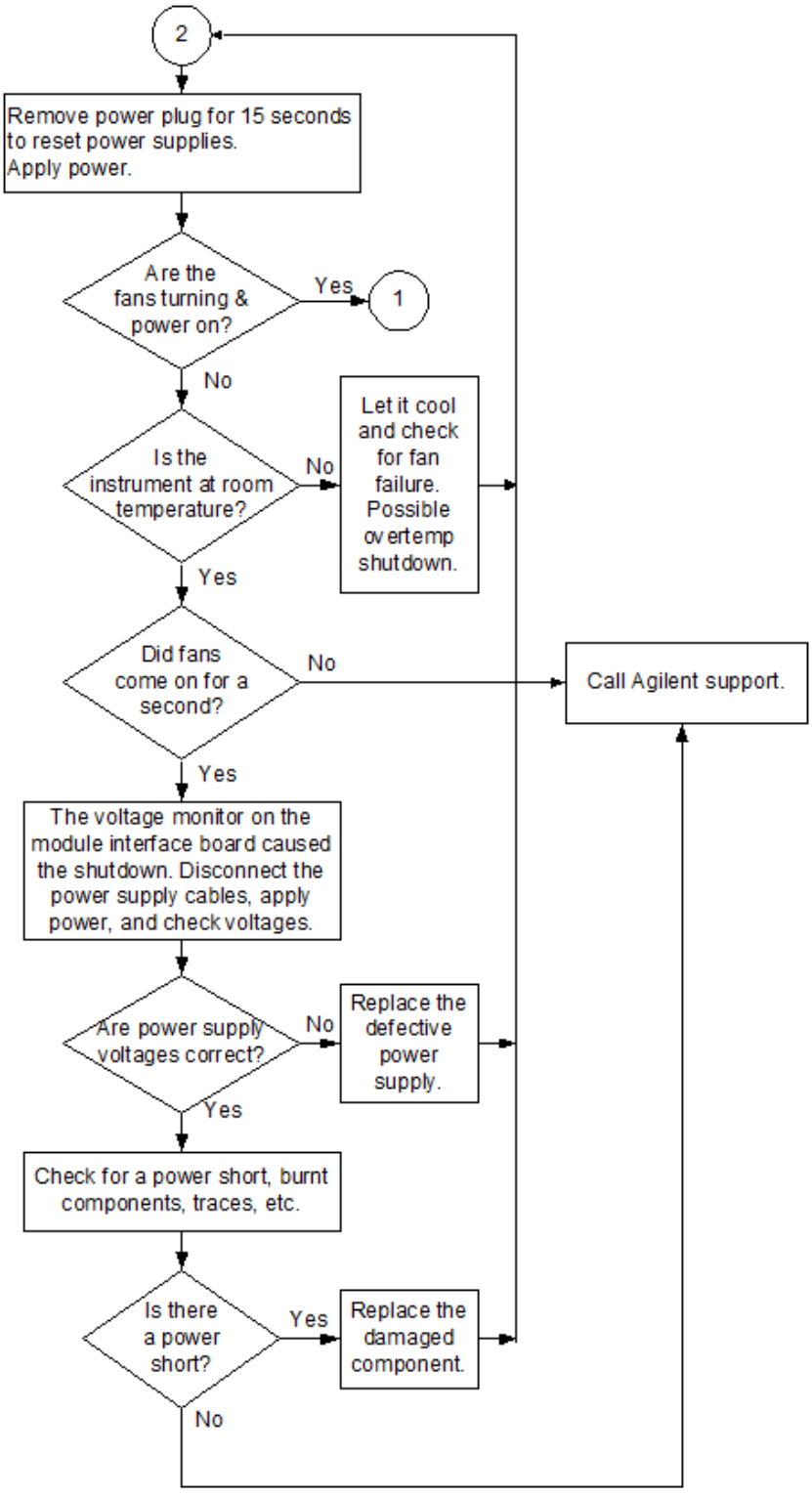


Figure 2 System Power Troubleshooting Flowchart

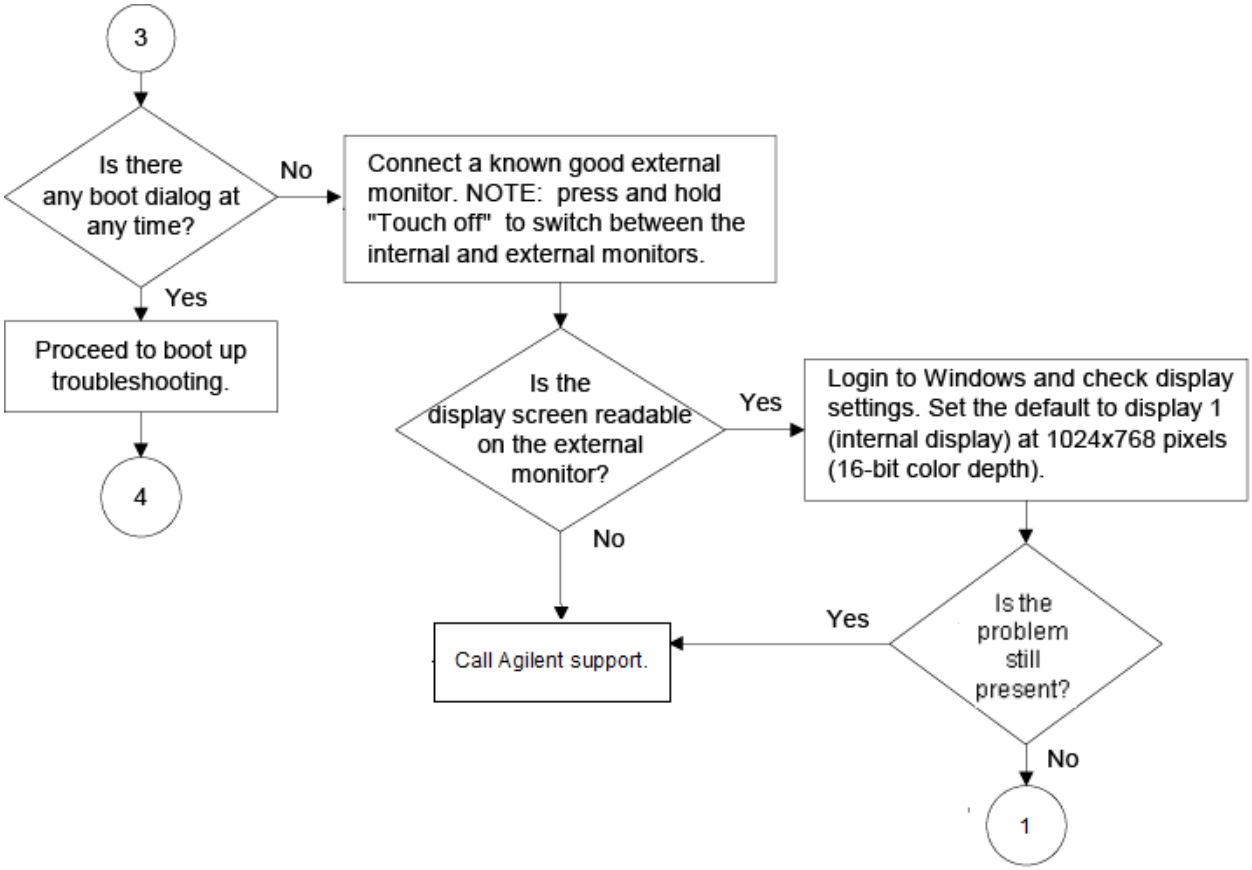


Figure 3 System Display Troubleshooting Flowchart

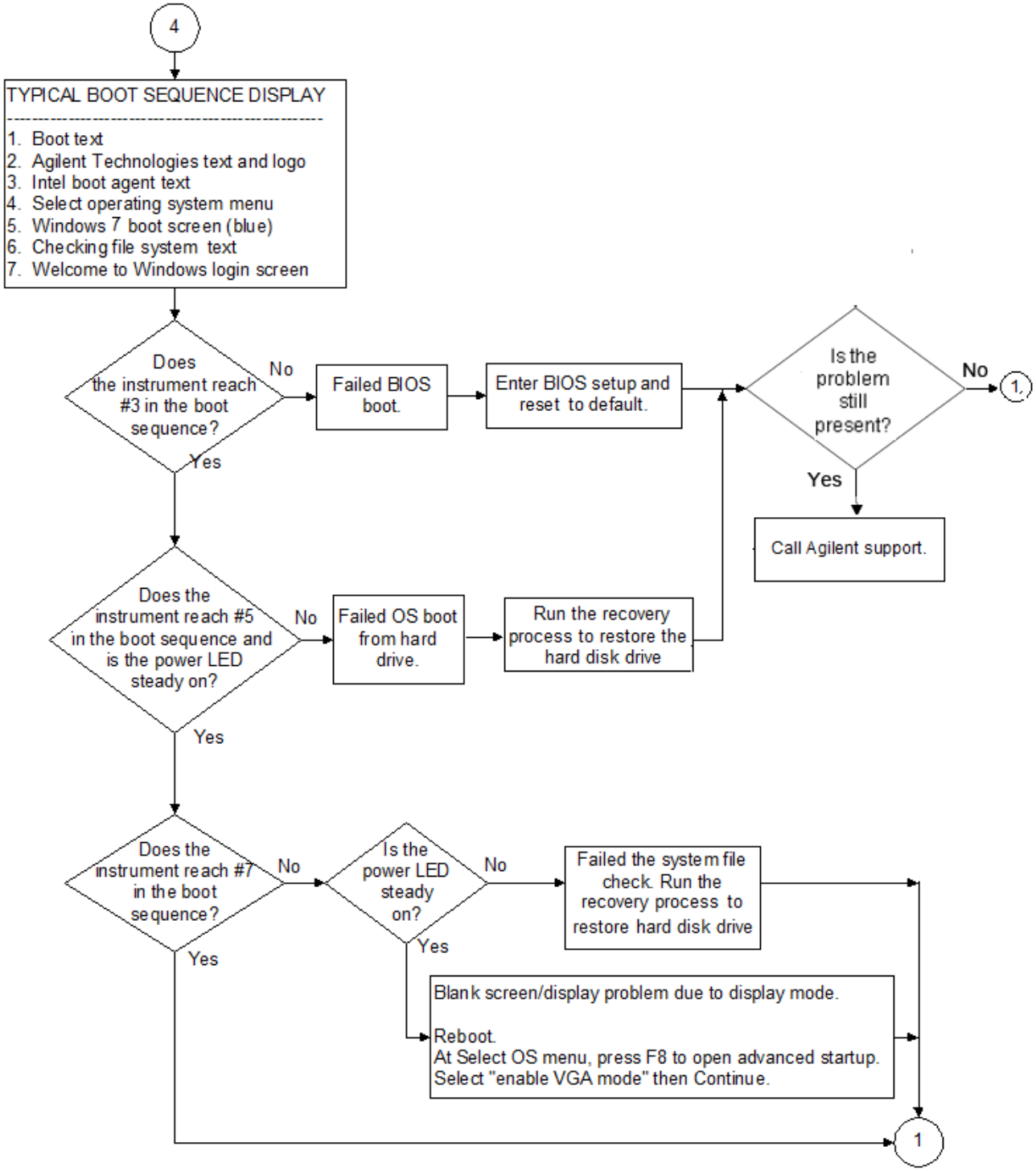


Figure 4 System Boot Up Troubleshooting Flowchart

To use the logic acquisition troubleshooting flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowchart. Start your troubleshooting at the top of the first flowchart.

If the module still doesn't work correctly after completing all the procedures described in the flowchart, return it to Agilent Technologies for repair. Be sure to include a note describing the problem in detail.

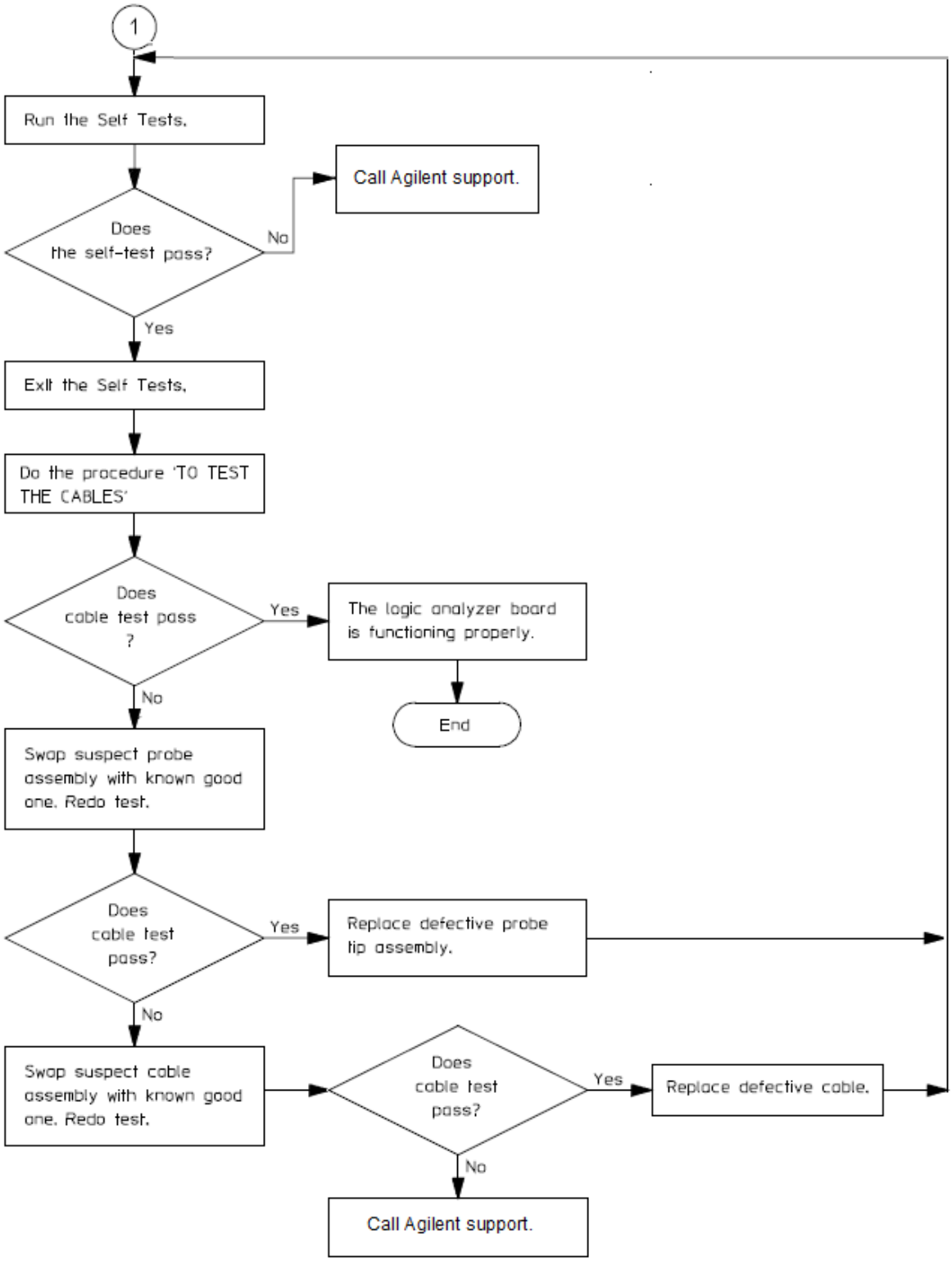


Figure 5 Logic Acquisition Troubleshooting Flowchart

To troubleshoot system power problems

If the system warns you it is powering down before it powers down, it is a fan/overtemp problem. If it just powers down, it is a power supply problem.

If the lights do not come on and if the system powers up momentarily when you plug it in, make sure the power button hasn't become jammed or stuck in the pushed-in position.

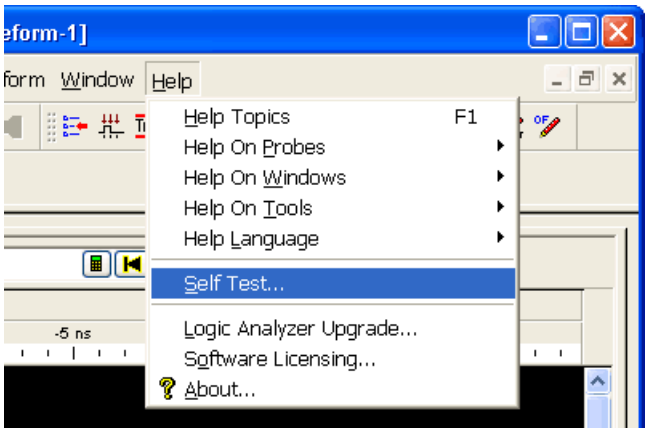
Power Supplies

All 16850 Series logic analyzers have the same 600 W power supply and a second 15 W power supply. The power supplies must remain connected in order to test their output voltages. There are power supply test points on the MIB board.

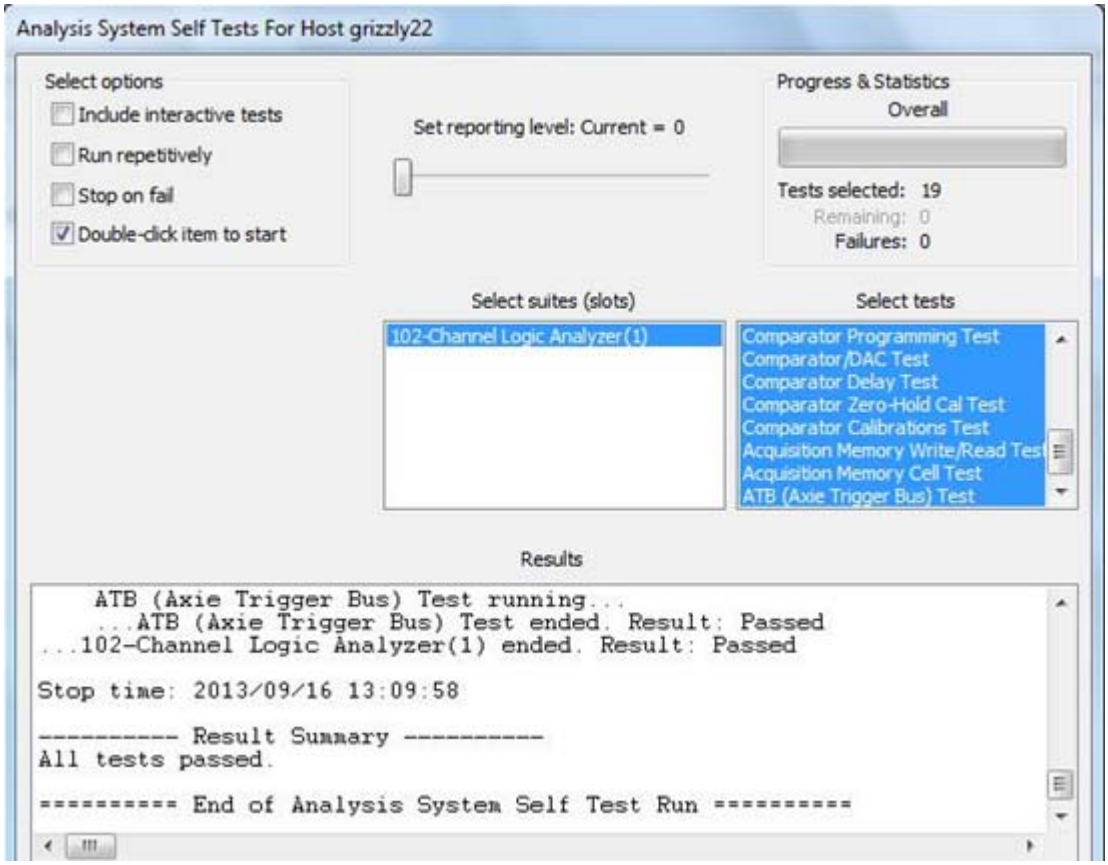
To run the self-tests

The self-tests check the functional operation of the logic analyzer. Perform the self-tests as an acceptance test when receiving the logic analyzer or when the logic analyzer is repaired.

1 In the *Agilent Logic and Protocol Analyzer* application, click **Help>Self Test...**



2 In the **Analysis System Self Test** dialog, double-click the test you want to run.



Logic Acquisition Self-Test Descriptions

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

Interface FPGA Version Test

This test verifies that the FPGA program is a version that the software can use. This is necessary because new features will be added to the 16850 logic analyzer that will require both new software and new FPGA bits.

Interface FPGA Register Test

The purpose of this test is to verify that the backplane interface can communicate with the backplane FPGA. The FPGA must be working before any of the other circuits on the board will work. Also, the FPGA generates the board ID code that is returned to identify the module and slot.

FPGA to FPGA Communication Test

This test is only run if there are two or more logic analyzer installed and connected together with the flex cables. The purpose of this test is to verify that the FPGAs can drive and receive the signals correctly.

SPI Bus Communication Test

The purpose of this test is to verify communications over the SPI bus from the Interface FPGA to various devices attached to the SPI bus.

EEPROM Test

The purpose of this test is to verify:

- The address and data paths to the EEPROM.
- That each cell in the EEPROM can be programmed high and low.
- That individual locations can be independently addressed.
- The EEPROM can be block erased.

Probe ID Read Test

The purpose of this test is to verify that the Probe ID values can be correctly read and to verify the functionality of the Digital to Analog Converter by testing the two Probe ID DAC outputs at various voltage levels.

Chip Registers Read/Write Test

The purpose of this test is to verify that each bit in each register of the Analysis chip can be written with a 1 and 0 and read back again. The test also verifies that a chip reset sets all registers to their reset condition (all 0s for most registers).

Freq Synth Lock Detect Test

This test determines if all the voltage-controlled oscillators (VCOs) are working properly.

Acquisition Chip BIST Test

Tests the Timing Zoom memory and other internal memories on the acquisition chip.

Resource Bus Connection Test

The purpose of this test is to verify global resources.

Comparator Programming Test

The purpose of this test is to verify the programming path to each of the comparators.

Comparator/DAC Test

This test is executed only if all probes are detached.

This test uses the pod, bonus, and calibration DACs, the calibration oscillator (implemented in the interface FPGA), the comparators, the connections between the comparators and the Analysis chip, and the activity indicators in the Analysis chip. We verify that we can use the DACs to control the data input to the comparators. We verify that each comparator data channel produces output. We verify that each comparator output is connected to each ASIC data input.

Comparator Delay Test

The comparator delay test verifies the integrity of all the delay line elements for each delay line in the comparators. Each delay line consists of 11 delay elements. When set for maximum delay, all 11 elements are connected in series. If any element is faulty, then data will not propagate through the comparator. If this is the only test failing, then it is almost certainly a bad comparator.

Comparator Zero-Hold Cal Test

Tests the delay elements for each delay line in the comparators. It tests that each delay line can increase its delay in a linear way through a range of delay values.

Comparator Calibrations Test

The purpose of this test is to verify that each of the comparator one-time calibrations can successfully be performed. This verifies that all of the calibration circuitry and components are within the tolerance limits required for proper calibration. This test is executed only if all probes are detached.

Acquisition Memory Write/Read Test

This test checks that each acquisition chip can write data to DDR acquisition memory and read the same data back.

Acquisition Memory Cell Test

Tests every bit of the DDR acquisition memory. The test verifies that every bit can be written to 0 and written to 1 and read back accurately.

ATB (AXIe Trigger Bus) Test

This test verifies the ATB signal connections between the acquisition chips, the interface FPGA and the two 8-bit transceiver chips.

To exit the test system

1 Close the self-test dialog. No additional actions are required.

To restore the system software

Restoring your system software might be necessary for the following reasons:

- Hard drive failure.
- Virus in the system or unstable system.
- Intentional disk clean - for example if you are passing the system to another team or returning it to a rental company and you do not want any data left on it.

The 16850 series of Logic Analyzers have the Windows 7 operating system installed. These systems also have the Agilent Logic and Protocol Analyzer software version 5.70 or later preinstalled.

If you need to restore the logic analysis system software, you run the recovery process on the hard drive of the system. This recovery process uses the hidden partition on the hard drive to restore the hard disk drive back to its original state in which it was shipped. When you run this process, the recovered hard disk drive contains:

- the Windows 7 operating system
- the version of the Logic Analyzer software which was installed when the system was originally shipped and not the latest or upgraded version of the software that might be available at the time of system recovery.
- the license files of any licensed optional products that you had purchased with the Logic Analyzer and that were installed when the system was originally shipped.

NOTE When you run the recovery process, the software licensing Host ID of your logic analyzer may change. If this happens, the restored license files will not work with the new host ID and you will need rehosted license files. To get these files, you can contact your nearest Agilent sales/service office. To locate a sales or service office, go to www.agilent.com/find/contactus.

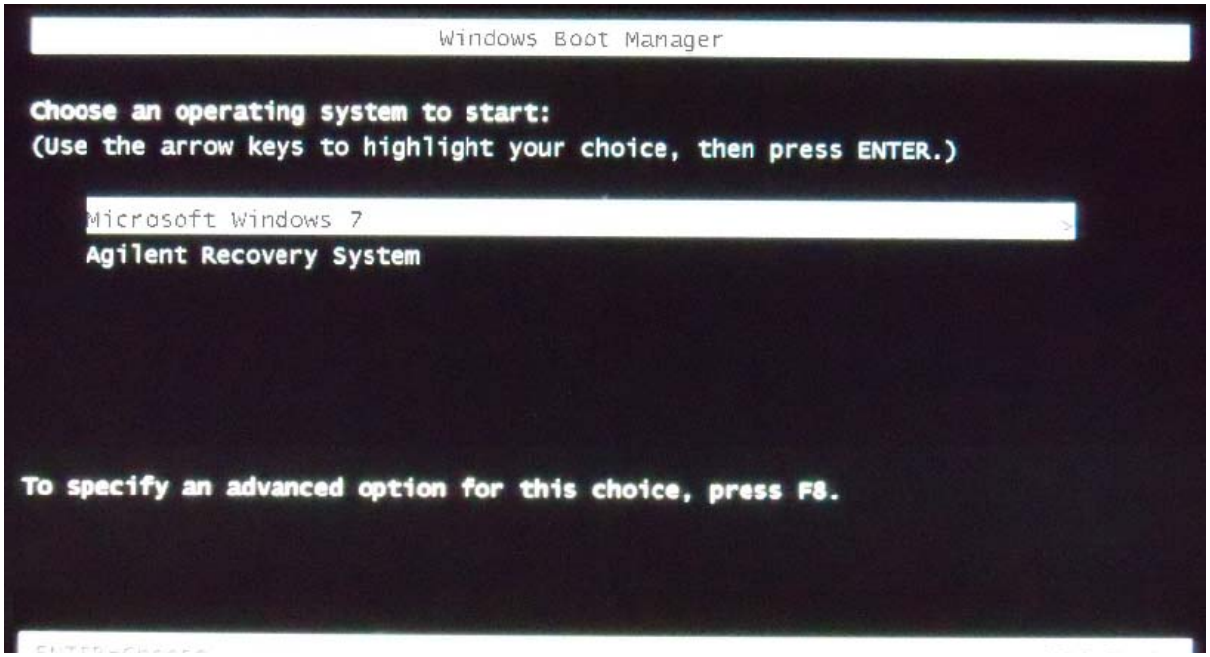
CAUTION Running the recovery process reformats your logic analyzer's hard disk drive to the state in which it was originally shipped to you. All user data files and programs are overwritten when the recovery process runs. Therefore, save your data to a CD or to another machine before you start recovering the system software.

To run the recovery process

1 Shut down and then restart your Logic Analyzer.

While booting up, the Logic Analyzer displays the Windows Boot Manager screen. This screen provides you the following options:

- **Microsoft Windows 7** - This is the default selected option. This option starts the Logic Analyzer with the Windows 7 operating system. This is the normal startup of the system.
- **Agilent Recovery system** - You should select this option when you want to restore/repair your Logic Analyzer software by running the Agilent recovery process.

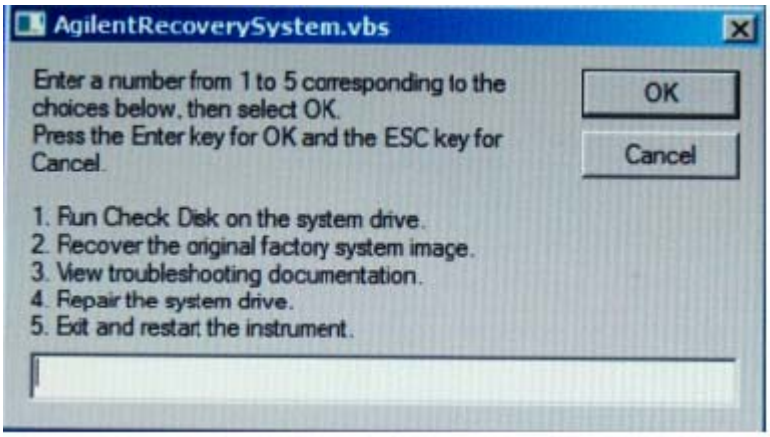


2 After a few seconds, Logic Analyzer automatically starts with the option selected in the Windows Boot Manager. Select the **Agilent Recovery system** option in the Windows Boot Manager screen using the arrow keys and then press Enter.

The recovery process starts preparing the system for recovery and displays the following screen with options to choose. You can enter:

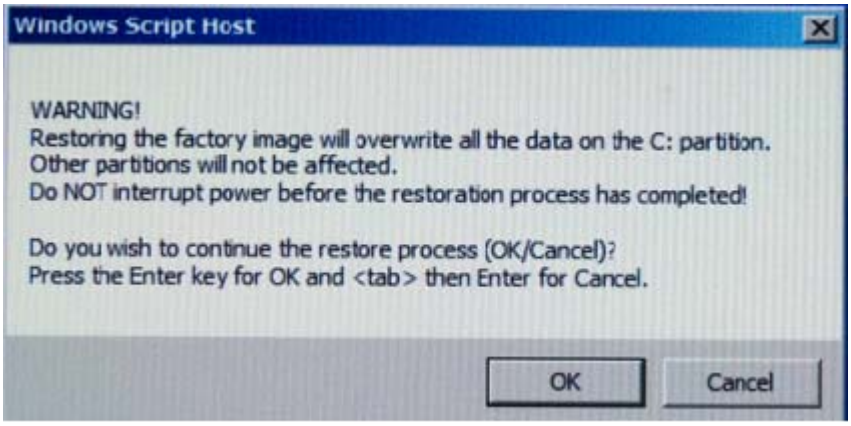
- **1** to run Check Disk on the Logic Analyzer's hard disk drive. If the recovery process encounters any problems while running Check Disk, it reports these problems else it returns to the Agilent Recovery system prompt on completion of Check Disk.

- **2** to restore your Logic Analyzer software back to its original state in which it was shipped.
- **3** to view a document that provides information on the recovery process.
- **4** to repair the Logic Analysis system hard disk drive.
- **5** to exit the recovery process and restart the Logic Analyzer in the normal mode.



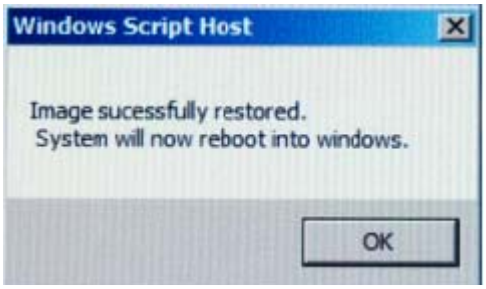
3 Select the second option in the above screen by entering **2** in the text box and clicking **OK**.

4 A warning message is displayed stating that the recovery process overwrites the data on C: drive. If you want to save your data to a CD or to another machine before you proceed further, then exit the recovery process and save your data. Else, click **OK** to proceed with the recovery process.



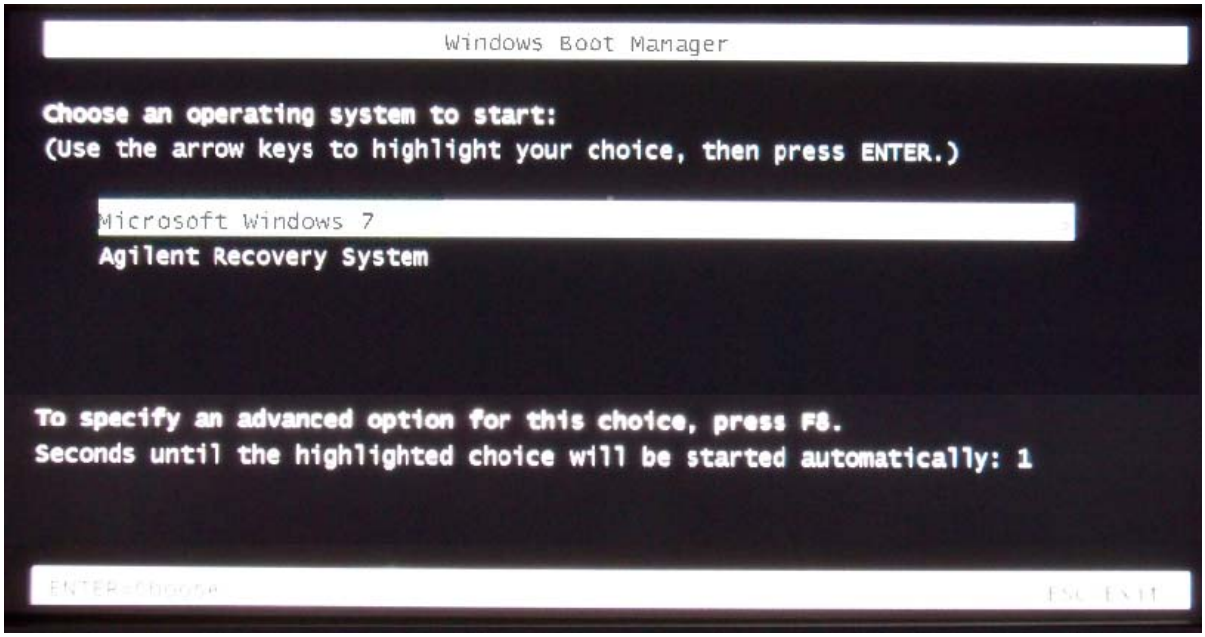
The recovery process starts.

If the recovery process is able to restore the system software successfully, then the following screen is displayed.



5 Click **OK** to proceed. You Logic Analysis system now reboots to Windows 7.

6 The Windows Boot Manager screen is displayed with **Microsoft Windows 7** as the default selection. The system automatically starts with this default selection. Alternatively, you can press Enter to proceed with the default selection.



NOTE There are situations when you are not able to run the recovery process, (for instance, when the hard disk drive of your system fails) or when running the recovery process does not recover your system software. In such situations, you can send your Logic Analysis system for hard disk repair/replacement to Agilent. Alternatively, you can contact your nearest Agilent sales/service office. To locate a sales or service office, go to www.agilent.com/find/contactus.

Contacting Agilent Service/Support

To locate a sales or service office near you, go to: http://www.agilent.com/find/contactus

To test the logic acquisition cables

This test allows you to functionally verify the logic analyzer cable and the flying lead probe of any of the logic analyzer pods. Only one probe and cable can be tested at a time. Repeat this test for each probe and cable to be tested. Two Flying Lead Probes are required if you need to test pods other than Pod 1 because the clock from Pod 1 will be used to acquire data.

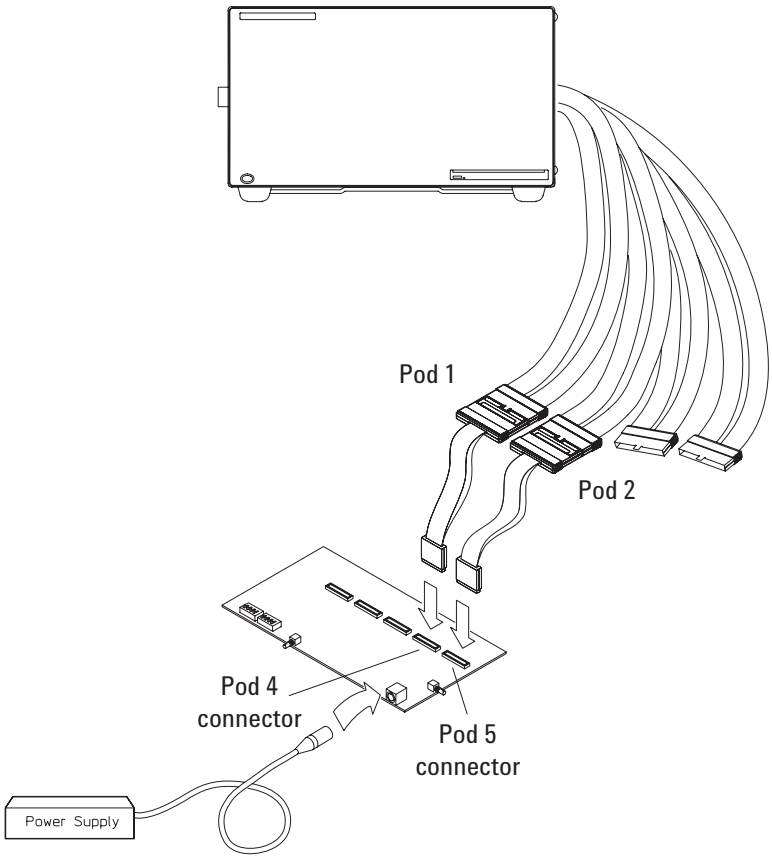
This test allows you to functionally verify U4201A logic analyzer cables and Agilent E5379A probes.

Table 11 Equipment Required to Test Cables

Equipment	Critical Specification	Recommended Part
Stimulus Board	No Substitute	16760-60001
Differential Probes	No Substitute	E5379A (Qty 2)

1 Connect the 16850 logic analyzer to the stimulus board.

- **a** Connect the Agilent E5379A 90-pin differential probes to the logic analyzer cable (also called “Pods”) to be tested. Start with Pods 1 and 2.
- **b** Connect the E5379A probe from logic analyzer Pod 1 to connector “Pod 4” on the stimulus board.
- **c** Connect the E5379A probe from logic analyzer Pod 2 to connector “Pod 5” on the stimulus board.
- **d** Connect the stimulus board power supply output to the stimulus board power supply connector J82.
- **e** Plug in the stimulus power supply to line power. The green LED DS1 should illuminate showing that the stimulus board is active.



2 Set up the stimulus board

   a Configure the oscillator select switch S1 according to the following settings:

      - S1 0 (Off).
      - S2 1 (On).
      - S3 0 (Off).
      - Int.

   b Configure the data mode switch S4 according to the following settings:

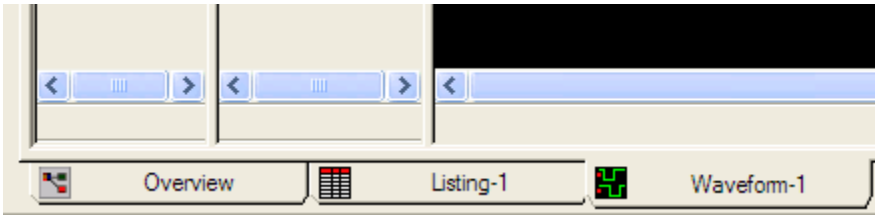
      - Even.
      - Count.

   c Press the Resynch VCO button, then the Counter RST (Counter Reset) button.

3 In the *Agilent Logic and Protocol Analyzer* application, choose File→New. This puts the logic analysis system into its initial state.

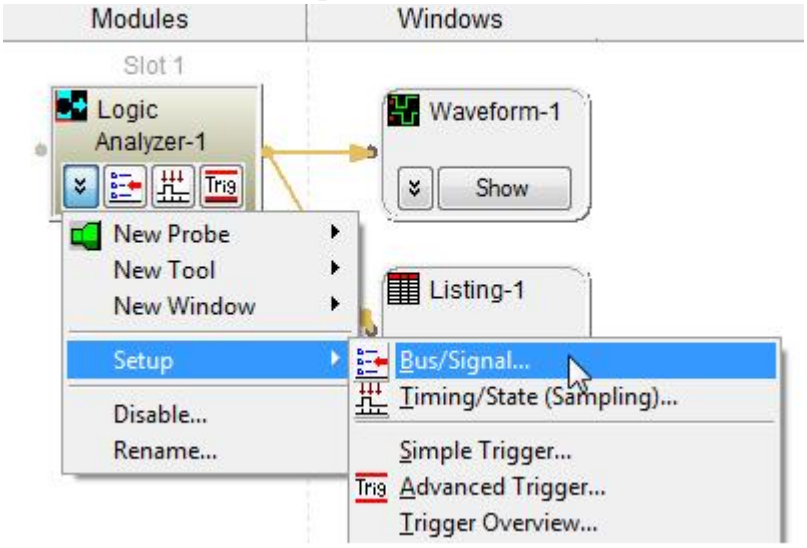
4 Disable all analyzers except the one being tested. This simplifies the instructions and makes module initialization faster.

a Select the Overview tab at the bottom of the main window.

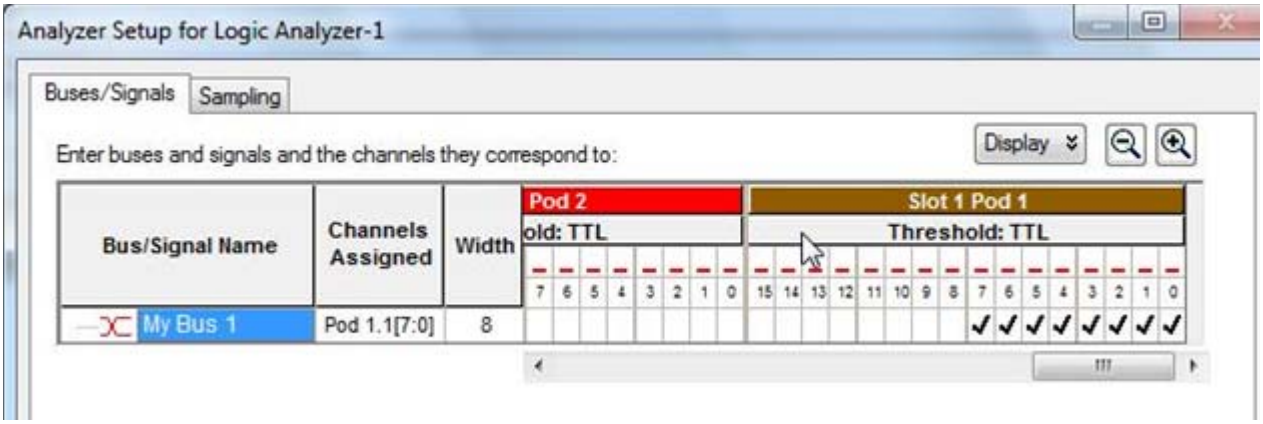


5 Set up the bus:

a In the Overview window, select Setup -> Bus/Signal... from the module's drop-down menu.



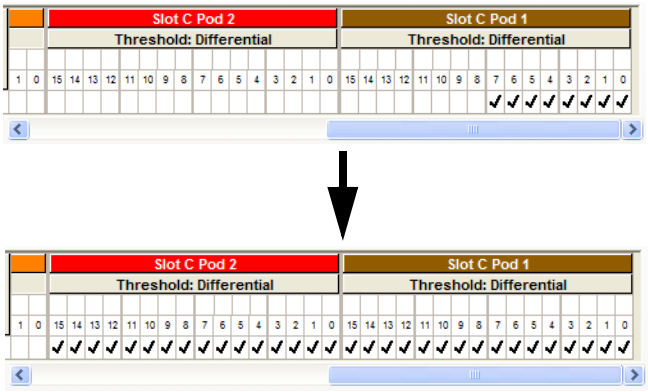
b Scroll if necessary to view the pods you are testing.



c Verify that the pod threshold buttons say "Threshold: Differential", as shown above. If they don't, make sure the correct probes (E5379A) are attached to pods 1

and 2. The threshold is set to Differential automatically when E5379A probes are attached.

d Channels 7 through 0 are already assigned by default. Assign pod 2 channels 15 through 0 and pod 1 channels 15 through 8 by clicking and dragging from the left-most channel box to the right-most channel box. Your display should look like the lower picture when you are done.



6 Select the State sampling mode and set the State Clock options:

a Select the **Sampling** tab of the Analyzer Setup window.

b Select **State - Synchronous Sampling**.

c For State Clock, select **CLK1 Clock** and **Both edges**.

7 Set the trigger position and acquisition memory depth:

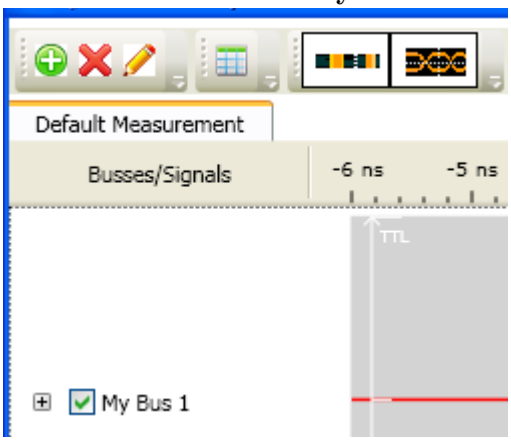
a Set the Trigger Position to **100% Poststore**.

b Set the **Acquisition Depth** to **8K**.

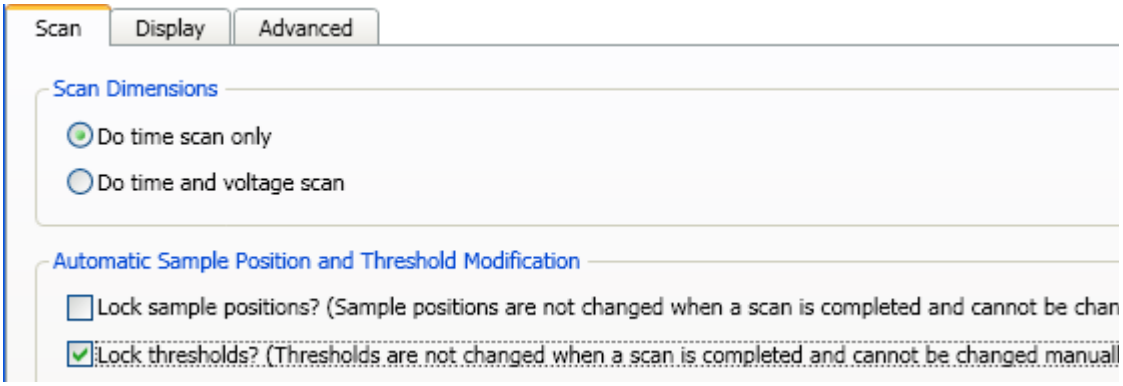
8 Adjust sampling positions:

a Click the **Eye Scan: Thresholds and Sample Positions** button. The **Eyescan - Sample Positions and Threshold Settings** dialog will appear.

b In the "Buses/Signals" section of the Eyescan - Sample Positions and Threshold Settings dialog, make sure the check box next to "My Bus 1" is checked.



c Click **Edit,** select the **Do time scan only** option as the scan dimension and then select the **Lock Thresholds** checkbox.



d Select the **Run This Measurement** button in the **Eyescan - Sample Positions and Threshold Settings** dialog.

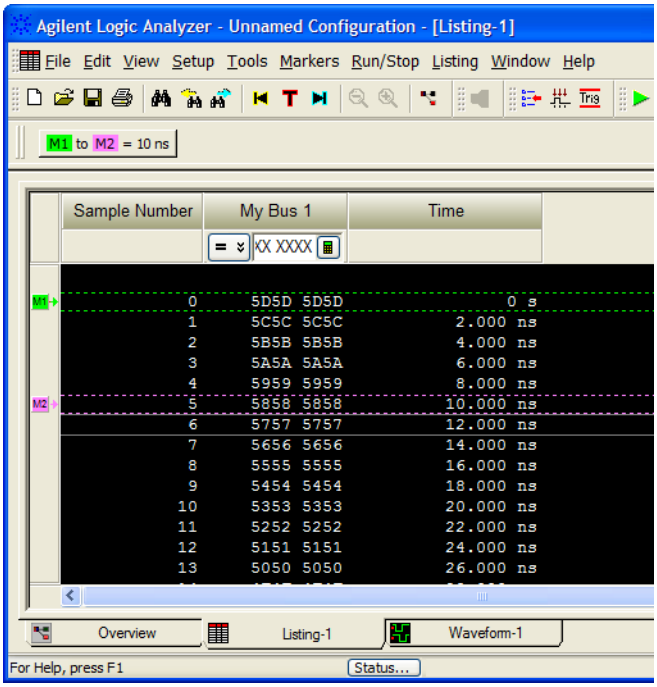
e Make sure the sampling positions are set properly, and re-align any stray channels if necessary.

f Select **OK** to close the **Eyescan - Sample Positions and THreshold Settings** window.

g Select **OK** to close the **Analyzer Setup** window.

9 Switch to the **Listing** window by selecting the Listing tab at the bottom of the main window.

10 Click the **Run** icon  . The listing should look similar to the figure below when you scroll down a bit.



Scroll down at least 256 samples to verify the data. My Bus 1 shows four 8-bit binary counters decrementing by 1. If the listing does not look similar to the figure, there is a possible problem with the cable or probe. Cause for cable test failures include:

- Open channel.
- Channel shorted to a neighboring channel.
- Channel shorted to either ground or a supply voltage.

If the test data is not correct, then perform the following step to isolate the failure.

11 Verify the failure:

a Swap the E5379A probes so that the pod 1 cable remains connected to the stimulus board's pod 4 connector and the pod 2 cable remains connected to

the stimulus board's pod 5 connector — just using different probes.

b Click the **Run** icon  .

If the failure is the same (that is, the error follows the cable) then the cable is faulty.

If the failure switches pods (that is, the error follows the E5379A probe) the probe is faulty.

12 Repeat the cable test for pods 3 and 4:

a Connect the logic analyzer's pod 3 cable to the stimulus board's pod 4 connector.

b Connect the logic analyzer's pod 4 cable to the stimulus board's pod 5 connector.

c In the **Buses/Signals** tab of the Analyzer Setup window, assign the pod 3 and 4 channels to "My Bus 1".

d In the **Sampling** tab of the Analyzer Setup window, for State Clock, select **Both edges**.

e Adjust sampling positions.

f Click the **Run** icon  . In the **Listing** window, check at least 256 samples for failures; if necessary, verify any failures by swapping the E5379A probes.

13 Repeat the cable test (step12) for pod pairs 5 and 6 and 7 and 8 connecting the odd pod cable to the stimulus board's pod 4 connector and the even pod cable to the stimulus board's pod 5 connector:

Return to the troubleshooting flowchart.

6 Repairing or Replacing a 16850 Series Logic Analyzer

If the 16850 series logic analyzer or any of its parts are faulty, return it to Agilent Technologies for repair/replacement. Agilent requires that the 16850 logic analyzer unit be repaired only at qualified repair facilities such as the Agilent Repair Centers.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this instrument.

WARNING Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect power from the instrument before performing the following procedures. After disconnecting the power, wait at least six minutes for the capacitors on the power supply board to discharge before servicing the instrument.

CAUTION Damage can occur to electronic components if you remove or components when the instrument is on or when the power cable is connected. Turn off the 16850 logic analyzer before performing the following procedures.

To remove the logic analyzer cable

To remove the logic analyzer cable:

1. Remove power from the logic analyzer.
   a. Turn off the logic analyzer.
   b. Disconnect the power cord.
2. Remove the logic analyzer pod cable.
   a. Remove the thumb screws that secure the logic analyzer cable to the pods.
   b. Disengage thumb screws completely from the module.
3. Pull the cable straight out from the logic analyzer.

If the logic analyzer cable is faulty, return it to Agilent Technologies for repair/replacement or order a new cable which is available as a replaceable part, and follow the next procedure to install the replaced logic analyzer cable.

To return the 16850 Logic Analyzer or Cable for Repair/Exchange

Before returning the logic analyzer or a logic analyzer cable to Agilent Technologies, contact your nearest Agilent Technologies Sales Office for additional details. Information on contacting Agilent can be found at www.agilent.com.

1 Write the following information on a tag and attach it to the logic analyzer/cable.

- Name and address of owner.
- Model number.
- Serial number.
- Description of service required or failure indications.

2 Remove accessories from the module.

Only return accessories to Agilent Technologies if they are associated with the failure symptoms.

3 Package the module/cable.

You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION For protection against electrostatic discharge (ESD), package the module in ESD-safe material.

4 Seal the shipping container securely, and mark it FRAGILE.

7
Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your 16850 Series logic analyzer.

Ordering Replaceable Parts

To order a part, visit us on the web at www.parts.agilent.com or contact your nearest Agilent Technologies Sales Office for assistance. To locate a sales office near you, go to www.agilent.com/find/contactus.

System Replaceable Parts List

The following table lists the replaceable parts for the 16850 series logic analyzer. Information included for each part in the list consists of the following:

- Agilent Technologies part number
- Total quantity included with the instrument (Qty)
- Description of the part

Table 12 Replaceable parts for the chassis subassembly

Agilent Technologies Part Number	Qty	Description
16850-68700		Chassis subassembly
0515-0430	6	Screw-Machine W/-Washer Pan-HD Torx-T10 M3X0.5 6mm
1250-2075	3	Nut-RF Connector 9/16-in HEX 1/2-28 UNEF-2B ThreadS .095-in
2190-0068	6	Washer-Lock-inTL T 1/2-in .505-in-ID
16850-04104	1	Cover, multiframe
0960-2939	1	Motherboard Flex-ATX Core 2 DUO 4GB with Inverted Backlight enable
16850-94301	1	Label, motherboard ports
0515-0458	7	Screws M3.5
9170-1547	1	Ferrite (flat black)
16850-61603	1	Cable, paddle board
1400-0308	1	Cable-Tie self-Locking 7.31-in-LG 184-mil-Wide Nylon Gray
16800-61601	1	Cable-Power
16800-61600	1	Cable-PCI/MIB
1400-2120	1	Bracket right-Angle 120X18.6X12.5-mm Cold-rolled-Steel
0515-2143	4	Screw-Machine W/PATCH-LK Pan-HD Torx-T20 M4X0.7 6mm-LG SST-300
0515-2032	6	Screw-Machine W/Patch-Lock 90-DEG-Flat-HD Torx-T10 M3X0.5 8mm
1400-0249	2	Cable-Tie self-Locking 91-mil-Wide Nylon Gray
1400-3327	3	Clip-Medium Grey (Panduit LC5-A-C8)
1400-3191	1	Clip-Small Grey (Panduit LC3-A-C8)
16800-61617	1	Cable-cpu power
3160-4243	1	Fan with Heat-SInk 12-VDC 4500-RPM

Table 12 Replaceable parts for the chassis subassembly

Agilent Technologies Part Number	Qty	Description
16901-61607	1	Motherboard Switch Cable
9170-2224	1	Ferrite 7mm black Laird (28A2025-0A2)
0624-1066	4	Mounting Hardware for fans
16800-68501	1	Fan
16850-68707	1	Chassis Assembly
16850-61601	1	Fan cable
16850-68702	1	Power supply subassembly - 600 w
16850-68715	1	Power Supply Subassembly - 15 Watt
16903-66504	1	PCI Board with Bracket
16850-68704	1	Removable HDD drive subassembly
7121-8317	1	Shock hazard label
16850-68710	1	MIB Subassembly

Table 13 Replaceable parts for the final assembly

Agilent Technologies Part Number	Qty	Description
16850-68700	1	Chassis subassembly
9170-2206	1	Ferrite 13mm black Laird (28A2024-0A2)
0515-0430	13	Screw-Machine W/ Washer Pan-HD Torx-T10 M3X0.5 6mm
0515-2032	21	Screw-Machine W/Patch-Lock 90-DEG-Flat-HD Torx-T10 M3X0.5 8mm-
16850-68712	1	Touchscreen front panel
16850-68714	1	Chassis strap sub assembly
16850-68706	1	Fan Deck sub assembly
16600-68707	1	Handle assembly
5090-4157	1	Serial Label
1685x-66501	1	Tested acquisition board sub assembly, xx and xx channel
1400-0308	1	Cable-Tie self-Locking 7.31-in-LG 184-mil-Wide Nylon Gray
1400-0249	1	Cable-Tie self-Locking 91-mil-Wide Nylon Gray
16702-81204	1	Copper Foil Label

Table 13 Replaceable parts for the final assembly (continued)

Agilent Technologies Part Number	Qty	Description
9320-6648	1	Label-PTD 2MIL Matte Chrome POLYE
54904-94319	1	CSA label
8160-1884	0.8	RFI gasket - no snag copper 16 inches Laird (0077003302)
16900-92019	1	Logic-signup Front Card English
5190-1836	2	Clear Sticker
9010-0305	1	Software-Windows Embedded Standard 7 (WSE7)
16850-04101	1	Outer Cover
1685x-22201	1	Bezel, 34 Channel
0515-1644	4	Bezel screws
1685x-94301	1	Label-ID
01680-68702	1	Accessory Pouch
1150-7997	1	STYLUS-PEN Cushion Grip 5.54-in-LG 0.44-in-DIA
5190-1835	1	Card - Stylus Holder

Table 14 Replaceable parts for the front panel

Agilent Technologies Part Number	Qty	Description
8160-1884	1.125	RFI gasket - no snag copper 16 inches Laird (0077003302)
54904-61617	1	Cable - Display and Inverter
2090-0993	1	Display-Touch Screen 15-in 330.08X254.9X2.25mm 8-wire resistive
2090-0978	1	Display LCD 15-Inch TFT 1024X768-Pixels 253.5X326.5X12-mm
16901-61606	1	Touchscreen cable
16901-61602	1	Cable-usb dual
16800-66403	1	PC board assembly - front panel
16800-47402	1	Keypad-touchscreen

Table 14 Replaceable parts for the front panel

Agilent Technologies Part Number	Qty	Description
16800-40201	1	Frame-front
1400-3549	3	Clip-Large Grey (Panduit LC10-A-L8)
1400-3191	2	Clip-Small Grey (Panduit LC3-A-C8)
16850-01201	1	Front panel bracket
16850-94304	1	Label, front panel insert
16702-47402	1	Knob - Curser
0960-2796	1	Touch Screen Controller Board 5V-DC
0515-2032	4	Screw-Machine W/Patch-Lock
0515-1246	17	Screw-Machine W/Patch-LK
0950-5443	1	Inverter DC to AC 4-WATT 2-Output

Table 15 Replaceable parts for the handle

Agilent Part Number	Qty	Description
16600-68707	1	Handle assembly
5021-4309	2	Screw-Machine W/PATCH-LK
54801-24702	2	Spacer-Strap Handle
54810-44901	1	Molded-Over Handle
54810-45001	2	End Cap - Handle

Table 16 Replaceable parts for the HDD

Agilent Part Number	Qty	Description
16850-68704		HDD assembly
54904-04101	1	Sheet metal hard drive bracket
54904-94317	1	Label
16850-83700	1	Hard drive 2.5" (0950-5457 formatted)
0515-0430	4	Screw

Table 17 Replaceable parts for the power supply (600 Watts)

Agilent Part Number	Qty	Description
16850-68702		Power supply assembly (600 Watts)
0950-4891	1	Power Supply AC-AC Adapter 600-Watt 1-Output
16850-61602	1	Cable, power supply 600w
16700-61602	1	Cable Assembly-Power Supply

Table 18 Replaceable parts for the power supply (15 Watts)

Agilent Part Number	Qty	Description
16850-68715		Power Supply Assembly (15 Watt)
0515-0430	2	M3 Screw
16800-01206	1	Plate - power supply 15w
16700-61602	1	Cable Assembly-Power Supply
16800-61606	1	Cable - ps 15w
0950-4822	1	Power Supply 15-WATT 1-Output

Table 19 Replaceable parts for the PCI card

Agilent Technologies Part Number	Qty	Description
16903-66504		PCI Card assembly
0515-0430	2	M3 screw
16800-01205	1	Bracket - PCI card
16903-66404	1	PCI Board

Table 20 Replaceable parts for the MIB Board

Agilent Technologies Part Number	Qty	Description
0515-2035	2	M3 Screw - flat
0515-2994	5	M3 Screw
16850-00104	1	MIB Bracket
0403-1116	2	Guide
54904-41202	2	Cable Clamp top/bottom
54904-61614	1	Cable HDD Sata/Power
16800-61615	1	Cable-Front panel
16850-24701	1	MIB Support Block
1400-3191	1	Cable clip
16850-61607	1	Cable, HDD power adapter
16850-66402	1	Upper Paddle Board
16850-66501	1	Tested, Module Interface Board (MIB) PCA

Table 21 Replaceable parts for the fan

Agilent Technologies Part Number	Qty	Description
16850-68706		Fan assembly
0624-1066	12	Screw 10-14 0.5-in-LG
16800-68501	3	Fan-assembly
16850-00103	1	Fan bracket

Table 22 Replaceable parts for the chassis strap

Agilent Technologies Part Number	Qty	Description
16850-68714		Chassis strap assembly
16850-21201	1	Chassis support strap
0515-1946	2	M3 screw
1400-0308	2	Cable-Tie self-Locking 7.31-in-LG 184-mil-Wide Nylon Gray
1400-0528	2	Cable-Tie pressure sensitive Adhesive mounting

Table 23 Replaceable parts for the acquisition tray

Agilent Technologies Part Number	Qty	Description
0515-1941	13	M2.5 Screw
16850-00102	1	Acquisition Tray
16852-66401	1	68 Channel Acquisition Loaded Printed Circuit Board
16854-66401	1	136 Channel Acquisition Loaded Printed Circuit Board
1400-2225	1	Clamp-Cable pressure sensitive Adhesive mount
16850-66403	1	Lower Paddleboard
1205-1499	1	Gap filler replacement Kit 1.181X1.181X0.059-in
1205-1487	16	Gap filler replacement kit .492X.492X.059-in
U4154-21103	1	Regulator heat sink
U4154-21102	1	Acquisition heat sink
U4154-21101	1	Comparator heat sink
16850-04102	1	Probe filler plate
U4154-21201	2	Probe attach bracket
0380-5191	21	Standoff-HEX Male M2.5X0.45 5mm-A/F 3mm-LG SST Passivated
0535-0008	21	Nut-HEX M2.5X0.45 2mm-THK 5mm-A/F Steel Ni-Plated
8160-1883	0.8	RFI Finger gasket
0905-1866	1.33	Fabric over foam RFI gasket

7 Replaceable Parts

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