

FEATURES

Offset voltage and offset voltage drift

B grade: 25 μV and 0.25 $\mu\text{V}/^\circ\text{C}$ at $V_{\text{SY}} = \pm 5 \text{ V}$

A grade maximum offset at 25 $^\circ\text{C}$ and maximum drift from -40°C to $+125^\circ\text{C}$

SOIC: 50 μV and 0.55 $\mu\text{V}/^\circ\text{C}$ single/dual and 0.75 $\mu\text{V}/^\circ\text{C}$ quad

MSOP: 90 μV and 1.2 $\mu\text{V}/^\circ\text{C}$ dual and 120 μV and 1.2 $\mu\text{V}/^\circ\text{C}$ single

TSSOP: 120 μV and 1.2 $\mu\text{V}/^\circ\text{C}$ quad

MSL1 rated

Low input bias current: 1 nA maximum at $T_A = 25^\circ\text{C}$

Low voltage noise density: 6.9 nV/ $\sqrt{\text{Hz}}$ typical at $f = 1000 \text{ Hz}$

CMRR, PSRR, and $A_v > 120 \text{ dB}$ minimum

Low supply current: 400 μA per amplifier typical

Wide gain bandwidth product: 3.9 MHz at $\pm 5 \text{ V}$

Dual-supply operation: $\pm 2.5 \text{ V}$ to $\pm 15 \text{ V}$

Unity gain stable

No phase reversal

APPLICATIONS

Process control front-end amplifiers

Wireless base station control circuits

Optical network control circuits

Instrumentation

Sensors and controls: thermocouples, RTDs, strain bridges, and shunt current measurements

Precision filters

GENERAL DESCRIPTION

The single ADA4077-1, dual ADA4077-2, and quad ADA4077-4 amplifiers feature extremely low offset voltage and drift, and low input bias current, noise, and power consumption. Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

Applications for this amplifier include sensor signal conditioning (such as thermocouples, RTDs, strain gauges), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems. The ADA4077-1, ADA4077-2, and ADA4077-4 are useful in line powered and portable instrumentation, precision filters, and voltage or current measurement and level setting.

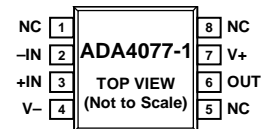
Unlike amplifiers by some competitors, the ADA4077-1/ADA4077-2/ADA4077-4 have an MSL1 rating that is compliant with the most stringent of assembly processes, and they are specified over the extended industrial temperature range from -40°C to $+125^\circ\text{C}$ for the most demanding operating environments.

Rev. C

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PIN CONNECTION DIAGRAMS



NC = NO CONNECT. NOT INTERNALLY CONNECTED. 10238-101

Figure 1. ADA4077-1, 8-Lead SOIC (and 8-Lead MSOP)

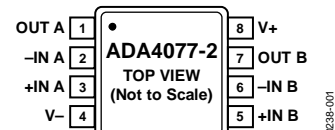


Figure 2. ADA4077-2, 8-Lead MSOP (and 8-Lead SOIC)

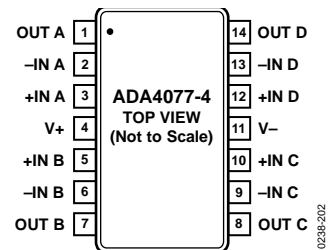


Figure 3. ADA4077-4, 14-Lead TSSOP (and 14-Lead SOIC)

The ADA4077-1 and ADA4077-2 are available in an 8-lead SOIC package, including the B grade, and in an 8-lead MSOP (A grade only). The ADA4077-4 is offered in a 14-lead TSSOP and a 14-lead SOIC package.

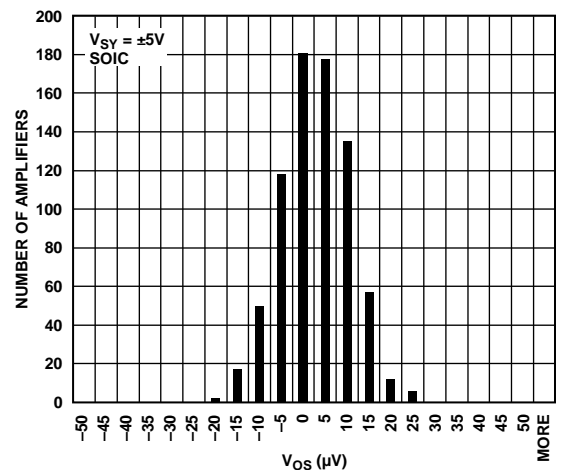


Figure 4. Offset Voltage Distribution

Table 1. Evolution of Precision Devices by Generation

Op Amp	First	Second	Third	Fourth	Fifth	Sixth
Single	OP07	OP77	OP177	OP1177	AD8677	ADA4077-1
Dual				OP2177		ADA4077-2
Quad				OP4177		ADA4077-4

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REVISION HISTORY

6/15—Rev. B to Rev. C

Change to Figure 63	18
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1/14—Rev. A to Rev. B

Added ADA4077-1	Universal
Changes to Features Section.....	1
Added Figure 1; Renumbered Sequentially	1
Changes to Table 2.....	3
Changes to Table 3.....	4
Added Figure 5, Figure 6, and Table 6; Renumbered Sequentially	7
Changes to Figure 17, Figure 20, and Figure 21	11
Changes to Figure 65.....	19
Added Figure 67 and Figure 68.....	19
Changes to Output Phase Reversal Section and Figure 70	21
Changes to Ordering Guide	24

10/13—Rev. 0 to Rev. A

Added ADA4077-4.....	Universal
Changes to Features, General Description, and Figure 1.....	1
Deleted Figure 2; Renumbered Sequentially	1
Added Figure 2.....	1
Changes to Table 2.....	3
Changes to Table 3.....	4
Changes to Table 4.....	6
Added Figure 6, Figure 7, and Table 7; Renumbered Sequentially	8
Changes to Typical Performance Characteristics Section	9
Changes to Figure 65.....	20
Updated Outline Dimensions	21
Changes to Ordering Guide	23

10/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ± 5 V

$V_{SY} = \pm 5.0$ V, $V_{CM} = 0$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade, 8-Lead SOIC, ADA4077-1/ADA4077-2)	V_{OS}			10	25	μV
Offset Voltage Drift (B Grade, 8-Lead SOIC, ADA4077-1/ADA4077-2)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			65	$\mu\text{V}/^\circ\text{C}$
Offset Voltage (A Grade) 8-Lead SOIC (ADA4077-1/ADA4077-2) and 14-Lead SOIC (ADA4077-4)	V_{OS}			15	50	μV
8-Lead MSOP (ADA4077-1)		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			105	μV
8-Lead MSOP (ADA4077-2)			50		120	μV
14-Lead TSSOP (ADA4077-4)		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			90	μV
Offset Voltage Drift (A Grade) 8-Lead SOIC (ADA4077-1/ADA4077-2) 14-Lead SOIC (ADA4077-4) 8-Lead MSOP (ADA4077-1/ADA4077-2) and 14-Lead TSSOP (ADA4077-4)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			220	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B		-1	-0.4	+1	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.5		+1.5	nA
Input Offset Current	I_{OS}		-0.5	+0.1	+0.5	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.0		+1.0	nA
Input Voltage Range Common-Mode Rejection Ratio	CMRR	$V_{CM} = -3.8$ V to +3 V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-3.8		+3	V
			122	140		dB
Large Signal Voltage Gain	A_V	$R_L = 2$ k Ω , $V_O = -3.0$ V to +3.0 V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	121	130		dB
			120			dB
Input Capacitance	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		70		G Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1$ mA $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.1			V
			4			V
Output Voltage Low	V_{OL}	$I_L = 1$ mA $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			-3.5	V
					-3.2	V
Output Current Short-Circuit Current	I_{OUT} I_{SC}	$V_{DROPOUT} < 1.6$ V $T_A = 25^\circ\text{C}$		± 10 22		mA mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1$ kHz, $A_V = +1$		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5$ V to ± 18 V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	123 120	128		dB dB
Supply Current per Amplifier	I_{SY}	$V_O = 0$ V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		400	450 650	μA μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		1.2		V/ μ s
Settling Time to 0.1%	t_s	$V_{IN} = 1\text{ V step}, R_L = 2\text{ k}\Omega, A_V = -1$		3		μ s
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}, R_L = 2\text{ k}\Omega, A_V = +100$		3.9		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}, R_L = 2\text{ k}\Omega, A_V = +1$		3.9		MHz
-3 dB Closed-Loop Bandwidth	-3 dB	$A_V = +1, V_{IN} = 10\text{ mV p-p}, R_L = 2\text{ k}\Omega$		5.9		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}, R_L = 2\text{ k}\Omega, A_V = +1$		55		Degrees
Total Harmonic Distortion Plus Noise	THD + N	$V_{IN} = 1\text{ V rms}, A_V = +1, R_L = 2\text{ k}\Omega, f = 1\text{ kHz}$		0.004		%
NOISE PERFORMANCE						
Voltage Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		0.25		μ V p-p
Voltage Noise Density	e_n	$f = 1\text{ Hz}$		13		nV/ $\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		7		nV/ $\sqrt{\text{Hz}}$
		$f = 1000\text{ Hz}$		6.9		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.2		pA/ $\sqrt{\text{Hz}}$
MULTIPLE AMPLIFIERS CHANNEL SEPARATION						
	C_S	$f = 1\text{ kHz}, R_L = 10\text{ k}\Omega$		-125		dB

ELECTRICAL CHARACTERISTICS, $\pm 15\text{ V}$

$V_{SY} = \pm 15\text{ V}, V_{CM} = 0\text{ V}, T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
INPUT CHARACTERISTICS							
Offset Voltage (B Grade, 8-Lead SOIC, ADA4077-1/ADA4077-2)	V_{OS}			10	35	μ V	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			65	μ V	
Offset Voltage Drift (B Grade, 8-Lead SOIC, ADA4077-1/ADA4077-2)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.25	$\mu\text{V}/^\circ\text{C}$	
Offset Voltage (A Grade) 8-Lead SOIC (ADA4077-1/ADA4077-2) and 14-Lead SOIC (ADA4077-4)	V_{OS}			15	50	μ V	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			105	μ V	
		8-Lead MSOP (ADA4077-1)				120	μ V
		8-Lead MSOP (ADA4077-2)		50	90	μ V	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				220	μ V
		14-Lead TSSOP (ADA4077-4)		15	120	μ V	
Offset Voltage Drift (A Grade) 8-Lead SOIC (ADA4077-1/ADA4077-2) 14-Lead SOIC (ADA4077-4) 8-Lead MSOP (ADA4077-1/ADA4077-2) and 14-Lead TSSOP (ADA4077-4)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			220	μ V	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	0.55	$\mu\text{V}/^\circ\text{C}$	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.4	0.75	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current	I_B		-1	-0.4	+1	nA	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.5		+1.5	nA	
Input Offset Current	I_{OS}		-0.5	+0.1	+0.5	nA	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.0		+1.0	nA	
Input Voltage Range			-13.8		+13	V	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -13.8\text{ V to }+13\text{ V}$	132	150		dB	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	130			dB	

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Large Signal Voltage Gain 8-Lead SOIC and 8-Lead MSOP (ADA4077-1/ADA4077-2)	A_V	$R_L = 2\text{ k}\Omega$, $V_O = -13.0\text{ V to }+13.0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	125	130		dB
14-Lead TSSOP and 14-Lead SOIC (ADA4077-4)	A_V	$R_L = 2\text{ k}\Omega$, $V_O = -13.0\text{ V to }+13.0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	122	130		dB
Input Capacitance	C_{INDM}	Differential mode		3		pF
	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		100		G Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	14.1			V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	14		-13.5	V
Output Current	I_{OUT}	$V_{DROPOUT} < 1.2\text{ V}$		± 10	-13.2	mA
Short-Circuit Current	I_{SC}	$T_A = 25^\circ\text{C}$		22		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ kHz}$, $A_V = +1$		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5\text{ V to } \pm 18\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	123	128		dB
Supply Current per Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120	400	500	μA
					650	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		1.2		V/ μs
Settling Time to 0.01%	t_s	$V_{IN} = 10\text{ V p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = -1$		16		μs
Settling Time to 0.1%	t_s	$V_{IN} = 10\text{ V p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = -1$		10		μs
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = +100$		3.6		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = +1$		3.9		MHz
-3 dB Closed-Loop Bandwidth	-3 dB	$A_V = +1$, $V_{IN} = 10\text{ mV p-p}$, $R_L = 2\text{ k}\Omega$		5.5		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = +1$		58		Degrees
Total Harmonic Distortion Plus Noise	THD + N	$V_{IN} = 1\text{ V rms}$, $A_V = +1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$		0.004		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ Hz}$		13		nV/ $\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		7		nV/ $\sqrt{\text{Hz}}$
		$f = 1000\text{ Hz}$		6.9		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.2		pA/ $\sqrt{\text{Hz}}$
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_s	$f = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$		-125		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$\pm V_{SY}$
Input Current ¹	± 10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
ESD Human Body Model (HBM) ²	6 kV
Field Induced Charge Device Model (FICDM) ³	1.25 kV

¹ The input pins have clamp diodes to the power supply pins and to each other. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

² ESDA/JEDEC JS-001-2011 applicable standard.

³ JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	190	44	°C/W
8-Lead SOIC	158	43	°C/W
14-Lead TSSOP	240	43	°C/W
14-Lead SOIC	115	36	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

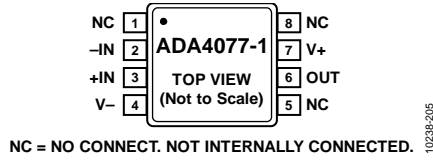


Figure 5. ADA4077-1 Pin Configuration, 8-Lead MSOP (RM-8)

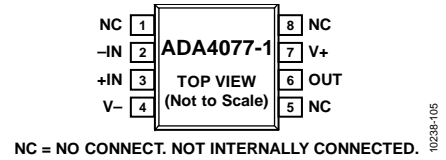


Figure 6. ADA4077-1 Pin Configuration, 8-Lead SOIC (R-8)

Table 6. ADA4077-1 Pin Function Descriptions, 8-Lead MSOP and 8-Lead SOIC

Pin No.	Mnemonic	Description
1, 5, 8	NC	No Connect. Not internally connected.
2	-IN	Inverting Input.
3	+IN	Noninverting Input.
4	V-	Negative Supply Voltage.
6	OUT	Output.
7	V+	Positive Supply Voltage.

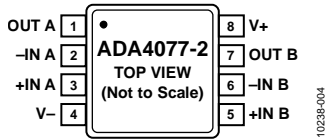


Figure 7. ADA4077-2 Pin Configuration, 8-Lead MSOP

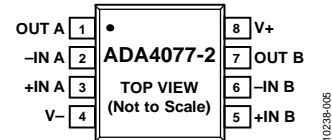


Figure 8. ADA4077-2 Pin Configuration, 8-Lead SOIC

Table 7. ADA4077-2 Pin Function Descriptions, 8-Lead MSOP and 8-Lead SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	-IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V-	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	-IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.

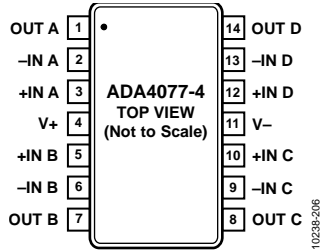


Figure 9. ADA4077-4 Pin Configuration, 14-Lead TSSOP

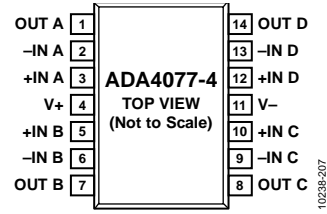


Figure 10. ADA4077-4 Pin Configuration, 14-Lead SOIC

Table 8. ADA4077-4 Pin Function Descriptions, 14-Lead TSSOP and 14-Lead SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	-IN A	Negative Input Channel A.
3	+IN A	Positive Input Channel A.
4	V+	Positive Supply Voltage.
5	+IN B	Positive Input Channel B.
6	-IN B	Negative Input Channel B.
7	OUT B	Output Channel B.
8	OUT C	Output Channel C.
9	-IN C	Negative Input Channel C.
10	+IN C	Positive Input Channel C.
11	V-	Negative Supply Voltage.
12	+IN D	Positive Input Channel D.
13	-IN D	Negative Input Channel D.
14	OUT D	Output Channel D.

TYPICAL PERFORMANCE CHARACTERISTICS

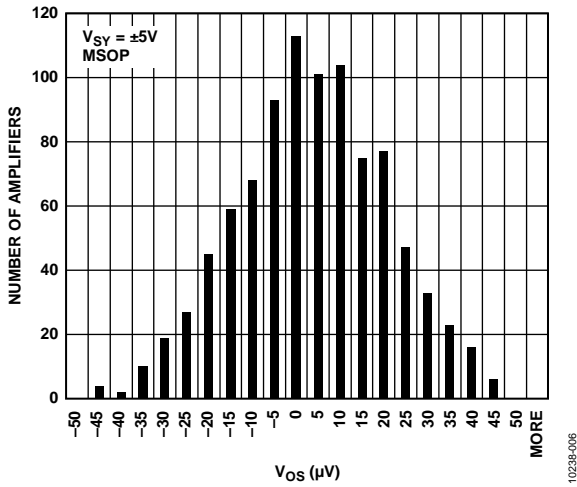


Figure 11. ADA4077-2 Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 5V$

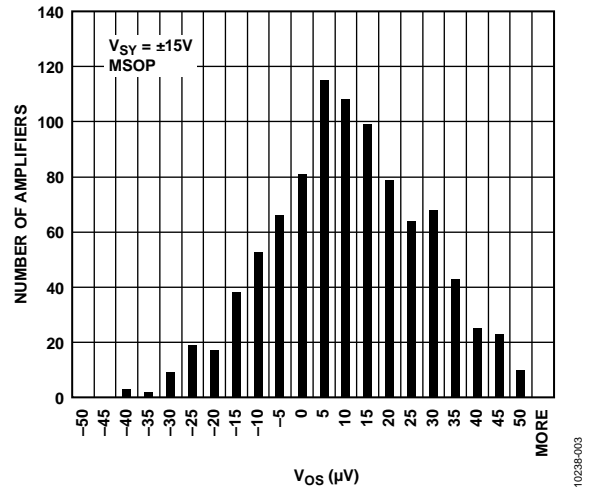


Figure 14. ADA4077-2 Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 15V$

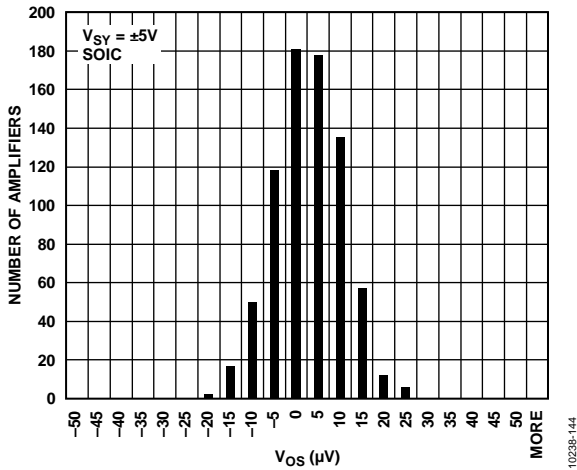


Figure 12. Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 5V$

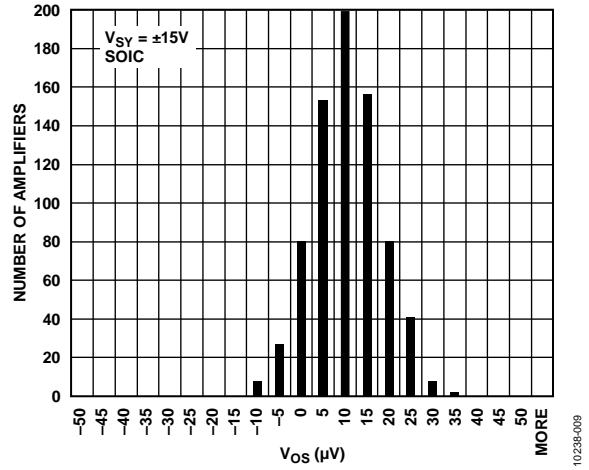


Figure 15. Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 15V$

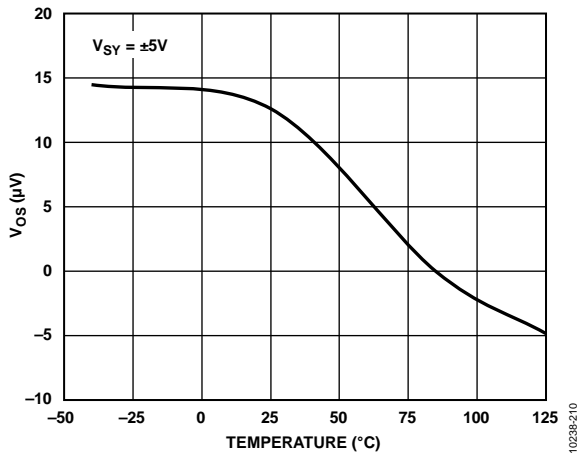


Figure 13. Offset Voltage (V_{OS}) vs. Temperature, $V_{SY} = \pm 5V$

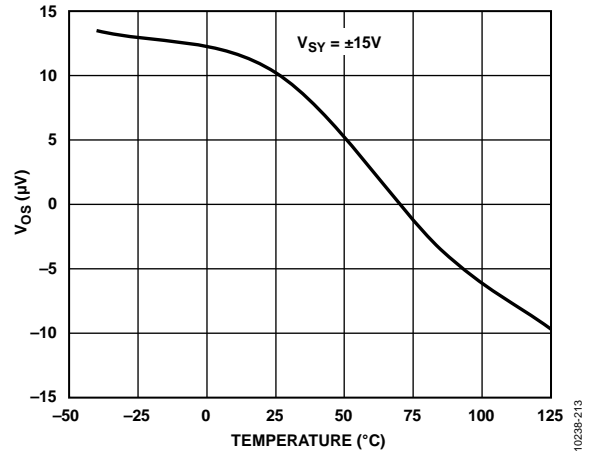


Figure 16. Offset Voltage (V_{OS}) vs. Temperature, $V_{SY} = \pm 15V$

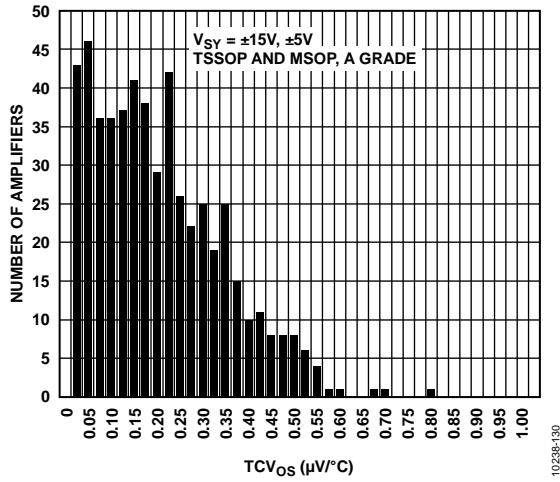


Figure 17. TCVos (TSSOP and MSOP, A Grade)

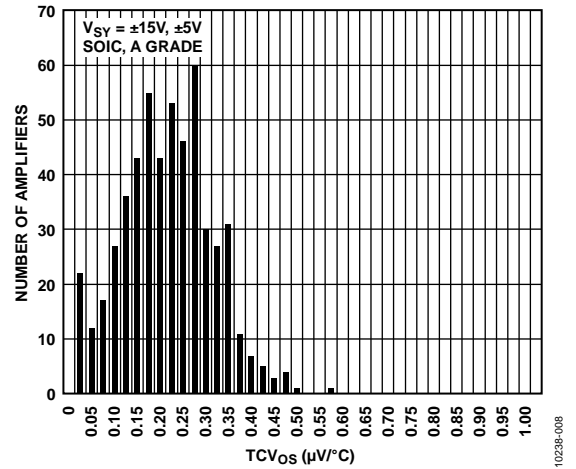


Figure 20. TCVos (SOIC, A Grade)

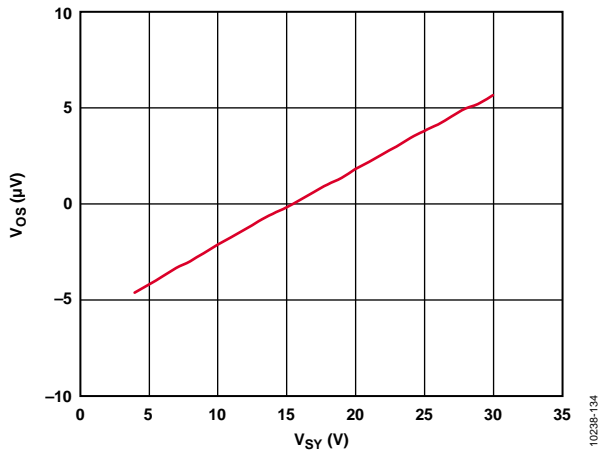


Figure 18. Offset Voltage (V_{OS}) vs. Voltage Supplies (V_{SY})

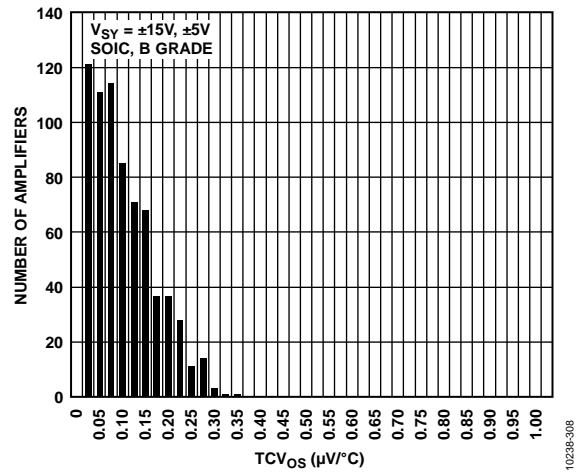


Figure 21. TCVos (SOIC, B Grade)

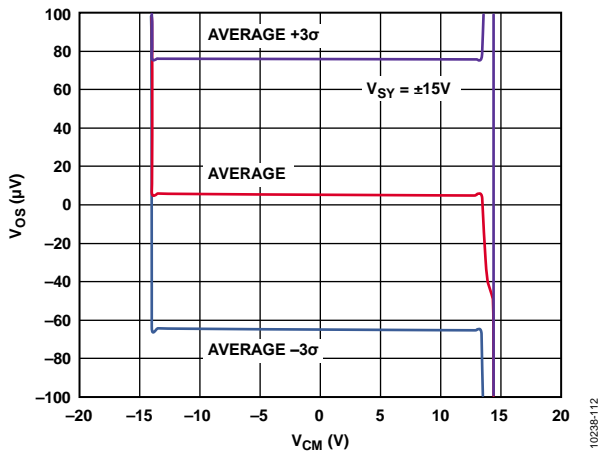


Figure 19. Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = \pm 15\text{ V}$

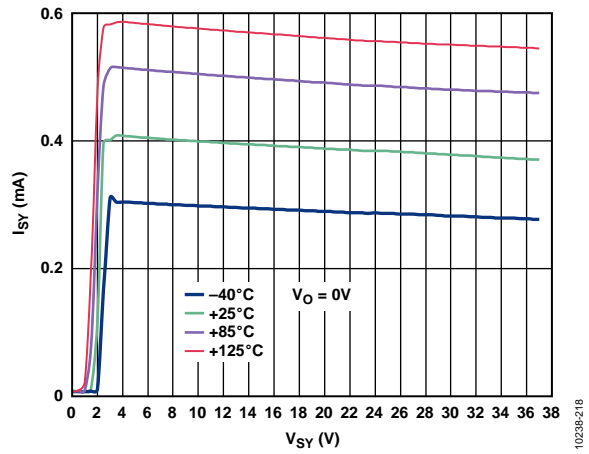


Figure 22. Supply Current per Amplifier (I_{SY}) vs. Power Supply Voltage (V_{SY})

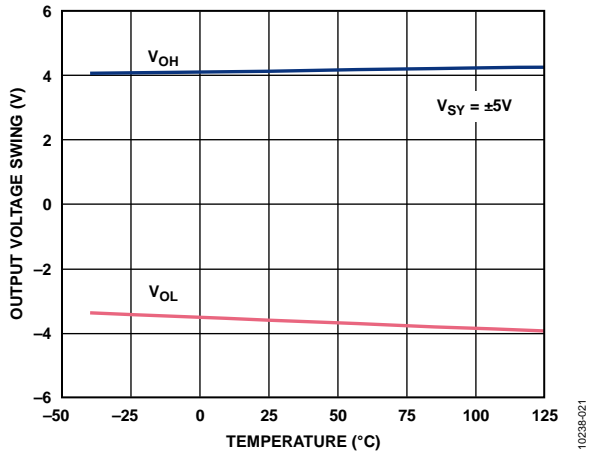


Figure 23. Output Voltage Swing vs. Temperature, $V_{SY} = \pm 5V$

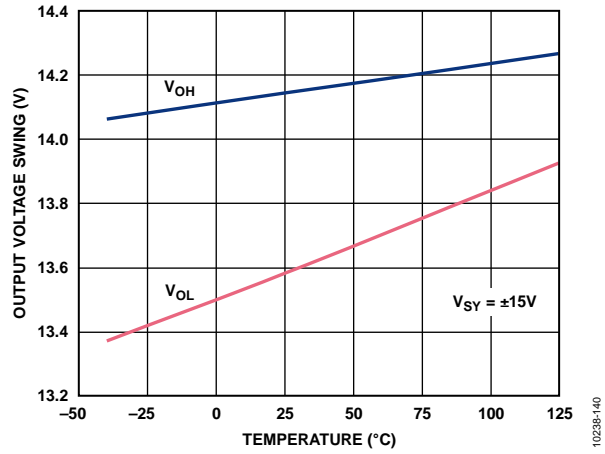


Figure 26. Output Voltage Swing vs. Temperature, $V_{SY} = \pm 15V$

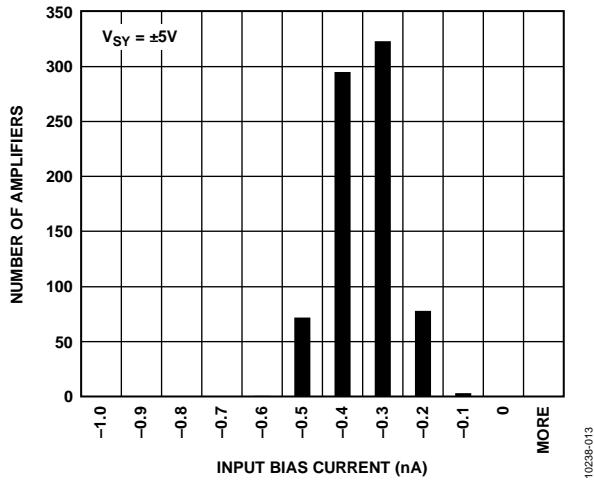


Figure 24. Input Bias Current, $V_{SY} = \pm 5V$

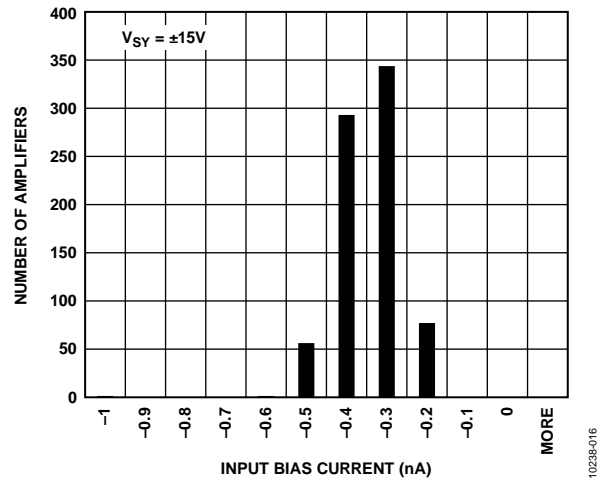


Figure 27. Input Bias Current, $V_{SY} = \pm 15V$

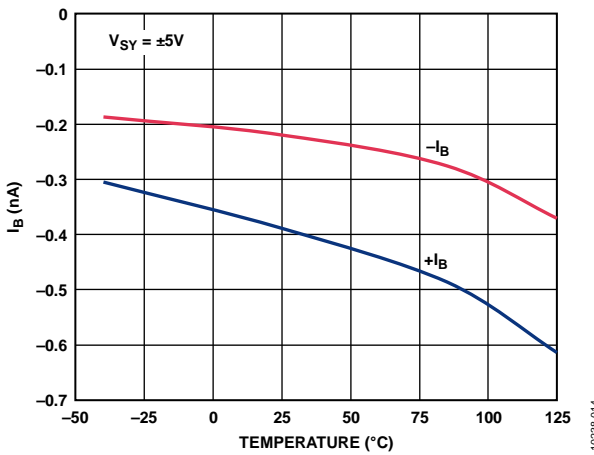


Figure 25. Input Bias Current (I_b) vs. Temperature, $V_{SY} = \pm 5V$

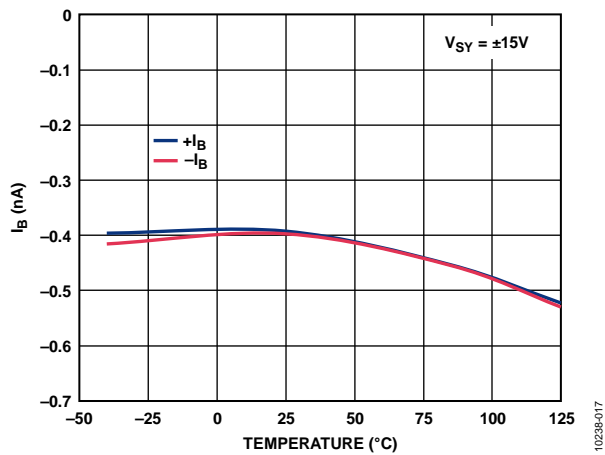


Figure 28. Input Bias Current (I_b) vs. Temperature, $V_{SY} = \pm 15V$

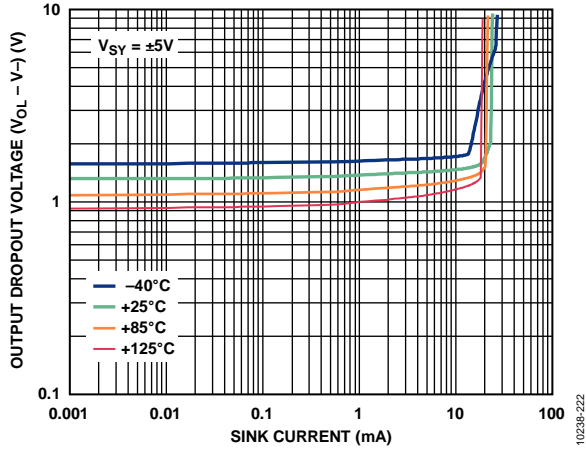


Figure 29. Output Dropout Voltage vs. Sink Current, $V_{SY} = \pm 5V$

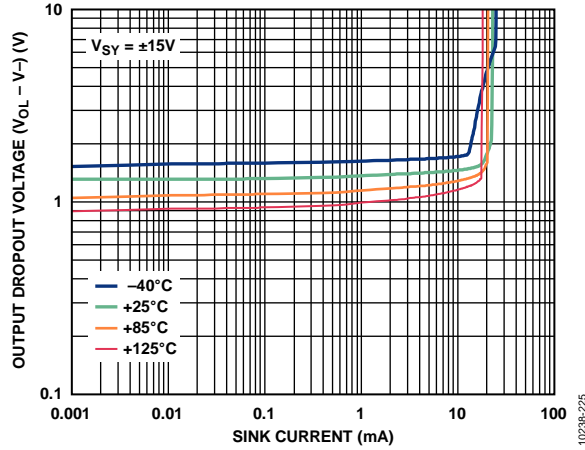


Figure 32. Output Dropout Voltage vs. Sink Current, $V_{SY} = \pm 15V$

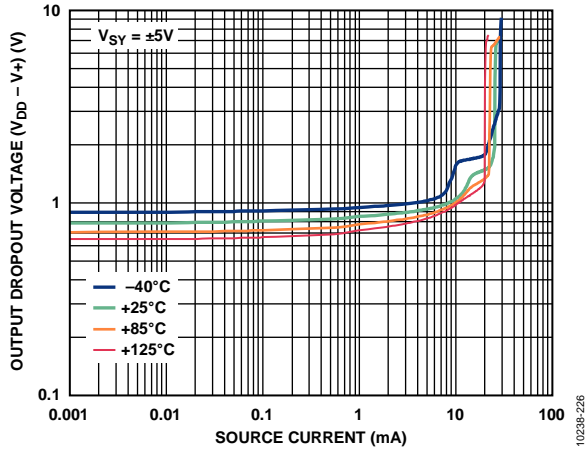


Figure 30. Output Dropout Voltage vs. Source Current, $V_{SY} = \pm 5V$

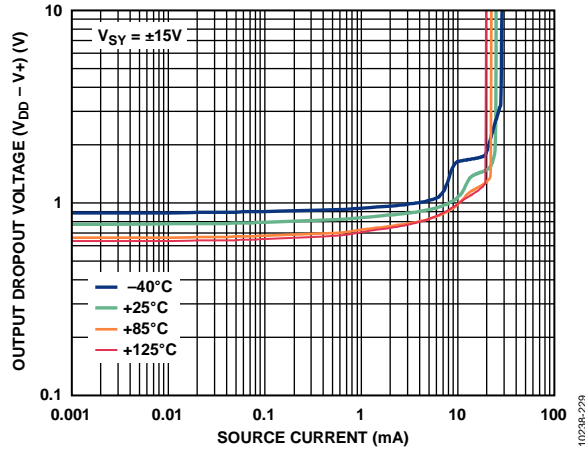


Figure 33. Output Dropout Voltage vs. Source Current, $V_{SY} = \pm 15V$

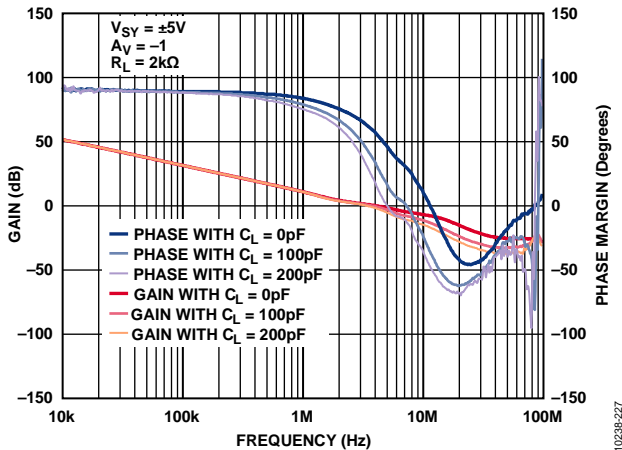


Figure 31. Open-Loop Gain and Phase vs. Frequency, $V_{SY} = \pm 5V$

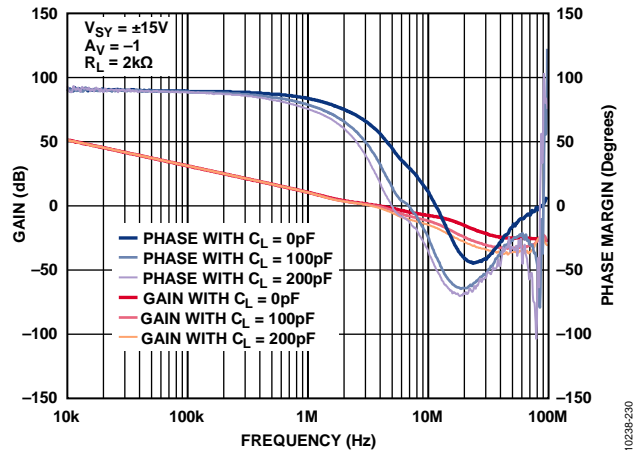


Figure 34. Open-Loop Gain and Phase vs. Frequency, $V_{SY} = \pm 15V$

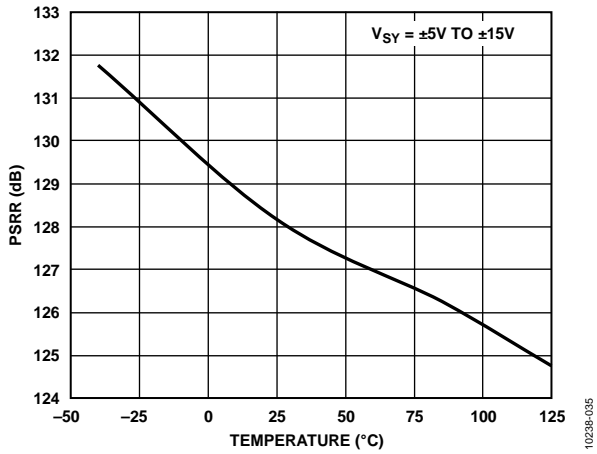


Figure 35. PSRR vs. Temperature, $V_{SY} = \pm 5 V$ TO $\pm 15 V$

10238-035

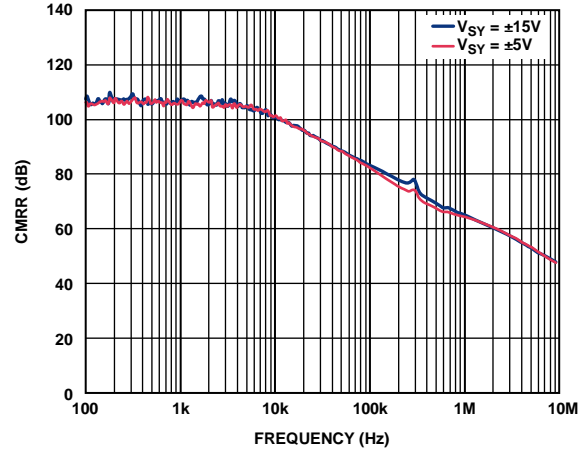


Figure 38. CMRR vs. Frequency, $V_{SY} = \pm 5 V$ and $V_{SY} = \pm 15 V$

10238-029

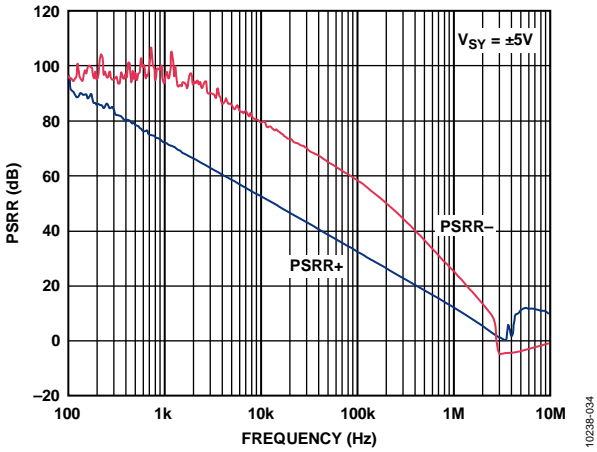


Figure 36. PSRR vs. Frequency, $V_{SY} = \pm 5 V$

10238-034

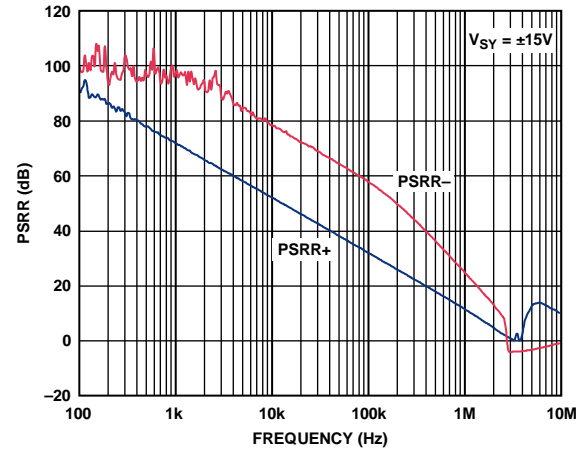


Figure 39. PSRR vs. Frequency, $V_{SY} = \pm 15 V$

10238-037

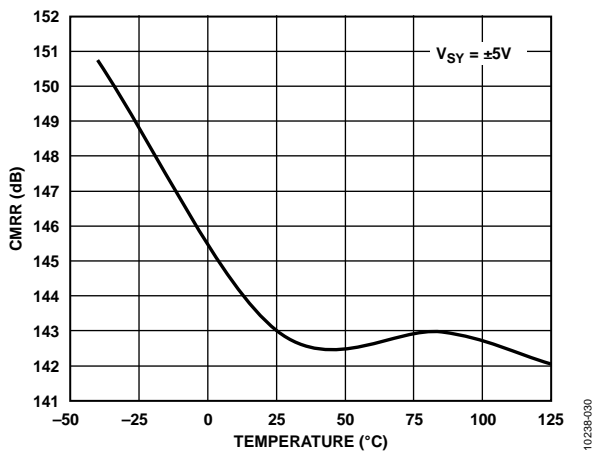


Figure 37. CMRR vs. Temperature, $V_{SY} = \pm 5 V$

10238-030

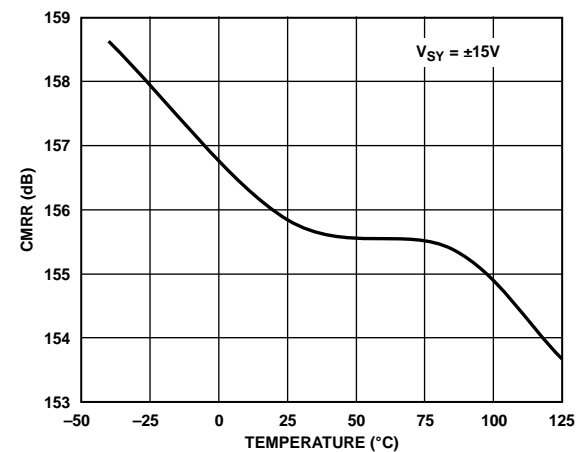


Figure 40. CMRR vs. Temperature, $V_{SY} = \pm 15 V$

10238-033

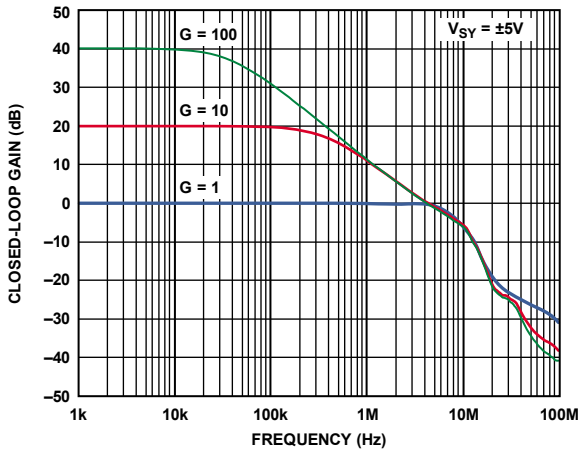


Figure 41. Closed-Loop Gain vs. Frequency, $V_{SY} = \pm 5V$

10238-028

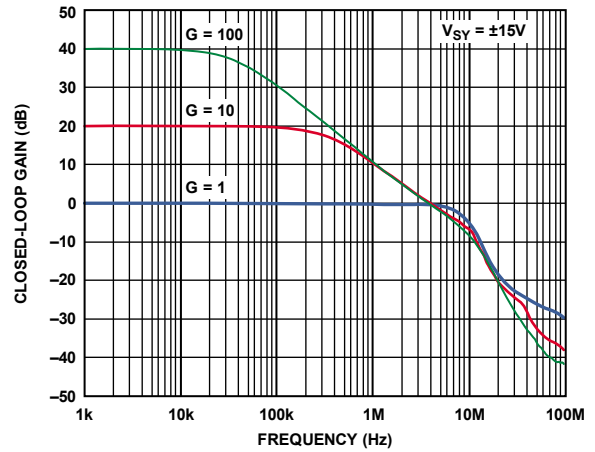


Figure 44. Closed-Loop Gain vs. Frequency, $V_{SY} = \pm 15V$

10238-031

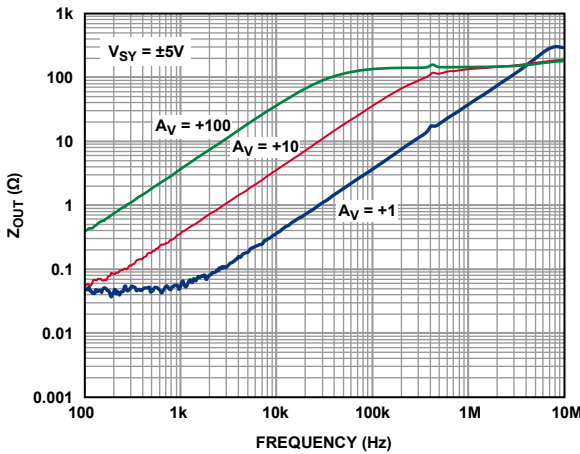


Figure 42. Output Impedance (Z_{OUT}) vs. Frequency, $V_{SY} = \pm 5V$

10238-036

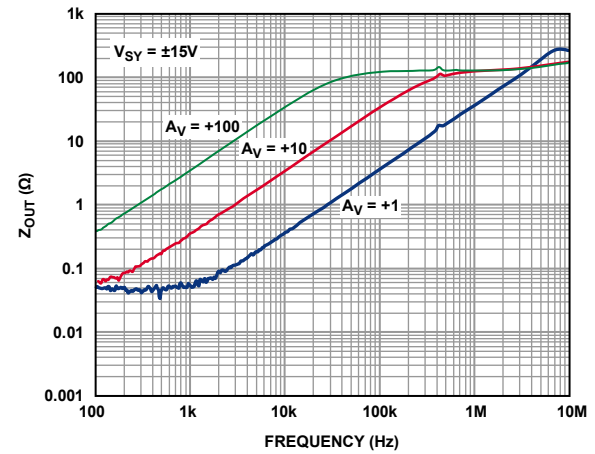


Figure 45. Output Impedance (Z_{OUT}) vs. Frequency, $V_{SY} = \pm 15V$

10238-039

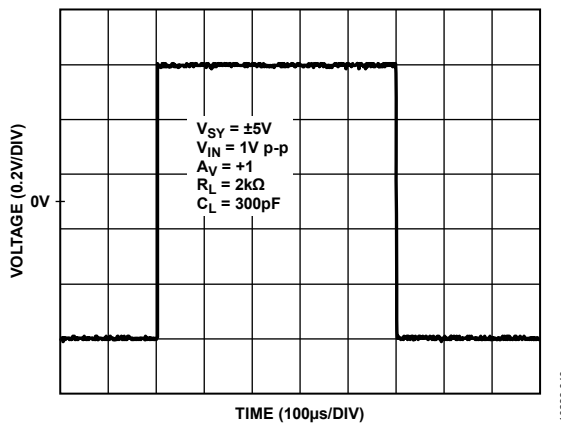


Figure 43. Large Signal Transient Response, $V_{SY} = \pm 5V$

10238-040

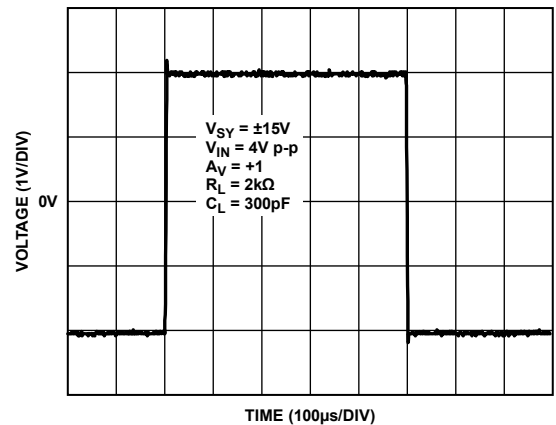


Figure 46. Large Signal Transient Response, $V_{SY} = \pm 15V$

10238-043

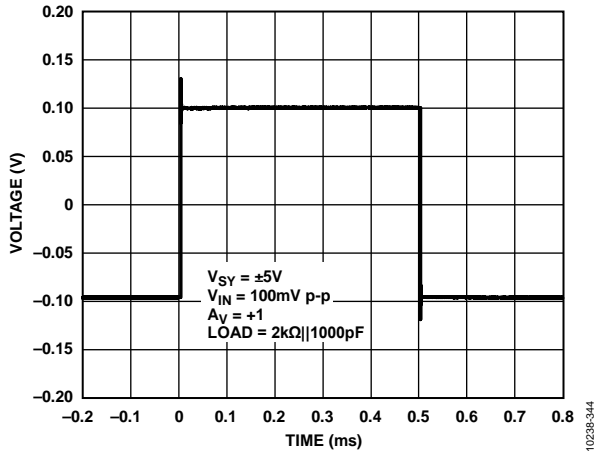


Figure 47. Small Signal Transient Response, $V_{SY} = \pm 5 V$

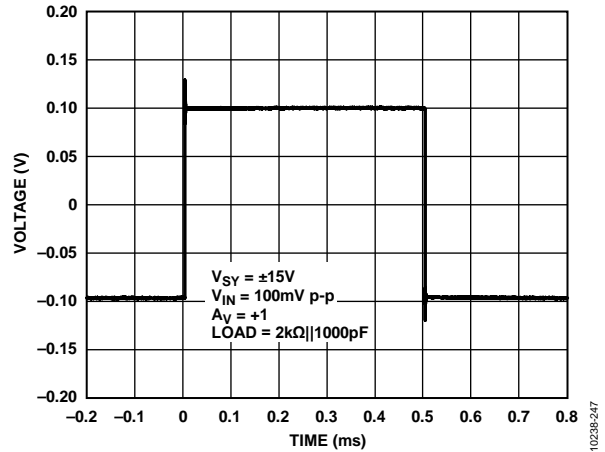


Figure 50. Small Signal Transient Response, $V_{SY} = \pm 15 V$

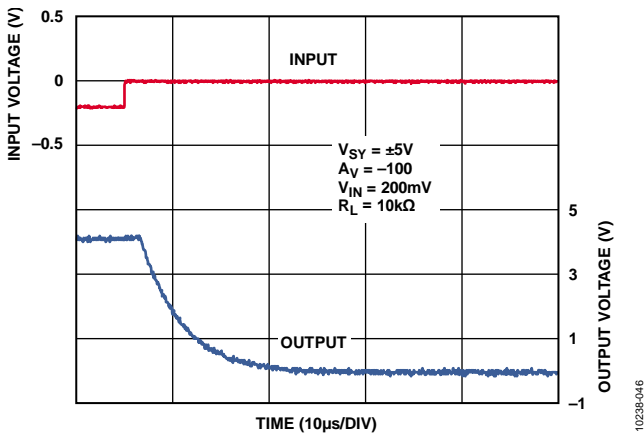


Figure 48. Positive Overload Recovery, $V_{SY} = \pm 5 V$

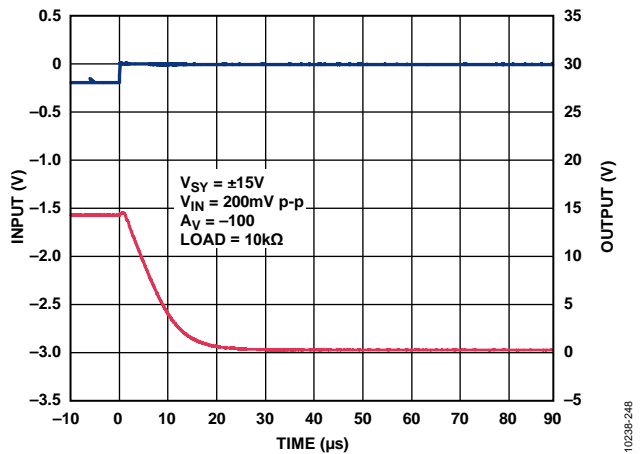


Figure 51. Positive Overload Recovery, $V_{SY} = \pm 15 V$

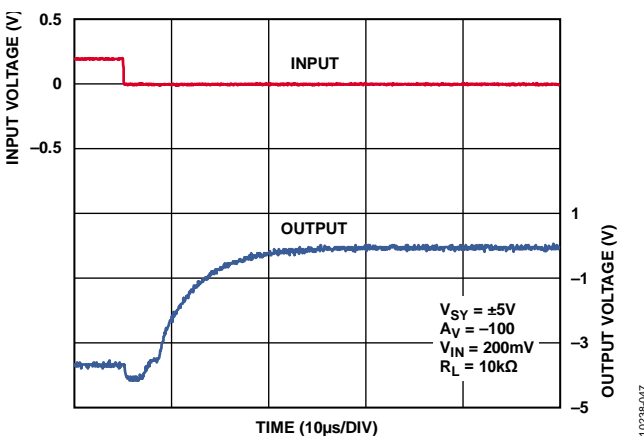


Figure 49. Negative Overload Recovery, $V_{SY} = \pm 5 V$

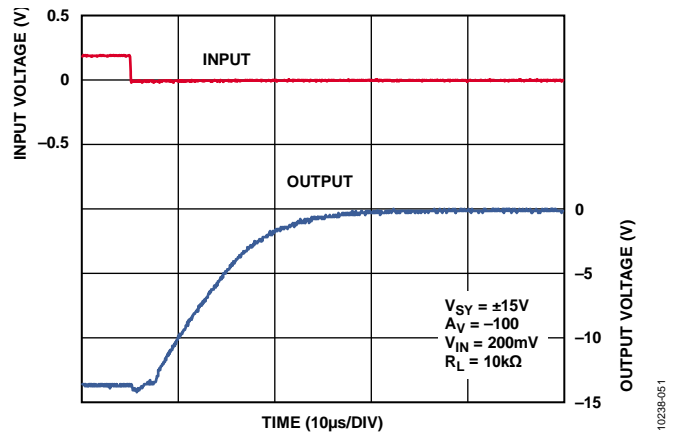


Figure 52. Negative Overload Recovery, $V_{SY} = \pm 15 V$

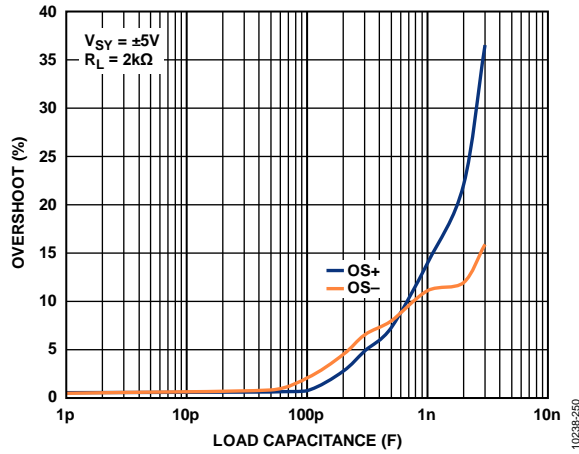


Figure 53. Small Signal Overshoot vs. Load Capacitance, $V_{SY} = \pm 5 V$

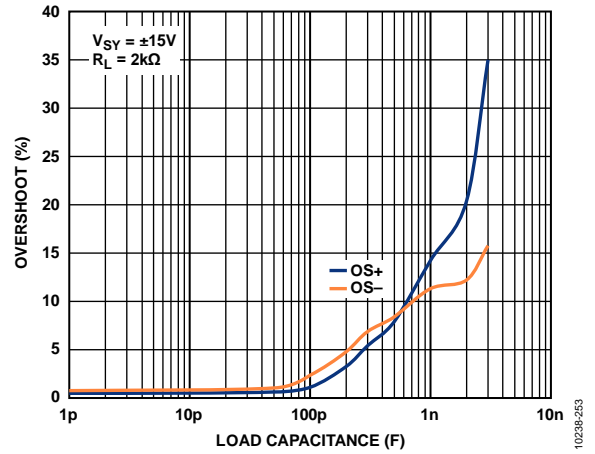


Figure 56. Small Signal Overshoot vs. Load Capacitance, $V_{SY} = \pm 15 V$

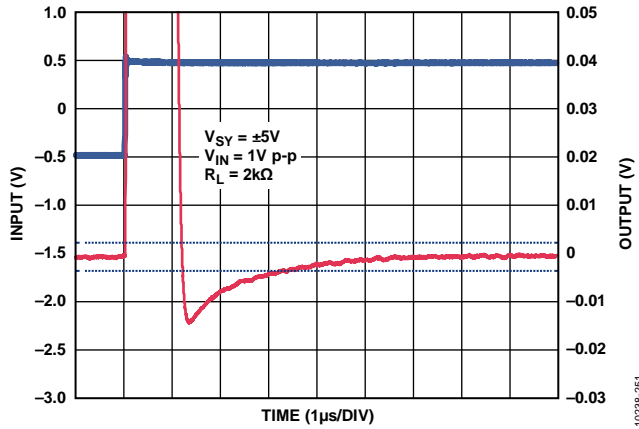


Figure 54. Positive 0.1% Settling Time, $V_{SY} = \pm 5 V$

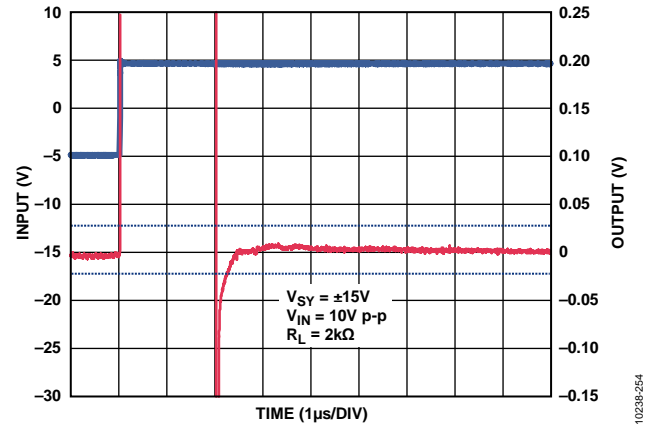


Figure 57. Positive 0.1% Settling Time, $V_{SY} = \pm 15 V$

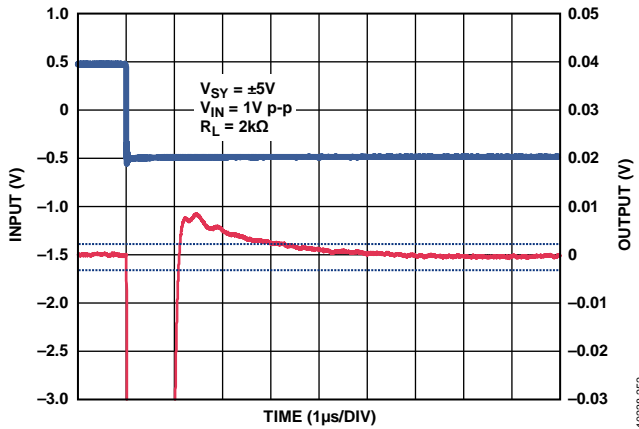


Figure 55. Negative 0.1% Settling Time, $V_{SY} = \pm 5 V$

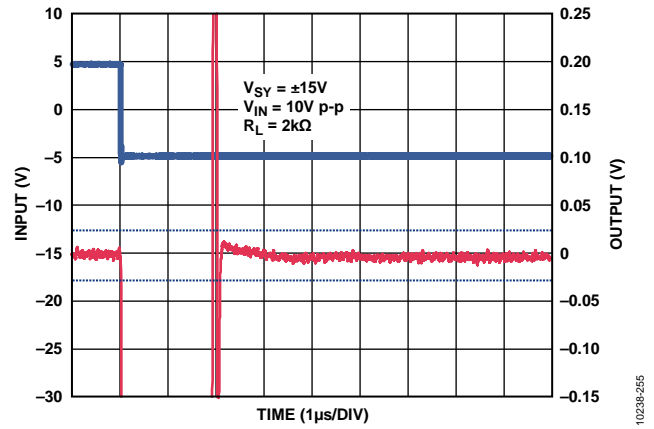


Figure 58. Negative 0.1% Settling Time, $V_{SY} = \pm 15 V$

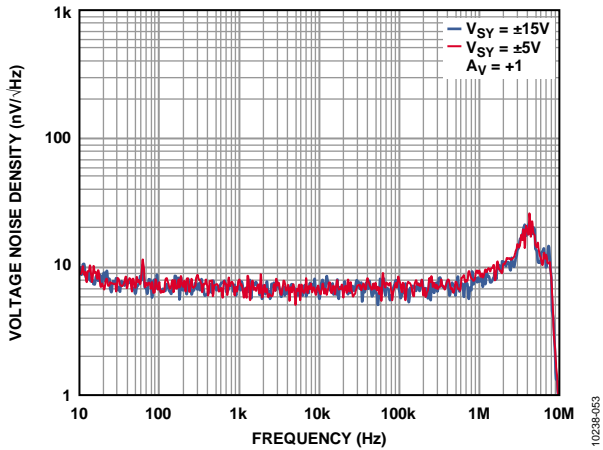


Figure 59. Voltage Noise Density vs. Frequency, $V_{SY} = \pm 5 V$ and $V_{SY} = \pm 15 V$

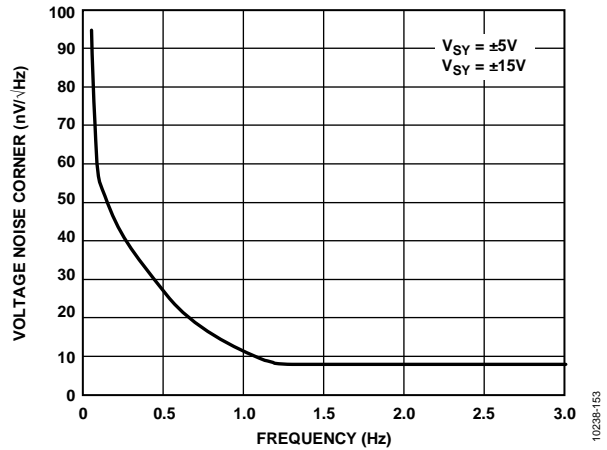


Figure 62. Voltage Noise Corner vs. Frequency, $V_{SY} = \pm 5 V$ and $V_{SY} = \pm 15 V$

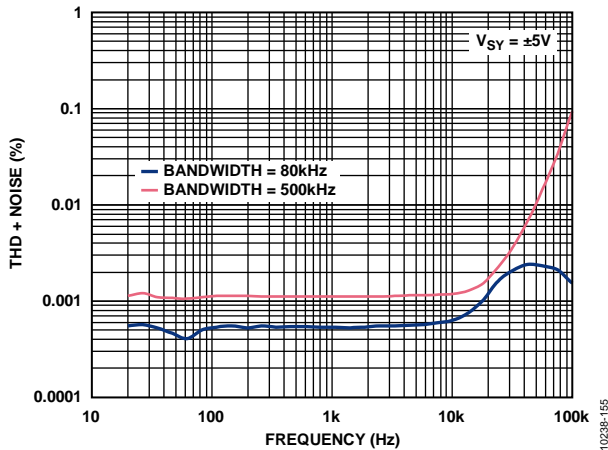


Figure 60. THD + N vs. Frequency, $V_{SY} = \pm 5 V$

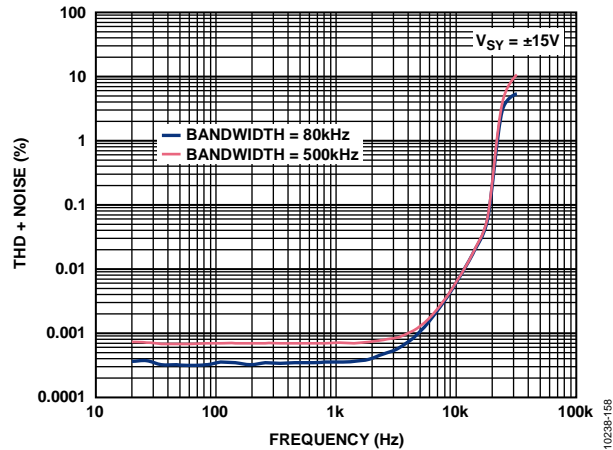


Figure 63. THD + N vs. Frequency, $V_{SY} = \pm 15 V$

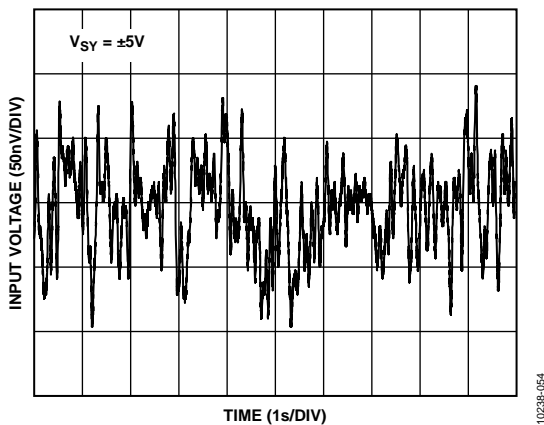


Figure 61. 0.1 Hz to 10 Hz Noise, $V_{SY} = \pm 5 V$

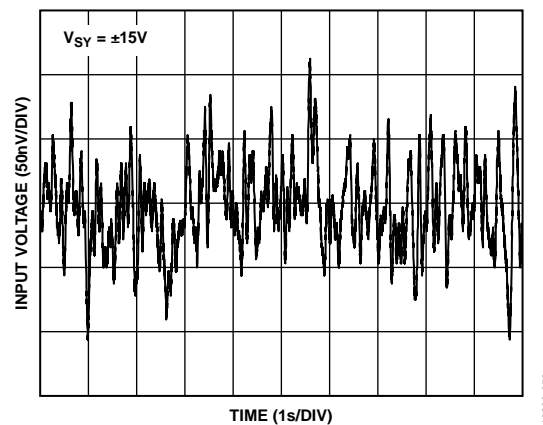


Figure 64. 0.1 Hz to 10 Hz Noise, $V_{SY} = \pm 15 V$

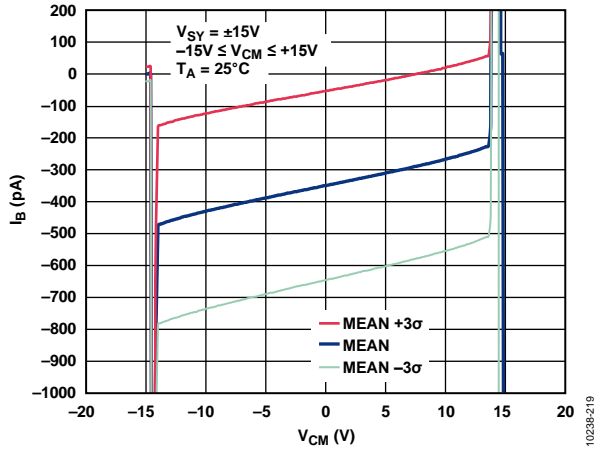


Figure 65. Input Bias Current (I_b) vs. Common-Mode Voltage (V_{CM})

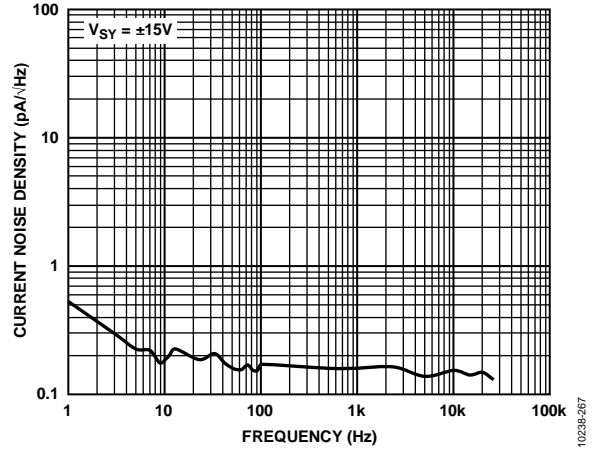


Figure 67. Current Noise Density, $V_{SY} = \pm 15$ V

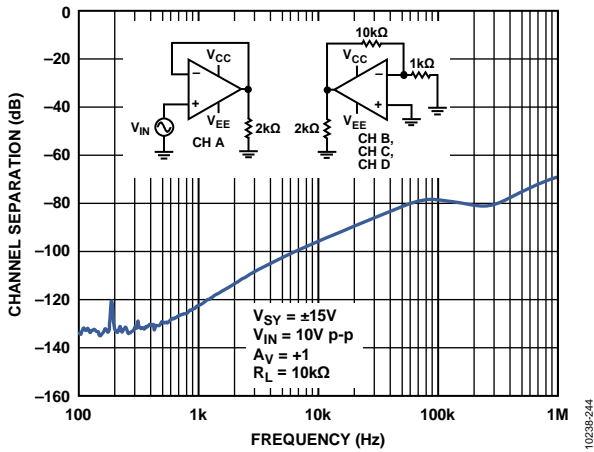


Figure 66. Channel Separation, $V_{SY} = \pm 15$ V

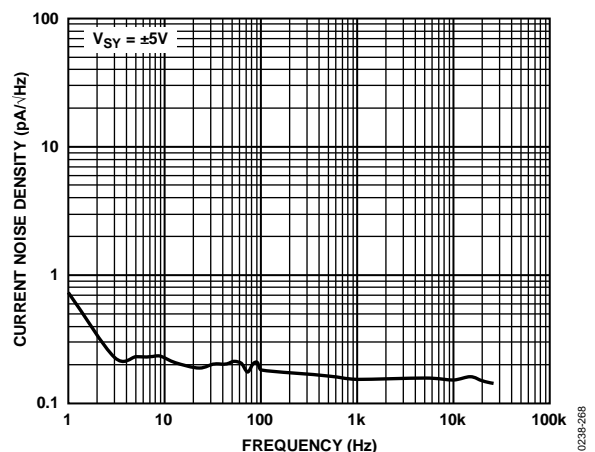


Figure 68. Current Noise Density, $V_{SY} = \pm 5$ V

THEORY OF OPERATION

The [ADA4077-1](#), [ADA4077-2](#), and [ADA4077-4](#) are the sixth generation of the Analog Devices, Inc., industry-standard [OP07](#) amplifier family. The [ADA4077-1](#), [ADA4077-2](#), and [ADA4077-4](#) are high precision, low noise operational amplifiers with a combination of extremely low offset voltage and very low input bias currents. Unlike JFET amplifiers, the low bias and offset currents are relatively insensitive to ambient temperatures, even up to 125°C.

The Analog Devices proprietary process technology and linear design expertise have produced a high voltage amplifier with superior performance to the [OP07](#), [OP77](#), [OP177](#), and [OP1177](#) in tiny, 8-lead SOIC and 8-lead MSOP packages ([ADA4077-1](#) and [ADA4077-2](#)) and 14-lead TSSOP and 14-lead SOIC packages ([ADA4077-4](#)). Despite their small size, the [ADA4077-1](#), [ADA4077-2](#), and [ADA4077-4](#) offer numerous improvements, including low wideband noise, wide bandwidth, lower offset and offset drift, lower input bias current, and complete freedom from phase inversion.

The [ADA4077-1](#), [ADA4077-2](#), and [ADA4077-4](#) have a specified operating temperature range of -40°C to $+125^{\circ}\text{C}$ with an MSL1 rating, which is as wide as any similar device in a plastic surface-mount package. This MSL1 rating is increasingly important as printed circuit board (PCB) and overall system sizes continue to shrink, causing internal system temperatures to rise.

In the [ADA4077-1](#), [ADA4077-2](#), and the [ADA4077-4](#), the power consumption is reduced by a factor of four compared to the [OP177](#), and the bandwidth and slew rate are both increased by a factor of six. The low power dissipation and very stable performance vs. temperature also reduce warmup drift errors to insignificant levels.

Inputs are protected internally from overvoltage conditions referenced to either supply rail. Like any high performance amplifier, maximum performance is achieved by following appropriate circuit and PCB guidelines.

APPLICATIONS INFORMATION

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this phase reversal can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The [ADA4077-1](#), [ADA4077-2](#), and the [ADA4077-4](#) are immune to phase reversal problems even at input voltages beyond the power supply settings.

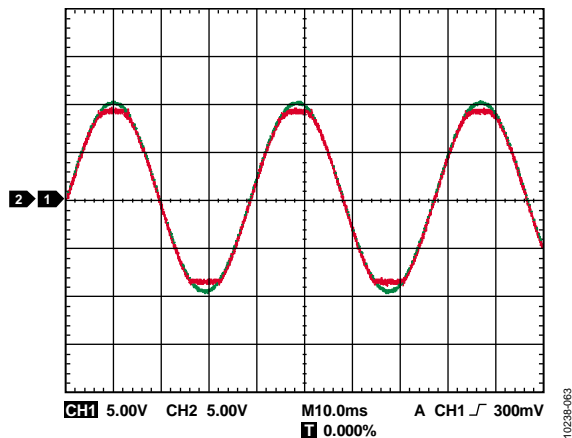


Figure 69. No Phase Reversal

LOW POWER LINEARIZED RTD

A common application for a single element varying bridge is a resistance temperature detector (RTD) thermometer amplifier, as shown in Figure 70. The excitation is delivered to the bridge by a 2.5 V reference applied at the top of the bridge.

RTDs can have a thermal resistance as high as 0.5°C to 0.8°C per mW. To minimize errors due to resistor drift, keep the current low through each leg of the bridge. In this circuit, the amplifier supply current flows through the bridge. However, at a maximum supply current of 500 μ A for the [ADA4077-2](#), the RTD dissipates less than 0.1 mW of power, even at the highest resistance. Therefore, errors due to power dissipation in the bridge are kept under 0.1°C.

Calibration of the bridge is made at the minimum value of the temperature to be measured by adjusting R_P until the output is zero.

To calibrate the output span, set the full-scale and linearity potentiometers to midpoint, and apply a 500°C temperature to the sensor, or substitute the equivalent 500°C RTD resistance.

Adjust the full-scale potentiometer for a 5 V output. Finally, apply 250°C or the equivalent RTD resistance, and adjust the linearity potentiometer for 2.5 V output. The circuit achieves higher than $\pm 0.5^\circ\text{C}$ accuracy after adjustment.

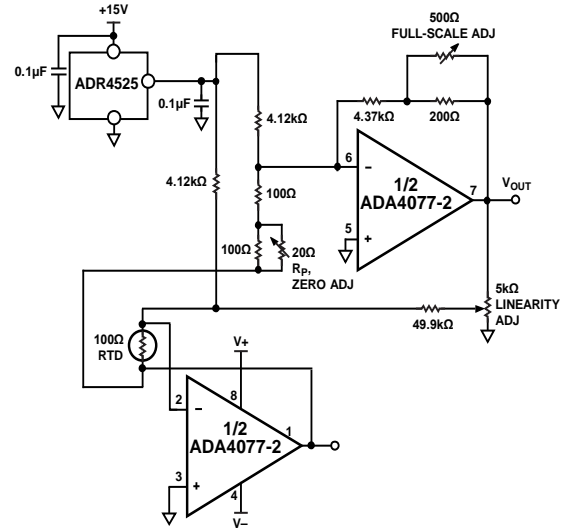


Figure 70. Low Power Linearized RTD Circuit

PROPER BOARD LAYOUT

The [ADA4077-1](#), [ADA4077-2](#), and [ADA4077-4](#) are high precision devices. To ensure optimum performance at the PCB level, care must be taken in the design of the board layout.

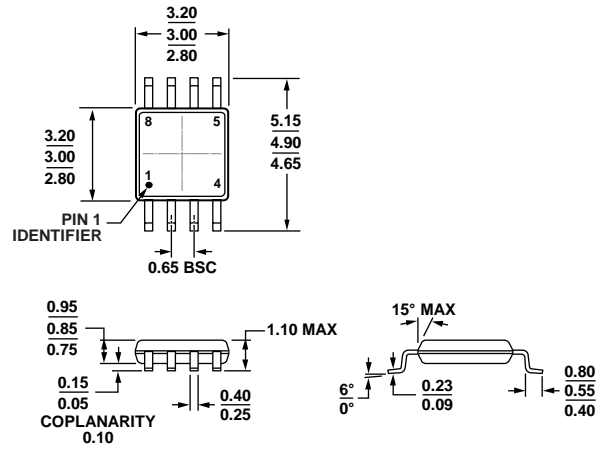
To avoid leakage currents, maintain a clean and moisture free board surface. Coating the surface creates a barrier to moisture accumulation, and reduces parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes the power supply disturbances caused by the output current variation, such as when driving an ac signal into a heavy load. Connect bypass capacitors as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that the signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Ensure, where possible, that input signal paths contain matching numbers and types of components, to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Place matching components in close proximity to each other, and orient them in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and maintains a constant temperature across the circuit board.

OUTLINE DIMENSIONS

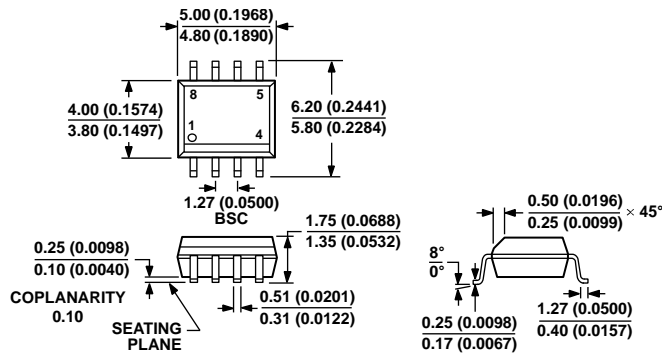


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 71. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

1007-2009-B

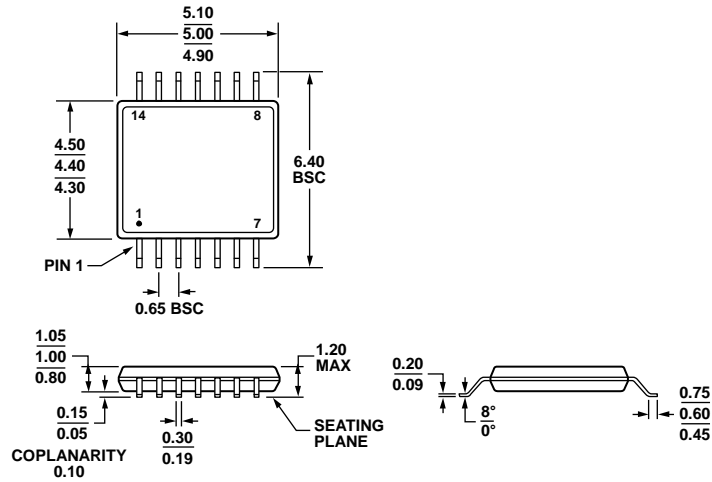


COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 72. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407-A

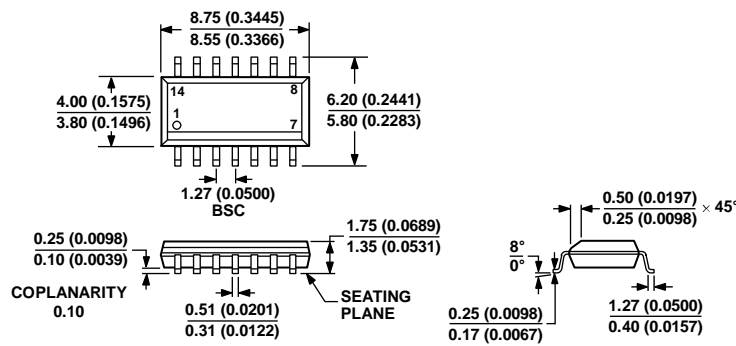


COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 73. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061908-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 74. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)

068606-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADA4077-1ARMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A35
ADA4077-1ARMZ-R7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A35
ADA4077-1ARMZ-RL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A35
ADA4077-1ARZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-1ARZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-1ARZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-1BRZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-1BRZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-1BRZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARMZ-R7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARMZ-RL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-4ARUZ	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4077-4ARUZ-R7	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4077-4ARUZ-RL	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4077-4ARZ	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADA4077-4ARZ-R7	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADA4077-4ARZ-RL	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	

¹ Z = RoHS Compliant Part.