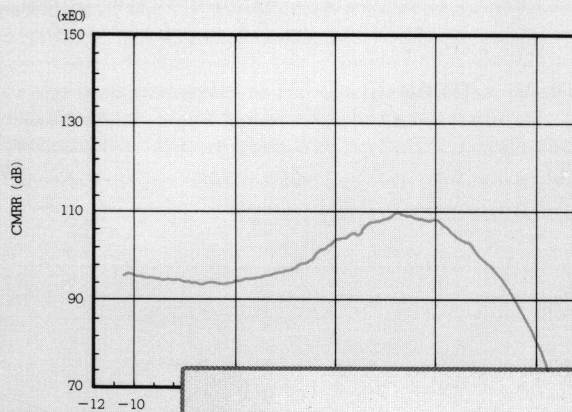
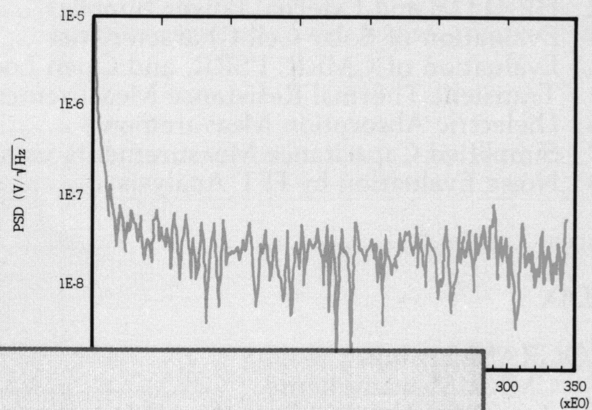
Application Note 356-1

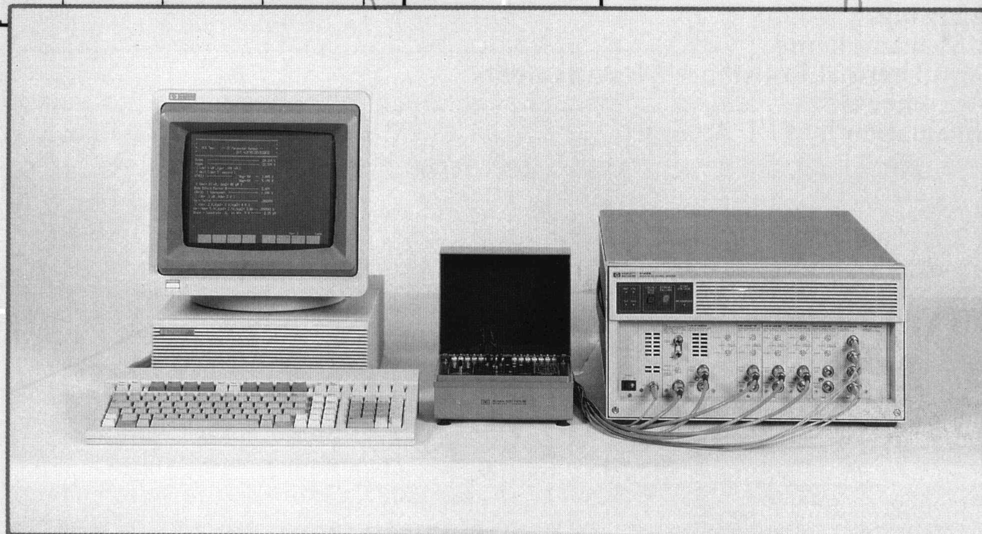
HEWLETT PACKARD

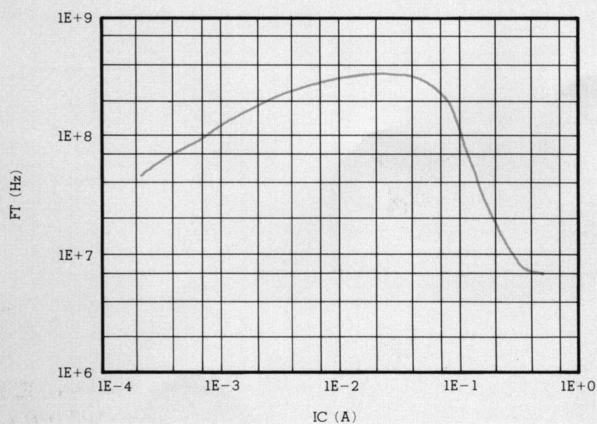
— HP 4142B Modular DC Source/Monitor —

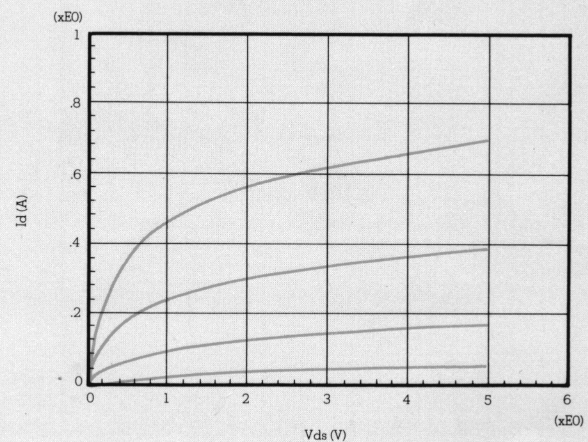
Techniques and Applications for High Throughput and Stable Characterization











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INTRODUCTION

The HP 4142B Modular DC Source/Monitor is a high speed, highly accurate computer-controlled DC parametric measurement instrument for characterizing semiconductor devices, such as MOSFETs, GaAs devices, operational amplifiers, etc., plus other components, such as capacitors, insulators, etc.

This Application Note provides helpful information on using the HP 4142B, and includes many application examples.

Chapter 1 describes techniques for high-speed measurement of low currents, and how to prevent oscillation in high-frequency semiconductor devices.

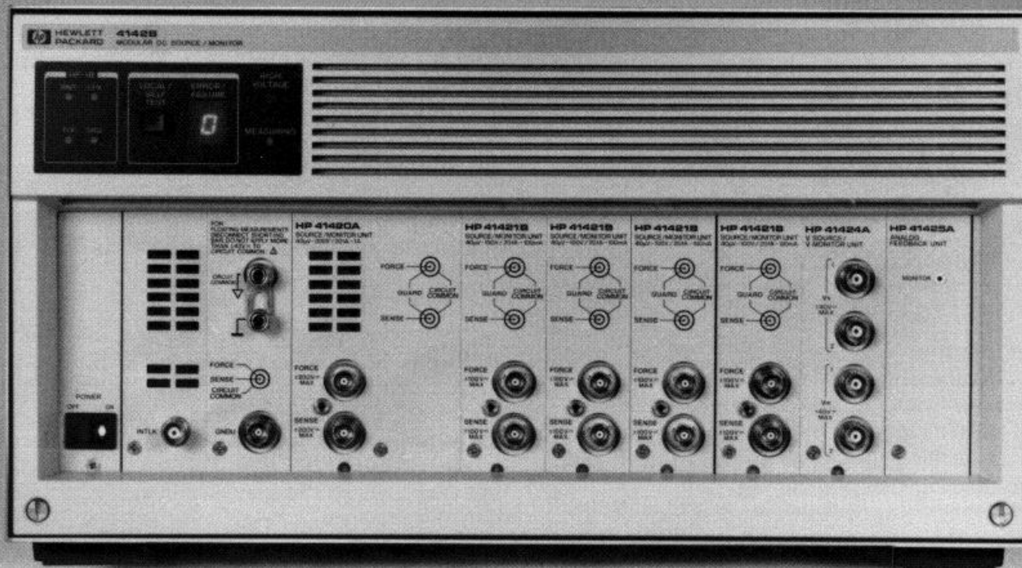
Chapter 2 describes practical application examples utilizing the Analog Feedback Unit (AFU) and various testing capabilities of the HP 4142B such as synchronous staircase sweep, high-speed spot measurements, etc.

For the basic principles of HP 4142B operation, refer to the application note "High Speed DC characterization of Semiconductor Devices from Sub pA to 1A" (Application Note 356).

Module Configuration as shown below

Model	Description	Quantity
HP 41420A	Source Monitor Unit 40μV~200V/20fA~1A	1
HP 41421B	Source Monitor Unit 40μV~100V/20fA~100mA	4
HP-41424A	Voltage Source/ Voltage Monitor Unit 1mV~40V, 20μA~100mA/4μV~40V	1
HP 41425A	Analog Feedback Unit	1

HP 4142B Modular DC Source/Monitor



1. TECHNIQUES FOR HIGH THROUGHPUT AND STABLE CHARACTERIZATION

1.1 High Speed Measurements of Very Low Currents

Electronic devices made by advance process technology, such as micro lithography, require highly accurate high speed measurements of very low currents. This section describes several programming techniques that will enable you to make high-speed, low currents measurements.

Generally, the higher the accuracy of measuring picoampere-level currents, the longer the measurement time. This is due to the following reasons:

1. The ranging time required for switching to a low current range increases.
2. A lower current range requires longer time for charging the parasitic capacitance of devices and the test system.
3. Since the frequency bandwidth of the measuring instrument is narrower with a lower current range, the settling time becomes longer.
4. Lower current ranges require a longer time for averaging in order to reduce the influence of noise.
5. In low current ranges, devices and dielectric absorption elements in a test system have a great influence on the time required for settling after a change of set voltage.

Important points for compensating for these conditions when measuring low currents at high speed using the HP 4142B are described below.

• Minimize Ranging Time

If a current range is not specified, HP 4142B operates in the auto-ranging mode. In other words, the current ranges are switched one by one, starting from the range determined by current compliance, until the current range of maximum resolution without overflow is reached. The HP 4142B has ten current ranges. This means that it may be necessary to traverse across as many as nine ranges in some cases.

Table 1.1.1 lists typical times required for switching from one range to another. The values in the table include waiting time accompanying range-switching operation. The table shows that the lower the final current range in auto-ranging mode, the longer the time required for switching (ranging time).

Table 1.1.1 Typical Time Required for Switching from One Range to Another

I range	Ranging time
100 μA ~ 1A	10 ms
10nA ~ 100 μA	20 ms
1 nA ~ 10nA	50 ms

To specify a current range, two ranging methods are available: Limited Auto-Ranging and Fixed-Range. Limited Auto-Ranging allows automatic range changes between the specified range and higher ranges. This method does not involve unnecessary switching to a lower current range, and thereby reduces the ranging time accordingly.

Another method is Fixed-Range operation, in which the range is switched from the present range to a specified range along the shortest route. For example, switching from 100μA (initial range) to 1 nA (minimum range) in the fixed range mode takes about 50 ms including waiting time (>130 ms in auto-ranging mode). Therefore, to minimize the ranging time, it is recommended to specify a range and switch to it in the Limited Auto-Ranging mode or Fixed-Range mode.

• Consideration of Balance between Maximum Resolution and Measurement Waiting Time

Table 1.1.2 lists the ratio of measurement waiting time of three low current ranges (taking the waiting time for the 100 nA range as 1) and the maximum measurement resolution.

The table shows that in low current ranges the waiting time doubles successively for each lower range. It is therefore desirable to select the range that provides acceptable resolution with as large a full scale as possible.

Table 1.1.2

I range	Wait time*	Resolution (measurement)
100nA	1	2 pA
10nA	2.4	200 fA
1nA	5.5	20 fA

* Ratio from the time at 100 nA

• Minimizing Settling Time

The settling time is the time required to settle to a newly set value when the setting of the Source/Monitor Unit (SMU) output is changed. The settling time consists of a slewing period and a period of convergence to a final value.

Figure 1.1.1 shows an example of a measurement circuit applying a voltage to a load resistance. figure 1.1.1 (a) shows the case of a purely resistive load. The SMU output rises at the maximum slew rate, which is determined by the SMU current range and current compliance. Figure 1.1.3 shows the maximum slew rate with respect to current compliance.

In actuality, there are stray capacitances in the measurement environment, such as in the instrument, cabling, fixturing and DUT, so the slew rate is limited by current compliance Ic and load capacitance C_L to Ic/C_L.

Figure 1.1.2 shows this situation with the SMU operation curve. Route ⓐ corresponds to figure 1.1.1 (a), and routes ⓑ and ⓑ' to figure 1.1.1 (b). In other words, if the DUT has parasitic capacitances, the SMU operates with constant current while the voltage is rising.

Route ⓑ represents the case of small-current compliance, and ⓑ' large current compliance. It is assumed, in the case of route ⓑ', the current is decided by the maximum slew rate of the SMU, while, in other case ⓑ, the current is limited by the current compliance.

After the slewing period, the SMU operates with constant voltage (from points B and B') until converging to the final value at point A. This period of convergence is longer for lower current ranges.

Thus, to minimize the settling time, set as large a current compliance as possible when changing SMU output.

• Example

This section gives an example of measuring low currents using an actual device. Figure 1.1.4 shows a measurement circuit, items being measured, and test conditions. Figure 1.1.5 shows the SMU output voltage waveforms during the measurement: (a) corresponds to leakage current measurement in the auto-ranging mode, and (b), to the measurement in the limited auto-ranging mode. This shows that the total measurement time is reduced by about half.

Figure 1.1.1 SMU Output Change

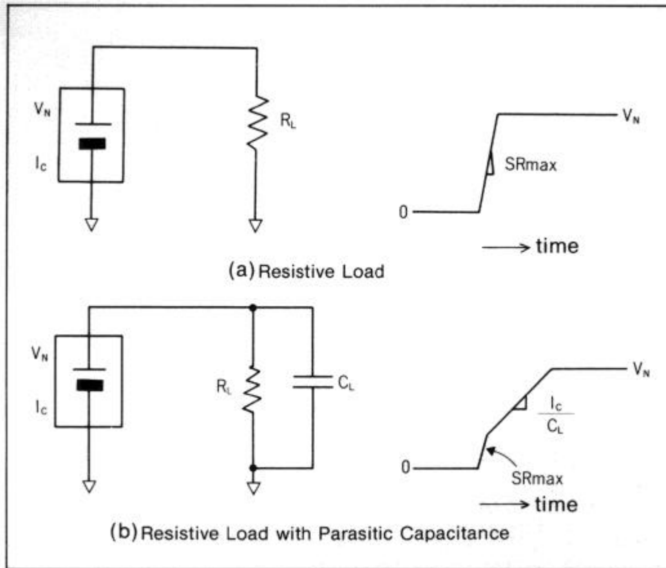


Figure 1.1.2 Operating Curve of SMU

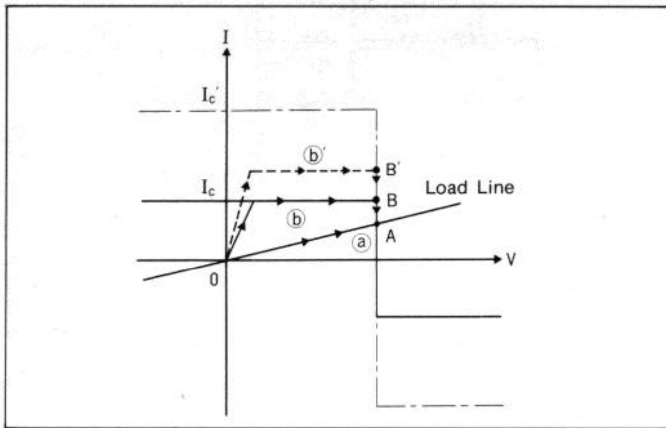


Figure 1.1.3 Maximum Slew Rate in I Source Mode

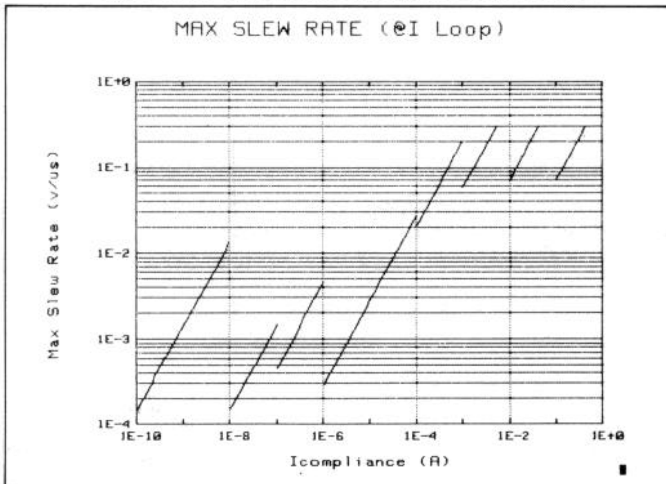
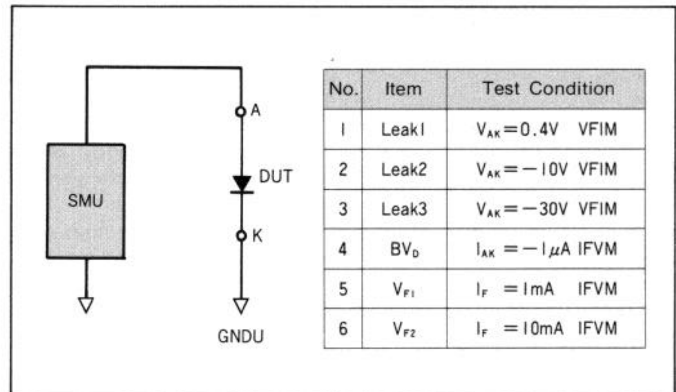


Figure 1.1.4 Diode Test Example



No.	Item	Test Condition
1	Leak1	V_{AK}=0.4V VFIM
2	Leak2	V_{AK}=−10V VFIM
3	Leak3	V_{AK}=−30V VFIM
4	BV_D	I_{AK} =−1μA IFVM
5	V_{F1}	I_F =1mA IFVM
6	V_{F2}	I_F =10mA IFVM

Figure 1.1.5 (a) SMU Output Waveform in Auto-Ranging Mode

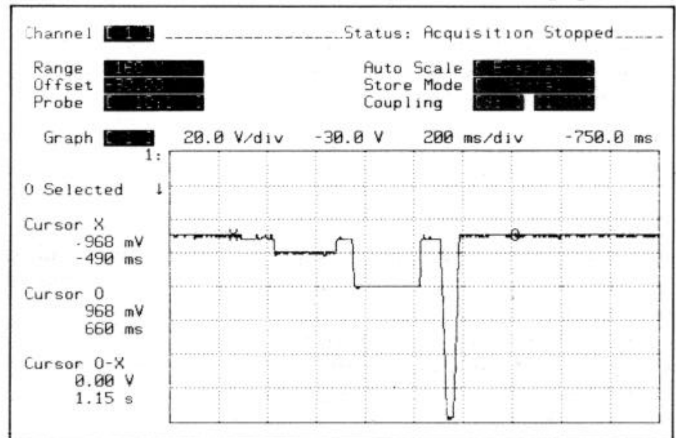
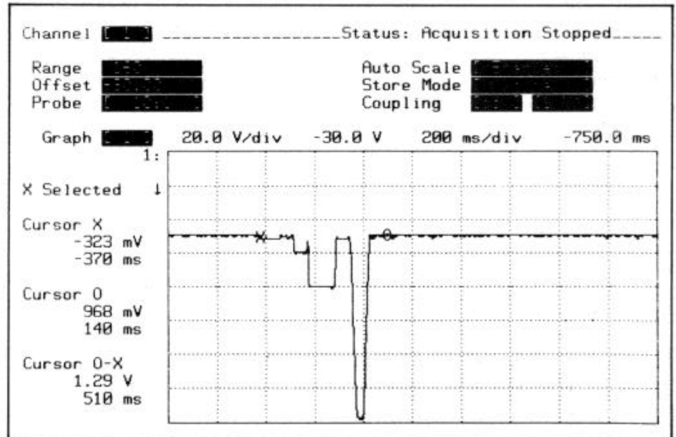


Figure 1.1.5 (b) SMU Output Waveform in Limited Auto-Ranging Mode



1.2 Preventing Oscillation in High-Frequency Devices

When measuring parameters (HFE, gm, etc.) of high-frequency devices like power MOSFETs, GaAs MESFETs and high-frequency bipolar transistors using an HP 4142B SMU, oscillation may cause measurement problems. This section describes oscillation problems and techniques for solving them.

There are two type of oscillation that may occur when using SMUs.

1. Oscillation Related to the SMU
(Oscillation frequency < 300 kHz)

(1) Oscillation of SMU output part (guard amplifier*) caused by inductive load
(2) Oscillation when inductive load is connected to SMU in I source mode.

* *Note: The guard amplifier forces a guard voltage. (See A/N356 p.2.)*

2. Oscillation Not Related to the SMU
(Oscillation frequency > 3 MHz)
Oscillation associated with the following devices:

(1) FETs (power MOSFETs, GaAs MESFETs)
(2) High frequency bipolar transistors

Oscillation in 1. may not arise as a problem because the minimum capacitance required to prevent oscillation is added to the SMU output part. This section, therefore, will focus on the oscillation not related to the SMU.
This section uses GaAs MESFET as an example and describes conditions for oscillation and techniques to prevent oscillation.

• Conditions for Oscillation
Figure 1.2.1 shows the general setup of a measurement circuit. Suppose that both drain and gate are connected to the SMU in the voltage mode via a cable of 1.5 m to 3 m length.
Figure 1.2.2 shows an AC equivalent circuit. The output impedance of the SMU at 3 MHz or higher is capacitive regardless of the SMU operation mode (voltage/current mode) and so can be considered as equivalent to a common voltage. It can be seen that this circuit forms a negative feedback amplifier, with feedback by Cgd. If this negative feedback amplifier meets the conditions for oscillation, it becomes a Hartley oscillator. The frequency of oscillation of the circuit is expressed as

$$f_o = \frac{1}{2\pi\sqrt{LgCgd}}$$

When Lg = 1 μH and Cgd = 100 pF, the frequency of oscillation is calculated as

$$f_o = \frac{1}{2\pi\sqrt{10^{-6} \cdot 10^{-10}}} \fallingdotseq 16 \text{ MHz}$$

Figure 1.2.1 General Setup of a Measurement Circuit

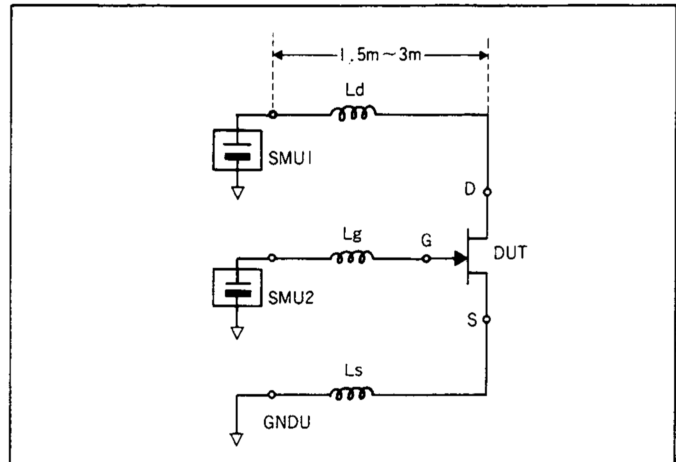


Figure 1.2.2 AC Equivalent Circuit

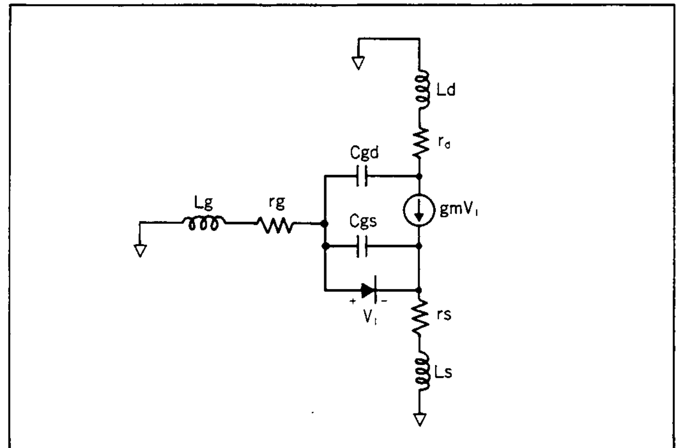


Figure 1.2.3 Equivalent Circuit with an Open Feedback Loop

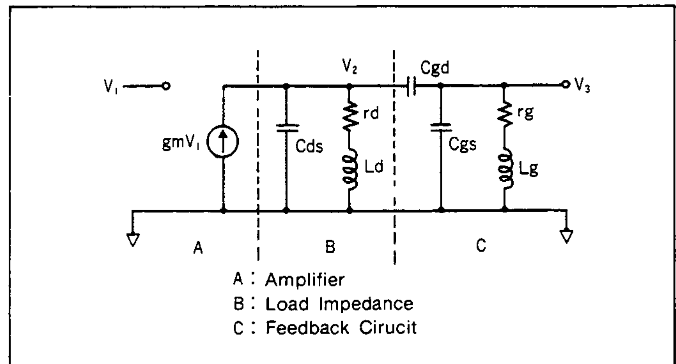
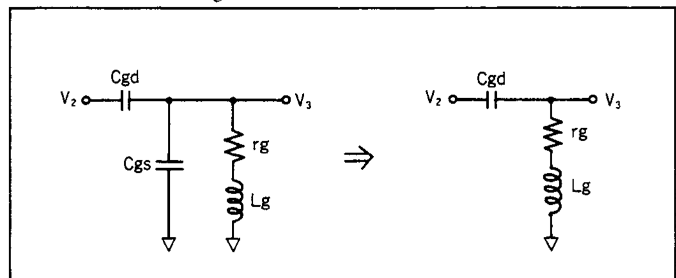


Figure 1.2.4 Feedback Circuit



Next, let us examine the conditions for oscillation from the aspect of loop gain. Figure 1.2.3 shows an equivalent circuit with an open feedback loop. In the figure, rs and Ls are stabilizing elements and considered as 0 in the worst case. The voltage-controlled current source is inverted to make the polarity of loop gain positive. The equivalent circuit can be divided into three blocks: amplifier, load impedance, and feedback circuit.

Now, let us look at the feedback circuit. In a frequency range of 3 to 30 MHz, we can assume the following:

$$\frac{1}{\omega Cgs} >> \omega Lg$$

Cgs, therefore, can be omitted. As a result, the feedback circuit can be represented as shown in figure 1.2.4. Figure 1.2.5 shows the transfer characteristic of the circuit.

Figure 1.2.5 (a) shows the gain and phase characteristics, and figure 1.2.5 (b) the characteristics represented on a vector plane.

The transfer characteristic of the feedback circuit has a resonance point, the peak of which is equal to Q of a series resonance circuit.

Next, let us look at the load impedance. In a frequency range of 3 to 30 MHz, the following can be assumed:

$$\frac{1}{\omega Cgs} >> \omega Ld$$

The load impedance, therefore, can be considered to be inductive.

Thus, the frequency characteristic of loop gain is represented on a vector plane (Nyquist Plane) as shown in figure 1.2.6 ⓐ. In the figure, point U (-1, 0) is where the conditions for oscillation are met, and point P is where loop gain is at its peak. Spacing between points U and P is proportional to the gain margin. As the spacing is reduced, oscillation is more likely to occur. The maximum loop gain at point P is proportional to gm, Q of the feedback circuit, and load inductance Ld. Therefore, conditions for instability are as follows:

- **More unstable as gm increases.**
- **More unstable as Lg increases or rg decreases.**
- **More unstable as Ld increases.**

Figure 1.2.7 shows the qualitative interrelationship of gm, Lg, and rg with respect to their influence on stability.

Figure 1.2.5 Transfer Characteristic of Feedback Circuit

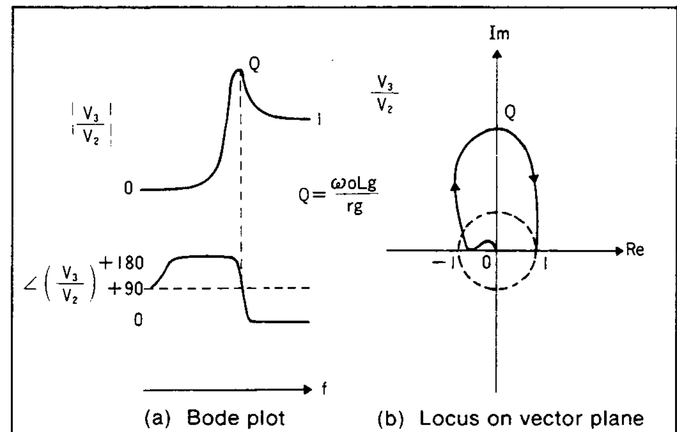


Figure 1.2.6 Loop Gain Characteristics (Nyquist Plane)

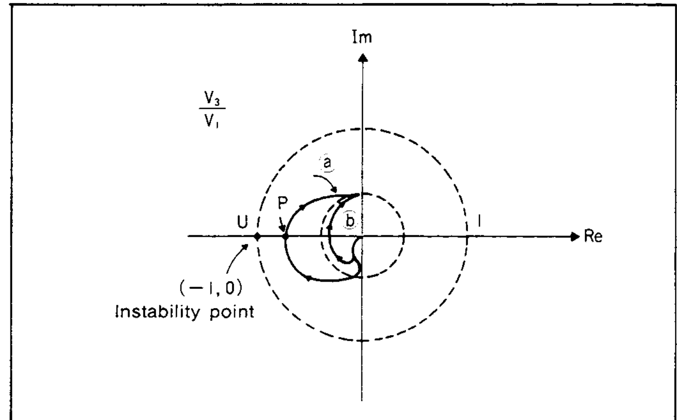
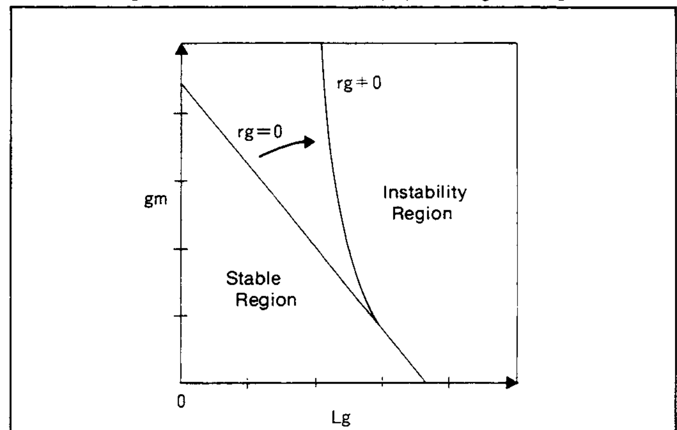


Figure 1.2.7 Interrelationship of Gm, Lg, and rg



• Preventing Oscillation

Taking into consideration the above, the following methods can be used to prevent oscillation (figure 1.2.8).

① Add external series resistance Rg or resistive ferrite beads at the input to the gate.
② Add a series RC circuit between the gate and drain.
③ Add a series RC circuit between the gate and source.
④ Add a bypass capacitor between the drain and source.

Reasons for these methods are explained below.
First, method ① is intended to increase the gain margin by decreasing the Q of the feedback circuit and thereby reducing the loop gain. Since the resistive impedance of ferrite beads is at most 100 ohms or so, devices of large gm require multiple sets of ferrite beads.

To make the measure effective, Rg must meet

$$Rg > \frac{1}{\omega_0 Lg}$$

where ω_0: frequency of oscillation ($\omega_0 = 2\pi fo$)

If an external resistance cannot be inserted, for example when the gate resistance rg of the device itself is to be measured, methods ② and ③ are effective. The additional RC element operates near a resonance point of the feedback circuit to reduce the peak of the loop gain that would occur due to resonance. These methods bring the loop gain to characteristic ⓑ in figure 1.2.6 and thus add an increase of gain margin, thereby stabilizing the operation of the SMU.

To make the solutions effective, the additive elements must meet the following criteria:

$$\text{(i)}\ R_1, R_2 < \sqrt{\frac{Lg}{Cgd}}$$

$$\text{(ii)}\ \frac{1}{C_1R_2}, \frac{1}{C_2R_2} < \omega_0$$

Method ④ reduces the inductance due to a long cable connected to drain and source by means of the bypass capacitor, and thereby decrease the loop gain.

Connect this bypass capacitor as near the device as possible. The capacitance should be in the range 100—1000 pF. Do not use a large capacitance, otherwise the SMU will oscillate or respond slowly.

The above description used a GaAs MESFET as an example of a device. The same solutions can be applied to power MOSFETs and high-frequency bipolar transistors to prevent them from oscillating.

• Example

This section gives an example of oscillation during an actual measurement and describes methods for preventing oscillations. This example concerns the measurement of the Id-Vds characteristics of a GaAs FET having the characteristics shown in table 1.2.1. The device and HP 4142B are connected via a 1.5 m cable. Figure 1.2.9 shows the measurement results. With Vds = 0.5 V or higher, proper measurement is not possible due to oscillation. The oscillation waveform is shown in figure 1.2.10. The oscillation frequency and amplitude are 26 MHz and 8 Vpp respectively.

To prevent oscillation, an RC circuit is inserted between the gate and drain as shown in figure 1.2.11. Figure 1.2.12 shows measurements after inserting the RC circuit. The measurement can be made properly after this has been done.

Table 1.2.1

Parameter	Value	Unit	Conditions
Idss	10	A	$V_{GS} = 0$
Vth	−2.3	V	Id = 100μA, Vds=0.1V
gm	3	S	Id = 0.6A, Vds = 4V
Cgs	138	PF	$V_{GS} = 0$, Is = 0
Cgd	25	PF	$V_{GD} = -4V$, Id = 0

Figure 1.2.8 Methods to Prevent Oscillation

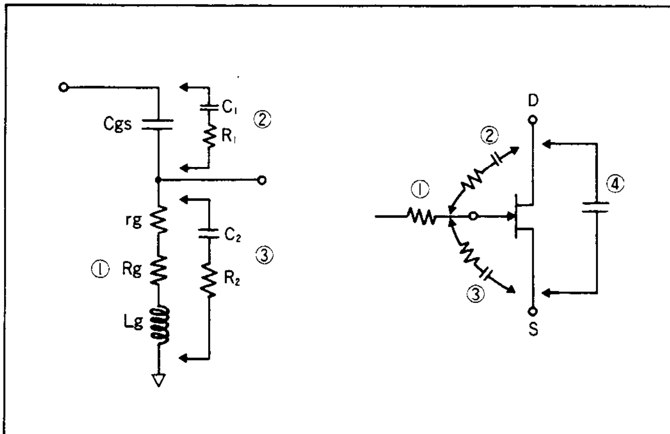


Figure 1.2.11 Practice Example of Oscillation Prevention

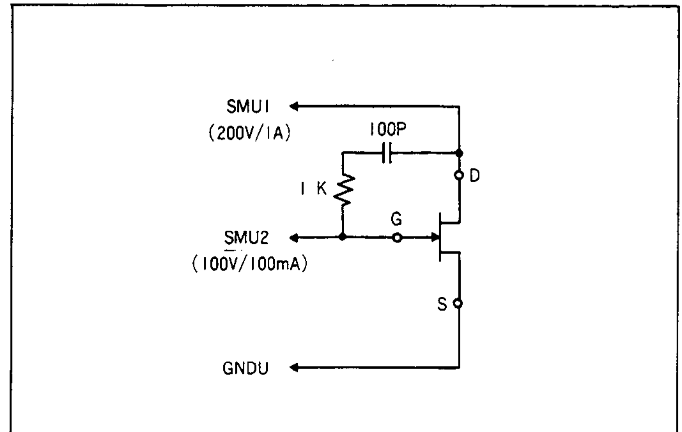


Figure 1.2.9 Measurement Result

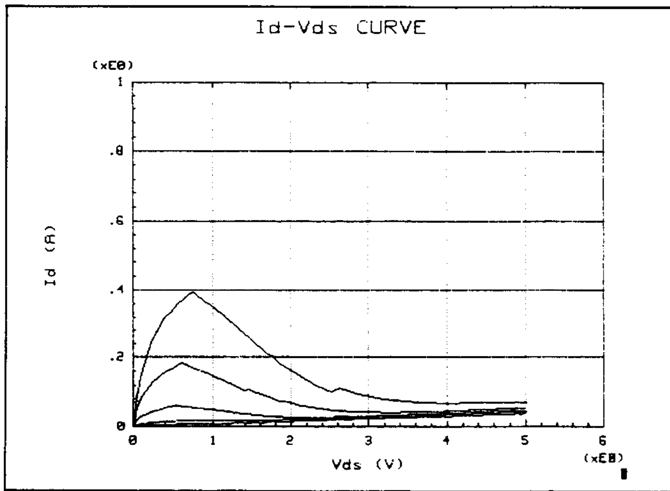


Figure 1.2.12 Measurement Result after Inserting the RC Curcuit

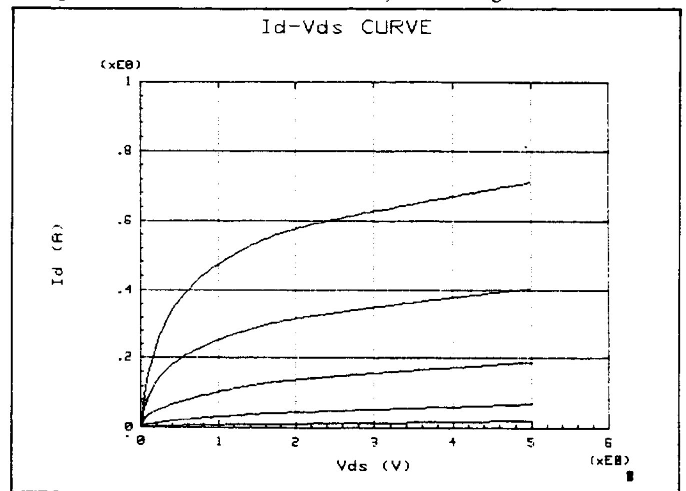
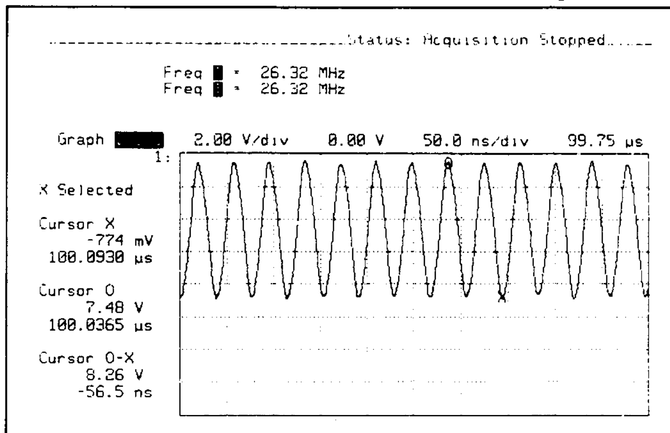


Figure 1.2.10 Oscillation Waveform (Drain Voltage)



2. APPLICATION EXAMPLES

2.1 Bias Source in S Parameter Measurements

S parameter measurement using network analyzers is a very commonly used method for evaluating high-frequency semiconductor devices, such as GaAs MESFETs and microwave range bipolar transistors (BJT). Use of the HP 4142B as the external bias source improves device characterization by using the advanced output control capability of the Analog Feedback Unit (AFU).

This section shows the advantage of the HP 4142B by reviewing BJT measurements as an example.

Present biasing difficulties are as follows:

(1) Biasing Point Drift

The usual S parameter test set uses two independent DC bias sources to supply bias to the base and collector. By this method (figure 2.1.2), the biasing points tend to drift due to internal heating caused by current flows as shown in figure 2.1.3(a) . This is because Ie-Vbe characteristics and HFE are temperature dependent (figure 2.1.3(b)).

(2) Unexpected Damage to Test Devices

Such high-frequency devices can easily be damaged by spikes during biasing.

Using the HP 4142B AFU with two SMUs solves these problems. Figure 2.1.1 shows the HP 4142B test setup. SMU1 supplies Vce, and SMU2 supplies Vbe and Ib. SMU1 monitors the current, and the AFU operates SMU2 in response to the monitored current. Figure 2.1.4 shows a simplified feed back loop to stabilize Ico. This method has the following advantages:

(1) A stable biasing point that eliminates drift because the AFU regulates IC to a steady specified value.

(2) A slew rate that is programmable from 0.5 V/s to 50kV/s without spikes, thus preventing device damage.

Using the HP 4142B as shown in figure 2.1.1 enables reliable measurements up to ±500mA (limited by HP 85046A).

Figure 2.1.5 shows an example of measuring the S parameter by the method of biasing using the AFU and the circuit in figure 2.1.1, then calculating fT from the measured S parameter.

Figure 2.1.1 S Parameter Measurement Circuit

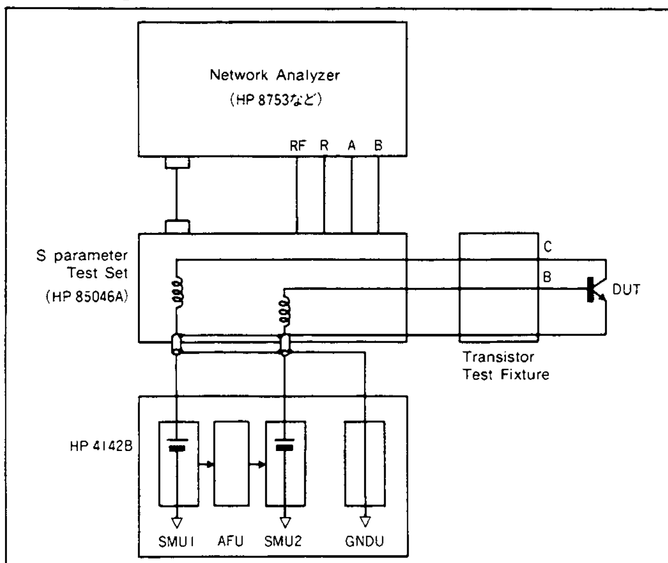


Figure 2.1.2 Biasing Using Two Independent Sources

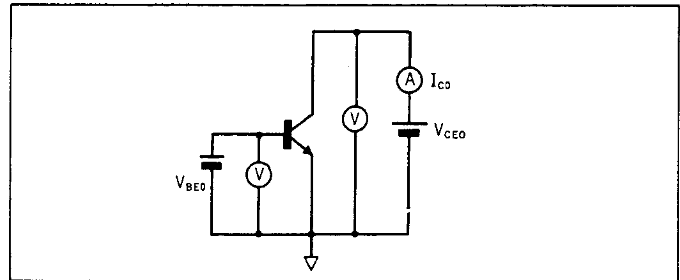


Figure 2.1.3 Drift after Biasing

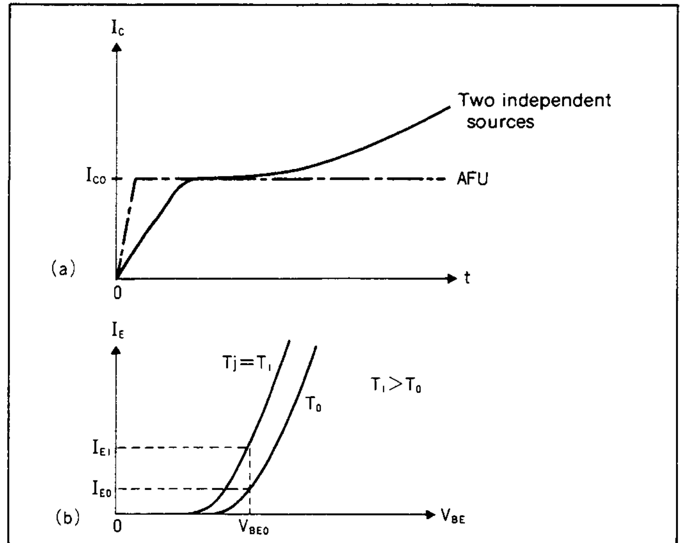


Figure 2.1.4 Bias using AFU

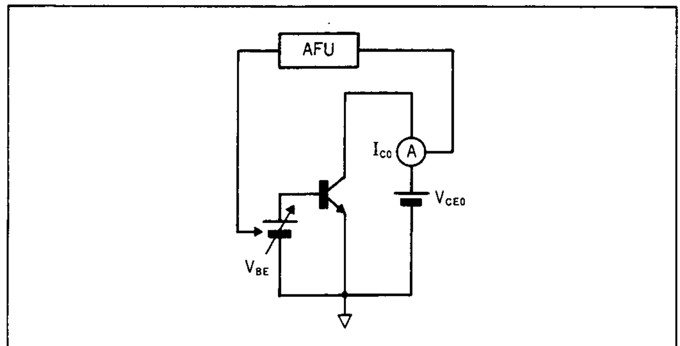
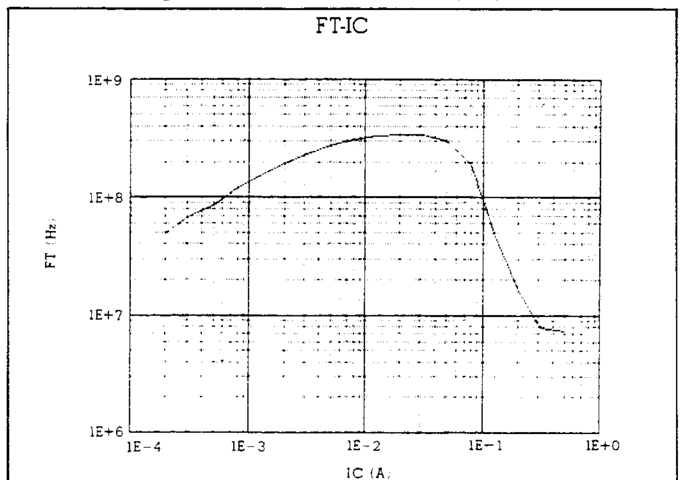


Figure 2.1.5 Measurement Example (f_T)



2.2 HP 4142B and External Power Supplies

The combination of the HP 4142B and an external power supply can easily evaluate the characteristics to 1 A or higher. This section describes the method of evaluating characteristics of power devices by effectively combining an external power supply and the Analog Feedback Unit (AFU).

Figure 2.2.1 shows an example of a measurement circuit to measure the gm and ON resistance of a power MOSFET by the combination of an external power supply with a maximum current of 10 A (HP 6621A) and an HP 4142B. For this measurement, use an external power supply of the series regulator type featuring quick response. Measure a current by measuring the voltage drop across external resistance Rs.

To set bias points Vds, Id for measuring gm, first use the AFU to establish the gate bias Vgs that gives bias point Id, then apply voltage pulses of this Vgs to the gate (pulse width 1 ms). (Pulse mode measurement, see figure 2.2.2.)

As for ON resistance, use the external power supply in the current mode, measure Vds by the voltage monitor (VM) of the HP 4142B, then calculate ON resistance as

$$R_{ON} = \frac{Vdso}{Ido}$$

Figure 2.2.1 Measurement Circuit with External Power Supply

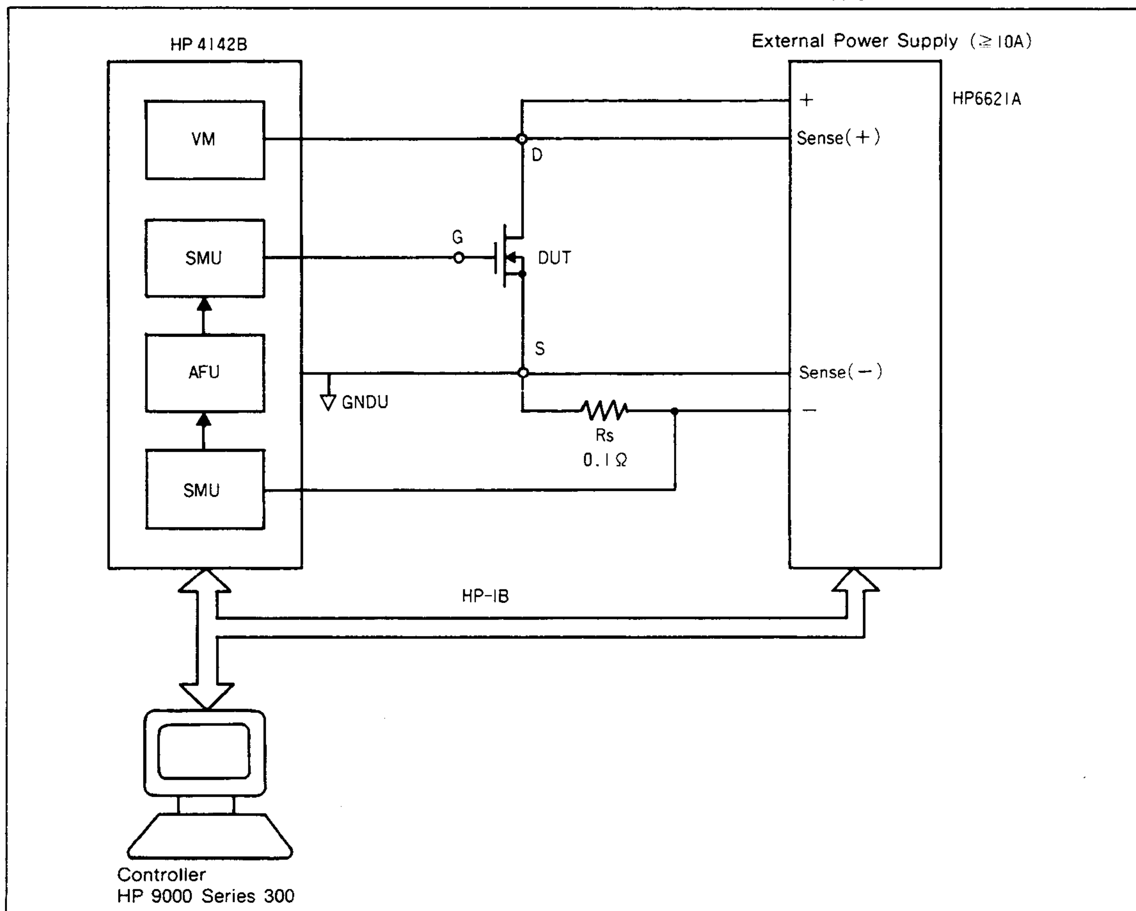
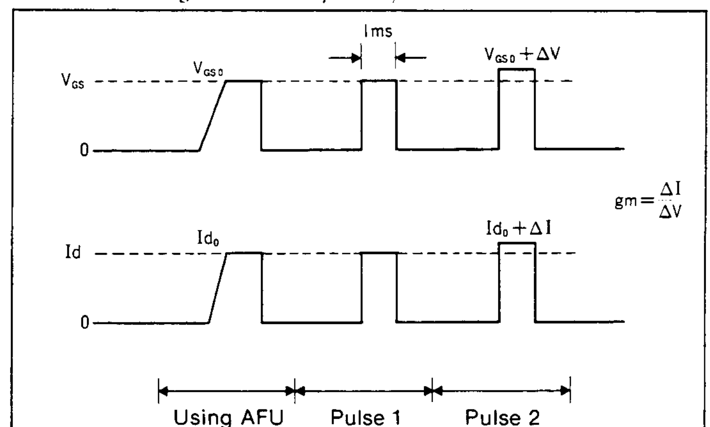


Figure 2.2.2 Sequence of Gm Measurement



2.3 Evaluation of Solar Cell Characteristics

Recently inexpensive solar cells with high conversion efficiency made of amorphous silicon and other materials have been developed and used in many fields.

The power SMU of the HP 4142B (200 V/1 A) enables easy and quick evaluation of V-I characteristics of solar cells with a maximum current up to 1 A.

Figure 2.3.1 shows a measurement circuit for solar cells. The circuit can be made up of just the 200 V/1A range SMU and GNDU. Expose a solar cell to light, increase the output voltage of the SMU from 0 V, and measure the current Io flowing from the solar cell to SMU (figure 2.3.2). The measurements yield the maximum power (Pmax) and optimum voltage/current (Voc) when the terminals are open, and short-circuit current (Ioc).

Figure 2.3.1 Solar Cell Measurement Circuit

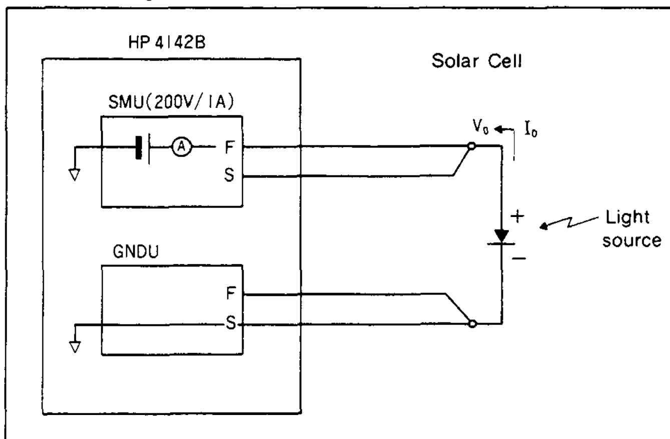
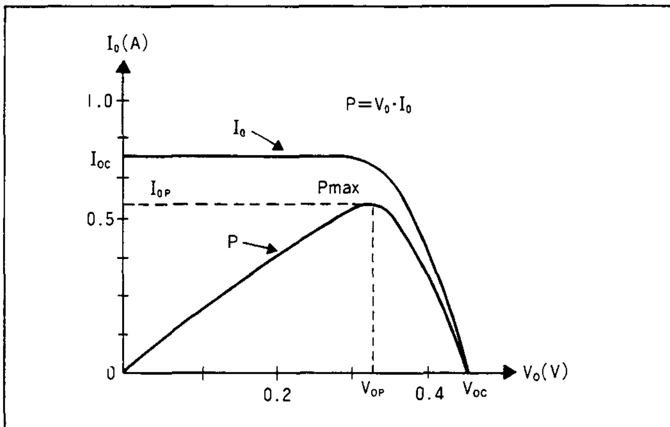


Figure 2.3.2 Measurement Result Example



2.4 Evaluation of CMRR, PSRR, and Open Loop Gain of an Opamp

This section describes how to measure important parameters of an operational amplifier (opamp), CMRR, PSRR and open loop gain, using various sweep functions and highly accurate measurement.

Figure 2.4.1 shows the opamp measurement circuit. The measurement circuit uses the NULL AMP method. The measurement circuit uses two SMUs to supply power to the opamp to be measured, one SMU to set its output voltage, and VS/VMU to measure the output voltage of the null amp.

• CMRR Measurement

Operate the SMU used to supply power to the DUT to vary the common-mode voltage from -12 V to 12 V to DUT in the synchronous sweep mode as figure 2.4.2. Measure the null-amp output voltage Vo to obtain the change in input offset voltage caused by the common-mode voltage (figure 2.4.3).

The CMRR is obtained as

$$CMRR = \left(\frac{\Delta Vo}{\Delta Vco} \frac{1}{1000}\right)^{-1}$$

where

ΔVo: change in null-amp output

ΔVco: change in common-mode voltage

Figure 2.4.4 shows an example of measurements of a TLO71. *Note: See the sample program list on page 17.*

• PSRR Measurement

PSRR is defined as the ratio of the change in input offset voltage to the change in power supply voltage producing it. Vary the power supply voltage (±Vcc) from ±5 V to ±15 V in the synchronous staircase sweep mode (figure 2.4.5). Using the changes in input offset voltage thus obtained, PSRR is calculated as

$$PSRR = \left(\frac{\Delta Vo}{\Delta Vcc} \frac{1}{1000}\right)^{-1}$$

where ΔVcc: change in power supply voltage

Figure 2.4.6 shows an example of measurements of a TLO71.

• Open Loop Gain Measurement

Vary the SMU3 output voltage to the DUT and obtain the open loop gain from the resultant change in input voltage. In other words, perform a staircase sweep of the SMU3 output from -10 V to 10 V, and measure the input voltage. Then, the open loop gain is calculated as

$$Ad = \left(\frac{\Delta Vo}{\Delta V_I} \frac{1}{1000}\right)^{-1}$$

where ΔV_I: change in DUT output voltage, equal to SMU3 change.

Figure 2.4.7 shows an example of measurements of a TLO71.

Figure 2.4.1 OP Amp Measurement Circuit (NULL AMP Method)

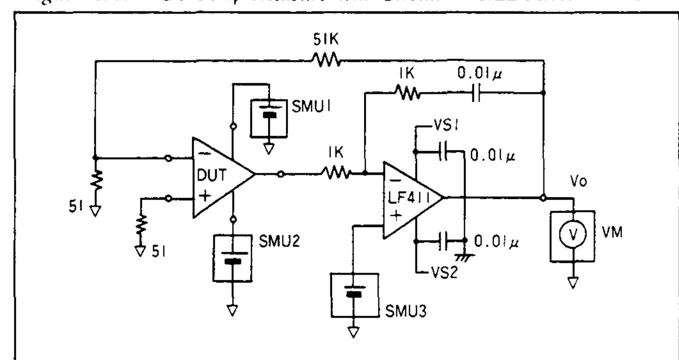


Figure 2.4.2 Force Mode on CMRR Measurement

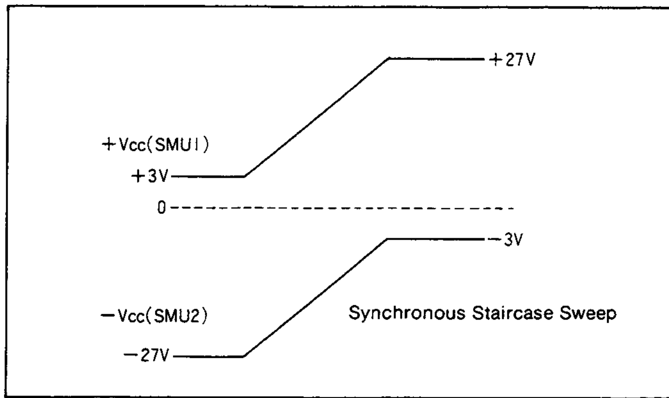


Figure 2.4.5 Force Mode on PSRR Measurement

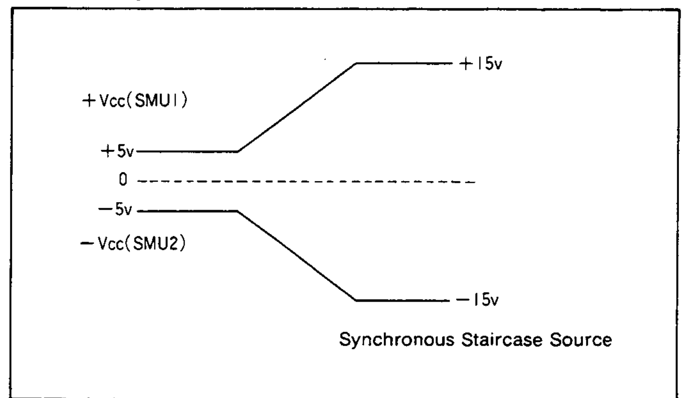


Figure 2.4.3 Measurement Results (CMRR)

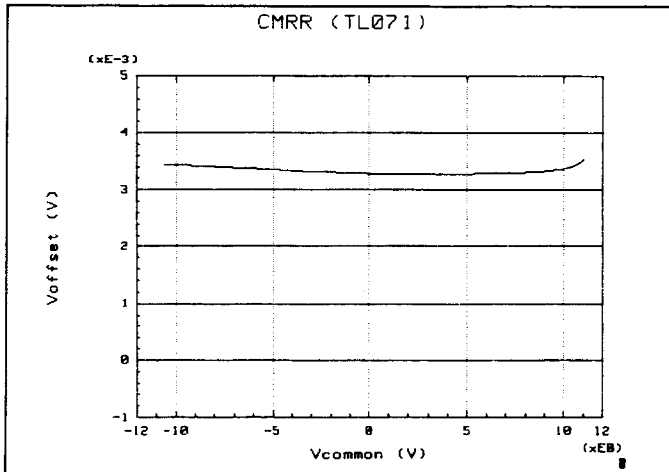


Figure 2.4.6 Measurement Results (PSRR)

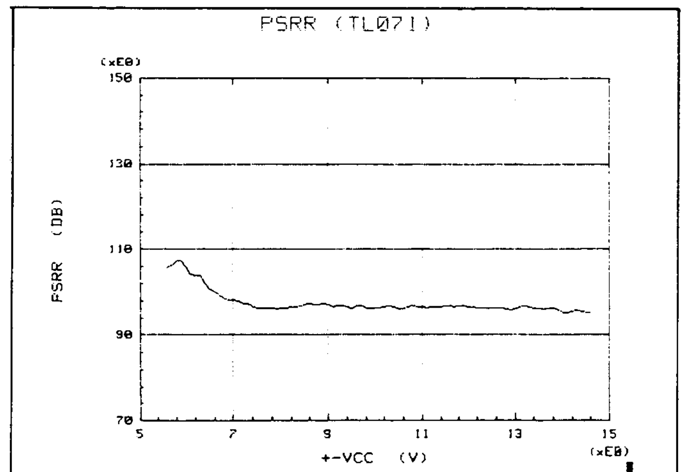


Figure 2.4.4 Measurement Results (CMRR)

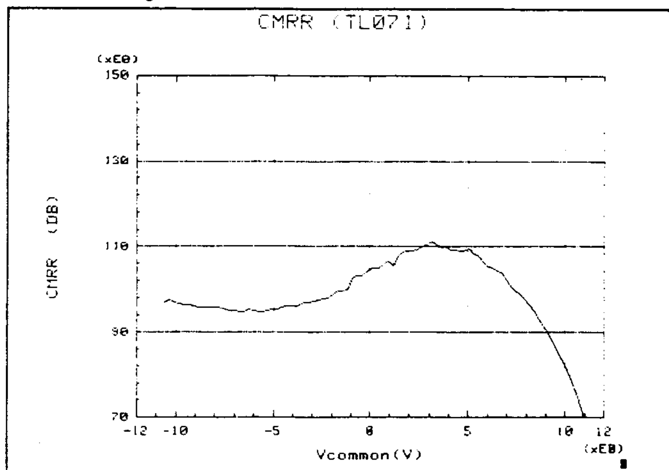
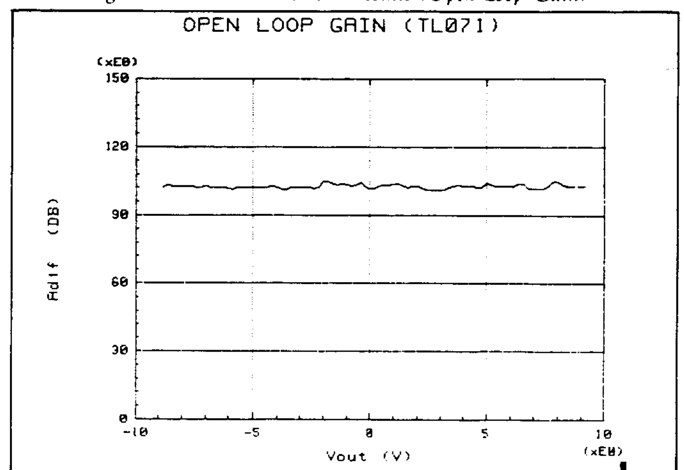


Figure 2.4.7 Measurement Results (Open Loop Gain)



2.5 Transient Thermal Resistance Measurements

The thermal characterization of power semiconductor devices is important for predicting the reliability and performance of these devices, and ensuring their safe operation. This section gives information about the transient thermal resistance of bipolar power transistors and the method for measuring thermal resistance.

Usually, thermal resistance is defined as the ratio of the applied power dissipation to the temperature rise at the reference point. The temperature rise is caused by thermal conduction from a heat source (PN junction). Therefore, a certain amount of time which is proportional to the thermal time constant, is required for the device to reach steady state. The ratio of the temperature rise to the applied power in the transient state is defined as transient thermal resistance (figure 2.5.1). Figure 2.5.2 shows the structure of a package device. Component parts are made of different materials with various masses and thus have different thermal resistances and thermal time constants. Figure 2.5.3 shows an electric circuit model of the device.

The concept of thermal resistance is based upon an analogy between the electrical and thermal properties of materials, with temperature, power dissipation, and thermal resistance being analogous to voltage, current, and electrical resistance respectively. One of the aims of transient thermal resistance measurement is to ensure satisfactory contact between the silicon substrate and case. If the attachment is nonuniform and there are voids, the thermal resistance between the substrate and case will be higher. This can be detected by measuring the transient thermal resistance between the junction and the case.

Figure 2.5.4 shows the measurement circuit. This example uses two power SMUs (200 V/1 A) and one GNDU. Power to be applied to a device is set by the product of V_{CB} and I_E. Set V_{CB} with SMU1, and apply I_E in the form of pulses with SMU2. For example, with V_{CB} = 20 V and I_E = 0.7 A, peak power is approx. 14 W.

To obtain the junction temperature (Tj), use the temperature coefficient of V_{BE} (approx. -2 mV/°C). To estimate Tj, accurately, measure the temperature coefficient at a certain bias current (I_{E1}) in advance.

In this example, V_{BE1} is sampled N times by high speed spot measurement (figure 2.5.5) ("TV" commands are written to program memory of the HP 4142B N times, and then triggered.). Bias (I_{E1}) must be set such that power applied to a device small. For example, set the bias to 1 mA.

Plot the V_{BE} values thus obtained using $\sqrt{t}$ along the horizontal axis (figure 2.5.6). In the range of small t, the plot forms a straight line. Obtain V_{BE} at t 0 by drawing an asymptotic line. Subtract V_{BE} before applying pulses from the value of V_{BE} thus obtained, then divide by the temperature coefficient of V_{BE} to obtain the junction temperature rise.

$$\Delta T = \frac{\Delta V_{BE}}{K}$$

where K: temperature coefficient of V_{BE}

From the temperature rise of this junction and applied power dissipation (14 W), transient thermal resistance Rth (t) for the pulse width used in this measurement is obtained as

$$Rth\ (t) = \frac{\Delta T}{P}$$

Figures 2.5.6 and 2.5.7 show actual measurements of a power transistor with I_{cmax} = 10 A and P_{cmax} = 150 W.

Note: See the sample program list on page 18.

Figure 2.5.1 Temperature Rise after Forcing Power

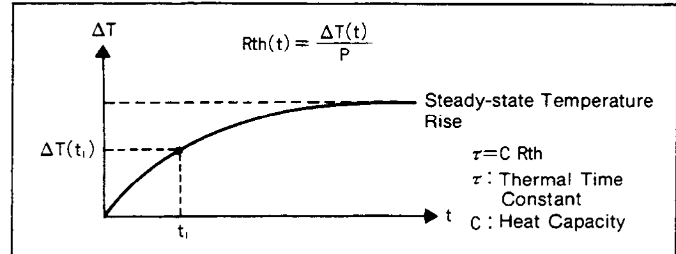


Figure 2.5.2 Packaged Device Structure and Thermal Time Constant

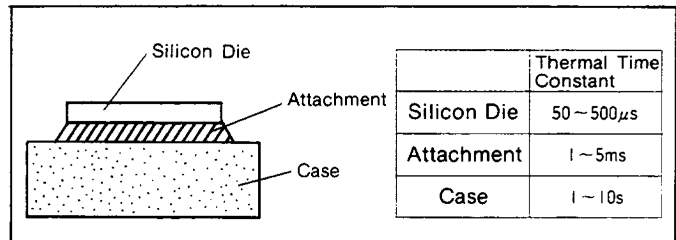


Figure 2.5.3 Circuit Model

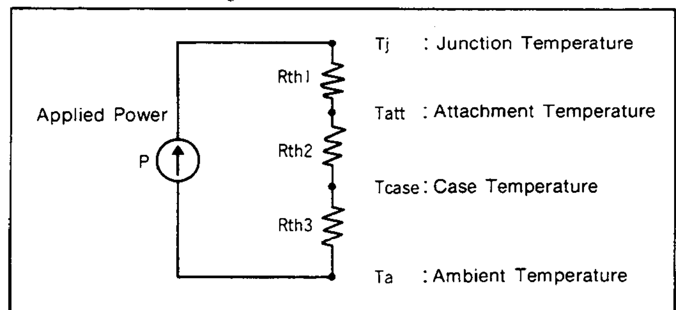


Figure 2.5.4 Transient Thermal Resistance Measurement Circuit

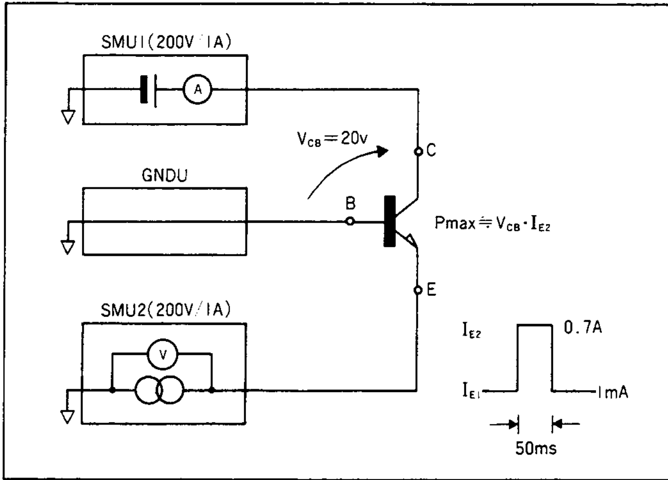


Figure 2.5.5 V_{BE} Measuring Timing

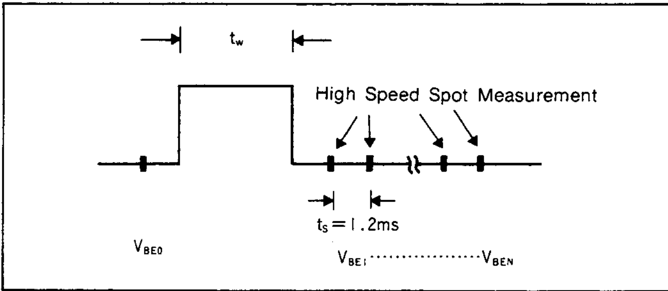


Figure 2.5.6 Change of V_{BE} after Forcing Power Pulse (P_{cmax}=14W, t_w=50ms)

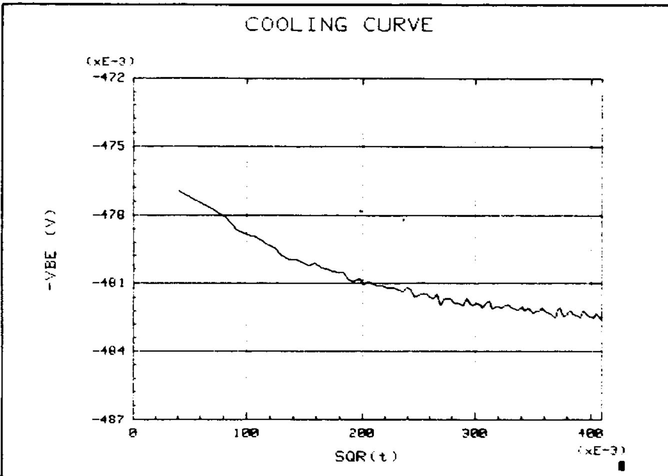


Figure 2.5.7 Measurement Results

```
TRANSIENT THERMAL RESISTANCE  Rth(C/W)

FORCING POWER PULSE : 15W , 50ms
DELTA Vbe           : 6.85498743711   (mV)
DELTA Tj            : 3.42749371855   (C)
 Rth                : .236627058128   (C/W)
```

2.6 Dielectric Absorption Measurements

When using a capacitor in circuits requiring high accuracy, such as S/H circuits and integrator circuits, dielectric absorption must be taken into consideration. This section describes how to measure dielectric absorption.

Figure 2.6.1 (a) shows the principle measurement diagram. Capacitor Cx to be tested is charged for time t at constant voltage, is discharged (short circuit) for the same time t, then is disconnected from the circuit (figure 2.6.1 (b)). After such an operation, the capacitor terminal voltage usually increases. This is because an actual capacitor does not have an ideal capacitance and there exist dielectric absorption elements (C1, R1, C2, R2) as represented in figure 2.6.2.

Figure 2.6.3 shows an actual measurement circuit using an HP 4142B. The measurement circuit setup is very simple because the SMU serves as a voltage source for charging and discharging and as a voltmeter when the capacitor is disconnected (open circuit).

Set the SMU using the following procedure. First, set the SMU to operate as a 10 V voltage source for time t to charge the capacitor.

Next, set the SMU as a 0 V voltage source for the same time t to discharge the capacitor. Then, set the SMU to act as a voltmeter (current compliance 0A) and sample the voltage N times by high speed spot measurement (figure 2.6.4). For quicker measurement, write N "TV" commands to the HP 4142B program memory.

Figure 2.6.5 shows an example of measurements, a test of a 0.01 uF ceramic capacitor and a 0.01 uF polyester film capacitor. It can be seen from this example that the dielectric absorption characteristic of a ceramic capacitor is very poor.

Figure 2.6.1 Dielectric Absorption Measurement

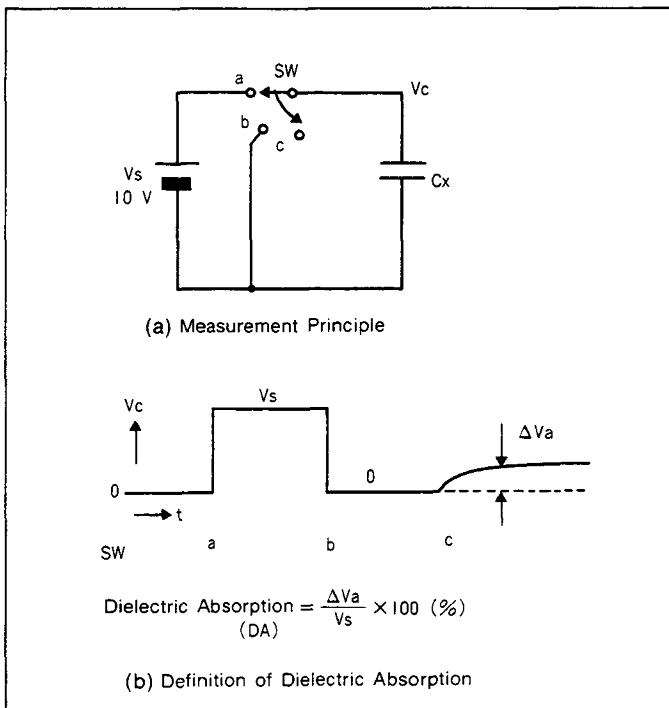


Figure 2.6.2 Capacitor Equivalent Circuit

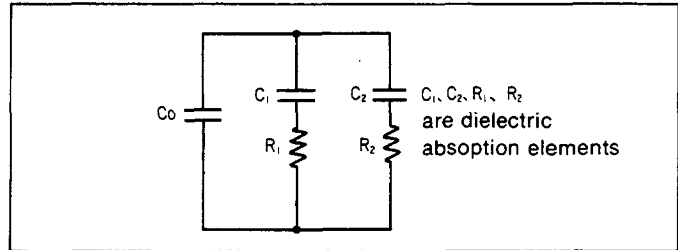


Figure 2.6.3 Measurement Circuit

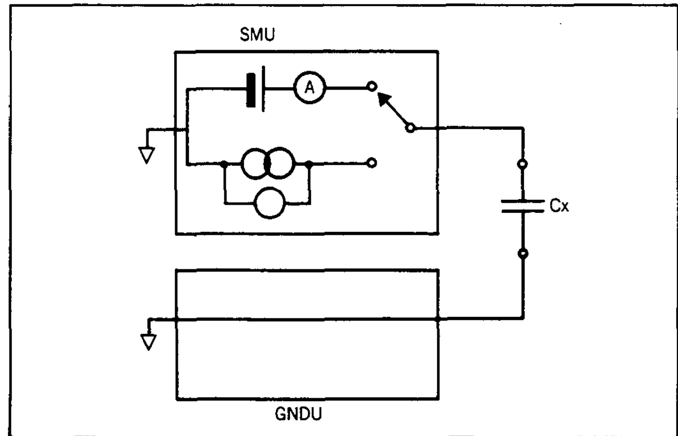
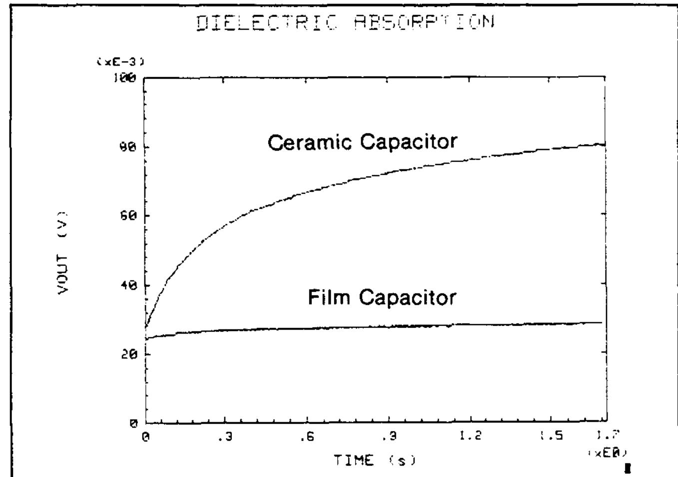


Figure 2.6.4 Programming Example

```
200  OUTPUT @DSM;"DV2,0,10"
210  WAIT 0.1
220  OUTPUT @DSM;"DV2,0,0"
230  WAIT 0.1
240  OUTPUT @DSM;"DI2,0,0,3"
240  OUTPUT @DSM:"DO 1"
```

Figure 2.6.5 Measurement Results



2.7 Simplified Capacitance Measurements using the AFU

The HP 4142B does not have the capability of measuring capacitance using AC signals, but it enables measuring a capacitance ranging from 10 pF to 10 nF or so by the DC method using a precision low current source. This section describes a simplified capacitance measuring method using the AFU as a timer for time measurement.

Figure 2.7.1 (a) shows the principle of measurement. When constant current Io is applied to capacitance Cx, terminal voltage Vc increases linearly at a gradient of Io/Cx (figure 2.7.1(b)). The terminal voltage at time t_1, therefore, can be calculated as

$$Vc(t_1) = \frac{Io}{Cx} t_1$$

One of the two following methods can be used to obtain Cx:

1. With charging current Io and charging time t_1 given, the terminal voltage at t_1 is measured to obtain Cx.
2. With charging current Io and terminal voltage given, t_1 is measured to obtain Cx.

In method 1, there are two ways of setting the charging time: one is to use current pulses and set the pulse width, and the other is to use the system controller's timer. The disadvantage of using current pulses is that the range of current pulses (100 μA min, $\geqq$ 20 V range) has a lower limit. The disadvantage of using the system controller's timer is that there is a difference in time resolution with various models. This section describes an example of capacitance measurement by method 2. This method uses the AFU as a timer for measuring t_1.

Figure 2.7.2 shows an example of an actual measurement circuit. Use SMU1 as a sense SMU, and SMU2 as a search SMU. Keep the output of the SMU2 disconnected. The AFU is used in the ramp mode only. First, set charging current Io, target voltage Vct and ramp speed RS, then trigger the measurement. (Set the hold time, delay time, and feedback integration time to 0, 0, and minimum respectively.)

Figure 2.7.3 shows the change in outputs from SMU1 and SMU2. Charging time t_1 is obtained by measuring Vs as

$$t_1 = \frac{Vs}{RS}$$

Then, capacitance Cx is obtained as

$$Cx = \frac{Io}{Vct} t_1 = \frac{Io}{Vct} \frac{Vs}{RS}$$

Although the hold time is set to 0, preprocessing by the AFU causes a time lag (4 ms to 5 ms) between rise of charging current and start of ramp voltage. To minimize the error caused by this time lag,make the charging time at least 40-50 ms by adjusting Vs and RS.

The measurement range of this method is expressed as

$$C = 10pF \sim 10nF \pm 10\%$$

$$(t \geqq 50ms,\ V_{ct} = 10V,\ Io = 1nA \sim 1\mu A)$$

Note: See the sample program list on page 19.

Figure 2.7.1 C Measurement Principle

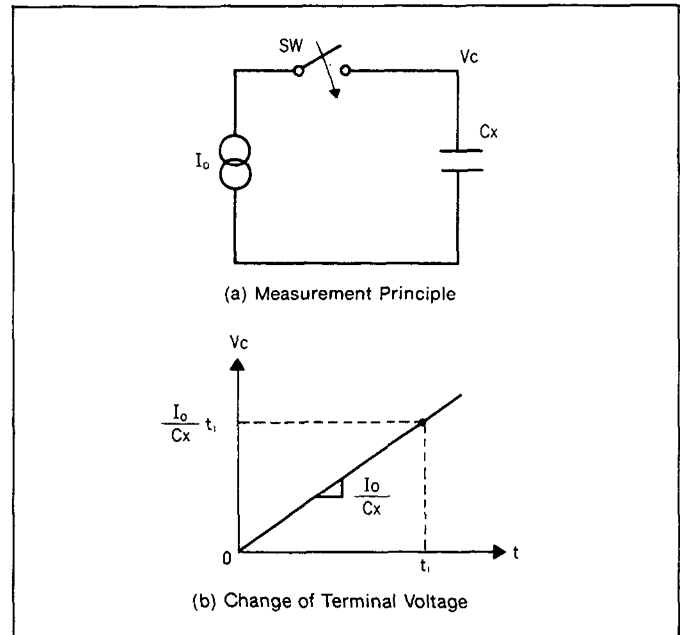


Figure 2.7.2 Measurement Circuit

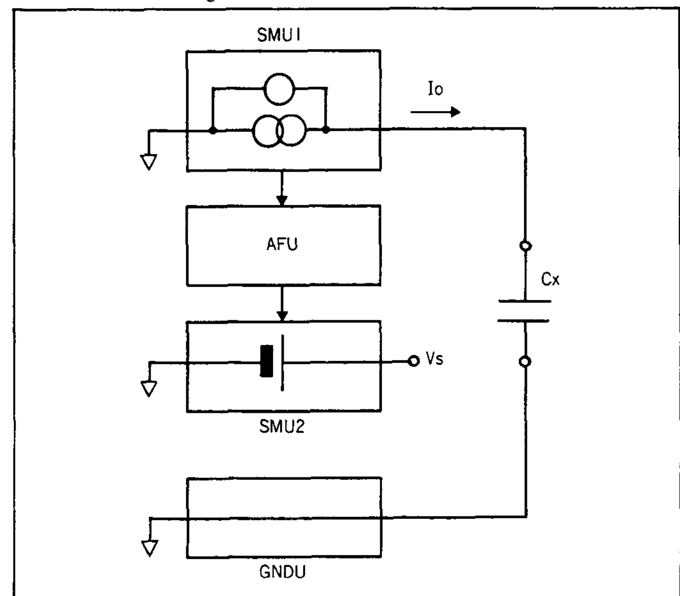
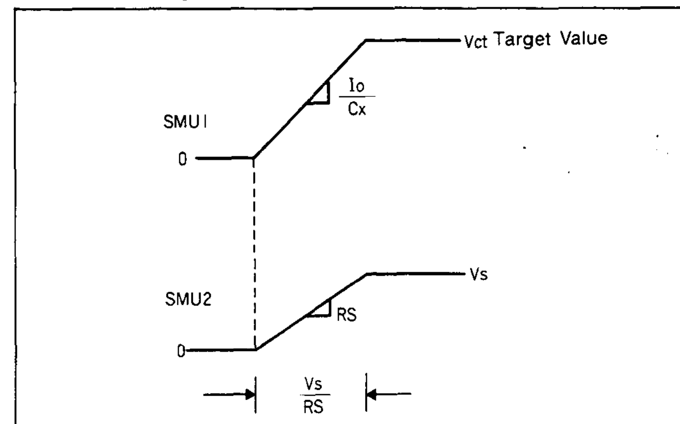


Figure 2.7.3 AFU-Related Waveforms



2.8 Noise Evaluation by FFT Analysis

The precision measurement performance of the HP 4142B (17-bit accuracy) and improved time resolution (1 ms) enable fast Fourier transform (FFT) analysis with a maximum frequency of 400 Hz and dynamic range of 80 dB or more.

This section describes how to evaluate the noise characteristics of an opamp by FFT analysis using high-speed spot measurements.

Figure 2.8.1 shows the measurement circuit. Set the gain of the opamp to 1000x, connect a low-pass filter to the output to prevent Aliasing effect, and connect the VS/VMU.

Write N "TV" commands to the HP 4142B program memory to enable trigger measurements and sampling to be done at maximum speed. The sampling interval ts should be about 1.2 ms (figure 2.8.2). Make the number of sampling points a power of 2 for convenience in FFT operation. (N=512 maximum because of HP 4142B data memory capacity in ASCII Data format)

Weight the obtained data by a proper window function Hanning, etc. and then perform the FFT.

The results obtained are in the form of a complex number, and the power is the sum of squares. Divide it by the maximum frequency resolution (corresponding to the filter width) to obtain the power spectrum density. (This value is independent of the number of sampling points N and interval ts.)

Figure 2.8.3 shows an example of measurements. This graph shows the noise characteristics of a TLO71 FET opamp. The average noise level at 100 Hz and above is about 20—30 nV/Hz.

Note: See the sample program list on pages 20—21.

Figure 2.8.1 Noise Measurement Circuit

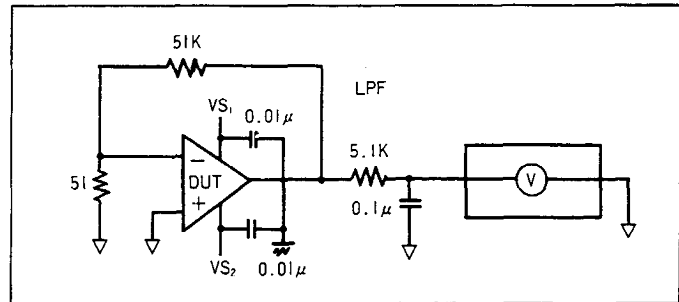


Figure 2.8.2 Sampling Timing

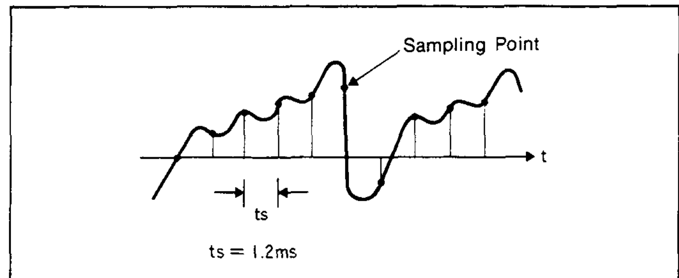
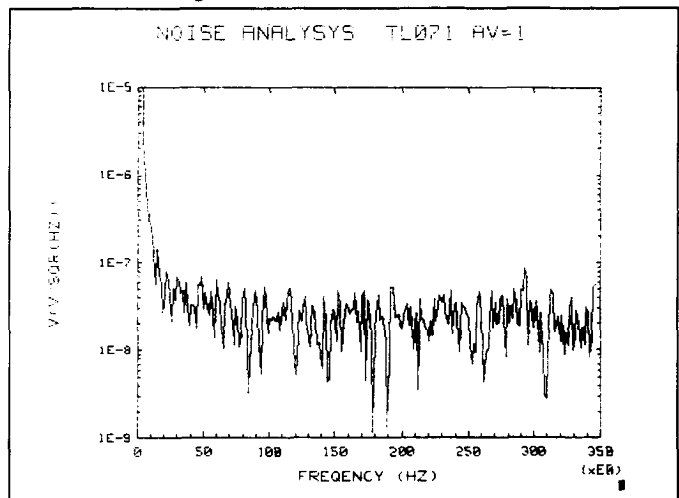


Figure 2.8.3 Measurement Results



References

1. Siliconix Inc: [MOSPOWER Application]
2. S. Takagi et al: [Programmable Stimulus/ Measurement Units Simplify Device Test Setups] HP Journal, October 1982, P15—20
3. S. Rubin et al: [Thermal Resistance Measurement on Power Transistors] NBS 400-14

APPENDIX

PROGRAM Listings

CMRR Measurements

CONNECTION: SMU1 HP41420A Slot 1, 2
SMU2 HP41421B Slot 3
SMU3 HP41421B Slot 4
VS1, 2 HP41424A Slot 6

```
10    !4142B OP AMP EVALUATION EXAMPLE
20    !CMRR
30    OPTION BASE 1
40    DIM D(101),E(101),F(101)
50    GCLEAR
60    !
70    OUTPUT 722;"*RST"
80    !
90    OUTPUT 722;"CN"
100   OUTPUT 722;"FL0"
110   OUTPUT 722;"AV16,1"
120   !
130   OUTPUT 722;"MM2,16"
140   !
150   OUTPUT 722;"DV16,12,15"
160   OUTPUT 722;"DV26,12,-15"
170   !
180   !OUTPUT 722;"VM16,2"
190    !
200   OUTPUT 722;"DV4,11,0"
210   OUTPUT 722;"WV2,1,13,3,27,101,0.05"
220   OUTPUT 722;"WSV3,13,-27,-3,0.05"
230   !OUTPUT 722;"WT0,1E-3"
240   OUTPUT 722;"XE"
250   ENTER 722;D(*)
260   Lingraph(-12,12,70,150,"Vcommon(V)","CMRR  (DB)","CMRR (TL071)",1)
270   G=1000
280   Dv=24/100
290   FOR L=1 TO 101
300     D(L)=D(L)/G
310   NEXT L
320   FOR K=2 TO 100
330     IF D(K+1)-D(K-1)=0 THEN
340       E(K)=E(K-1)
350     ELSE
360       E(K)=20*LGT(ABS(2*Dv/(D(K+1)-D(K-1))))
370     END IF
380   NEXT K
390   FOR I=6 TO 96
400     F(I)=(E(I+4)+E(I+3)+E(I+2)+E(I+1)+E(I)+E(I-1)+E(I-2)+E(I-3)+E(I-4))/9
410   NEXT I
420   MOVE 6*Dv-12,F(6)
430   FOR M=6 TO 96
440     DRAW M*Dv-12,F(M)
450   NEXT M
460   OUTPUT 722;"*RST"
470   !Dump_screen
480   END
```

Transient Thermal Resistance Measurements

CONNECTION: SMU1 HP41420A Slot 1, 2
SMU2 HP41420A Slot 5, 6

```
10     !4142B APPLICATION EXAMPLE
20     !TRANSIENT THERMAL RESISTANCE
30     OPTION BASE 1
40     ASSIGN @Dsm TO 722   ! DC SOURCE/MONITOR
50     COM @Dsm
60     DIM D(101),E(101)
61     N=101
70     !
80     OUTPUT @Dsm;"*RST"
100    OUTPUT @Dsm;"CN"
110    OUTPUT @Dsm;"FL0"
120    OUTPUT @Dsm;"AV1,1"
121    OUTPUT @Dsm;"MM3,2"
131    !SET_UP
132    OUTPUT @Dsm;"SCR"
134    OUTPUT @Dsm;"ST1"
141    OUTPUT @Dsm;"DV2,12,20,0.7"
142    OUTPUT @Dsm;"DI6,20,-1E-3,-1"
151    OUTPUT @Dsm;"PI6,20,-1E-3,-0.7,-1"
161    OUTPUT @Dsm;"PT0,50E-3,0"
162    OUTPUT @Dsm;"XE"
171    FOR L=1 TO N-1
181      OUTPUT @Dsm;"TV6,11"
191    NEXT L
201    OUTPUT @Dsm;"END"
211    !
212    Time1=TIMEDATE
221    OUTPUT @Dsm;"DO1"
222    OUTPUT @Dsm;"*OPC?"
223    ENTER @Dsm;A
224    Time2=TIMEDATE
225    Pw=5.0E-2
227    Dt=(Time2-Time1-Pw)/N
228    FOR K=1 TO N
231      ENTER @Dsm;D(K)
241    NEXT K
242    !CALCULATION
243    Pow=.7*(20+ABS(D(1)))
245    A=2.E-3     !VBE TEMP COEFFICIENT
246    B=D(2)-(D(2)-D(12))/(SQR(Dt)-SQR(Dt*11))*SQR(Dt)
247    Dvbe=ABS(B-D(N))
248    Dtj=Dvbe/A
249    Rth=Dtj/Pow
252    !REPORTING
253    PRINT
254    PRINT "      TRANSIENT THERMAL RESISTANCE  Rth(C/W)"
255    PRINT
256    PRINT "  FORCING POWER PULSE : 15W , 50ms"
257    PRINT "  DELTA Vbe            :";Dvbe*1.E+3;"  (mV)"
258    PRINT "  DELTA Tj             :";Dtj;"  (C)"
259    PRINT "   Rth                 :";Rth;"  (C/W)"
261    !PLOTTING
262    Lingraph(0,SQR(N*Dt),D(101)-5.0E-3,D(2)+5.0E-3,"SQR(t)","-VBE (V)","COOLIN
G CURVE",1)
271    MOVE SQR(Dt),D(2)
281    FOR J=3 TO N
282      DRAW SQR(J*Dt),D(J)
283    NEXT J
288    !Dump_screen
289    !
290    END
```

C Measurements

CONNECTION: SMU1 HP41420A Slot 1, 2
SMU2 HP41421B Slot 3

```
10     !4142B APPLICATION EXAMPLE
20     !C MEASUREMENT
30     OPTION BASE 1
40     ASSIGN @Dsm TO 722    ! DC SOURCE/MONITOR
50     COM @Dsm
60     DIM D(2)
70     !
80     OUTPUT @Dsm;"*RST"
90     !
100    OUTPUT @Dsm;"CN"
110    OUTPUT @Dsm;"FL0"
120    OUTPUT @Dsm;"AV1,1"
130 Set_up:  !
140    Io=1.E-7      ! FORCE CURRENT
150    Vta=10        ! TARGET VOLTAGE
160    Rs=10         ! RAMP SPEED
170    OUTPUT @Dsm;"ASV";3,0,2,Rs
180    OUTPUT @Dsm;"AIV";2,Io,Vta,20
190    OUTPUT @Dsm;"ASM3,3,5E-5"
200    OUTPUT @Dsm;"AT0,0"
210    OUTPUT @Dsm;"MM6"
220    !
230    OUTPUT @Dsm;"XE"
240    ENTER @Dsm;D(*)
250    Cap=(Io/D(2))*(D(1)/Rs)*1.E+12
260    DISP Cap;"pF"
270    END
```

For more information, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic Instruments Department or write to Hewlett-Packard; **U.S.A.**–P.O.Box 10301, Palo Alto, CA 94303-0890. **Europe/Middle East/Africa**–Central Mailing Department, P.O.Box 529, 1180 AM Amstelveen, the Netherlands. **Canada**–6877 Goreway Drive, Mississauga, L4V1M8, Ontario. **Japan**–Yokogawa-Hewlett-Packard Ltd., 3-29-21, Takaido-Higashi, Suginami-ku Tokyo 168. **Elsewhere** in the world, write to Hewlett-Packard Intercontinental, 3495 Deer Creek Road, Palo Alto, CA 94304.

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