Keysight Technologies

Converting Tescon Point 70 Fixtures and Programs for Use on the *Medalist* i1000D In-Circuit Test System

Application Note

KEYSIGHT TECHNOLOGIES

Contents

Introduction to *Medalist* i1000D

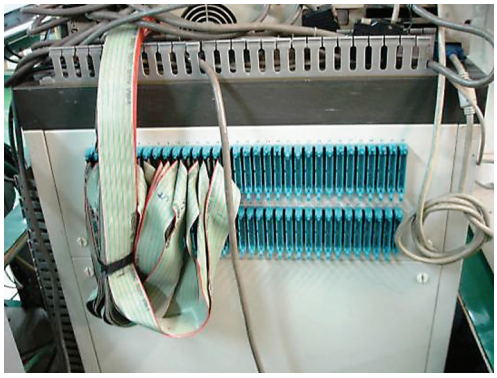
The Keysight Technologies, Inc. *Medalist* i1000D in-circuit test (ICT) system is a revolutionary platform targeted for maximum cost effectiveness. It offers award winning state-of-the-art features with answers to most test challenges faced by today's manufacturers. Advanced defects coverage features coupled with a simplified software model shorten the learning curve of new users, making this an ideal investment for manufacturers who need a cost effective ICT solution. It's back to the basics with the *Medalist* i1000D software to help new users get up to speed in the shortest time possible.

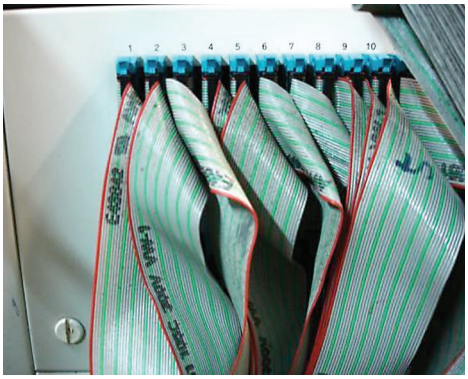
Following the development model of a typical manufacturing defects analyzer (MDA), the user can now get a fixture and program up and running in just a few days. Simplified graphical user interfaces allow the user to quickly make changes to individual tests during debug, with a comprehensive toolset of menus and buttons complete with AutoDebug features. This allows inexperienced users to start using the system quickly.

The purpose of this application note is to guide users on how they can convert both the hardware and software systems of their old Teson MDA platform over to the *Medalist* i1000D platform so as to enjoy the capabilities offered by the i1000D ICT system.

Overview of the Tescon System

The picture above shows the Tescon Point 70 system. It consists of the system tower and a press down unit. The press down unit is slightly smaller in size as compared to the i1000D wide press option. The press down unit sits separately on a table that is provided by the user. All other mechanical aspects of the press down unit are similar to the i1000D system. The system runs on an old MS DOS PC controller which makes integration of today's 3rd party software almost impossible.





From the back of the system tower are the flat cables connectors. These flat cables are to be connected to the test fixtures in the press down unit.

Benefits of Conversion

Tescon Point 70 systems are over a decade old. Operating on MS-DOS environment, the software doesn't offer much flexibility or capability. For instance, the system doesn't support 3rd party software integration and Microsoft Windows window-based interface, which are much more user friendly.

Today's production environments require efficient data tracking. Each board is labeled with a serial number which is then scanned and logged into the data logging system of each tester for tracking and analysis purpose. Therefore, it is critical that the test machines on the production line are able to support data logging. Data log files are frequently analyzed using tools like Microsoft Excel and other statistical applications. Therefore, having a simple data log file format like CSV will allow the user to import the log files easily. By migrating to a new platform like the *Medalist* i1000D, it simply eases the implementation of new hardware which probably uses an interface which is not supported in MS DOS. It will also allow a wide range of Windows-based applications to be used for analytical purposes.

The *Medalist* i1000D software is a Windows-based design which provides much more flexibility and usability. The user can simply click on the tasks required, and have a much wider vision of the test parameters available for use. Moreover, the test files are CSV formatted, making it easy to import into popular applications like Microsoft Excel editing or analysis.

Over the years, technology had evolved and new controllers and chipsets are now able to make faster measurement and response integrations. This basically results in much lower test time on the *Medalist* i1000D. Also, new test techniques, like Keysight VTEP, bring the meaning of ICT testing to a whole new level. Test coverage is increased dramatically with these new techniques. The Tescon Point 70 system does not have much room for expansion, both in terms of software and hardware.

A modern test system needs to have flexibility for user to deploy it under different environment and requirement. It needs to have compatibility to expand the system capabilities with external 3rd party hardware. It needs to be fast, accurate and efficient.

Staying on an old platform simply does not make sense unless the user does not plan to make any improvements to their existing production operations. Summarizing the benefits to move from Tescon Point70 to the *Medalist* i1000D:

- Faster test time with latest measurement technologies
- Better compatibility of hardware and software by running on today's operating systems.
- Greater user friendliness achieved with Windows-based software design
- Higher test coverage with Keysight VTEP and other advanced test capabilities of the *Medalist* i1000D

Conversion Process

Hardware conversion

The hardware conversion simply involves bringing an existing Tescon fixture onto the *Medalist* i1000D system. The mechanical aspect of the Tescon fixture is very similar to the i1000D fixture, therefore, only slight modifications need to be done to complete the conversion.

The Tescon fixture is an MDA type press-down fixture. Each probe is wired to a 34-pin connector at the back of the fixture where the 32-pin flat cables from the tester connect. Both the fixture and cable use a 34-pin connector instead of 32 pins because of standardization in the market. It is easier to get replacement connectors with 34 pins rather than 32 pins. The flat cable remains at 32 pins though. Therefore, the last 2 pins of each connector (fixture and cable) are not used.

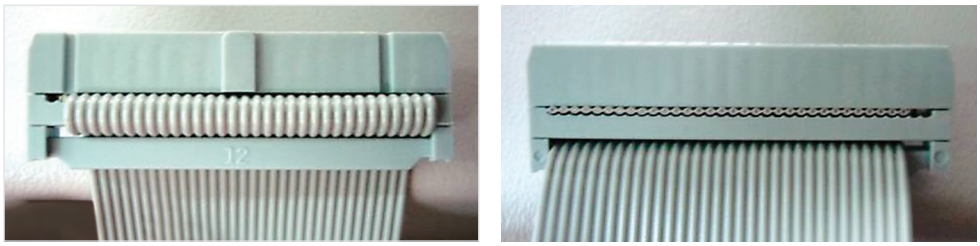


Figure 1. 34-pin female connector on flat cables

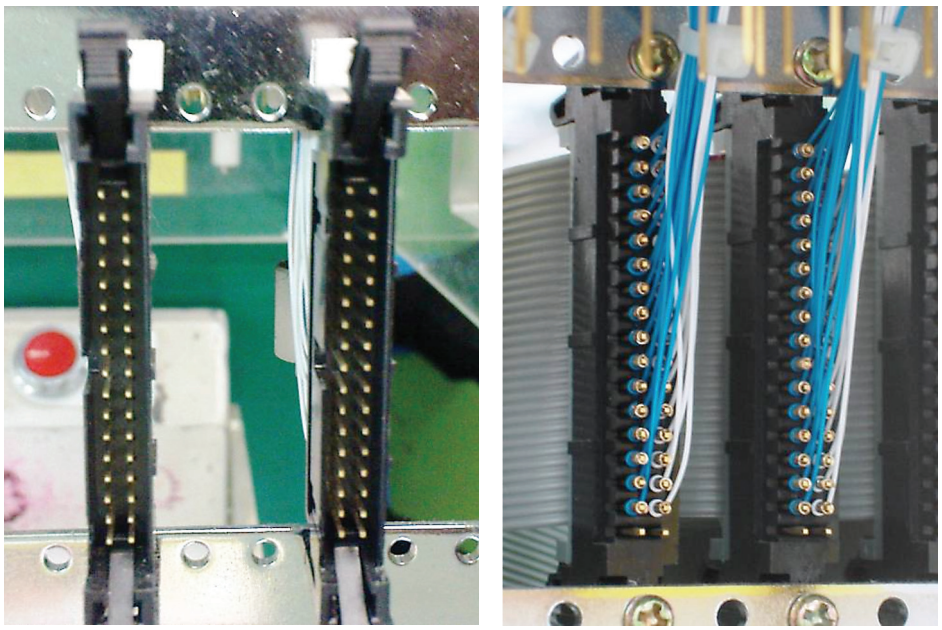


Figure 2. 34-pin male connector on flat cables

The test resource pin out on the connectors of the Tescon fixture is almost the same as that of the i1000D fixtures. The first test resource (nail #1) starts from the first pin of the first connector and the rest follow on. Tescon fixtures use 34 pin connectors with the last 2 pins unused. This means that the first connector on the fixture will contain the test resource nail #1 to nail #32. The second connector will start from nail #33 and end with nail #64.

The *Medalist* i1000D system uses a 64-pin flat cable as a standard. Therefore, in order to interface the Tescon fixture onto the i1000D, the 64-pin flat cable needs to be replaced with a new flat cable that has a 64-pin connector at one end and 2 x 34 pins connector at the other end. This basically splits the 64-pin resources from a single connector into two separate connectors to fit the Tescon fixture. Similarly, at the 34-pin connector end of the flat cable, the last two pins of the connectors are left disconnected as in figure 1 above.

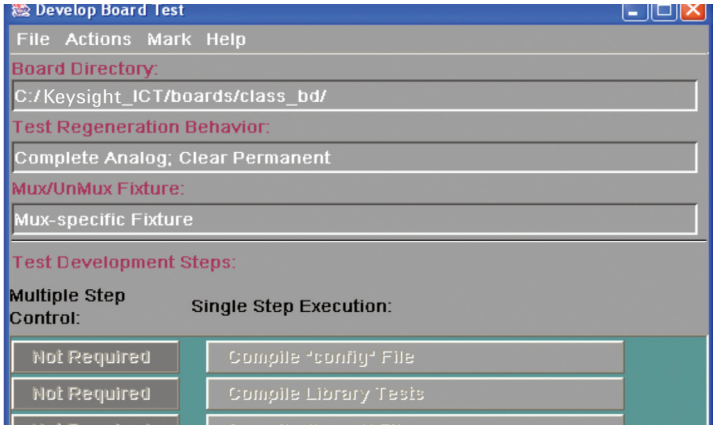


Figure 3. Connector pin out of Tescon fixture

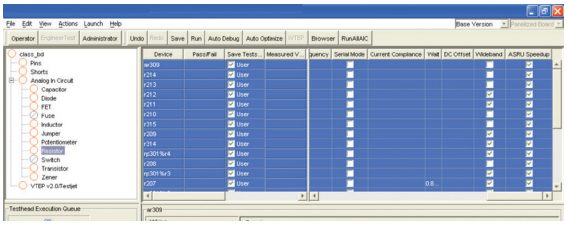


Figure 4. Connector pin out of i1000D fixture

Figure 5. 64-pins to 32-pins split flat cable

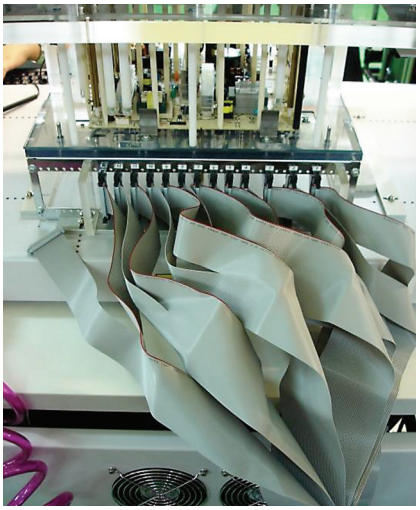


Figure 6. Tescon fixture connected to i1000D

There are two sizes of the press-down unit available for the *Medalist* i1000D. The larger- sized option allows user to build larger fixture for bigger boards, whereas the smaller- sized version cater for smaller fixtures, with the benefit offered by a lower-priced system. Depending on the size of the Tescon fixture, the large size press-down unit may not be able to fully secure the fixture if it gets too small. The alternative is to use the small size press-down unit. However, if the small press-down unit is unavailable, then some improvising will need to take place in order to secure the smaller fixture properly.

The normal i1000D fixture is secured by means of four aluminum bars located on the base of the press-down unit. Place the fixture at the middle and push each bar towards the fixture and secure the two screws on the bar to fix the position. Once fixed, the fixture will not be allowed to move on the horizontal axis. The user can simply pick up the fixture and place another similar-size fixture onto the press-down unit without needing to readjust the bars.

However, if the fixture size is too small, the bars may not reach far enough to secure the fixture. In this case, the user will need to improvise by adding some form of extension. Figure 7 shows that the aluminum bar with a spacer added to extend its reach to the small sized fixture. Figure 8 shows the fixture properly secured by the bars. Instead of adding the spacer, the user can purchase some L-brackets which are commonly used for shelving from their local hardware store. See figure 9.

Figure 7. Spacer bar added between bar and fixture.

Figure 8. Fixture is properly secured.

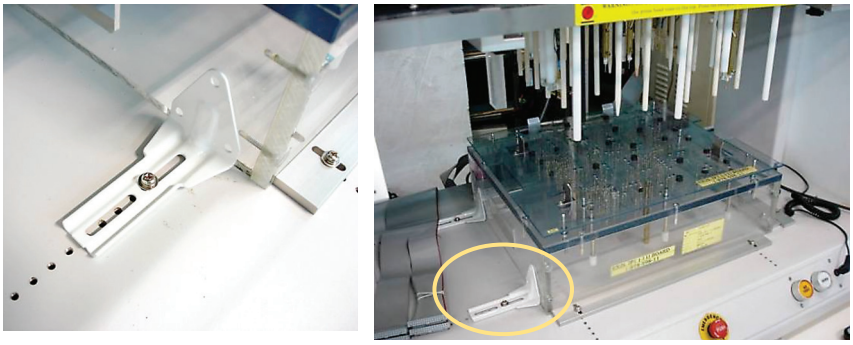


Figure 9. Improvising with off-the-shelf brackets

As with any new fixture setup, the user needs to adjust the press-down travel to cater for the height of the test fixture. The objective of this adjustment is to ensure that the press cylinder travels far enough to achieve 2/3 compression on the test probe. Depending on the fixture design, some fixture is added with stopper on the probe plate to prevent over-compression of the test probes, others may just leave it to the user to decide.

Adjusting the press travel is simple. Bring the press down to a level where 2/3 probe compression is achieved. Then remove the back cover of the press-down unit and adjust the lower sensor to a position where it is lit. Because the press works on compressed air, the adjustment may need to be fine-tuned two or three times to achieve the optimum setting.

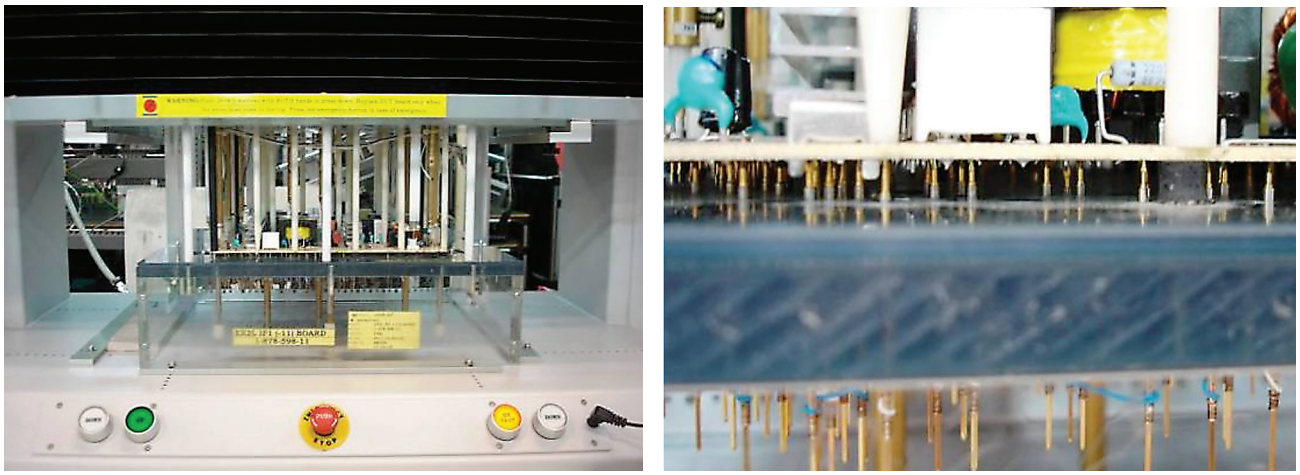


Figure 10. Fixture engaged with 2/3 probe compression.

Figure 11. Adjust the lower sensor to lit position

Software conversion

At the time of release of this document, there is no software available from Keysight to support the conversion of the Tescon Point 70 test files over to the *Medalist* i1000D program. Tescon Point 70 operates in a simple executable file and the test data files are formatted such that it is only readable using the Tescon software interface. On the other hand, the i1000D test data files are written in the common text file format which all text editor software can read and edit. This makes it easy for the user to manage the test files.

So what is the information that we need from the Tescon files in order for us to build the i1000D test program?

Regardless of test systems models and brand, all the test programs will need to have some basic information about the board device under test (DUT) and also the fixture wiring. The basic information will include the items below:

- Reference designators of components
- Expected test value of the components
- Expected tolerance of the components
- Test resource assignment for each components (Pins File*)

With this information, the user can start building the i1000D test program to a stage where it can be used for production testing purpose. But because there is no other information like the components x-y coordinates, etc, the resulting test program will have limited capability with graphics.

Among the information listed above, the Reference Designators, Test Value and Tolerances can be obtained from the customer's Bill-of-Materials (BOM). This will allow us to build a test program with all the components information includes, but without any test resource assignment.

In most cases, fixture vendors would have manually numbered the nodes on the schematics and created the Tescon test program based on their assignment. There is no CAD translation process where CAD translation tools are used to assign test points. In the absence of a CAD translated fixture, there are no standard Pins and Nails files that we can use to perform an automated test program generation for the i1000D. The test resource assignment will need to be manually entered into the test program using either the schematics or from an output file of the Tescon system which will be discussed later in this document.

→ *See appendix for Pins and Nails file sample*

Let's first discuss the process of generating an ATD file using the BOM and dummy pins and nails files. To generate the ATD file, first we will need to have the customer's BOM formatted in accordance to the i1000D BOM requirement. Details of the BOM format can be found in the online help manual of the i1000D. Table 1 below shows a general format of the BOM required. A sample of a formatted BOM can be found in the Appendix of this document.

Table 1. Medalist *i1000D BOM format*

Item	Description
File type	Text file
Filename	No restrictions

Data format	**Header:**
	`Name Type Value +Tol(%) -Tol(%) Part No Comment`
	`----------`
	The header is optional. Note that semi-colons must not be used in the header.
	Data:
	`Name; Type; Value; +Tol(%); -Tol(%); Part No; Comment;`

With the BOM correctly formatted, the user can simply generate the ATD file using the BOMtoATD application that comes with the *Medalist* i1000D software. The BOMtoATD requires three files as input before it can generate the ATD file.

These three files are: BOM, PIN and NAIL. BOM is formatted by the user but PIN and NAIL are missing. What the user needs to do is to obtain a dummy copy of the PIN and NAIL file. These dummy files can be from any existing fixture or projects. They do not need to be actual translations of the CAD file for that board. What we need is just a file with the correct formatting so that the BOMtoATD assumes that it is reading the correct files.

The BOMtoATD will attempt to match the components listed in the BOM with the test resource numbers (nail numbers) stated in the PINs file in order to create the ATD file. If a match is found, the BOMtoATD will write the nail numbers of the component into the ATD. In any case, user will be overwriting these nail numbers anyway at the later part, so what the BOMtoATD writes onto the Nail numbers column is irrelevant.

Refer to the Online Help manual of the i1000D for detailed instructions on the use of this application.

Now that the ATD file is already generated using the BOM and dummy files, the user can now start to enter the nail information into the ATD file. To do this, user can either check the nail numbers assigned to each device in the ATD from the schematics, provided that the schematics is properly "nailed". Or the user can attempt to use some files from the Tescon test program for referencing.

Either method will still require the user to manually enter the nail numbers into the ATD file via the i1000D Test Editor Interface.

Test program files from Tescon systems bear the extension .TPF . These files are formatted to be read by the Tescon software only. The user will not be able to simply open the files using any text editor and checking for the nail numbers of the components. However, it was found that it is possible to save the TPF file to a text-formatted file with a PGA extension. Below is an example of the PGA file and an ATD file loaded in the i1000D software.

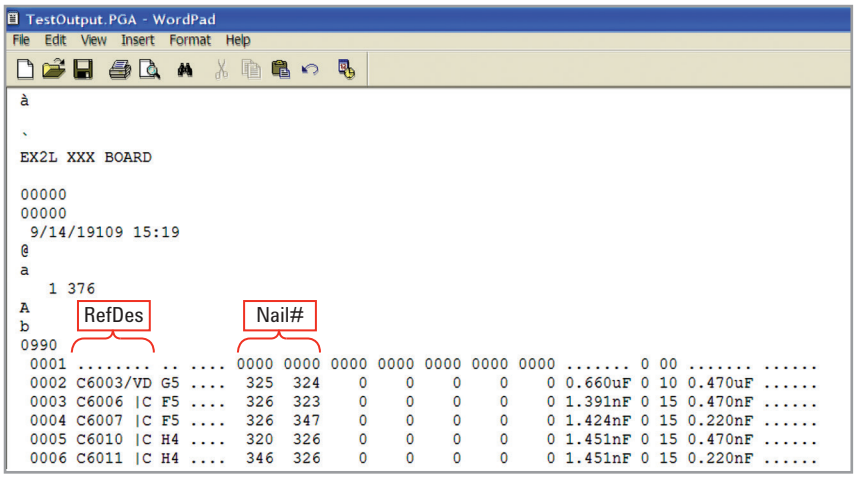


Figure 12. Sample of .PGA file

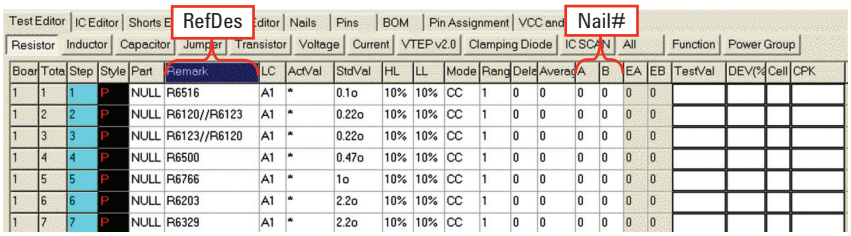


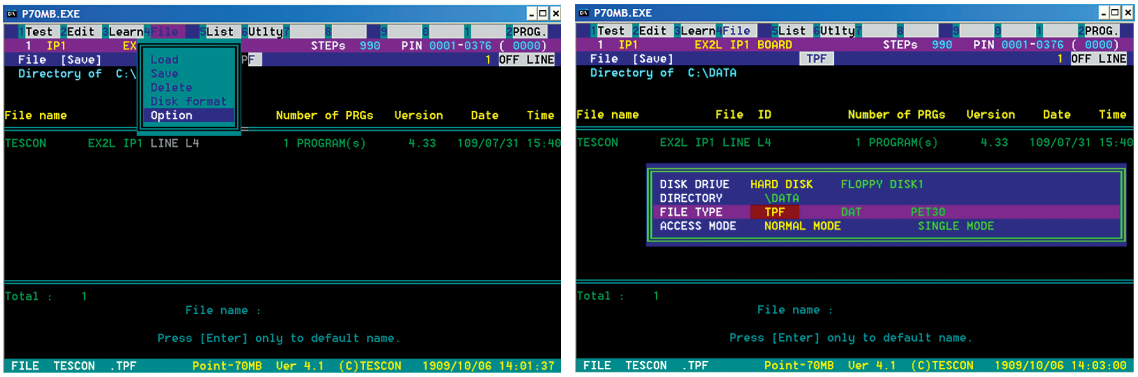
Figure 13. Raw ATD file without nail numbers in i1000D debug interface.

The only missing information in the ATD file is the nail numbers. This is where the user needs to take reference to the PGA file to look for the appropriate nail numbers for the component tests in the ATD file. Although time consuming, this process is the easiest method to complete a test program conversion.

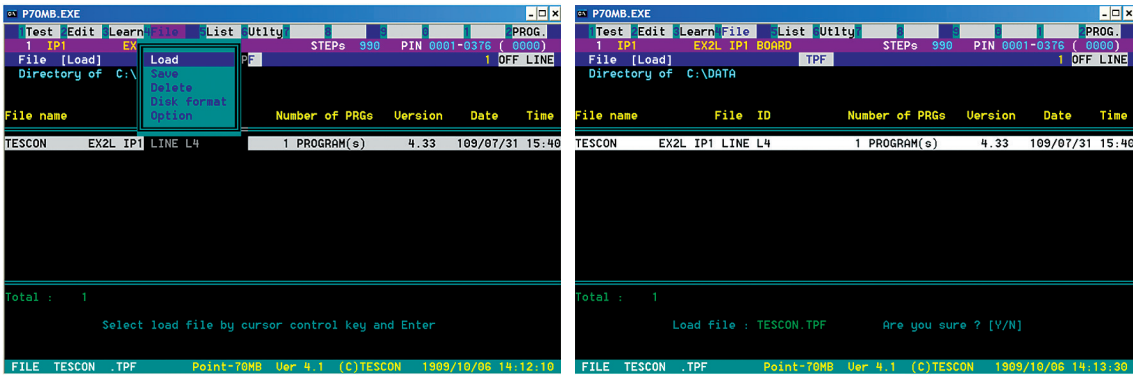
However, if the board contains a huge number of components to the tested, then this method will be too tedious and too error prone. In such cases, the user may need to source for other methods like writing a software script to automate the search process.

The below steps describes the conversion of the TPF file into the text formatted PGA file.

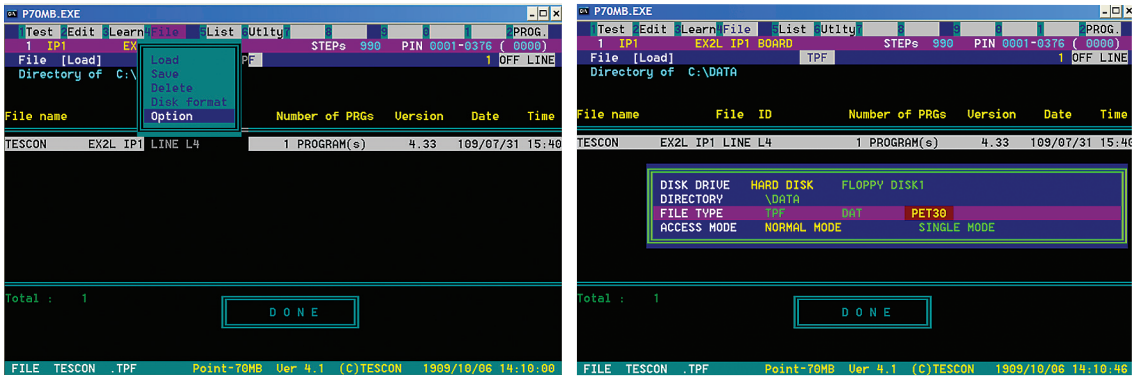
Step 1. Set the file format under the Option menu to TPF format.



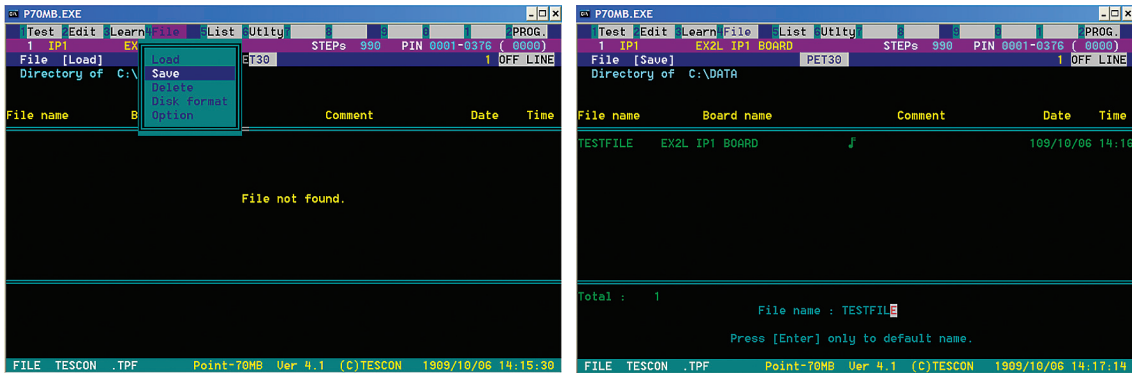
Step 2. Use the arrow keys and Enter to load the TPF file into the Tescon software.



Step 3. Set the file format under the Option menu to PET30 format.



Step 4. Save the loaded file. The PGA file should now be available.



The PGA file is saved to the same folder where the TPF file is located.

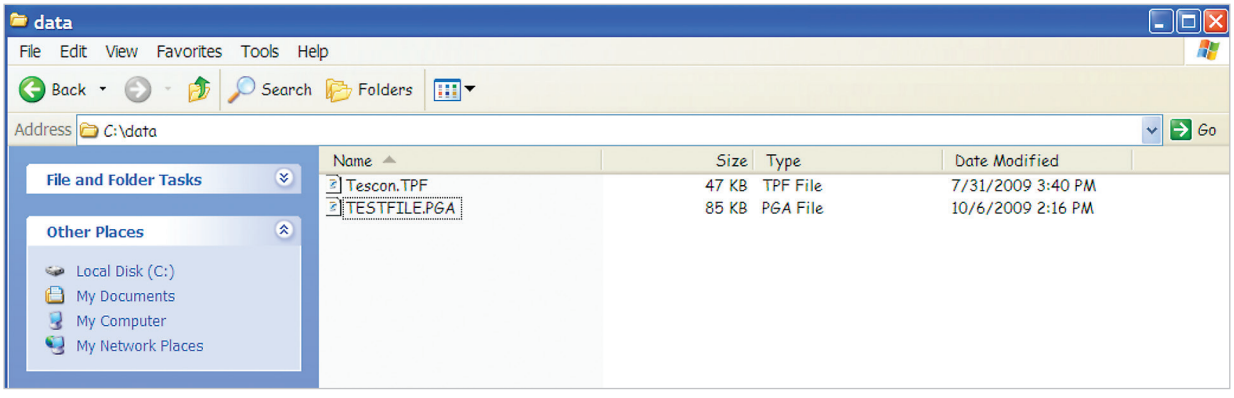


Figure 14. PGA file generated

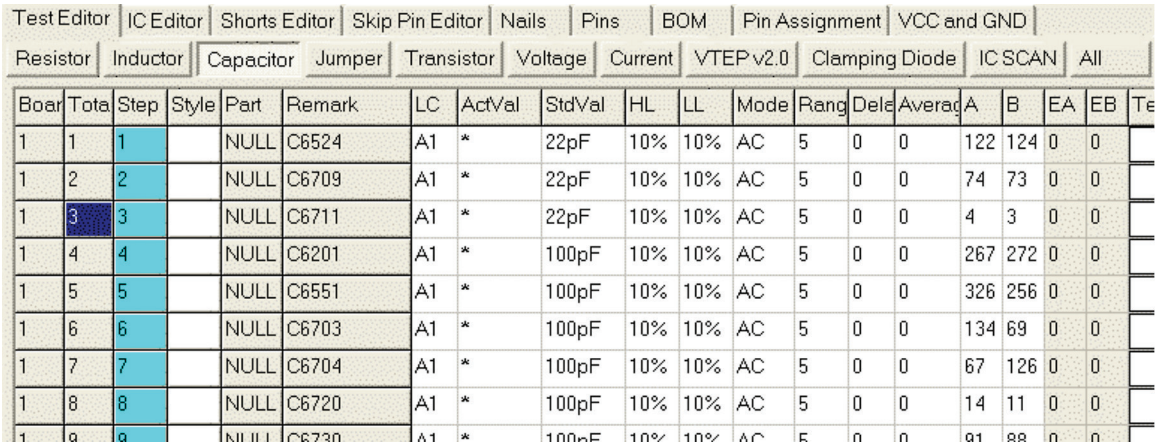
Now that the nails information are available from the PGA file, the user can try to extract the nail numbers from the PGA file and then enter them into the i1000D ATD file. This will complete the test program software conversion process.

Figure 15 below shows a section of the complete ATD file after the nail numbers are entered.

With the ATD file completed, you can now proceed with the debugging of the tests on using the Tescon fixture on the *Medalist* i1000D system. The debug will need to be done as though it is a brand new program because the ATD was converted directly from the existing Tescon program. Therefore, you will need to treat the ATD file as a new program and debug from scratch.

Users can apply their usual debugging techniques for the tests but should also bear in mind that because the nail numbers of the ATD file had been manually entered, there is a possibility of mistakes and type errors. Therefore, it's always a good idea to double check the nail numbers of the fail tests to the schematics.

The next section of this document shares the result of an evaluation that take place between the *Medalist* i1000D and the Tescon Point70 system.



Boar	Tota	Step	Style	Part	Remark	LC	ActVal	StdVal	HL	LL	Mode	Rang	Dela	Averag	A	B	EA	EB	Te
1	1	1		NULL	C6524	A1	*	22pF	10%	10%	AC	5	0	0	122	124	0	0	
1	2	2		NULL	C6709	A1	*	22pF	10%	10%	AC	5	0	0	74	73	0	0	
1	3	3		NULL	C6711	A1	*	22pF	10%	10%	AC	5	0	0	4	3	0	0	
1	4	4		NULL	C6201	A1	*	100pF	10%	10%	AC	5	0	0	267	272	0	0	
1	5	5		NULL	C6551	A1	*	100pF	10%	10%	AC	5	0	0	326	256	0	0	
1	6	6		NULL	C6703	A1	*	100pF	10%	10%	AC	5	0	0	134	69	0	0	
1	7	7		NULL	C6704	A1	*	100pF	10%	10%	AC	5	0	0	67	126	0	0	
1	8	8		NULL	C6720	A1	*	100pF	10%	10%	AC	5	0	0	14	11	0	0	
1	9	9		NULL	C6730	A1	*	100pF	10%	10%	AC	5	0	0	91	88	0	0	

Figure 15. Medalist i1000D ATD file with nail numbers.

Customer Evaluation Results

The target device under test (DUT) is a power supply board used for LCD TVs. The customer's test strategy for this board is mainly unpowered analog test since it has be tested on the Tescon Point70. The board is small in node count and contains mostly analog devices.

Board Information

Board Type:	LCD power supply board
Total Nodes:	Approximately 350 nodes
Accessibility:	100%

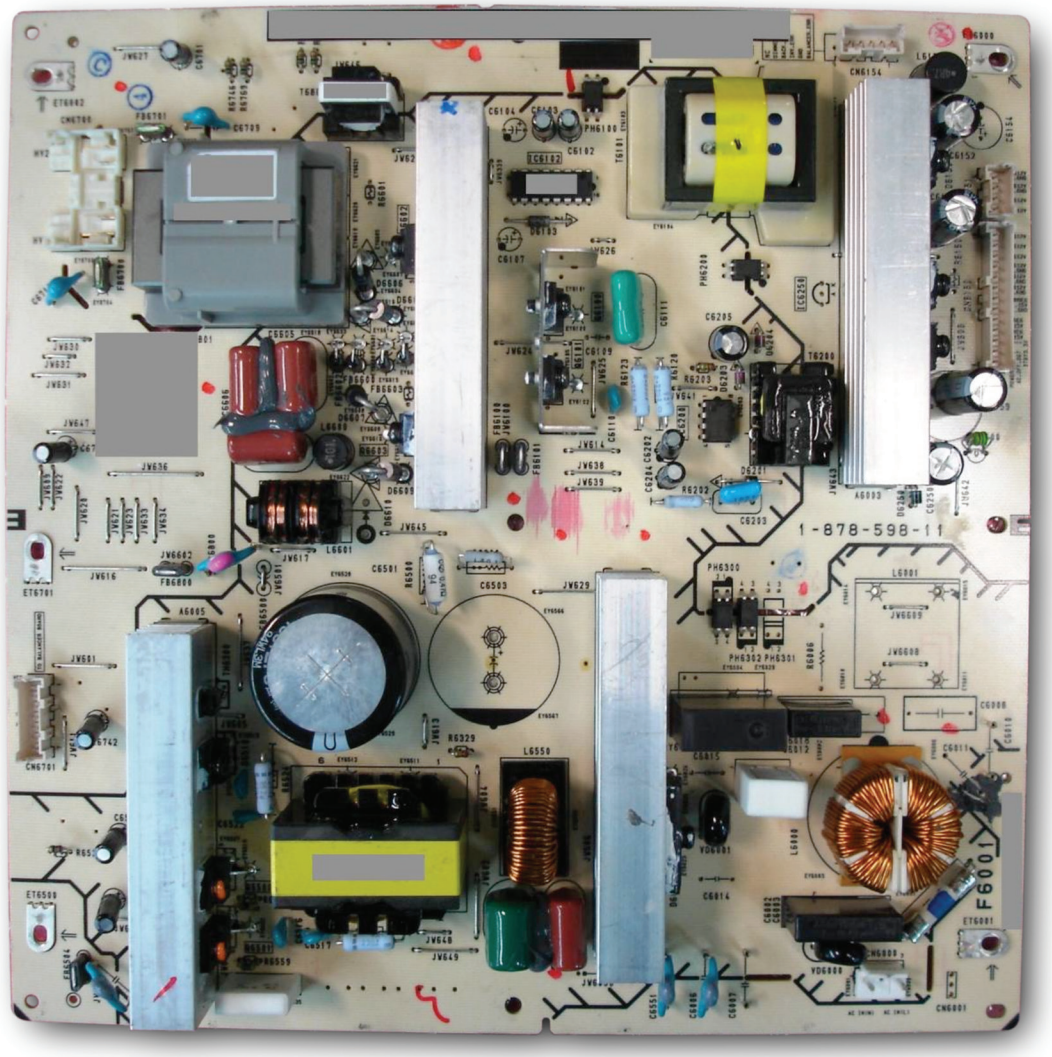


Figure 16. Picture of target board for evaluation.

Evaluation setup

– Boards selected at random to test on i1000D
– All boards to be tagged with serial numbers for tracking purposes
– Each board tested 1 time without fixture cycling retest
– All failures to be diagnosed but NOT repaired
– Data logging enabled to collect data.

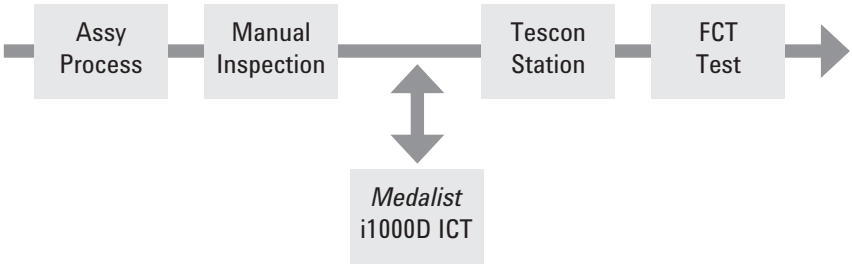


Figure 17. Evaluation test setup flow

Hardware conversion

The pictures below show the hardware conversion that has taken place in order to put the Tescon fixture onto the i1000D system.

– Customize flat cables for 64-pins to 32-pins connection (Figure 18a)
– Improvised fixture guide to secure smaller Tescon fixtures (Figure 18b)
– Adjusted press travel to cater for the height of Tescon fixtures (Figure 18c)

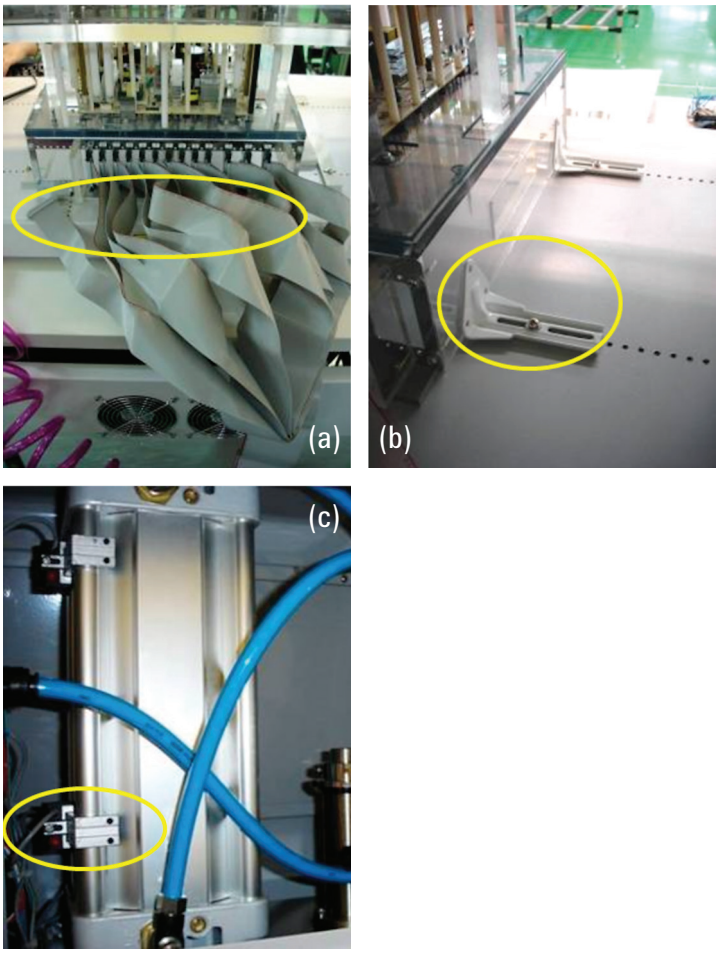


Figure 18. Converting Tescon fixture for i1000D

Test coverage of DUT on i1000D

Being 100% test accessible, the test coverage of the board can be near to 100% if we consider parallel capacitors as tested devices. The Tescon system does not support Keysight VTEP Technology, as such only clamping diode tests are employed. However, as the board consists of many analog ICs, which may not have clamping diodes at all, it resulted in some of the pins of the IC being not testable. However, if the fixture was to be modified to include Keysight VTEP technology, the over test coverage will be increased dramatically.

Type	Untested	Tested	Total	Coverage
Capacitors	8	112	120	92.5%
Resistors	0	173	173	100%
Jumpers	0	90	90	100%
Inductors	0	17	17	100%
Diodes	0	35	35	100%
Transistors/FET	0	30	30	100%
Fuse	0	1	1	100%
Relays	0	1	1	100%
Connectors	0	11	11	100%
Thermistors	0	1	1	100%
Varistors	0	2	2	100%
Transformers	0	4	4	100%
IC	16pins	55pins	71pins	77.46%

Overall Test Coverage for board = 95.68%

Test time comparison

Table 2 shows the detailed breakdown of the test time of each test type on the i1000D. For the Tescon system, no breakdown was available. With the test of the i1000D running at below 7 sec/board and the Tescon test time at 17sec/board, the i1000D proves to be more than twice as fast as the Tescon system. These test times are measured using the same test coverage on both systems.

Table 2. Test time comparison

Test Time (sec)	i1000D	Tescon
Discharge, open/short	**1.141**	
Discharge	0.109	
Open	0.141	
Shorts	0.891	
Component	**5.844**	
Resistors	2.375	
Capacitor	1.172	
Jumper	0.922	
Inductor	0.125	
Transistor/Diode/FET	1.188	
VTEP/Clamp Diode	0,062	
Total	**6.985**	**17.1**

Production run results

A total of 190 boards were tested on the i1000D. These boards were fresh from the assembly line and were not tested on any other station prior to the i1000D. On the i1000D station, the automatic Fixture Retest feature was intentionally turned off in order to monitor the level of probe contact related failures.

The result achieved on the i1000D shows a probe contact related failure rate of 6.3%. False calls resulting mostly from tight test limits of a new test program were at 2.11%. If the probe contact failures are eliminated, the effective first pass yield is projected at above 95%. Out of the 190 boards tested on the i1000D, 90 boards were tested through the Tescon system to gather data for correlation. The false call rate was slight higher on the Tescon system by about 1%. Probe contact related failures came in at about 4%, but this was with the fixture retest feature of the Tescon system turned on.

The Fixture Retest feature mentioned above is the feature for the system to automatically release the fixture and reengage it when there is a failure occurring. Upon the second engagement of the fixture, only the failed tests will be retested. This feature is widely used in the industry to minimize the effect of poor probe contact issues.

On defects correlation, most of the failures are correlated except for a transformer (T6800) upon which both systems were performing inductance test. The board was found to fail at the i1000D system but it managed to pass marginally on the Tescon.

Table 3. Initial production test data

Summary Results	**i000D**	**Tescon**
Total Board Tested	100 Fresh Bds = 90 Good Bds	90 Good Bds
Contact Failures	6.32% (without Fixture Retest)	4.44% (with Fixture Retest)
False Calls	2.11%	3.33%
True Failures	2.63%	2.22%
Effective Passing Yield	95.28%	94.44%
Failures Breakdown		
Contact Failures	Open Fail (Nail 5 to 9) x 2	
	Open Fail (JR608) x 1	
	C6003 x 1	
	C6110 x 1	
	C6601, C6602 x 1	
	C6744, R6747, R6749, Q6706 x 1	
	C6724 x 1	D6152 x 1
	C6738, R6158 x 1	R6156SI x 1
	R6500 x 2	Q6305S x 1
	T6200 Open x 1	Q6101 x 1
Marginal Failures	C6800 x 2	D6511S x 1
	C6024 x 1	FB6601, FB6603 x 1
	C6011 x 1	R6307, R6737 x 1
No Solder	Q6702 x 1	Q6702 x 1
Defective part	D6003 x1	D6003 x1
	L6501 x 1	L6501 x 1
	T6800 x 2	T6800 x 2

More production boards were tested through the i1000D for four days to collect more data on the i1000D performance.

For the first three days, the i1000D was operating without the Fixture Retest enabled. This resulted in higher Contact Issue and False call rate. On Day 4, the fixture retest on the i1000 was enabled. It can be seen that a significant improvement in the contact failures was achieved. The false call rate dropped to about 1%.

Overall, the customer was impressed with the 2.5x improvement on test time that the i1000D offers over the Tescon system. This comes along with the test stability and repeatability that resulted in lower false call percentage and a real first pass yield above 96.6%.

Table 4. Production test data collated over four days.

	Number of boards tested without Fixture Retest			Number of boards tested with Fixture Retest
	Day 1	Day 2	Day 3	Day 4
Total Tested	120	110	150	150
Passed	107	97	133	145
True Fail	3	2	5	3
Contact Issue	4	6	7	0
False Fail	6	5	5	2
Pass Yield (%)	89.17	88.18	88.67	96.67

Conclusion

The i1000D is designed to span across low to mid-high complexity board testing where operational costs is a huge factor in the equation. With its low cost prepress-down fixture, the i1000D proves to be a perfect fit in these environments.

Converting the Tescon fixture and program to the i1000D is not difficult. The main challenge lies in the manual conversion of the test program for nail numbers. However, if the user develops a script to automate the conversion process, this will make the migration from the Tescon system to Medalist i1000D a simple task.

Appendix

Sample of PIN File

E9900 eM-Test Expert (R)
Part Pins List 0/1100 Selected Parts 20-Mar-2007 10:35
INCH units

Part	T/B					
Pin	Name	X	Y	Layer	Net	Nail(s)
Part C1	(T)					
1	1	0.5124	4.3500	1	02_23_64	453
2	2	0.4376	4.3500	1	SERIES_02_23_64	533
Part C2	(T)					
1	1	-0.0250	8.7750	1	DCOM	1
2	2	-0.1250	8.7750	1	VCC	2
Part R1	(T)					
1	1	0.5124	4.2500	1	02_23_64	453
2	2	0.4376	4.2500	1	VCC	2
Part R2	(T)					
1	1	0.4376	4.1500	1	DCOM	1
2	2	0.5124	4.1500	1	02_23_64	453
Part J8	(T)					
1	1	2.5250	7.9500	1	DCOM	1
2	2	2.4750	7.9500	1	02_14_64	622
3	3	2.4250	7.9500	1	02_22_64	425
4	4	2.3750	7.9500	1	N$152684	308
5	5	2.3250	7.9500	1	02_20_64	460
6	6	2.2750	7.9500	1	02_17_64	534
7	7	2.2250	7.9500	1	DCOM	1
8	8	1.9750	7.9500	1	VCC	2
9	9	1.9250	7.9500	1	VCC	2
10	10	1.8750	7.9500	1	VCC	2
11	11	1.8250	7.9500	1	DCOM	1
12	12	1.7750	7.9500	1	DCOM	1
13	13	1.7250	7.9500	1	DCOM	1
14	14	1.6750	7.9500	1	VCC	2
15	15	1.6250	7.9500	1	VCC	2
16	16	1.5750	7.9500	1	VCC	2
17	17	1.5250	7.9500	1	DCOM	1
18	18	1.4750	7.9500	1	02_15_64	623
19	19	1.4250	7.9500	1	DCOM	1
20	20	1.3750	7.9500	1	VCC	2
21	21	1.3250	7.9500	1	VCC	2
22	22	1.2750	7.9500	1	VCC	2

Sample of NAIL file

E9900 FABMASTER (R)
Test Fixture Nails 884/5682 Selected Drills 5-Mar-2007 13:08
884 Nails, 898 Nets INCH units

Nail	X	Y	Type	Grid	T/B	Net	Net Name	Virtual Pin/Via
$1	1.0713	3.5229	2	8D	(B)	#873	DCOM	PIN J3.242
$1	-0.1910	7.5364	2	9G	(B)	#873	DCOM	PIN J4.11
$1	2.9500	0.0500	1	7A	(B)	#873	DCOM	PIN TP_1038.1
$1	8.2500	11.5500	1	3J	(B)	#873	DCOM	PIN TP_17.1
$1	2.7500	11.5500	1	7J	(B)	#873	DCOM	PIN TP_72.1
$1	7.8500	-0.0500	1	3A	(B)	#873	DCOM	PIN TP_989.1
$1	6.0000	5.0000	1	5E	(B)	#873	DCOM	PIN JMP10.3
$1	10.7000	3.3250	1	1D	(B)	#873	DCOM	PIN JMP9.3
$2	5.9406	4.7248	2	5E	(B)	#1	VCC	PIN J10.2
$2	1.3343	4.5004	2	8E	(B)	#1	VCC	PIN J10.235
$2	2.8304	3.6804	2	7D	(B)	#1	VCC	PIN J3.197
$2	-0.0335	7.3002	2	9G	(B)	#1	VCC	PIN J4.30
$2	6.2500	11.5500	1	4J	(B)	#1	VCC	PIN TP_37.1
$2	9.8500	2.4500	1	2C	(B)	#1	VCC	PIN TP_529.1
$3	1.1500	11.0500	1	8J	(B)	#117	02_05_164	PIN TP_176.1
$4	1.2500	11.0500	1	8J	(B)	#129	02_05_64	PIN TP_175.1
$5	1.3500	11.0500	1	8J	(B)	#85	2_04_164	PIN TP_174.1
$6	1.4500	11.0500	1	8J	(B)	#97	02_04_64	PIN TP_173.1
$7	1.5500	11.0500	1	8J	(B)	#116	02_05_163	PIN TP_172.1
$8	1.6500	11.0500	1	8J	(B)	#128	02_05_63	PIN TP_171.1
$9	1.7500	11.0500	1	8J	(B)	#84	02_04_163	PIN TP_170.1
$10	1.8500	11.0500	1	8J	(B)	#96	02_04_63	PIN TP_169.1
$11	1.9500	11.0500	1	8J	(B)	#115	02_05_162	PIN TP_168.1
$12	2.0500	11.0500	1	8J	(B)	#127	02_05_62	PIN TP_167.1
$13	2.1500	11.0500	1	8J	(B)	#83	02_04_162	PIN TP_166.1
$14	2.2500	11.0500	1	8J	(B)	#95	02_04_62	PIN TP_165.1
$15	2.3500	11.0500	1	7J	(B)	#114	02_05_161	PIN TP_164.1
$16	2.4500	11.0500	1	7J	(B)	#126	02_05_61	PIN TP_163.1
$17	2.5500	11.0500	1	7J	(B)	#82	02_04_161	PIN TP_162.1
$18	2.6500	11.0500	1	7J	(B)	#94	02_04_61	PIN TP_161.1
$19	1.1500	11.5500	1	8J	(B)	#54	02_03_164	PIN TP_88.1
$20	1.2500	11.5500	1	8J	(B)	#65	02_03_64	PIN TP_87.1
$21	1.3500	11.5500	1	8J	(B)	#23	02_02_164	PIN TP_86.1
$22	1.4500	11.5500	1	8J	(B)	#34	02_02_64	PIN TP_85.1
$23	1.5500	11.5500	1	8J	(B)	#53	02_03_163	PIN TP_84.1

Sample of NAIL file (continued)

Nail	X	Y	Type	Grid	T/B	Net	Net Name	Virtual Pin/Via
$24	1.6500	11.5500	1	8J	(B)	#64	02_03_63	PIN TP_83.1
$25	1.7500	11.5500	1	8J	(B)	#22	02_02_163	PIN TP_82.1
$26	1.8500	11.5500	1	8J	(B)	#33	02_02_63	PIN TP_81.1
$27	1.9500	11.5500	1	8J	(B)	#52	02_03_162	PIN TP_80.1
$28	2.0500	11.5500	1	8J	(B)	#63	02_03_62	PIN TP_79.1
$29	2.1500	11.5500	1	8J	(B)	#21	02_02_162	PIN TP_78.1
$30	2.2500	11.5500	1	8J	(B)	#32	02_02_62	PIN TP_77.1
$31	2.3500	11.5500	1	7J	(B)	#51	02_03_161	PIN TP_76.1
$32	2.4500	11.5500	1	7J	(B)	#62	02_03_61	PIN TP_75.1
$33	2.5500	11.5500	1	7J	(B)	#20	02_02_161	PIN TP_74.1
$34	2.6500	11.5500	1	7J	(B)	#31	02_02_61	PIN TP_73.1
$35	3.5500	11.0500	1	7J	(B)	#113	02_05_144	PIN TP_152.1
$36	3.6500	11.0500	1	6J	(B)	#125	02_05_44	PIN TP_151.1
$37	3.7500	11.0500	1	6J	(B)	#81	02_04_144	PIN TP_150.1
$38	3.8500	11.0500	1	6J	(B)	#93	02_04_44	PIN TP_149.1
$39	3.9500	11.0500	1	6J	(B)	#112	02_05_143	PIN TP_148.1
$40	4.0500	11.0500	1	6J	(B)	#124	02_05_43	PIN TP_147.1
$41	4.1500	11.0500	1	6J	(B)	#80	02_04_143	PIN TP_146.1
$42	4.2500	11.0500	1	6J	(B)	#92	02_04_43	PIN TP_145.1
$43	4.3500	11.0500	1	6J	(B)	#111	02_05_142	PIN TP_144.1
$44	4.4500	11.0500	1	6J	(B)	#123	02_05_42	PIN TP_143.1
$45	4.5500	11.0500	1	6J	(B)	#79	02_04_142	PIN TP_142.1
$46	4.6500	11.0500	1	6J	(B)	#91	02_04_42	PIN TP_141.1
$47	4.7500	11.0500	1	6J	(B)	#110	02_05_141	PIN TP_140.1
$48	4.8500	11.0500	1	6J	(B)	#122	02_05_41	PIN TP_139.1
$49	4.9500	11.0500	1	5J	(B)	#78	02_04_141	PIN TP_138.1
$50	5.0500	11.0500	1	5J	(B)	#90	02_04_41	PIN TP_137.1
$51	3.5500	11.5500	1	7J	(B)	#50	02_03_144	PIN TP_64.1

Sample of formatted i1000 BOM

```
C6003;C;0.47uF;10%;10%;;0.47uF;
C6006;C;470pF;10%;10%;;470pF;
C6007;C;220pF;10%;10%;;220pF;
C6010;C;470pF;10%;10%;;470pF;
C6011;C;220pF;10%;10%;;220pF;
C6018;C;0.22uF;10%;10%;;0.22uF;
CN6000;J;;;;;3Pin connector;
CN6150;J;;;;;13Pin connector;
D6000;Q;;;;;D10XB60S;
D6001;Q;;;;;MA2J1110GLS0;
D6003;Q;;;;;MA4J1130GLS0;
F6001;JP;1JP;F;F;;FUSE (H.B.C.);
FB6100;JP;1JP;F;F;;"INDUCTOR, FERRITE BEAD";
FB6101;JP;1JP;F;F;;"INDUCTOR, FERRITE BEAD";
FB6600;L;0.45UH;10%;10%;;0.45UH;
FB6601;L;0.45UH;10%;10%;;0.45UH;
IC6101;IC;;;;;MM1431CURE;
IC6102;IC;;;;;CXD9969P;
IC6200;IC;;;;;MIP2H2;
IC6251;IC;;;;;MM1530CURE;
IC6300;IC;;;;;MM3313AFFE;
JR605;JP;1JP;F;F;;3216;
JR606;JP;1JP;F;F;;"CONDUCTOR, CHIP";
L6000;JP;1JP;F;F;;LINE FILTER COIL;
L6151;L;4.7UH;10%;10%;;4.7UH;
L6501;L;165UH;10%;10%;;165UH;
L6550;L;260UH;10%;10%;;260UH;
L6600;L;100UH;10%;10%;;100UH;
Q6100;Q;;;;;TK8A50D;
Q6101;Q;;;;;TK8A50D;
Q6300;Q;;;;;2SA1364-T111-1DE;
Q6302;Q;;;;;2SC3052EF-T1-LEF;
Q6305;Q;;;;;ISA1235AC1TP-1EF;
Q6400;Q;;;;;RT1N14BC-TP-1;
R6010;R;1.0M;10%;10%;;1.0M;
R6011;R;1.0M;10%;10%;;1.0M;
R6015;R;560K;10%;10%;;560K;
R6016;R;6.8;10%;10%;;6.8;
R6017;R;100K;10%;10%;;100K;
R6018;R;470K;10%;10%;;470K;
R6019;R;560K;10%;10%;;560K;
R6100;R;150K;10%;10%;;150K;
R6102;R;100;10%;10%;;100;
R6103;R;12K;10%;10%;;12K;
R6105;R;2M;10%;10%;;2M;
R6106;R;2M;10%;10%;;2M;
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