Keysight Technologies

In-Circuit Test (ICT): The King Is Dead; Long Live the King!

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Position Statement

Reports of the demise of In-Circuit Testing have been exaggerated for at least 20 years. Like Mark Twain in his day, ICT is still here and kicking. Why is this? Some reasons have been offered:

- It's what we know how to do.
- There's no alternative with decent defect coverage.
- ICT gives me actionable information like no other technology out there.
- It's pretty scary to think of not having it.
- We've got lots of equipment, all paid up – we can't just junk it!
- We can work with board designers to regain access.
- Even as hard as it is to test today's boards, it's worth it.

Some of these reasonings are emotional, or hard to quantize. But people cling to ICT because the "next big thing" is simply not out there to replace it. Losing structure-based tests leaves us with functional test and system test, right out of the reflow oven. This view of the future keeps production managers up late at night.

Another factor is that in the domain of ICT that can run powered-up tests, Design-for-Test technologies driven by the IEEE 1149.1-based family of DFT standards, have been able to augment "real" access with virtual access, with reasonable success. Boundary Scan has helped ICT users adapt to access problems. No longer do we need "100% node access" (as if we ever had that). Now we need to be very smart about "critical access". Not all nodes are created equal when it comes to the needs of testing.

I represent a company with a line of In-Circuit testers used across the globe. What has kept us viable has been to recognize "critical access" and to concentrate on developing new ways to keep ICT relevant. Some examples are capacitive sensing technologies (e.g., the well-known TestJet technology). The aforementioned 1149.1, and then 1149.6 DFT standards that industry has embraced are also critical complements to ICT. Both these examples allow us to use the access we have more effectively. That is, when access is incrementally degraded, our coverage may degrade incrementally rather than catastrophically. In some cases, coverage can even stay constant as access goes down. As an example, when testing a digital component using ICT nails only (no Boundary Scan), then losing access to just one input pin of that device may kill the test altogether with total loss of coverage on all its pins. If that same device is part of a Boundary Scan test, then there are only four pins (the TAP port) that are absolutely critical to coverage. If that same device were tested with capacitive sensing, then losing access to a few pins just loses opens coverage for those same few pins, not all of them; degradation is linear.

It should also be recognized that an ICT platform is like a large box of tools. Having a lot of tools are your disposal is better than having a very limited set. Twisting in a screw is most easily done with a screwdriver, not a hacksaw. Thus, it is likely that adding new tools to the ICT toolbox will be the success strategy for the future, not eliminating the toolbox itself. At this time we see no other toolboxes on the horizon that have the wide range of capabilities we will continue to need, moving forward.

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