

# Keysight Technologies

## Instrumentation-grade Clock Recovery Solutions to 32 Gb/s



## Synchronization for receiver BER testing and transmitter waveform analysis

- Continuous, un-banded tuning from 50 Mb/s to 32 Gb/s
- Ultra low residual jitter: as low as 100 femtoseconds rms
- Simplified receiver test with jitter tolerance test mode and data demultiplexer
- Golden PLL operation with adjustable peaking and a tunable loop bandwidth from 30 kHz to 20 MHz for configurable industry standard compliance test
- Optical and electrical configurations
- PLL BW/jitter transfer and phase noise/jitter spectrum analysis



Figure 1: The N4877A accepts single ended or differential electrical inputs to 32 Gb/s



Figure 2: For optical test, two coupler/converter solutions are available to pair with the N4877A

## Clock recovery solutions for BER based receiver test and waveform analysis

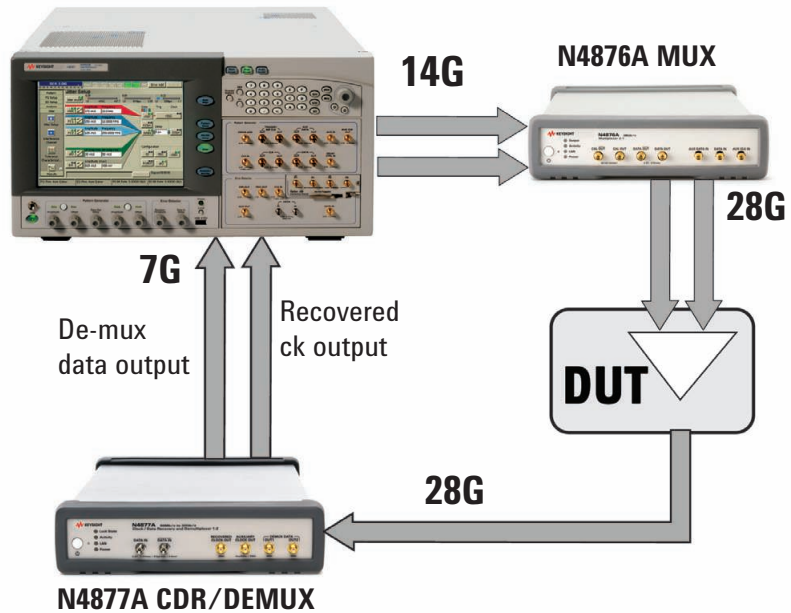
Both bit-error-ratio-testers (BERTs) and DCA's require a clock signal to synchronize the measurement system to the incoming data stream. When the necessary synchronous clock/trigger is not available, a common solution is to derive a clock from the data being measured. But the recovered clock approach can be more than just an alternative method for instrument synchronization. Many test standards (IEEE 802.3 Ethernet, Fibre Channel etc.) require the use of a "Golden PLL" (phase locked loop) jitter transfer characteristic or loop bandwidth to control what spectrum of jitter is observed and what is removed from the tests. If the loop bandwidth is too wide, too much high-frequency jitter is removed from the observed signal. If the loop bandwidth is too narrow, measurements can be obscured with lower frequency jitter. This jitter is usually less important since receivers easily tolerate this. Testing with an optimal loop bandwidth assures that good parts do not appear to be bad, and bad parts do not appear to be good.

The Keysight Technologies, Inc. N4877A is a clock recovery instrument that can derive a clock from differential or single-ended NRZ signals at rates as low as 50 Mb/s, as high as 32 Gb/s, and any rate between, providing the ultimate in flexibility and value. Output signals include extracted clock (full rate and user defined divide ratios), auxiliary clock (from 4 to 8 GHz for use with the 86100 precision timebase) and a two-port de-multiplexed data stream used to extend the effective operating range of 12.5 Gb/s error-detectors to 28 Gb/s. With jitter as low as 250 femtoseconds rms, the residual jitter of the output clock allows high margin in jitter tolerance/receiver tests.

The auxiliary clock provided by the N4877A is ideal for use with the 86100 sampling oscilloscope when configured with the 86107A precision timebase. With under 100 fs of residual jitter, this timing reference assures accurate measurements of high-speed, low-jitter waveforms. These products have tunable loop bandwidths to as wide as 20 MHz. This critical feature allows the

clock recovery system to be configured as a Golden PLL with the optimal loop bandwidth for whatever data rate is being tested. Test systems can now be designed according to the exact specifications of industry standards.

There are two versions of the N4877A. Option -216 operates from 50 Mb/s to 16.5 Gb/s while option 232 operates from 50 Mb/s to 32 Gb/s.



## Clock recovery for optical signals

When testing optical signals, the N1070A combines the N4877A with the N1075 optical coupler/converter. The N1075A has a single-mode/multimode configuration that operates to over 16 Gb/s and another configuration that operates on single-mode signals to 32 Gb/s



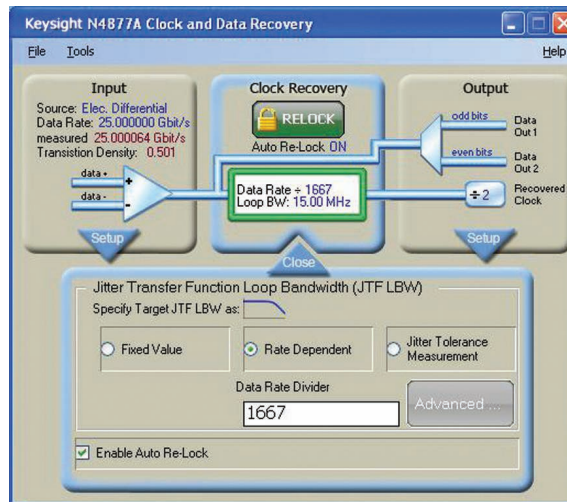
## Compact and easy to use

The clock recovery instrument form factor is very compact allowing easy placement with other instruments whether in a rack or on a benchtop. A USB 2.0 connection to a laptop PC provides a simple and intuitive user interface for data rate, loop BW, and clock controls.



## PLL and jitter spectrum analysis

Use 86100CU-400 software to make fast, accurate and repeatable measurements of phase-locked loop (PLL) bandwidth/jitter transfer. With a precision jitter source, the 83496B, N4877A, and N1070A can be configured as a jitter receiver to create a PLL stimulus-response test system. PCI Express® approved PLL bandwidth compliance tests and SONET/SDH jitter transfer measurements are pre-configured, with automatic report generation. 86100CU-400 software also provide insights into the root causes of jitter through phase noise and jitter spectrum analysis on both clock and data signals.



## Target Applications

- Receiver tolerance compliance testing
- System level waveform analysis
- Root cause analysis of jitter
- General purpose clock recovery applications

## (Key specification table)

- Data rates: 50 Mb/s to 32 Gb/s, continuously tunable
- Tunable loop bandwidth to 20 MHz
- Optical signals: MMF to 16 Gb/s, SMF to 32 Gb/s
- Residual jitter as low as 100 fs
- Demultiplexed data (dual half rate outputs)

For detailed specifications see Keysight literature 5990-9949EN

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