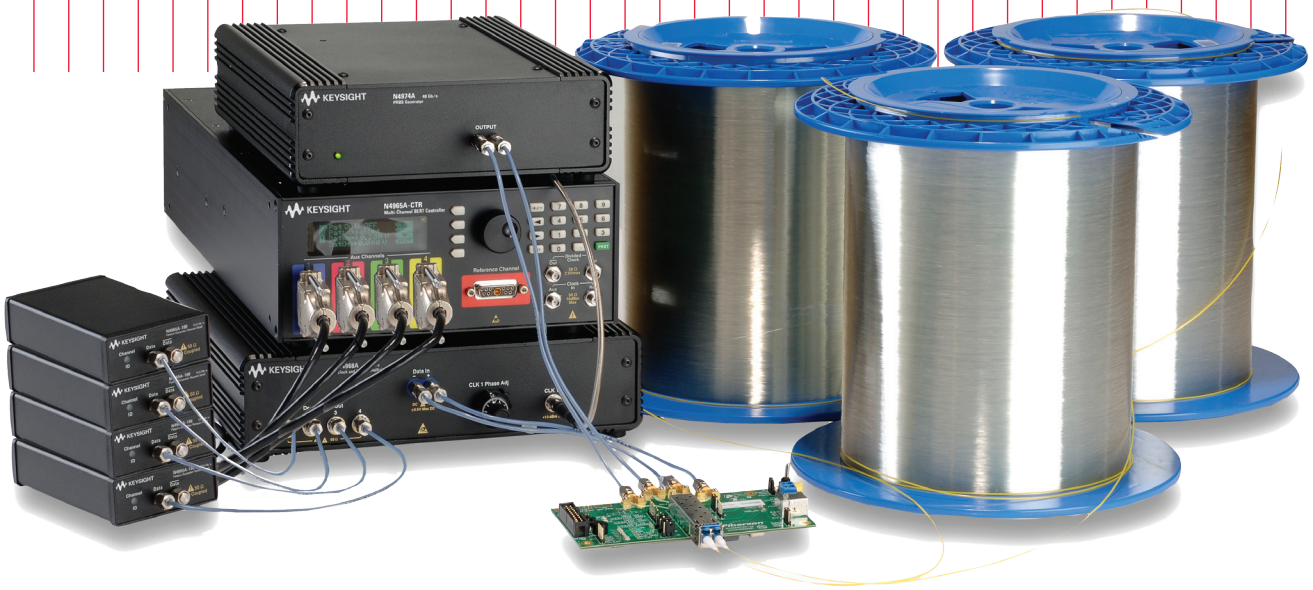
Keysight Technologies

N4967A Serial BERT System 44 Gb/s 40G BER test system

Data Sheet



KEYSIGHT TECHNOLOGIES

Complete cost effective solution for 40, 28, and 25 Gb/s device characterization and production testing

Key features

- Operates at data rates from 22 to 44 Gb/s with external clock
- Built-in clock for operation at 40 Gb/s
- True PRBS pattern generation at full data rate
- Supports differential or single ended inputs and outputs
- Remote control through USB or GPIB
- Compact size

Modular system architecture

The N4967A serial BERT system 44 Gb/s is formed from three main components:

- N4974A PRBS Generator 44 Gb/s
  Provides a true PRBS pattern at full data rate to stimulate the device under test.
- N4968A clock and data demultiplexer 44 Gb/s
  De-multiplexes the full rate output data stream from the device under test into 4x sub-rate data streams. Also divides the high speed clock to provide a selection of lower speed clock outputs.
- N4965A multi-channel BERT 12.5 Gb/s
  Measures the bit error rate of the 4x de-multiplexed data streams and provides clock control for the clock and data demultiplexer 44Gb/s.

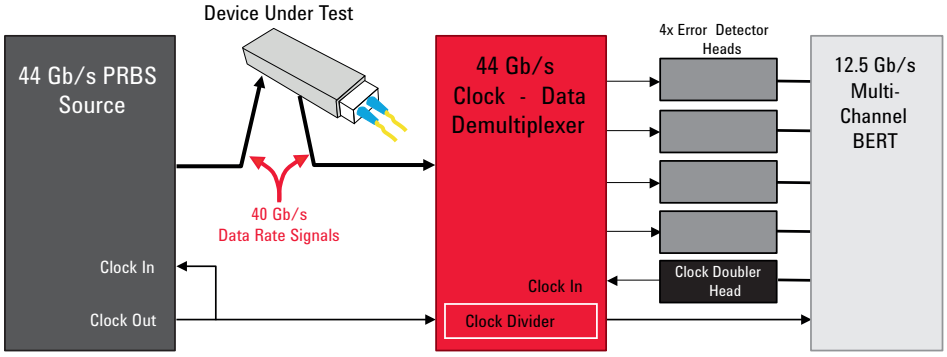


Figure 1. Typical test setup at 40Gb/s using internal clock.

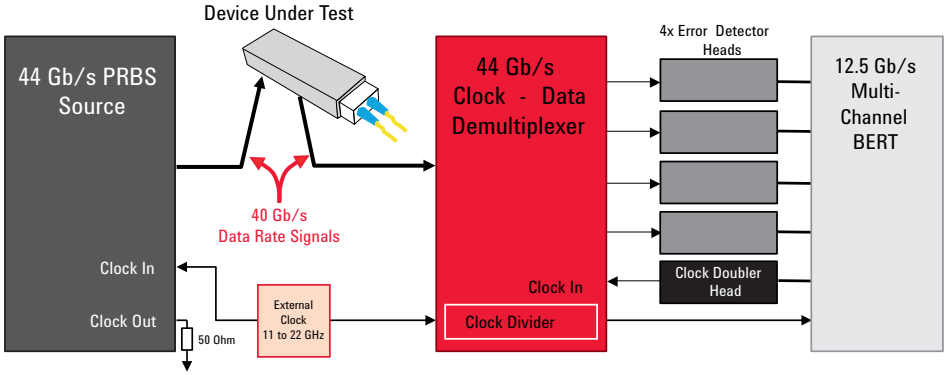


Figure 2. Typical test setup using external clock for 22 to 44 Gb/s operation.

System configuration

The N4974A PRBS generator 44 Gb/s source can produce PRBS 7, 15, or 31 patterns, providing flexible trade-off between test duration and pattern dependent stress level. An internal low jitter clock source provides operation at 39.8 Gb/s. Alternatively the generator can be clocked from an external source for operation at any rate between 22 and 44 Gb/s (half-rate clock required).

Data outputs are differential, and can be used in single-ended applications by terminating the unused output with a 50 ohm load. The PRBS source also provides pattern trigger and clock outputs, which can be used to trigger a sampling oscilloscope to view the bit stream or a classic eye diagram.

Figure 3. N4974A

The N4968A clock and data demultiplexer 44 Gb/s can accept differential or single ended input signals, and has 4x data outputs at ¼ of the bit rate. Also included in the N4968A clock and data demultiplexer 44 Gb/s are separate clock dividers which can be used to provide the correct divided-clock rate for the BERTs measuring the data outputs.

Electronic control of the high speed clock phase shifter allows for automatic clock-data timing of the N4968A clock and data demultiplexer 44 Gb/s clock and data inputs.

Figure 4. N4968A

The N4965A multi-channel BERT 12.5 Gb/s with 4x N4956A-E12 12.5 Gb/s error detector remote heads monitors the demultiplexer data outputs bit error ratio. The N4957A-C12 clock doubler remote head facilitates electronic phase adjust of the N4968A clock and data demultiplexer 44 Gb/s Clock input for optimizing clock-data phase for the N4968A clock and data demultiplexer 44 Gb/s.

The N4965A multi-channel BERT 12.5 Gb/s can be controlled manually through the front panel, or remotely through IEEE-488 (GPIB) or USB.

Figure 5. N4965A

System automation

In both production testing as well as engineering characterization, automation of the system for instrument control and results data collection are essential.

Tools are provided with the N4967A serial BERT system 44 Gb/s system to simplify the setup and integration into an automated test system.

The N4980A multi-instrument BERT software provides a complete user control interface for performing multi-channel BER testing for the N4967A serial BERT system 44 Gb/s. The application computes the BER at the full data rate.

Bar graphs display the computed BER of the full rate data stream, as well as BER on each de-multiplexed data output - giving a quick visual indication of any sub rate related bit errors.

Figure 6. N4980A multi-instrument BERT software

Specifications

The following tables list specifications of the individual instruments relevant to application in the 40G BERT system. For complete specifications relevant to other applications, refer to the individual product data sheets.

N4974A PRBS Source Specifications

Parameter	Specification
Data Output	
Data rate	22 to 44 Gb/s[1] (option 001)
PRBS patterns	2^7–1 : 1 + X^4 + X^7
	2^{15}–1 : 1 + X^{14} + X^{15}
	2^{31}–1 : 1 + X^{28} + X^{31}
Output amplitude (single-ended)	> 500 mV p-p typical
Output level	High: 0 V nominal
	Low: –500 mV nominal
Jitter	500 fs rms typical[2]
Rise/fall time (20% to 80%)	8 ps typical
Data crossover	55% typical
Data phase adjust range	30 ps nominal
External interface	Differential. DC coupled, 50 Ω nominal, 1.85 mm female connectors.
	NOTE: Outputs are CML and must be externally DC terminated with 50 Ω to GND.
Clock input	
External half-rate clock input range	11 to 22 GHz (option 001)
External half-rate clock input power required	+10 to +16 dBm
External interface	Single-ended. AC coupled, 50 Ω nominal, 2.92 mm female connector.
Internal clock	
Internal half-rate clock frequency	Single frequency internal oscillator
	19.90656 GHz (for 39.81312 Gb/s data rate)
Output power	+16 dBm (4 V p-p) typical
External interface	Single-ended. AC coupled, 50 Ω nominal, 2.92 mm female connector.
Clock trigger output	
Clock trigger (CLK/1) output power	Nominally –16 dB less than Clock Input power
External interface	Single-ended. AC coupled, 50 Ω nominal, 2.92 mm female connector. Terminate if not used.
Pattern trigger output[3]	
Pulse width	64 * (1/Bit_rate)
	e.g. at 40 Gb/s pulse width = 1.6 ns
Repetition period	64 * (1/Bit_rate)*Pattern_length
	e.g. at 40 Gb/s, 2^{31}–1 pattern, period = 3.4 s
Output amplitude	200 mV p-p typical
External interface	Single-ended. DC coupled, 50 Ω nominal, SMA female connector
Power requirements	42 W external AC adapter, 100 to 240 V AC, 47 to 63 Hz

1. With an external clock.
2. At ≤ 40 Gb/s.
3. Pattern trigger specified at ≤ 40 Gb/s only. Remove termination from CLK/1 output when using the Pattern Trigger.

Table 1

Specifications (continued)

N4968A Clock and Data Demultiplexer 44 GB/s Specifications

Parameter	Specification
Data input	
Data rate	3.5 to 44 Gb/s
Data amplitude	150 to 1000 mV p-p single-ended
	Maximum DC voltage ±0.5 V
Interface	Differential. DC coupled, 50 Ω nominal, 1.85 mm female connectors. Can be used single-ended if unused input is terminated with 50 Ω load.
Data output	
Data rate	0.875 to 11 Gb/s
Data amplitude	> 210 mV p-p typical
Interface	Single-ended outputs. AC coupled, 50 Ω nominal, 2.92 mm female connectors.
Clock input	
Type	Half-rate clock
Frequency	1.75 to 22 GHz
Clock amplitude	+2 to +10 dBm (0.8 to 2 V p-p)
Interface	Single-ended input. AC coupled, 50 Ω nominal, 2.92 mm female connector.
Divided clock outputs	
Division ratios	1, 2, 4, 8, 16, 32, and 64
Clock amplitude	> –5 dBm (355 mV p-p) typical
Interface	Differential outputs. AC coupled, 50 Ω nominal, SMA mm female connectors. Can be used single-ended if unused input is terminated with 50 Ω load.
Power requirements	42 W external AC adapter, 100 to 240 V AC, 47 to 63 Hz

Table 2

N4965A-CTR with N4956A-E12 and N4957A-C12 Specifications

Parameter	Specification
Data rate	1.0 to 12.5 Gb/s (timing parameter determined by N4965A controller)
Data line coding	Non-return to zero (NRZ)
Data patterns	2n-1 PRBS patterns (n = 7, 10, 15, 23, 31)
Data input sensitivity	< 0.1 V p-p single-ended
Data threshold adjustment	–1.0 to +1.0 V, 1mV steps
Data delay adjustment	–1000 to +1000 UI, 1 mUI steps (timing parameter determined by N4965A controller)
Autoalign	Set optimum 0/1 threshold and data delay
	Search step size range
Threshold	5 to 20 mV in 1 mV steps
Delay	5 to 20 mUI in 1 mUI steps
BER measurement period	0 to 99,999.999 seconds in 1 msec steps
BER results	Bit error rate, error count, bit count, measurement seconds
Phase margin	> 0.6 UI typical @ 10 Gb/s, 2^{31}-1 PRBS
Data connectors	2.92 mm female
Remote control interface	IEEE-488 (GPIB) or USB2.0
Power requirements	100 to 240 VAC, 50 to 60 Hz, 170 W maximum

Table 3

Physical and environmental

N4965A-CTR with N4956A-E12 and N4957A-C12 Specifications

Temperature, operating	+10 °C to +40 °C
Temperature, non-operating	–40 °C to +70 °C
Dimensions (height, width, and depth)	
N4974A PRBS generator 44 Gb/s	63.5 mm (2.5 in) x 230.2 mm (8 in) x 254 mm (10 in)
N4968A clock and data demultiplexer 44 Gb/s	63.5 mm (2.5 in) x 254 mm (10 in) x 254 mm (10 in)
N4965A-CTR multi-channel BERT controller	100 mm (3.9 in) x 214 mm (8.4 in) x 425 mm (16.7 in)
N4956A-E12 12.5 Gb/s error detector remote head	33 mm (1.3 in) x 72 mm (2.8 in) x 130 mm (5.1 in)
N4957A-C12 clock doubler remote head	33 mm (1.3 in) x 72 mm (2.8 in) x 130 mm (5.1 in)
Mass	
N4974A PRBS generator 40 Gb/s	2.7 kg (6 lbs)
N4968A clock and data demultiplexer 44 Gb/s	3.2 kg (7 lbs)
N4965A-CTR multi-channel BERT controller	3.3 kg (7.1 lbs)
N4956A-E12 12.5 Gb/s error detector remote head	0.38 kg (13.4 oz)
N4957A-C12 clock doubler remote head	0.38 kg (13.4 oz)

Table 4

Regulatory standards

EMC

- CISPR Pub 11 Group 1, Class A
- AS/NZS CISPR 11
- ICES/NMB-001

This ISM device complies with Canadian ICES-001.
Cet appareil ISM est conforme a la norme NMB-001 du Canada.

Ordering information

N4967A serial BERT system 44 Gb/s

Related products

Recommend external clock source for 22-44 Gb/s operation:

- N5183A MXG Analog Signal Generator with options
- N5183A-532 Frequency range 100kHz to 31.8 GHz
- N5183A-1EA High output power

Typical configurations

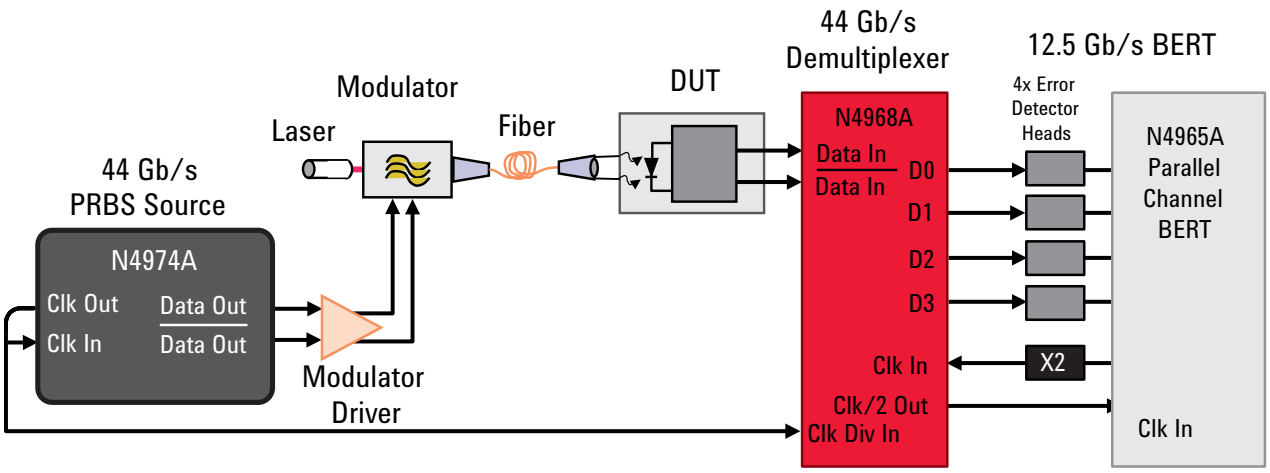


Figure 7. Typical BER test system for 40 Gb/s optical receiver

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