Keysight Technologies
x1149 Boundary Scan Analyzer

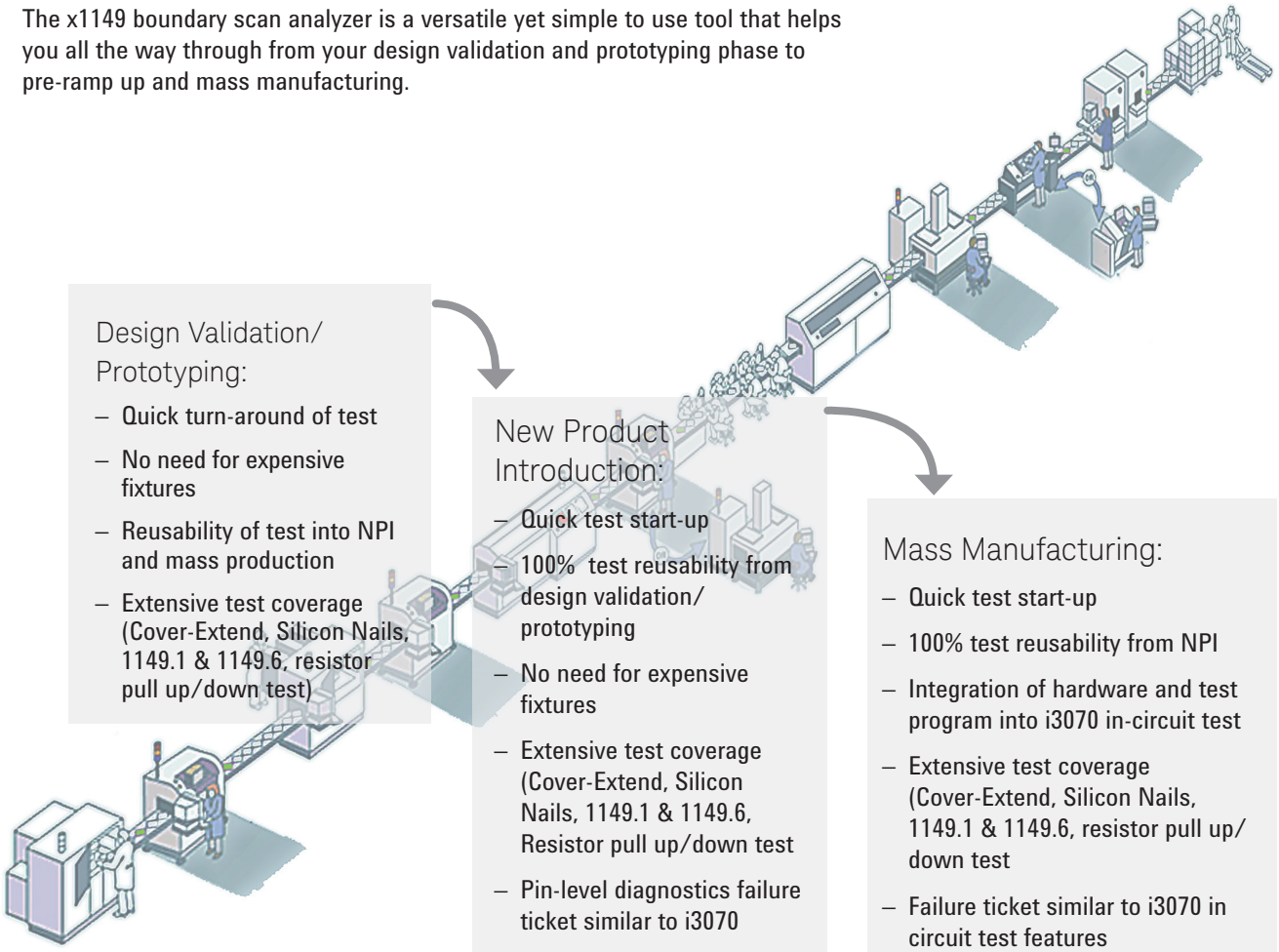
Technical Overview

KEYSIGHT TECHNOLOGIES

Better Coverage, Better Diagnostics, Best-in-Class Usability

Boundary scan has become an indispensable technology as engineers like you face increasing test challenges. Keysight Technologies, Inc. is proud to introduce the new x1149 Boundary Scan Analyzer — bringing the best of our technology and vast test experience — to your workbench!

The x1149 boundary scan analyzer is a versatile yet simple to use tool that helps you all the way through from your design validation and prototyping phase to pre-ramp up and mass manufacturing.



Design Validation/ Prototyping:

- Quick turn-around of test
- No need for expensive fixtures
- Reusability of test into NPI and mass production
- Extensive test coverage (Cover-Extend, Silicon Nails, 1149.1 & 1149.6, resistor pull up/down test)

New Product Introduction:

- Quick test start-up
- 100% test reusability from design validation/ prototyping
- No need for expensive fixtures
- Extensive test coverage (Cover-Extend, Silicon Nails, 1149.1 & 1149.6, Resistor pull up/down test
- Pin-level diagnostics failure ticket similar to i3070

Mass Manufacturing:

- Quick test start-up
- 100% test reusability from NPI
- Integration of hardware and test program into i3070 in-circuit test
- Extensive test coverage (Cover-Extend, Silicon Nails, 1149.1 & 1149.6, resistor pull up/ down test
- Failure ticket similar to i3070 in circuit test features

Key features

- Cover-Extend Technology (coverage on non-scan components)
- In-system programming for CPLD/FPGA
- Integrated scan-path linker
- Actionable pin-level failure reporting
- Built-in remote access via Ethernet
- 22.5 MHz test clock
- 4 dedicated TAP/IO ports

Hardware

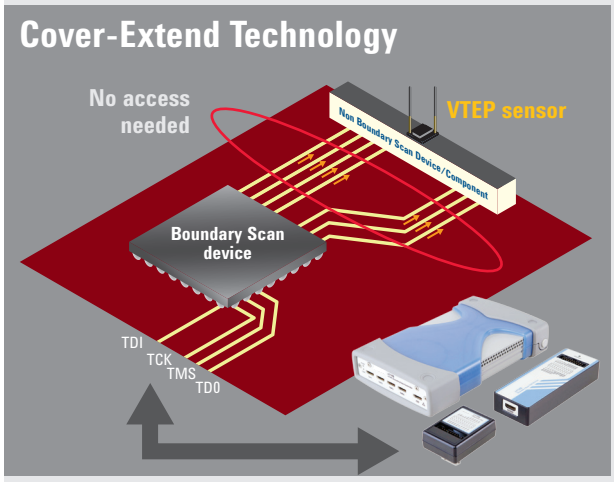
- 4-test access port (TAP) boundary scan controller
- Boundary scan TAP/IO ports
- Self-diagnostic clip
- 12 V power supply
- LAN cable
- USB cable
- HDMI cable with filter
- Ribbon cable 20-pin female-to-female
- CET module (accessory)

Better Coverage

Cover-Extend Technology (CET)

x1149 is the only bench top solution in the market that offers Cover-Extend Technology (CET). CET is a patented and award-winning* innovation that combines boundary scan and capacitive-coupled sensing technology. (See inset on how it works.)

- Provides easy coverage
- Extends coverage for non-scan components
- No extra cost working with digital plug-in modules for connectors
- No hassle writing libraries
- Based upon Vectorless Test Extended Performance (VTEP), an industry-proven technology
- Auto-debug



How does it work?

1. The VTEP sensor, which is able to capacitively pick up electrical signals, is placed on the component to be tested (e.g. a connector).
2. By controlling the test access port, users can control the boundary scan device to drive out stimulus signals.
3. The stimulus signal is delivered to the connector where the VTEP sensor is.
4. A defect (e.g. an open) in the path between the boundary scan device and the VTEP sensor will affect the stimulus signal that is bound for the sensor.
5. The result is captured and diagnosed by the x1149 Boundary Scan Analyzer and thus, the defect is detected!

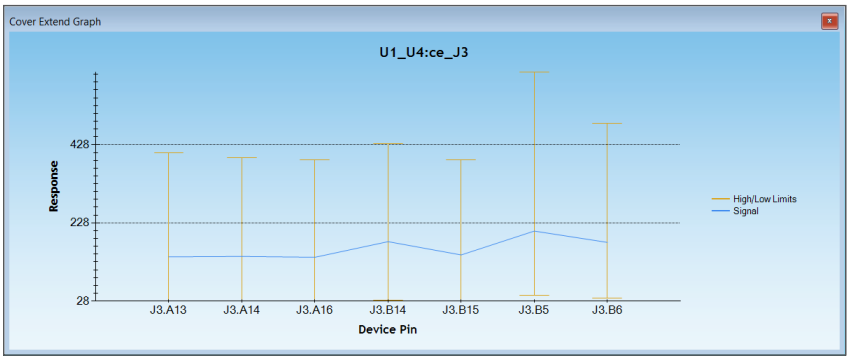
* *Winner of TMW Best In Test 2009, Circuit Assembly NPI 2009, SMT Vision 2009, EMAsia Innovation 2009, SMT China Vision 2009, EDN Innovation 2008, IPC Innovative Technology Center Award 2008.*

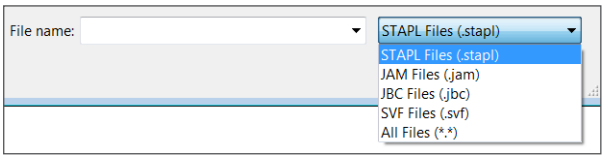
Better Coverage

In-System Programmer

Programming CPLDs and FPGAs has never been easier. With a built-in Standard Test And Programming Language (STAPL) player, programming these devices is as a simple as executing a file.

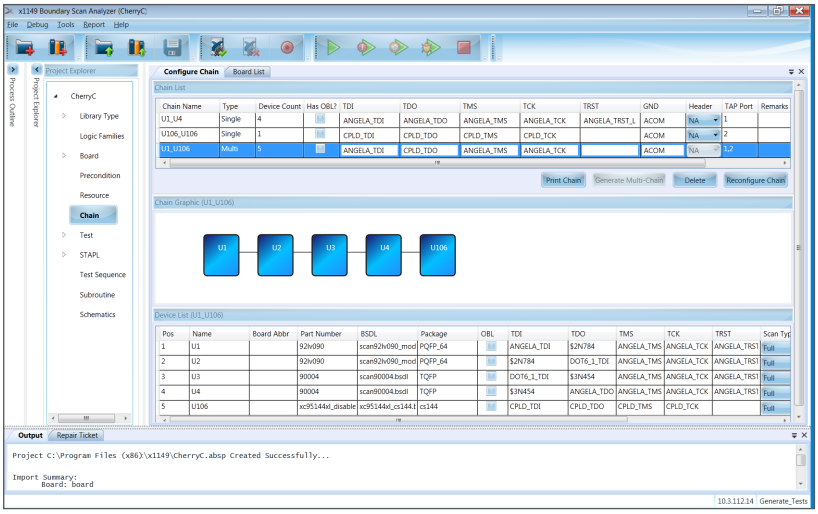
The software accepts any of these file formats: STAPL, SVF, JAM and JBC which it takes and executes using the built-in engine. You can change the files as you go, making the implementation of In-system Programming simple while leveraging upon your efforts upstream.





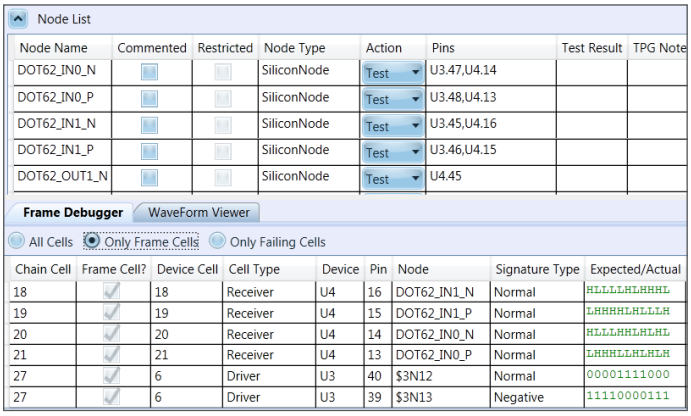
Integrated Scan Path Linker

With your integrated scan path linker, you have the power to maximize test coverage on interconnect nodes between scan chains by linking them into one; test coverage that you won't otherwise have if the chains were treated separately. During your debug, you may decide to keep the chains separate and break up a linked-up chain – the flexibility is yours!



IEEE 1149.6

Cover today's high speed digital networks such as AC-coupled differential lines. Your x1149 unit already comes with support for the IEEE 1149.6 standard.



Node List

Node Name	Commented	Restricted	Node Type	Action	Pins	Test Result	TPG Note
DOT62_IN0_N			SiliconNode	Test	U3.47,U4.14		
DOT62_IN0_P			SiliconNode	Test	U3.48,U4.13		
DOT62_IN1_N			SiliconNode	Test	U3.45,U4.16		
DOT62_IN1_P			SiliconNode	Test	U3.46,U4.15		
DOT62_OUT1_N			SiliconNode	Test	U4.45		

Frame Debugger | WaveForm Viewer

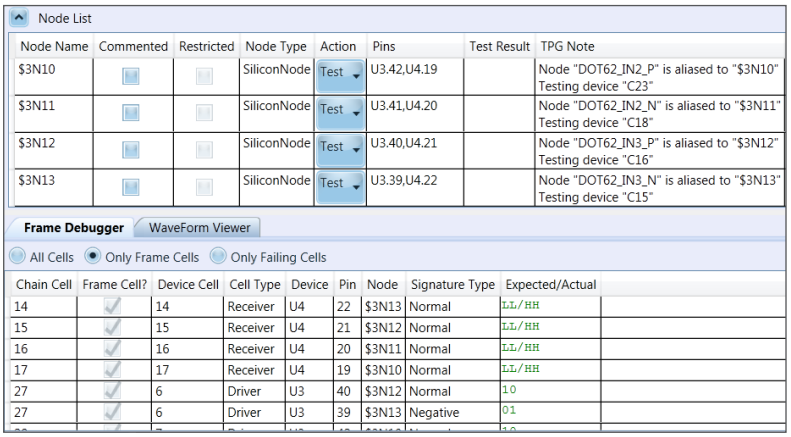
All Cells | Only Frame Cells | Only Failing Cells

Chain Cell	Frame Cell?	Device Cell	Cell Type	Device	Pin	Node	Signature Type	Expected/Actual
18	✓	18	Receiver	U4	16	DOT62_IN1_N	Normal	HLLLLHLHHHL
19	✓	19	Receiver	U4	15	DOT62_IN1_P	Normal	LHHHHLHLLLH
20	✓	20	Receiver	U4	14	DOT62_IN0_N	Normal	HLLLHHLHLHL
21	✓	21	Receiver	U4	13	DOT62_IN0_P	Normal	LHHHLLHLHLH
27	✓	6	Driver	U3	40	$3N12	Normal	00001111000
27	✓	6	Driver	U3	39	$3N13	Negative	11110000111

Better Coverage

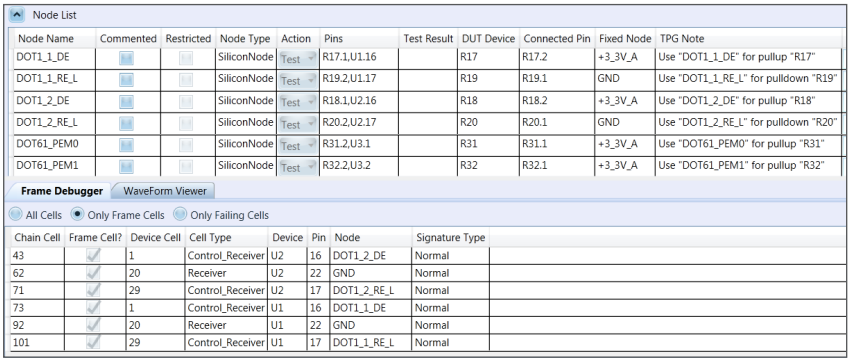
Shorted Capacitors

With the implementation of IEEE 1149.6 on advanced digital networks, you have the additional coverage on shorted coupling capacitors. The test effectiveness depends on the ability to properly manage the timing of state changes in relation to the time constant of the AC-coupled capacitor. All this is done automatically for you in the background.



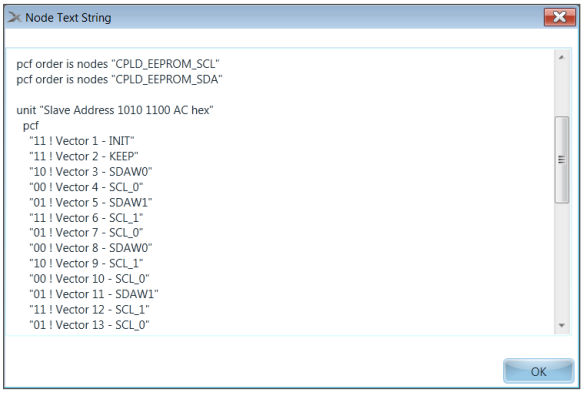
Pull-up/Pull-down Resistors

Modern board designs are peppered with either pull-up resistors or pull-down ones for purposes of termination, voltage divide, logic tie, etc. x1149 gives users coverage on these components as a default feature using the network of boundary scan cells to determine their presence.



Silicon Nails

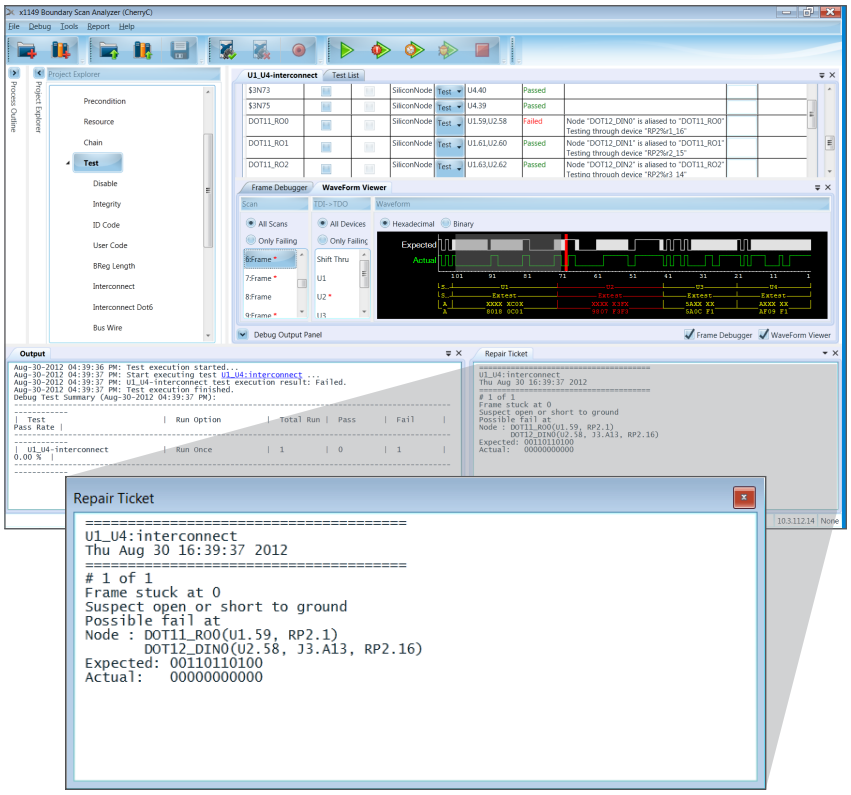
Got non-boundary-scan devices? No problem. Silicon nails test, or sometimes called cluster test, uses the boundary scan cells in the scan chain as drivers and/or receivers to stimulate non-boundary scan devices which may include memory devices. Silicon nails increases your test coverage as you are no longer confined to just IEEE 1149.x compliant devices.



Better Diagnostics

Actionable Failure Report

Failure reports enable corrective actions. The x1149 produces actionable pin-level failure reports that highlights defect locations that can be understood by everyone – encouraging faster resolution and reduces miscommunication especially when dealing across geographies.



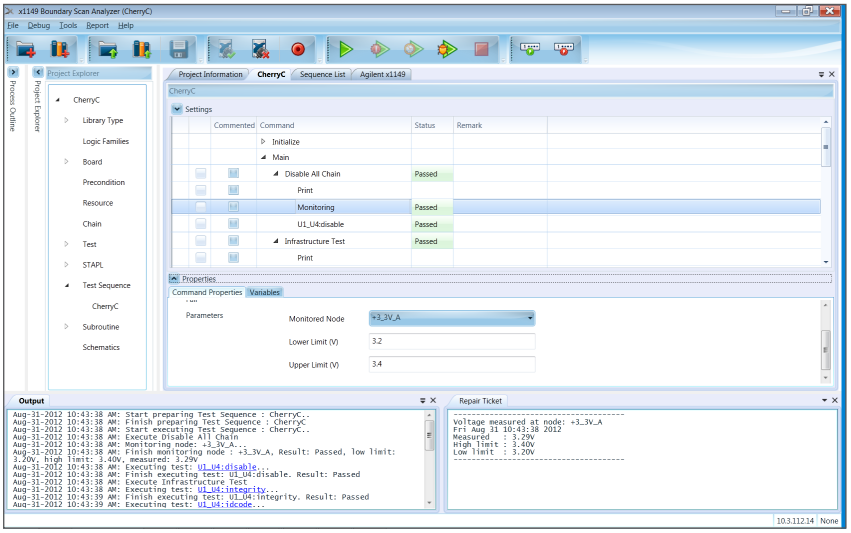
Buswire Test

Board defects that are detected can either originate from the driving or receiving end of a net or both.

Buswire test ensures that nets that have bidirectional boundary scan cells are exercised both ways to give better diagnostic resolution to detected defects.

Voltage Monitoring

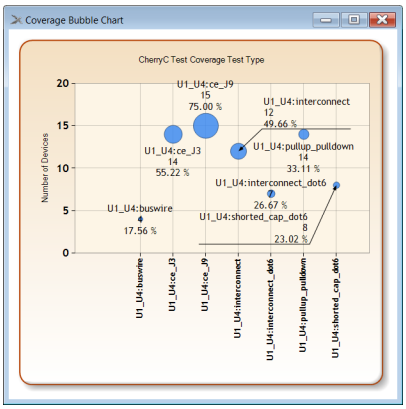
Ability to monitor voltages is critical not only as a debug tool but as a foundation of subsequent structural tests. It gives you control and ensures lines that are supposed to be held continue to do so even in between tests. This avoids false impressions of failures that could be due to improper power rather than defective parts.

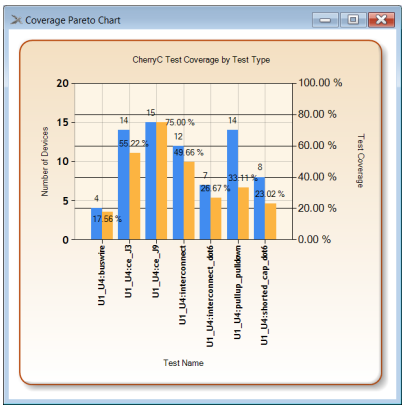


Better Diagnostics

Coverage Report

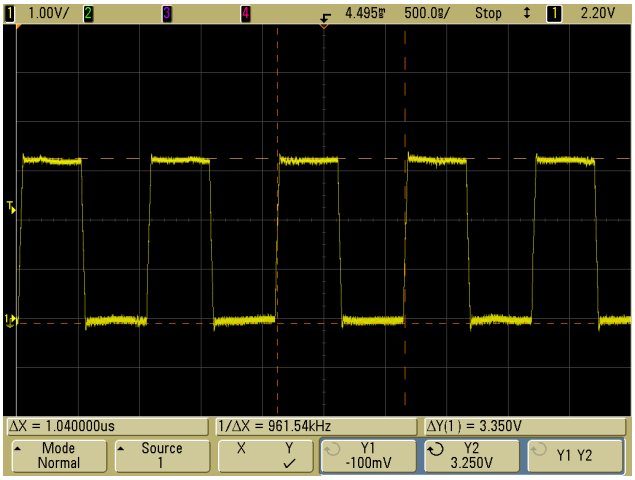
Test coverage report tells you how effective your tests are and how much test coverage you are getting before you commit your board design to volume production.



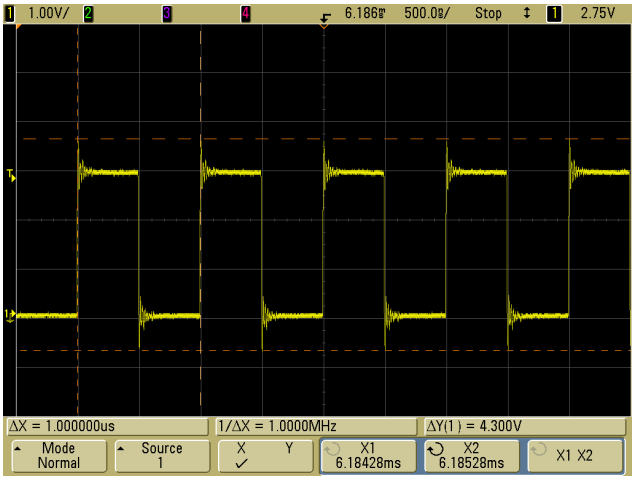


Superior Signal Quality

Signal quality is increasingly important as logic levels trend lower. To prevent unintended state transitions leading to false calls, you need to have better control of your I/Os and have them respond to the way you want them to.



Keysight x1149 Boundary Scan Analyzer



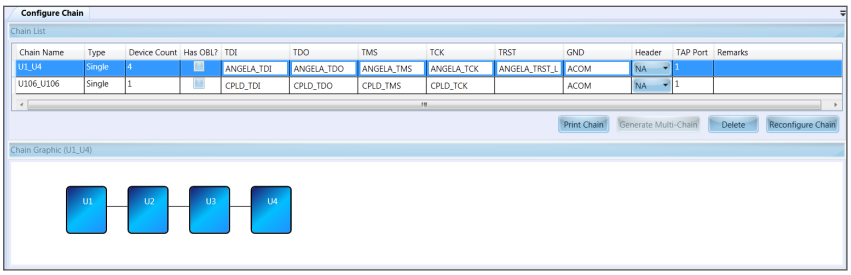
Competitor PC scan

Best-in-Class Usability

Best-in-class User Interface

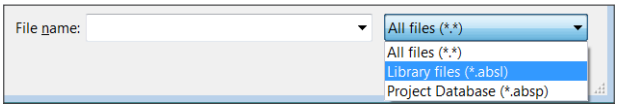
More than ever before, usability plays a critical role in the effectiveness of the tools we use. User interfaces have to be intuitive and help to intelligently assist you with your tasks. x1149 presents a user interface (UI) that is best in class.

Automatic Scan Chain Detector



One of the key tasks when working with boundary scan is validating the scan chain. The UI comes with the ability to identify the potential scan chain! This is powerful especially for complex and long chains. The software is able to analyze the board topology, even taking into consideration components between boundary scan devices to present to you how the scan chain looks like.

Get the right BSDL



Another key task is ensuring you have the right Boundary Scan Description Language (BSDL) files. The UI has a built-in BSDL syntax checker and compiler. It is able to automatically look for BSDL files in your depository folder without needing you to explicitly point to it. You can even port over BSDL files from a known good project – just by importing that one project name; and not the dozens of BSDL file names. It is cleaner, easier and saves you time.

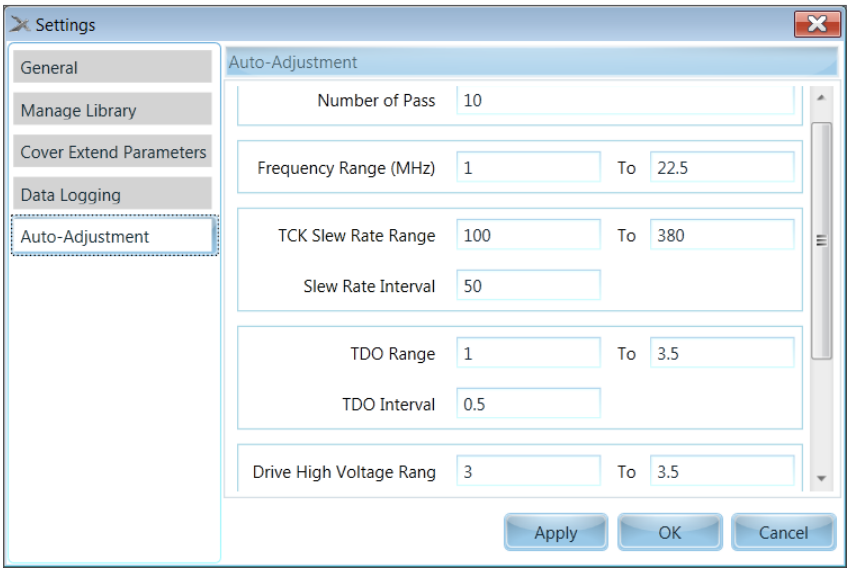
Best-in-Class Usability

Best-in-class User Interface

Debug Tools

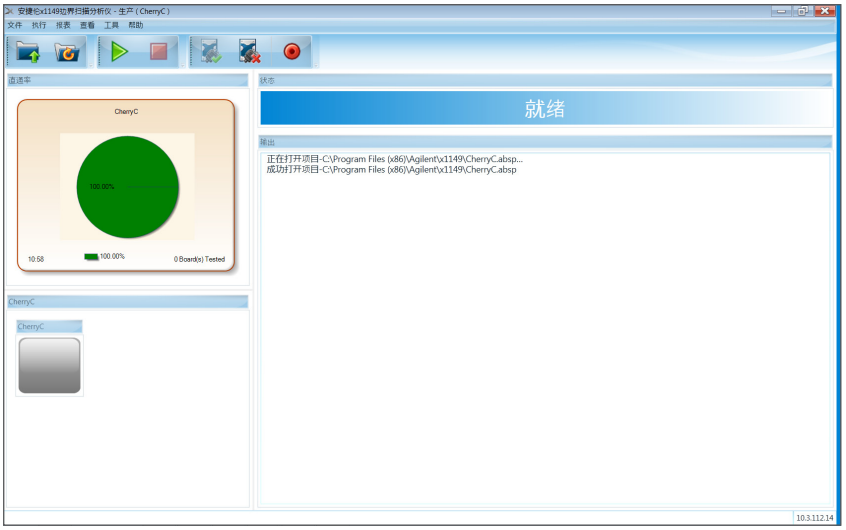
You have a number of debug tools at your disposal. There is the Auto-Adjust that helps you *automatically* tweak various parameters like the slew rates, TCK speed, voltage offsets for TDI/TDO, etc. to find the optimum setting for your UUT. The Frame Debugger lets you do a deep dive debug if you want to analyze frame by frame. The Cover-Extend Test (CET) auto debug tool helps to automatically set the thresholds while maintaining the level of test quality (i.e. Cpk) that you want.

Other examples include a BOM parser, waveform viewer and other efficiency features like ability to do side-by-side code comparison, filtering of node names to ease viewing and selection and much more.



Language Localization

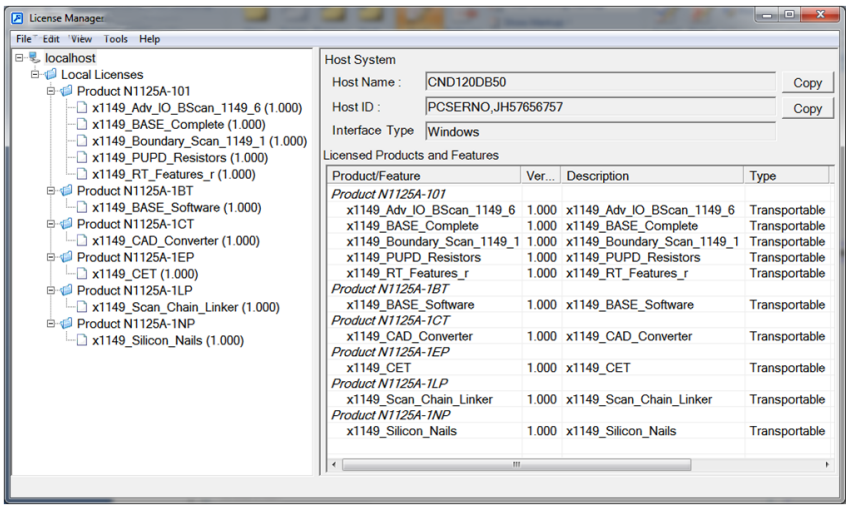
The standard English user interface comes with a Simplified Chinese option. With our translation matrix, additional languages can be added. As your operations span the globe, having local language support eases your daily tasks.



Best-in-Class Usability

Transportable license

Want to maximize your investment? Our software licenses allow trans-portability – without needing you to set up a license server – so you can share your licenses within your team. Unlike a hardware dongle, you can share licenses across buildings and even across countries – easily! Think of it as a soft-dongle.



Centralized Power Supply Control

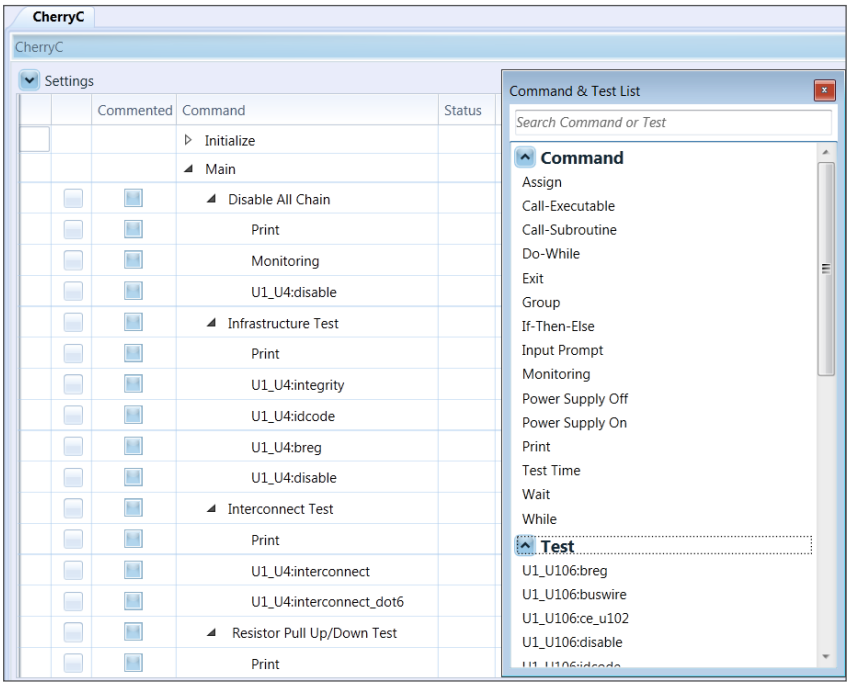
Do you manually flip the switch of your power supply every time you run your boundary scan tests? With the bundled Keysight I/O library, x1149 allows you to control your power supply through the use of Standard Commands for Programmable Instruments (SCPI) standard from your User Interface!

Furthermore, it enables you to insert the power-up/power-down sequence as part of your test execution.

Best-in-Class Usability

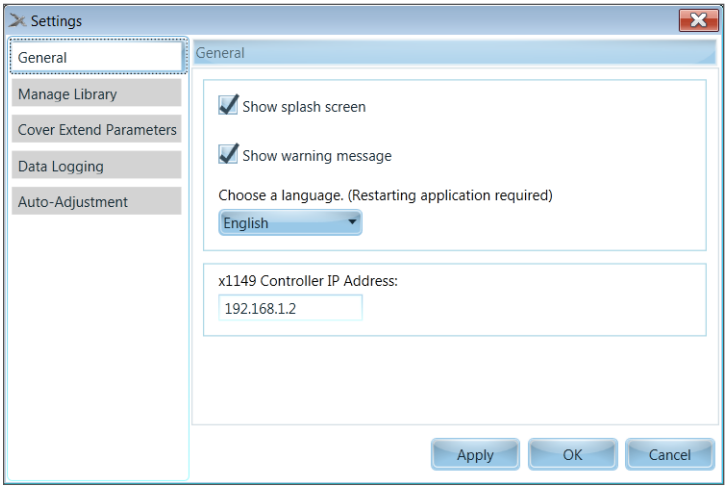
Test Sequencer

Having control of your test execution goes beyond just rearranging the order of tests that you want to run. Today, engineers need the ability to insert decision-making branches and subroutines in addition to the usual prompts and wait times. The x1149 test sequence gives engineers more power over how they want the test execution to progress.



Remote Access to Controller

Work from your desk while your x1149 controller sits in the lab – or even miles away. With the built-in Ethernet connection, control is just one IP address away. Unlike remote desktop control, you do not need any additional host PC or other additional hardware – instead you just connect directly to your controller.



Dedicated TAP/IO Ports

With dedicated hardware for the Test Access Port and Digital Inputs/ Outputs (TAP/IO Port), you can bring the parts that matter closer to your Unit-Under-Test (UUT) to ensure maximum signal integrity. The ports are small enough to fit into tight spots in fixtures if needed.

The best experience is a personal experience. Contact Keysight to learn more about how you can make the x1149 work for you today!

Feature	COMPLETE Bundle	RUNTIME Bundle
Test Development for :		
Infrastructure test : Scan path integrity	√	
Infrastructure test : IDCODE	√	
Infrastructure test : USERCODE	√	
Infrastructure test : BREG	√	
Infrastructure test : DISABLE	√	
Interconnect test : IEEE 1149.1	√	
Buswire test : IEEE 1149.1	√	
Interconnect test : IEEE 1149.6	√	
Buswire test : IEEE 1149.6	√	
IEEE 1149.6 shorted capacitor test	√	
Pull-Up/Pull-Down resistors test	√	
Scan path linker	√	
Cover-Extend Technology (CET) test	√	
CPLD/FPGA in-system programming	√	
Silicon Nails test (e.g. memory test)	√	
Voltage monitoring	√	
Power supply control via SCPI	√	
Transportable licenses	√	
CAD Translator – Full access to all formats (including i3070 board file)	√	
BOM parser	√	
Auto scan chain detection and visualization	√	
Automatic test generation	√	
Test sequence creation	√	
Debug tools (Auto Adjust, Frame Debugger, Waveform Viewer, CET auto debug)	√	
Auto threshold setting – CET test	√	
User-defined source code insertion	√	
Intra-test logic level change	√	
Test coverage report	√	
Fixture info generation	√	
Test execution (all tests)	√	√
Production tools (first pass yield, utilization report, alarms)	√	√
Self-diagnostic clip and test	√	√
Language localization	√	√
Built-in remote access via Ethernet	√	√
Remote firmware upgrade	√	√
Pin-level failure reporting	√	√
2-year software support	√	√
2-year hardware support	√	√

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Three-Year Warranty

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Keysight's commitment to superior product quality and lower total cost of ownership. The only test and measurement company with three-year warranty standard on all instruments, worldwide.

Keysight Assurance Plans

www.keysight.com/find/AssurancePlans
Up to five years of protection and no budgetary surprises to ensure your instruments are operating to specification so you can rely on accurate measurements.

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