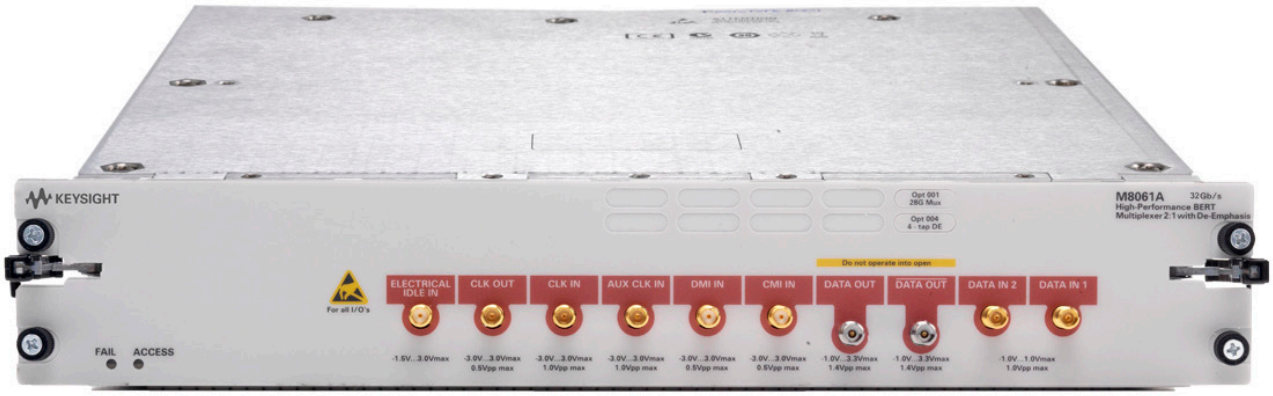
Keysight Technologies
M8061A 32 Gb/s Multiplexer with De-Emphasis

Data Sheet
Version 1.5



KEYSIGHT TECHNOLOGIES

Key features

- Extension for J-BERT M8020A for data rates up to 32 Gb/s
- Expands data rate of J-BERT N4903B pattern generator up to 28.4 Gb/s
- Integrated and calibrated 4-tap de-emphasis, expandable to 8 taps
- Internal superposition of interference for common-mode and differential mode
- Transparent to jitter generated by J-BERT, Clock/2 jitter can be added
- Electrical idle
- Control from J-BERT M8020A and N4903B user interface via USB

Description

R&D and test engineers who need to characterize serial interfaces of up to 32 Gb/s can use the M8061A 2:1 Multiplexer with optional de-emphasis to extend the rate of J-BERT M8020A and J-BERT N4903B pattern generator. For the most accurate receiver characterization results, the M8061A provides four calibrated de-emphasis taps, which can be extended to eight taps, built-in superposition of level interference and Clock/2 jitter injection. The N4877A 32G CDR and de-multiplexer can be used to complement the setup for the analyzer side. The M8061A is a 2-slot AXIe module that can be controlled via USB from the user interfaces of J-BERT M8020A as well as J-BERT N4903B.

Typical applications that require testing at data rates up to 32 Gb/s are:

- Optical transceiver such as 100GBASE-LR4, -SR4 and -ER4, 32G Fibre Channel
- SERDES and chip-to-chip interfaces, such as OIF CEI
- Backplanes, cables, repeaters, such as 100GBASE-KR4
- Thunderbolt 20G and active optical cables

32 Gb/s BERT setup with J-BERT M8020A and M8061A

To characterize receivers that operate up to 32 Gb/s, the M8061A multiplexer can be used with J-BERT M8020A and N4877A as a 32 Gb/s high-performance BERT. It provides excellent intrinsic jitter performance, integrated and calibrated jitter injection capabilities to stress receivers under test, 4/8-tap de-emphasis to emulate transmitter de-emphasis and to compensate for losses in the channel and a tunable CDR to enable full sampling BER and jitter tolerance measurements up to 32 Gb/s. A powerful pattern sequencer allows generating algorithmic PRBS as well as memory pattern sequences. Up to two 32 Gb/s channels can be configured for crosstalk testing and PAM-4 pattern generation.

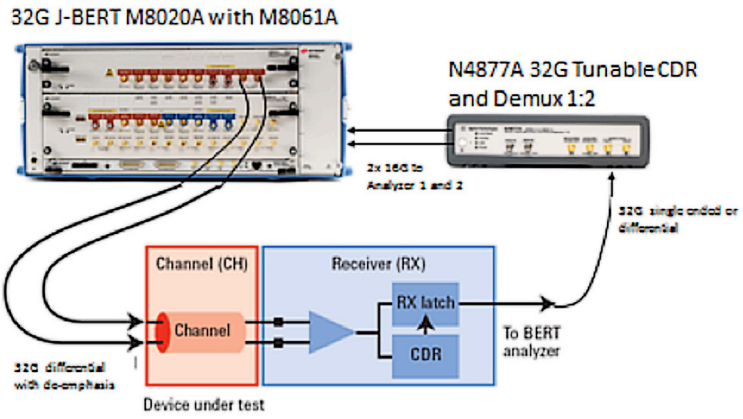


Figure 1: The 32 Gb/s high-performance BERT configuration is based on J-BERT M8020A, M8061A and N4877A. Its perfectly suited to characterize receiver tolerance up to 32 Gb/s. It provides integrated jitter injection up to 1 UI for HF jitter and hundreds of UIs for LF jitter, 8-tap de-emphasis and tunable CDR capability for BER analysis and jitter tolerance testing. All parameters can be controlled from a common user interface.

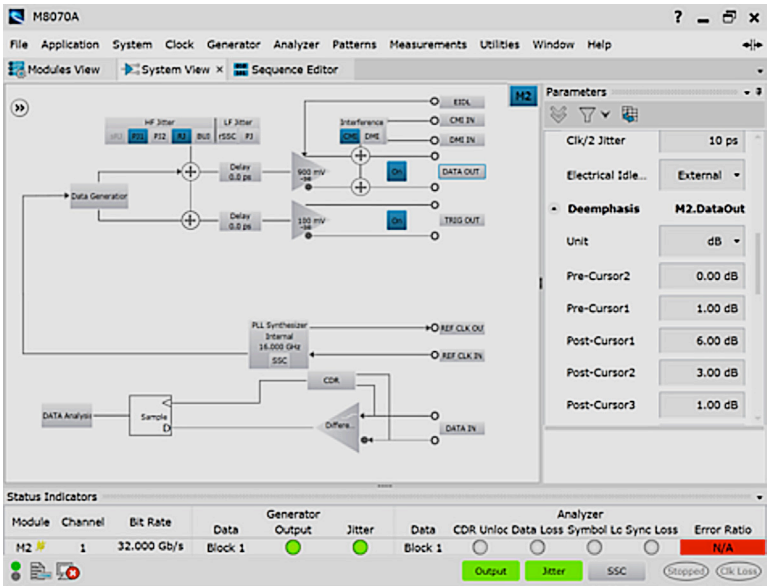


Figure 2: The 32G J-BERT M8020A configuration can be controlled from the M8070A system software. It allows adjusting all parameters of M8061A, M8020A and N4877A from one common user interface. The system view on the left side shows the block diagram of the 32G BERT with its synthesizer, pattern generation, jitter sources, interference, de-emphasis, output amplifier, the analyzer and CDR. At the right side you can adjust all related parameters.

Extend the data rate of J-BERT N4903B up to 28.4 Gb/s

The M8061A multiplexer can be used to extend the data rate of the J-BERT N4903B pattern generator to 28.4 Gb/s as shown below. All jitter injection capabilities of J-BERT N4903B are available also with M8061A as it is transparent to the jitter from N4903B. When clean signals are required, it can operate with a clean clock source to further lower its intrinsic jitter. A USB connection between J-BERT N4903B and M8061A allows controlling all parameters of the M8061A via the user interface of J-BERT N4903B.

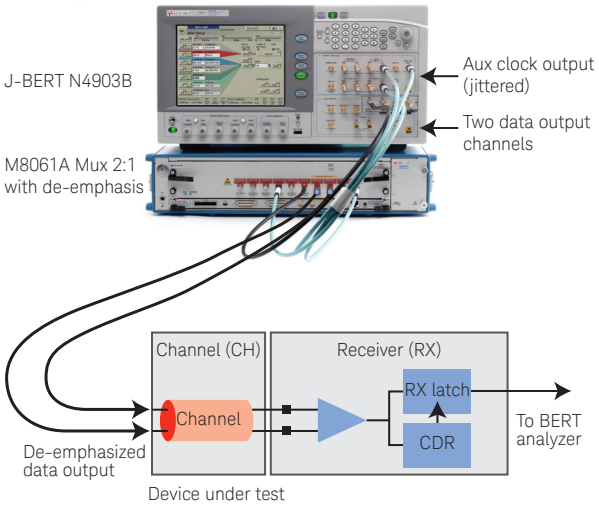


Figure 3. This setup shows how to emulate transmitter de-emphasis up to 28.4 Gb/s with M8061A and J-BERT N4903B.

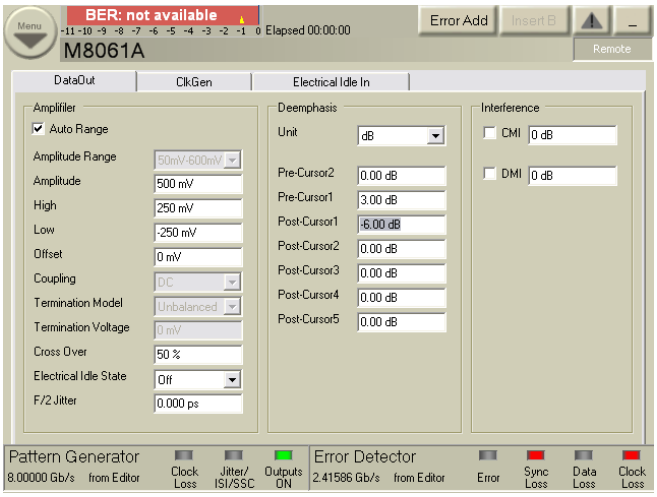


Figure 4. Users can control all M8061A parameters via the J-BERT N4903B GUI and remote control interface. M8061A is connected via USB 2.0 to J-BERT.

Emulate transmitter de-emphasis with up to 8 taps

Many multi gigabit serial interfaces use transmitter de-emphasis to compensate for electrical signal degradations caused by printed circuit boards or cables between the transmitter and the receiver ports. R&D and test engineers who need to characterize receiver ports under realistic and worst case conditions require a pattern generator that allows to accurately emulate transmitter de-emphasis with adjustable multi-tap de-emphasis levels.

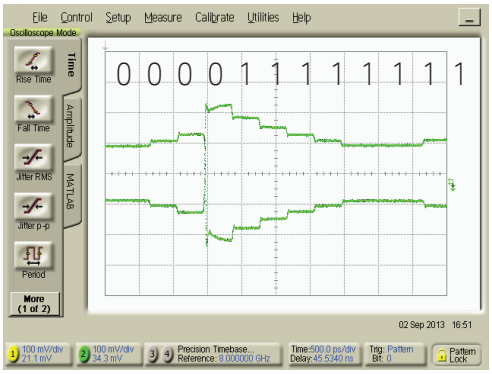


Figure 5. Emulate 8-tap de-emphasis signals with M8061A for data rates up to 32 Gb/s. The example shows a pattern with eight consecutive “0”s and eight “1”s with a 8 tap de-emphasis setting: 2 pre-cursors and 5 post cursors (the 8th tap is the main cursor).

De-embed signal degradations caused by the test set up and fixtures using the de-emphasis

Minimizing the influence of the test environment is a challenge especially if bit rates exceed 20 Gb/s. To de-embed the signal degradations caused by cables, test fixtures, adapters, etc. The de-emphasis technique is commonly used. M8061A is the only instrument that offers up to 8 tap de-emphasis up to 32 Gb/s, allowing compensation of signal degradations in very fine steps.

Emulate channel loss with negative de-emphasis

Channel losses can be emulated by using the negative de-emphasis funcion of the M8061A. See figure 2. The post-cursor taps can be used to emulate channel losses for higher frequencies. As a guideline: with the 5 post-cursor taps of M8061A loss frequencies above f / 5 can be emulated; for example for a data rate of 28 Gb/s, f equals 14 GHz, and f/5 corresponds to 2.8 GHz. See figure 7.

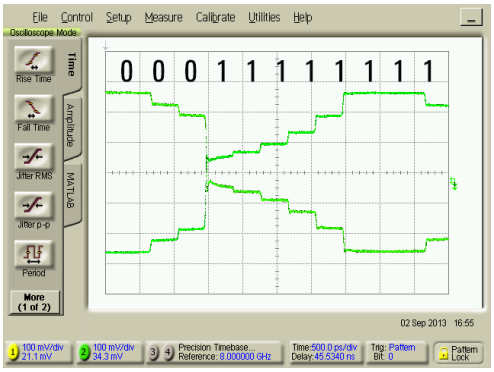


Figure 6. Emulate high-frequency channel losses by using M8061A‘s with inverted de-emphasis taps. The differential signal shows a pattern of eight 0‘s and eight 1‘s. Pre-cursor 2+1: -1.5 dB. Post-cursor 1,2,3,4,5: +1.5 dB.

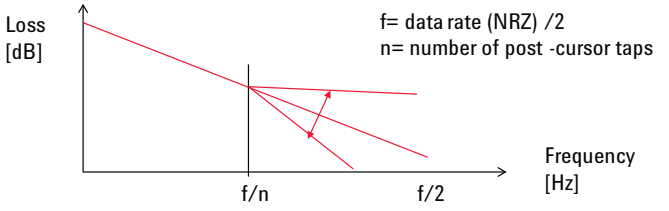


Figure 7. Emulate high-frequency channel losses by using the negative de-emphasis capability of M8061A.

Accurately characterize receivers up to 32 Gb/s

Many SERDES, backplane, cables and optical receivers operate at data rates of 25 Gb/s and beyond. To characterize the receiver tolerance against jitter, cross-talk, level interference, and voltage sensitivity the M8061A can be used as 2:1 multiplexer to extend the pattern generator data rate of the J-BERT M8020A up to 32 Gb/s and J-BERT N4903B up to 28.4 Gb/s. But it can also be used to provide calibrated jitter, because it is transparent to the calibrated jitter from J-BERT and offers additional Clock/2 jitter injection. Built-in interference superposition (common-mode and differential mode) eliminates the need for external adders.

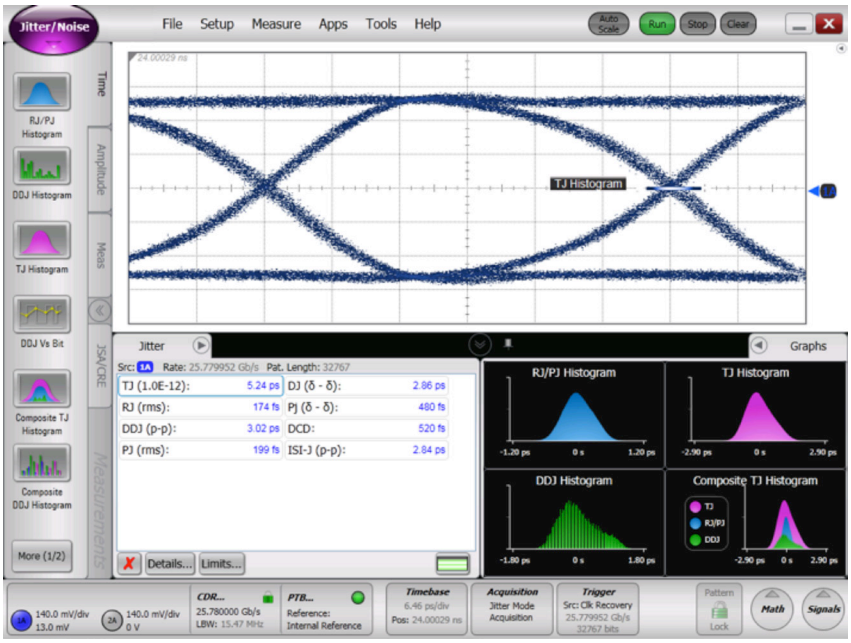


Figure 8. The M8061A shows excellent intrinsic jitter performance. The screen shot is taken at 25.78 Gb/s with 86108B with HBW and PTB options using the M8041A as clock source with the band pass filter M8061A-802 at the aux clock input of M8061A.

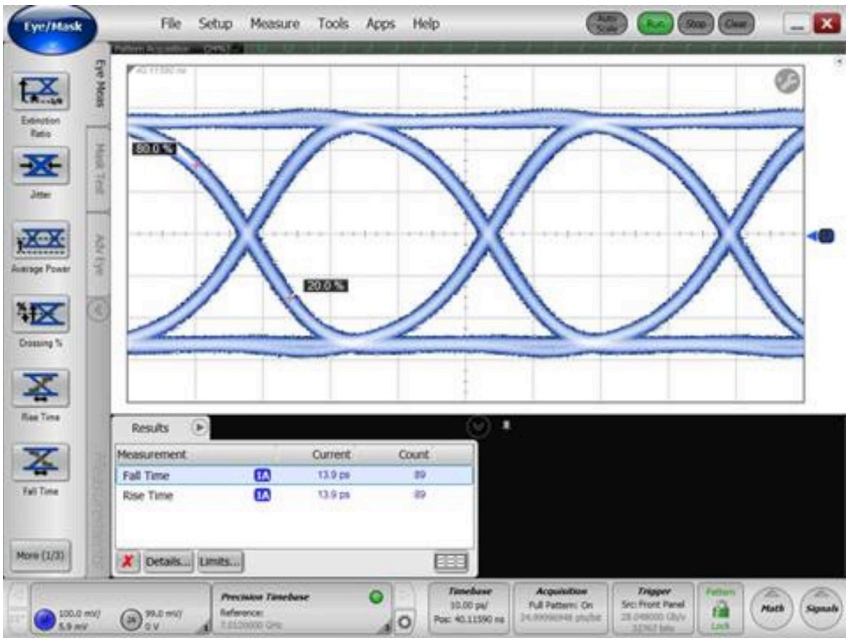


Figure 9. Output signal of M8061A at 28 Gb/s when clocked from M8041A. The transition times are measured with 86118A, at 28 Gb/s, with 500 mV output voltage and de-emphasis turned on.

M8061A Specifications

The specifications below apply for use with J-BERT N4903B and J-BERT M8020A.

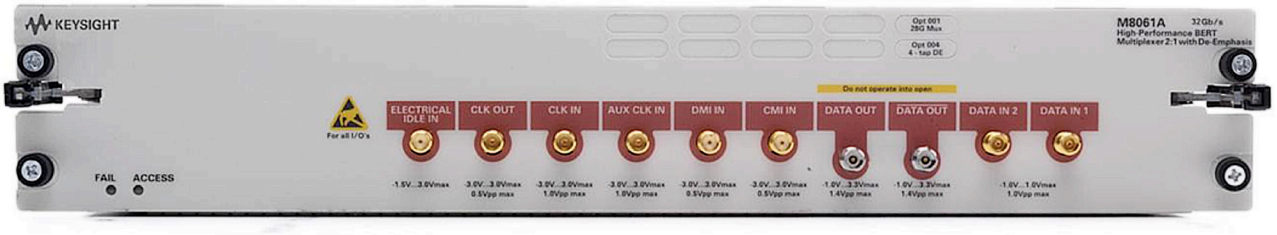


Figure 10. Front panel of M8061A .

Table 1. Specifications for data out

	When used with N4903B	When used with M8020A
Output data rate	300 Mb/s to 27.0 Gb/s (28.4 Gb/s when using J-BERT N4903B option D14)	512 Mb/s to 32.0 Gb/s, over-programming up to 32.4 Gb/s For M8061As with a S/N below DE53800200 or a front panel showing 28 Gb/s all specifications are valid up to 28.4 Gb/s with over-programming up to 32.4 Gb/s.
Channels	1	1, can be extended to 2 channels. This requires additional M8051A, M9505A and a second M8061A.
Output format	NRZ	
Output amplitude	0.05 Vpp to 1.200 Vpp, (for single ended operation) 0.1 to 2.4 Vpp for differential operation See table 2 for max. output amplitude if offset is > 1.9 V and CMI/DMI are turned on.	
Resolution	5 mV	1 mV
Output voltage window	–1 V to +3 V	
External termination voltage	–1 V to +3 V For offset > 1.3 V the termination voltage should be ± 0.5 V of offset.	
Transition times	14 ps typical (20% to 80%) for data rates > 25 Gb/s, de-emphasis disabled	
Intrinsic random jitter [1]	200 fs rms typical with external clock from Precision Signal Generator E8257D-520 and clock pattern. When using J-BERT N4903B as clock source, its intrinsic clock jitter applies.	180 fs rms typical @ 25.78 Gb/s with band pass filter M80961A-802 at aux clock input of M8061A 210 fs rms typical @ 25.0 to 32.0 Gb/s with band pass filter M8061A-803 at aux clock input of M8061A 350 fs rms typical @ 28.4 Gb/s clock pattern using M8041A as clock source without band pass filter.
Total jitter	6 ps pp typical @ PRBS 2^{15}-1, at a target BER of 10^{-12}, room temperature [1, 2]	
Peak-peak jitter	6 ps pp typical @ PRBS 2^{31}-1, based on 1000 waveforms captured at 50% crossing point [1, 2]	
Jitter feed-through	Transparent for timing jitter on clock. ISI has to be added after multiplexer. Notice: When controlled from J-BERT N4903B the jitter amplitude values refer to the output of M8061A (2 UI). When used with M8020A the jitter amplitude values in UI refer to the output of M8061A (sum of HF jitter is 1UI max).	
Variable clock/2 jitter	± 0.1 UI or ± 20 ps typical (whatever is less) Notice: This means that first eye can be up to 20 ps longer or shorter than subsequent eye.	
Crossing point	Adjustable 30% to 70% typical	
Electrical idle transition time	4 ns typical + 60 ns ± 10 ns (reaction time from EIDLE input to data outputs starting to go into EIDL state).	
Interface	Differential or single-ended, DC coupled, 50 Ω output impedance	
Connectors	2.4 mm, female	

1. Measured with Oscilloscope with < 50 fs rms intrinsic jitter, such as 86108B with HBW and PTB.
2. Measured at a data rate of 28.4 Gb/s, using the Keysight E8257D-520 as precision clock source.

M8061A Specifications (continued)

Table 2. Data output amplitude maximum in presence of CMI, DMI, offset voltage

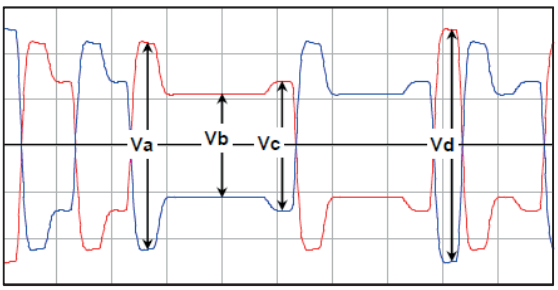
		When used with N4903B and M8020A	
CMI	**DMI**	**offset ≤ 1.9 V**	**offset > 1.9 V**
Disabled	Disabled	1.2 V	0.9 V
Disabled	Enabled	0.9 V	0.675 V
Enabled	Disabled	0.9 V	0.75 V
Enabled	Enabled	0.675 V	0.5625 V
Enabled	Enabled [1]	0.8 V	0.666 V

1. For DMI < 12.5% of amplitude.

Table 3. Specifications for de-emphasis at data out (Option 004 and 008)

	When used with N4903B and M8020A	
	Option 004 (4 taps)	**Option 008 (extension to 8 taps)**
Pre-cursor 2 range		± 6 dB
Pre-cursor 1 range	± 12 dB	
Post-cursor 1 range	± 20 dB	
Post-cursor 2 range	± 12 dB	
Post-cursor 3 range		± 12 dB
Post-cursor 4 range		± 6 dB
Post-cursor 5 range		± 6 dB
Cursor accuracy	± 1.0 dB typical at 8 Gb/s at PCIe 3 presets	n/a
Cursor resolution	0.1 dB	0.1 dB

Footnote: Sum of all cursors may not exceed Vpp max.



Post-cursor 1 = $20\log_{10}$ Vb/Va
Pre-cursor = $20\log_{10}$ Vc/Vb
Vpp nominal = $20\log_{10}$ Vd

Figure 11. Definition of nominal output amplitude and de-emphasis (aligned to N4916B and PCI-SIG PCI Express 3.0 specification).

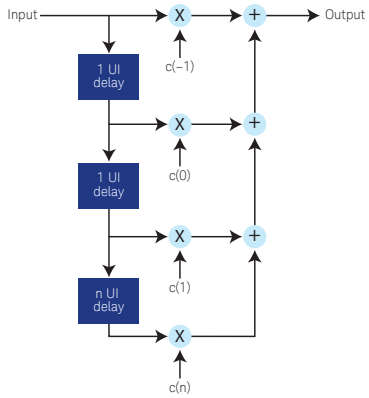


Figure 12. Simplified block diagram for multi-tap FIR (finite pulse respone) circuit.

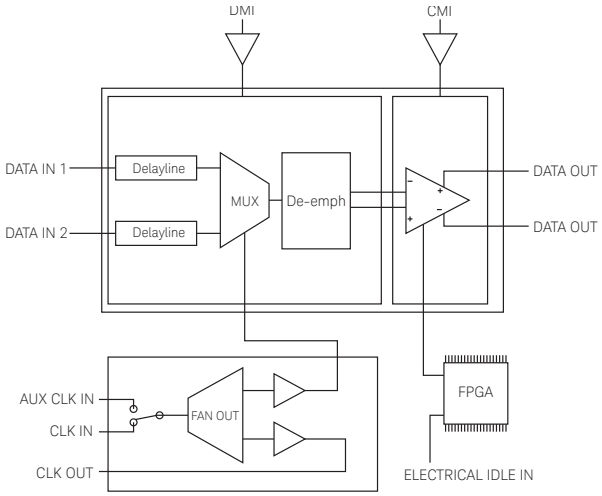


Figure 13. Blockdiagram of M8061A.

M8061A Specifications (continued)

Table 4. Specifications for data in	
	When used with N4903B and M8020A
Input voltage data inputs	500 to 800 mVpp single ended and -70 mV offset (this is automatically set when controlled from J-BERT N4903B)
Input format	NRZ
Interface	Single-ended, 50 Ω input impedance
Connectors	3.5 mm, female

Table 5. Specifications for clock out, aux clock in and clock in		
	When used with N4903B	**When used with M8020A**
Frequency range	150 MHz to 14.2 GHz	256 MHz -16.2 GHz (data rate / 2)
Input format	RZ, full rate	
Input voltage clock inputs	0.2 to 1.0 V	
Input clock transition time	< 200 ps	
Amplitude clock output	1 Vpp typical, single ended	
Interface	AC coupled, 50 Ω nominal	
Connector	3.5 mm, female	
CLK IN	For clean clock input from PSG	
AUX CLK IN	For jittered clock from N4903B AUX CLK output	For jittered clock from M8041A CLK output

Table 6. Specifications for CMI in, DMI in, electrical idle in		
	When used with N4903B / M8020A. M8020A needs external source for CMI/DMI but the combiners and adjustable gain are built-into M8061A.	
	Differential mode interference (DMI)	**Common mode interference (CMI)**
Input voltage	Nominal: 400 mV single ended	
Modulation bandwidth	10 MHz to 6 GHz	10 MHz to 1 GHz
Modulation amplitude	0% to 30% of output amplitude corresponds to gain range of 0 to 1	0 to 400 mV
EIDL input threshold voltage range	–1 to +3 V	
EIDL input termination voltage	–1 to +3 V	
Connectors	SMA	

M8061A Specifications (continued)

Table 7. General characteristics

	When used with N4903B	When used with M8020A
Operating temperature	5 °C to 35 °C (–23 to + 95 °F)	
Storage temperature	–40 °C to +70 °C (module) (–65 to + 158 °F)	
Operating humidity	15% to 95% relative humidity at 35 °C (non-condensing)	
Storage humidity	90% to 24% relative humidity at 65 °C (non-condensing)	
Power requirements (module only)	80 W	
Physical dimensions (W x H x D)	2-slot AXIe module:351 x 61 x 315 mm (13.8 x 2.4 x 12.4 in) Installed in 2-slot AXIe chassis:463 x 105 x 428 mm (18.2 x 4.1 x 16.9 in)	
Weight net	Module:4.1 kg (9.0 lb) Installed in 2-slot-AXIe chassis:11.8 kg (26.0 lb)	
Weight shipping	Module:7.1 kg (15.7 lb) Installed in 2-slot-AXIe chassis:> 38 kg (> 83.8 lb), palletized	
AXIe chassis	2-slot: M9502A-U20, 5-slot: M9505A-U20	5-slot: M9505A-U20. One 32G channel: The M8061A has to be in the same chassis as M8041A. Two 32G channels: Two M9505A-U20s are required. The M8041A and M8051A in one chassis, the two M8061As in a second chassis.
Recommended recalibration period	1 year	
Warranty period	3 years return to Keysight	
Warm-up time	30 minutes	
Cooling requirements	Slot airflow direction is from right to left. To ensure adequate cooling and ventilation, leave a gap of at least 50 mm (2 “) around vent holes on both sides of the chassis. See also Start-up guide for M9502A chassis.	
EMC	IEC 61326-1	
Safety	IEC 61010-1	
Quality management	ISO 9001, 14001	

Table 8. Remote control interface

	When used with N4903B	When used with M8020A
Interface to controlling PC	USB 2.0 mini (requires AXIe chassis with USB option, e.g. M9502A-U20 or M9505A-U20)	USB 2.0 (requires AXIe chassis with USB option, e.g. M9505A-U20), For two 32G channels: external PC with two USB interfaces to two AXIe chassis.
Remote Control	See N4903B Data Sheet GPIB, LAN, USB2.0	LAN
Programming language	SCPI	
Software pre requisites	Requires N4903B SW rev 7.50 or later	Requires M8070A rev 1.5.0.0 or later. See pre-requisites for M8020A.
Download latest software	For J-BERT N4903B: www.keysight.com/find/n4903	For J-BERT M8020A: www.keysight.com/find/m8070a

Specification assumptions

The specifications in this document describe the instruments warranted performance when used with J-BERT M8020A or N4903B. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50 Ω to GND. All specifications if not otherwise stated are valid using the recommended cable set N4910A (2.4 mm, 24" matched pair).

Related Keysight literature	
J-BERT N4903B High-Performance Serial BERT - Data Sheet	5990-3217EN
J-BERT M8020A High-Performance BERT - Data Sheet	5991-3647EN
N4877A Clock Data Recovery and Demultiplexer 1:2, N1075A Optical Pick-Off/Converter, N1070A Optical Clock Recovery Solution, Data Sheet	5990-9949EN
Error Detection Up to 28.4 Gb/s During Receiver Test with the Keysight J-BERT N4903B Using Under-Sampling Techniques, Application Note	5990-6239EN
M9502A and M9505A 2- and 5-Slot AXIe Chassis, Data Sheet	5990-6584EN
2-Slot and 5-Slot AXIe Chassis M9502A, M9505A, Start-up Guide	M9502-90001
Characterizing and verifying compliance of 100 Gb Ethernet components and systems, Application Note	5992-0019EN

Ordering instructions

The M8061A module includes the following accessories by default: Two 50 Ω terminations, USB cable, getting started guide, commercial calibration report ("UK6"), ESD protection kit. For M8061As with S/N larger than DE53800200 one M8061A-803 band pass filter is included.

For M8061A-BU2 and M8020A-BU2 some additional accessories for the AXIe chassis are provided, such as getting started guide, filler panel.

Multiplexer 2:1 up to 28.4 Gb/s, 2-slot AXIe module	M8061A-001
De-emphasis, 4 calibrated taps	M8061A-004
De-emphasis, extension to 8 taps	M8061A-008
M8061A bundles with AXIe chassis	
Bundle consisting of M9505A-U20 AXIe 5 slot chassis with USB option (requires external PC and M8070A software). Recommended for use with J-BERT M8020A.	M8020A-BU2
Bundle consisting of M9502A-U20 AXIe 2 slot chassis with USB option. Recommended for use with J-BERT N4903B.	M8061A-BU2
Software for M8061A	
For use with J-BERT M8020A the M8070A system software for the M8000 series is required:	
– Transportable, perpetual license	M8070A-0TP
– Network, perpetual license	M8070A-0NP
Note: for use with N4903B the M8061A is controlled from N4903B user interface via USB connection.	
Recommended accessories	
Cable kit for connecting M8061A with J-BERT M8020A, 3 x 3.5 mm, 0.6 m (required)	M8061A-804
Matched cable kit for connecting M8061A with J-BERT N4903B (required)	M8061A-801
Matched cable pair, 2.4 mm (m f) to 2.4 mm (m f) for data outputs	N4910A
Four SMA cables, unmatched	15442A
Band pass filter 11.4 to 15.6 GHz, SMA (for use with M8020A and M8061A in clock path to minimize intrinsic RJ of M8061A for data rate of 25.78 Gb/s)	M8061A-802 [1]
Band pass filter 11.1 to 17.5 GHz, SMA (for use with M8020A and M8061A in clock path to minimize intrinsic RJ of M8061A for data rates from 25.0 to 32.0 Gb/s)	M8061A-803 [1]
6 dB attenuator, 50 GHz (when data outputs is driving into non- 50 Ω inputs and for over-voltage protection, e.g. for some high-performance oscilloscopes)	8490D
DC block, 50 GHz (when data output drives into a single ended, AC coupled input, such as 81490A ref. transmitter)	N9398F
Rack-mount kit for AXIe 2-slot chassis M9502A	Y1225A
5-slot AXIe chassis (alternatively to M8061A-BU2) with USB option	M9505A-U20
Rack-mount kit for AXIe 5-slot chassis M9505A	Y1226A
External USB hub 6:1 with power supply	non-Keysight
Warranty, calibration and productivity services	
Extended 5 year warranty Return-to-Keysight	R1280
Calibration services (3 and 5 years)	R1282
Productivity assistance for N4903B Productivity assistance for M8020A	R1380-N49xx R1380-M80xx

Ordering instructions (continued)

Upgrade options for M8061A (note: upgrades are possible on-site via licenses for M8020A users.)	
Upgrade to de-emphasis, 4 calibrated taps	M8061A-U04
Upgrade to de-emphasis extension to 8 taps	M8061A-U08
Recommended J-BERT M8020A configuration for 1 channel 32 Gb/s BERT	
– J-BERT with 5-slot AXIe chassis, requires external PC with USB connection	M8020A-BU2
– M8000 System Software	M8070A-0TP
– J-BERT 16G Generator Analyzer Clock Module with options for second generator channel, second analyzer channel	M8041A-C16,-0G2,-0A2
– 32G Mux 2:1	M8061A-001
– 32G CDR and Demultiplexer 1:2	N4877A-232
– Accessories: cable triplet for connecting M8061A with M8041A (also for connecting N4877A with M8041A), 2.4 mm matched cable pair for M8061A data outputs	M8061A-804, N4910A
Optional:	
– Advanced jitter sources in M8041A	M8041A-0G3
– De-emphasis 4 tap	M8061A-004
– Extension to 8 tap de-emphasis	M8061A-008
– Optimized intrinsic RJ @25.78 Gb/s with band pass filter Note: De-emphasis on M8041A is not required for operation with M8061A. Equalization and interference sources of M8041A cannot be used for operation with M8061A/ N4877A.	M8061A-802
Recommended J-BERT N4903B configuration for 1 channel 28G BERT configuration	
N4903B with options -C13 (BERT 12.5 G), -002 (second channel), and -D14 (extension PG to 14.2 G).	
Optional: N4903B -J10 (jitter sources), -J20 (interference and ISI).	
Optional: N4877A-232 CDR and Demux 1:2, 32 Gb/s	
Optional: E8257D-520 (Precision Signal Generator 20 GHz as clean clock source)	

[1] below 25 Gb/s a band pass filter is not required. When M8061A is used with N4903B the band pass filters should not be used in the clock path.

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