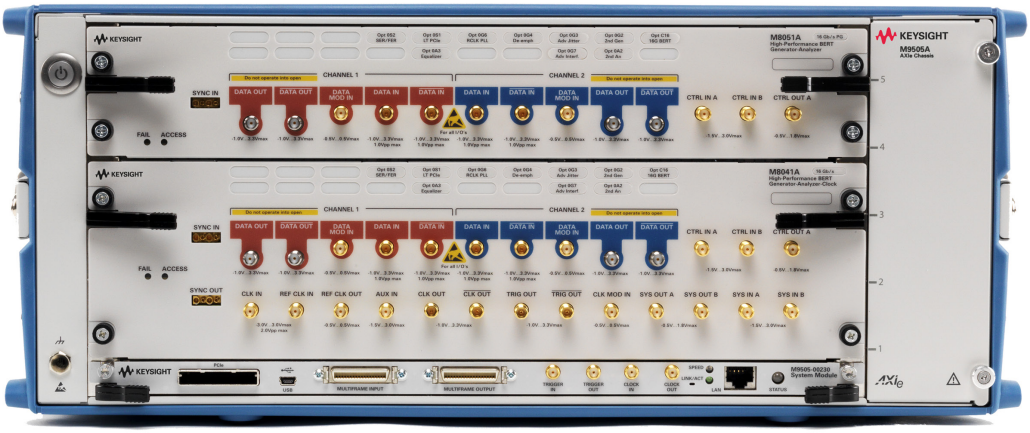
Keysight J-BERT M8020A
High-Performance BERT

Data Sheet
Version 1.5



KEYSIGHT TECHNOLOGIES

Description

The high-performance Keysight Technologies, Inc. J-BERT M8020A enables fast and accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s.

With today's highest level of integration, the M8020A streamlines your test setup. In addition, automated in situ calibration of signal conditions ensures accurate and repeatable measurements. And, through interactive link training, it can behave like your DUT's link partner. All in all, the J-BERT M8020A will accelerate insight into your design.

Key features:

- Data rates up to 8.5 and 16 Gb/s expandable to 32 Gb/s
- 1 to 4 BERT channels in a 5-slot AXIe chassis
- Integrated and calibrated jitter injection: RJ, PJ1, PJ2, SJ, BUJ, sinusoidal level interference (common-mode and differential-mode), SSC (triangular and arbitrary, residual) and Clock/2
- 8 tap de-emphasis, positive and negative
- Interactive link training for PCI Express
- Built-in clock recovery and equalization

M8000 Series of BER Test Solutions

Simplified time-efficient testing is essential when you are developing next-generation computer, consumer, or communication devices.

The Keysight M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing.

With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.

Shift into high gear with the M8000 Series and take the design verification express lane.

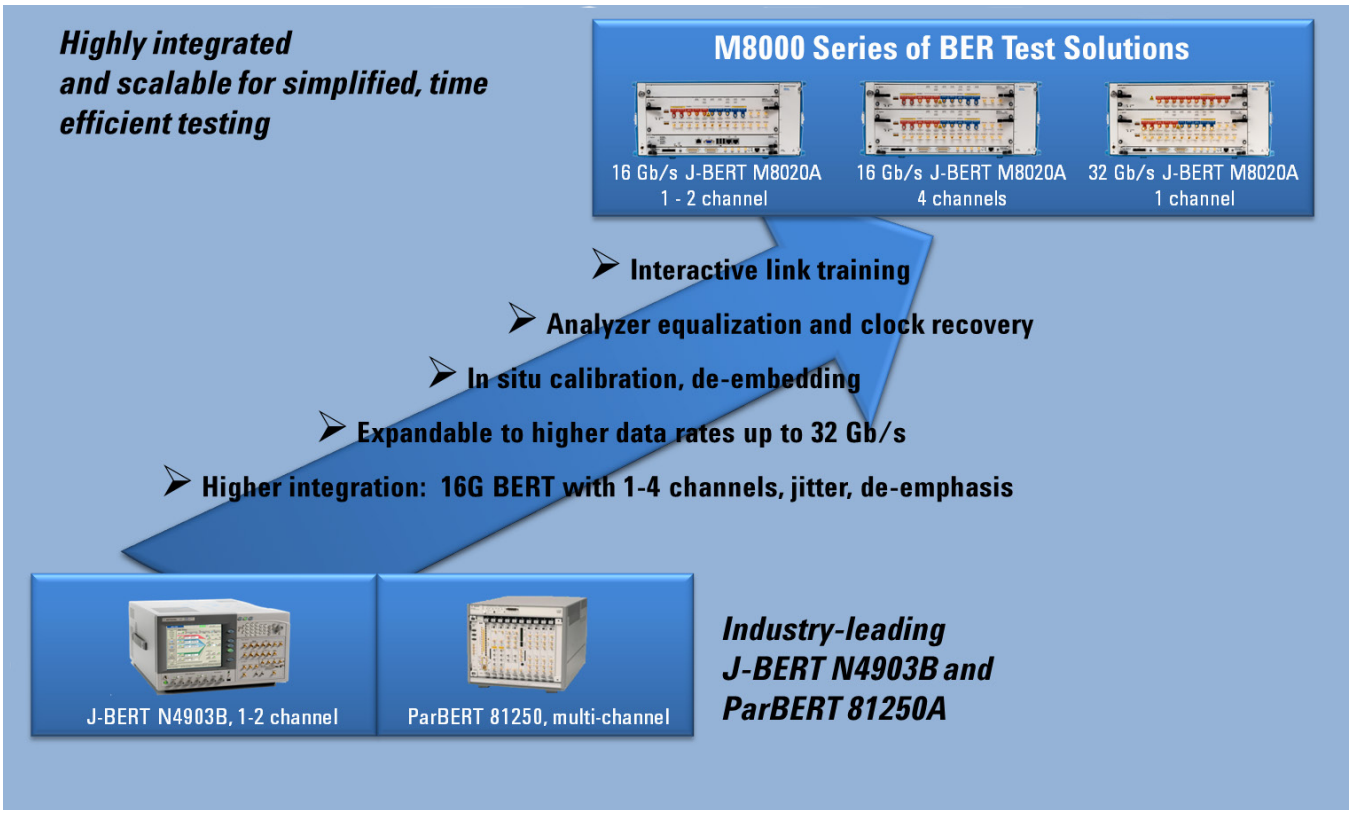


Figure 1. The M8000 Series BER Test Solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.

J-BERT M8020A high-performance BERT

Enabling fast, accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s.

Highest level of integration for streamlined test setups

With J-BERT M8020A all receiver (RX) test capabilities are built-in: jitter sources, "common- and differential-mode level interference, and de-emphasis to emulate the transmitter (TX) of the device under test (DUT). In addition M8020A provides a built-in reference clock multiplier for synchronization of the BERT pattern generator with the DUT's reference clock which can carry spread spectrum clocking (SSC). On the analyzer side an equalizer to open closed eyes and a clock recovery with adjustable loop bandwidth for the analyzer is built-in.

With this high level of integration a receiver test set-up with M8020A is now much easier to connect and more robust. Set up and debug time is shortened, calibration is simpler and the frequency of recalibration is lower, resulting in more efficient use of overall test time.

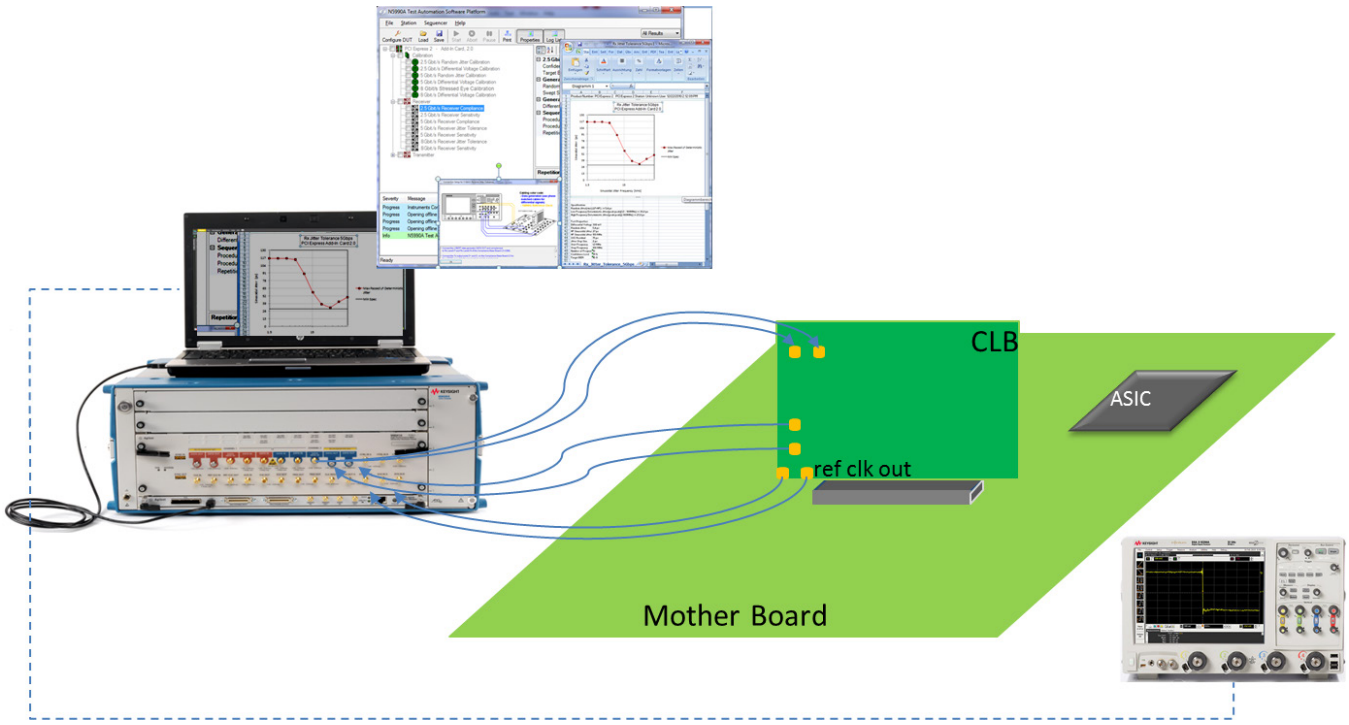


Figure 2: J-BERT M8020A streamlines complex receiver test setups. The example shows a PCIe 3 (8 GT/s) mother board RX test (CEM spec) with J-BERT M8020A connected via a compliance load board (CLB). J-BERT M8020A provides built-in de-emphasis, jitter sources, common-mode and differential mode interference (CMI, DMI), reference clock multiplier, clock recovery and continuous time linear equalizer (CTLE) – everything that is needed is built-in and calibrated.

In situ calibration for the most accurate and repeatable results

At data rates above 5 Gb/s, the influence of the channel (PC-board, cable, connectors) between transmitter (TX) and receiver (RX) is no longer negligible. The reference point for the RX specification moves to the RX input, the test set-up typically has to contain a certain channel characteristic, often an ISI channel, as well. To accurately inject a defined stress condition to the RX in situ calibration is required: at that same exact point where the receiver under test has to be connected during test, a reference load is connected instead and the generated signal is measured. This allows calibration of the test signal at that point where the specification applies by adjusting the instrument generated stress such as jitter in a way that the target signal with all its ingredients is achieved.

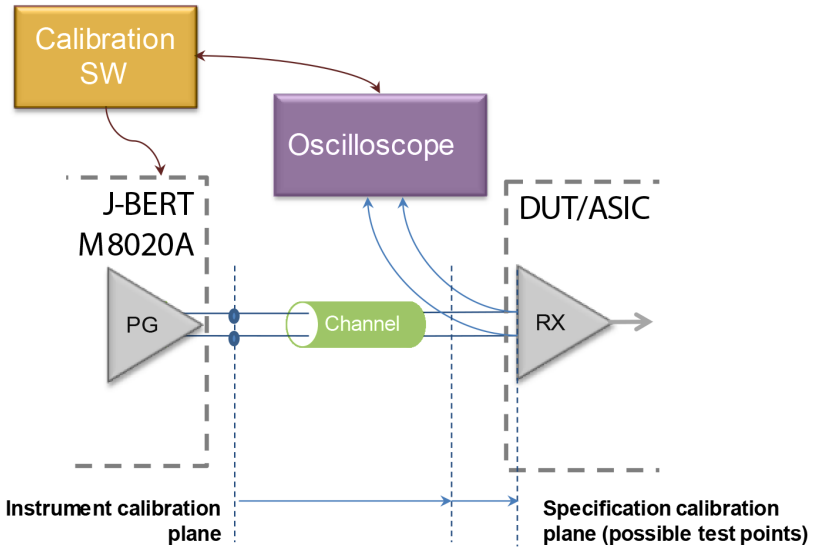


Figure 3: With increasing bit rates the calibration plane for the receiver stress conditions moves closer to the receiver inputs. J-BERT M8020A supports in situ calibration to achieve higher accuracy of the signal and stress conditions at the relevant definable test point.

Interactive link training to fasten loopback

The ever increasing data rate of computer buses and datacom interfaces results in shrinking margins and the necessity to use equalization techniques in transmitters and receivers to compensate for the lossy channels caused by inexpensive PC board material or long cables. For the latest industry standards, such as PCI Express 3 or 4, SAS 12G, and backplanes such as 100GBASE-KR4, the link partners are required to optimize the TX de-emphasis and RX equalization combination. The RX takes the active part during this procedure. In order to do so, the BERT must be capable to understand the low level protocol and to react accordingly, i.e. change its TX de-emphasis as requested. J-BERT M8020A can behave like a real link partner with its interactive link training capability, initially PCIe is supported.

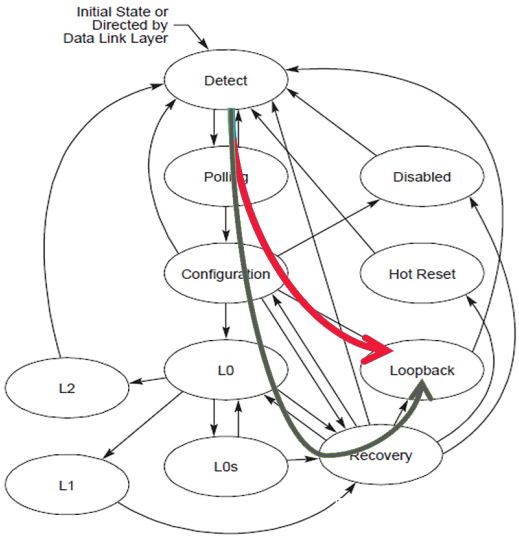


Figure 4: J-BERT M8020A can behave like a real link partner. Due to its interactive link training capability it is able to train the device into the loopback state via recovery state, as shown in this example for PCIe.

Overview J-BERT M8020A High-performance BERT

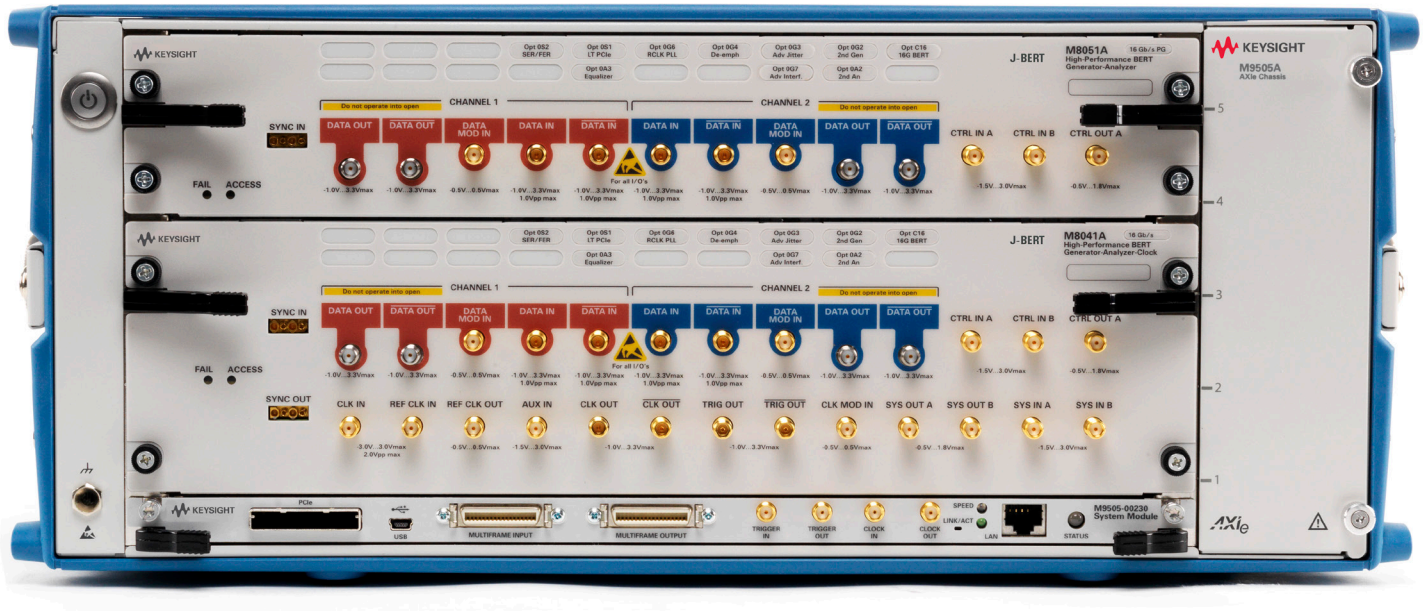


Figure 5: J-BERT M8020A high-performance BERT for accelerated receiver characterization. The configuration shows a 4 channel 16 Gb/s BERT in a 5-slot AXIe chasssis consisting of one M8041A module with two BERT channels and clock synthesizer and one M8051A extender module with two additional BERT channels.

Applications

R&D and test engineers who characterize and verify compliance of chips, devices, boards and systems with serial I/O ports up to 16 Gb/s. The M8020A can be used to test popular serial bus standards, such as PCI Express®, SATA/SAS, DisplayPort, USB Super Speed, MIPI M-PHY, SD UHS-II, Fibre Channel, QPI, memory buses, backplanes, repeaters, active optical cables, Thunderbolt, 10 GbE/SFP+, 100GbE/CFP2.

Receiver characterization and compliance test

Most multi-gigabit digital interfaces define a receiver tolerance test where the receiver must detect the incoming data bits properly while a certain amount of stress is applied. J-BERT M8020A provides calibrated and built-in jitter sources and automated jitter tolerance measurements. Users can define the modulation frequency range, the number of frequency steps, the min. and max. applied jitter, BER and confidence level and relax time. Results can be exported.

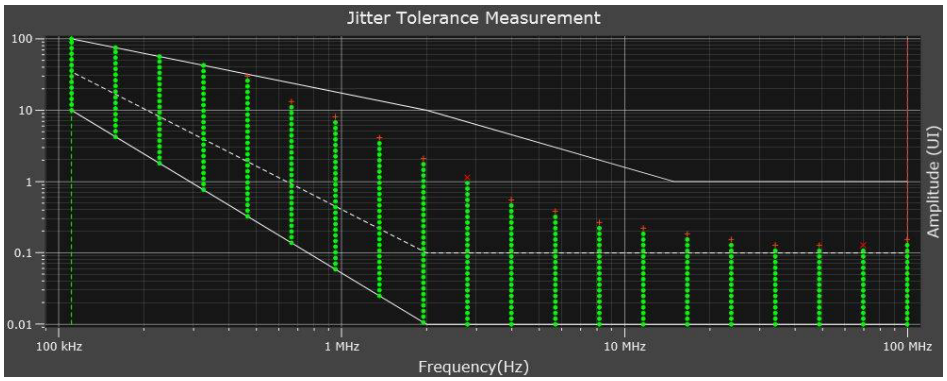


Figure 6: J-BERT M8020A provides automated jitter tolerance characterization and compliance measurements. A library of Jitter tolerance templates is available. To opimze test time, customized jitter tolance templates can be created with a graphical jitter tolerance template editor. The red dots in the result screen show where the BER level was exceeded, the green dots show where the DUT tolerated the received jitter.

Emulate de-emphasis and compensate for channel loss

Most serial interfaces that operate above 5 Gb/s use transmitters with de-emphasis to compensate for electrical signal degradations caused by printed circuit boards or cables between the transmitter and the receiver ports. R&D and test engineers who need to characterize receiver ports under realistic and worst case conditions require a pattern generator that allows to accurately emulate transmitter de-emphasis and the channel with adjustable 8-tap de-emphasis levels.

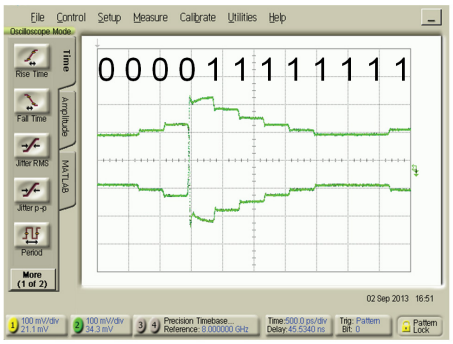


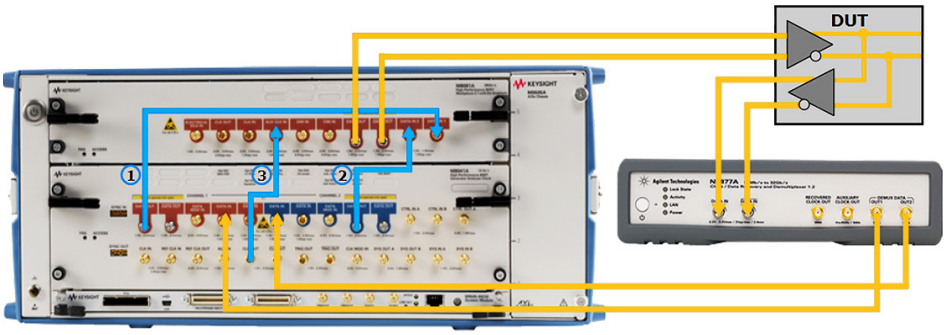
Figure 7: J-BERT M8020A provides built-in de-emphasis with up to 8 taps to emulate a transmitter de-emphasis and to compensate for channel loss. The example shows a bit sequence of eight “0“s and eight "1"s with two pre-cursors and 5 post-cursors that can be adjusted individually.

J-BERT M8020A configuration for 32 Gb/s

The J-BERT M8020A can be configured as a full 32 Gb/s BERT for accurate receiver characterization. It provides built-in jitter sources, up to 8-tap de-emphasis, and a clock recovery for full-sampling BER and jitter tolerance measurements up to 32 Gb/s. One common user interface allows controlling all parameters of the 32 Gb/s pattern generator and analyzer.

Key features of the 32 Gb/s BERT configuration:

- Excellent intrinsic jitter performance
- Calibrated jitter sources up to 1 UI eye closure for HF jitter, multi -UI LF jitter, BUJ and Clk/2 jitter
- No step increase when turning on jitter sources
- 8 tap de-emphasis with positive and negative cursors
- Superposition of level interference avoids external adders
- Clock recovery with adjustable loop bandwidth
- Add-on to 16 Gb/s BERT configuration
- Common user interface



(1) M8041A DATA OUT 1 -> M8061A DATA IN 1
(2) M8041A DATA OUT 2 -> M8061A DATA IN 2
(3) M8041A CLK OUT -> M8061A AUX CLK IN
N4877A DUMUX DATA OUT1 -> M8041A DATA IN 1
N4877A DUMUX DATA OUT2 -> M8041A DATA IN 2

Figure 8: The J-BERT M8020A can be configured as a full 32 Gb/s BERT for accurate receiver characterization. A two channel M8041A BERT can be extended with the M8061A multiplexer and the N4877A CDR/de-multiplexer to data rates up to 32 Gb/s.

User interface and measurements

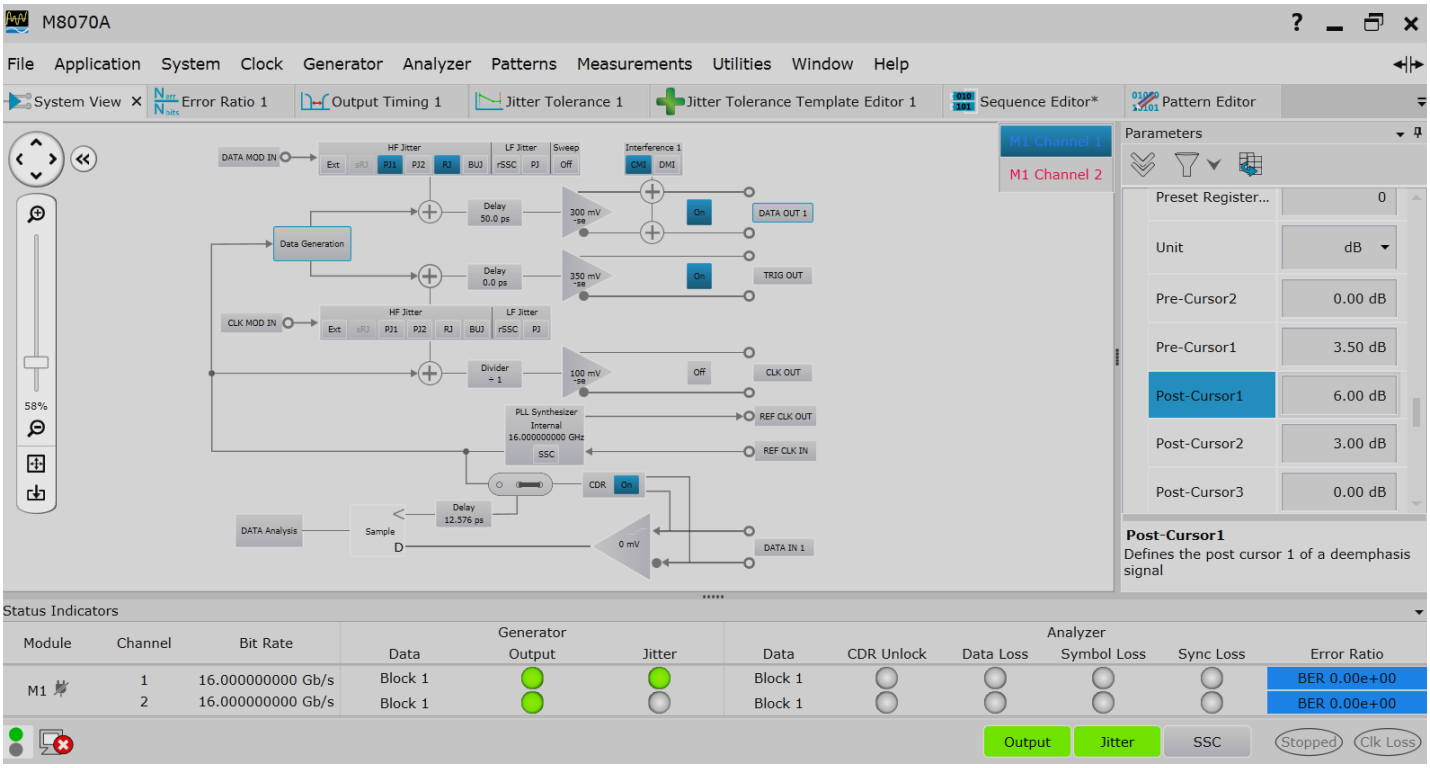


Figure 9: The graphical user interface for J-BERT M8020A offers multiple views that can be defined by the user. This example shows the system view on left side and the pattern generator data output parameters at the right.

Pattern sequencer, coding and interactive link training

To simplify test pattern creation, J-BERT M8020A provides unique tools such as an interactive link training state machine, pattern sequencer with break and branch conditions, a real-time scrambler for coded patterns, masking, symbol filtering for meaningful BER measurements for retimed loop back, a library of pre-defined patterns and loop-back sequences, and a grahical pattern editor.

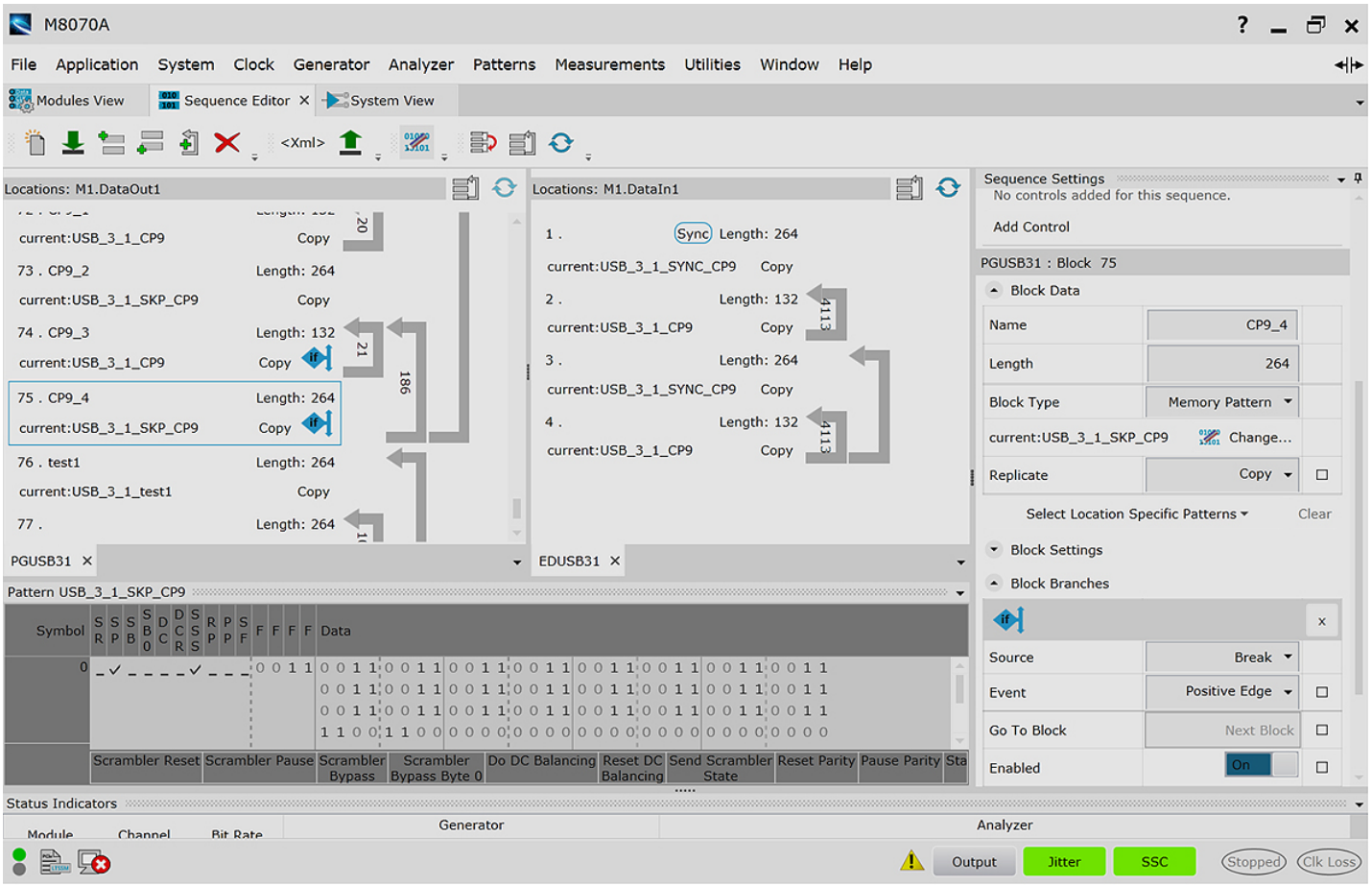


Figure 10: The J-BERT M8020A provides powerful pattern sequencing capabilities. For each pattern generator and analyzer channel a pattern seqeunce with multiple loop levels, breaks and bock controls can be defined. A library of link training sequences for popular standards is available. The example shows a USB 3.1 link training sequence.

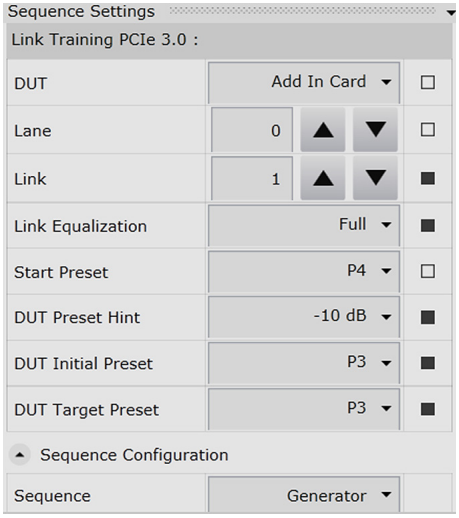


Figure 11: The interactive link training capability of J-BERT M8020A significantly reduces the effort to generate and tune a loopback sequence for your device under test. The example shows the properties you can choose for the PCIe3 link training state machine.

Accuracy and performance

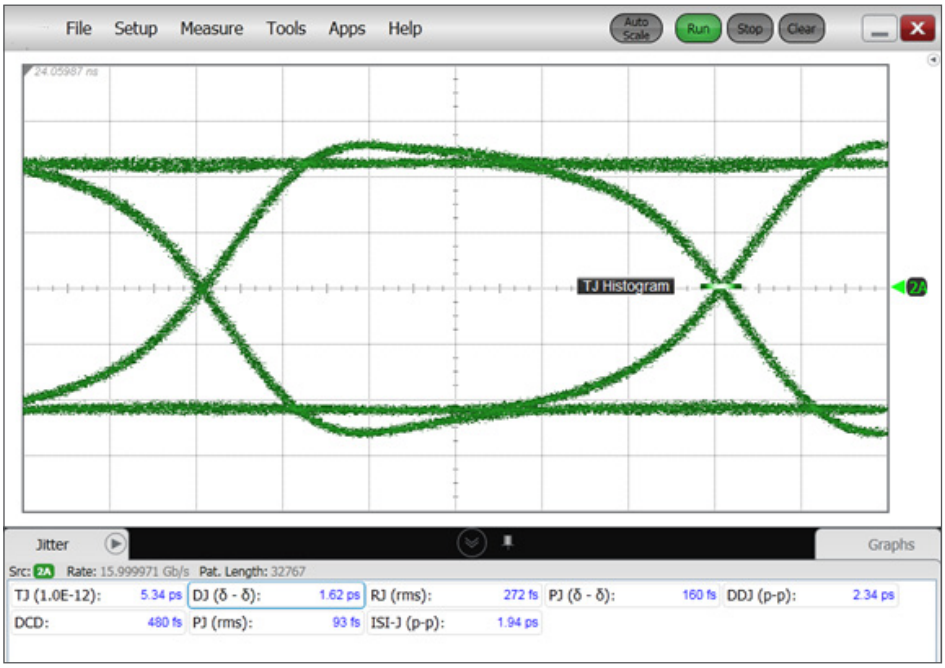


Figure 12: Clean 16.0 Gb/s output signal of J-BERT M8020A with M8041A BERT module using its internal clock source and PRBS 2 1_5-1 pattern.

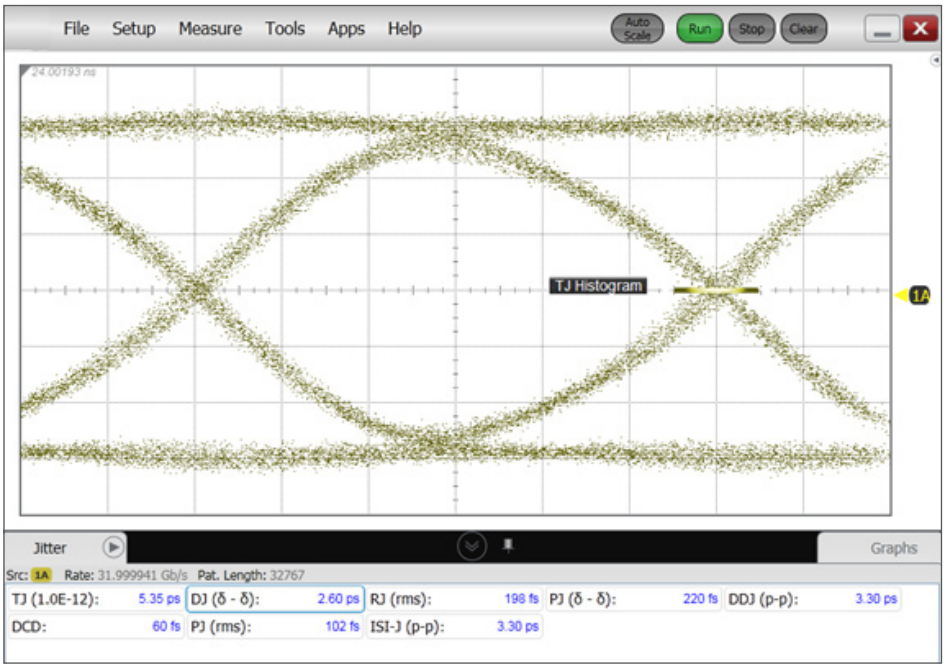


Figure 13: The 32 Gb/s output signal shows excellent intrinsic jitter. This shows the output signal of M8061A when used with M8041A BERT module and its internal clock source and PRBS 2 ^{15}-1 pattern, and the band pass filter M8061A-803 in the clock path.

Specifications for M8041A and M8051A J-BERT high-performance BERT modules

Figure 14: Front panel view of M8041A module (bottom) and M8051A (top).

Specification for M8061A

Please refer to M8061A data sheet (5991-2506EN) for specification details.

Specifications pattern generator

Data output (DATA OUT 1, DATA OUT 2)

Table 1. Data output characteristics for M8041A and M8051A.

All timing parameters are measured @0.5 V into ground		M8041A	M8051A
Data rate	256 Mb/s to 8.50 Gb/s (opt. G08 or C08), 256 Mb/s to 16.20 Gb/s (opt. G16 or C16)	x	x
Data format	NRZ		
Channels per module	1 or 2 (second channel requires opt. 0G2)		
Amplitude	50 mV to 1.2 Vpp single ended, 100 mV to 2.4 Vpp differential, 1 mV resolution; addresses LVDS, CML, low-voltage CMOS, others. See table 2 for max. output amplitude in presence of CMI or DMI		
Amplitude accuracy	5 % ± 5 mV typical (AC)[3]		
Output voltage window	-1 V to +3.0 V		
External termination voltage	-1 V to +3.0 V. For offset > 1.3 V the termination voltage should be ± 0.5 V of offset		
Transition time	15 to 20 ps typical (20%-80%)		
Crossing point	Adjustable from 30% to 70%		
Intrinsic total jitter [1]	8 ps p-p typical		
Intrinsic random jitter [2]	300 fs rms typical		
Data delay range	0 to 10 ns, resolution 100 fs		
Data delay accuracy	± 1% ± 20 mUI typical [5]		
Deskew accuracy	± 10 ps typical between data out 1 and 2 of the same module		
Electrical idle transition time	Output transitions from full swing signal to 0 V amplitude and vice versa at constant offset within 4 ns typical. Electrical idle can be controlled from sequencer. Latency is TBD.		
Termination	50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage.		
Output protection	This is an emergency shut down feature. It disables an output in case an unexpected voltage is detected. DC coupling mode: Termination range for devices connected to data out: – unbalanced 50 Ω ± 10 Ω typical – balanced 100 Ω ± 20 Ω typical Operation into open is possible for these ranges when “DC coupled“ and “balanced“ termination modes are selected: – output amplitude max. 300 mV [4] – offset 0 to 270 mV AC coupling mode: An external DC blocking capacitor is expected. If a resistive load is discovered the output will not be enabled.		
Termination modes	Balanced/unbalanced DC/AC coupling		
Connectors	3.5 mm, female		

1. At 16.2 Gb/s PRBS 2^{15}-1, BER 10^{-12}, with internal clock.
2. At 16 Gb/s and clock pattern.
3. At 256 Mb/s measured with DCA-X 86108B and clock pattern and in the middle of the eye.
4. Per output when differentially terminated into 100 Ω. Results in doubled swing when driving into open.
5. At constant temperature.

Specifications pattern generator (continued)

Data output (DATA OUT 1, DATA OUT 2) (continued)

Table 2. Data output amplitude maximum (single ended) in presence of DMI, CMI, offset voltage.

Offset ≤ 1.9 V	Offset > 1.9 V	CMI	DMI
1.2 Vpp	0.9 Vpp	disabled	disabled
0.9 Vpp	0.675 Vpp	disabled	enabled
0.9 Vpp	0.75 Vpp	enabled	disabled
0.675 Vpp	0.562 Vpp	enabled	enabled
0.8 Vpp	0.666 Vpp	enabled	enabled [1]

1. For DMI < 12.5 % of amplitude.

De-emphasis (DATA OUT)

M8020A provides built-in de-emphasis with positive and negative cursors based on a finite impulse response (FIR) filter.

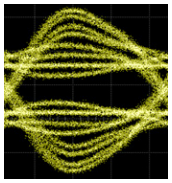
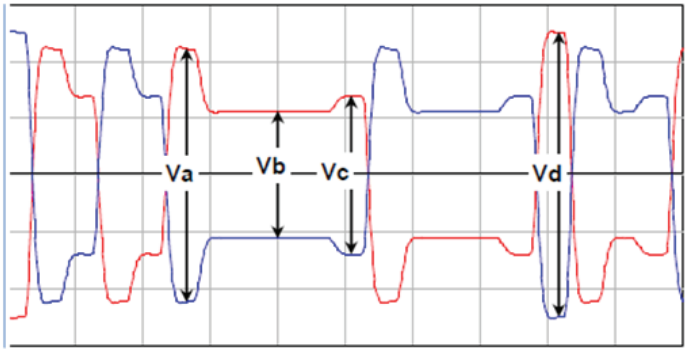


Table 3. Specifications for multi-tap de-emphasis (requires option 0G4).

		M8041A	M8051A
De-emphasis taps	8 (requires opt. 0G4) can be adjusted for each channel independently	opt. 0G4	opt. 0G4
Pre-cursor 2	± 6.0 dB		
Pre-cursor 1	± 12.0 dB		
Post-cursor 1	± 20.0 dB		
Post-cursor 2	± 12.0 dB		
Post-cursor 3	± 12.0 dB		
Post-cursor 4	± 6.0 dB		
Post-cursor 5	± 6.0 dB		
De-emphasis tap resolution	± 0.1 dB		
De-emphasis tap accuracy	± 1.0 dB [1] typical		

1. Sum of all cursors may not exceed Vpp max. The tap accuracy applies for PCIe 3 presets for pre-cursor 1 and post-cursor 1 at 8 Gb/s.



$$\text{Post-cursor 1} = 20\log_{10} Vb/Va$$
$$\text{Pe-cursor} = 20\log_{10} Vc/Vb$$
$$\text{Vpp nominal} = 20\log_{10} Vd$$

Figure 15. Definition of nominal output amplitude and de-emphasis.

Specifications pattern generator (continued)

Clock output (CLK OUT)

Table 4. Clock output specifications

		M8041A	M8051A
Frequency range	256 MHz to 8.50 GHz (opt. G08 or C08), 256 MHz to 16.20 GHz (opt. G16 or C16)	x	no clk
Frequency resolution	1 Hz		
Frequency accuracy	± 15 ppm		
Amplitude	0.1 to 1 V, 5 mV steps, single ended		
Output voltage window	-1 V to +3 V [1]		
External termination voltage	-1 V to +3.0 V		
Transition times	20 ps typical (20%-80%)		
Duty cycle	50%, accuracy ± 15%		
Clock divider	1, 2, 4, 8, 10, 16, 20, 24, 30, 32, 40, 50, 64, 66, 80. For other dividers use TRG output		
Clock modes	See table 5		
Intrinsic random jitter	300 fs rms typical at 16.2 GHz and clock divider = 1		
SSB phase noise [2]	– 85 dBc/ Hz typical at 10 kHz offset and internal clock and 10/100MHz as external reference clock. – 80 dBc/Hz with 10 kHz offset for reference clock multiplier bandwidth 0.1/2/5 MHz		
Termination	50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage.		
Connectors	3.5 mm, female		

1. If V_{term} is other than 0 V the following applies:
   High level voltage range= $2/3 * V_{term}$ - 0.95 V < HIL < V_{term} + 2 V
   Low level voltage range= $2/3 * V_{term}$ - 1 V < LOL < V_{term} + 1.95 V
2. For 8.1 to 16.2 GHz clocks.

Table 5. Clock modes (M8041A only).

Clock mode	Clock generation	Input frequency range		
		Option G08/ C08	Option G16/ C16	Option
Reference	PLL with bandwidth below 1 kHz	10/100 MHz	10/100 MHz	
Direct	No PLL	8.1 GHz to 8.5 GHz	8.1 GHz to 16.2 GHz	
Reference clock multiplier bandwidth 100 kHz	m/n PLL with loop bandwidth 100 kHz m, n = 1 to 1620	10 MHz to 8.5 GHz	10 MHz to 16.2 GHz	
Reference clock multiplying PLL with loop bandwidth 2 MHz	Integer PLL with loop bandwidth 2 MHz [1]	10 to 105 MHz	10 to 105 MHz	0G6
Reference clock multiplying PLL with loop bandwidth 5 MHz	Integer PLL with loop bandwidth 5 MHz [1]	50 to 105 MHz	50 to 105 MHz	0G6

1. Intended use with settings in Table 7 (other settings may be possible, contact factory)

Specifications pattern generator (continued)

Reference clock input (REF CLK IN)

This input on the M8041A module allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator. It also allows to use an external clock, see clock modes.

Table 6. Reference clock input specifications (M8041A only).

		M8041A	M8051A
Input amplitude	0.2 to 1.4 Vpp	x	no
Input frequency	10 MHz to 16.2 GHz, depends on clock mode and max. data rate option		
Interface	Single ended. 50 Ω nominal		
Connector	SMA, female		

Table 7. Predefined settings for reference clock multiplier (M8041A with option 0G6 only).

Ref clock input	Standard	Target data rate	Multiplier	PLL loop BW	M8041A
100 MHz	PCIe 4	16 Gb/s	160	2 MHz	0G6
100 MHz	PCIe 3	8 Gb/s	80	5 MHz	
100 MHz	PCIe 2	5 Gb/s	50	5 MHz	
100 MHz	PCIe 1	2.5 Gb/s	25	5 MHz	
26 MHz to 52 MHz	SD UHS-II	390 Mb/s to 780 Mb/s	15	2 MHz	
26 MHz to 52 MHz	SD UHS-II	780 MHz to 1.56 Gb/s	30	2 MHz	
52 MHz to 104 MHz	SD UHS-II Gen 2	1.56 Gb/s to 3.12 Gb/s	30	2 MHz	
52 MHz to 104 MHz	SD UHS-II Gen 2	3.12 Gb/s to 6.24 Gb/s	60	2 MHz	
19.2 MHz	MIPI M-PHY	1.248/ 1.4592/ 2.496/ 2.9184/ 4.992/ 5.8368 Gb/s	65/ 76/ 130/ 152/ 260/ 304	2 MHz	
26 MHz	MIPI M-PHY	1.248/ 1.456/ 2.496/ 2.912/ 4.992/ 5.824 Gb/s	48/ 56/ 96/ 112/ 192/ 224	2 MHz	
38.4 MHz	MIPI M-PHY	1.248/ 1.4592/ 2.496/ 2.9184/ 4.992/ 5.8368 Gb/s	65:2/ 38/ 65/ 76/ 130/ 152	2 MHz	
52 MHz	MIPI M-PHY	1.248/ 1.456/ 2.496/ 2.912/ 4.992/ 5.824 Gb/s	24/ 28/ 48/ 56/ 96/ 112	2 MHz	

Supplementary inputs and outputs of M8041A and M8051A

Trigger output (TRG OUT)

The trigger output can be used in different modes:

1. Divided clock, dividers: 2 to 65535
2. Sequence block trigger with adjustable pulse width and offset
3. PRBS sequence trigger with adjustable pulse width

Table 8. Trigger output specifications (M8041A only).

		M8041A	M8051A
Amplitude	0.1 to 1 Vpp single ended; 0.2 to 2 Vpp differential	x	no trg
Output voltage window	-1 to 3 V [1]		
External termination voltage	-1 to 3 V		
Interface	Differential, 50 Ω		
Connector	3.5 mm, female		

1. If V_{term} is other than 0 V the following applies:
   High level voltage range= 2/3 * V_{term} - 0.95 V < HIL < V_{term} + 2 V
   Low level voltage range= 2/3 * V_{term} – 1 V < LOL < V_{term} + 1.95 V

Reference clock output (REF CLK OUT)

Outputs a 10 MHz clock, 1 Vpp single ended into 50 Ω. M8041A only.
Connector: SMA, female.

Clock input (CLK IN)

For future use. For M8041A only. See reference clock input for direct clock mode.

Control input A and B (CTRL IN A, CTRL IN B)

Functionality of each input can be selected as: sequence trigger, error add input.

Table 9. Control input specifications (M8041A and M8051A).

		M8041A	M8051A
Input voltage	-1 V to +3 V	x	x
Termination voltage	-1 V to +3 V		
Threshold voltage	-1 V to +3 V		
Connector	SMA, female		

Control output A (CTRL OUT A)

Outputs a pulse in case of an error.

Table 10. Control output specifications (M8041A and M8051A).

		M8041A	M8051A
Amplitude [1]	0.1 to 2 V	x	x
Output voltage [1]	-0.5 to 1.75 V		
Connector	SMA, female		

1. When terminated with 50 Ω into GND. Doubles into open.

Supplementary inputs and outputs of M8041A and M8051A (continued)

Synchonization input and output (SYNC IN, SYNC OUT)

The Sync output on M8041A: clock output to synchronize multiple modules to a common clock.
The Sync input is a clock input on M8051A module to synchronize additional modules to a common clock.
A sync cable is delivered with each M8051A module by default.

System input A/B and auxillary input (AUX IN)

Control inputs to synchronize events for the pattern sequencer.
Auxiliary input: for future use. For M8041A only.

Table 11. System input and auxiliary input specifications (M8041A only)

		M8041A	M8051A
Input voltage	-1 V to +3 V	x	no
Termination voltage	-1 V to +3 V		
Threshold voltage	-1 V to +3 V		
Connector	SMA, female		

System output A/B (SYS OUT A/B)

Control outputs to synchronize events for the pattern sequencer.

Table 12. System output specifications (M8041A only).

		M8041A	M8051A
Amplitude [1]	0.1 to 2 V	x	no
Output voltage [1]	-0.5 to 1.75 V		
Connector	SMA, female		

1. When terminated with 50 Ω into GND. Doubles into open.

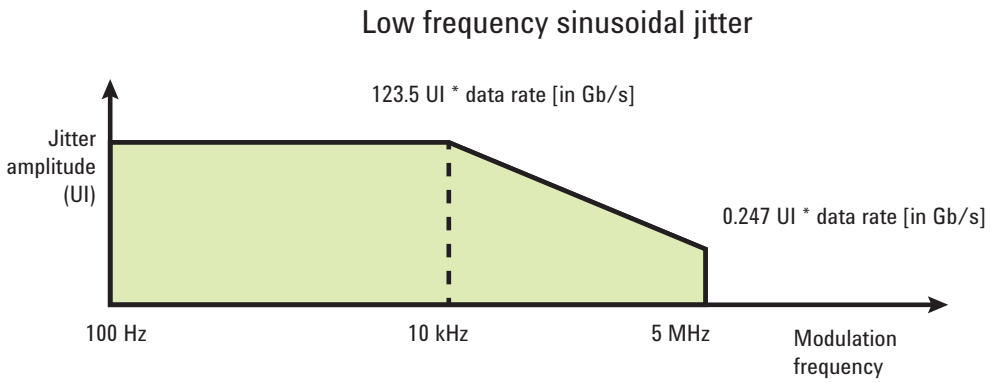
Jitter tolerance test specifications

M8020A provides built-in calibrated jitter sources designed to cover receiver test needs for most of the popular multi-gigabit standards such as: PCIe, USB, MIPI, SATA, DisplayPort, CPU frontside buses, CEI, 10GbE, 100GbE, SFP+, QSFP, CFP2/4, etc. M8020A provides automated jitter tolerance measurements. A library of pre-defined compliance curves is provided.

For 32 Gb/s setups using M8061A, the jitter sources of M8041A/51A can be used. The M8061A multiplexer is transparent to jitter. The ranges specified in table 13 to 17 refer to the datarate at the output of M8061A when the mux configuration is selected.

Table 13. Specifications for low frequency sinusoidal jitter (requires option 0G3 advanced jitter sources).

			M8041A	M8051A
Low frequency sinusoidal jitter (LF SJ) (generated by IQ modulator)	Amplitude range	0 to 1000 UI. For frequencies between 10 kHz and 5 MHz see figure 16 for maximum LF SJ. For frequencies between 10 kHz and 5 MHz the max. jitter amplitude = $\frac{1.235\ ns * 10^{-3} * data\ rate}{modulation\ frequency}$	opt. 0G3	opt. 0G3
	Frequency	100 Hz to 5 MHz		
	Jitter amplitude accuracy	± 2 % ± 1 ps typical		
	Adjustable	For each data channel independently, same LF SJ for clock and trigger		



Data rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency 5 MHz
256.0 Mb/s to 506.25 Mb/s	31.6 to 62.5 UI	0.0632 to 0.125 UI
506.25 Mb/s to 1.0125 Gb/s	62.5 to 125 UI	0.125 to 0.25 UI
1.0125 Gb/s to 2.025 Gb/s	125 to 250 UI	0.25 to 0.5 UI
2.025 Gb/s to 4.05 Gb/s	250 to 500 UI	0.5 to 1 UI
4.05 Gb/s to 8.1 Gb/s	500 to 1000 UI	1 to 2 UI
8.1 Gb/s to 16.2 Gb/s	1000 to 2000 UI	2 to 4 UI

Figure 16. Low frequency sinusoidal jitter maximum depends on data rate and modulation frequency.

Jitter tolerance test specifications (continued)

Table 14. Specifications for high frequency periodic jitter, random jitter, spectrally distributed random jitter, bounded uncorrelated jitter, Clock/2 jitter (requires option 0G3 advanced jitter sources).

			M8041A	M8051A
High frequency jitter (generated by delay line)	Range	1 UI p-p for data rates > 1 Gb/s note: this is max sum of RJ, HF-PJ1 and HF-PJ, spectral RJ, external delay modulation and BUJ.	opt. 0G3	opt. 0G3
High frequency periodic jitter (HF PJ1 and HF PJ2)	Range	See HF jitter above [1]	opt. 0G3	opt. 0G3
	Frequency	1 kHz to 500 MHz. For data rates < 4 Gb/s the max modulation frequency is data rate / 8. Two tone possible. Sweep.		
	Jitter amplitude accuracy	± 3 ps ± 10 % typical		
	Adjustable	For each channel independently		
Random jitter (RJ)	Range	0 to 72 mUI rms (1 UI p-p max.) [1]	opt. 0G3	opt. 0G3
	Jitter amplitude accuracy	± 300 fs ± 10 % typical		
	Filters	High-pass: 10 MHz, Low-pass: 100 MHz, Low pass: 500 MHz (for data rates ≥ 3.75 Gb/s) Off (1 GHz bandwidth, for data rates ≥ 7.5 Gb/s)		
	Adjustable	For each channel independently		
Spectrally distributed RJ according to PCIe 2 (sRJ) [2]	Range	0 to 72 mUI rms (1 UI p-p), [1]	opt. 0G3	opt. 0G3
	Frequency	LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz		
	Jitter amplitude accuracy	± 300 fs ± 10 % typical		
	Adjustable	For each channel independently		
Bounded uncorrelated jitter (BUJ)	Range	See HF jitter above[1]	opt. 0G3	opt. 0G3
	PRBS polynomials	2^n -1, n = 7,8,9,10,11,15,23,31		
	Filters	50/100/200 MHz low pass 3rd order		
	Jitter amplitude accuracy	± 5 ps ± 10% typical for settings shown in table 15		
	Adjustable	For each channel independently		
Clock/2 jitter	Range	± 20 ps or ± 0.1 UI typical (whatever is less). Note: this means that first eye can be up to 20 ps longer or shorter than subsequent eye.	opt. 0G3	opt. 0G3
	Jitter amplitude accuracy	± 3 ps typical		
	Adjustable	For each channel independently		

1. 1 UI is the maximum sum of RJ, HF-PJ1 and HF-PJ2, spectral RJ, external delay modulation and BUJ.
2. Spectrally distributed random jitter is mutually exclusive with RJ and BUJ.

Table 15. BUJ accuracy applies for these BUJ settings.

BUJ calibration settings [1]	Rate for PRBS generator	PRBS polynomial	Low pass filter
CEI 6G	1.25 Gb/s	PRBS 2^9-1	100 MHz
CEI 11G	2.5 Gb/s	PRBS 2^{11}-1	200 MHz
Gaussian	2.5 Gb/s	PRBS 2^{31}-1	100 MHz

1. Other settings are not calibrated and do not necessarily generate the desired jitter historgrams for all data rates of the PRBS generator.

Jitter tolerance test specifications (continued)

Table 16. Specifications for Spread Spectrum Clocking (SSC) (requires opt. 0G3: advanced jitter sources).

			M8041A	M8051A
SSC (Spread Spectrum Clock)	Range	0 to 10,000 ppm (0 to 1%) peak-peak. Select center-spread, up-spread, and down-spread.	opt. 0G3	na
	Frequency	30 kHz to 100 kHz		
	Modulation	Triangular and arbitrary modulation		
	SSC amplitude accuracy	± 0.025 % typical		
	Outputs	Can be turned on/off together for CLK OUT, DATA OUT 1, DATA OUT 2, TRG OUT		
Residual SSC (@ PCIe2)	Range	0 to 100 ps	opt. 0G3	opt. 0G3
	Frequency	10 to 100 kHz		
	Outputs	Can be turned on/off independently for DATA OUT 1, DATA OUT 2		

Table 17. Specifications for external jitter modulation (DATA MOD IN 1 and 2, CLK MOD IN).
M8041A allows individual jitter injection for data 1, data 2 and clock. M8051A for data 1 and data 2. The option 0G3 is not needed.

			M8041A	M8051A
External jitter - data modulation input 1 and 2	Description	Input for delay modulation for each DATA OUT individually.	x	x
	Range	Up to 1 UI [1], 0.8 Vpp max		
	Frequency	Up to 1 GHz		
External jitter - clock modulation input	Description	Input for delay modulation for the TRG OUT and CLK OUT. Affects both.	x	na
	Range	Up to 1 UI , 0.8 Vpp max		
	Frequency	Up to 1 GHz		
Gain		1UI / 0.725 V ± 5%	x	x
Linearity		50 mUI	x	x
Connectors		SMA, female		

1. 1 UI is the maximum sum of RJ, HF-PJ1 and HF-PJ2, spectral RJ, external delay modulation and BUJ.

Jitter tolerance test specifications (continued)

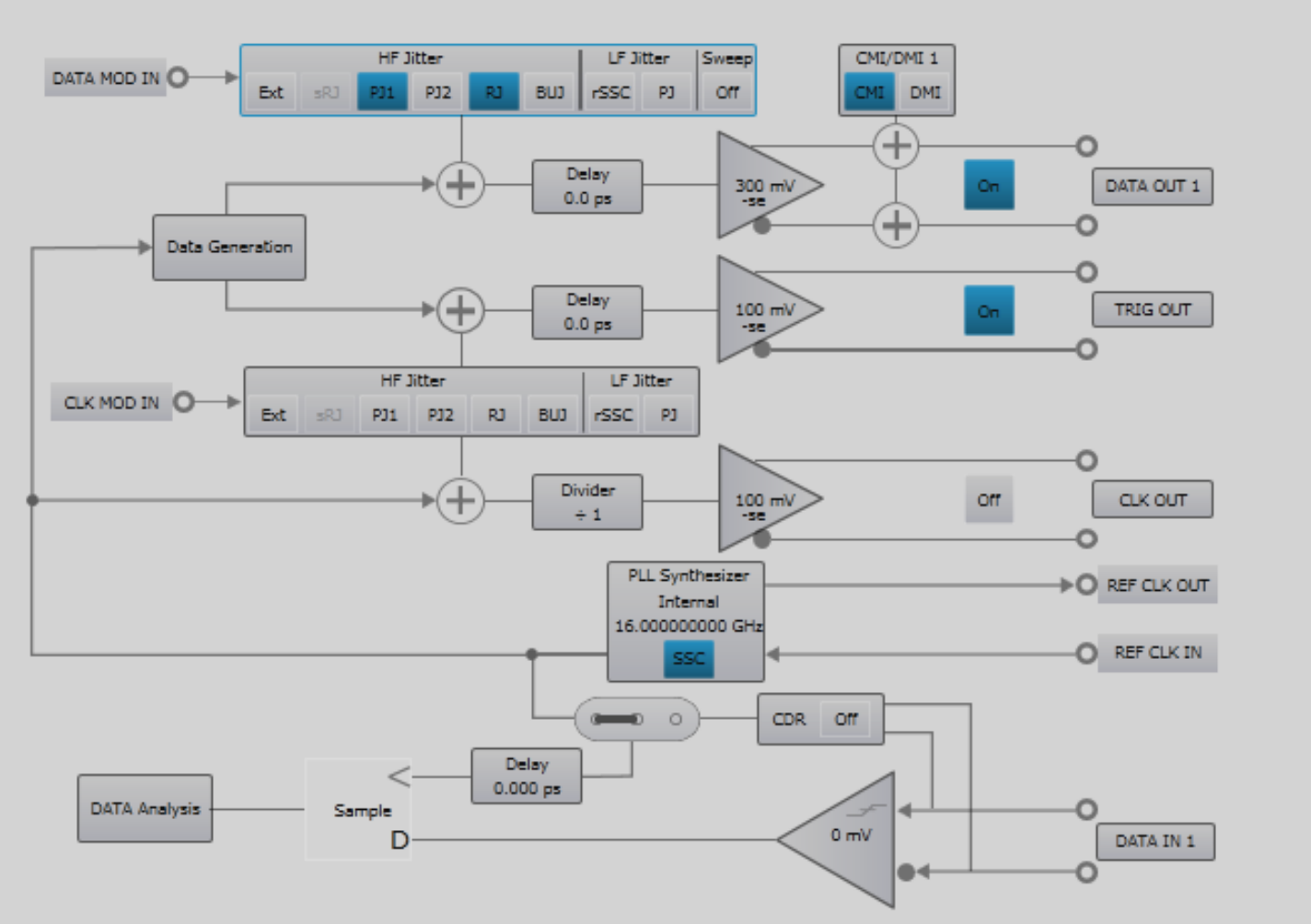


Figure 17. J-BERT M8020A system view for 1 channel.

Jitter tolerance test specifications (continued)

ISI channels

External ISI channels are available to emulate channel loss. Keysight offers dedicated compliant ISI channels for DisplayPort, PCIe3 (base spec) and SATA. M8048A is offererd in addition.
For detailed specifications see M8048A data sheet.

M8041A-001 ISI Channels provides four short traces:
7.7”(196 mm), 9.4” (240 mm), 11.12 “(282 mm), 12.8”(324 mm)
M8041A.002 ISI Channels provides four long traces:
14.8” (366 mm), 16.1” (408 mm), 24.4” (620 mm), 34.4”(874 mm)

Level interference injection

Common mode and differential mode level interference can be generated internally to test common mode rejection of a receiver and vertical eye closure tolerance. Simultaneous injection of CMI and DMI is possible. In 32 Gb/s configurations with M8061A, external sources for M8061A are required. See M8061A data sheet for details on built-in level interference superposition and gain adjust parameters.

Table 18. Specifications for sinusoidal level interference (CMI, DMI) (requires option 0G7).

			M8041A	M8051A
Differential mode interference (DMI)	Amplitude [2]	Max. 30% of output amplitude [1]	opt 0G7	opt 0G7
	Amplitude accuracy	±10 mV ±10% typ		
Common mode interference (CMI)	Amplitude [2, 3]	Up to 320 mV [1]		
	Amplitude accuracy	±10 mV ±10% typ		
Modulation frequency	Ranges	LF: 10 MHz to 1 GHz, sinusoidal only HF: 1 GHz to 6 GHz, sinusoidal only		
Simultaneous injection of CMI and DMI		Yes. HF modulation cannot be used simultaneously for CMI and DMI. LF modulation cannot be used simultaneously for CMI and DMI. See figure below.		

1. The maximum output amplitude decreases when CMI or DMI is enabled. See table 2.
2. For each channel independently.
3. Up to 5 GHz.

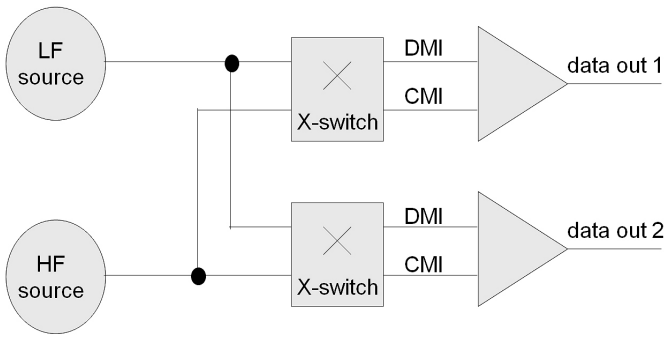


Figure 18: M8020A provides calibrated level interference sources for simultaneous injection of CMI (common mode interference) and DMI (differential mode interference).

Pattern, sequencer and interactive link training

Table 19. Specifications for pattern, sequencer and link training.

		M8041A	M8051A	M8061A
PRBS [1]	2^n-1, n= 7, 10, 11, 15, 23, 23p [3], 31	x	x	x
PRBS	2^n, n = 7, 10, 11, 13, 15, 23			
Mark density	Mark density: PRBS 1/8 to 7/8			
Zero substitution	Yes			
Export/Import	Patterns from N4900 series can be imported			
Pattern library	Yes			
User definable memory	2 Gbit/channel [4]			
Interactive link training	Link training state machine (LTSSM) for PCIe 3 [4] to achieve loopback state via recovery with or without link training. Is suitable for testing downstream and upstream ports according to PCI Express Architecture PHY Test Specification. Supports the following tests: 2.3 Add-in Card Transmitter Initial Tx EQ Test for 8 GT/s 2.4 Add-in Card Transmitter Link Equalization Response Test for 8 GT/s 2.7 System Board Transmitter Link equalization Response Test for 8 GT/s 2.10 Add-in Card Receiver Link Equalization Test for 8 GT/s 2.11 System Board Receiver Link Equalization Test for 8 GT/s – The LTSSM reports to a log file: states, de-emphasis requests by DUT – Supported channels: 1, 2 [2]	opt. 0S1	na	no
Coding	8B/10B, 128B/130B, 128B/132B, binary, hex	x	x	no
Scrambler	PCIe, USB, SATA	x	x	no
Vector/sequence granularity	64/80/130/132 bit	x	x	* 2
Pattern capture	Yes [2]	x	x	na
Pattern sequencer	3 counted loop levels, 1 infinite loop, # of blocks: 500			

1. Note: polarity is inverted compared to ParBERT and J-BERT N4903A/B and N49xx models.
2. For availability: contact factory. Free software update.
3. Modified compliance pattern for PCIe3.
4. Requires M8070A software revision 1.5.0.0 or later. Free upgrade (interactive link training requires option 051).

Specifications analyzer (error detector)

Each M8041A/51A analyzer channel includes a clock recovery.
For the following functions a separate module option is required:

- Equalizer CTLE option (option 0A3 for M8041A and M8051A)
- SER/FER analysis (option 0S2 is offered for M8041A only, but applies for all analyzers channels in the same clock group): this option provides handling of 8B/10B coded, 128B/130B coded and 128B/132B coded patterns. 8B/10B coded patterns support automatic handling of running disparity changes, scrambling/descrambling and up to 4 filler primitives consisting of up to 4 symbols each. No dead time while filtering filler symbols. Supports changes of length of 128B/130B and 128B/132B coded Skip Ordered Sets for PCIe und USB 3.1.
- For 32 Gb/s setups the N4877A-232 CDR and Demultiplexer is required to use the M8020A analysis functions. Please refer to the N4877A data sheet for details on the 32Gb/s input specifications. All parameters of the N4877A can be controlled via the M8070A system software when the "mux and demux" configuration is selected (requires M8070A software revision 1.5.0.0.or later). The CTLE and SER/FER analysis are not available for 32 Gb/s configurations with M8061A and N4877A.

Table 20. Specifications for analyzer / error detector (Option C08 or C16).

		M8041A	M8051A
Data rate	256 Mb/s to 8.50 Gb/s (opt. C08), 256 Mb/s to 16.20 Gb/s (opt. C16)	x	x
Channels per module	1 or 2 (opt. 0A2)		
Data format	NRZ, single ended and differential		
Input sensitivity [1]	50 mV typical @ normal sensitivity mode[4] 40 mV typical @ high sensitivity mode[4]		
Input voltage window	-1.0 V to + 3.3 V		
Maximum voltage window	1.0 Vpp single ended @ normal sensitivity mode 0.50 Vpp single ended @ high-sensitivity mode		
Termination voltage	-1.0 V to + 3.3 V [3]		
Timing resolution	1 mUI		
Input bandwidth	17.5 GHz typical		
CTLE	Yes. Four presets are available: PCIe 3.0 @ 8 Gb/s: -6.0 dB, - 9 dB, - 12 dB USB 3.0 @ 5 Gb/s	opt. 0A3	opt. 0A3
Clock data recovery	Yes for each input channel. See table 21 for more details.	x	x
Sampling point	Manual and automatic. Finds optimum voltage threshold and delay of the sampling point. Delay accuracy ±30 mUI		
Decision threshold range	-1.0 V to + 3.3 V in 1 mV steps. Must be within ± 0.5 V range from common mode voltage. Threshold accuracy ±25 mV		
Phase margin	1 UI - 16 ps typical for PRBS 2^{15}-1 1 UI - 7 ps typical for clock pattern		
Interface	Differential: 100 Ω, single ended: 50 Ω, DC coupled	x	x
Data input connectors	3.5 mm, female		

1. Measured with PRBS 2^{31}-1 at 16 Gb/s, AC coupling mode, BER of 10^{-12}, CTLE disabled.
2. For availability please contact factory.
3. Termination voltage must be within a window of DC common mode voltage ± 1.7 V.
4. Eye height measured at input of reference cable M8041A-801 with DCA-X module 86117A. Applies for single ended and differential input signals.

Specifications analyzer (error detector) (continued)

Table 21. Specifications for clock recovery.

		Condition	M8041A	M8051A
CDR data rate range	1.0125 to 16.2 Gb/s		x	x
Selectable loop type	1st and 2nd order PLL - see figure below for description			
Tunable loop bandwidth	102 kHz to 20 MHz depends on data rate as shown in figure below.			
	Data rate/ 10000 to data rate/ 500 [2,3]	Data rate from 1.0125 Gb/s to < 8.1 Gb/s, transition density of 50 %		
	Data rate/ 10000 to data rate/ 660 [2,3]	Data rate > 8.1 Gb/s, transition density of 50%		
Loop bandwidth accuracy	± 20% typical	1 MHz < loop BW < data rate/ 900, transition density of 50% and peaking ≤ 2 dB		
Tunable peaking range	0.. 3 dB @loop BW ≤ data rate/ 900 0.. 1 dB @loop BW > data rate/ 900	With type 2 second order loop selected		
Transition density compensation	The user can set the expected transition density and the loop compensates the loop bandwidth accordingly			
Tracking range (maximum frequency deviation)	Frequency deviation [ppm] = ±(9000 – 500 * data rate [Gb/s]	With type 2 selected and loop BW ≥ data rate / 800		
CDR freeze	After 256 consecutive bits without transition the CDR goes automatically into a freeze state. At every transition the CDR recovers from the freeze state.	If CDR is enabled		

First order PLL (type 1)

- A type 1 is defined by bandwidth. No peaking.
- JTF bandwidth = OJTF bandwith.
- Used by some communication standards

Second order PLL (type 2)

- This type 2 is defined by JTF loop bandwidth and peaking.
- JTF bandwidth > OJTF bandwidth.
- Used by some computing standards.

Figure 19: Each M8041A/51A analyzer has a built-in clock recovery. Choose between first and second order PLL.

Specifications analyzer (error detector)(continued)

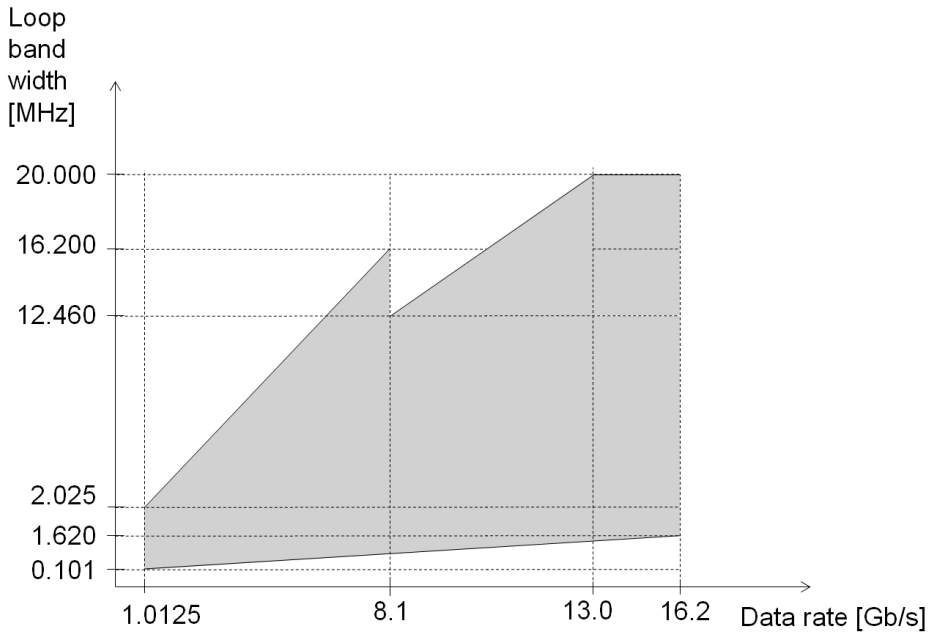


Figure 20: CDR loop bandwidth range for a transition density of 50%

Table 22. Measurement capabilities (Option C08 or C16).

		M8041A	M8051A	M8061A
BER	Accumulation and instant	x	x	x
BERT Scan with RJ, DJ separation	Yes, up to 16.2 Gb/s and PRBS 2^{31}-1	x	x	no
Jitter tolerance	Yes	x	x	x
Eye contour	Yes [1]	x	x	no
Quick eye diagram	Yes [1]			
Output level and Q factor	Yes [1]			
Bit recovery mode	Yes [1]	x	x	x
Symbol/Frame error rate	8B/10B, 128B/130B, 128B/132B [2] coded and retimed patterns	opt. OS2	na	no
Filtering of filler symbols	Automatic removal of filler symbols. See also the description above.			
Counters	8B/10B: compared symbols, errored symbols, illegal symbols, filler symbols, wrong disparity, frames, errored frames 128B/130B: blocks, errored blocks, illegal sync headers, filler symbols, modified filler symbols 128B/132B [2]: blocks, errored blocks, illegal sync headers, filler symbols, modified filler symbols, corrected sync headers			

1. For availability: contact factory. Free software update.
2. 128B/132B SER/FER, filler symbol removal and counters are supported for data rates from 9 to 11 Gb/s (USB 3.1). Requires software revision 1.5.0.0 or later.

User interface and remote control

The M8070A system software for the M8000 Series of BER Test Solutions is required to control M8041A, M8051A and M8061A.

Table 23. User interface and remote control interface.

System software	M8070A
Software licensing	Offline version does not require a license. For controlling the hardware you can choose between a transportable, perpetual license (M8070A-0TP) and a network, perpetual license (M8070A-0NP) . The network license is only recommended when using multiple M8020A setups within one company. When ordering M8020A-BU1 the M8070A-0TP license will be pre-installed on the embedded controller.
Controller requirements	Embedded PC: Choose M8020A-BU1 for a pre-installed embedded controller M9536A including pre-installation of M8070A software and module licenses. Otherwise: M9536A 1-slot AXIe embedded controller, choose options for Windows 7 or 8, 8 or 16 GB RAM, USB External PC: USB connection recommended between external PC and AXIe chassis. Minimum of 8 GB RAM recommended. For PCIe connectivity please refer to list of tested PCs for AXIe Technical Note, pub no. 5990-7632EN
Operating system	Microsoft Windows 7 (64 bit) SP1, Windows 8 (64 bit), Windows 8.1 (64 bit)
Controller connectivity with AXIe chassis	USB 2.0 (Mini-B) recommended, PCIe 2.0/8x (only for highest data throughput and desktop PC)
Programming language	SCPI. Not compatible with N4900 series and ParBERT 81250A
Remote control interface	Desktop or Laptop PC: LAN M9536A: LAN
Save/Recall	Yes
Export of measurement results	Jitter tolerance results as *.csv file
Display resolution	Minimum requirement 1024 x 768
Scripting interface	The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as other test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device.
Software pre-requisites	Microsoft Win 7 SP1 or 8 / 8.1, Keysight IO library rev. 16.3
Software download	See www.keysight.com/find/m8020a for latest version

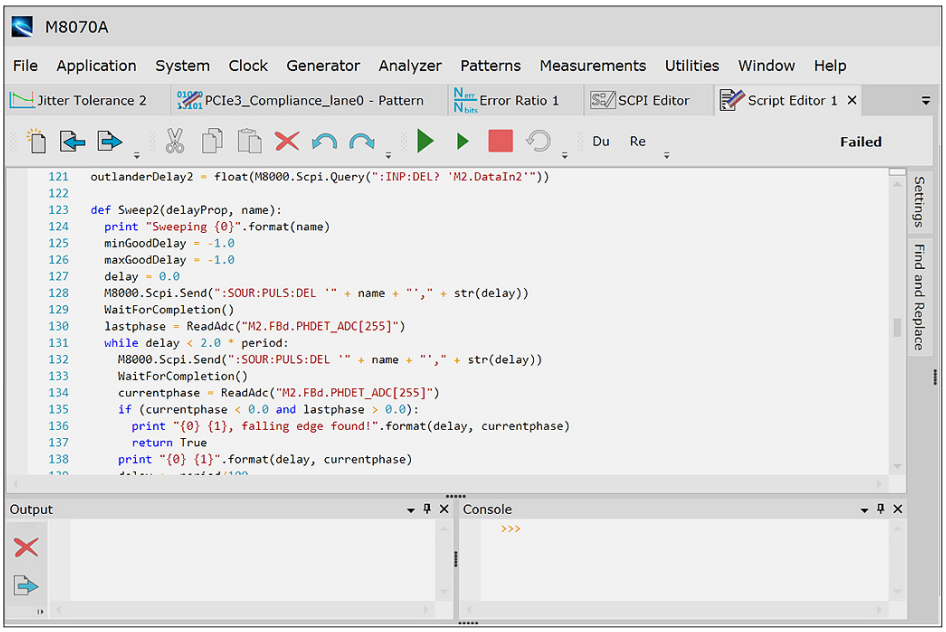


Figure 21: The built-in scripting engine of J-BERT M8020A allows to communicate with the DUT or other instruments. The scripting language is Iron Python.

General characteristics and physical dimensions

Table 24. General characteristics for M8041A and M8051A modules.

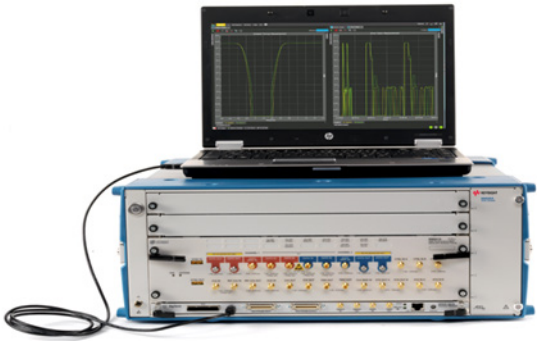
	M8041A	M8051A
Operating temperature	5 °C to 40 °C (-41 °F to + 104 °F)	
Storage temperature	-40 °C to +70 °C (modules) (-40 °F to + 158 °F)	
Operating humidity	15% to 95% relative humidity at 40°C (non-condensing)	
Storage humidity	24% to 90% relative humidity at 65°C (non-condensing)	
Power requirements (module only)	350 W	250 W
Physical dimensions for modules (W x H x D)	3- slot AXIe module: 351 x 92 x 315 mm (13.8 x 3.6 x 12.4 inch)	2-slot AXIe module: 351 x 61 x 315 mm (13.8 x 2.4 x 12.4 inch)
Physical dimensions for M8020A-BU1/-BU2 (W x H x D)	Installed in 5-slot AXIe chassis: 463 x 194 x 446 mm (18.2 x 7.6 x 17.6 inch)	
Weight net	M8041A module: 6.6 kg (14.6 lb) With M8020A-BU1: 24 kg (53 lb) With M8020A-BU2: 19.9 kg (43.9 lb)	M8051A module: 5.0 kg (11.0 lb) In bundle with M8041A and in a 5-slot chassis: 24.9 kg (54.9 lb)
Weight shipping	With M8020A-BU1: 37 kg (82 lb) With M8020A-BU2: 32.5 kg (71.7 lb)	N/A
Recommended recalibration period	1 year	
Warranty period	3 years return to Keysight	
Warm-up time	30 minutes	
Cooling requirements	Slot airflow direction is from right to left. When operating the M8041A/51A choose a location that provides at least 50 mm of clearance at each side. See also start-up guide for M9505A chassis.	
EMC	IEC 61326-1	
Safety	IEC 61010-1	
Quality management	ISO 9001, 14001	

Specification assumptions

The specifications in this document describe the instruments' warranted performance. Preliminary values are written in italic. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50 Ω to GND. All M8041A and M8051A specifications if not otherwise stated are valid using the recommended cable pair M8041A-801 (2.92 mm, 0.85 m, matched pair).

Ordering instructions

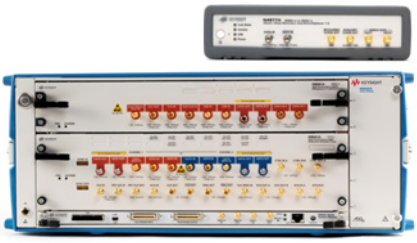
Please refer to M8020A configuration guide for ordering details.



M8020A-BU2
16 Gb/s High-performance BERT, 1-2 channel
with external PC

M8020A-BU1
with embedded PC

16 Gb/s High-performance BERT, 3-4 channel
(external PC not shown)



32 Gb/s High-performance BERT, 1 channel
(external PC not shown) with N4877A CDR / Demux

Figure 22: Overview of possible J-BERT M8020A configurations.

Default accessories included with shipment:

M8041A module: eight 50 Ω terminations, commercial calibration report (“UK6”), certificate of calibration, ESD protection kit.
M8051A module: four 50 Ω terminations, clock synchronization cable (M8051A-801), commercial calibration report (“UK6”), certificate of calibration
M8061A module: see M8061A data sheet
M8020A-BU1: M9505A AXIe chassis with embedded controller, USB cable, getting started guide, AXIe filler panel, power cord
M8020A-BU2: M9505A AXIe chassis, USB cable, getting started guide, AXIe filler panel, power cord
M8070A: CD-ROM with M8070A system software

Recommended accessories:

Matched cable pair, 2.92 mm (m) to 2.92 mm (m), 0.85 m (recommended for each data output of M8041A/51A. This 2.92 mm cable is compatible with 3.5 mm front panel connectors of M8041A/51A.)	M8041A-801
Bandpass filter 11.4 to 15.6 GHz, SMA (for use with M8061A in clock path to minimize intrinsic RJ of M8061A for data rate of 25.78 Gb/s)	M8061A-802
Bandpass filter 11.1 to 17.5 GHz, SMA (for use with M8061A in clock path to minimize intrinsic RJ of M8061A for data rates from 25.0 to 32.0 Gb/s)	M8061A-803
Cable kit for connecting M8061A with M8020A, 3x 3.5 mm, 0.6 m	M8061A-804
DC block, 26 GHz, 3.5 mm	N9398C
ISI channels, four short traces	M8048A-001
ISI channels, four long traces	M8048A-002
Short matched cable pair, SMA (m) to SMA (m) for cascading M8048A ISI channels	M8048A-801
Four SMA cables, unmatched	15442A
Rack-mount kit for AXIe 5-slot chassis M9505A	Y1226A

Test automation software with support of M8020A

Test automation software for PCIe receiver test	N5990A-101
Test automation software for USB receiver test	N5990A-102
Test automation software for SATA receiver test	N5990A-103
PCIe link training suite	N5990A-301
Test automation software, core	N5990A-010

Warranty, calibration and productivity services:

Extended 5 year warranty Return-to-Keysight	R1280 (R-51B-001-5Z)
Calibration services (3 and 5 years)	R1282
Productivity assistance	R1380-M8000

Related Keysight literature

Data sheets and configuration guides:

M8048A ISI Channels Data Sheet	5991-3548EN
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